“ Scan Construction and Validation of Channel and Rectilinear Designs ”

Major Project Report

Submitted in Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN

By

Ankit Dhama
19MECV03

Department of Electronics and Communication Engineering,
Institute of Technology,
Nirma University,
Ahmedabad 382 481
May 2021

CERTIFICATE

This is to certify that the Major Project Report entitled **"**Scan Construction and Validation of Channel and Rectilinear Designs**"** submitted by **Mr. Ankit Kumar Dhama (19MECV03)** towards the partial fulfillment of the requirements for the award of degree in Master of Technology in the field of VLSI Design of Nirma University is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

Date: May 2021

Dr. Vaishali Dhare (Internal Guide)
Assistant Professor
Electronics and Communication
Engineering Department
Institute of Technology
Nirma university, Ahmedabad

Dr. Usha Mehta
PG-Coordinator (M. Tech. VLSI Design)
Electronics and Communication
Engineering Department
Institute of Technology,
Nirma University, Ahmedabad

Dr. Dhaval Pujara
Head of Department
Electronics and Communication
Engineering Department
Institute of Technology
Nirma university, Ahmedabad

Dr. R N Patel
Director
Institute of Technology,
Nirma University, Ahmedabad

Undertaking for Originality of the Work

I, Ankit Kumar Dhama, Roll No. 19MECV03 give undertaking that the Major Project entitled "Scan Construction and Validation of Channel and Rectilinear Designs" submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in VSLI Design of Nirma University, Ahmedabad, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any other published work or any project report elsewhere; it will result in severe disciplinary action.

Signature of Student Date: Ankit Dhama, May 2021

Place: Ahmedabad

Acknowledgement

I would like to express a deep sense of gratitude and wholehearted thanks to my project mentor **Maithri Dinesh** and my manager **Mr.Rajesh Uppuluri** in order to guide me throughout the way. It was his keen interest, encouragement and full cooperation that have made it possible for me to move ahead with the work.

I express my profound gratitude to the **Dr. Vaishali Dhare**, Electronics and Communication Engineering Department, for allowing me to proceed with the Major Project, for her valuable guidance, constant encouragement and kind help at different stages for the execution of this dissertation work.

My heartfelt thanks to my guide for taking time and helping me throughout this project. She has been a constant source of encouragement and motivation without which the project might not have been completed on time. I am very grateful for her guidance.

Ankit Kumar Dhama
19MECV03

Abstract

According to Moore's law number of transistors placed in an integrated circuit (IC) or chip doubles approximately every two years hence chances of occurring defect is also increasing. The technology is scaling day by day. There are other reasons also which is leading to the presence of defect, error and fault in the design. Hence various strategies are applied to detect such defects and make our design error free. Design for test is one of the technique in which we add extra hardware to the design. This extra hardware added provide the controllability and observability points in the circuit. The main objective of adding this extra hardware to our design is to convert difficult to test sequential circuit into easy to test combinational circuit. Hence the testing of the circuit becomes easier. Random patterns are made to target the faulty sites, if the pattern is successful in targeting the fault then it saved else more patterns are generated to target the faults.

Inserting DFT in complex design is not easy. Hence, we need to divide the large design into partitions or small block so that we can analyze each block individual. The goal here is to make design power and area aware by adding some extra circuitry.

In this project of Scan construction and Validation of channel and rectilinear designs the netlist checker were developed to validate the multi Scan controller flow. The main objective to develop this flow was to provide a solution for a long channel elongated design, sometimes it becomes difficult to have only a single controller for the single partition as the blocks present inside the design becomes too much congested. Hence the routing becomes a challenge. Therefore we use a divide and conquer approach, means multiple scan controllers for a single partition. It will help to overcome the timing degradation which occurs due to the long routing area.

Table of Contents

Acknowledgement **4**
List of Figures **7**
Abbreviations **8**
Chapter 1: Introduction to Testing **9**
1.1 Introduction 9
1.2 Need for testing 9
1.2.1 Defects introduced by lithography 11
1.3 DFT Introduction **12**
1.4 Motivation **13**
1.5 Objective **13**
Chapter 2: Introduction to DFT **14**
2.1 Introduction to Scan Design 14
2.2 Scan Design Methodology 15
2.3 Scan Benefits 17
2.4 Wrapper Chains 18
Chapter 3: Literature Review **20**
3.1 Core Wrapper 20
3.1.1 Wrapper chains and Wrapper cells **20**
3.2 Inserting Test Points 22
3.3 Simultaneous Launch on Shift (LOS) 22
Chapter 4: Implementation **23**
4.1 Scan Synthesis flow 24
4.2 Design rule checking Flow 24
4.3 Netlist checker: 1 25
4.4 Netlist checker: 2 26
4.4 Netlist checker: 3 27
.... **27**
Chapter 5: Conclusion **28**
References **29**

List of Figures

Figure 1: Categorization of reliability issues in CMOS circuits 9
Figure 2:Impurities causing defect 10
Figure 3:Lithography defect 11
Figure 4: Defects 11
Figure 5:Shift capture cycles 12
Figure 6: Design Before and After Adding Scan 14
Figure 7: Scan Equivalent 16
Figure 8: Scan Representation 16
Figure 9:Design with partition 18
Figure 10: Wrapper Chains Added to Partition A 19
Figure 11: A Wrapped Core 20
Figure 12:Core Wrapper-Inactive mode 20
Figure 13:Core Wrapper -Inward Facing mode (INTEST) 21
Figure 14:Core Wrapper -Outward Facing mode (EXTEST) 21
Figure 15:Core Wrapper -Safe Mode 21
Figure 16:Long channel rectilinear design 23
Figure 17: SCAN SYNTHESIS flow 24

Abbreviations

DFT	Design for Test
IC	Integrated Circuits
CMOS	Complementary metal-oxide semiconductor
DRC	Design Rule Check
ATE	Automatic Test Equipment
BIST	Built in Self-Test
LOS	Launch on shift
TPI	Test point Insertion

Chapter 1: Introduction to Testing

1.1 Introduction

Today IC design includes complex VLSI system. Techniques are deployed to ensure high performance low power design. Apart from such changes there is also a drastic change that can be seen in technology scaling of transistors. So, number of transistors on a die is also increasing at a rapid rate. Hence, the testing of circuit with huge number of design components depends on effective and efficient test techniques for reliable screening of the defects. Deep-submicron integrated circuit manufacturing technology nodes are suffering from inherent intra-die, inter-die, lot-to-lot parameter fluctuations for both gates and interconnects [4]. The variation in physical parameters of elements effects the device performance and may result in permanent or temporary erroneous response. The complementary metal-oxide semiconductor (CMOS) circuit reliability issues can be categorized into two categories: spatial and temporal. The spatial unreliability can be defined as changes in physical parameters of the device when it is fabricated on different or the same wafer at distance apart. Whereas temporal unreliability is defined as changes in physical parameters of the device which occurs over a period under specific environmental conditions and workload. Chances that a defect is present in such a complex design is very high, so need for testing circuit becomes very crucial now-a-days. The technique which we use for testing a chip to say whether is faulty or not is DFT.

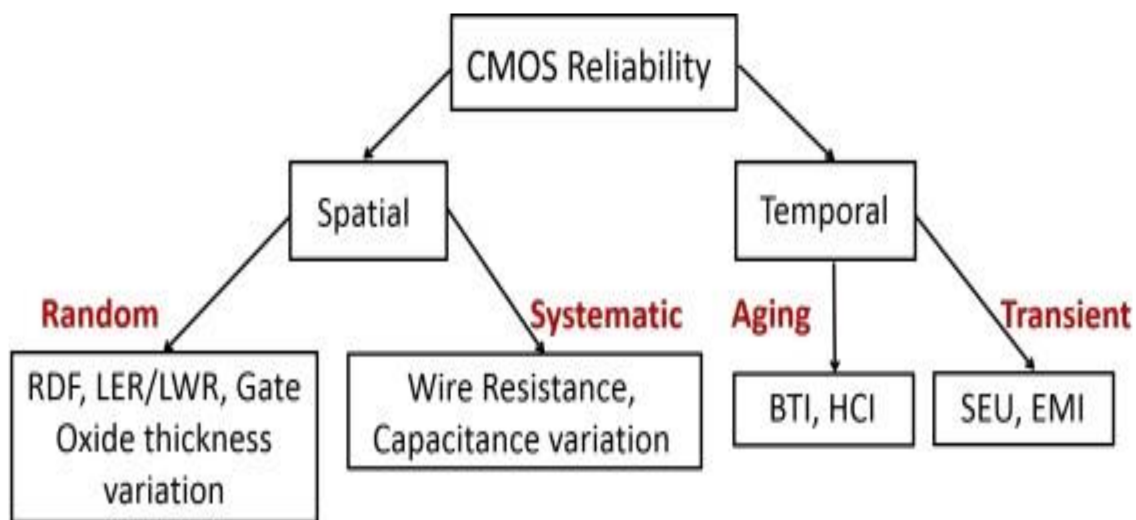


Figure 1: Categorization of reliability issues in CMOS circuits

1.2 Need for testing

Defects can be introduced at any step while designing a circuit, hence testing becomes very important to make sure that our design is working properly. In early days none of circuit designers were worried about generating test patterns that target the defects in circuit. At that time circuit consists of a few hundred to thousand transistors on a die. Hence in such a small design probability of occurring a defect was very small.

The Moore’s law has changed the paradigm of circuit testing after the integrated circuit (IC) manufacturers started putting double the transistors on same silicon area every 18 months and it is still going on below 14nm technology node. The whole process resulted in adding more than several million flip-flops on the same die. More number of transistors on a die result in more interactions between the transistors which can lead to the improper behavior of the circuit due to power supply noise, crosstalk, single event upset, electromagnetic interaction etc. Apart from these defects many others are also introduced during the fabrication of the circuit. So, in present scenario no one can guarantee the proper functioning of the circuit without carrying any specific pattern generation test which can target such faults, Defects, Errors, and faults.[5]

The terms defects, errors, and faults are confusing many times. A defect is a difference between the hardware implemented and the hardware that is desired. A wrong output signal that comes from a defected circuit is an error. A defect which we can express in form of Boolean expression becomes a fault. Here we will focus on defects that can occur in design process. Defects can be caused by dirt/impurities introduced during manufacturing process. Dirt can cause short or open in design, which will result in error.

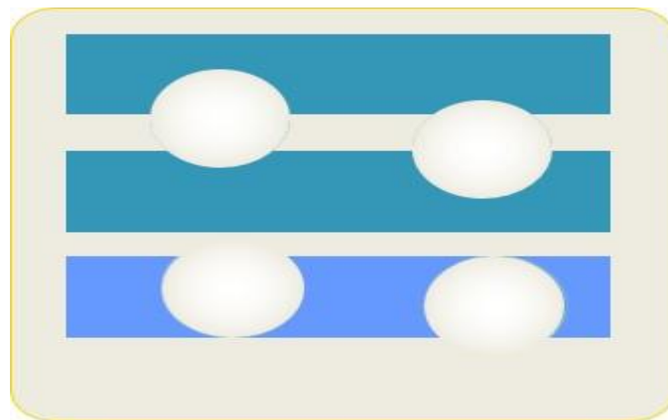


Figure 2:Impurities causing defect

1.2.1 Defects introduced by lithography

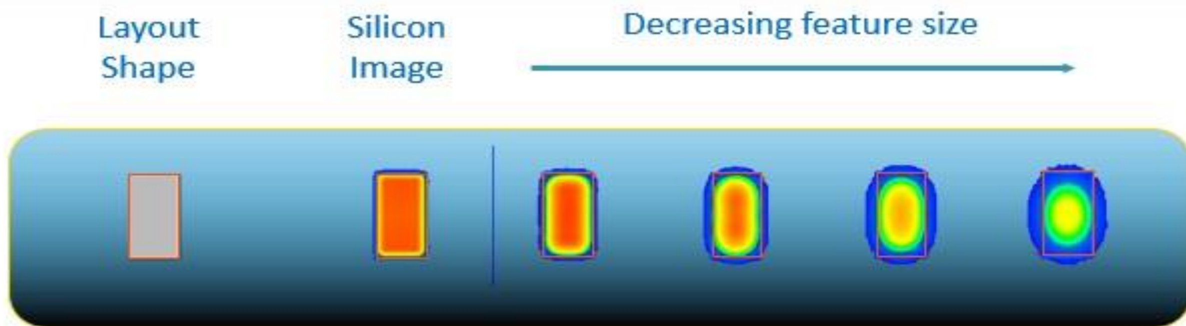
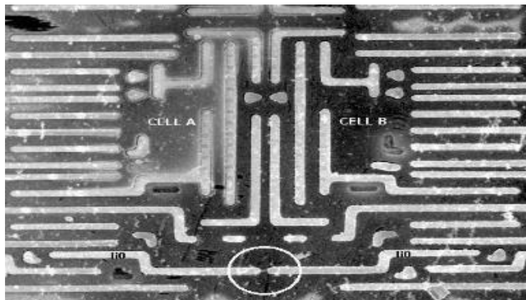
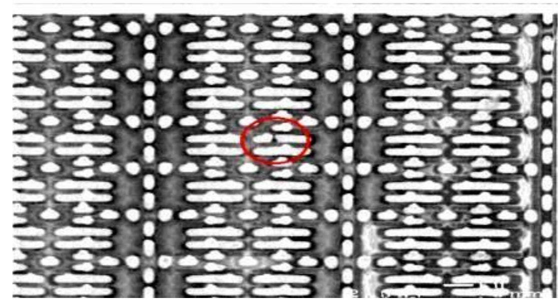
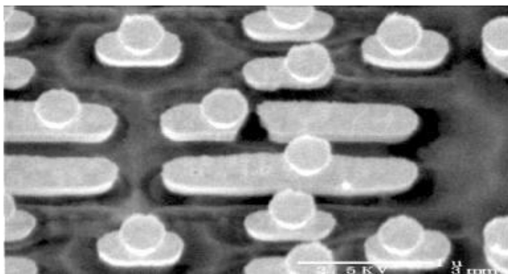


Figure 3:Lithography defect

IC process is defect prone







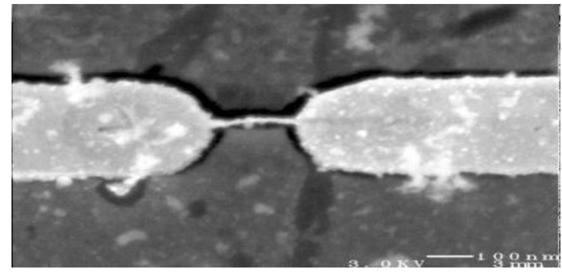


Figure 4: Defects

Other defects can be functional defects which causes a logical failure in the circuit. There can be open or short in the circuit. Current defects cause the high current to be drawn when the circuit is in static state. Speed defects prevents the at-speed circuit operations. Covering all kinds of defects will involve making patterns that can target those defects. After manufacturing of chip, patterns are sent to the tester which applies those patterns on chip and compare the output from expected to obtain. These patterns are applied at different clock frequencies to state the maximum frequency on which the chip can operate. Patterns are also applied by varying the operating voltage to find the maximum operating voltage.

1.3 DFT Introduction

Design for testability is a technique which adds the testability features to the design. Designs which are hard to test can be made testable easily by adding some extra hardware. Combinational circuits are easy to test so we apply the DFT technique mainly on the sequential circuits. In case of testing a simple digital counter if we want to test its output when counter is in state 5, then we require 6 clock cycles, first five cycles will make counter in state 5 and 6^{the} cycle will capture its output response. But if we apply DFT then we can directly make counter in 5th state and then apply inputs to capture the response.

DFT adds extra hardware to the circuit, it also makes impact on the timing requirements of the circuit. Hence it is not always advisable to add this extra hardware in circuit. Intel high end servers works at very high frequency clock adding extra hardware for testing will cause timing violations, so no extra hardware is added in such cases it is beneficial to waste some clock cycles to drive the system in desirable state.

So practically it is not possible to convert all the memory elements present in our design to scannable elements.

Generally, we give inputs to set the state of memory elements, this phase is named as launch phase then after this we apply the external inputs and capture the response of circuit by giving the capture cycle. After capture cycle shift cycles are given to shift out the data from the memory elements.

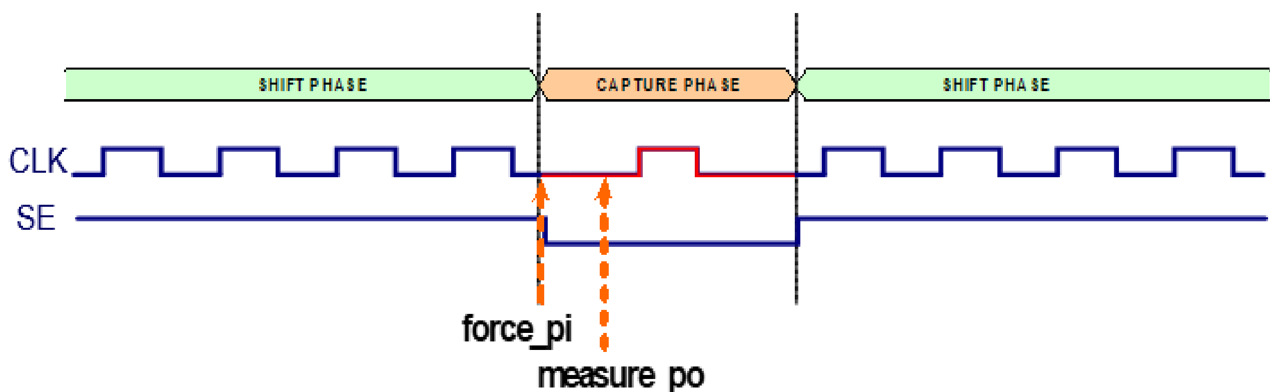


Figure 5:Shift capture cycles

Above figure shows while scan enable is high the data is fed into the design to set the internal states of the memory elements. As the design is having sequential depth of size four so after four clock cycles we made scan enable 0 and fed the input from external source. We then capture the output in capture phase.

We can serially shift the data to all the flops and capture the response or we can also shift the data in parallel and then capture the response. Loading data in parallel to the circuit will require a single clock cycle but it will also require additional pins through which we can apply the input so it will result in extra pins so, we avoid this case.

1.4 Motivation

- For a long elongated design, sometimes it becomes difficult to have only a single controller for the single partition as the blocks present inside the design becomes too much congested. Hence the routing becomes a challenge.
- There we use a divide and conquer approach, means multiple scan controllers for a single partition.
- It will help to overcome the timing degradation which occurs due to the long routing area.

1.5 Objective

- To understand the flow of SCAN SYNTHESIS Compiler.
- To provide a Scan construction solution for long rectilinear designs.
- Optimize area and power of complex multipower SoC's while inserting Core wrapper/LOS/test points.

Summary

In this chapter the basic points regarding the need for testing were discussed. Defects can creep in at various points of the fabrication process, so there arises the need to test our circuit thoroughly. In the latter half of the chapter the objectives and the motivation of the project were laid.

Chapter 2: Introduction to DFT

2.1 Introduction to Scan Design

We modify the design of circuitry by adding the scan design so that the testability of design can increase. Sequential circuits are generally hard to test whereas combinational circuits can easily be tested so main idea behind this scan design is to make sequential circuits easily testable. To make such thing possible we replace the sequential elements of the circuit with scannable sequential elements which are also known as scan cells and then we tie these scan cells together to form a scan register or scan chains. We can have any number of scan chains in our design. Generally, these scan chains are not made very long instead we use to have a greater number of scan chains of shorter length. Data can be shifted in and out of the design using these scan chains when design is in scan mode. So now our design consists of two modes one is scan mode and other is normal mode.

The design shown in figure below contains both combinational logic and sequential logic blocks. Before adding the scan design, we were having A, B and C as three inputs and Out 1 and Out 2 as two outputs of the design. This circuit is not easy to initialize to any specific state.

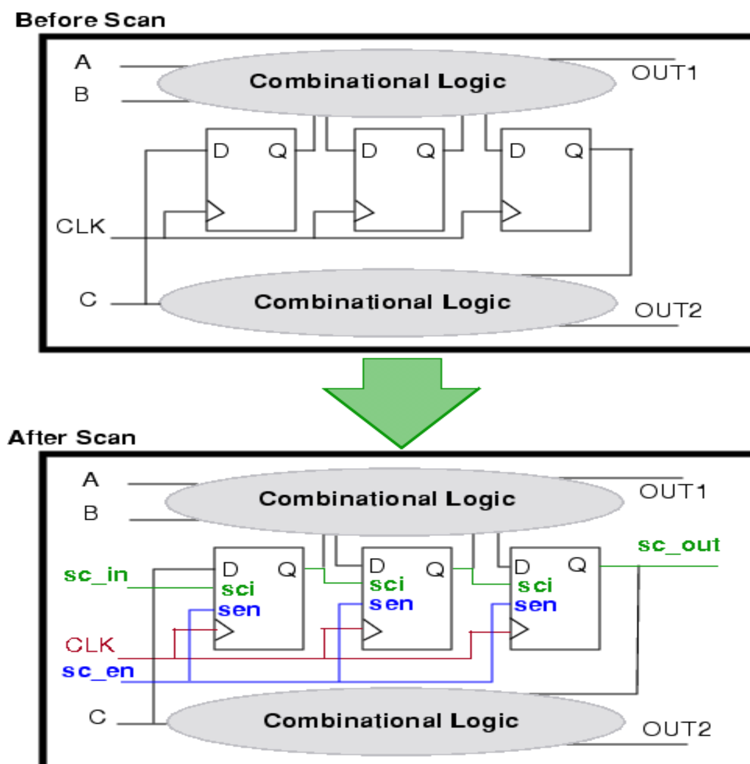


Figure 6: Design Before and After Adding Scan

So as discussed above we must convert this difficult to test sequential logic too easy to test combinational logic by adding some additional hardware to the design.

So once the scan circuitry is added, now the design has 2 more inputs, skin and sc_en, and it also now have one more output sc_out. Non-scan cells are nor converted to scan cells so when shifting of data is done i.e sc_en pin is high, the data which we want to feed in the circuit (to set any particular state) is driven in from the sc_in pin, thus we can drive our circuit to a desired state by giving the proper inputs through sc_in pin.

The procedure according to which scan circuitry works is stated below :

1. Set scan enable pin high to start the scan operation which allows the shifting of data through the scan cells.

2. After the data is shifted/loaded into the scan elements, scan enable pin is set low and data is applied to the design through primary input pins.

3. Corresponding to the applied inputs we will get some output from output pins which are now measured.

4. Again, make scan enable high to insert data into scan equivalents.

2.2 Scan Design Methodology

If any memory element is present in the design then we replace the memory elements in the design with their scannable equivalents. It is generally not possible to convert all the memory elements into their scannable equivalents as adding scan circuitry also adds to the delay of signals. Flops operating on high frequency clock cannot be converted as it may cause timing violations. So, we can do one thing we can convert all memory elements to their scan equivalents and run the test, later we can remove scan circuitry from the flops where timing violations are taking place. It's nearly impossible to app the DFT technique in high end Intel servers. Figure 6 shows the conversion of D-FF to scannable D-FF.

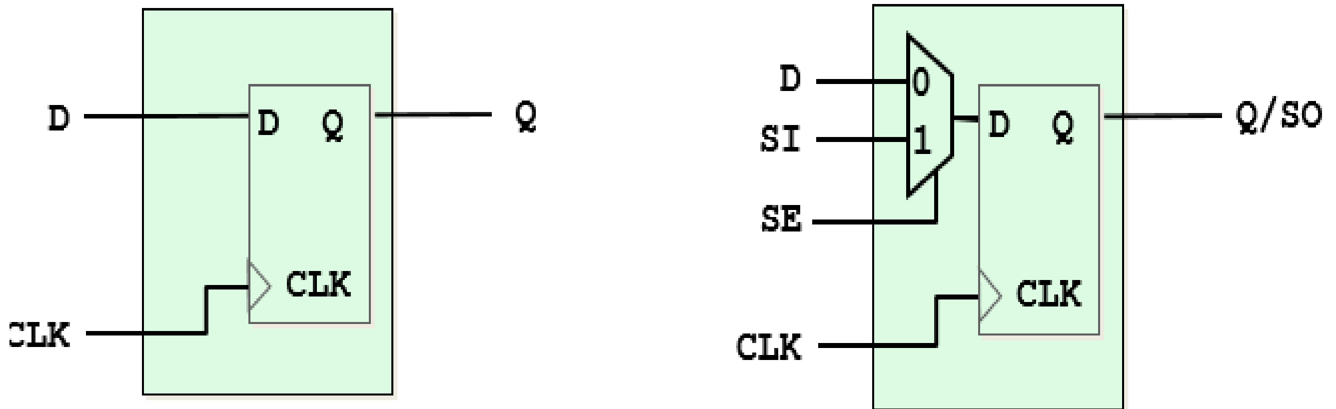


Figure 7: Scan Equivalent

In Scannable version of D-FF we add one multiplexer whose select line will decide whether we want to operate our flop in normal mode or in scan mode.

Figure 7 shown below display the representation of the scan design.

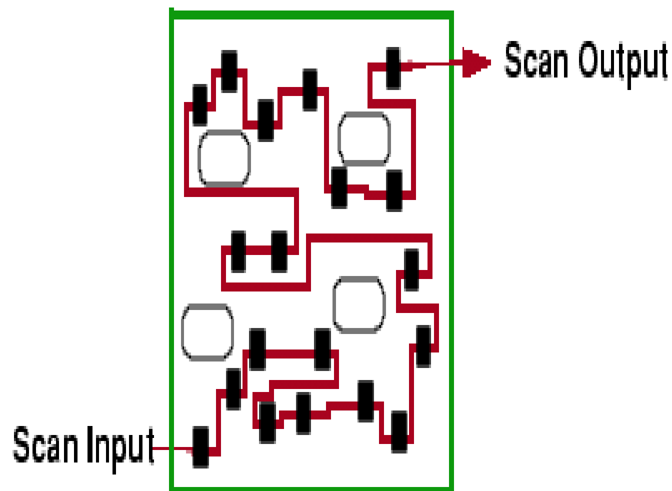


Figure 8: Scan Representation

The black boxes represent the scan circuit. The line joining all the scan elements is the scan path. The connected scan elements form one scan chain through which data can be shifted in and output can be observed at the end of the scan chain. The round blocks shows the combinational part of the design and thus they are not a part of the scan chains.

2.3 Scan Benefits

- **Highly automated process**

If the process is highly automated then the chances of occurring an error also decreases. There is a feature of scan insertion available in the tool using which we can insert scan circuitry in our design thus insertion of scan circuitry becomes highly automated, thus it requires very little manual effort. In a typical design we are having millions of flip flops present making each flip flop scannable manually is not easy at all. If we want don't want to convert some memory elements into their scan equivalent then we can provide a list of those memory elements to the tool, it will skip those during the process.

- **Highly effective**

Scan design is a highly effective, it helps in increasing the test coverage for the design. High test coverage is always desirable, using wrapper cell around the scan elements also increase the test coverage. So, while applying the scan methodology we should consider various factors which will help to obtain high test coverage.

- **Ease of use**

Following the scan methodology correctly we can easily insert scan circuitry to the design, and we can directly run the ATPG test without taking the help of test engineer. Running ATPG test will give us patterns which we can directly send to the tester. Tester can use these patterns to find the defects in the design.

- **Moderate area**

Scan design generally increases the area of whole design by 10% and increases the speed overhead by 5 %. So, instead of adding the extra hardware the area of the whole design do not increase much .

Following are the drawbacks of using scan strategy :

- Large test data volumes which results in a more test time.
- Increases the overheads and may cause timing related issues.

2.4 Wrapper Chains

The ATPG process on very large, complex designs can often be unpredictable. This problem is especially true for large sequential or partial scan designs. To reduce this unpredictability, several hierarchical techniques for test structure insertion and test generation are beginning to emerge. Creating wrapper chains is one of these techniques [3]. Performing ATPG test directly on the large design can be difficult hence we split our large design into a few small design blocks that are independently performing any specific task.

At the boundary of a design partition we have some scan cells, these scan cells relate to each other and forms a chain which is known as a wrapper chain. Scan cells that are having low controllability and observability from the outside block are converted to the scan cells by the wrapper chain. As now the controlling points in our design has increased so it will also improve test coverage as well as run time.

The wrapper chain formation is given in the figure shown below, the design shown in the figure below consists of the three partition.

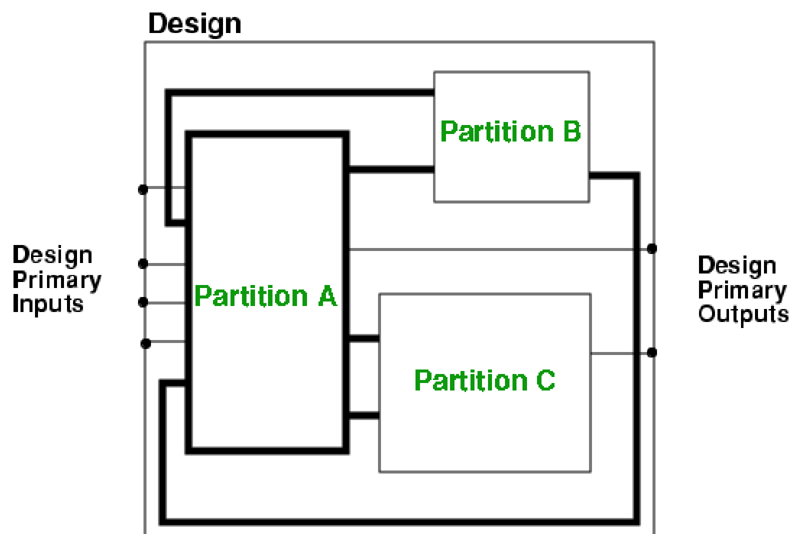


Figure 9:Design with partition

Dark lines in the above figure shows inputs and outputs of partition A which are not directly controllable or observable. Because of this, the circuitry whose operation depends on these pins can cause testability problems, as we cannot force any data to the input and output pins of partition A, and it will also cause low test coverage.

In next figure wrapper chain structure has been inserted which increases the controllability and observability, or overall testability of the whole design. Now we can insert the data according to our need in these pins and it will also increase the test coverage.

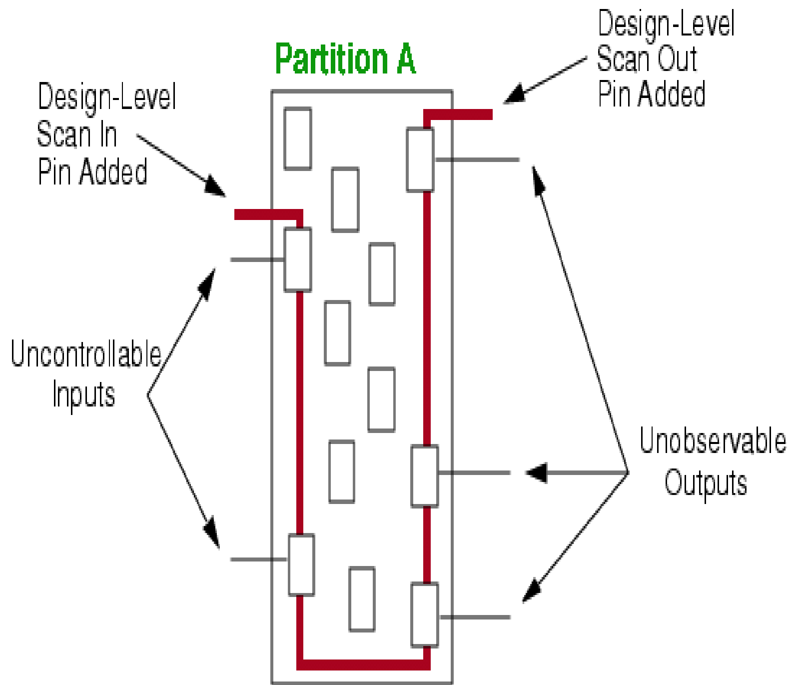


Figure 10: Wrapper Chains Added to Partition A

The inputs which were earlier uncontrollable can now be controlled through the wrapper chain, we can insert the data through this chain. The wrapper chain is formed by joining the scan cells present at the boundary of the design partition.

Chapter 3: Literature Review

3.1 Core Wrapper

Core must be wrapped core in order it to test it separately from the top-level logic. Scan Synthesis flow provides an advantage such that it uses the existing functional registers which helps in to minimize the area and timing impact on the design.

3.1.1 Wrapper chains and Wrapper cells

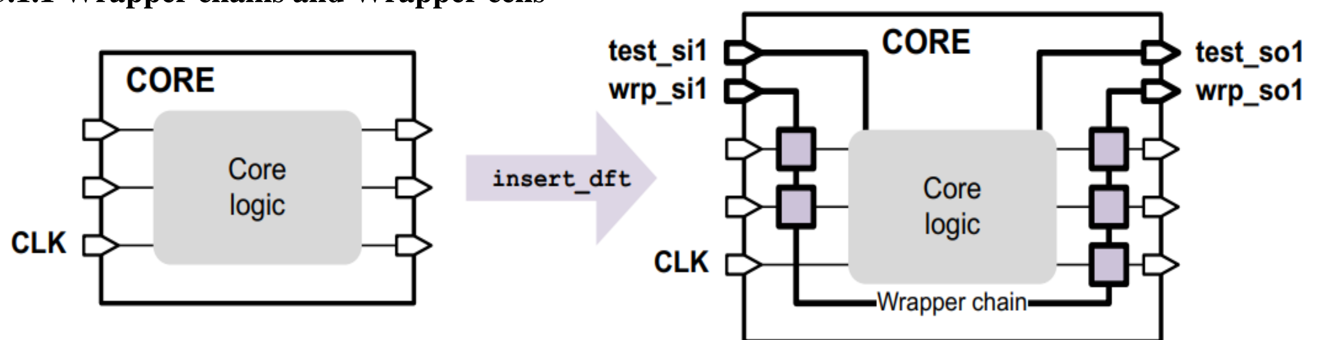


Figure 11: A Wrapped Core

A wrapped core has a wrapper chain that allows the core to be isolated from the surrounding logic. A wrapper chain is composed of *wrapper cells* inserted between the I/O ports and the core logic of the design.

The wrapper chain operates the following modes:

a) Inactive Mode

The I/O pass through it, wrapper chain is inactive.

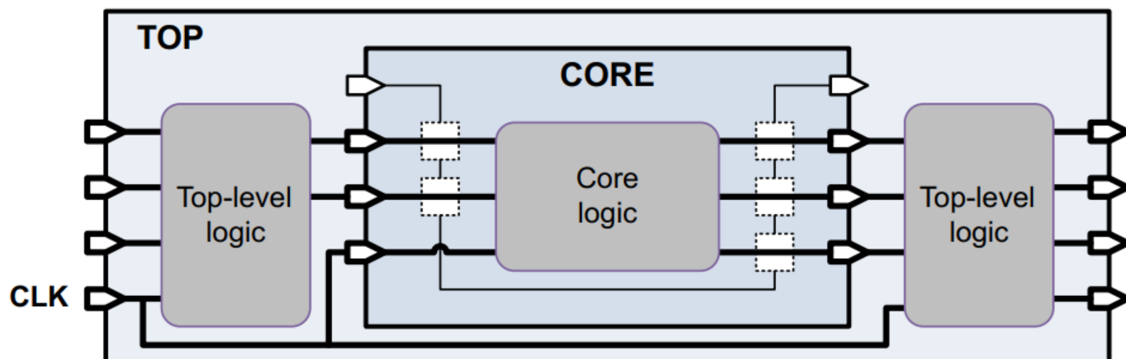


Figure 12:Core Wrapper-Inactive mode

b) Inward Facing mode (INTEST)

In this mode core is tested in isolation with the logic.

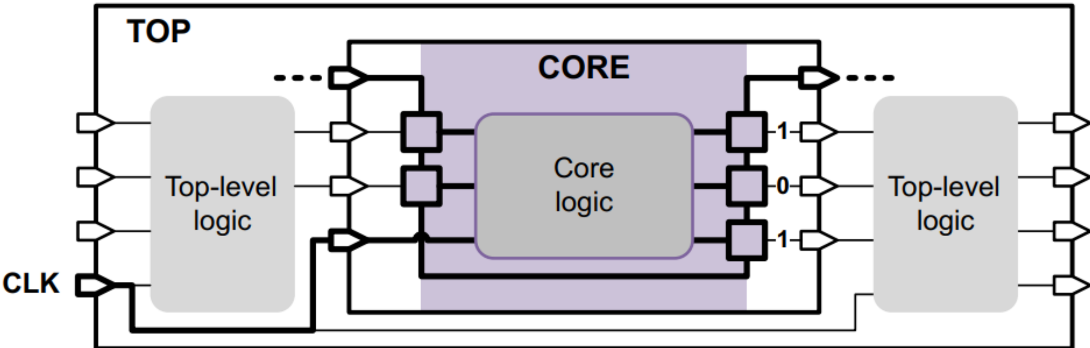


Figure 13:Core Wrapper -Inward Facing mode (INTEST)

c) Outward-facing mode (EXTEST)

In this mode surrounding logic is tested in isolation with the core logic itself.

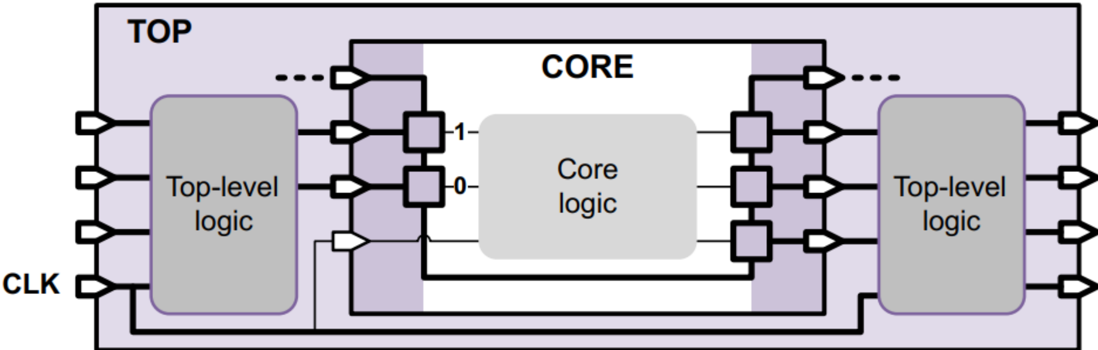


Figure 14:Core Wrapper -Outward Facing mode (EXTEST)

d) Safe Mode

This is an optional mode. In this mode safe values are passed through the wrapper cells.

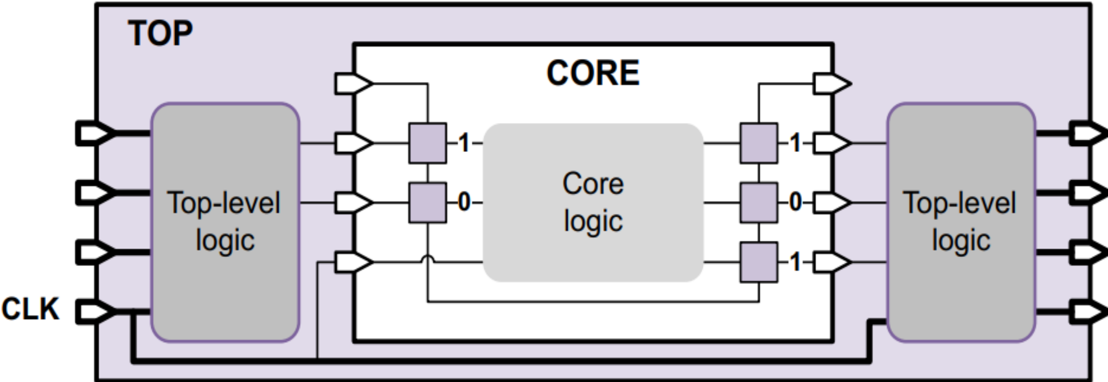


Figure 15:Core Wrapper -Safe Mode

3.2 Inserting Test Points

Test points are inserted by the tool to improve the testability of the design. The tool decides automatically where to place the Test points in order to improve the testability, test coverage and the to make the ATPG easier. Test points can be added manually.

Test Point Types

In Force test points the signal gets overwritten throughout the test program.

1. Force Test Points
2. Control Test Points
3. Observe Test Points
4. Multicycle Test Points

3.3 Launch on Shift (LOS)

LOS provides an advantage for the testing to be performed in parallel. This method is useful when there is no Clock domain crossing (CDC).

Following are the advantages provide by this approach:

(1) All interlock-domain delay faults can be tested simultaneously

(2) This method can be used to test all clock domains in parallel without the need to arrange or place the clock in a certain order, but simply using whatever clock pulses are available in each clock domain.

Summary

In this chapter the literature survey on the topic of LOS, Core wrapper and test point insertion was carried out. Core wrappers are inserted in order to test the core or the logic separately. It makes the process of the testing faster and more compact. Similarly, the test points are inserted so that the node can be tested more conveniently.

Chapter 4: Implementation

In this chapter the implementation part of the project is discussed. Several design rule checks were implemented to validate the flow. These DFT checks helps us to check the working of the design. Many checks were implanted such as each DFT partition must be driven from control signals defined per partition. Scan-data-in pins/ports should drive the scan chains and Scan-data-out pins/ports should be driven by the Scan-chain. Test port creation checks. If LOS enabled, then all scan flops must be driven through LOS register which will be later described in the chapter.

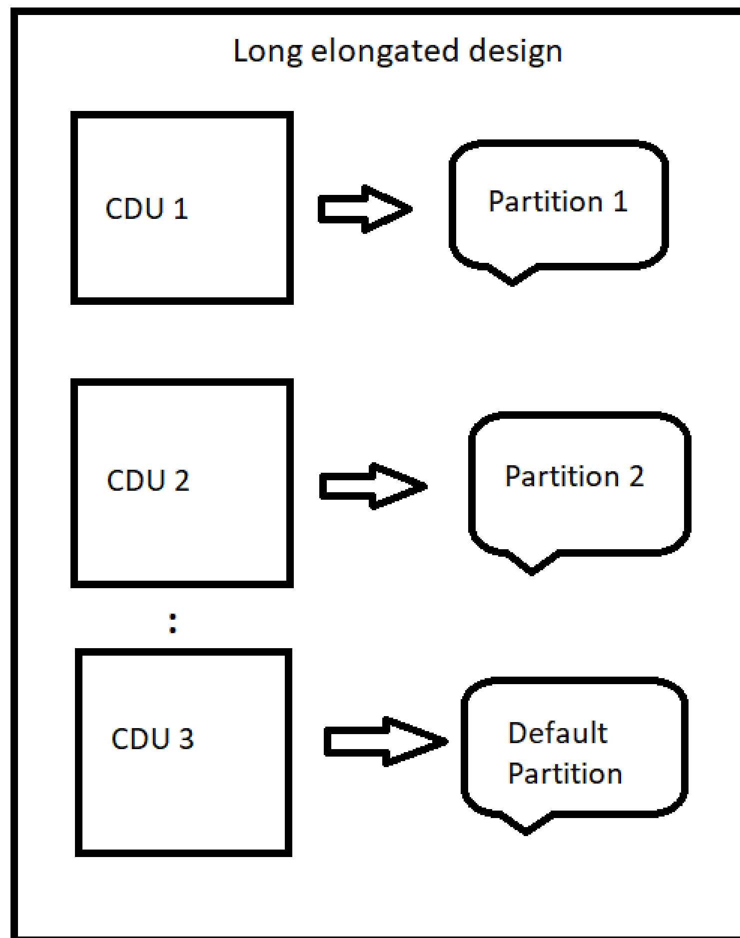


Figure 16:Long channel rectilinear design

4.1 Scan Synthesis flow

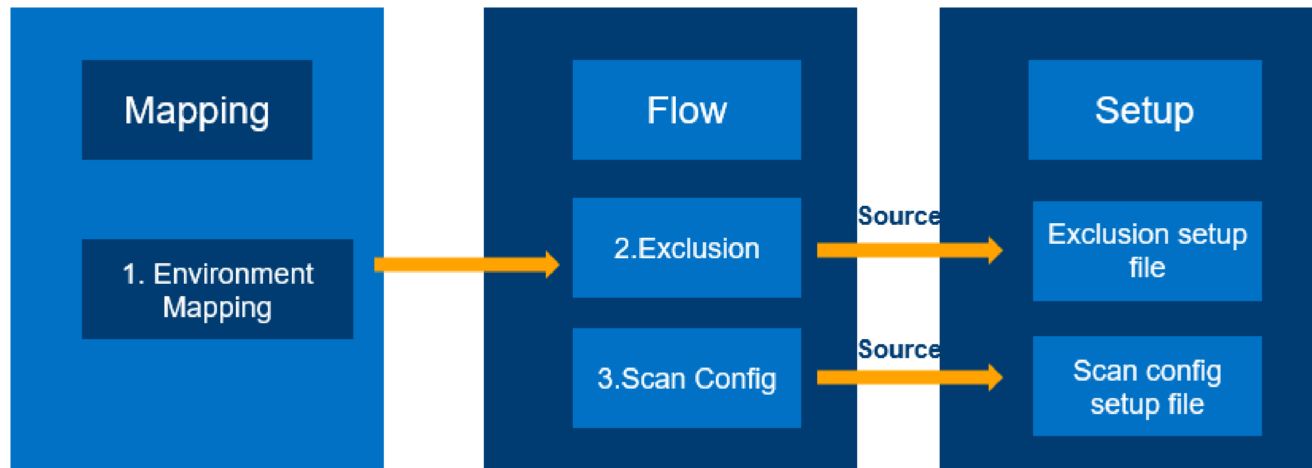


Figure 17: Scan synthesis flow

4.2 Design rule checking Flow

Read scan_def to extract the scan chain information

- Collect all scan flops on chain
- settting of clock gating test enable pin
- Preparing a list of non scan deisgns
- Preaparing a list of non scan instances
- Removing latches from scan chains

Setting dft non scan elements

Each DFT partition must be driven from control signals defined per partition.

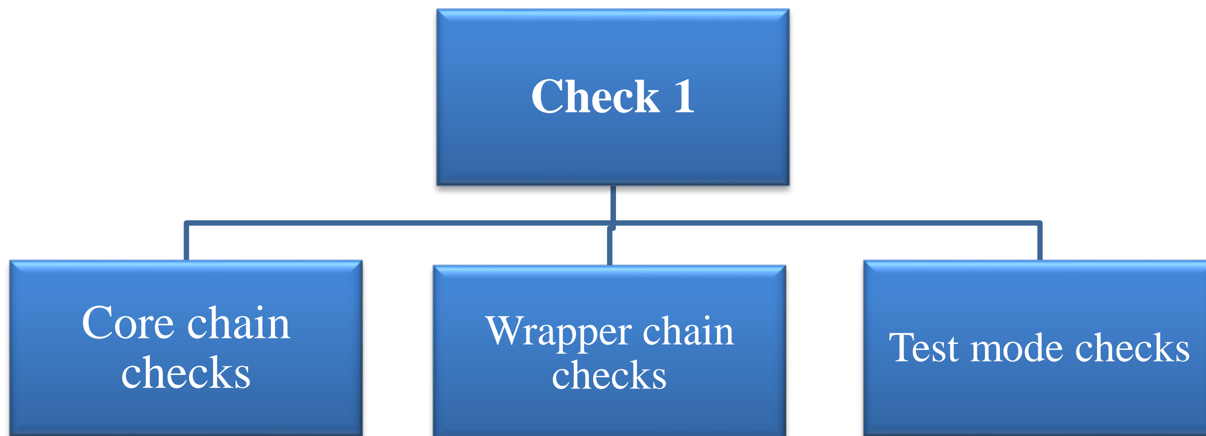
Setting all signals

- scan enable
- wrapper enable input and output
- wrapper enable out
- wrapper capture enable out
- clock gate enable
- LOS enable
- clock gate enable signals

Before defining the rules all the signals must be set in order that all the signals are having the required Value.

4.3 Netlist checker: 1

Each DFT partition must be driven from control signals defined per partition



1.a. Core Chain checks

1. Scan enable must drive the scan chains of the same partition

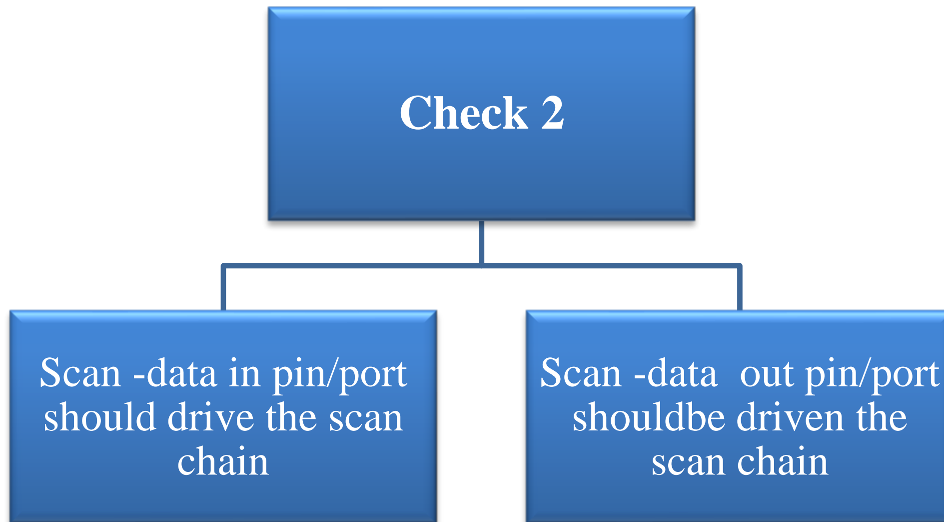
1.b. Wrapper chain checks

1. Input wrapper chain shift enable must drive the wrapper flops of the same partition.
2. Output wrapper chain shift enable must drive the wrapper flops of the same partition.
3. Input wrapper chain capture enable must drive the wrapper flops of the same partition.
4. Output wrapper chain capture enable must drive the wrapper flops of the same partition.

1.c. Test Mode checks

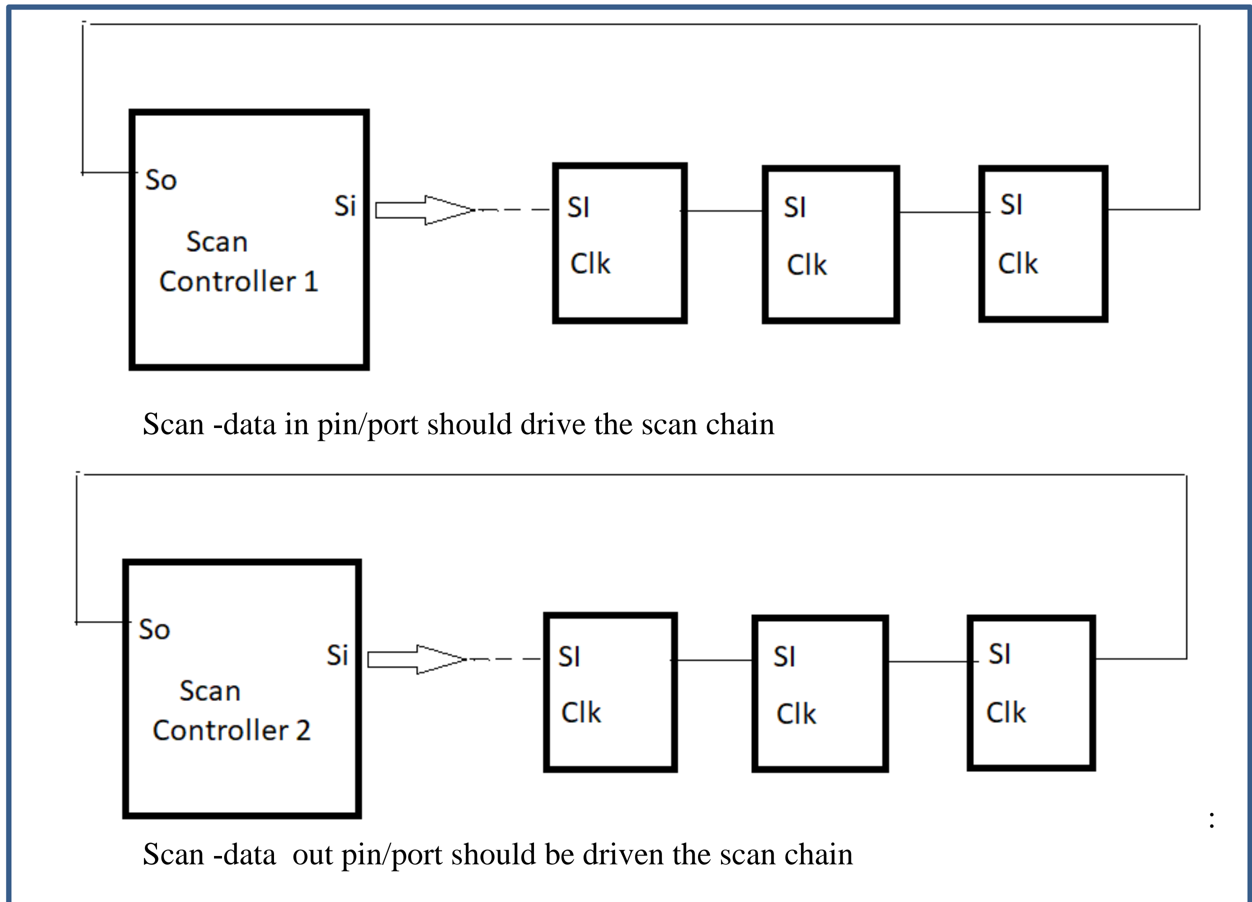
1. Clock-gating enable signal must drive Integrated clock gating cells during Synthesis from the same partition.
2. Clock-gating enable signal must drive the RTL added ICGs (Integrated clock gating cells) from the same partitions.

4.4 Netlist checker: 2



2.a. Scan -data in pin/port should drive the scan chain

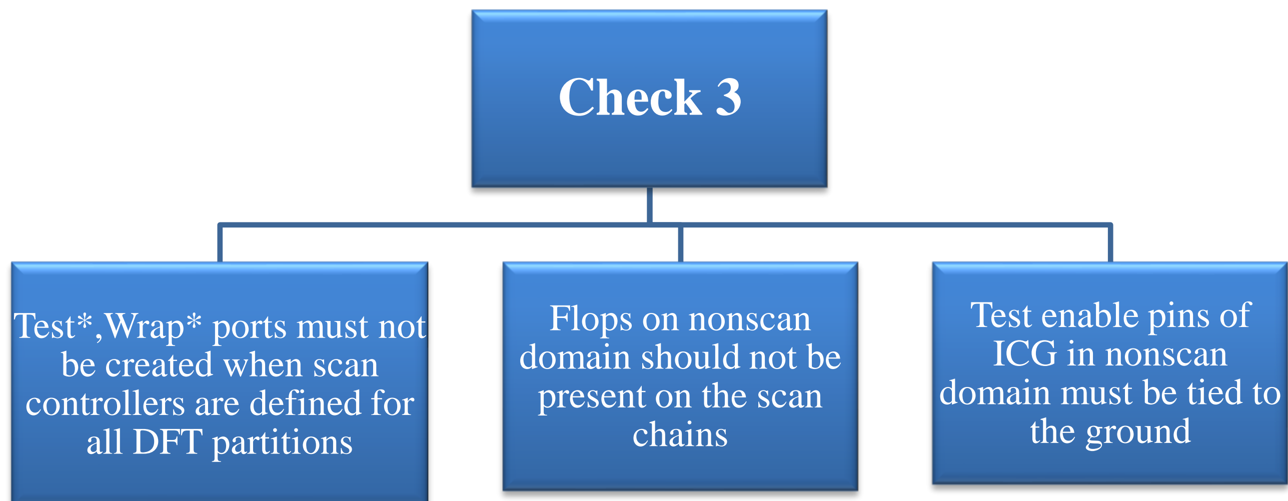
2.b. Scan -data out pin/port should be driven the scan chain



Scan -data in pin/port should drive the scan chain

Scan -data out pin/port should be driven the scan chain

4.4 Netlist checker: 3



These netlist checkers helps us to verify the connectivity of all the signals after the scan insertion. These Checkers helps us to validate the multiple scan controller flow.

Summary

In this chapter the implementation part of the project were discussed. Intel tools works on lot of automation. So, Multi scan controller Netlist checkers were created in order to validate the correct working of the flow.

Chapter 5: Conclusion

Conclusion

DFT process lies between the design and verification process. Because of adding this extra logic in our design, we can verify whether our design is fault free or not. Company need its product to be reliable, so that customer can buy its product again and this reliability comes by DFT. A single transistor can leave entire part unusable. By applying DFT we save our design from bigger loss. DFT not only helps to detect the defect but in many case it also provides the repairability option as in case of memory. If any bit in memory gets defected than simply throwing the memory applying the new one can cost a lot in such case provide some spare memory which can work in case any bit gets defected.

In today's world doing everything manually is not a good option. Amount of work is increasing so we need to automate our task by scripting. By designing a small piece of relevant code, you can save your working hours.

For a long elongated rectilinear design, sometimes it becomes difficult to have only a single controller for the single partition as the blocks present inside the design becomes too much congested. Hence the routing becomes a challenge.

If a design is having 20 partitions and 20 scan controllers. So that means one controller for each partition but if the design is having an elongated partition then it becomes a problem due to congestion. So, the validation rules for multi Scan controller based flow were developed

References

[1]. Complex SoC Testing with a Core-Based DFT Strategy by Sandeep Kaushik, Synopsys and Paul Policke, Qualcomm 02.26.2008 Test and measurement designline EE|times.

[2]. https://solvnetplus.synopsys.com/s/.

[3]. Teresa McLaurin consulting member of the technical staff at the ARM Design Center in Austin, TX. Title Wrap' your cores to enable SoC test, Nov 24 2004 EDN.

[4]. A. Srivastava, V. Singh, A. Singh, and K. Saluja, "Identifying high variability speed-limiting paths under aging," in Proc. of IEEE Latin American Test Symposium, 2017.

[5]. S. K. Goel, N. D. Prasanna, and R. P. Turakhia, "Effective and efficient test pattern generation for small delay defect," in Proc. of VTS, 2009.

[6] A.T.E. Solutions, Inc., Design for Testability and for Built-In Self Test, Course Notes, http://www.besttest.com/Courses/00001-DFTBIST.cfm, last updated August 2016.

[7] Institute of Electrical and Electronics Engineers, 1149.1-2013 IEEE Standard for Test Access Port and Boundary-Scan Architecture, 2013. (Supersedes IEEE-1149.1-1990 and IEEE-1149.1-2001)

[8] Brandon Davis, Economics of Automatic Testing, McGraw-Hill, 1994

[9] J. Lee, M. Tehranipoor, C. Patel, and J. Plusquellic, ``Securing designs against scan-based sidechannel attacks,'' IEEE Trans. Dependable SecureComput., vol. 4, no. 4, pp. 325_336, Oct. 2007.