Gigabit Ethernet Based Image Acquisition System for IR Camera

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***Abstract*—. With the advancements in the hardware technology, it is now possible to transmit data over Ethernet at the rate of 100Mbps/1Gbps. The only limiting factor for such a high speed data transfer is the speed of the processor in the computer which does all the TCP/IP processing by using the TCP/IP software written in it. In the present system, the IR sensor used is taking 50 images of plasma per second. When these images data are converted into digital, 7.3 Mbytes of data is required to be transmitted over the Ethernet. To transfer such a huge amount of data over the Ethernet, a TCP/IP Offload Engine (TOE) is used. TOE has the TCP/IP protocols implemented in hardware and does the all the TCP/IP processing. Thus, the image data transfer at Gigabit speed is achieved.**

Keywords: Ethernet, FPGA, Gigabit Ethernet, IR camera, TCP/IP, TOE

I. Introduction

As the network connections scale beyond Gigabit Ethernet speeds, the CPU becomes burdened with the large amount of TCP/IP protocol processing. In high-speed networks, the CPU has to dedicate more processing time to handle the network traffic than to the applications it is running. The TCP/IP Offload Engine (TOE) is emerging as a solution to reduce the processing required by CPU for networking links. The TOE may be embedded in a network interface card, NIC, or Host Bus Adapter, HBA. The TOE has the TCP/IP protocols implemented in hardware. So, it can reduce the amount of TCP/IP processing handled by microprocessor and server I/O subsystem, and thus ease server networking bottleneck. Deployment of TCP/IP offload in conjunction with high-speed Ethernet technologies enable applications to take full advantage of the networking capabilities.

The Fig. 1 shows the block diagram of the Gigabit Ethernet Based Image Acquisition System for IR Camera using Gigabit Ethernet TOE (GigE TOE).

The frame size of the image, taken by the IR sensor,is 240 X 320 pixels. This is called the raw image. The analog signal output from an IR camera is transmitted to the 4-stage amplifier. A 14-bit, 10MSPS (Mega Samples per Second) Analog to Digital Converter (ADC)is used to convert these analog signals into equivalent digital signals. The digital

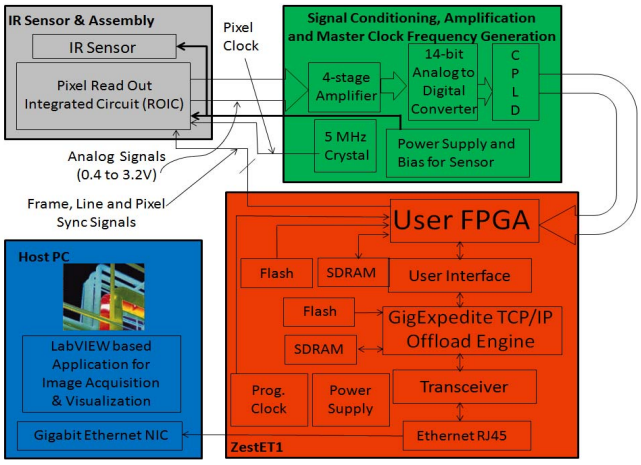

Fig. 1. Block Diagram of the Image Acquisition System for IR Camera

signal output is transmitted to the Host PC over the network using TCP/IP protocol. The image data packetization is performed by the TOE to transmit the data over the high speed Ethernet. The Spartan-3A FPGA is used to generate the frame synchronization, line synchronization and the pixel synchronization signals for the IR sensor. The data is, then, received by the NIC, the Gigabit Ethernet card available on the host PC, from the TOE. To receive and visualize the images taken by the IR camera, a client-based application is developed using the LabVIEW. The TOE is here configured as the server.

II. Hardware Description

A. IR Sensor & Assembly

The IR sensor is an infrared opto electronic device sensitive to radiation in the Long Wave (8 to 14 micrometers) spectral region. It includes a microbolometer focal plane array (FPA) based on a 340 240 (configurable to 384 X 288) elements two dimensional detectors array made from amorphous silicon resistive bolometers connected to a silicon readout integrated circuit (ROIC). The frame rate can be either 25-30 Hz or 50 - 60 Hz; typical is 50 Hz which is used here.The reason behind

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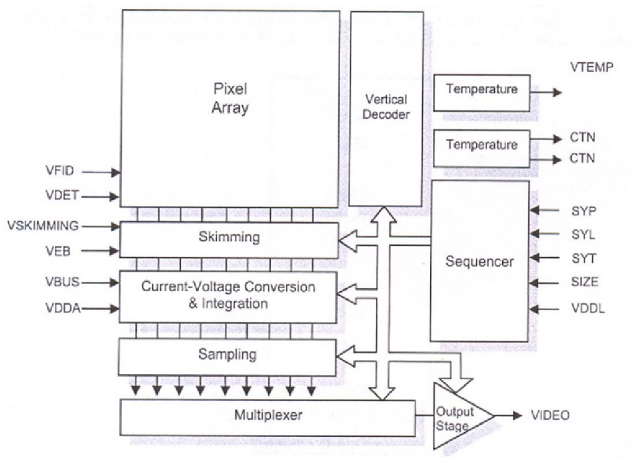

Fig. 2. Block Diagram of the Image Acquisition System for IR Camera

using the uncooled type of sensor is the operating range (Long Wave Infra Red, LWIR) which is the requirement to measure the very high temperature of the plasma produced in the tokamak. The power supply requirement for analog circuit in the ROIC is +5V and 3.3V for digital circuit in the ROIC. The output dynamic range of the IR sensor assembly is 0.4V to 3.2V and the typical responsivity is 4mV/K.

The Fig. 2 shows the block diagram of the pixel Read Out Integrated Circuitry (ROIC). The pixel array size is 320 X 240, i.e., there are 76,800 pixels in the pixel array of the sensor. That means there are 76,800 microbolometer sensors to sense the temperature. therefore, there are 76,800 associated readout integrated circuitries (ROICs) to convert the measured temperature into equivalent current. Each pixel ROIC consists of an active bolometer, a blind bolometer and a current to voltage convertor and integration amplifier (CTIA). The output of the active microbolometer is given to the CTIA for converting the corresponding current into equivalent voltage and for integration. The blind bolometer is used for the range adjustment and for calibration. The readout circuit allows the detector signal readout and the integration of the same row by row. The integration of a row occurs during the readout of the preceding row. For the sequential reading of each pixel, three external clock signals; so called synchronization signals are given. These signals are frame synchronization (SYT), line synchronization (SYL) and pixel clock (SYP). The readout circuit operates in a pulse mode, i.e., microbolometers are only biased during the integration.

B. B. IR Sensor Output Signal Amplification, Conditioning and Pixel Clock Generation

The output of the ROIC is given to the 4-stage amplifier; which is high input impedance (1st stage) and a low output impedance amplifier (4th stage). The 2nd stage in the amplifier removes the offset (0.4V) introduced by the IR sensor. The 3rd stage provides amplification using a digital potentiometer to choose one of the four gain settings available. The output of the amplifier is given to the 14-bit, 10MSPS ADC. The digital output of the ADC is then given to the TCP/IP Offload Engine for TCP/IP processing. The pixel clock signal (5 MHz)to read the pixel values in the image is also generated here. The value of the pixel clock signal (5 MHz) is calculated as follows:

Frame rate = 50Hz, i.e., 50 frames/second
Therefore,Time for one frame (SYT) =1/50Hz = 20 ms

240 lines in a frame, therefore, time for one line (SYL)
= (20 ms / 240 lines) - blanking time
= 80 sec- 19 sec = 64 sec

320 pixels in a row, therefore, time for each pixel (SYP)
= 64 sec/320 pixels = 0.2 sec

Therefore, the pixel clock signal frequency
= 1 / 0.2 sec = 5 MHz

C. The TCP/IP Offload Engine (TOE)

The output of the ADC is passed on to the write FIFO configured on the Spartan-3A FPGA available on the ZestET1 board, having the GigExpedite^{TMTM} TOE of Orange Tree Technologies (Fig. 3).

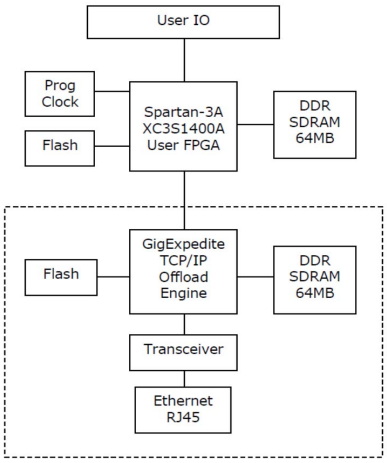

Fig. 3. Block Diagram of ZestET1 Board

The FPGA is programmed to generate the synchronization signals for the IR sensor and enables the data transmission to the GigExpedite^{TM}, configured as the server here. The FPGA is also programmed to buffer the data from the IR sensor temporarily using DDR SDRAM available on the ZestET1^{TM} as FIFO buffer. The data output from the read FIFO configured on the FPGA is passed on to the GigExpedite^{TM} for TCP/IP processing of the image data through the Ethernet Interface which the user can access using the GigExpedite^{TM} wrapper IP core. The Fig. 4 shows the block diagram of the

GigExpedite™.

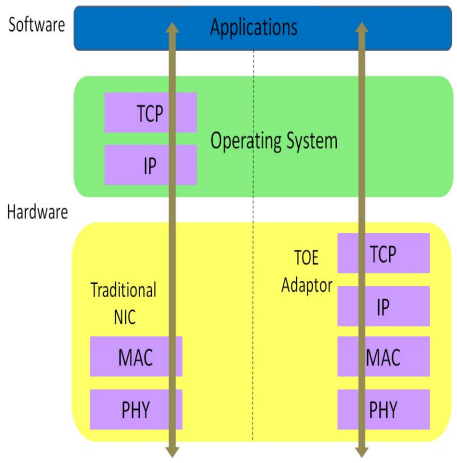

Fig. 4. Block Diagram of GigExpedite™

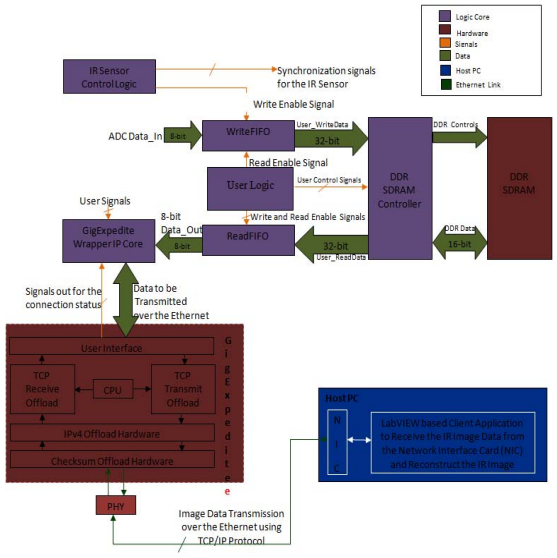

Fig. 5. Data Flow Diagram

The data in the GigExpedite™ is processed and is converted into TCP data packets and is transmitted over the Ethernet. The data from the Ethernet is received by the Gigabit Ethernet Card available on the Network Interface Card (NIC) of the host PC (or the client).

D. Host PC

The client application residing on the host PC, designed using the LabVIEW™, manages the data communication over the Ethernet. Whenever, the client is ready for the communication, it sends the connection request to the server. The server which is listening to the network continuously, accepts the request and opens the port for the communication. Once the port is open for the communication, the image data is sent to the host PC. The client application here receives the data and reconstructs the IR Camera image using the NI vision and motion functions. Whenever, the client wants to stop the communication, it sends the corresponding request to the GigExpedite™ (server) and the communication gets over.

III. Data Flow Diagram to Acquire the Image from IR Camera

The Fig. 5 shows the data flow diagram for the Image Acquisition system. The VHDL code is written in the FPGA (on the server side) to accomplish the image acquisition. In the host PC, a LabVIEW based client application is developed to receive the data from the Ethernet and to reconstruct the image.

IV. Flow Chart for VHDL Code

After the initialization of the GigExpedite™ as a server, there are three processes running parallel; the one process is sensitive to Ethernet Clock and handles the communication with the host PC, the client, the other is sensitive to the Pixel Clock and receives the data from the GigExpedite, the server,

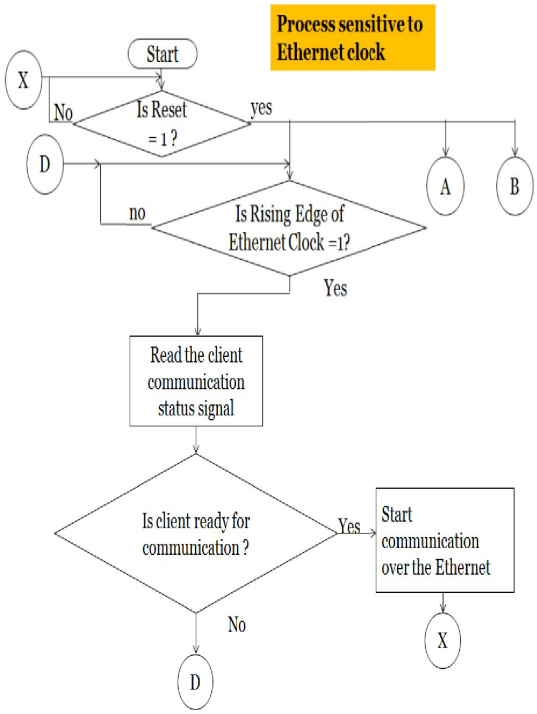

Fig. 6. Flow Chart for communication with the host PC, the client

and the third one in sensitive to the RAM Clock and buffers the image data in the DDR SDRAM. The Fig. 6,7 and 8 shows the flow chart for all the three processes:

V. Experimental Results

The Fig. 9 shows one of the frames of the AVI file received using the Image Acquisition application developed

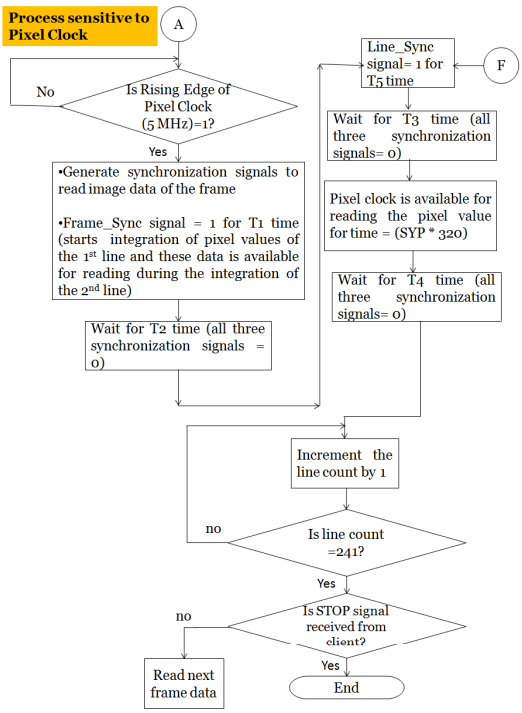

Fig. 7. Process for generating synchronous signals and reading the pixel data

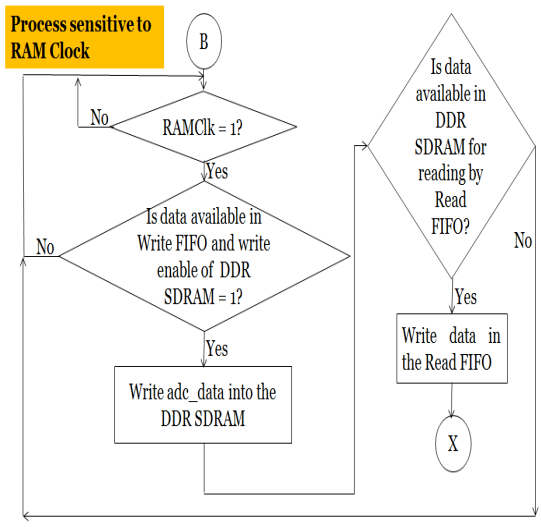

Fig. 8. Flow chart for buffering the image data in the DDR SDRAM

using LabVIEW™ for test data. The frame rate is 15 frames / second.

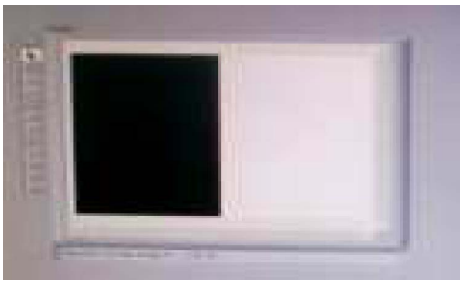

Fig. 9. Image of one of the frames of an AVI file generated using test data

The Fig. 10 shows one of the frames of the. The frame rate is 50 frames/second and the IR image is of a soldering iron.

Fig. 10. Image (one of the frames of an AVI file) of a Soldering Iron taken by the IR Camera

VI. Conclusion

By using the TCP/IP Offload Engine, the 7.3M-bytes/sec(50frames/sec) is transferred without the loss of any data. Such a high speed data transfer is supported by the ADC AD9420. It is capable of processing 10 mega samples of an analog signal per second. The IR sensor generates 76800*2*50= 7,500 K bytes per second. This much amount of IR raw data is transferred to host computer in real time by TOE Gig Expedite. Using the TOE on the embedded electronics at IR Camera side allows the computer to acquire the image data at such a high speed as the TCP/IP processing is taken care by it. The IR images are then stored as AVI files in the Computer.

VII. Future Scope

At present, this camera does not have any facility to perform the Non Uniformity Correction (NUC). The NUC can be due to the manufacturing defects in the IR sensor because of which when it is exposed to a black body, the image does produce zero greyscale values uniformly in the focal plane area. This defect can be taken care by applying the NUC algorithm.

REFERENCES

[1] W. Zhang, Z. Wei, X. He, P. Qiao and G. Liang, *The design of high speed image acquisition system over Gigabit Ethernet* Wireless Communications, Networking and Information Security (WCNIS), 2010 IEEE International Conference on, pp. 111-115, 2010.

[2] Y. Li, C. Wang, J. Zhou and Q. Liu, *Real-Time Infrared Laseer Measurement System Design and Development*, Software Engineering, 2009. WCSE '09. WRI World Congress on, vol. 1, pp. 435-439, 2009.

[3] H. Xiawoei, S. Qinglei and M. Changyun, *Acquisition board design of high-speed image data based on ARM and FPGA*, Computer Design and Applications (ICCDA), 2010 International Conference on, vol. 1, pp. 374-376, 2010.

[4] R. Ribalda, A. de Castro, G. Glez-de-Rivera and J. Garrido, *Open and Reconfigurable System on Chip Architecture with Hardware and Software Preprocessing Capabilities Used for Remote Image Acquisition*, Programmable Logic, 2008 4th Southern Conference on, pp. 167-172, 2008

[5] *Basic TCP/IP Communication in LabVIEW*,http://www.ni.com/white-paper/2710/en, Sep 06, 2006