Low Power Checks and Power Estimation at RTL Level.

Thesis Report

Submitted in Partial Fulfillment of the Requirements for the Degree of

MASTER Of TECHNOLOGY

IN

Very Large-Scale Integration Engineering

By

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May 2023

CERTIFICATE

This is to certify that the Thesis Project Report entitled “Low Power Checks and Power Estimation at RTL Level.” submitted by Mr. Patel Ayush Ashok(21MECV07) towards the partial fulfillment of the requirements for the award of a degree in Master of Technology(MTech) in thefield of Very Large-Scale Integration(VLSI) Engineering in Nirma University is the record of work carried out by him under our supervision and guidance. The work presented has reached a level that is required for being accepted for a related examination. The results embodied in this thesis project work to the best of our knowledge have not been submitted to any other University or Institution for the award of any degree or diploma.

Date: 22nd May

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TO WHOM SO EVER IT MAY CONCERN

This is to certify that Mr. Patel Ayush Ashok(21MECV07), a student of MTech in Very Large-Scale Engineering (VLSI) from the Institute of Technology, Nirma University. Also worked in Intel Corporation as a project trainee from 6 June 2021. During this period, he was found regular and has Worked on his project "Low Power Checks and Power Estimation at RTL Level," under my supervision.

He has worked with utmost dedication and a high level of engineering and analytical competence.

We wish him all the best in his future endeavors.

Date: 22nd May

Name of the External Guide: Bansal Virendra

Undertaking for Originality of the Work

I, Patel Ayush Ashok, Roll-No.21MECV07, give undertaking that the Thesis Project entitled "Low Power Checks and Power Estimation at RTL Level". submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in Very Large-Scale Integration(VLSI) Engineering of Nirma University, Ahmedabad 382481, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any other published work or any project report elsewhere; it will result in severe disciplinary action.

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Signature of Internal Guide :

Acknowledgment

A journey is easier when you travel together. Interdependence is certainly more valuable than independence. The result of the work in this thesis where I must go along with and support by many people. I express my gratitude to the people who supported me in this work.

With immense pleasure, I express my sincere gratitude, regards, and thanks to my supervisor Prof Piyush Bhatasana for his excellent guidance, invaluable suggestions, and continuous encouragement at all the stages of my research work. His time and effort in this project were the reason for all my success. I have been fortunate to have him as my guide as he has been a great influence on me, both as a person and as a professional.

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The chain of my gratitude would be incomplete if I would forget to thank the first cause of this chain, using Aristotle's words, The Prime Mover for showering His blessings on me always.

Name of the student: Patel Ayush Ashok.

Abstract

In the last many years power management has become the major problem when it comes to lower node technology, where static power dissipation is more than dynamic power dissipation. In nanometer technology, the power is an important issue as the technology node decreases the transistor number, the Speed of the performance, and leakage current increases so power dissipation will be more. Power can be optimized using different power-saving techniques like Power Gating, Multi-Voltage, Dynamic Voltage Frequency Scaling (DVFS), clock gating.

The low power verification tool uses a multi-voltage design and low power static verification rule checker which will check the functionality and verify whether the low power architecture is designed in a perfect manner and checks whether any electrical violation is found or not. Low power standard which is also known as Unified Power Format (UPF) makes ICs reliable, robust, and standardized and it needs to verify their functionality and behaviorally correctness which ensures that it follows IEEE 1801 low power standards.

Unified Power Format (UPF) comes into action when power intent information is not specified in Hardware Description Language (HDL). UPF specifies all power intent information in the design flow. Using UPF commands power management can be controlled by specific cells like isolation, retention, power switches, and level-shifter cells which can be checked by a low power verification tool. The Low Power Verification tool normally checks and verifies any missing cells in the design in the Design Stage and their connections in the Power/Ground stage and finally, it will debug the issues.

To estimate power at an early stage is more important before silicon, so that if power dissipation is high necessary step ‘s will take at initial stage only, for measuring accurate power number we are using Prime Power tool developed by Synopsys. This tool will generate the most accurate power number’s. Based on the power number’s designer will make necessary changes to lower down the power number.

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Chapter 1

1.1 Introduction

In this modern world, technology is developing at a very fast rate, and technology node is decreasing per the American businessman Gordon Moore the pioneer of intel has observed that the number of the transistor on a computer chip was doubling every 18 to 24 months and the size of IC's are shrinking too. The small size of an IC has many advantages, but its power density increases which leads to many concerns. An IC with a high-power density not only heats up the product but also becomes unstable early. Because of this issue, the IEEE 1801 low-power standards are formed to make the ICs reliable, robust, and standardized which will mitigate these issues. Once IC is designed, we need to verify it by verifying its functionality and behaviorally correct and ensure that it follows IEEE 1801 low power standard which is also known as Unified Power Format (UPF). This IEEE standard provides portable, specifications of low power which can be used in electronic products, design flow, analysis, and verification implementation flow.

As the node technology is even better every year and demand is also very high so power consumption is also increased. (i.e., the technology node, which is above 90 nm, dynamic power dissipation also increases compared to static power consumption. To decrease the dynamic power consumption, decreases average switching frequency, it is the amount of power consumed to transit a node from a 0 to 1 state or vice versa). With the technology node, which is below 90 nm, static power consumption is dominant compared to dynamic power consumption. Static power consumption is due to the result of leakage quiescent current (i.e., when there is no toggling of a node from HIGH to LOW and vice versa).

Low Power Verification tools are used for voltage-aware functional verification as a low power solution. Coverage for all advanced power management functions is done using an advanced Low Power Static-rule Checker. Low power techniques are used for advanced low power management as it is used in SOC designs. Low power Verification static lower checker can check and analyze all the error it performs 500 plus checks, gives maximum chip capacity, and process all the steps to perform overall low power static signoff. Low Power verification supports the IEEE standard

format known as Unified Power format and absolute static analysis for capturing the power intent, power state shift, and multi-rail macros of the low power design.

For estimating power at RTL level, we are using prime power tool.

The Synopsys Prime Power product family provides power analysis solutions that accurately analyze power dissipation of block-level and full-chip designs starting from RTL, through different stages in the design implementation process, and leading to power signoff.

Both Prime Power and Prime Power RTL provide accurate power analysis reports for designers to perform timely design optimizations to achieve power targets. Prime Power RTL leverages the Predictive Engine from the RTL Architect tool to enable RTL designers to analyze, explore, and optimize their RTL with confidence, improving power and energy efficiency, and shortening the design cycle.

During implementation and signoff, Prime Power provides accurate gate-level power analysis reports for SoC designers to make timely design optimizations and achieve power targets. Supported power analysis modes include average power, peak power, glitch power, clock network power, dynamic and leakage power, and multivoltage power; with activity from RTL and gate-level vectors from simulation, emulation, and vector less analysis. By closely integrating with the Primetime tool, the golden industry standardfor timing and signal integrity analysis and signoff, Prime Power expands the Primetime solution to deliver accurate dynamic and leakage power analysis and signoff for gate-level designs

1.2 Motivation

Low Power Verification static signoff tool provides the design report, intelligent process analysis, fast unified debug, support unified power format, fast and rapid outputs and performs overall checks in less time. Accurate issues and violations can be found in the design and low Power verification can be done using GUI to debug the design's violation.

Prime power tool is the most accurate tool to generate power number of an IP, it takes many input's to generate power number, so once we have power number at initial stage and if power dissipation is more than necessary steps will be taken by designer's to lower down the power number. Accurate issues and violations can be found in the design and low Power verification can be done using GUI to debug the warnings and errors

1.3 Objective

The main objective of the low power checks is to perform different kinds of checks on design like a functional check, power intent consistency check, structural check, power ground check, functional check, and signal corruption checks on UPF. There can be many power domains in the design which can be easily solved by a low power verification tool also it understands the power intent and can transform many power states to a lesser one, thus it reduces the effort which is involved in it and then verifies all the power states, transitions, and sequences.

The main objective of power estimation at RTL level is to have more accurate number's for an IP so if the power dissipation is more than expected than necessary changes will be taken at RTL level. Prime power tool generates the most accurate power number.

1.4 Problem Statement

There are two problem statements:

- How Low Power Verification performs various checks in synthesis and placement and route with following Functional check, Signal Corruption check, Power Intent Consistency Check, Structural checks, Power and Ground check. How it is used to pipe clean the UPF according to the IEEE standard 1801 according to these checks.
- How we will generate more accurate power numbers for an IP at an early stage.

1.5 Approach

- Checking signal corruption and continuing and performing various checks by Low Power verification tool and by debugging these signal and cells issues. Checking strategies and missing cells which will determine the properness of the UPF and netlist file.
- For prime power will check the list of warnings and error's thrown by the tool and will debug to get more accurate power numbers.

1.6 Scope of the Project

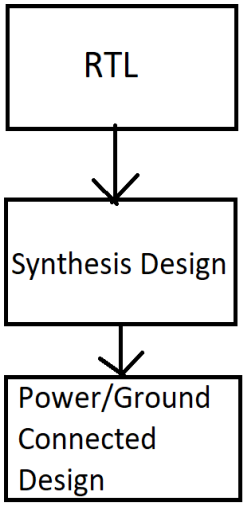
The Scope of the project is to reduce the issues/violations by reducing the run time and machine usage using the Low power verification (VCLP) Tool. And to remove all the warning and error generated by prime power tool so that whatever power number's that are generated by the tool will have the most accuracy.

Chapter 2

2 Literature review

2.1 Low Power verification Checks Flow

Low Power Verification performs different kinds of checks, here in Fig 2.1(a) shows a low power check where the first step is to check the RTL block which can be done using UPF consistency and signal corruption check, Synthesis design block can be checked using signal corruption, structural and functional check and Power/Ground connected block can be checked using signal corruption, structural, functional and PG check. At RTL Block, Low power verification helps in identifying the power intent issues in UPF early in the design life cycle and it will give clean UPF before initializing the design flow[3].



Low power Checks flow

Fig 2.1(a) Low Power Checks Flow

Low power verification takes in RTL like Verilog, VHDL, SVD, PG Netlist, or post-layout netlist of the design. Low Power verification requires standard Liberty (Library) files (.db. file), Low power verification read the Liberty DB file for timing information, annotates power connections, describes the design, and checks special cells for the Gate level netlist. It will take power intent which is in UPF. In the output, Low power verification generates log files, errors, and warning reports for the violation specified in reports which are related to the low lower static rule check. low power verification provides TCL as a basic physical system that helps to debug these violations. Low Power verification also helps to debug using low power verification GUI (Graphical User Interface) as shown in Fig 2.1(b)

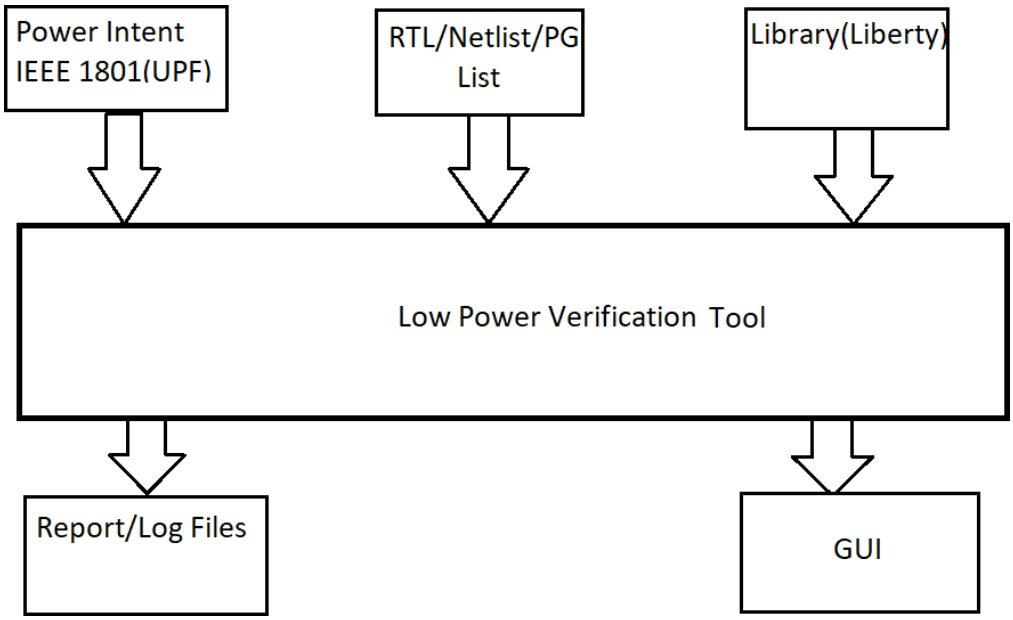


Fig 2.1(b) Low power verification Checks

The UPF is checked according to Fig 2.1 Low Power Check Flow, and these checks include:

2.1.1 Power Intent Consistency Checks

Performs syntax and semantic checks on the UPF that help to approve the consistency of the UPF before starting with the implementation.

2.1.2 Signal Corruption Checks

It detects the violation of power architecture at the gate-level netlist.

2.1.3 Structural Checks

Validates insertion and connection of special cells used in low power design such as isolation cells, power switches, level shifters, retention registers, and always-on cells throughout the implementation flow.

2.1.4 Power and Ground (PG) Checks

Check the PG consistency against the UPF specification for power network routing on physical netlists.

2.1.5 Functional Checks

Check and verify the correct functionality of isolation cells and power switches.

After low power verification GUI debug, violation reports are generated which include special cells, checking the connections, strategy, and missing of these special cells include.

2.2 Low Power Techniques

Low power technology is used to reduce the total power consumption in a system by means of reducing capacitive load and activity factor which will further reduce the switching component of the dynamic power they are classified as:

1) **clock gating:** It is used to reduce the dynamic power in the design. It is simply to turn off the design when it is not needed without affecting the functionality of the design.

2) **Multi-Voltage:** It is used to save the static power and dynamic power of the design. The chip is implemented with different supply voltages. Various functional blocks run at different supply voltages, and we can save the power losses by reducing the supply voltage.

3) **Dynamic voltage and frequency scaling:** By changing the voltage with the frequency we can reduce the power consumption. When a high operating is required the supply voltage is increased to attain a higher frequency.

4) **Multi Vth:** In the Multi threshold voltage technique use both Low Vth and High Vth cells. Use lower threshold gates or critical paths with higher threshold gates of the critical path. Using the Multi Vth technique performance can be improved without increasing power but fabrication complexity using multi-Vth cell can be increased. It also lengthens the design time. Improper optimization of the design may utilize lower Vt cells and hence could end up with increased power.

5) **Power Gating:** Power gating is used to reduce the consumption of the power by shutting off the current which is not used in the blocks. Thus, it saves overall power in the chip.

2.3 Special Power management cells:

Power management cells are the special cells that are used to manage the power distribution in the design through the Unified Power Format (UPF) file. These techniques use special cells which are power management cells. Power management command defines the characteristics of the instances of the power management cells used to implement and verify the power intent of the design. These power management cells solve the Voltage error, Voltage crossover, and power domain error. Power management cells are also known as Dual power rail Supply Cells as they have two sets of rails. Dual Power Rail has primary as well as secondary power rail to give power to these cells. These cells are:

1)Isolation Cell
2)Retention Cell
3)Power Switch Cell
4)Always-On Cell

2.3.1 Isolation Cell:

Isolation cells are also known as clamp cells. These are the special cells used in low power design. It is inserted by a synthesis tool for the isolation of the wires and buses crossing from the power gated domain to the always-on domain. Isolation cells are used to reduce the power dissipation in the design. The Power domain, which is off will not drive any output, so these outputs will act as floating nodes and problems can occur for active power domains which will get floating nodes as input. It would lead to a crowbar current that exceeds the defined limit which would affect the functionality of the power-up domain. 'AND' gate and 'OR' gates are the types of clamp cells that are used when isolation cells pass Unknown signal 'X', which will lead to leakage of power. Hence to pass a Signal 'HIGH' or '1', it needs an OR gate and if it passes a Signal 'LOW' or '0', it needs AND gate as an isolation cell.

Consider that design has two power domains PD_1 and PD_2 and signal S1 d from PD_1 to PD_2. When both the power domain is powered-up, the signal has either 0 or 1 value. But when the power domain PD_1 is powered down and PD_2 is powered up. S1 value will become unknown. This corrupts the power-up logic in the PD_2 domain. To avoid this, the design engineer placed isolation cells between the outputs of the powered-down domain and the input of the powered-up domain.

During normal working conditions, an isolation cell works as a buffer. When PD_1 is powered down, the isolation cells clamp their output value to either 0 or 1 value. The isolation cell has an isolation enable signal that determines whether the isolation cell should provide isolation or work as a buffer.

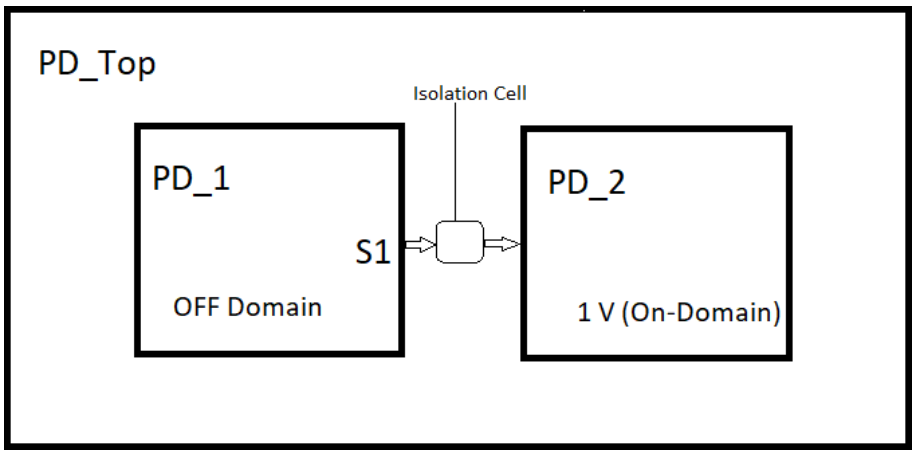


Fig 2.3.1(a) Block diagram of Isolation cell Function.

Without an isolation cell, there will be leakage of power when the MOSFET gate receives a don't care signal/Unknown signal (X). When to pass '0', AND gate is used as shown in fig 2.3(b), and to pass '1', Or gate is used as shown in fig 2.3(c).

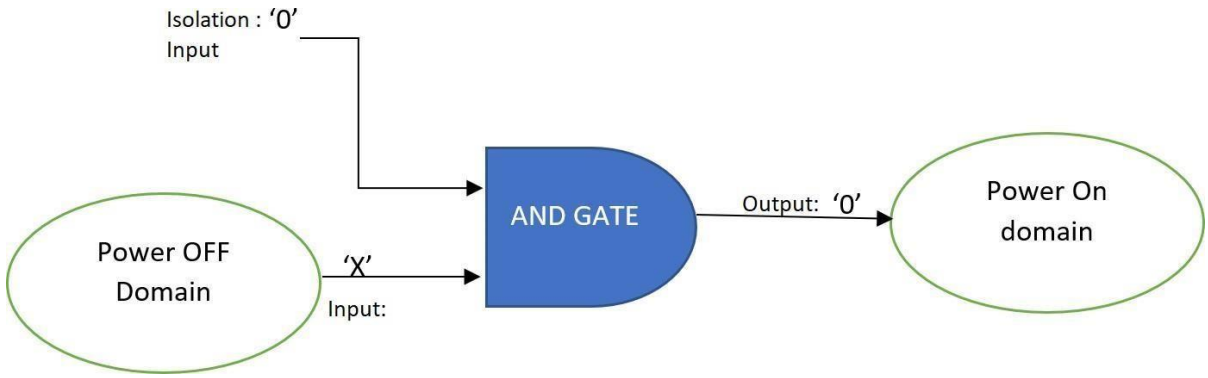


Fig 2.3.1(b) Type 'LOW' Signal transmission using 'AND' gate as Isolation cell.

Truth Table of ISOLATION Cell		
Isolation Input	Input	Output
0	X	0
1	X	X
X	1	X
X	0	0

Table no 2.3(a) Truth Table for isolation cell using AND GATE retaining or clamp '0'

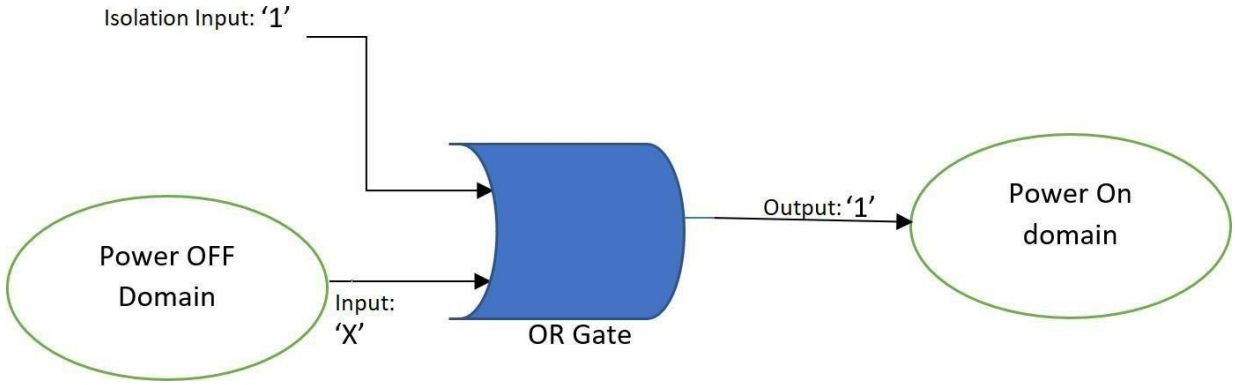


Fig 2.3.1(c) Type 'HIGH' Signal transmission using 'OR' gate as Isolation cell.

Truth Table of ISOLATION Cell		
Isolation Input	Input	Output
0	X	X
1	X	1
X	1	1
X	0	X

Table no 2.3(b) Truth Table for isolation cell using OR GATE retaining or clamp '1'

2.3.2 Retention Cell:

Retention cells are the special cells used to store information which is in the form of binary format. It can hold its internal state/data in the register which is also known as the shadow register before powering down. When the primary power supply is cut off/Shut down it can retain its state when power is switched on again. The best example for retention cell is Master-Slave alive Flip flop. It consists of a Master latchand a Slave latch whose output depends on a Negative/positive clock. The Slave latch stores the data when primary power is switched off in the retention operation. The mainpower of the latch comes from the main power rail of the "ALWAYS-ON" cell. State saving latch is implemented with a high threshold transistor to decrease the power dissipation and this power is active even in power-down mode. The control of the retention cell operation is done by the "SLEEP" signal. States in the register in a power domain should be retained when their power supply is removed. Retention cells are always on so they always absorb power. It is generally a low leakage cell. Low Threshold cells are high-performance cells whose power comes from a normal supply it can be latch/regular Flip Flop.

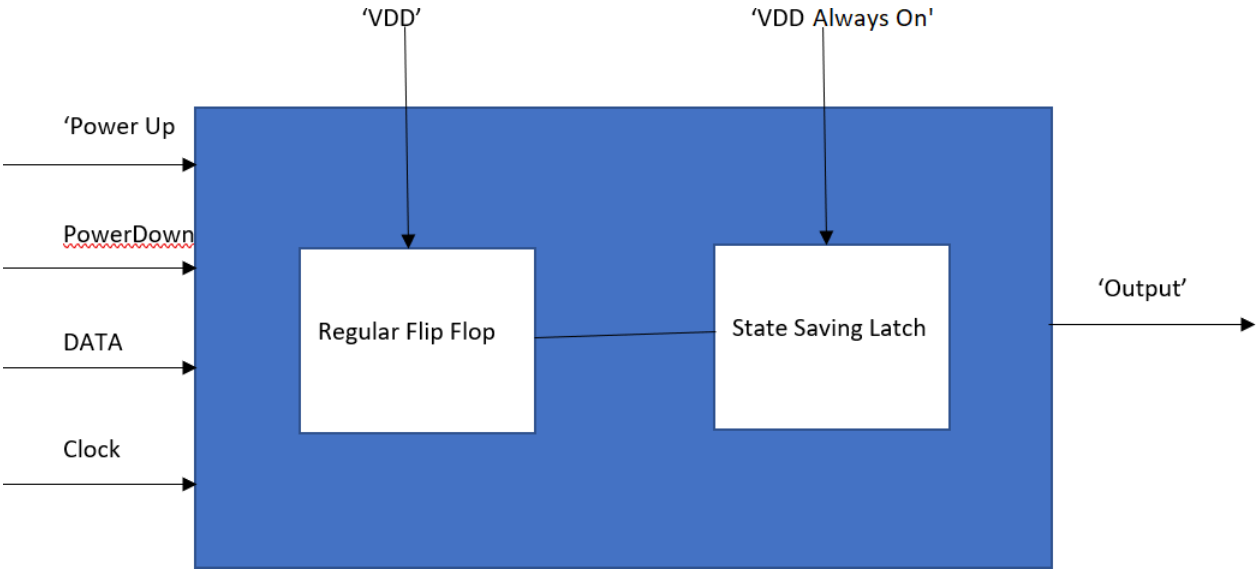


Fig 2.3.3(a) Simple block diagram of Retention Cell

The State saving latch is not active in ‘normal mode’. Before power down of the regularflop but the value of the regular flip flop will transfer its value to the state latch before power down. The power of regular flip flop is shut down but the state saving register ispowered up for retention of states.

2.3.3 Power Switch

Power Switch cells are used for Power Gating in the design by powering off the portion of the design. When any of the subblocks are not needed or not in use it can be shut down using a power switch cell, scope command is used to switch off the voltage domain. Header (PMOS) and Footer (NMOS) transistor of fixed size are used as Power Switch. When Power Switch is needed to work then the sleep signal is given the signal ‘LOW’ to activate the power switch of the PMOS transistor. The power switch is inserted in the column as well as in a ring manner.

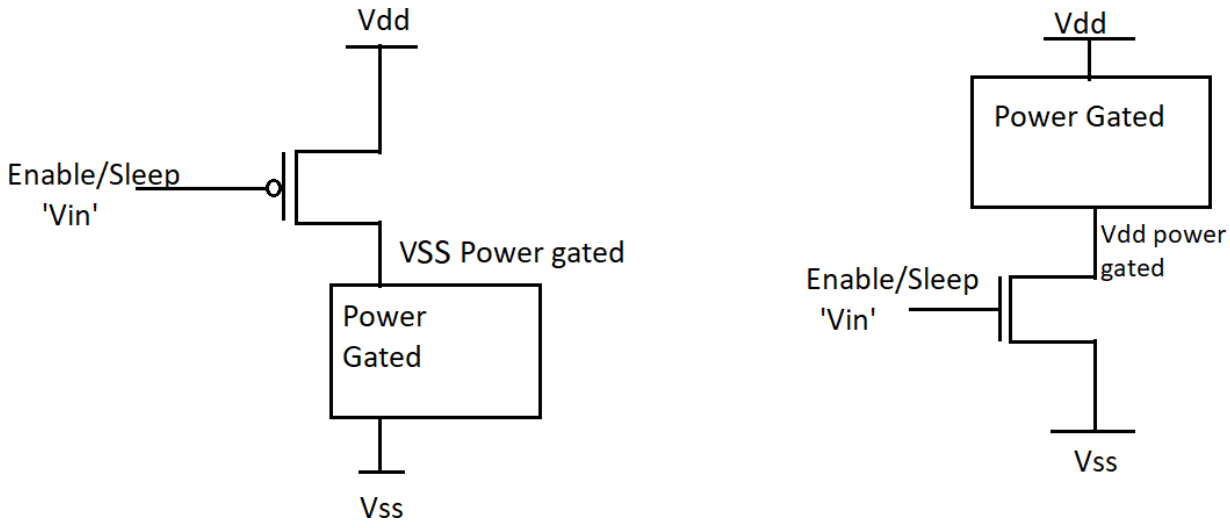


Fig 2.3.4(a) MTCMOS Power Switch used for Power Gating.

Consider PMOS with an MTCMOS power switch at drain which will control the power gating by powering off the MOSFET using power gated logic. This Multi Threshold CMOS are of two types 1) Low Voltage Threshold(LVT) 2)High Voltage Threshold (HVT)
Short circuit power can be reduced by a Low Voltage Threshold during normal mode and leakage power can be reduced by a High Voltage Threshold during off mode.

2.3.4 Always-On Cell

Always on the cell cannot be switched off. Generally, buffer and inverters are used as Always-On cells. Logic cells should be powered on irrespective of power domain is switched off. The power domain which can be switched off is known as the power down domain. The logic inside the cell is used to transfer signal in the off domain while Source and Sink domains are in the 'ON' state.

Always on cell are of two types 1) Single power rail supply 2) Dual Power rail supply. Single Rail Power cells: They contain only single power in inverters and buffers from the standard cell libraries. Dual Rail Power cells: It contains a dual power supply for invertersand buffers and it is used for always-on cells.

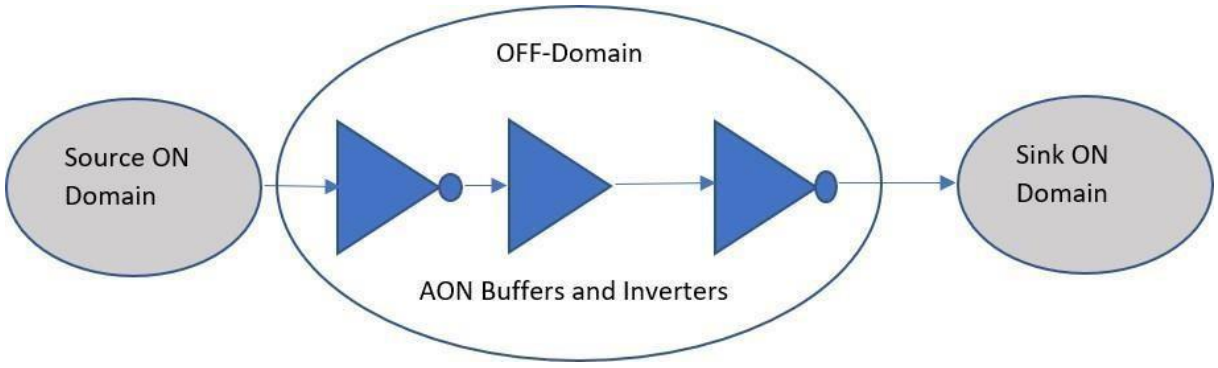


Fig 2.3.5(a) AON buffer & Inverter are in off domain for signal transfer between on domain

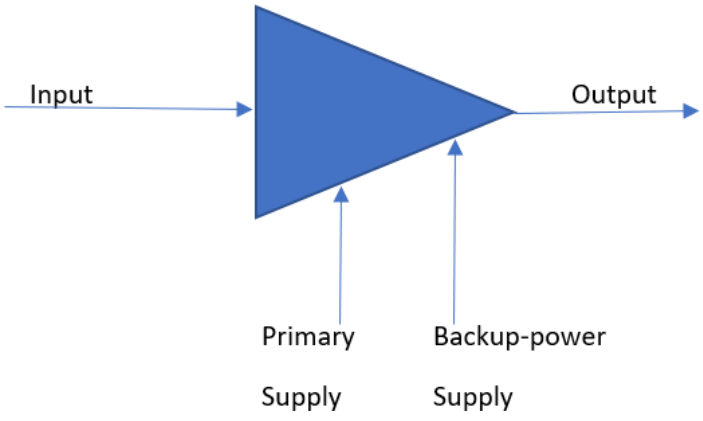


Fig 2.3.5(b) Dual Power Rail Supply AON Cell

The dual power rail supply consists of two powers: primary power and secondary power.Primary power is always on power while secondary power can be switched off and turned on according to RTL Engineer. While Single Power rail supply only consists of primary power.

Chapter 3

3 Low Power Verification

3.1 Low Power Verification Flow Design:

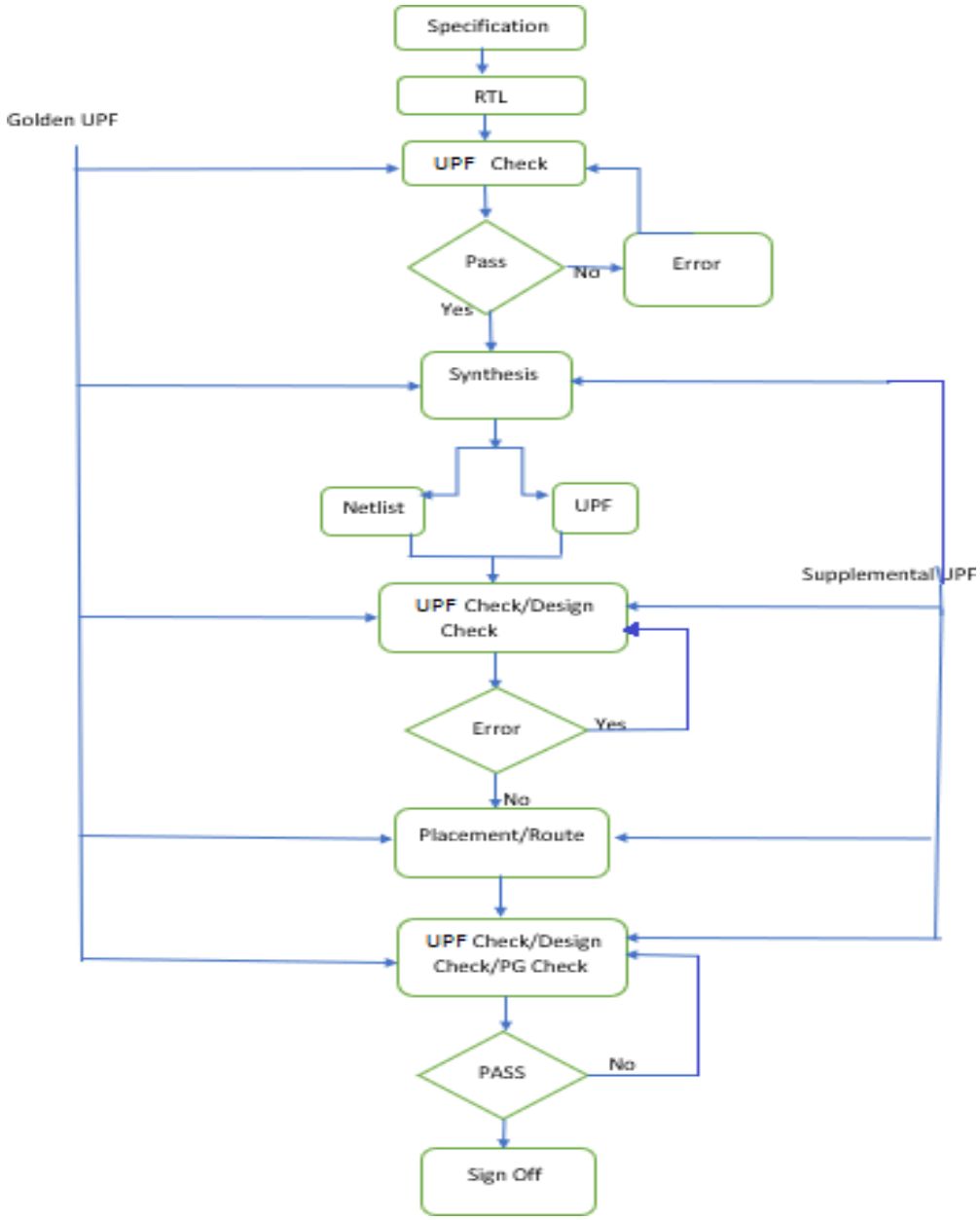


Fig 3(a) Low Power Verification Design Flow block diagram

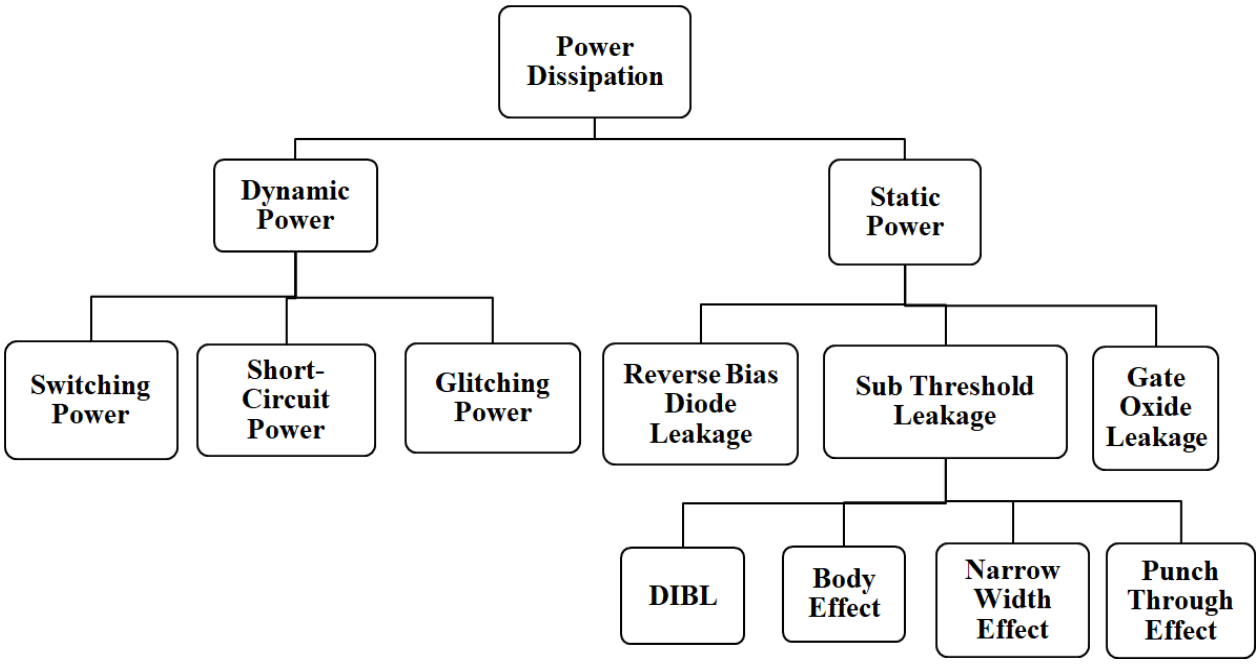
In Low Power verification design Flow, it starts with the specification of the design specification including area, power, and performance. Register Transfer Level (RTL) block tells about how the data is transferred from one register to another register. This data is operated using Boolean logic expression when transferred to different registers with each clock cycle. This process is done using high-level codes such as Verilog and VHDL and these files are accepted by the synthesis tool. RTL is added with UPF. It defines the power architecture. It ensures that the design will work properly under a power management unit (PMU) with defined power architecture then is converted to gate-level netlist. Here Golden-UPF comes with RTL. UPF file is used in various blocks in Low power verification design flow such as synthesis, placement, and route with various low power verification designs and PG checks. UPF is checked before the synthesis step, to check the quality of the UPF and its errors of it. Low Power Verification checks are performed at this stage. It is then transferred to the synthesis stage where low power synthesis is performed by the compiler. Synthesis normally converts the RTL to the gate-level netlist. All other low power information is written in Supplemental UPF by the design compiler. This combined Supplemental UPF and Golden UPF together are used for “UPF check” and “Design Check” using low power verification tool to check insertion of the cell is correct or not during synthesis. Then both are passed to PNR (Placement and Route) together with a synthesized netlist where “UPF/low power checks”, “Design Checks” and “PG Checks” are performed using the UPF file and physical netlist. The last stage is Sign-Off it is also known as tape out where our design is ready and can go for physical implementation.

Chapter 4 Power Consumption in digital design.

For power analysis, your Synopsys library must contain power models for all the cells. The NLPM power models contain tables that Prime Power uses to calculate leakage power and internal power. Prime Power calculates switching power based on the voltage, netlist capacitance, and switching of the nets. The leakage and dynamic power calculation results are used for peak power analysis and average power analysis.

Prime Power provides an automated mechanism to generate a power model in which power data for IP blocks or large blocks are saved. The power model generated by the tool can be instantiated for a faster chip-level power analysis and is based on the Extracted Timing Model Extracted Timing Model (ETM) feature of the Primetime tool. The power model is generated by incorporating power information into the ETM

Power Consumed in digital design



4.1 Dynamic Power Dissipation

Switching Power

The switching power of a driving cell is the power dissipated by the charging and discharging of the load capacitance at the output of the cell. The total load capacitance at the output of a driving cell is the sum of the net and gate capacitances on the driving output. Because such charging and discharging is the result of the logic transitions at the output of the cell, switching power increases as logic transitions increase. Therefore, the switching power of a cell is a function of both the total load capacitance at the cell output and the rate of logic transitions.

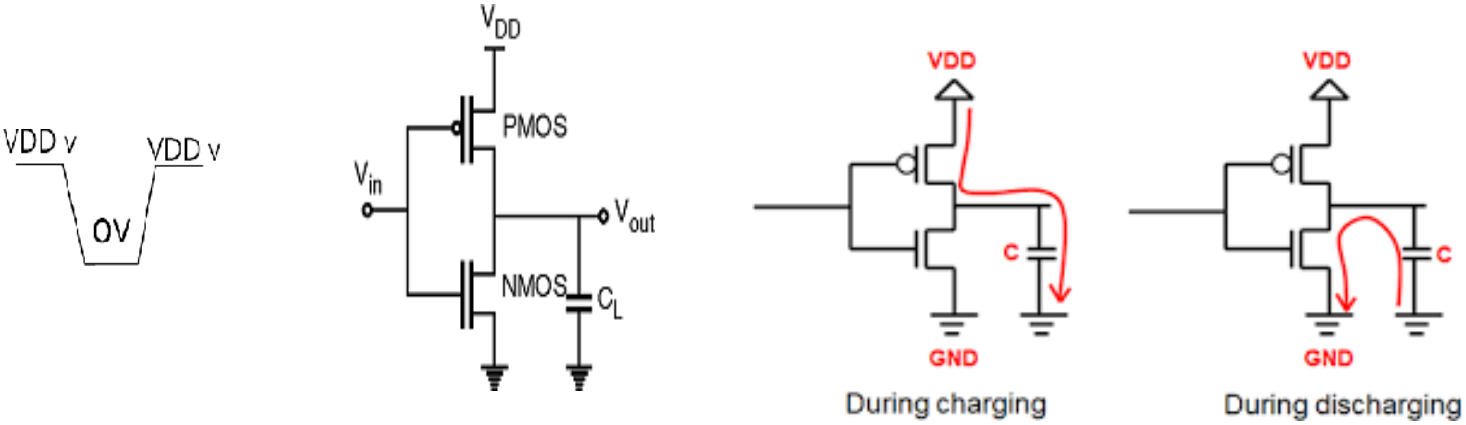


Fig 4.1(a) Switching Power block diagram

Total Power Dissipated = Cl*Vdd^2 $P_{0\to1}$*f

Short Circuit Power

Short-circuit power is the power dissipated by an instantaneous short-circuit connection between the supply voltage and the ground at the time the gate switches state. Finite slope of an inputsignal causes a direct path from VDD to GND for short time period. Short circuit current flows for short time duration when both the transistors are in saturation region.

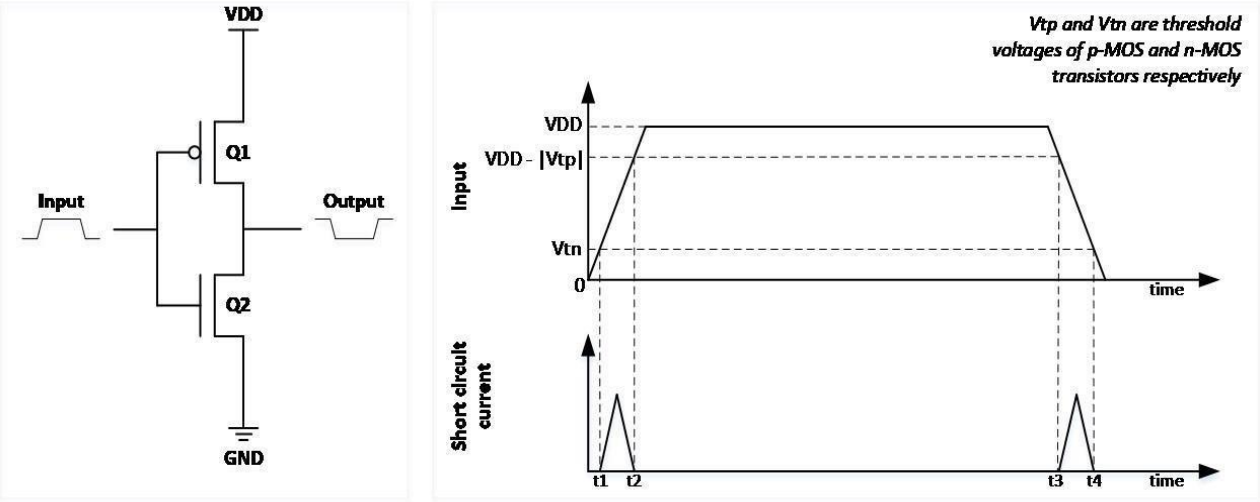


Fig 4.1(b) Short Circuit Power block diagram

$P_{avg}(\text{short circuit}) = 1/12.k.\tau r.F_{clk}.(Vdd-2Vt)^3$.

Glitching Power

All the logic gates will have some finite delay associated with them, and because of thatdelay only glitch occurs. Example: Let A, B, C are the input's changing from 010 to 111.

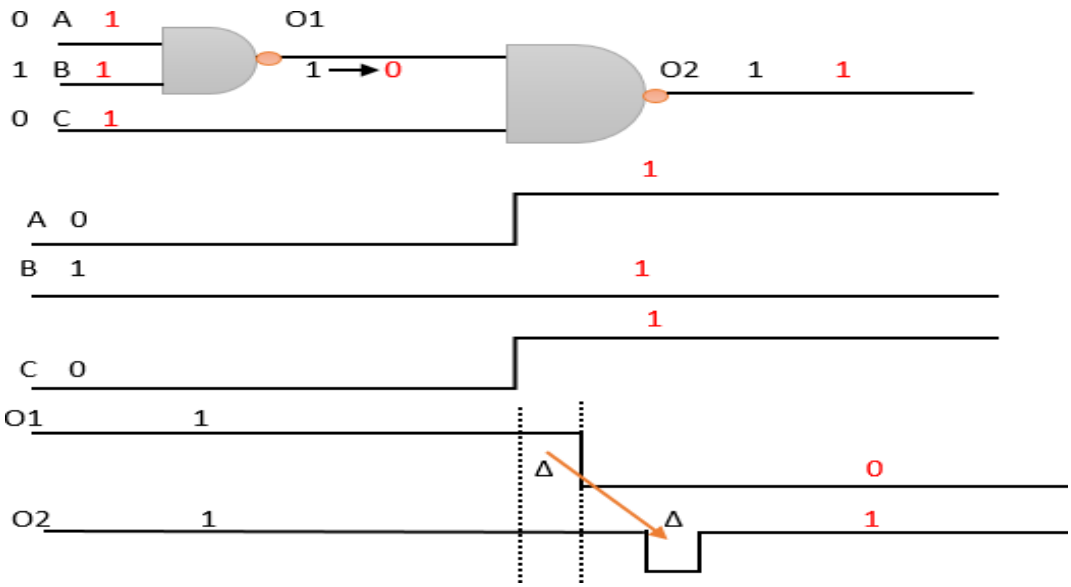


Fig 4.1(c) Glitching Power block diagram

4.2 Static Power Dissipation.

When the circuit is not in an active mode of operation, there is static power dissipation due to various leakage mechanisms. In deep-submicron devices, these leakage currents are becoming a significant contributor to power dissipation of CMOS circuits. Figure 6.17 illustrates the seven leakage mechanisms. Here, *I*1 is the *reverse-bias* p–n *junction diode leakage current*; *I* 2 is the reverse-biased p–n junction current due to *tunneling* of electrons from the valence bond of the *p* region to the conduction bond of the n region; *I*3 is the *subthreshold leakage current* between the source and the drain when the gate voltage is less than the threshold voltage *V*t; *I*4 is the *oxide-tunneling current* due to a reduction in the oxide thickness; *I*5 is gate current due to *hot-carrier injection* of elections; *I*6 is the *GIDL current* due to a high field effect in the drain junction; and *I*7 is the *channel punch-through current* due to the close proximity of the drain and the source in short-channel devices. These leakage components are discussed in the following subsections.

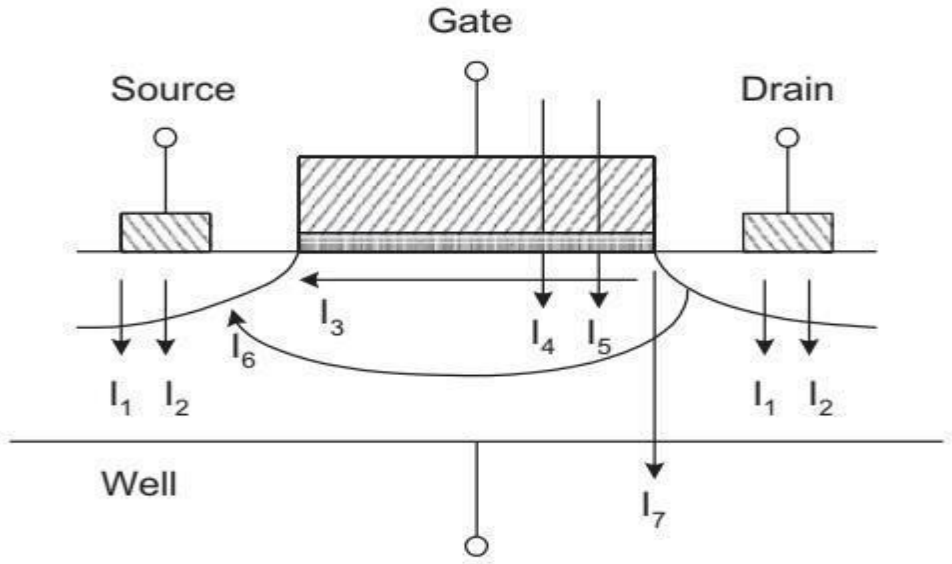


Fig 4.2(a) Leakage power block diagram

P-N Junction Reverse Bias Current.

Let us consider the physical structure of a CMOS inverter. As shown in the figure, source–drain diffusions and n-well diffusions form parasitic diodes in the bulk of silicon substrate. As parasitic diodes are reverse-biased, their leakage currents contribute to static power dissipation. The current given by

$$I_{\text{rdlc}} = AJ_{\text{s}}\left[\text{e}^{-\frac{qV_{\text{d}}}{nKT}} - 1\right],$$

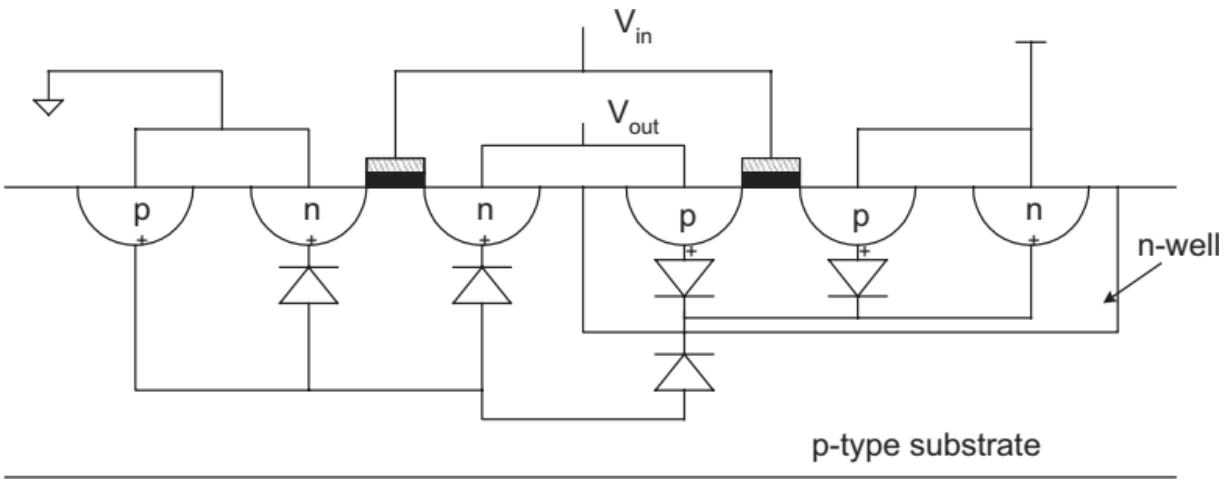


Fig 4.2(b) Reverse bias current block diagram

The leakage current approaches *I*s, the reverse saturation current even for a small reverse-biased voltage across the diode. The reverse saturation current per unit area is defined as the current density *J*s, and the resulting current is approximately *I*L=*A*D ·*J*s, where *A*D is area of drain diffusion. For a typical CMOS process, *J*s ≈ - 1 5pA/ m μ 2 at room temperature, and the *A*D is about 6 μm2 for a 1.0-μm minimum feature size. It leads to a leakage current of about 1 fA per device at room temperature. The reverse diode leakage current *I*rdlc increases significantly with temperature. The total static diode leakage current for *n* devices is given by, and the total static power dissipation for *n* devices is equal to.

$$I_{rdlc} = \sum_{i=1}^{n} I_i$$

$$P = V_{\text{dd}} \cdot \sum_{i=1}^{n} I_i.$$

Band to Band Tunneling Current.

When both n regions and p regions are heavily doped, a high electric field across a reverse biased p–n junction causes a significant current to flow through the junction due to tunneling of electrons from the valence band of the p region to the conduction band of n region. This is illustrated in Fig. 6.19. It is evident from this diagram that for the voltage drop across that junction should be more than the band gap.

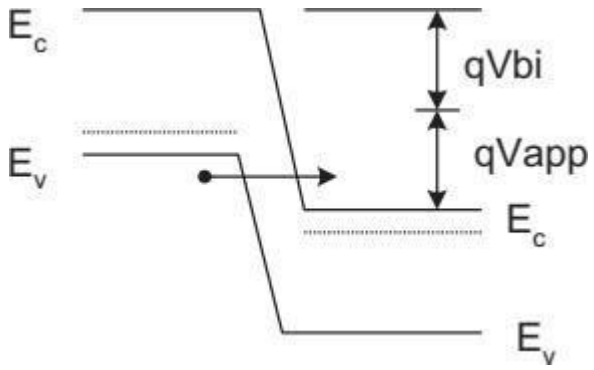


Fig 4.2(c) Band to band tunneling block diagram

Sub – Threshold Leakage Current.

The subthreshold leakage current in CMOS circuits is due to carrier diffusion between the source and the drain regions of the transistor in weak inversion, when the gate voltage is below V_t. The behavior of an MOS transistor in the subthreshold operating region is similar to a bipolar device, and the subthreshold current exhibits an exponential dependence on the gate voltage. The amount of the subthreshold current may become significant when the gate-to-source voltage is smaller than, but very close to, the threshold voltage of the device. The sub threshold current is given by

$$I_{stlc} = Ae^{\frac{q}{N'KT}(V_{gs}-V^{th})}\left(1-e^{\frac{-qV_{ds}}{kT}}\right)$$

$$= \mu_0 c_{ox}\frac{W}{L}(m-1)(V_T)^2 \times e^{(V_g-V_{th})/mV_t} \times \left(1-e^{-V_{ds}/V_T}\right)$$

Various mechanisms which affect the subthreshold leakage current are:

- Drain-induced barrier lowering (DIBL)
- Body effect
- Narrow-width effect
- Effect of channel length and *V*th roll-off
- Effect of temperature

Chapter 5. Prime Power for Power Estimation.

The Synopsys Prime Power product family provides power analysis solutions that accurately analyze power dissipation of block-level and full-chip designs starting from RTL, through different stages in the design implementation process, and leading to power signoff.

Both Prime Power and Prime Power RTL provide accurate power analysis reports for designers to perform timely design optimizations to achieve power targets. Prime Power RTL leverages the Predictive Engine from the RTL Architect tool to enable RTL designers to analyze, explore, and optimize their RTL with confidence, improving power and energy efficiency, and shortening the design cycle.

During implementation and signoff, Prime Power provides accurate gate-level power analysis reports for SoC designers to make timely design optimizations and achieve power targets. Supported power analysis modes include average power, peak power, glitch power, clock network power, dynamic and leakage power, and multivoltage power; with activity from RTL and gate-level vectors from simulation, emulation, and vector less analysis. By closely integrating with the Primetime tool, the golden industry standard for timing and signal integrity analysis and signoff, Prime Power expands the Primetime solution to deliver accurate dynamic and leakage power analysis and signoff for gate-level designs.

Prime Power gate-level analysis supports two types of power analysis modes—averaged and time-based. In each of the modes, the tool supports various options to suit different types of designs and applications. To perform power analysis for a design, select the required power analysis mode and the specific options supported of the mode.

5.1 Power Analysis Input's

- Prime Power requires the following data for performing power analysis:

  Logic library: A cell library containing timing and power characterization information for each cell. The supported formats are nlpm and ccs for timing data, and nlpm for power data.
- Gate-level netlist: A flat or hierarchical gate-level netlist in Verilog, VHDL, or Synopsys database format, containing leaf-level instantiation of the library cells.
- Design constraints: An SDC file containing design constraints to calculate the transition time on the primary inputs and to define the clocks.
- Switching activity: The design switching activity information for averaged power analysis or accurate peak power analysis. The switching activity information can be specified in an event file in the VCD for FSDB format.

  Net parasitic: A parasitic file (SPEF) containing net capacitances for all the nets.
- UPF file.

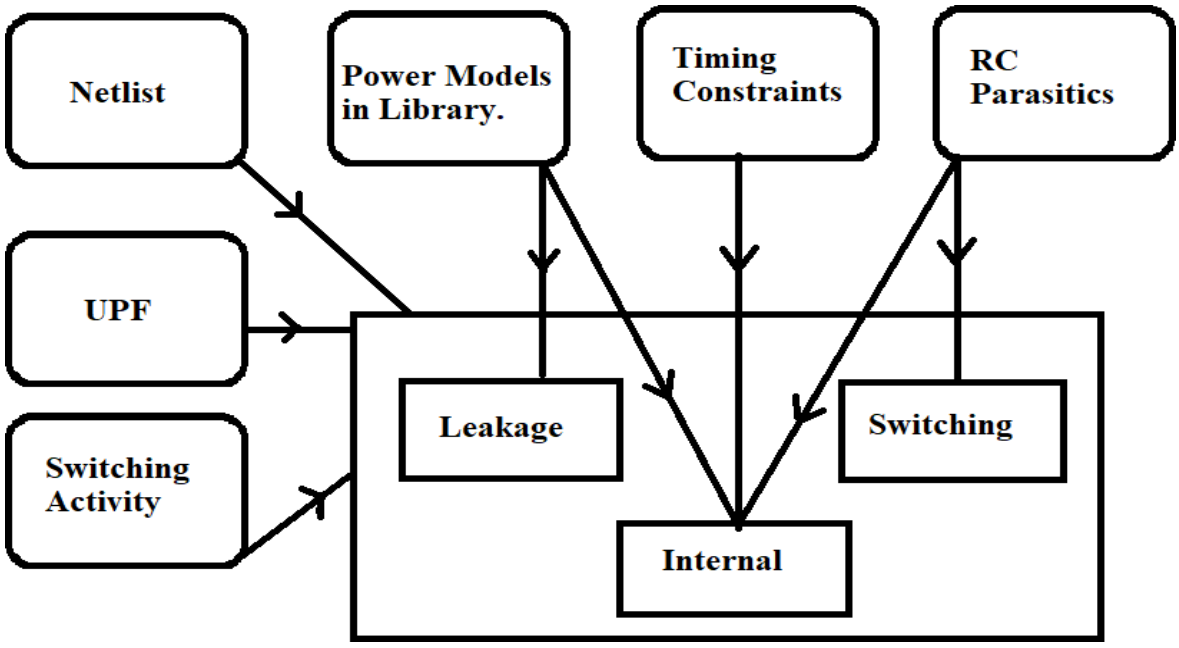


Fig 5.1(a) Input to prime power block diagram

5.2 Inputs and Outputs of Power Analysis.

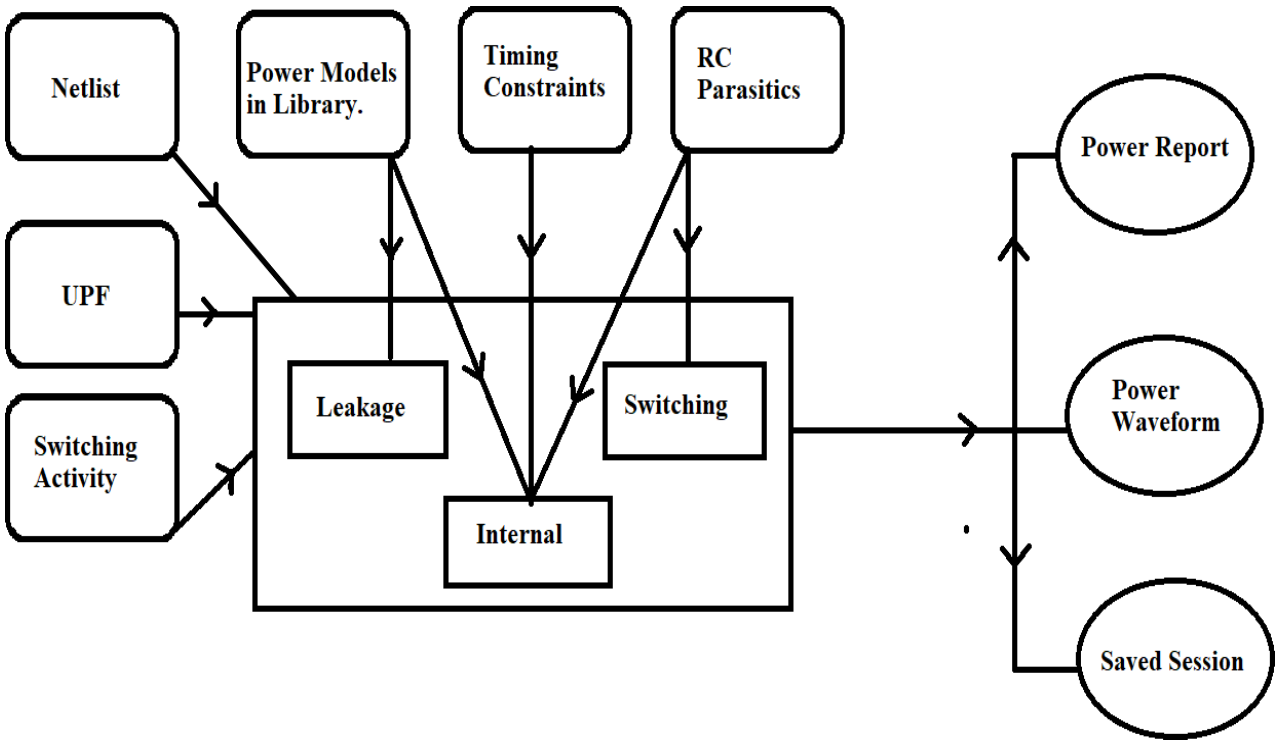


Fig 5.2 Input and output to prime power block

5.3 Power Analysis Modes.

There are two types of power analysis modes supported in prime power.

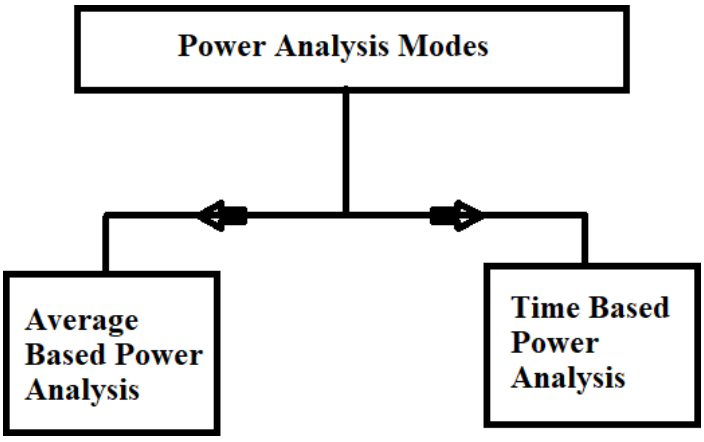


Fig 5.3 Power Analysis Mode block diagram

In the averaged power analysis mode, the tool calculates average power based on the toggle rates. The sources of annotated activity can be the default toggle rates, user defined switching activity, SAIF files, or VCD files generated from simulation. In the averaged power mode, the switching activity consists of toggle rates and static probabilities. The accuracy of the power analysis results depends on the accuracy of the switching activity values. Therefore, the switching activity obtained from the RTL or gate-level simulation must be annotated correctly. The tool supports the annotation of simulation-based switching activity file formats: VCD, FSDB, VPD, and SAIF. If activity files are not available, use the user-defined switching activity commands to provide realistic activity for accurate analysis results.

In time-based power analysis mode, you can annotate the switching activity files for calculating power. In this mode, the tool calculates the power per event to generate power waveforms over time, as well as the averaged power. Based on the type of event-based switching activity file provided, the tool performs instantaneous peak power analysis. In the time-based power analysis mode, Prime Power uses the events in the event-based switching activity file to calculate the power per event. It supports both RTL and gate-level activity files. When RTL-based switching activity files are provided, the tool propagates the RTL events per clock cycle to determine the activity on the non-annotated nets. For both types of event files, the tool can accurately identify the related pin for each event to calculate power per event.

Chapter 6. Results

6.1 Unified Power Format Reports.

VCLP run generate log file, UPF compressed report and UPF uncompressed report.

ERROR_COUNT	:	1
WARNING_COUNT	:	2
DESIGN_READ_ERROR_VIOLATION_COUNT	:	3
DESIGN_READ_WARNING_VIOLATION_COUNT	:	4
LP_ERROR_VIOLATION_COUNT	:	5
LP_WARNING_VIOLATION_COUNT	:	6
START/FINISH TIME	:	

Management Summary

```
14
15  ------------------------------------------------------------------------------
16  Management Summary
17  ------------------------------------------------------------------------------
18  Stage  Family                Errors  Warnings     Infos    Waived
19  -----  -------------------  --------  --------  --------  --------
20  UPF    DesignFeedthrough          0         0       150         0
21  UPF    Isolation                  0         0         0         4
22  UPF    PowerSwitch                0         0         0         1
23  UPF    Retention                  0         0         0         2
24  UPF    UpfConsistency             0         1         0         0
25  -----  -------------------  --------  --------  --------  --------
26  Total                             0         1       150         7
27
```

Tree Summary.

```
-------------------------------------------------------------------------
Tree Summary
-------------------------------------------------------------------------
Severity  Stage  Tag                              Count      Waived
--------  -----  -------------------------------  -----  ----------
error     UPF    ISO_STRATCONTROL_GLITCH              0           1
error     UPF    ISO_STRATEGY_MISSING                 6           0
error     UPF    ISO_STRATMISSING_NOBOUNDARY          2           0
error     UPF    PSW_MAP_MISMATCH                     1           0
error     UPF    RET_MAP_MISMATCH                     0           1
error     UPF    RET_STRATCONTROL_GLITCH              0           1
```

Run Summary.

```
|                                    RUN SUMMARY                                    |
+---------+-----------+-----------+-----------+-----------+-------------+-------------+---------------+
| Stage   | Flow Error | Tool Error | Total Fatal | Total Error | Flow Warning | Tool Warning | Total Warning |
+---------+-----------+-----------+-----------+-----------+-------------+-------------+---------------+
| vclp_run |         0 |         0 |         0 |         0 |           3 |          55 |            58 |
'---------+-----------+-----------+-----------+-----------+-------------+-------------+---------------'
```

Report_UPF

The command report_upf will show the design top name which is the main project. It generates the power intent information after it reads the UPF file. By report_upf command, one can find how many isolation instances, a level shifter, retention, power switch, and multi-rail macros instance are there in the UPF file similarly by using report_design one can get knowledge about the design and library file.

Read upf	
Design top:	Design top name
Isolation instances:	The total number of isolation instances used
Level Shifter Instances:	The total number of Level Shifter instances used
Retention instances:	The total number of retention instances used
Power Switch instances:	Total number of Power switch instances used
Multirail macro-Instances:	The total number of Multi rail macro instances used
Total Instances:	Total number of all the instance
Crossovers:	Total number of crossovers
Merged power states:	The number of power states merged

6.2 Prime Power Reports

Read_fsdb.

```
============================================================================
Summary:
Total number of nets = 1625
Number of annotated nets = 437 (26.89%)
Total number of leaf cells = 1339
Number of fully annotated leaf cells = 114 (8.51%)
============================================================================
```

The number of annotated nets is the number of nets for which switching activity is specified in the VCD file. The total number of leaf cells is the number of leaf cells in the design. The number of fully annotated leaf cells is the number of leaf cells in the design for which switching activity is annotated for all the leaf cell pins

Report Power.

```
********************************************
Report: Time Based Power
Design: mac
...
********************************************
  Attributes
       i  -  Including register clock pin internal power
       u  -  User-defined power group
Power            Internal   Switching   Leakage    Total
Group            Power      Power       Power      Power   (     %)  Attrs
--------------------------------------------------------------------------
clock_network    7.133e-04 0.0000000  0.0000000   7.133e-04(19.43%)   i
register         4.703e-04 1.095e-04  6.660e-08   5.799e-04(15.80%)
combinational    8.964e-04 1.208e-03  1.836e-07   2.104e-04(57.33%)
sequential       5.289e-05 2.200e-04  9.163e-09   2.729e-04( 7.43%)
memory           0.0000    0.0000     0.0000      0.0000(0.00%)
io_pad           0.0000    0.0000     0.0000      0.0000(0.00%)
black_box        0.0000    0.0000     0.0000      0.0000(0.00%)
--------------------------------------------------------------------------

Net Switching Power  = 1.537e-03 (41.88%)
Cell Internal Power  = 2.133e-03 (58.11%)
Cell Leakage Power   = 2.594e-07 ( 0.01%)
 ---------------------------------------
Total Power          = 3.670e-03 (100.00%)
---------------------------------------

X Transition Power   = 2.171e-07
Glitching Power      = 2.942e-05
Peak Power           = 0.0970
Peak Time            = 1956
```

Report of five worst power at a time instance.

```
# Power (uW)       Time (ns)
------------------------------
  2.1                50.2
  1.9                10.7
  1.8                80.0
  1.7                45.0
  1.5                20.1
```

Switching Activity Report.

```
****************************************
Report : Switching Activity

Design : ish_main_top
Version: T-2022.03
Date   : Sat Jan 21 06:31:59 2023
****************************************

 Switching Activity Overview Statistics for "ish_main_top"
```

Object Type	From Activity File (%)	From SSA (%)	From SSA Force (%) Annotated	From SSA Force (%) Implied	From SCA (%)	From Clock (%)	Default (%)	Propagated(%)	Implied(%)	Not Annotated(%)	Total
Nets	494546(53.22%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	251896(27.11%)	12147(1.31%)	170679(18.37%)	929268
Nets Driven by											
Primary Input	1679(94.49%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	98(5.51%)	1777
Tri-State	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0
Black Box	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0
Sequential	123528(99.92%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	92(0.07%)	0(0.00%)	8(0.01%)	123628
Combinational	368506(46.22%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	246083(30.86%)	12147(1.52%)	170573(21.39%)	797309
Memory	408(100.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	408
Clock Gate	425(6.92%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	5721(93.08%)	0(0.00%)	0(0.00%)	6146

 Static Probability Overview Statistics for "ish_main_top"

Object Type	From Activity File (%)	From SSA (%)	From SSA Force (%) Annotated	From SSA Force (%) Implied	From SCA (%)	From Clock (%)	Default (%)	Propagated(%)	Implied(%)	Not Annotated(%)	Total
Nets	494546(53.22%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	251896(27.11%)	12147(1.31%)	170679(18.37%)	929268
Nets Driven by											
Primary Input	1679(94.49%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	98(5.51%)	1777
Tri-State	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0
Black Box	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0(0%)	0
Sequential	123528(99.92%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	92(0.07%)	0(0.00%)	8(0.01%)	123628
Combinational	368506(46.22%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	246083(30.86%)	12147(1.52%)	170573(21.39%)	797309
Memory	408(100.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	408
Clock Gate	425(6.92%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	5721(93.08%)	0(0.00%)	0(0.00%)	6146

Chapter 7

Conclusion.

Low power verification tools will reduce UPF complexity, machine usage, and run time is very less. It can handle large databases and it also supports GUI. Low Power verification helps us to identify and report low-power issues and provide a bug-free design. Power estimation at RTL level using most accurate tool will help us to know how much amount of power is dissipating, is the power dissipated is more than the requirement than necessary steps will be taken by designer to reduce the power and meet requirements.

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