“Wide range LDO (Low DropOut) design for DCDC converter”

Major Project Report

Submitted in fulfilment of the requirements
for the degree of

MASTER OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

(VLSI Design)

By

Ruchi Shah

(21MECV17)

Department of Electronics and Communication Engineering,
Institute of Technology,
Nirma University,
Ahmedabad 382 481

Declaration

This is to certify that

a. The thesis comprises my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

b. Due acknowledgment has been made in the text to all other material used.

- Ruchi Shah

21MECV17

Disclaimer

“The content of this paper does not represent the technology, opinions, beliefs or positions of Infineon Technologies its employees, vendors, customers, or associates.”

Certificate

This is to certify that the Major Project entitled **"Wide range LDO (Low DropOut) design for DCDC converter"** submitted by **Ruchi Shah (21MECV17)**, towards the partial fulfillment of the requirements for the Masters of Technology in VLSI Design, Nirma University, Ahmedabad is the record of work carried out by him under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this Project, to the best of our knowledge haven't been submitted to any other university or institution for award of any degree or diploma.

Date: Place: Ahmedabad

Dr. Jayesh Patel
Internal Guide,
Assistant Professor,
Institute of Technology,
Nirma University, Ahmedabad

Dr. Usha Mehta
Program coordinator,
Professor,
Institute of Technology,
Nirma University, Ahmedabad

Dr. Usha Mehta
Professor and Head,
EC Department,
Institute of Technology,
Nirma University, Ahmedabad.

Dr. Rajesh Patel
Director,
Institute of Technology,
Nirma University, Ahmedabad.

Certificate

This is to certify that the Major Project entitled “Wide range LDO design for DCDC converter" submitted by Ruchi Shah (21MECV17), towards the partial fulfilment of the requirements for the degree of Master of Technology in Embedded Systems, Nirma University, Ahmedabad is the record of work carried out by her under our supervision and guidance. In our opinion, the submit-ted work has reached a level required for being accepted for examination.

Date: 18/05/2023

Mr. Supreet Bhanja Deo
Sr. Manager Design
Infineon Technologies.

Undertaking for Originality of the Work

I Ruchi Shah Roll No 21MECV17, give undertaking that the Major Project entitled "Wide range LDO (Low DropOut) design for DCDC converter" submitted by me towards the partial fulfilment of the requirements for the degree of Master of Technology in Electronics and Communication of Nirma University, Ahmedabad 382 481, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any other published work or any project report elsewhere; it will result in severe disciplinary action.

Ruchi Shah

Signature of the Student

Date: 18/05/2023

(Signature of the Guide)

Acknowledgment

To learn new things is an opportunity, but a chance given to implement what you have learned is a bigger opportunity. I take this opportunity to thank **Nirma University** and **Infineon Technologies** who gave me an opportunity to undertake this interesting and innovative work.

On the very outset of this thesis, I would like to extend my sincere and heartfelt obligation towards our Head of Department **Dr. Usha Mehta**. I am grateful for their encouragement, understanding and insightful support in the development process.

Firstly, I take the opportunity to acknowledge the contribution to my guide **Prof. Jayesh Patel** for his constant support and computable acts of timely advice throughout the course of project work. His sincerity, thoroughness and determination have been a constant source of inspiration for me.

I am so grateful to my manager **Mr. Supreet Bhanja Deo** for giving me superb opportunity to work under his guidance. I am also thankful to my mentors **Mr. Sharath Maggada** and **Mr. Srinivasa Murthy** and team members for their active help and encouragement during development of this project.

Ruchi Shah

Abstract

Voltage regulator circuits are the backbone of modern embedded electronic products. Typically, these devices need a supply voltage of 5V or 3V DC depending on the application. This project discusses the design, verification, and layout of LDO, which is used for buck regulators PMIC. Owing to the rise in power requirements for electronic devices used in servers, automation, and consumer electronics; there is a need for high-efficiency buck converters that support a wide range of input voltage operations. To enable the switching of buck drivers and give a good supply for the control logic and analog circuitry of buck regulators, proper LDO design is also required. As our PMIC is used for server applications, one of the key requirements for the LDO is to support a wide input voltage operating range like 2.95V to 6V. The second requirement is to support a regulator with a very low dropout as the V_{in} starts from 2.95V and the V_{out} is 2.75V, leaving only 250 mV of headroom. The third requirement is to support a high operating current and to have a high current limit for buck-switching applications in order of 150mA to 200mA.

This project focuses on developing an LDO which meets the specifications listed above for our PMIC. Various circuit performances like DC behaviors, transient, Stability, and PSRR will perform. The layout will design; optimizing for the area, and noise and keeping latch-up constraints in mind.

Contents

List of figures

List of tables

Abbreviation

IC	Integrated Circuits
SOC	System on Chip.
AC	Alternating Current
DC	Direct Current
LDO	Low Dropout
HDO	High Dropout
PCB	Printed Circuit Board
I/O	Input/Output.
NMOS	N-channel Metal Oxide Semiconductor.
PMOS	N-channel Metal Oxide Semiconductor.
PSRR	Power Supply Rejection Ratio
UGB	Unity Gain Bandwidth
DRC	Design Rule Checking

Chapter 1

Introduction

Voltage regulators are a crucial component of embedded microcontroller-based applications' power management architecture. Voltage regulators are the power source of choice for systems where simplicity, adaptability, and economy are the main issues. For optimal operation and power management, the majority of current IC building pieces, such as digital and analogue macros, require a constant power source. Voltage regulators are devices that reject changes in the input voltage when the load current varies. They provide a stable, and noise-free supply voltage to all the essential blocks of an IC.

1.1 Prologue

Linear regulators and switching regulators are the two primary types of voltage regulators. Switching regulators offer advantages such as high efficiency and the ability to step up, step down, or invert voltage. However, they are more complex, requiring larger chip area, additional design effort, and higher cost. Moreover, their high-frequency switching operation generates noise, which is unsuitable for applications requiring stable and ripple-free voltage supply to sensitive components. To address these shortcomings, linear regulators are preferred. They are simple, provide ripple-free output due to the absence of switching, and exhibit better noise rejection. Dropout voltage (Vdropout) is a critical parameter used to classify linear regulators into high dropout (HDO) and low dropout (LDO) regulators. LDOs

typically have a dropout voltage ranging from 150mV to 350mV, while those with a dropout voltage exceeding 600mV are classified as HDO regulators. As power management circuits increasingly demand high efficiency, linear voltage regulators, specifically LDOs, play a significant role. For the purpose of this project, the term "voltage regulator" or "regulator" refers to a linear voltage regulator. Table 1.1 below provides a brief comparison of linear and switching voltage regulators.

	Switching Regulator	Linear Regulator
Function	$V_{out} > V_{in}$ or $V_{out} < V_{in}$	$V_{out} < V_{in}$
Efficiency	High	Low
Cost	High	Low
Noise or ripple	High	Low
Regulation	Comparatively less	High
Transient response	Slow	fast
Area	Large	Small
Applications	Microprocessors, SRAMs	Analog cells, RF

Table 1.1: Key contrasts of linear and switching regulators

Table 1.1 demonstrates that linear regulators offer a regulated output voltage with minimal design complexity and PCB area, resulting in low ripple.

1.2 Motivation

In the portable electronics gadget dominated world, the main difficulty is to manage battery power as efficiently as possible for extended periods of time. So, every portable and non-portable electronic device must include a power controlling macro. The rising demand for portable electronic devices in today's technology-driven world necessitates the exploration of more efficient power management techniques to enhance battery life. Voltage regulators play a crucial role in this regard, serving as a core component for improved performance.

Furthermore, these regulators provide protection against sudden variations in supply voltages, preventing potential damage to the integrated circuits (ICs) of electronic devices.

1.3 Problem Definition

Fluctuations in the power supply of Integrated Circuits (ICs) can lead to undesired behaviours within the IC. It is crucial to supply a consistent voltage to the chip, regardless of the load current demands arising from various digital circuits within it. Additionally, modern system-on-chip devices require voltage regulators that can reject variations in the main power supply, deliver regulated voltage, and offer isolation from input noise. In SOC devices based on the mode of operation there will be a need for multiple regulated voltages. To design a LDO without external capacitor which will regulate the output voltage by suppressing the input supply variations.

1.4 Objective

The main objective of the work is to design the wide range LDO (Low DropOut voltage) regulator with the proper understanding of its functionality and design aspects so that the same procedure and design follow in any technology node. This works aims to design of LDO regulator with Vin range of 2.95V to 6V and supports I_{load} of 20mA with I limit approximately 200mA for DCDC buck converter.

1.5 Organization

Chapter 1 introduce to project work by briefing about the voltage regulator circuits and their classification. The importance of voltage regulators in the portable electronic gadgets and thetarget specifications of the design is presented along with the implementation.

Chapter 2 discusses the basic linear low dropout regulator architecture and the past works onthe linear voltage regulators with PMOS based linear low dropout voltage regulators at focus. The chapter concludes with the discussion and other theoretical background needed in designing various building blocks of LDO voltage regulators such as error amplifier.

Chapter 3 elaborates on the methodology followed in this work which includes block

diagram, circuit diagrams, component specification, selection, and justification to the selection of components and concludes with the tools used in the system design.

Chapter 4 Some simulation setup and summarizes the results obtained and the analysis of waveforms.

Chapter 5 presents the summary of the project work done and the conclusions for the same work. The chapter is concluded with future scope to the presented work.

Chapter 2

Background Theory

In this chapter the basic low dropout regulator architecture is studied along with its transfer characteristics and then some past works on the same architecture is discussed. Some important characteristics and terminologies are explained. All the theoretical background for the various building blocks of the architecture is mentioned. Finally, the conclusions drawn from the literature review of the past work concludes the chapter.

1.1 Overview

The primitive level block diagram of the dropout-based regulator is as shown in Fig. 2.1. The circuit composed of a voltage reference, an error amplifier, a feedback network, and a pass device.

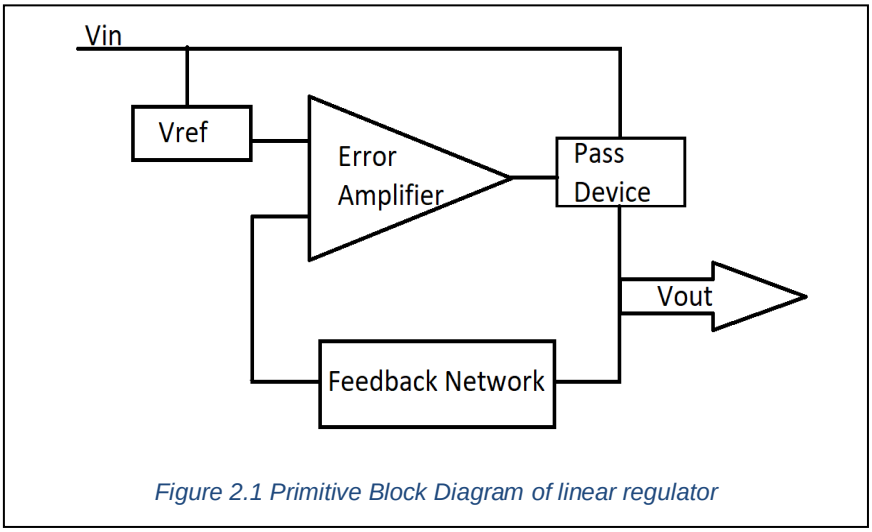

Figure 2.1 Primitive Block Diagram of linear regulator

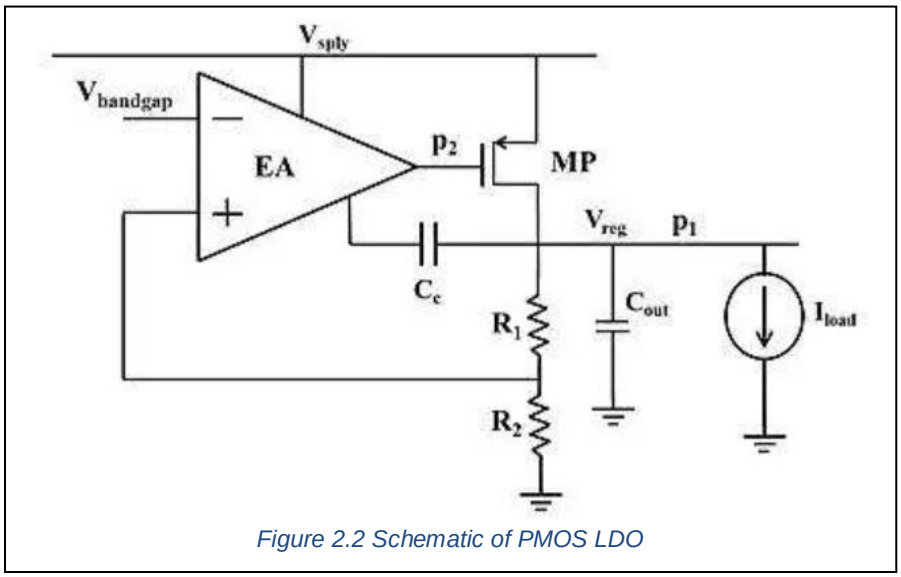

Figure 2.2 Schematic of PMOS LDO

In the linear voltage regulator illustrated in Figure 2.2, the pass device is responsible for delivering the required load current whenever there are variations in the load. This is achieved through the use of an error amplifier and a feedback loop, which continuously adjusts the gate voltage of the driving device. As a result, the output voltage remains regulated regardless of changes in the load. The discrepancy between the input and output voltage is referred to as the dropout voltage, and it influences the selection of the pass device.

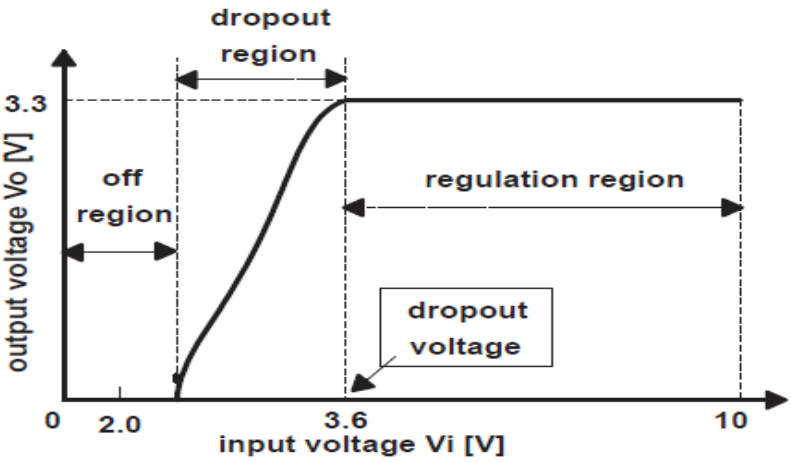

Figure 2.3 Typical Transfer Characteristics of voltage regulator

Figure 2.3 illustrates the typical transfer characteristic curve of a voltage regulator, which is divided into three main regions: the OFF region, the dropout region, and the regulation region.

A power management system often consists of multiple Low Dropout Regulators (LDO) and switching regulators. Traditional LDO regulators typically require a large output capacitor in the microfarad (uF) range. LDOs used in analog applications require power rails with low noise and high accuracy. Voltage regulators ensure a stable and constant voltage supply, even when there are changes in the load current or load impedance, such as fast transients or sudden load variations.

Many handheld and battery-operated devices incorporate a power-saving feature to minimize power dissipation. Idle circuits that are not actively performing tasks are temporarily turned off, reducing overall power consumption. In such cases, the voltage regulator must respond promptly to these system requirements and power up the connected circuits swiftly.

1.2 Literature Review

In a study by M. H. Kamel et al. [2], a comparison was made between two voltage regulator architectures while keeping the quiescent current, input voltage, output voltage, and compensating capacitors the same. PMOS-based voltage regulators

exhibit lower dropout compared to NMOS counterparts, but they can have stability issues due to two poles at lower frequencies—one at the output of the error amplifier or pass device gate node, and the other at the output node. On the other hand, NMOS-based LDOs offer advantages in terms of area and fast transient response, with minimal driver resistance at high currents. Two approaches were suggested to achieve a wide range of load current capability: increasing the pass transistor width or boosting the voltage at the error amplifier output to the gate of the pass transistors using charge pump circuits.

In the work by V. Gupta et al. [3], a simple potential divider network was used to analyze the Power Supply Rejection (PSR) of linear voltage regulators. The analysis helped derive guidelines for achieving high PSR. The dominant pole position, where the performance begins to degrade, and the subsequent poles are determined by the DC open-loop gain, error amplifier bandwidth, unity gain frequency, and ESR zero. The relationship between power supply rejection and the open-loop gains of the voltage regulator provides insights into achieving high PSR. The authors also proposed two types of error amplifiers: Type-A and Type-B. Type-A employs an NMOS at the input side and a PMOS-based current mirror load, while Type-B has PMOS devices at the input side and NMOS devices connected to the ground as the current mirror load. Type-B topology with PMOS driver achieves high PSR bandwidth, while Type-A topology with NMOS driver is also considered. Detailed descriptions of both Type-A and Type-B error amplifier topologies, as well as the trade-off between the two considering PSR performance, are provided in section 3.2.1.

T. Coulot et al. [4] introduced a multi-stage power management block that incorporates approximately 10 LDOs to control various power domains within a system-on-a-chip (SOC), such as analog and digital power domains. A charge pump is used to boost the gate voltage of the driver NMOS and achieve a power supply rejection ratio (PSRR) higher than -40dB. However, the use of charge pumps for voltage boosting introduces additional switching noise in the circuit. To minimize this switching noise, a cascode current mirror is employed. The system utilizes two error amplifiers to improve line and load regulation: one amplifier drives the charge pump output, while the other directly drives the gate of the driver NMOS, forming a fast feedback loop that is primarily active at high frequencies.

1.3 Characteristics of Linear Voltage Regulator

In the design of linear voltage regulators, several important performance parameters need to be considered.

Drop Out: One such parameter is the dropout voltage, which refers to the difference between the unregulated input voltage and the regulated output voltage at which the regulator ceases to regulate the output. This value is sometimes referred to as the headroom voltage in certain literature.

$$Dropout\ voltage = V_{in} - V_{out}$$

It decides the highest current allowable and the minimum supply voltage. In general, while regulator design the max load current and the lower limit of the power supply voltage that keepsthe driver device in saturation region is mentioned. Alternatively

$$Dropout\ voltage = I_{load} * R_{on}$$

The pass transistor design is done utilizing the max load current and the lower limit of theoverdrive voltage that will the pass device in saturation region.

Load Regulation: It specifies how well the regulator is against the load current variations. Itis defined as follow and is measured at steady state conditions.

$$Load\ Regulation = \frac{\Delta V_{out}}{\Delta I_g}$$

Line Regulation: It signifies ability of the regulator when the supply itself is varying. It is alsomeasured at steady state condition for a particular load current. It is defined as follow

$$Line\ Regulation = \frac{\Delta V_{out}}{\Delta V_{in}}$$

Temperature coefficient: Mathematically, the dropout voltage can be expressed as the partial derivative of the output voltage with respect to temperature. It directly depends on the drift in the reference voltage caused by temperature variations and the input offset voltage of the error amplifier.

$$TC = \frac{1}{V_{out}} \frac{\partial V_{out}}{\partial Temp}$$

By improving the error amplifier's offset voltage, the accuracy of the regulator's output is enhanced, and the dependency of the reference voltage on temperature is reduced.

Load transients:

The load regulation of a voltage regulator measures the change in the regulated output voltage during sudden variations in load current. When the load current changes abruptly from zero to its highest specified value, peak variations in the output voltage occur. This output voltage variation can be modeled as follows:

$$\Delta V_{out} = \frac{I_{max}}{C_{out}} \Delta t$$

Here, Imax represents the specified maximum output current, Δt is the response time of the LDO, and Cout denotes the output capacitance of the LDO. Improving the load regulation can be achieved by using a larger output capacitor and increasing the closed-loop bandwidth of the regulator.

Quiescent current: The quiescent current, also known as ground current or off current, refers to the current drawn from the power supply when there is no load connected. It can be determined by performing a DC operating point simulation and measuring the total current consumed by the error amplifier, feedback resistors, and other supporting circuitry. The quiescent current is calculated as the difference between the input current and the output current or load current.

$$I_Q = I_i - I_o$$

Power supply rejection ratio: The power supply rejection ratio (PSRR) is an indicator of how effectively a circuit suppresses the ripple in the supply voltage across a wide range of frequencies. It provides a measure of the circuit's ability to attenuate variations in the supply voltage, whether they are low or high frequency small signals. PSRR is quantified using an equation, which determines the level of ripple suppression achieved by the circuit.

$$PSSR = -20log_{10}\left(\frac{V_{out}}{V_{in}}\right)$$

PSRR depends on the driver transistor parasitic capacitances and is proportional to the reciprocal of the loop gain at lower frequencies. The error amplifier plays a major role in improving the PSRR.

Chapter 3

Methodology

This chapter describes the design flow and the implementation of the design which includes block diagram, circuit diagram of the design, component specification, selection, and justification to the selection of components and concludes with the tools used in the system design.

3.1 Design Flow

The design process of an LDO voltage regulator necessitates a thorough comprehension of the system and its load characteristics. Achieving objectives such as maximizing load regulation, ensuring stability, and minimizing transient output voltage variations can be challenging and often conflicting. These challenges arise due to the inherent characteristics of the regulator architecture and its operating environment. This chapter delves into the subsystems that constitute the entire system, while also discussing the key blocks of the design in light of circuit theory and system requirements. These crucial blocks encompass the pass device, digital logic, error amplifier, reference voltage, and comparator.

3.2 Design Consideration

To meet the design specifications there will be tradeoffs which will ensure the best performanceacross different environments the device is used. Some of the design considerations are discussed below.

3.2.1 Power Supply Rejection

The primary function of the regulator is to maintain a stable output voltage in the presence of both high and low frequency small signal variations in the power supply. While this characteristic shares similarities with Line Regulation (LNR) in terms of stabilizing the output against supply variations, it differs in that LNR specifically addresses DC variations, whereas the regulator's capability encompasses variations across a wide range of frequencies.

The reciprocal of the small signal variations in the output voltage due to small variations on the input side is referred to as the transconductance or conductance gain. It quantifies the relationship between the input and output signals in terms of their voltage variations.

$$PSRR = \frac{1}{\Delta V_{in}}$$

Where ΔV_{IN} is the supply gain defined above

The noise has several ways to get into the system as shown in fig 3.1 below

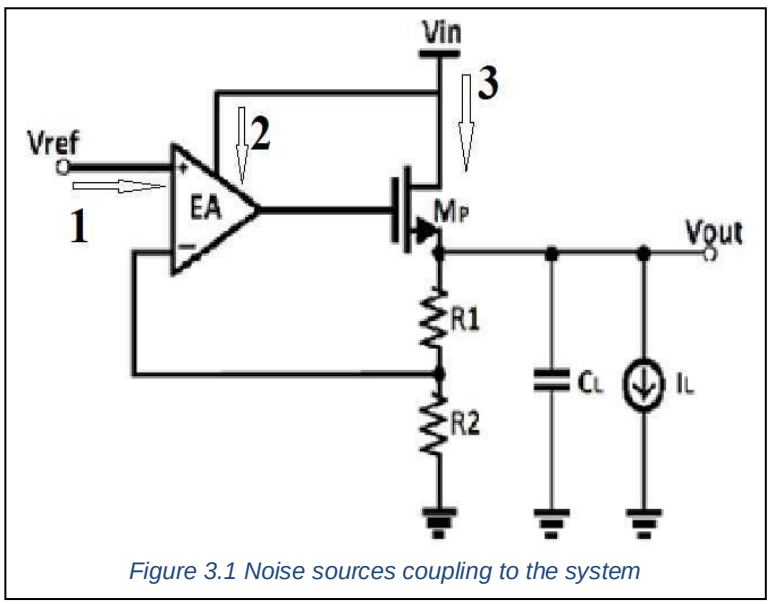

Figure 3.1 Noise sources coupling to the system

Among the sources of supply noise entering the system depicted in fig 3.1, the noise from voltage reference circuit is minimal comparatively from sources 2 and 3. This may be from the fact that usually the output of the reference circuit is filtered out to reduce the ripples in the output.

3.2.2 Stability

The stability related issues of the regulator require solutions in the form of compensation techniques [1]. The figure 3.2 shown below is one such scheme for compensation called the external compensation where the dominant pole is due to the externally connected capacitor and the high output impedance and the parasitic capacitors like Cgs, Cgd and the output impedance of the error amplifier forms the non-dominant pole.

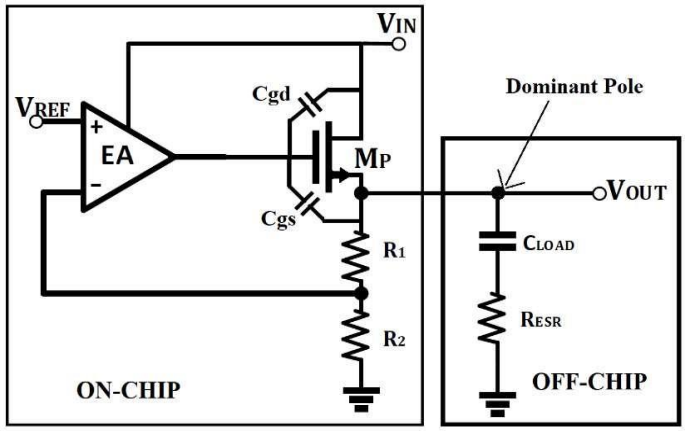

Figure 3.2 Conventional voltage regulator with external capacitor

To achieve stability, external compensation is employed in voltage regulators, which typically involves using a large capacitor in the range of 1 to 10µF at the output node. This capacitor serves to establish the dominant pole, ensuring stability of the regulator. Additionally, the equivalent series resistance (ESR) of the load capacitor contributes to a left-half plane zero, compensating for the phase shift introduced by the non-dominant pole. By carefully selecting the ESR and capacitor values, the regulator's stability and performance can be effectively managed.

The internal compensation is also called the capless architecture since there is no need to have any external capacitor for achieving the stability. The fig 3.3 depicts the architecture of capless LDO. In internal compensation an internal node is chosen to place the

dominant pole and it will be at the gate node of the pass device.

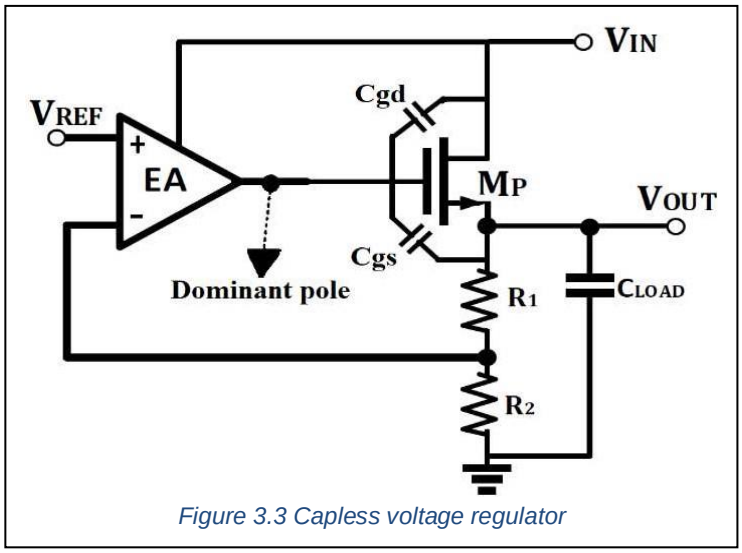

Figure 3.3 Capless voltage regulator

3.2.3 Efficiency

The efficiency of a voltage regulator is determined by three key parameters: quiescent current, load current, and pass transistor voltage drop. The efficiency can be calculated using the following equation:

$$\eta = \frac{V_{out} * I_{load}}{V_{in}\left(I_{gnd} + I_{load}\right)}$$

The efficiency of a voltage regulator is influenced by two crucial factors: the quiescent current (Ignd) and the load current (Iload). To achieve a highly efficient regulator, it is essential to minimize both the dropout voltage and the quiescent current. This can be accomplished by designing the regulator with large feedback resistors and utilizing a low quiescent current error amplifier. These measures contribute to improving overall efficiency and optimizing the performance of the voltage regulator.

3.2.4 Load regulation

Load regulation is a metric that indicates the ability of a regulator to maintain a

consistent output voltage in the face of changing load conditions, specifically variations in load current. It is typically measured once the output voltage has stabilized. In the context of a PMOS LDO, the load regulation can be approximated using the equation

$$\frac{\Delta V_{out}}{\Delta I_{load}} \approx -\frac{1}{\beta A_v g_{mn}}$$

The load regulation of a regulator depends on two important factors: the open-loop gain (Av * β), where β represents the ratio of R2 to the sum of R1 and R2, and the transconductance of the NMOS pass device (gm,n). These parameters play a significant role in determining the load regulation characteristics of the regulator.

3.2.5 Line regulation

Line regulation is the regulators characteristic to maintain a stable output voltage during variations in supply voltage. This quantity is quite close to PSRR. Vaguely it is PSRR at 0 Hzfrequency. It is a DC parameter measured when the output has reached a steady state. It can be derived by referring to the schematic in fig 2.2 as follows,

$$\frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{1}{\beta A_v g_{mn} r_{on}}$$

Upon examining the provided equation, it becomes apparent that line regulation exhibits a significant reliance on both the gain of the error amplifier and the intrinsic gain of the NMOS pass device.

3.2.6 Pass device size

The dimensions of the driver in a voltage regulator are determined based on two key factors: the maximum load current and the minimum dropout requirement necessary to maintain the driver in saturation mode of operation. The sizing of the driver is typically based on an equation that considers the saturation region current. It's worth noting that increasing the dimensions of the driver also increases the associated gate capacitance,

leading to a decrease in the error amplifier slew rate and consequently slower transient response. There are two potential options for the MOSFETs used as drivers: NMOSFET and PMOSFET. The choice between these two types depends on various factors such as silicon area, speed requirements, and the specific application. In general, NMOSFETs are typically employed in a common drain or source follower configuration, while PMOSFETs are utilized in a common source configuration. The selection of the pass device is also influenced by the desired dropout voltage for the design.

3.3 Design Block

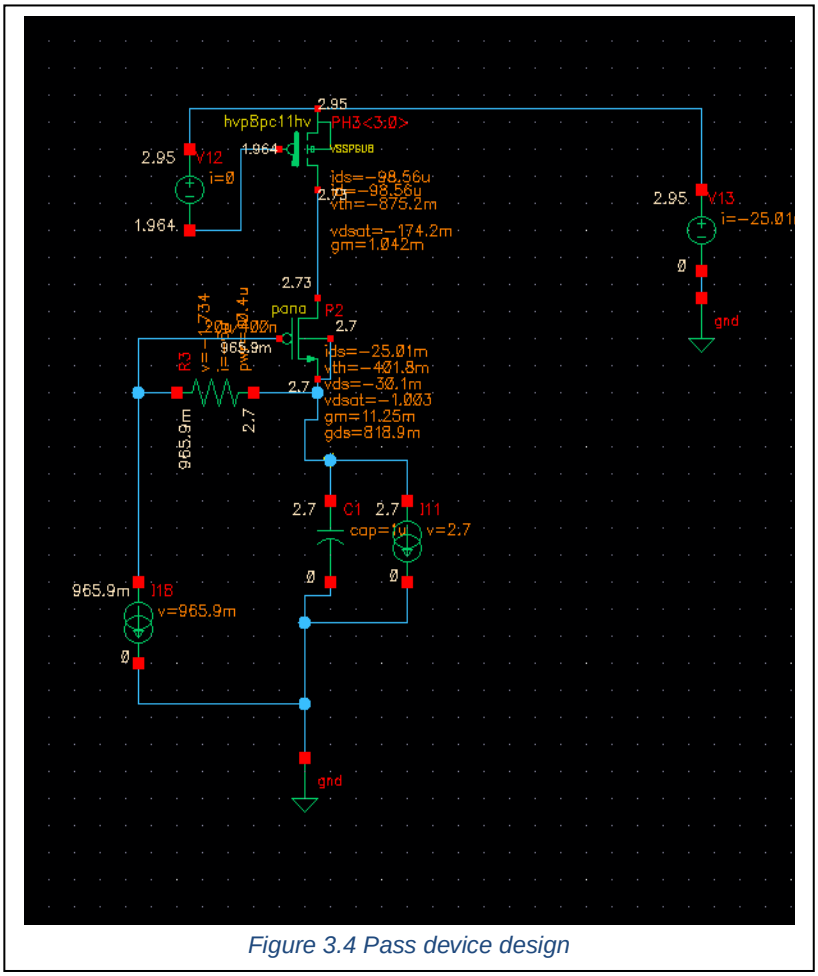

Figure 3.4 Pass device design

Designing a Pass Device is the first fundamental stage of LDO design. Therefore, the Pass device design is represented in the diagram below together with several other significant devices. These devices are in place because they in some way aid in the proper operation of the pass device.

One driver and one cascode device are utilized in this design to create a pass device. The cascode is a basic PMOS device, while the driver is an 8V device. The PMOS is referred to as a cascode device because the connection between the Driver and the PMOS is series (cascode), and the 8V device is known as a driver since it is the primary device that drives the entire circuit with some feedback.

The following basic specifications are provided to help with the design of this circuit:

Parameter	value
Vin	2.95 V
Vdsat	150 mV
Vds	220 mV
Id	25 mA
Vcc/Vout	2.7 V

Table 3.1 Specification of LDO

The 2.95V to 6V Vin range is mentioned in the preceding chapter. Consideration is given to Vin here.

Therefore, the driver's source wire is connected to a constant voltage source with a value of 2.95V in order to assume Vin=2.95V. The driver's gate terminal is coupled to a DC power source. This voltage source's minimum value is Vth + 200mV. This value is necessary because, for this driver to function properly, we must drive it into the saturation region. The 2.73 volts at the drain terminal are also maintained using this voltage source. The cascode device is attached to the driver's drain terminal.

The LDO's fixed 2.7V output voltage. Therefore, there is only a 250mV difference between the input and output voltage. what is referred to as Dropout. This Dropout is divided into two halves by the circuit's design: one is 220 mV and the other is 30 mV. The driver experienced a 220mV decrease, and the cascode device experienced a 30mV drop.

The maximum current is 25 mA. Therefore, a current source and capacitor are utilized to produce a 25mA continuous current. The drain terminal of the cascode is connected to the one terminal of this combination, which connects the current source and capacitor in parallel. The capacitor and current source have values of 1uf and 25mA, respectively.

The gate and drain terminals of the cascode device are linked via a resistor. One can obtain 2.7V at the output node by varying the resistance of that resistor, which helps to meet the requirement of a 30 mv drop in the cascode device.

Find the driver's suitable W/L ratio first. Use the Id_{sat} equation to do this because the driver needs to be in the saturation region for the LDO to function properly. Then, for the cascode device that is in the linear region, find the W/L ratio. Following the completion of both W/L, the multiplicity factor of both devices should be finalized for the provided specification by varying the resistor and voltage source located at the gate terminal of the driver.

Combining the major blocks such as error amplifier, the pass device, the feedback network,and the comparator into the final design for LDO and the schematic symbol of the design is as shown in Fig 3.4. Before the final integration each individual module is simulated for functionality check and then finally assembled to get thefinal design. All the individual functional blocks needed are developed and kept in library so whenever a new design with modified specifications needs to be developed the same designs can be reused. The digital logic module taken from the existing library. Finally, all the functional module output and input signals are identified and paired with corresponding input and output signals of the other module this will ensure the proper functional behavior of the circuit.

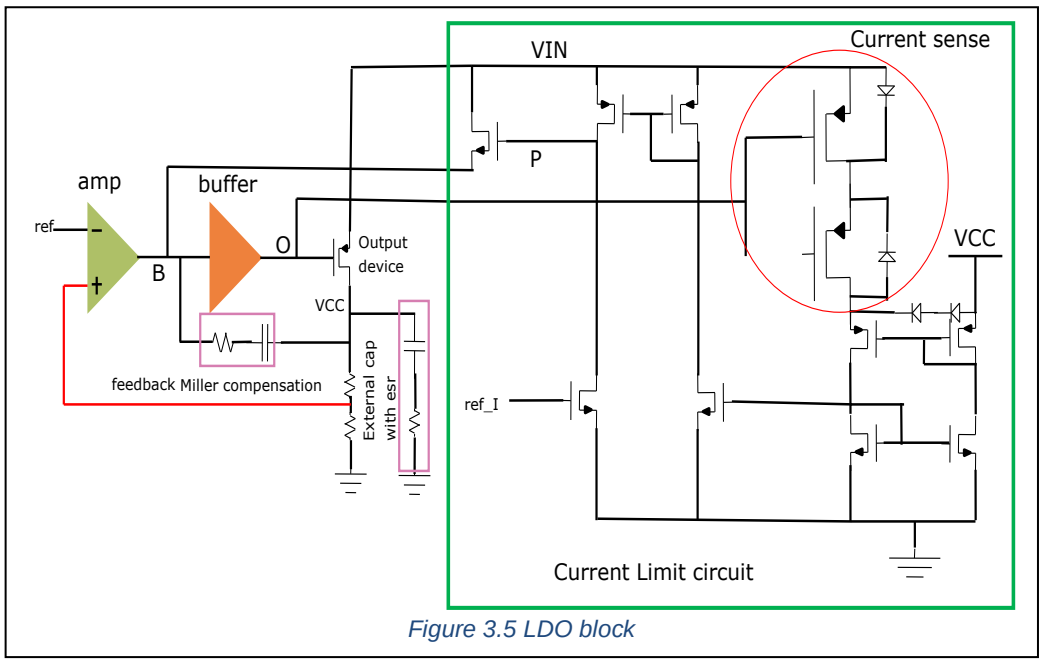

Figure 3.5 LDO block

3.4 Tool Used

In this section, we will provide an overview of the tools utilized in the design process. To begin with, the Cadence Virtuoso schematic editor is employed for schematic entry and the creation of system-level circuit designs. For all DC, transient, and AC simulations conducted across various process, voltage, and temperature (PVT) corners, the Cadence Analog Design Environment (ADE-L) and ADE Assembler with Spectre simulator are employed. Additionally, the Insight Analyzer tool is utilized for performing Electrical Rule Checks (ERC).

Chapter 4

Simulation Setup and Result Analysis

In this chapter the design is verified for functionality using transient analysis in spectre simulator across the corners. The design characteristics are also verified with simulation results across the PVT corners. At the end of the chapter justification is provided for any deviationsfrom the expected values. finally, the design is implemented in 130nm CMOS technology with DRCclean and zero static paths.

4.1 Simulation Setup

The fig 4.1 shows the simulation setup to verify the design functionality. The design is capable of operating from 2.95 V to 6 V with a typical dropout voltage of 250mV. The followingassumptions made while designing and simulating voltage regulator block are believed to remain unaltered throughout the experiment.

1. Reference voltage of 1.2V is available from the bandgap reference without any deviationripple in it.
2. Load capacitor of 1µF is being used at the output of the regulator.
3. Load current of LDO is 25mA

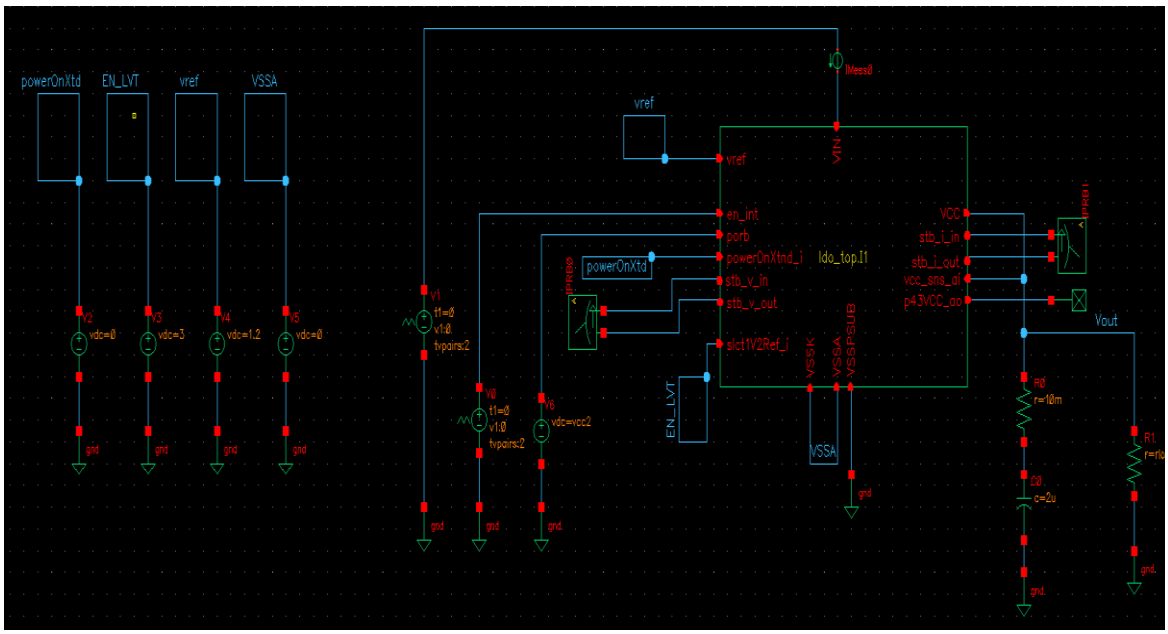

Figure 4.1 Testbench of functional simulation

4.2 Stability Analysis

Op-amp stability analysis is a process used to determine the conditions under which an operational amplifier (op-amp) circuit remains stable and free from oscillation. The stability of an op-amp circuit is crucial to ensure reliable and accurate operation. Determine the specific op-amp circuit configuration you are analyzing, such as an inverting amplifier, non-inverting amplifier, or a feedback network.

Analyze the feedback network connected to the op-amp to determine the closed-loop gain and phase response of the circuit. This can be done using circuit analysis techniques, such as nodal analysis or loop analysis. Compare the phase margin obtained in the analysis with the desired stability criterion. If the phase margin is greater than the specified threshold, the op-amp circuit is considered stable. Otherwise, additional measures, such as compensation techniques or component modifications, may be required to improve stability.

The stability of the design isanalyzed using stb analysis in spectre ADE.
The set up for stability analysis shown in the figure 4.2

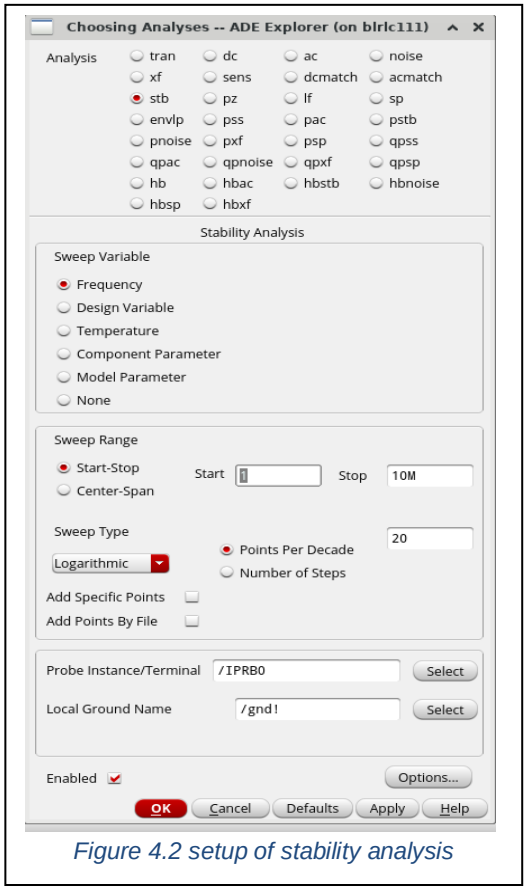

Figure 4.2 setup of stability analysis

In stability analysis two checks is important

1. Phase Margin

   The phase margin of an operational amplifier (op-amp) is a measure of its stability. It indicates the amount of phase shift margin between the output and input signals at the frequency where the closed-loop gain is unity (0 dB). A larger phase margin implies greater stability. According to figure 4.2, the LDO's phase margin is 76.733 degrees at 0dB gain.

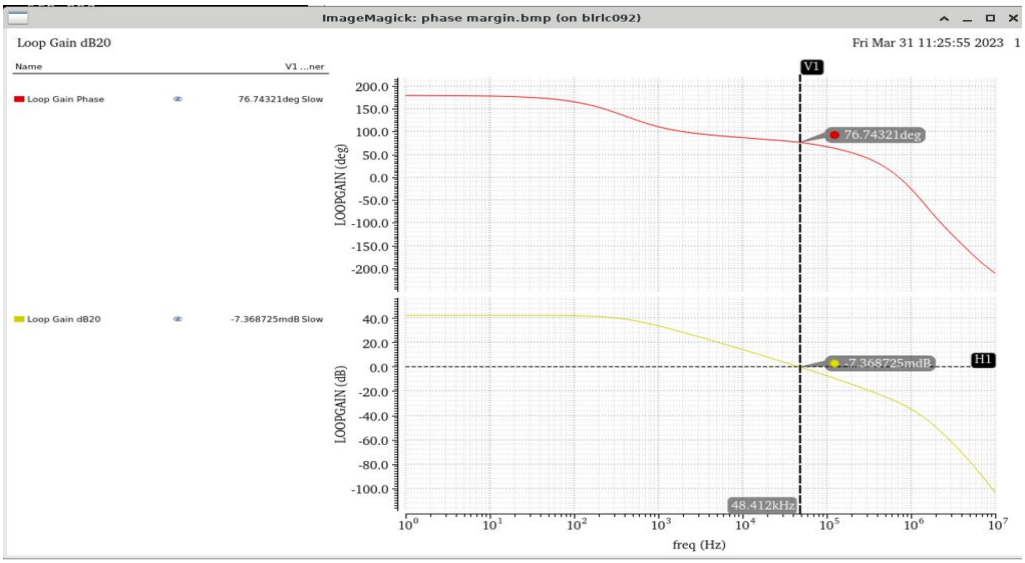

Figure 4.3 phase Margin of LDO

2. Gain Margin

   The gain margin of an operational amplifier (op-amp) is a measure of its stability and indicates the amount of gain margin between the closed-loop gain and unity gain (1). A larger gain margin implies greater stability. According to figure 4.2, the LDO's gain margin is 29.36 dB

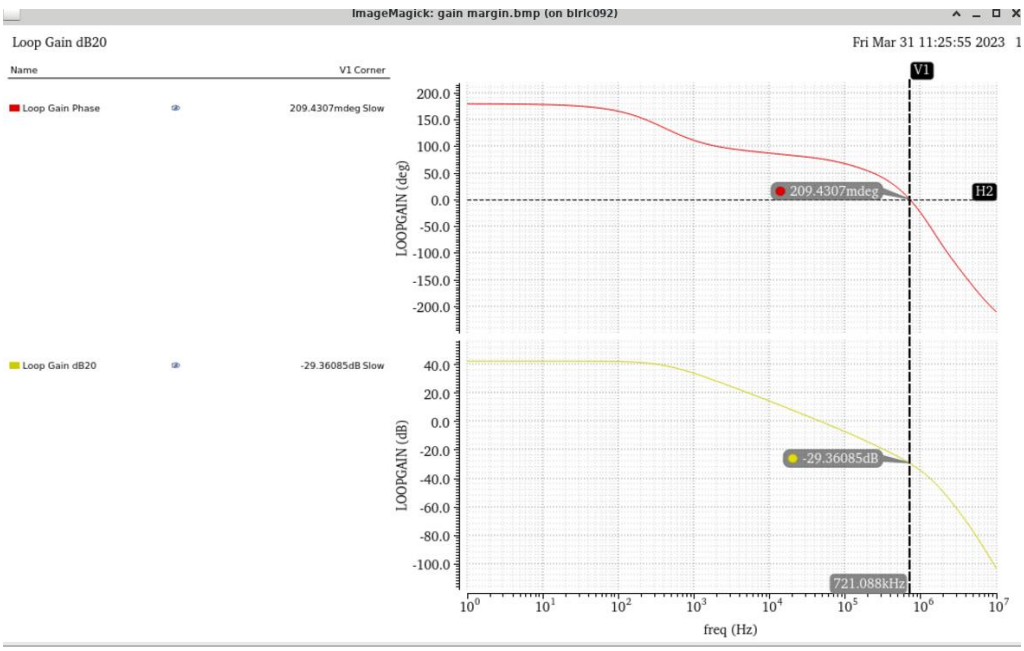

Figure 4.4 Gain Margin of LDO

4.3 Load Regulation

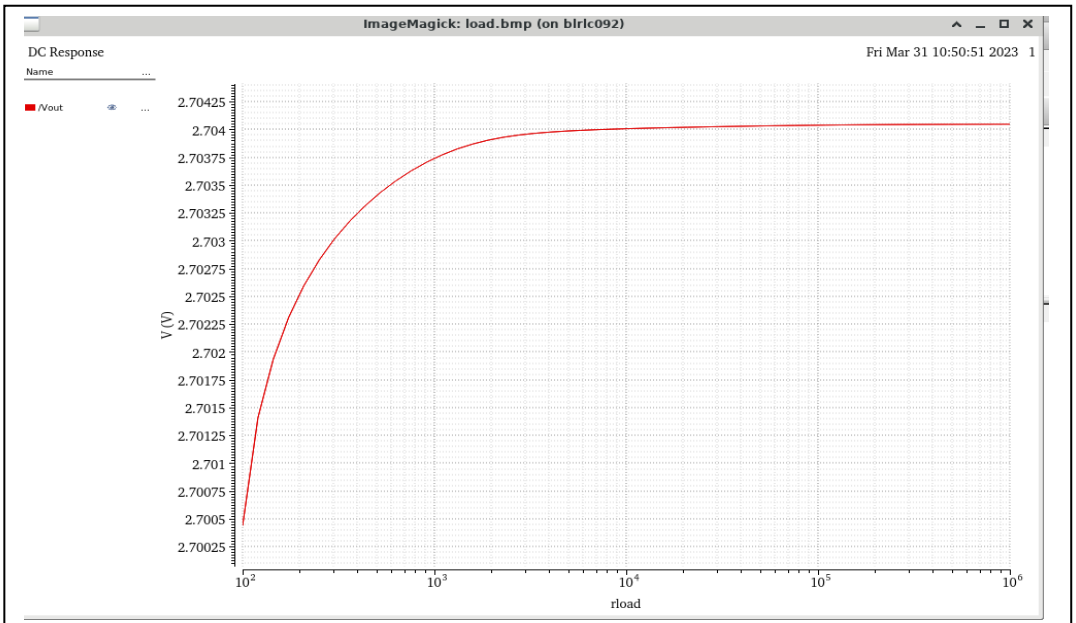

Figure 4.5 Output variation with respect to load current

Load regulation in an operational amplifier (op-amp) refers to its ability to maintain a stable output voltage when subjected to changes in the load resistance connected to its output. Load regulation is an important characteristic to consider, as it affects the op-amp's ability to provide a consistent output voltage regardless of variations in the load.

The perturbations in the output voltage with respect to the load current is simulated with a DC sweep of load current from 1mA to 25mA the results are shown in the fig 4.5

4.4 Line Regulation

The output voltage variations due to changes in the input voltage is specified through the line regulation parameter. It is simulated by performing a DC sweep on the input voltage from 2.95V to 17V and plotting the output voltage.

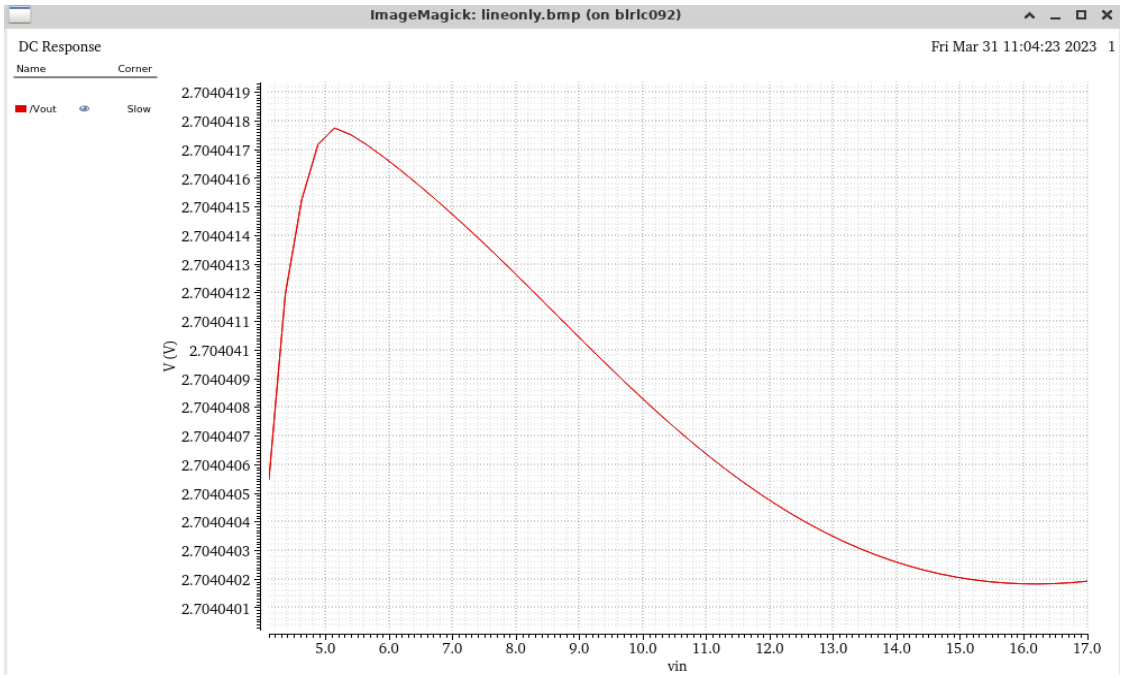

Figure 4.6 Output variation with respect to input voltage

Chapter 5

Layout of LDO

5.1 Basic Information of Layout

Layout refers to the physical arrangement and interconnection of components, devices, and interconnects in an integrated circuit (IC) design. It involves translating the circuit schematic into a geometric representation that can be fabricated on a semiconductor wafer. The layout process is essential for converting the design of an IC into a format suitable for manufacturing. It defines the exact locations, sizes, and shapes of components and their interconnections on the semiconductor substrate. he layout process typically involves several steps, including floor planning, placement, routing, and verification. Floor planning establishes the general layout of major blocks, placement determines the precise locations of individual components, routing creates interconnections between components, and verification ensures the correctness of the layout.

5.2 Important Technique to make Layout

There are a few important techniques that we need to consider when performing an analog layout.

1. **Common Centroid**

   The common centroid technique is a widely used layout technique in analog circuit design to minimize mismatches between components caused by process variations. It involves arranging pairs or groups of components in a symmetrical manner to mitigate the impact of variations and improve circuit performance. The main objective of the common centroid technique is to achieve precise matching between components that are critical for circuit performance, such as transistors in differential amplifiers or resistor networks. It helps ensure that any process variations affecting one component also affect its counterpart in a compensating manner, reducing the overall mismatch. The common centroid technique involves placing pairs or groups of components in a symmetrical manner with respect to certain layout axes or planes. This symmetry ensures that both components experience similar layout-induced variations, such as proximity effects or stray capacitance, minimizing the net mismatch between them.

   It's important to note that while the common centroid technique helps mitigate process variations, it does not eliminate them entirely. Other design techniques and considerations, such as process calibration, circuit design robustness, and circuit trimming, may also be employed to further improve matching and compensate for variations.

2. **Matching**

   Matching techniques in analog layout are employed to ensure precise matching between components, such as transistors or resistors, which is essential for achieving desired circuit performance. The common centroid technique, as discussed earlier, involves placing pairs or groups of components in a symmetrical manner. This technique helps compensate for process variations and layout-induced effects by ensuring that any variations affecting one component also affect its symmetric counterpart. The symmetrical placement minimizes the net mismatch between the components.

   Interdigitation is a technique where adjacent components are intertwined or interleaved with each other. For example, in interdigitated fingers of transistors, the source, drain, and gate terminals of adjacent transistors are alternated. This

technique helps achieve better matching by reducing the differences in parasitic capacitance, resistance, and other layout-induced effects between adjacent components. Dummy components, also known as fillers or dummies, are non-functional components added to the layout to enhance matching. These components are placed in areas with no specific circuit function but are strategically positioned to compensate for process variations, reduce layout-dependent variations, and improve overall matching.

3. **Shielding**

   Shielding techniques in analog layout are employed to minimize electromagnetic interference (EMI) and improve signal integrity by reducing unwanted coupling between components and external noise sources. These techniques involve the use of shields or barriers to isolate sensitive analog circuitry from interference. Metal shields are physical barriers made of conductive material, such as metal layers in the IC stack or metal shielding cans. These shields are placed strategically to enclose sensitive analog components or circuit blocks, protecting them from external electromagnetic fields. Metal shields can also be used to separate analog and digital sections to prevent digital noise coupling into the analog domain. Guard rings are conductive rings or loops surrounding sensitive analog components, such as amplifiers or low-noise circuits. They are connected to a reference potential, usually ground, and act as an electrostatic shield, reducing the influence of stray electric fields and minimizing capacitive coupling. It's important to note that shielding techniques should be carefully implemented, considering the specific requirements and constraints of the analog circuit design. Trade-offs between shielding effectiveness, layout area, signal integrity, and cost should be considered to achieve the desired balance.

The aforementioned three techniques are applied when creating the LDO layout. We always use the matching technique when designing the layout of a current mirror circuit to ensure proper mirroring. Also used here is the same. The current mirror circuit is designed using the same method here as well. Common centroid are used

in comparator layout, and shielding technique is employed during routing of power net and sensitive nets.

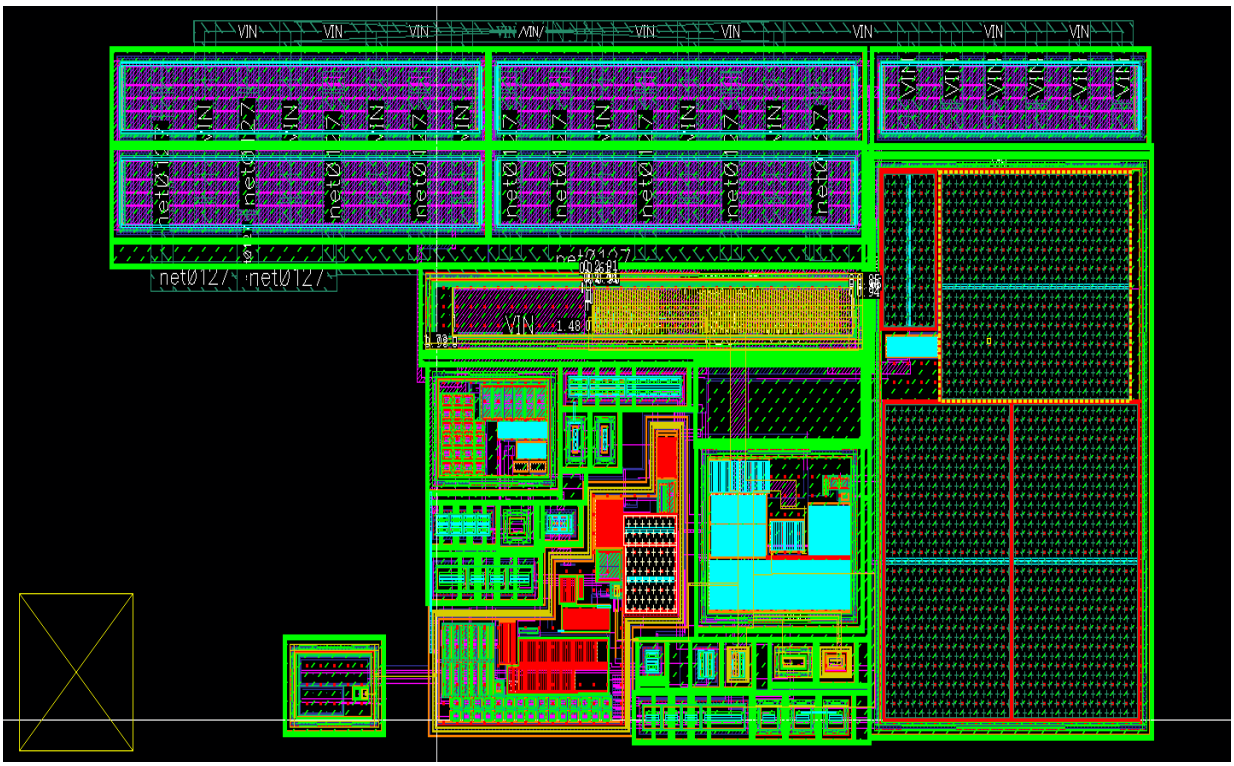

Figure 5.1 Layout of LDO

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

The primary objective of the work is to design a LDO voltage regulator with comprehensive understanding of the various functional blocks involved.

The design is implemented in 130nm technology node. The main design characteristics such as dropout voltage, quiescent current, load regulation, line regulation and power supply rejection, stability etc are studied before the design to make a correct design consideration. The individual functionalblocks are integrated into the final system and the functionality is verified through various simulations such as transient analysis, DC analysis AC analysis and stb analysis.

6.2 Future Scope

The present work involved in the design of LDO voltage regulator with capless architecture has a stability limit over a load current range of 0 to 25mA and the load

capacitor in the range of 1 to 10µf. The dynamic performance of the system is good for the given loadcurrent (25mA) in this work however in future if the load current requirement is increased then new design techniques have to be employed to keep the system stable with capacitor free outputnode. By making use of the gm/id technique of designing the analog circuits in subthreshold region operation better power optimization is achieved.

References

1. J. M. Hinojo, C. Luján Martínez, and A. Torralba, “Internally compensated LDO regulators for modern system-on-chip design.” Cham: Springer International Publishing, 2018.

2. M. H. Kamel, Z. K. Mahmoud, S. W. Elshaeer, R. Mohamed, A. Hassan, and A. I. A. Galal, "Comparative Design of NMOS and PMOS Capacitor-less Low Dropout Voltage Regulators (LDOs) Suited for SoC Applications," 2019 36th National Radio Science Conference (NRSC), 2019, pp. 305-314, doi: 10.1109/NRSC.2019.8734659.

3. V. Gupta, G. A. Rincon-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," IEEE International SOC Conference, 2004. Proceedings., 2004, pp. 311-315, doi: 10.1109/SOCC.2004.1362447.

4. T. Coulot et al., "Fully integrated power management unit (PMU) using NMOS Low Dropout regulators," Eurocon 2013, pp. 1445-1452, doi: 10.1109/EUROCON.2013.6625168.

5. H. Gupta, G. K. Mishra, N. Z. Rizvi and S. K. Patnaik, "Design of high PSRR folded cascode operational amplifier for LDO applications," 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), 2016, pp. 4617-4621, doi: 10.1109/ICEEOT.2016.7755591.

6. R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching converter power stages," in IEEE Power Electronics Specialists Conference, 1976, pp. 18-34.

7. C. Toumazou, F. J. Lidgey, and D. G. Haigh, "Analog IC design: the current-mode approach," in Proceedings of the IEEE, vol. 90, no. 4, pp. 606-640, Apr. 2002.

8. Y. Jiang, X. Zhang, and X. Zhang, "A low dropout voltage regulator with fast transient response and low output noise," in Proceedings of the IEEE International Conference on ASIC, 2009, pp. 747-750.

9. L. Y. Wu and C. J. Liu, "A 100 mA low-dropout voltage regulator with fast transient response," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 51, no. 6, pp. 289-292, Jun. 2004.

10. J. J. Liou and Y. S. Hwang, "A low dropout voltage regulator with a power-saving circuit," in Proceedings of the IEEE International Symposium on Circuits and Systems, 2005, pp. 515-518.

11. C. C. Chien, W. H. Tsai, and H. C. Tien, "A low dropout regulator with a fast-transient response for portable applications," in Proceedings of the IEEE International Conference on Electronics, Circuits and Systems, 2008, pp. 905-908.

12. A. E. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb. 1998.

13. W. M. Ng and R. P. Martins, "A low dropout voltage regulator with a dynamic load transient response enhancement technique," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 10, pp. 2676-2687, Oct. 2010.

14. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, 2nd edition, McGraw-Hill, 2017.

Thesis1

ORIGINALITY REPORT

9%	6%	3%	4%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	hdl.handle.net Internet Source	2%
2	Submitted to Manipal University Student Paper	2%
3	E.J. Brauer. "Performance evaluation of CMOS low drop-out voltage regulators", The 2004 47th Midwest Symposium on Circuits and Systems 2004 MWSCAS 04, 2004 Publication	1%
4	repository.iiitd.edu.in Internet Source	<1%
5	Submitted to De Montfort University Student Paper	<1%
6	usermanual.wiki Internet Source	<1%
7	Submitted to University of Florida Student Paper	<1%
8	arxiv.org Internet Source	<1%

9	baixardoc.com Internet Source	<1 %
10	www.researchgate.net Internet Source	<1 %
11	W KESTER. "Sensor Signal Conditioning", Sensor Technology Handbook, 2005 Publication	<1 %
12	tudr.thapar.edu:8080 Internet Source	<1 %
13	C.K. Chava, J. Silva-Martinez. "A Frequency Compensation Scheme for LDO Voltage Regulators", IEEE Transactions on Circuits and Systems I: Regular Papers, 2004 Publication	<1 %
14	Steven H. Voldman. "ESD Basics", Wiley, 2012 Publication	<1 %
15	archive.org Internet Source	<1 %
16	d-nb.info Internet Source	<1 %
17	dokumen.pub Internet Source	<1 %
18	www.ti.com Internet Source	<1 %