A Four-level Inverter Scheme with Reduced Common Mode Voltage for an Induction Motor Drive

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Abstract

A four-level inverter configuration for an induction motor is proposed in this paper. The drive used for this scheme is an open-end winding induction motor which can be obtained by separating the neutral connections of any general three-phase induction motor. The proposed scheme uses two three-level inverters, with asymmetric DC link voltage, feeding the induction machine from both sides and can generate voltage space vector locations similar to a conventional seven-level inverter. The four-level scheme is based on the use of only those space vector combinations of the seven-level inverter, which generate zero common mode voltage in the machine phase voltages. The proposed four-level inverter scheme requires only two isolated DC links as compared to the conventional diode-clamped four-level inverter scheme, which needs three isolated power supplies. The common mode voltage, in the pole voltages of the proposed four-level inverter, is significantly lower than that of the conventional four-level inverter while the machine phase voltages have zero common mode content. The proposed power circuit bus structure is simple to fabricate when compared to the conventional four-level inverter. A SVPWM scheme is presented, which generates the inverter gate switching signals from sampled amplitudes of reference phase voltages. The proposed four-level inverter scheme is implemented of a 1.5 kW open-end winding induction motor and the experimental results are presented.

Introduction

The multi-level inverters have been attracting major attention from academia as well as industrial sector, since they had been first introduced in 1981 [1]. Different multi-level topologies are proposed and studied extensively for drive applications as well as utility applications [2 - 4], but the practical applications in industrial sector didn't grow significantly beyond three-level schemes because of the circuit complexities of multi-level configurations and complicated control requirements. These multi-level inverters can be grouped into four main groups: Diode clamped or neutral point clamped inverter configurations, H-bridge cascaded configurations, flying capacitor topologies and multi-level inverter configurations obtained with feeding induction motor from both sides [5 - 6]. The four-level inverter schemes based on the diode clamped topologies are proposed in [7 - 9]. These schemes have inherent problem of capacitor voltage unbalance associated with the diode-clamped inverter topologies. More attention is focused on hardware modifications or control strategies to balance the capacitor voltages [8, 9].

A multi-level inverter configuration is proposed in this paper, which can produce the voltage space vectors equivalent to a conventional four-level inverter. The scheme uses an open end winding induction motor, supplied by two three-level inverters and each three-level inverter is a cascaded combination of two two-level inverters with asymmetrical DC link voltage [10, 11]. Higher resolution voltage space vector generation with cascaded inverters fed from asymmetric DC link have been preseneted in [12, 13]. The multi-level inverter configuration (with asymmetric DC link), proposed in this paper, generates space vector locations similar to a conventional seven-level inverter. If only certain space vector combinations, of this seven-level inverter, which produce zero common mode voltage in the phase voltages, are selected for inverter switching, the resultant space vector configuration represents a four-level space vector structure. This is the basic principle on which the proposed four-level inverter is based. The proposed inverter scheme results in lesser common mode voltages in the pole voltages of the inverter and zero common mode voltage in the machine phase voltages. The advantages of the proposed scheme, over conventional four-level inverter scheme are presented. A SVPWM scheme is used to generate the modulating signals for the proposed four-level inverter, directly from the sampled amplitudes of reference voltages [14, 15]. The proposed four-level inverter scheme is implemented on a 1.5 kW induction motor with open-end winding and the experimental results are presented.

Seven-level inverter configuration

The seven-level inverter configuration consists of two three-level inverters (inverter-A and inverter-B), connected to an open-end winding induction motor as shown in Fig. 1. The DC link voltage of the top two-level inverters (INV1 for inverter-A and INV3 for inverter-B), is $(1/3) \times V_{dc}$, while the DC link voltage of the bottom two-level inverters (INV2 for inverter-A and INV4 for inverter-B), is $(1/6) \times V_{dc}$, where V_{dc} is the DC link voltage of the conventional two-level inverter. Isolated power supplies are used for individual DC links, to suppress the common mode currents in the phase windings [12]. The pole voltages of the A, B and C phase of the inverter-A are denoted as V_{A2O}, V_{B2O} and V_{C4O} respectively while the pole voltages of the A, B and C phases of inverter-B are denoted as V_{A4O}, V_{B4O} and V_{C4O}.

Operation of the seven-level inverter

The pole voltage in any leg of three-level inverter is decided by the states of the switching devices in that particular inverter leg. For example, when the switches S_{11} and S_{21} are on, the pole voltage is equal to $V_{dc}/2$. When S_{14} and S_{21} are on, the pole voltage V_{A2O} is equal to $V_{dc}/6$, while when switching devices S_{24} is on, the pole voltage V_{A2O} is equal to zero. Thus, the poles of inverter-A and inverter-B can independently attain voltage levels of $V_{dc}/2$, $V_{dc}/6$ or zero volts. The pole voltages of the inverter-A and inverter-B

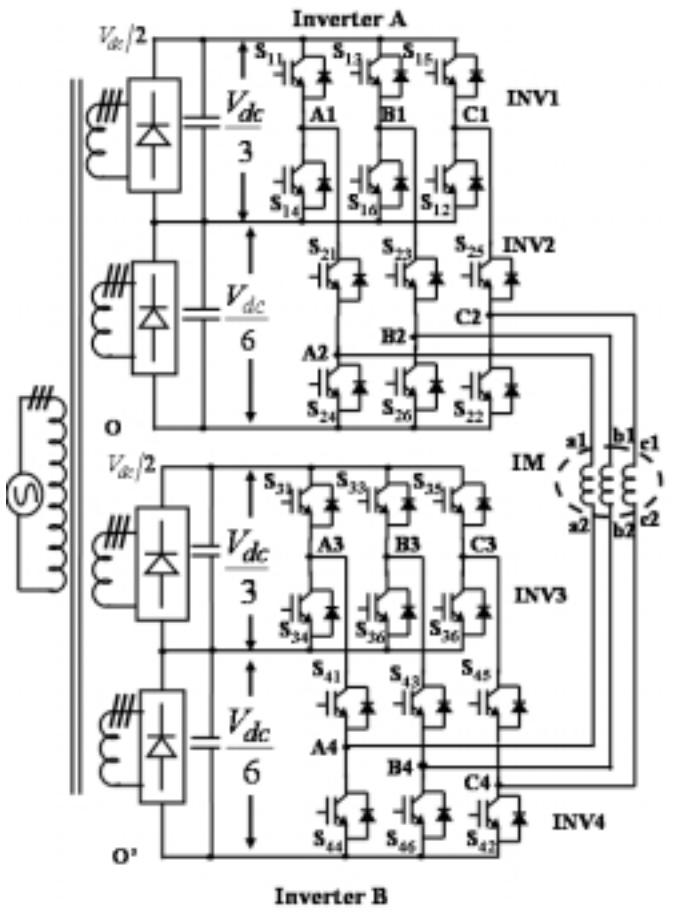


Fig. 1: The schematic of the seven-level inverter drive

Table 1: Pole voltages of inverter-A and inverter-B and resulting phase voltage across phase windings

Pole voltage of phase-A of Inverter-A, V_{A20}	Pole voltage of phase-A of Inverter-B, $V_{A40'}$	Phase voltage across the winding of induction motor, V_{A2A4}	Phase-A voltage Level
$V_{dc}/2$	0	$+ V_{dc}/2$	6
$V_{dc}/2$	$V_{dc}/6$	$+ V_{dc}/3$	5
$V_{dc}/6$	0	$+ V_{dc}/6$	4
0	0	0	3
0	$V_{dc}/6$	$- V_{dc}/6$	2
$V_{dc}/6$	$V_{dc}/2$	$- V_{dc}/3$	1
0	$V_{dc}/2$	$- V_{dc}/2$	0

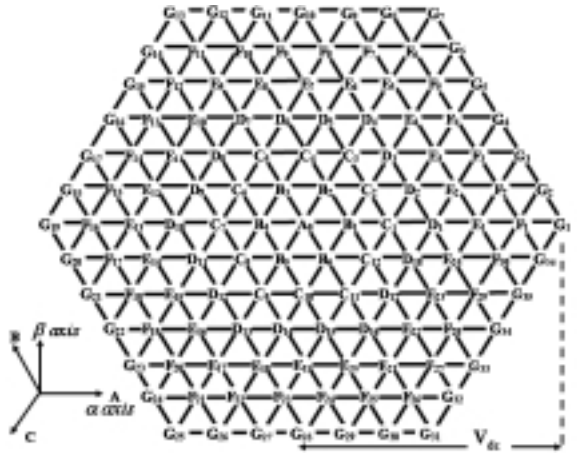


Fig. 2: Space vector locations of seven-level inverter scheme

legs determine the resultant voltage across the phase windings, in the respective leg, of the induction motor. Assuming that the points *O* and *O'* are connected, the voltage across the phase windings of induction motor can be written as

$$V_{A2A4} = V_{A20} - V_{A40'}$$

$$V_{B2B4} = V_{B20} - V_{B40'} \quad (1)$$

$$V_{C2C4} = V_{C20} - V_{C40'}$$

Different levels of phase voltages can be synthesized by using various combinations of pole voltages of three-level inverters (inverter-A and inverter-B). For example, when inverter-A pole voltage, V_{A20} and inverter-B pole voltage $V_{A40'}$ is $V_{dc}/2$ volts and zero respectively, the resultant voltage, V_{A2A4} is equal to $V_{dc}/2$. When V_{A20} and $V_{A40'}$ are equal to $V_{dc}/2$ and $V_{dc}/6$, the resultant voltages across the phase-A is equal to $V_{dc}/3$. Similarly, the resultant phase voltages of magnitude $V_{dc}/6$, 0, $- V_{dc}/6$, $- V_{dc}/3$, $- V_{dc}/2$ can be synthesized by appropriately switching the switching devices. The different levels of inverter-A and inverter-B pole voltages and the resulting phase voltage across the phase-A of the induction motor are summarized in Table 1.

The space vector representation of resultant machine phase voltage

The voltage space vector V_{SR}, resulting from the voltages across the three-phase winding of induction motor, separated by 120° in space is defined as,

$$V_{SR} = V_{A2A4} + V_{B2B4} \times e^{j120°} + V_{C2C4} \times e^{j240°}$$
$$= (V_{A2O} - V_{A4O'}) + (V_{B2O} - V_{B4O'}) \times e^{j120°} \quad (2)$$
$$+ (V_{C20} - V_{C40'}) \times e^{j240°}$$

The space vector locations can be determined for all combinations of phase voltage levels of A, B and C phases and are represented by the space vector diagram shown in the Fig. 2. There are in total 343 space vector combinations, which result in the 127 space vector locations and 216 triangular sectors.

Voltage ratings of the switching devices

The voltage rating of the switching devices is decided by the "off state" voltage across the switching device. For example, for Phase-A, when the pole voltage of inverter-A or inverter-B is at voltage level $V_{dc}/2$, the voltage across the bottom switching devices, S_{24}, S_{44} (of inverter-A and inverter-B respectively) is $V_{dc}/2$. Thus these switches shall be rated to block the voltage of magnitude $V_{dc}/2$ volts. The "off state" voltage across the switching devices in the top two-level inverters, (S_{11}, S_{14}, S_{31}, S_{34}, etc) is $V_{dc}/3$ and therefore these switching devices shall be rated to block voltage of magnitude $V_{dc}/3$ volts. The switching scheme is selected such that, when the bottom-switching device in any leg (for example, S_{24}, S_{44} for leg-A) is on, the bottom switches in the top two-level inverter (S_{14}, S_{34} for leg-A) shall be made on. Thus voltage across the top switching devices of bottom two-level inverters (S_{21}, S_{41}) is equal to $V_{dc}/6$. These voltage ratings of various switching devices are summarized in Table 2, for the seven-level inverter configuration.

Table 2: Voltage rating of switching devices	
Switching Device	Voltage Rating, volt
S_{11}, S_{13}, S_{15}, S_{14} S_{16}, S_{12} S_{31}, S_{33}, S_{35}, S_{34} S_{36}, S_{32}	$V_{dc}/3$
S_{21}, S_{23}, S_{25}, S_{41}, S_{43}, S_{45}	$V_{dc}/6$
S_{24}, S_{26}, S_{22}, S_{44}, S_{46}, S_{42}	$V_{dc}/2$

Proposed four-level voltage space phasor generation with common-mode voltage elimination

The common mode voltage generated in the pole voltage of inverter-A is expressed as [16],

$$V_{CM1} = (V_{A2O} + V_{B2O} + V_{C2O})/3 \quad (3)$$

while the common mode voltage generated in the pole voltage of inverter-B is expressed as

$$V_{CM2} = (V_{A4O} + V_{B4O'} + V_{C4O'})/3 \quad (4)$$

Then the resultant common mode voltage in the motor phase winding is,

$$V_{CM} = V_{CM1} - V_{CM2} \quad (5)$$

Fig. 3 shows the pole voltages, phase voltage across the phase windings, the corresponding common mode voltages in the pole voltages of inverter-A and inverter-B and the resultant common mode voltage in the phase voltages for the seven-level inverter. Unless isolation transformers are used to isolate the DC links from both sides, these common mode voltages in the phase windings may result into large triplen (common-mode) currents in the motor phases [12]. The isolation transformers are bulky, and also add up to the overall cost of the drive.

It can be seen from Fig. 3 that certain space vector combinations of the seven-level inverter generate zero common mode voltage, (Fig. 3e), in the phase voltage of the induction motor. If only these space vector combinations are used for inverter switching, the common mode voltage can be completely eliminated from the machine phase voltages. These space vector combinations (which have zero common mode voltage in phase voltages, V_{CM}) represent a four-level structure, as shown in Fig. 4, and are grouped according to the common mode voltage they generate in the pole voltages of inverter-A (V_{CM1}) and inverter-B (V_{CM2}), as shown in Table 3. As the common mode voltages are not present in the

Table 3: Space vector combinations of seven-level inverter, which result in zero common mode voltage in the phase voltages		
Space vector combinations of seven-level inverter	V_{CM1}, V_{CM2}	V_{CM}
342, 243, 234, 324, 423, 432	$V_{DC}/18$	0
153, 135, 315, 513, 531, 351 540, 450, 261 162, 054, 045 126, 216, 405, 504, 612, 621	$2*V_{DC}/9$	0
414, 441, 144, 252, 225,522 630, 360, 063, 036, 306, 603	$V_{DC}/6$	0
333	0	0

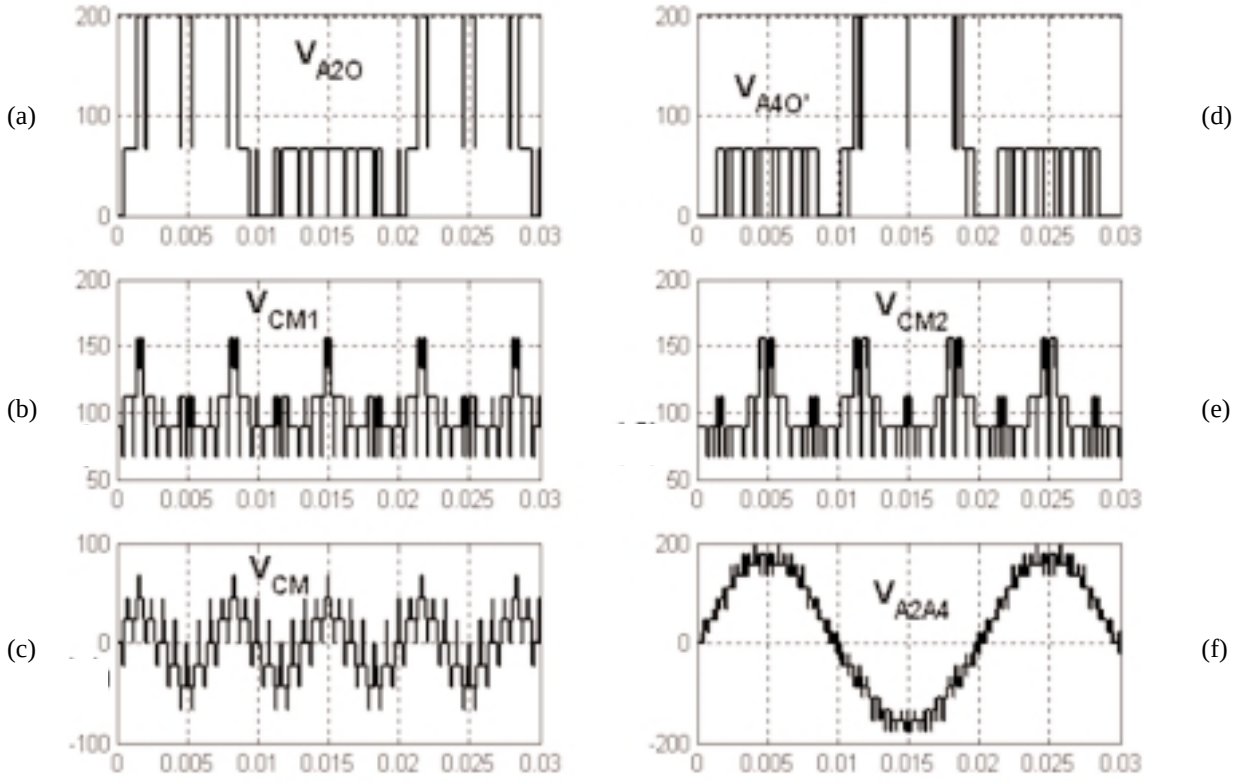


Fig. 3: Operation of the seven-level inverter, (a) Pole voltage V_{A2O} , (b) Pole voltage, $V_{A4O'}$, (c) V_{CM1}, (d) V_{CM2}, (e) V_{CM}, (f) V_{A2A4}

phase windings, the need for isolated DC links from both sides is also eliminated in the proposed structure. The modified power schematic of the proposed four-level inverter drive is shown in Fig. 5.

The space vector combinations, listed in Table 3, produce equal common mode voltage in the pole voltages of inverter-A and inverter-B. Thus the resultant common mode voltage across the machine phase is zero.

As shown in Fig. 4, the maximum amplitude of inverter vectors is equal to $\sqrt{3}V_{dc}/2$. Thus the maximum reference space vector possible in the linear range of modulation with this four-level inverter configuration with a total DC link voltage of $V_{dc}/2$ is

$$V_{SR\_max} = \sqrt{3}/2 \times \sqrt{3}V_{dc}/2 = (3/4)V_{dc} \quad (6)$$

The corresponding peak value of fundamental component in the phase voltage is

$$V_{peak\_max} = (2/3) \times 3V_{dc}/4 = V_{dc}/2 \quad (7)$$

This is the same as the maximum peak amplitude of phase voltage generated by conventional two-level inverter with Sine-PWM (i.e. 15 % less than what can be obtained with Space Vector PWM) [16]. This can be compensated with an additional voltage boost of 15% to the individual DC links [16]. Therefore, in the present work, the DC link voltage of top two-level inverters (of cascaded three-level inverters) is increased to $(2/\sqrt{3}) \times V_{dc}/3$ and of bottom two-level inverters to $(2/\sqrt{3}) \times V_{dc}/6$ (Fig. 5). Thus the maximum peak amplitude of phase voltage is

$$V_{peak\_max} = (2/\sqrt{3}) \times V_{dc}/2 = V_{dc}/\sqrt{3} = 0.577V_{dc} \quad (8)$$

With the additional boost by a factor of $2/\sqrt{3}$ in the DC link voltage, the magnitudes of the various space vector combinations for the proposed four-level inverter are shown in Fig. 6. It is to be noted that, with the modified DC link voltages, the common mode voltage in the pole voltages will be boosted by 15 %, as shown in Fig. 6.

Advantages of the proposed four-level inverter scheme over the diode-clamped configuration

Fig. 7 shows a four-level inverter configuration based on the diode clamped multi-level topology and the corresponding space vector combinations [7]- [9]. The drive requires six switching devices with the blocking voltage rating of (where V_{dc} is the total DC link voltage) and four clamping diodes per phase. The drive system requires three isolated power supplies for charging each of the three capacitors, as shown in Fig. 7 [7]-[9].

The four-level inverter configuration, proposed in this paper, requires eight switches per phase. The blocking voltage ratings of various devices are shown in Table 2. The four-level inverter drive (Fig. 5), proposed in this paper, requires only two isolated power supplies, while the conventional diode clamped scheme requires three isolated power supplies. The significant saving in the cost of isolation transformer can be achieved here. Special hardware additions or control strategy is required to balance the capacitor voltages in the conventional diode clamped schemes, with only one front end-rectifier [8], [9]. The power circuit bus structure is simple to fabricate for the proposed work when compared to the conventional four-level inverter. The clamping diodes used in the

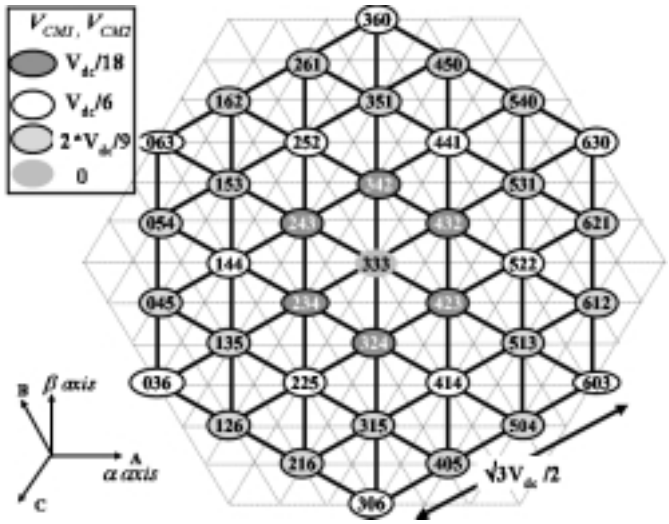


Fig. 4: Space vector combinations of seven-level inverter, which result in zero common mode voltage in the phase voltages

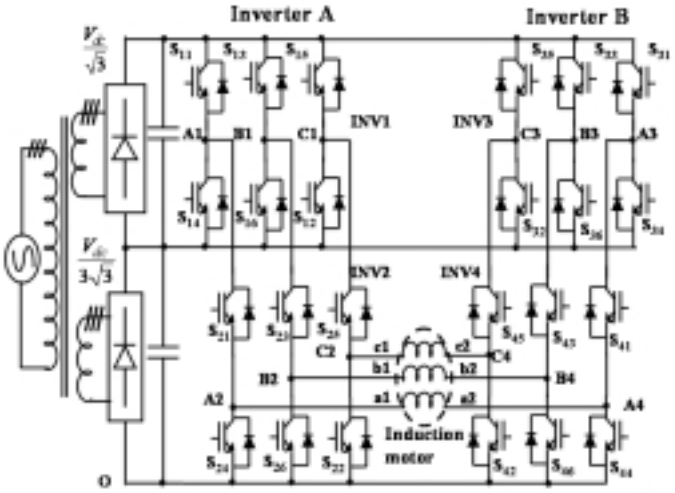


Fig. 5: The schematic of the proposed four-level inverter scheme

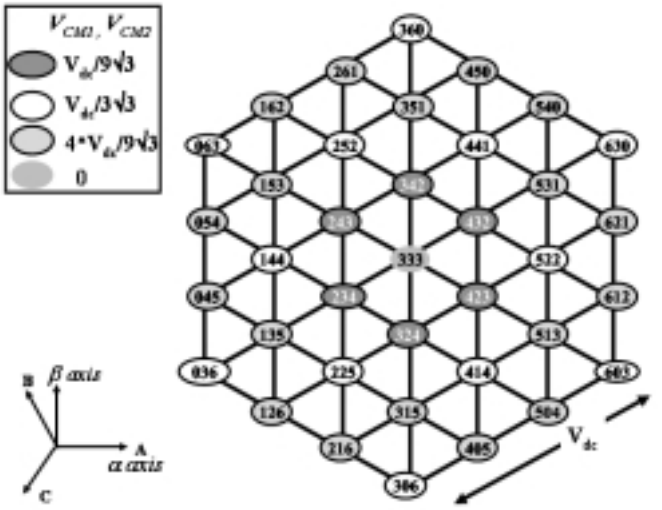
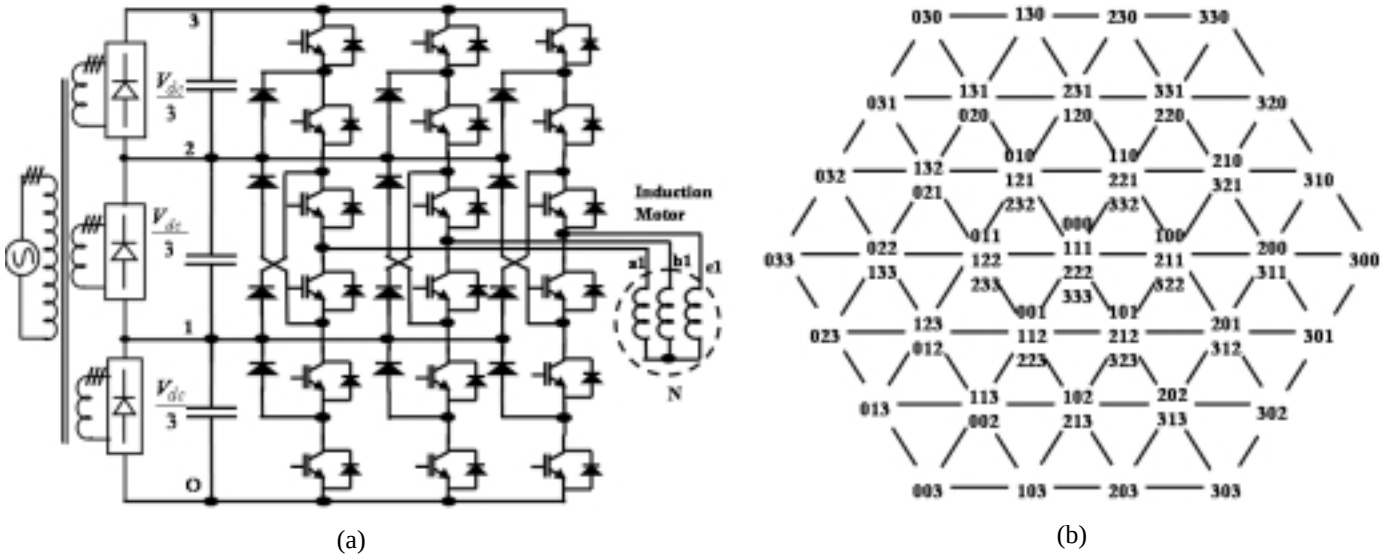


Fig. 6: Space vector locations of the proposed four-level inverter



(a) (b)

Fig. 7: Conventional four-level inverter, (a) power schematic (b) space vector combinations

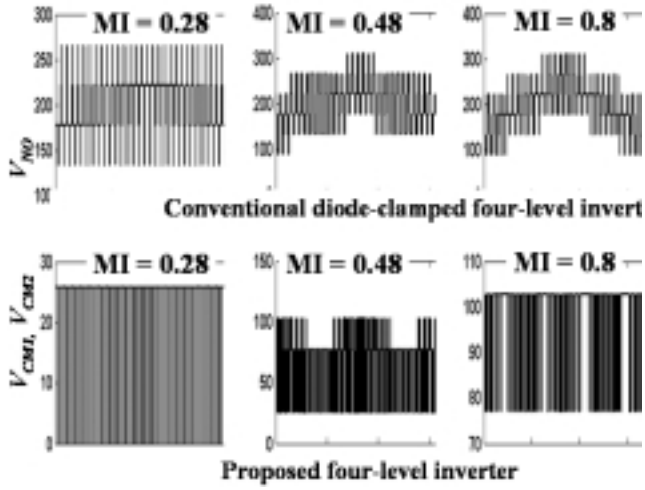


Fig. 8: The common mode voltage generated by conventional four-level inverter and proposed four-level inverter for various modulation indices (MI: modulation index)

NPC configuration are not required, thus the total device count also comes down for the same level of voltage generation, for the proposed scheme.

The common mode voltages between neutral point 'N' and the reference point 'O' for various space vector combinations of the conventional four-level inverter are shown in Table 4. These space vector combinations of conventional four-level inverter are grouped in various groups depending on the common mode voltage that they generate in the pole voltages (Table 4). The maximum value of the common mode voltage is equal to V_{dc} and special measures, like redundant state selection logic, have to be implemented, to reduce the common mode voltages [8, 9]. The maximum value of the common mode voltage in the pole voltages of the proposed four-level scheme is equal to $4*V_{dc}/(9\sqrt{3})$ (i.e.$0.256 \times V_{dc}$), while the machine phase voltages have zero common mode voltages.

The common mode voltage V_{NO}, generated by the conventional four-level inverter, and V_{CM}, generated by proposed four-level inverter (simulation waveforms with $V_{dc} = 400$) for various modulation indices are shown in Fig. 8. The modulation indices- 0.28, 0.48 and 0.8 corresponds to the operating condition when the reference space vector is traversing through inner-layer, middle-layer and outer-layer of inverter voltage space vector structure respectively. It is clear from Fig. 8 that there is significant reduction in the common mode voltages generated by the proposed four-level inverter over the conventional four-level inverter in the entire operating range (ref Table 3 and Table 4).

Pulse width modulation scheme for the proposed four-level inverter drive

A reference space vector of magnitude equal to 'V_{SR}' and rotating in the space at fundamental frequency, is sampled at regular intervals 'T_S'. The sampled value of reference space vector is then used to determine the inverter switching vectors and the time for which these vectors are switched, in a sampling interval. For example, consider the sampling interval when the tip of the reference vector is in a sector formed by space vector locations 8'7'20' (Fig. 9). The space vector OY' can be synthesized by switching inverter vectors 8', 7' and 20' for appropriate time durations such that the volt-seconds produced by these vectors are equal to the volt-seconds generated by the reference space vector OY', in a sampling period, and thus minimum switching of inverter legs is ensured.

Mapping of the reference space vector of proposed inverter to the reference space vector of conventional four-level inverter

The voltage space phasor locations, of proposed four-level inverter (Fig. 6), are compared with the space vector locations of a conventional four-level inverter with DC link voltage of V_{dc}, as shown in Fig. 9.

Consider a sampling instant when a reference space vector OY' is at an angle 'α' with respect to A phase axis. The reference space vector can be realized by switching appropriate vectors corresponding to the triangular sector. From Fig. 9, it can be noted that the triangular sectors for the proposed four-level inverter structure are leading by an angle 30°, with respect to the respective triangular sectors of the conventional four-level inverter structure (Fig. 9a). The length of the side of the triangular sector of the proposed four-level inverter (with a 15 % voltage boost in the DC link) is equal to that of triangular sector of conventional four-level inverter.

Table 4: Common mode voltage generated by the space vector combinations of a conventional four-level inverter		
Group	Common mode voltage,	Space vector combinations of four-level inverter
A	0	000
B	$V_{DC}/9$	100, 010, 001
C	$2*V_{DC}/9$	110, 011, 101, 200, 020, 002
D	$3*V_{DC}/9$	111, 210, 021, 012, 102, 120,201, 300, 030, 003
E	$4*V_{DC}/9$	211, 121, 112, 220, 022, 202, 310, 130, 031, 013, 103, 301
F	$5*V_{DC}/9$	221, 122, 212, 311, 131, 113, 320, 230, 032, 023, 203, 302
G	$6*V_{DC}/9$	222, 321, 231, 132, 123, 213, 312, 330, 033, 303
H	$7*V_{DC}/9$	322, 232, 223, 331, 133, 313
I	$8*V_{DC}/9$	332, 233, 323
J	V_{DC}	333

Therefore, the corresponding space vectors (forming a triangular sector) of the proposed inverter, are leading with respect to that of the conventional system by an angle 30° (Fig. 9). For example space vector location O-19' (Fig. 9b) is leading O-19 (Fig. 9a) by 30°. Therefore, the reference space vector of the conventional system can be obtained from the reference space vector of the proposed four-level inverter system as follows,

$$V_{SR1} = V_{SR} \times e^{-j30°} \quad (9)$$

The reference space vector 'V_{SR1}' is used to generate the PWM signals for a conventional four-level inverter. The inverter voltage space vectors generated by the controller are then mapped to the vectors of the proposed four-level inverter as described in the following sub-section.

Generation of voltage space vectors of proposed four-level inverter from the voltage space vectors of conventional four-level inverter

A space phaser based PWM algorithm is used to generate the switching times for the vectors of conventional four-level inverter [14, 15]. The inverter switching vectors and the time duration for which the inverter space vectors are to be switched, during a switching interval T_S, are determined directly from sampled amplitude of reference voltage [14, 15]. Thus it avoids the use of look up table for sector identification and increases the speed of computation, making it useful for real time implementation. The algorithm is explained in appendix 1. A digital logic, as described in the next sub-section, is used to translate the vectors generated, by PWM algorithm, for the conventional four-level structure to the vectors of the proposed four-level inverter drive. As shown in Fig. 9, a unique mapping is defined between the vector locations of a conventional four-level inverter and that of the proposed four-level inverter system. For the reference space vector OY, the conventional four-level PWM algorithm generates the timings for switching the vectors 8, 7 and 20 in the given sampling interval. These vectors can be uniquely transferred to the voltage space vectors of the proposed four-level inverter, which are shown as 8', 7' and 20' for generating the reference space vector OY'. Vectors 8', 7' and 20' are realized by switching appropriate switching states from inverter-A and inverter-B (Fig. 9). Thus the modulation scheme involves the following steps:

– sample the reference space vector V_{SR} with a sampling interval T_s;
– compute the modified reference vector V_{SR1} using (9);
– determine the switching times from the modified reference space phasors (Refer to appendix-1);
– translate the conventional four-level inverter vectors, forming the mapped triangular sector, to actual vectors of the proposed four-level inverter.

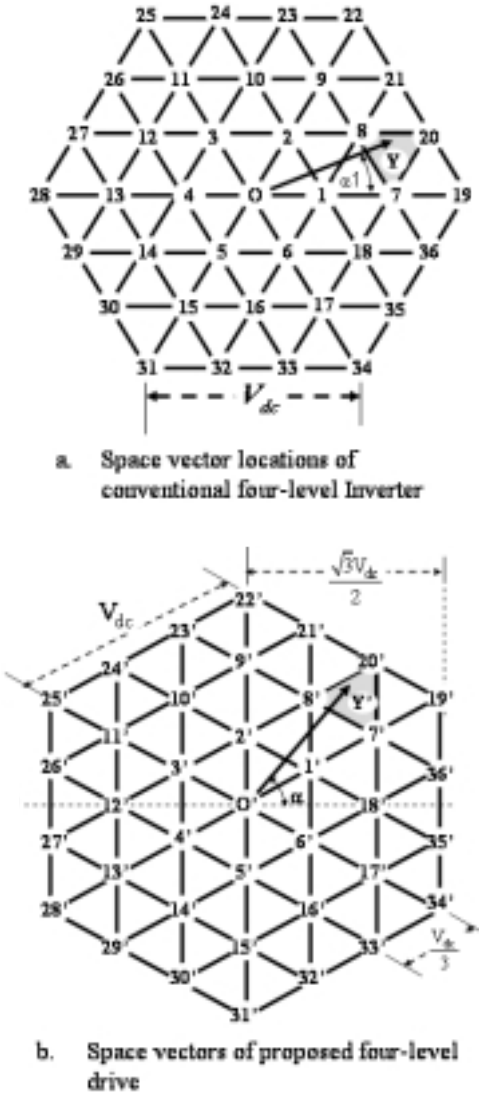


Fig. 9: Transformation of the actual reference vector OY' to a conventional four-level inverter space vector, OY

Generation of gate signal for inverter-A and inverter-B

The PWM algorithm is implemented using a digital signal processor TMS320C24. The values of T_{ga}, T_{gb}, T_{gc}, generated by PWM algorithm, are used in compare units of DSP to generate

pwm_a, *pwm_b* and *pwm_c* signals (refer to appendix-1). The carrier index, I_a, I_b and I_c for three phases is taken out from DSP I/O ports. Depending on the values of carrier index, I_a (taken out through DSP's digital I/O pins A2 and A1) for A phase, and *pwm_a* signal, value of the phase-A level signal *A_Level*, is assigned as per following Table 5 (refer to appendix-1).

Similarly, B and C phase level signals, i.e. *B_Level* and *C_Level* are generated from I_b, *pwm_b* and I_c, *pwm_c* respectively, as per the logic shown in Table 5. The voltage space vectors of conventional four-level inverters are determined from *A_Level*, *B_Level* and *C_Level* signals as shown in Table 6.

The inverter voltage space vector of conventional four-level inverter is transformed to the space vector combinations of the proposed four-level inverter (Fig. 9). The decoding logic for generation of gate signals for various switching devices of proposed four-level inverter is shown Table 7. The complete decoding logic of Table 5, 6 and 7 is implemented using PALCE22V10 devices.

Table 5: Generation of level signal *A_Level* from the carrier index, I_a and *pwm_a* signal

Carrier index, I_a	*A2*	*A1*	*pwm_a*	*A_Level*
1	1	0	1	3
			0	2
2	0	1	1	2
			0	1
3	0	0	1	1
			0	0

Table 6: Generation of voltage space vector of conventional four-level inverter from A_Level, B_Level and C_Level signals

[A_Level B_Level C_Level]	Voltage space vector of conventional four-level inverter	*[A_Level B_Level C_Level]*	Voltage space vector of conventional four-level inverter
000 / 111/ 222 / 333	0	300	19
100 / 211 / 322	1	310	20
110 / 221/ 332	2	320	21
010 / 121 / 232	3	330	22
011 / 122 / 233	4	230	23
001 / 112 / 223	5	130	24
101 / 212 / 323	6	030	25
200 / 311	7	031	26
210 / 321	8	032	27
220 / 331	9	033	28
231 / 120	10	023	29
131 / 020	11	013	30
132 / 021	12	003	31
133 / 022	13	103	32
123 / 012	14	203	33
113 / 002	15	303	34
102 / 213	16	302	35
202 / 313	17	301	36
201 / 312	18		

Experimental results and discussion

The proposed scheme is tested on a 1.5 kW three-phase induction motor drive with V/f control for different modulation indices covering the entire speed range. The motor parameters are given in appendix-2. The DC link voltage of around 100 V is used for top two-level inverters and 50 V for bottom two-level inverters. In the proposed PWM scheme, the dead-bands of the inverter legs are properly tuned, to avoid any common mode voltage generated due to dead-band mismatch. The modulation index is varied from low modulation index to over modulation region. The results are presented in Fig. 10 to Fig. 13. The carrier frequency used for PWM generation is maintained at 1.2 kHz.

The pole voltage waveforms of inverter-A, V_{A2O} and inverter-B, V_{A4O} and the difference between V_{A2O} and V_{A4O} (i.e $V_{A2O} - V_{A4O}$), for modulation index 0.28 (i.e. when the reference space vector is in the inner layer), are shown in Trace-1, Trace-2 and Trace-3 of Fig. 10a, respectively. The phase-A current and the resultant phase voltage across phase-A winding of induction motor are shown in Trace-1 and Trace-2 of Fig.10b respectively. Fig. 10c shows the normalized harmonic spectrums of the pole voltage and phase voltages. Both the pole voltage and the phase voltage show the absence of triplen voltage components. The pole voltage shows significant even harmonics, which are absent in the phase voltage waveforms. The even harmonics cancel each other in phase voltage and the fundamental component gets added up. As the pole voltages do not have common mode voltage, the difference between V_{A2O} and V_{A4O} (i.e. Trace-3 of Fig. 10a) is equal to the phase voltage across the motor phase V_{A2A4} (Trace-1 of Fig. 10b). Similarly, the pole voltage waveforms for Modulation Index = 0.48 (when the reference space vector is in outer layer) are shown in Fig. 11a. The resultant phase voltage and phase current are shown in Fig. 11b. Fig. 11c show the normalized harmonics spectrum of pole voltage and phase voltage. Here also the pole voltages and phase voltages do not contain any triplen harmonic order. Similar to the previous case, the difference in the pole voltages (Trace-3 of Fig. 11a) is equal to the phase voltage across the induction motor winding (Trace-1 of Fig. 11b).

The performance of the proposed four-level inverter scheme is checked for the inverter operation in outer-most sectors (modulation index 0.8). The pole voltages of inverter-A, V_{A2O} (Trace-1), inverter-B, V_{A4O} (Trace-2) and their difference (Trace-3) are shown in Fig. 12a while the phase voltage (Trace-1) and phase current (Trace-2) are shown in Fig. 12b. The normalized harmonic spectra of pole voltages and phase voltages are shown in Fig. 12c. Again pole voltage frequency spectrum indicates presence of even harmonics, which are absent in the phase voltages. The motor is speeded up to over-modulation range and the similar observations are taken. Fig.13a shows the pole voltages and their difference (Trace-1, Trace-2 and Trace-3 respectively) in the over-modulation region. The phase voltage (Trace-1) and phase current (trace-2) during over-modulation are shown in Fig.13b. Fig. 13c shows the normalized harmonic spectrums of the pole voltages and the phase voltage. Here also, it can be noted that the triplen components are absent. The phase voltages as well as line voltages show the 5^{th} and 7^{th} harmonic components, which are apparent in the over-modulation range.

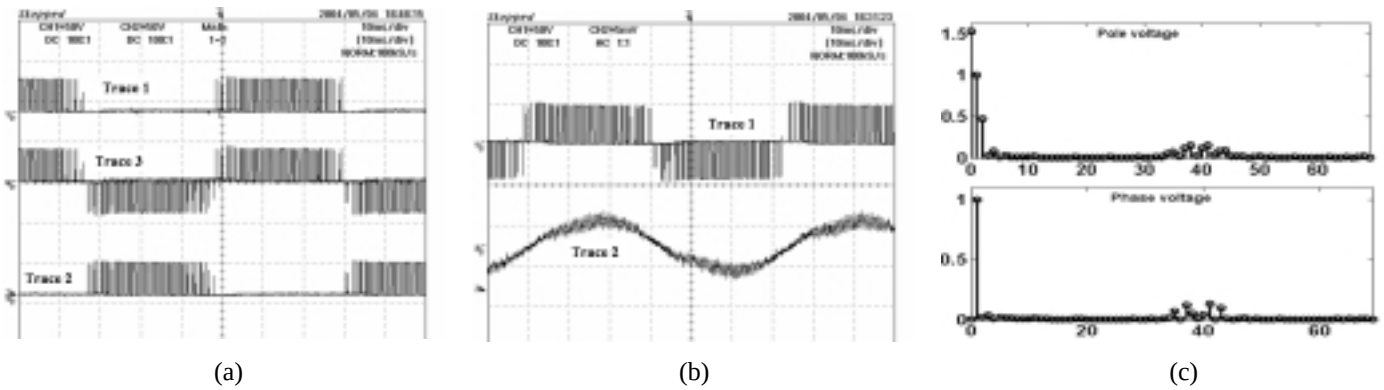
In the entire range of modulation, the elimination of the common mode voltage in the phase voltage is proved from the fact that the difference of the pole voltages is equal to the phase voltage across the induction motor windings.

Conclusion

A four-level inverter scheme is proposed in this paper for an open-end winding induction motor drive. The proposed four-level inverter drive requires only two isolated passive front-end power

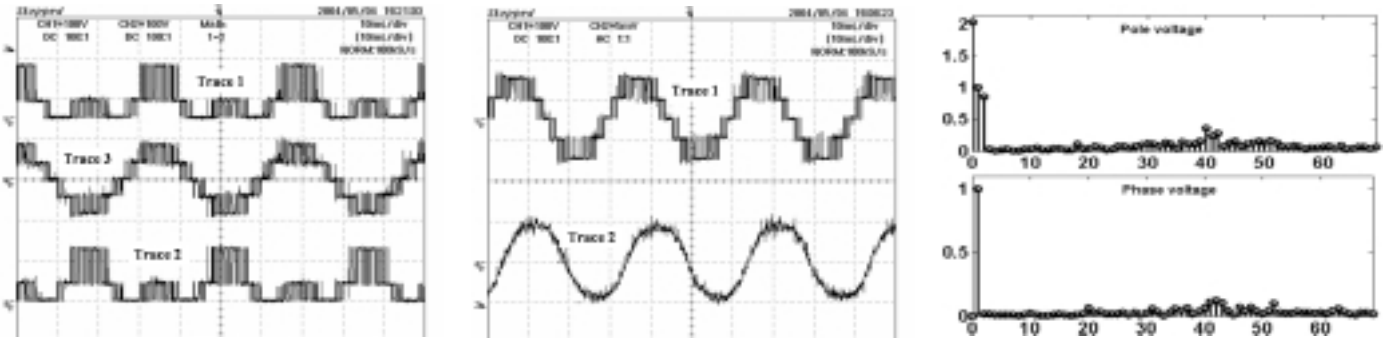
Table 7: Decoding of space vector combination of proposed four-level inverter and corresponding switching signals for inverter-A and inverter-B

Voltage space vector of conventional four-level inverter (Table 5)	Space vector combination for proposed four-level inverter	Gate signals for inverter-A						Gate signals for inverter-B					
		S11	S21	S13	S23	S15	S25	S31	S41	S33	S43	S35	S55
0	333	0	0	0	0	0	0	0	0	0	0	0	0
1	432	0	1	0	0	0	0	0	0	0	0	0	1
2	342	0	0	0	1	0	0	0	0	0	0	0	1
3	243	0	0	0	1	0	0	0	1	0	0	0	0
4	234	0	0	0	0	0	1	0	1	0	0	0	0
5	324	0	0	0	0	0	1	0	0	0	1	0	0
6	423	0	1	0	0	0	0	0	0	0	1	0	0
7	531	1	1	0	0	0	1	0	1	0	0	1	1
8	441	0	1	0	1	0	1	0	0	0	0	1	1
9	351	0	0	1	1	0	1	0	0	0	1	1	1
10	252	0	0	1	1	0	0	0	1	0	1	0	1
11	153	0	1	1	1	0	0	1	1	0	1	0	0
12	144	0	1	0	1	0	1	1	1	0	0	0	0
13	135	0	1	0	0	1	1	1	1	0	0	0	1
14	225	0	0	0	0	1	1	0	1	0	1	0	1
15	315	0	0	0	1	1	1	0	0	1	1	0	1
16	414	0	1	0	1	0	1	0	0	1	1	0	0
17	513	1	1	0	1	0	0	0	1	1	1	0	0
18	522	1	1	0	0	0	0	0	1	0	1	0	1
19	630	1	1	0	0	0	0	0	0	0	0	1	1
20	540	1	1	0	1	0	0	0	1	0	0	1	1
21	450	0	1	1	1	0	0	0	0	0	1	1	1
22	360	0	0	1	1	0	0	0	0	0	0	1	1
23	261	0	0	1	1	0	1	0	1	0	0	1	1
24	162	0	1	1	1	0	0	1	1	0	0	0	1
25	063	0	0	1	1	0	0	1	1	0	0	0	0
26	054	0	0	1	1	0	1	1	1	0	1	0	0
27	045	0	0	0	1	1	1	1	1	0	0	0	1
28	036	0	0	0	0	1	1	1	1	0	0	0	0
29	126	0	1	0	0	1	1	1	1	0	1	0	0
30	216	0	0	0	1	1	1	0	1	1	1	0	0
31	306	0	0	0	0	1	1	0	0	1	1	0	0
32	405	0	1	0	0	1	1	0	0	1	1	0	1
33	504	1	1	0	0	0	1	0	1	1	1	0	0
34	603	1	1	0	0	0	0	0	0	1	1	0	0
35	612	1	1	0	1	0	0	0	0	1	1	0	1
36	621	1	1	0	0	0	1	0	0	0	1	1	1



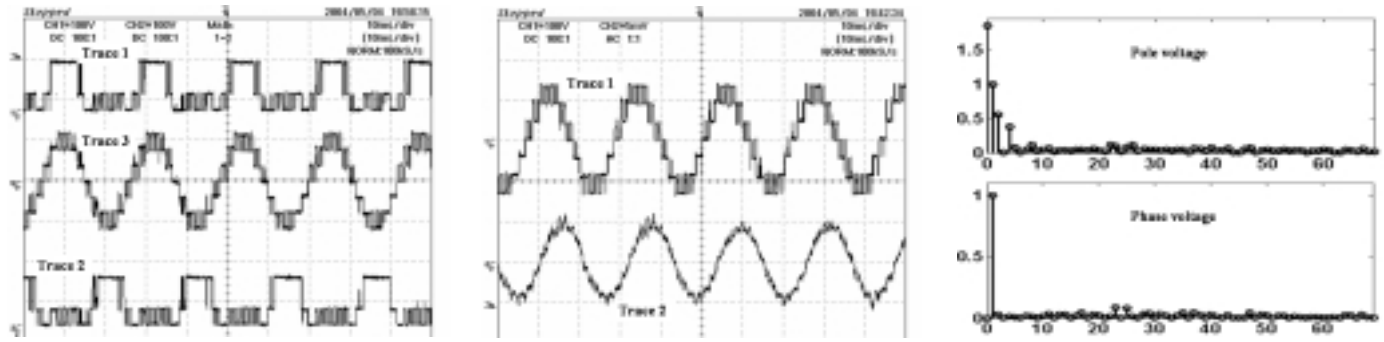
(a) (b) (c)

Fig. 10: The operation of four-level inverter in Layer-1 (Modulation index 0.28): (a) Pole voltages: Trace-1 Ł V_{A20}, Trace 2 Ł $V_{A40'}$, Trace 3 Ł (Trace 1 - Trace 2); Scale: X axis: 1div = 10ms, Y axis: 1 div = 50 V (b) Trace 1 Ł Phase voltage V_{A2A4} X axis: 1 div = 10 ms, Y axis: 1 div = 50 V; Trace 2 Ł Phase current; X axis: 1 div = 10 ms, Y axis: 1 div = 2A (c) Normalized harmonic spectrum for pole voltages and phase voltages (X axis: order of harmonics)



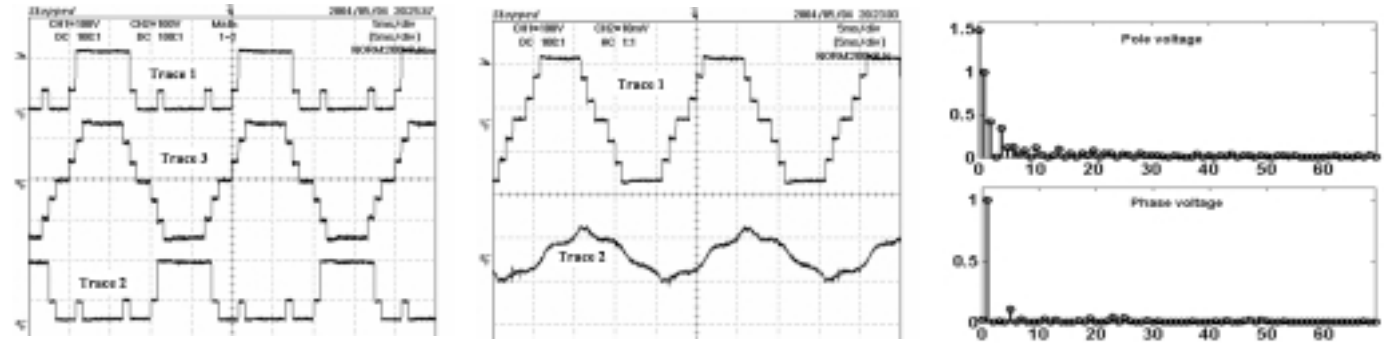
(a) (b) (c)

Fig. 11: The operation of four-level inverter in Layer-2 (Modulation index 0.48): (a) Pole voltages: Trace-1 – V_{A20}, Trace-2 – $V_{A40'}$, Trace 3 – (Trace 1- Trace 2) X axis: 1 div = 10 ms, Y axis: 1 div = 100 V; (b) Trace 1 – Phase voltage V_{A2A4}; X axis: 1 div =10 ms, Y axis: 1 div = 100 V; Trace 2 – Phase current; X axis: 1 div = 10 ms, Y axis: 1 div = 2A; (c) Normalized harmonic spectrum for pole voltages and phase voltages (X axis: order of harmonics)



(a) (b) (c)

Fig. 12: The operation of four-level inverter in Layer-3 (Modulation index 0.8): (a) Pole voltages Trace-1 – V_{A20}, Trace 2 – $V_{A40'}$, Trace 3 – (Trace 1- Trace 2); X axis: 1 div = 10 ms, Y axis: 1 div = 100 V; (b) Trace 1 – Phase voltage V_{A2A4}; X axis: 1 div = 10 ms, Y axis: 1 div = 100 V; Trace 2 – Phase current; X axis: 1 div = 10 ms, Y axis: 1 div = 2A; (c) Normalized harmonic spectrum for pole voltages and phase voltages (X axis: order of harmonics)



(a) (b) (c)

Fig. 13: The operation of four-level inverter in Over-modulation (Modulation index 1.1): (a) Pole voltages Trace-1 – V_{A20}, Trace 2 – $V_{A40'}$, Trace 3 – (Trace 1- Trace 2); X axis: 1div = 20 ms, Y axis: 1 div = 100 V; (b) Trace 1 – Phase voltage V_{A2A4} X axis: 1div = 20 ms, Y axis: 1 div = 100 V; Trace 2 – Phase current; X axis: 1div = 20 ms, Y axis: 1 div = 4A; (c) Normalized harmonic spectrum for pole voltages and phase voltages (X axis: order of harmonics)

supplies as compared to the conventional diode clamped scheme, which requires three isolated power supplies. The neutral point voltage fluctuations, associated with the diode clamped topology, are absent here, as the DC link capacitor does not carry the load currents. Also the clamping diodes used in the NPC configuration are not required. Although the number of switching devices are more than the conventional diode clamped four-level inverter, the device count comes down for the same level of voltage generation. The DC link voltage requirement for the proposed drive is approximately half to that of the conventional schemes, and hence, the device ratings for the propsed system will also get reduced, except for the bottom devices of the inverters. The bus structure of the proposed scheme is less complex compared to the conventional diode clamped four-level inverter scheme, because the present scheme is achievd by cascading the conventional two level inverter structure. The maximum value of the common mode voltage in the

pole voltages of the proposed four-level scheme is much less compared to the conventional diode clamped four-level inverter scheme.But the proposed scheme needs access to the neutral connection of the induction motor. Since the motor is fed from both the ends, matching of the switching devices with respect to on state drop and inverters dead time should be ensured, for proper reduction of the common mode voltage.

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Appendix 1: Algorithm for inverter leg switching time calculation for a '*n*' level Inverter scheme

1. Read V_{A2A4}, V_{B2B4} and V_{C2C4} values and find the reference space vector VSR using relation

$$V_{SR} = V_{A2A4} + V_{B2B4} \times e^{j120°} + V_{C2C4} \times e^{j240°} = V_{SR(\alpha)} + jV_{SR(\beta)}$$

2. Calculate the reference space vector VSR1 using transformation

$$V_{SR1} = V_{SR} \times e^{-j30°}$$

$$\therefore V_{SR1(\alpha)} + jV_{SR1(\beta)} = (V_{SR(\alpha)} + jV_{SR(\beta)} \times e^{-j30°}$$

3. Calculate the modified amplitudes of phase voltages V_{as}, V_{bs}, V_{cs} for the four-level PWM algorithm from V_{SR1}

$$\begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} = \begin{bmatrix} 2/3 & 0 \\ -1/3 & 1/\sqrt{3} \\ -1/3 & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_{SR1(\alpha)} \\ V_{SR1(\beta)} \end{bmatrix}$$

4. Determine switching vectors for three-level inverter using these modified amplitudes of reference phase described as below,

a. Convert the phase voltages V_{as}, V_{bs}, V_{cs} into equivalent time T_{as}, T_{bs}, T_{cs} where

$$T_{as} = V_{as} \times \frac{T_s}{V_{dc}/3}, T_{bs} = V_{bs} \times \frac{T_s}{V_{dc}/3}, T_{cs} = V_{cs} \times \frac{T_s}{V_{dc}/3}$$

b. Find out $T_{offset1}$ as $T_{offset1} = -(T_{max} + T_{min})/2$, where T_{max}, T_{min} are the maximum and minimum of T_{as}, T_{bs}, T_{cs}

c. Determine T^*_{as}, T^*_{bs} and T^*_{cs} as $T^*_{as} = T_{as} + T_{offset1}$, $T^*_{bs} = T_{bs} + T_{offset1}$, $T^*_{cs} = T_{cs} + T_{offset1}$

d. Determine the carrier indices I_a, I_b and I_c for A, B and C phase respectively.

if $T_{xs} > T_s/2$, $I_x = 1$,
elseif $T_s/2 > T_{xs} > -T_s/2$, $I_x = 2$
else $I_x = 3$

Where x = a, b, c

e. Determine T_{a_cross}, T_{b_croos} and T_{c_cross} as follows

$$T_{a\_cross} = (T_s/2) + T^*_{as} + ((I_a - 2)*T_s)$$

$$T_{b\_cross} = (T_s/2) + T^*_{bs} + ((I_b - 2)*T_s)$$

$$T_{c\_cross} = (T_s/2) + T^*_{cs} + ((I_c - 2)*T_s)$$

f. Sort T_{a_cross}, T_{b_croos} and T_{c_cross} to determine T_{first_cross}, T_{second_croos} and T_{third_cross}

The maximum of T_{a_cross}, T_{b_croos} and T_{c_cross} is T_{third_cross}

The minimum of T_{a_cross}, T_{b_croos} and T_{c_cross} is T_{first_cross}

And the remaining is T_{second_croos}

g. Assign *First_cross_phase*, *Second_cross_phase* and *Third_cross_phase* according to the phase which determines T_{first_cross}, T_{second_croos} and T_{third_cross}

h. If $(T_{third\_cross} - T_{first\_croos}) > T_s$, go to step l

i. Calculate $T_{offset2}$ as

$T_{middle} = T_{third\_cross} - T_{first\_croos}$

$T_0 = T_s - T_{middle}$ $\therefore$ $T_{offset2} = T_0/2 - T_{first\_cross}$

j. Determine (T_{ga}, T_{gb}, T_{gc})

$T_{ga} = T_{a\_cross} + T_{offset2}$, $T_{gb} = T_{b\_cross} + T_{offset2}$, $T_{gc} = T_{c\_cross} + T_{offset2}$

k. Go to step (5)

l. Over modulation

If $(T_{\_third\_cross} - T_{\_second\_cross}) < (T_{\_second\_cross\ s} - T_{\_first\_cross})$,

$T_{offset2} = -T_{\_first\_cross}$, else $T_{offset2} = T_s - T_{\_third\_cross}$

$T_{g\_first\_cross} = 0$, $T_{g\_second\_cross} = T_{\_second\_cross} + T_{offset2}$ $T_{g\_third\_cross} = T_s$

m. If $T_{g\_second\_cross} < 0$, $T_{g\_second\_cross} = 0$

n. If $T_{g\_second\_cross} > T_s$, $T_{g\_second\_cross} = T_s$

o. Determine T_{ga}, T_{gb}, T_{gc} by equating $T_{g\_first\_cross}$, $T_{g\_second\_cross}$ and $T_{g\_third\_cross}$ to T_{ga}, T_{gb}, T_{gc} depending on the phase, which determines first cross, second cross and third cross during the sampling interval.

5. The T_{ga}, T_{gb}, T_{gc} are used in compare units of DSP which generate *pwm_a, pwm_b and pwm_c*. Using the *pwm_a*, *pwm_b* and *pwm_c* signals and carrier index signals I_a, I_b and I_c, determine the vectors of conventional four-level inverter (refer to Table 5, 6).

6. Translate the voltage space vectors of conventional four-level inverters, generate the switching signals for inverter-A and inverter-B using digital logic presented in Table – 7.

7. Go to step 1

Appendix 2: Induction motor parameters

3 phase, 1.5 kW, 50 Hz, Poles: 4, Rated voltage: 230 V, *Rs* = 2.08 ohms, *Rr* = 1.19 ohms, *Lr* = 0.28 H, *Ls* = 0.28 H, M = 0.272 H

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