

Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC Link Capacitor Voltage Balancing for an Open-End Winding Induction Motor Drive

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Abstract—A dc link capacitor voltage balancing scheme along with common mode voltage elimination is proposed for an induction motor drive, with open-end winding structure. The motor is fed from both the ends with three-level inverters generating a five level output voltage space phasor structure. If switching combinations, with zero common mode voltage in the pole voltage, are used, then the resultant voltage space vector combinations are equivalent to that of a three-level inverter. The proposed inverter vector locations exhibit greater multiplicity in the inverter switching combinations which is suitably exploited to arrive at a capacitor voltage balancing scheme. This allows the use of a single dc link power supply for the combined inverter structure. The simultaneous task of common mode voltage elimination with dc link capacitor voltage balancing, using only the switching state redundancies, is experimentally verified on a 1.5-kW induction motor drive.

Index Terms—Capacitor voltage balancing, common mode voltage elimination, multilevel inverters.

I. INTRODUCTION

THE three-level neutral-point clamped (NPC) inverter will have dc link capacitor voltage balancing problem, unless it is controlled by separate voltage balancing scheme [1], [2]. The dc link capacitor voltage mismatch can lead to higher voltage stress on the power devices. The dependence of the neutral point voltage variation on the system parameters like load currents, load power factor, dc link capacitors etc., have been extensively studied for three-level NPC inverter [3]–[6]. The neutral point balancing schemes are mainly based on the effective use of the redundant switching states of the inverter voltage vectors. But only few inverter voltage vectors have redundancy of the switching combinations and thus limit the neutral point balancing capability of the three-level NPC inverter, especially at higher modulation indices [3], [5], [6]. The other strategies presented for neutral-point balancing are based on changing the time durations of the redundant voltage vectors in the sampling interval but the pulsewidth modulation (PWM) implemented in this way is no longer a space vector PWM (SVPWM) [7], [8].

Manuscript received June 10, 2005; revised October 26, 2005. Recommended by Associate Editor J. H. R. Enslin.

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Digital Object Identifier 10.1109/TPEL.2006.882940

This paper presents a dc link capacitor voltage balancing scheme with common mode voltage elimination for a three-level inverter fed induction motor drive. An open-end winding induction motor is fed by two three-level inverters from either side, thus resulting in five-level voltage space phasor locations [9]. When only those inverter voltage vectors, which do not generate any common mode voltage at inverter poles, are used for inverter switching, the resultant voltage vectors are similar to a three-level inverter [10] and the common mode voltage in the machine phase voltage is also zero [10]. The inverter voltage vectors of the proposed three-level inverter drive have more redundant switching combinations for the inverter voltages, with opposite effect on the capacitor voltage balancing. Alternate use of these switching combinations can be used to maintain the capacitor voltages. The redundancy offered by the inverter voltage vectors makes the proposed three-level inverter fed drive ideal for dc link capacitor voltage balancing for the entire modulation range. Thus, a single power supply along with two capacitors is used in the proposed induction motor drive. Since the open-end winding structure is used, the dc link requirement is nearly half as compared with a single three-level inverter fed drive. A hysteresis controller based closed loop voltage-balancing scheme is presented in this paper, which can balance the capacitor voltages under motoring as well as regenerative operating conditions. The simulation studies are carried out and response of the controller is demonstrated for steady state as well as for dynamic conditions. The experimental studies are carried out on a 1.5-kW open-end windings induction motor drive and the experimental results are presented.

II. THREE-LEVEL INVERTER SCHEME WITH COMMON-MODE VOLTAGE ELIMINATION FOR AN INDUCTION MOTOR DRIVE

A three-level inverter configuration with common mode voltage elimination is already presented in [10]. Only those switching combinations, which generate zero common mode voltage in the inverter poles, are used to switch the three-level inverters from both sides, thus resulting in zero common mode voltage across the machine phases [10]. The switching state “+,” “0,” and “–” in Fig. 1 indicates the inverter pole voltage level of $V_{dc}/4$, 0, and $-V_{dc}/4$ V, respectively, with respect to the midpoint of the dc rail. These switching state combinations of individual three-level inverters for the proposed drive are shown in Fig. 1, where first switching state in each pair corresponds to switching state of inverter-A, while second

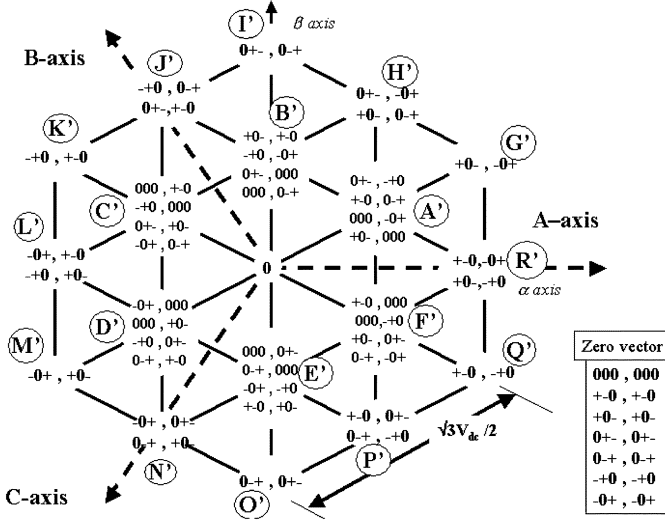


Fig. 1. Switching combinations for three-level inverter with common mode voltage elimination.

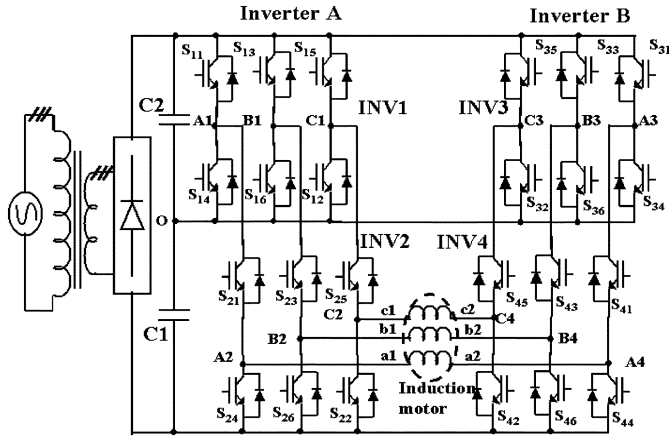


Fig. 2. Schematic of the proposed three-level inverter drive fed from single converter.

one corresponds to switching state of inverter-B (Fig. 1). Thus, appropriate selection of switching states, of individual three-level inverters, result into the total elimination of alternating common mode voltage from the inverter pole voltages as well as common mode voltages from the phase windings of the induction motor [10].

As the common mode voltages are absent in this scheme, individual three-level inverter structure can be supplied from single dc link as shown in Fig. 2. The three-level structure is realized by cascading two conventional two-level inverters, resulting in a simple power bus structure for the proposed power circuit [9], [10].

III. ANALYSIS OF DC LINK CAPACITOR VOLTAGE UNBALANCE FOR PROPOSED THREE-LEVEL INVERTER SCHEME

In the NPC three-level inverter, the current drawn through the mid-point of dc link will result in the unbalance of the capacitor voltage [3]. This section presents the analysis to determine

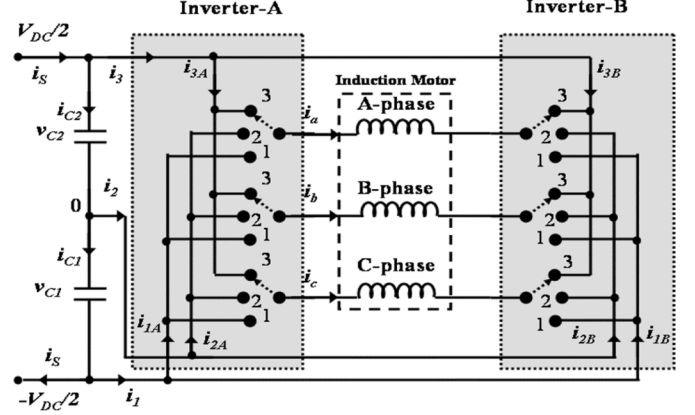


Fig. 3. Inverter-induction motor system model.

the unbalance in the dc link capacitor voltages for the proposed open-end winding induction motor drive.

A. System Model

The system model of the proposed inverter scheme is shown in Fig. 3. The voltage across the bottom and top dc link capacitors is referred as v_{C1} and v_{C2} . Under the balanced condition, $v_{C1} = v_{C2} = V_{DC}/2$. Each leg of individual three-level inverter can be modeled as a switch, with the three output levels 1, 2, 3, (this is used instead of $-$, 0 , $+$ for the ease of mathematical analysis in the following section) when the pole is connected to negative, mid-point and positive bus of the dc link, respectively, as shown in Fig. 3. The motor currents are denoted as i_a , i_b , and i_c while the total current drawn by the inverter from the bottom, middle, and top rails of the dc link are denoted as i_1 , i_2 , and i_3 , respectively. Similarly the inverter-A input currents are referred as i_{1A} , i_{2A} , and i_{3A} , and inverter-B input currents are i_{1B} , i_{2B} , and i_{3B} .

B. Determination of Capacitor Voltage Unbalance

The inverter pole voltage with respect to negative dc rail, for inverter-A and inverter-B (Fig. 2) can be expressed in terms of the capacitor voltages as shown in (1) and (2), respectively

$$\begin{aligned} v_{a1}(S_a) &= \delta(S_a - 1)v_{C1} + \delta(S_a - 2)(v_{C1} + v_{C2}) \\ v_{b1}(S_b) &= \delta(S_b - 1)v_{C1} + \delta(S_b - 2)(v_{C1} + v_{C2}) \\ v_{c1}(S_c) &= \delta(S_c - 1)v_{C1} + \delta(S_c - 2)(v_{C1} + v_{C2}) \\ v_{a2}(S'_a) &= \delta(S'_a - 1)v_{C1} + \delta(S'_a - 2)(v_{C1} + v_{C2}) \\ v_{b2}(S'_b) &= \delta(S'_b - 1)v_{C1} + \delta(S'_b - 2)(v_{C1} + v_{C2}) \\ v_{c2}(S'_c) &= \delta(S'_c - 1)v_{C1} + \delta(S'_c - 2)(v_{C1} + v_{C2}) \end{aligned} \quad (1)$$

where v_{a1} , v_{b1} , v_{c1} and v_{a2} , v_{b2} , v_{c2} are the pole voltages of inverter-A and inverter-B, respectively, with respect to lower dc link bus. In (1) and (2), $\delta(\cdot)$ is the continuous time Dirac function, where $\delta(0) = 1$, otherwise, its value is equal to zero. $S_a, S_b, S_c, S'_a, S'_b, S'_c$ are the switching functions defined for the poles of inverter-A and inverter-B, respectively, and can take any value from 1, 2, or 3 [11]. The currents drawn from the dc link nodes can be represented in terms of the motor currents as

shown in (3) for inverter-A (Fig. 2) and in (4) for inverter-B, respectively

$$\begin{bmatrix} i_{1A} \\ i_{2A} \\ i_{3A} \end{bmatrix} = \begin{bmatrix} \delta(S_a - 1) & \delta(S_b - 1) & \delta(S_c - 1) \\ \delta(S_a - 2) & \delta(S_b - 2) & \delta(S_c - 2) \\ \delta(S_a - 3) & \delta(S_b - 3) & \delta(S_c - 3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} i_{1B} \\ i_{2B} \\ i_{3B} \end{bmatrix} = - \begin{bmatrix} \delta(S'_a - 1) & \delta(S'_b - 1) & \delta(S'_c - 1) \\ \delta(S'_a - 2) & \delta(S'_b - 2) & \delta(S'_c - 2) \\ \delta(S'_a - 3) & \delta(S'_b - 3) & \delta(S'_c - 3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (4)$$

Now the total current drawn from the dc link can be written as

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} i_{1A} \\ i_{2A} \\ i_{3A} \end{bmatrix} + \begin{bmatrix} i_{1B} \\ i_{2B} \\ i_{3B} \end{bmatrix} \quad (5)$$

Therefore from (3) and (4)

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} \delta(S_a - 1) & \delta(S_b - 1) & \delta(S_c - 1) \\ \delta(S_a - 2) & \delta(S_b - 2) & \delta(S_c - 2) \\ \delta(S_a - 3) & \delta(S_b - 3) & \delta(S_c - 3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} \delta(S'_a - 1) & \delta(S'_b - 1) & \delta(S'_c - 1) \\ \delta(S'_a - 2) & \delta(S'_b - 2) & \delta(S'_c - 2) \\ \delta(S'_a - 3) & \delta(S'_b - 3) & \delta(S'_c - 3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (6)$$

For a three wire load, $i_a + i_b + i_c = 0$ and thus for dc link currents, we can write, $i_1 + i_2 + i_3 = 0$.

Substituting $i_c = -(i_a + i_b)$ and removing the dependent variable i_3 , (6) gets reduced to (7), shown at the bottom of the page.

The current flowing through the capacitors is given by

$$i_{C2} = i_S - i_3 = i_S - (-i_2 - i_1) = i_S + i_2 + i_1 \quad (8)$$

$$i_{C2} = i_S + i_1 \quad (9)$$

$$\therefore \begin{bmatrix} i_{C2} \\ i_{C1} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_S \\ i_2 \\ i_1 \end{bmatrix} \quad (10)$$

The currents flowing through capacitors is directly related to the voltage across it and the relationship is given by

$$\begin{aligned} \begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} &= \frac{1}{C} \int \left\{ \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{C2} \\ i_{C1} \end{bmatrix} dt \right\} \\ &= \frac{1}{C} \int \left\{ \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_S \\ i_2 \\ i_1 \end{bmatrix} dt \right\} \end{aligned} \quad (11)$$

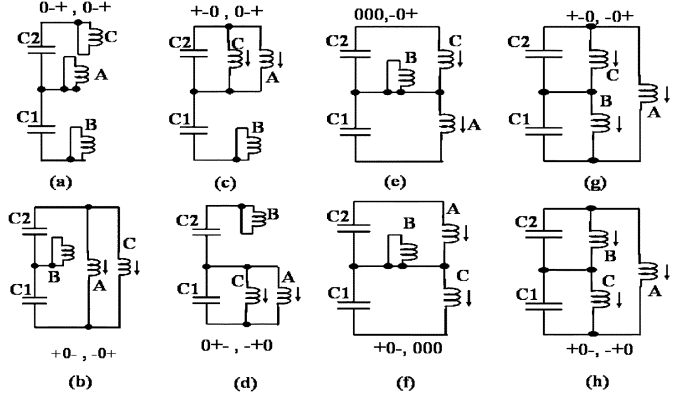


Fig. 4. Phase winding connections to the dc link capacitors for various vector groups: (a) ZV, (b) LV, (c) USV, (d) LSV, (e) NSV, (f) NSV, (g) MV, and (h) MV.

Let Δv_C be the change in the capacitor voltage because of load current flowing through the capacitors

$$\Delta v_C = v_{C2} - v_{C1} \quad (12)$$

Substituting from (11) into (12) results in

$$\Delta v_C = \frac{1}{C} \int i_2 dt \quad (13)$$

Thus, for the proposed scheme, the load current drawn from the middle node of the dc link is responsible for the variation in the capacitor voltages. From (7), it can be seen that the current i_2 is determined by the value of the switching functions $S_a, S_b, S_c, S'_a, S'_b, S'_c$ at that instant. So the ideal voltage-balancing scheme will be the one, which will reduce the current drawn from middle dc link node. Whenever the switching functions $S_a, S_b, S_c, S'_a, S'_b, S'_c$ assume value equal to two, there exists an unbalancing tendency for capacitor voltages. Different switching combinations, for the same inverter voltage vector locations of Fig. 1, have different effect on the capacitor voltages. The effect of the various switching combinations on the capacitor voltages is discussed in the next section.

IV. SWITCHING COMBINATIONS AND THEIR EFFECT ON DC LINK CAPACITOR VOLTAGES

As explained in the previous section, the inverter space vector locations have multiple switching combinations of inverter-A and inverter-B voltage space vectors (Fig. 1). Similar to three-level NPC inverter, the inverter voltage vector locations are divided into four main groups [2] as shown in Fig. 4. The central voltage location being referred as zero voltage vector (ZV), the voltage vector locations at the periphery of inner hexagon are

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} [\delta(S_a - 1) - \delta(S_c - 1)] - [\delta(S'_a - 1) - \delta(S'_c - 1)] & [\delta(S_b - 1) - \delta(S_c - 1)] - [\delta(S'_b - 1) - \delta(S'_c - 1)] \\ [\delta(S_a - 2) - \delta(S_c - 2)] - [\delta(S'_a - 2) - \delta(S'_c - 2)] & [\delta(S_b - 2) - \delta(S_c - 2)] - [\delta(S'_b - 2) - \delta(S'_c - 2)] \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \quad (7)$$

TABLE I
EFFECT OF DIFFERENT VECTOR GROUPS ON CAPACITOR VOLTAGES

Group	Capacitor C1	Capacitor C2
ZV	No effect	No effect
NSV	Less charging or discharging effect	Less charging or discharging effect
USV	Discharging	Charging
LSV	Charging	Discharging
MV	Less charging or discharging effect	Less charging or discharging effect
LV	No effect	No effect

referred as small voltage vectors (SV), the intermediate voltage vectors on outer periphery are referred as middle voltage vectors (MV), while the largest voltage vectors on outer periphery are referred as large voltage vectors (LV).

The small voltage vectors are again classified in to the three sub-groups as shown in Fig. 4. The small voltage vectors combinations, in which each capacitor of the dc link has one winding connected across it, are referred as normal small voltage vector (NSV) [Fig. 4(e)–(f)]. The small voltage vectors combinations, in which two windings are connected across the top capacitor C2, are referred as upper small voltage vectors (USV) Fig. 4(c). The small voltage vectors combinations, in which any two out of three phase windings are connected across bottom dc link capacitor-C1, are referred as lower small voltage vectors (LSV) Fig. 4(d). The phase winding connections to the dc link for various groups is as shown in Fig. 4. Each voltage vector combination has a charging/discharging effect on the dc link capacitors C1 and C2 and is summarized in Table I.

The inverter voltage vectors belonging to USV and LSV [Fig. 4(c)–(d)] groups have large unbalancing effect on the dc link capacitor voltages as the current drawn from the middle node of the dc link is significant. When the NSV vectors are used for inverter switching, only the difference between the current drawn by the phase connected to top capacitor and current drawn by the phase connected to bottom capacitor flows from middle node of the dc link [Fig. 4(g)–(h)]. Thus, NSV vectors will have less charging/discharging effect on the capacitor voltages as compared to USV and LSV vectors. Each of the MVs locations (Fig. 1) have two different switching combinations of three-level inverter voltage vectors (Fig. 1). There exists a similarity between the MVs and NSVs, except the third winding is connected directly across dc Link and does not have any effect on the capacitor voltages. The large voltage vector group is characterized by connection of any two phase windings across the dc link while the third winding is short circuited at dc link mid-point (Fig. 4). As the phase windings are directly connected across the full dc link, inverter voltage vectors belonging to this group has no effect on the capacitor voltages.

V. PROPOSED SCHEME FOR DC LINK CAPACITOR VOLTAGE BALANCING

The inverter voltage vectors belonging to ZV, NSV, MV, and LV groups can be effectively used to maintain the voltage balance across the dc link capacitors. The input to the voltage-balancing scheme can be either the difference in the capacitor voltages, or the load current drawn from middle node, as the voltage unbalance can be determined from (13). Thus, a single front-end

TABLE II
CLOSED LOOP VOLTAGE CONTROLLER OUTPUT “STATE” FOR DIFFERENT INPUT CONDITIONS

Δv_C	Hyst. controller output ‘O/P’	SEQ (1 - POS_SEQ, 0 - NEG_SEQ)	State
Normal	0	1	1
		0	2
Positive	1	1	3
		0	4
Negative	-1	1	5
		0	6

rectifier can be used, with two capacitors for splitting the dc link. The power schematic of the overall scheme is shown in Fig. 2.

Each inverter voltage vector locations from groups NSV and MV have two switching combinations. The basic difference in each of these two switching combinations is that the phase winding which is connected across top capacitor in one switching combination gets connected across bottom capacitor for other switching combination. Fig. 4(g) and (h) shows the phase winding connections for switching combinations for the inverter voltage vector R' (MV group) which has two switching combinations $(+ - 0, -0+)$ and $(+0-, - + 0)$. For switching combination $(+ - 0, -0+)$, the B-phase winding is connected across bottom capacitor and C-phase winding is connected across top capacitor Fig. 4(g). Whereas, when switching combination $(+0-, - + 0)$ is used for inverter switching, the windings get connected to the opposite capacitors, i.e., B-phase winding is connected to top capacitor and C-phase winding is connected to bottom capacitor Fig. 4(h). This is true for all vector combinations belonging to NSV and MV groups. Fig. 4(e) and (f) shows the winding connections to the dc link for the two switching combinations of inverter vector A' (Fig. 1), belonging to NSV group. It can be seen from Fig. 4(e) and (f) that phase windings are connected to opposite capacitors for switching combinations $(000, -0+)$ and $(+0-, 000)$ which belong to inverter vector location A' . It is to be noted that in both cases, the third winding is either connected across the full dc link or short-circuited at middle dc link point.

For the same inverter voltage vector location, if the redundant switching combinations are switched alternately, the capacitor voltage unbalance caused by first switching combination is nullified by the second switching combination. The PWM controller alternately switches the switching combinations for inverter vectors from NSV and MV groups while the inverter vectors from ZV and LV are switched in the normal way. In this manner, the average voltage unbalance caused in one switching interval is nullified in the next switching interval. In a similar way, the switching combinations of all the voltage vectors of Fig. 1 are grouped in two groups, POS_SEQ and NEG_SEQ (as shown in Table III for Δv_C within control band) which are switched alternately.

A. Hysteresis Controller Based Closed Loop DC Link Balancing Scheme

With the voltage-balancing scheme implemented in the above manner, a gradual deviation in the dc link voltages is observed. The possible reasons for this are, the use of the asynchronous PWM, the unequal time durations of the MV and NSV inverter

TABLE III
SELECTION OF SWITCHING COMBINATIONS FOR DIFFERENT INPUT CONDITIONS

Condition	Δv_C within control band		$\Delta v_C > P_H$		$\Delta v_C < N_H$	
State	1	2	3	4	5	6
Vector Location	POS_SEQ	NEG_SEQ	POS_SEQ	NEG_SEQ	POS_SEQ	NEG_SEQ
0	000, 000 (ZV)					
A'	+0-, 000 (NSV)	000, -0+(NSV)	+0-, 0-+(USV)		0+-, -+0(LSV)	
B'	0+-, 000(NSV)	000, 0-+(NSV)	-+0, -0+(USV)		+0-, +0(LSV)	
C'	-+0, 000(NSV)	000, +0(NSV)	0+-, +0-(USV)		-0+, 0-+(LSV)	
D'	-0+, 000(NSV)	000, +0-(NSV)	0-+, +0-(USV)		-+0, 0+-(LSV)	
E'	0-+, 000(NSV)	000, 0+-(NSV)	-0+, -+0(USV)		+0-, +0-(LSV)	
F'	+0-, 000(NSV)	000, -+0(NSV)	+0-, 0+-(USV)		0-+, -0+(LSV)	
G'	+0-, -0+ (LV)					
H'	0+-, -0+(MV)	+0-, 0-+(MV)	0+-, -0+(MV)	+0-, 0-+(MV)	0+-, -0+(MV)	+0-, 0-+(MV)
I'	0-+, 0-+ (LV)					
J'	0+-, +0(MV)	-+0, 0-+(MV)	0+-, +0(MV)	-+0, 0-+(MV)	0+-, +0(MV)	-+0, 0-+(MV)
K'	-+0, +0 (LV)					
L'	-+0, +0-MV)	-0+, +0(MV)	-+0, +0-(MV)	-0+, +0-(MV)	-+0, +0-(MV)	-0+, +0(MV)
M'	-0+, +0- (LV)					
N'	-0+, 0+-(MV)	0-+, +0-(MV)	-0+, 0+-(MV)	0-+, +0-(MV)	-0+, 0+-(MV)	0-+, +0-(MV)
O'	0-+, 0+ (LV)					
P'	0-+, -+0(MV)	+0-, 0+-(MV)	0-+, -+0(MV)	+0-, 0+-(MV)	0-+, -+0(MV)	+0-, 0+-(MV)
Q'	+0-, -+0 (LV)					
R'	+0-, -0+(MV)	+0-, -+0(MV)	+0-, -0+(MV)	+0-, -+0(MV)	+0-, -0+(MV)	+0-, -+0(MV)

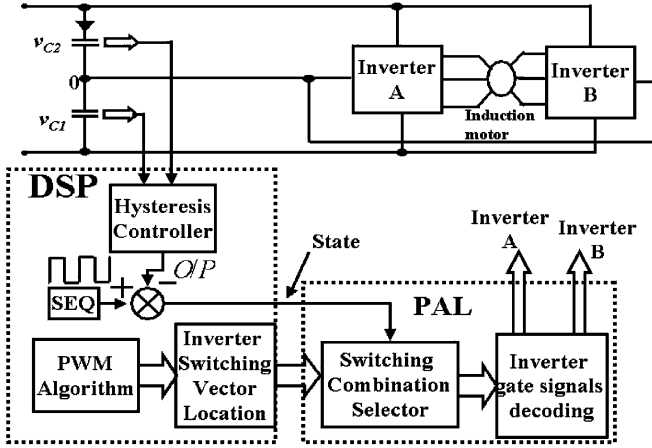


Fig. 5. Hysteresis controller based closed loop dc link capacitor voltage balancing scheme.

vectors in consecutive switching intervals, unbalanced load currents etc. As discussed in the previous section, the switching combinations belonging to USV and LSV group can charge the lower and the upper capacitor, respectively. Thus, if the difference in the two capacitors of the dc link is monitored, the switching combinations from USV or LSV groups can be selected for inverter switching, which will bring back the deviation in the capacitor voltages to zero. This is done using a hysteresis controller. The input to the controller is the difference between the dc link capacitor voltages, Δv_C . The normal control band is set depending upon the maximum deviation that can be allowed in the dc link voltages. The controller outputs, 0 if the Δv_C is within the normal band, 1 if Δv_C is greater than the control band and -1 if the Δv_C is less than the control band.

The schematic of the closed loop voltage balancing scheme is shown in Fig. 5. The output of the controller along with "SEQ" signal is used to select the appropriate value of the signal "state," which is given to a digital logic.

The values of signal "state" for various input conditions are shown in Table II. Depending upon the signal "state," the inverter switching combinations to be switched for the various voltage vector of the inverter (generated by PWM modulator [12]) are shown in Table III.

VI. DC LINK CAPACITOR VOLTAGE BALANCING DURING INVERTER OPERATION IN OVER-MODULATION AND 12-STEP MODE

It is to be noted that only the inverter vectors belonging to USV or LSV groups have strong capability to charge/discharge the dc link capacitors. During motor operation in over-modulation range, the inverter vectors belonging to MV and LV (Fig. 1) groups are switched for maximum duration, in a switching interval, as compared to the inverter voltage vectors belonging to SV group. The extreme case is the 12-step operation, wherein the inverter vectors from the SV group are not switched at all. Under steady state and dynamic operation, in over-modulation, the controller can maintain the capacitor voltage balance by switching MV and LV vectors (Fig. 1). The SV vectors are switched for less time duration, the time required to bring back the capacitor voltages to the balanced state, is more during over-modulation operation. In extreme case, the inverter vectors from SV group are not switched in 12-step mode. If there is mismatch in the capacitor voltages due to the asynchronous PWM or asymmetric loads, the capacitor voltages are balanced by reducing the modulation index momentarily. This allows the switching of the inverter vectors belonging to SV group and the dc link capacitor voltages are brought back to the balanced state as shown in the simulation results of Fig. 6.

VII. DC LINK CAPACITOR VOLTAGE BALANCING UNDER REGENERATIVE OPERATING CONDITIONS

The dc link voltage-balancing scheme described in previous section is based on the assumption that the load is always drawing current from the dc link. But under the regenerative

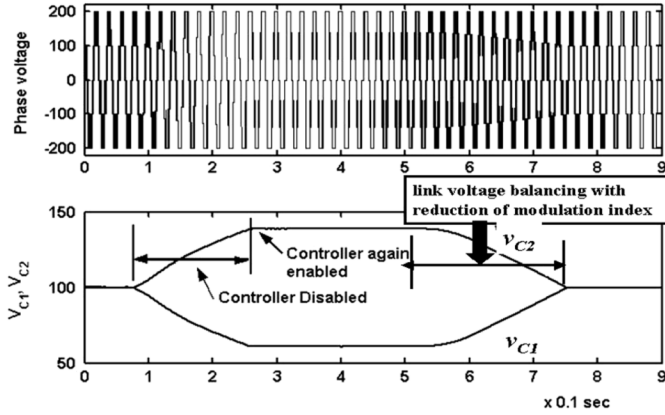


Fig. 6. DC link balancing with momentary reduction in modulation index [Scale: Top Trace: X axis—1 div = 0.1 s, Y axis: 1 div = 100 V, Bottom Trace 1: X axis: 1 div = 0.1 s, Y axis: 1 div = 50 V].

TABLE IV
EFFECT OF SWITCHING COMBINATIONS FROM USV
AND LSV GROUPS ON THE CAPACITOR VOLTAGES

Type of Load	USV		LSV	
	C1	C2	C1	C2
Motoring	Charge	Discharge	Discharge	Charge
Regenerating	Discharge	Charge	Charge	Discharge

mode of motor, this is not true. The current directions are opposite than what has been assumed for motoring mode. Thus while, USV vectors were having charging effect on C1 and discharging effect on C2 in motoring mode, they have discharging effect on C1 and charging effect on C2 in regenerative mode. This is summarized for USV and LSV vectors in Table IV.

Thus, the controllers need to sense the power direction, to suitably switch the switching combinations belonging to the vector group, which will reduce the error in the dc link capacitor voltages. Determining the operating mode (i.e., motoring/generating) requires current sensing. The determination of current direction for currents drawn from dc link involves hardware sensors or can be judged from direction of power flow (this again calls for sensing of dc link capacitor currents). The scheme proposed, in this section, does not call for current sensing. Initially, it is assumed that the motor is drawing currents from the source and the controller performs the voltage balancing actions as described in previous section. If the motor is operating in regenerative mode, the actions taken by the controller will worsen the voltage balance. An additional hysteresis comparator is used to sense this change. The control band of this comparator is placed above the control band of the main inner comparators. Thus, with motor operating in regenerative mode, the outer comparators of hysteresis controller gets activated if the dc link voltage unbalance exceeds the outer comparator settings and the switching combinations belonging to the USV or LSV vector group, which reduces the voltage unbalance, are selected for inverter switching.

As shown in simulation results of Fig. 7, the motor is initially operating in motoring mode and the load torque is made negative thus driving the motor in regenerative mode. The voltage-balancing controller is disabled which will cause rapid growth in dc link unbalance. When the voltage-balancing scheme is

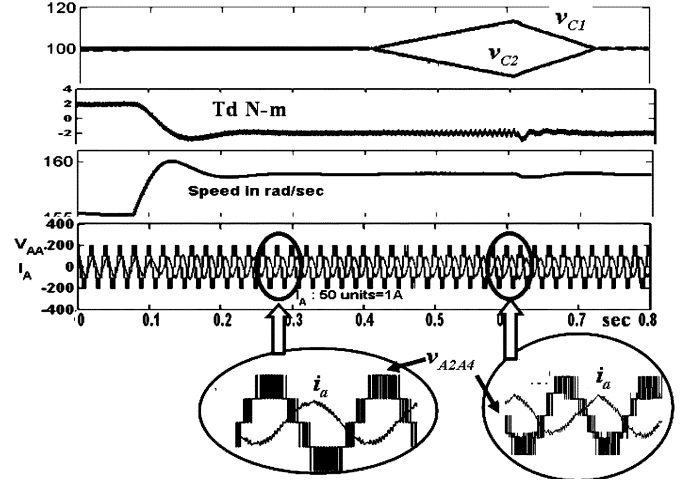


Fig. 7. Capacitor voltages when the closed loop dc link voltage balancing scheme is turned off in regenerating mode [Scale: X axis—1 div = 0.1 s, Y axis: Trace1—1 div = 20 V, Trace2—1 div = 2 N-m, Trace3—1 div = 10 rad/sec, Trace4—1 div = 200 V, 4 A].

enabled again, the capacitor voltages are brought back to the normal value, similar to the case with motor operating in motoring mode.

VIII. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed scheme is tested on a 1.5-kW three-phase open-end winding induction motor drive with V/f control for different modulation indices covering the entire speed range. The dc link voltage of around 130 V is used, thus the individual dc link capacitor voltages are kept around 65 V. The carrier frequency used for PWM generation is limited to 1.2 kHz. The hysteresis controller based closed loop dc link capacitor voltage balancing scheme is implemented using TMS320F24 processor and PALCE22V10 devices. The controller schematic is as shown in Fig. 5. The generalized n -level SVPWM scheme is used for the PWM signal generation, based on the sampled amplitudes of reference phase voltages [12]. The pole voltage, phase voltage and phase current waveforms for inverter operation in inner layer (two-level) and outer layer (three-level) operation are presented in Figs. 8 and 9, respectively, to prove the absence of common mode voltage in the pole as well as phase voltage. The pole voltages are symmetric and are out of phase with each other. The normalized FFTs of pole voltage and the phase voltage waveforms show the absence of triplen voltage components. The even harmonics components, present in pole voltages, cancel each other in phase voltage and the fundamental component gets added up. The dc link voltage balancing controller is implemented as described in Section V-B and its performance is tested in steady state as well as in dynamic conditions. The voltage band for the comparators is set to 4 V. The traces of dc link capacitor voltages with induction motor running at constant speed are shown in Fig. 10(a). The dc link capacitor voltages are well within the voltage band of the hysteresis controller. The slow drift in the capacitor voltages (as explained in Section V-B) can be observed in the capacitor voltages which is brought back to normal state by the controller. Whenever, the difference between capacitor voltages exceeds the voltages band, the controller selects appropriate

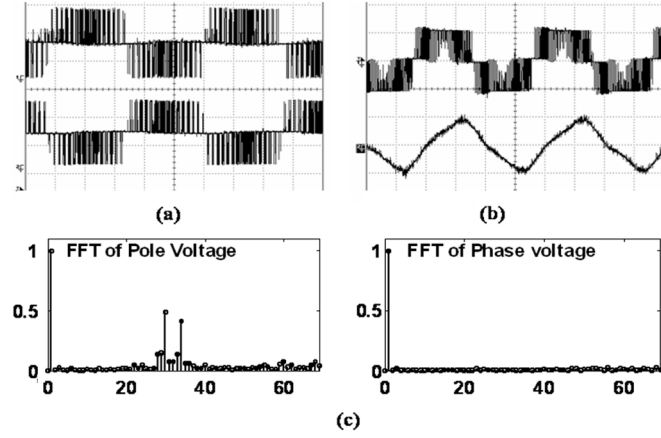


Fig. 8. Operation of three-level inverter in Layer-1 (Modulation index 0.28): [scale: (a) X axis—1 div = 10 ms, Y axis: 1 div = 50 V, (b) Top Trace \Rightarrow X axis: 1 div = 10 ms, Y axis: 1 div = 50 V, Bottom Trace \Rightarrow X axis: 1 div = 10 ms, Y axis: 1 div = 2 A], (c) Y -axis: relative harmonic amplitude with respect to fundamental, X -axis: harmonic order with respect to the fundamental.

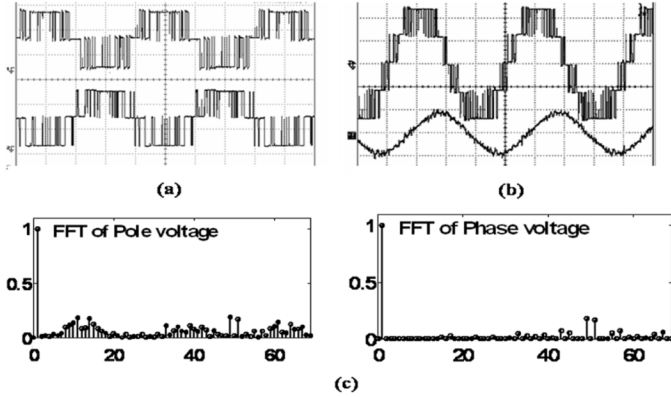


Fig. 9. Operation of three-level inverter in Layer-2 (Modulation index 0.48): [scale: (a) X axis—1 div = 10 ms, Y axis: 1 div = 100 V, (b) Top Trace \Rightarrow X axis: 1 div = 10 ms, Y axis: 1 div = 100 V, Bottom Trace \Rightarrow X axis: 1 div = 10 ms, Y axis: 1 div = 2 A], and (c) Y -axis: relative harmonic amplitude with respect to fundamental, X -axis: harmonic order with respect to the fundamental.

switching combinations from USV or LSV groups to bring back the capacitor voltages to their balanced condition as shown in Fig. 10. This proves the operation of the dc link capacitor voltage balancing controller. With the reference voltage space vector in the inner layer (two-level operation), the capacitor voltage balancing scheme is disabled for small interval. The capacitor voltages are shown in Fig. 10(b) at this instant. The capacitor voltages are balanced immediately, after the dc link voltage balancing controller is enabled again. Fig. 10(c) shows the performance of the capacitor voltage-balancing scheme for the inverter operation in outer layers. The capacitor voltages are balanced immediately after the dc link voltage balancing controller is enabled again. Fig. 11 shows the phase current and dc link capacitor voltages during the acceleration of machine from inner layer operation to outer layer operation and again to the operation in over-modulation. The dc link voltages are maintained within the control band. The speed reversal command is given to the controller and the machine phase current and the dc link voltages are shown in Fig. 12. The dc link voltages are maintained within the control band.

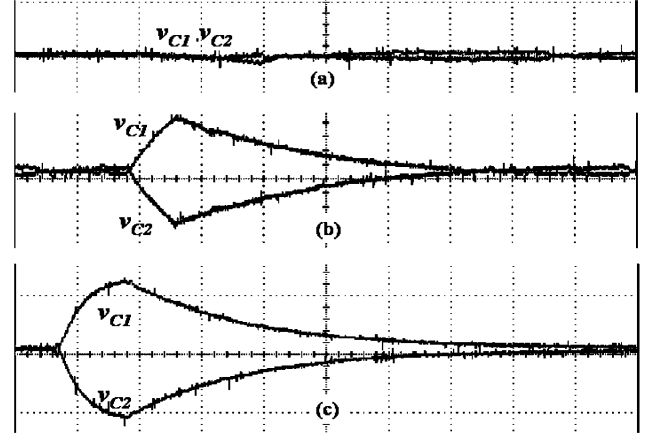


Fig. 10. (a) DC link capacitor voltages v_{C1} and v_{C2} during steady state operation [Scale: X -axis: 1 div = 20 V, Y -axis: 1 div = 2 s], (b) Balancing of the dc link capacitor voltages after the controller is disabled for small interval, inner layer operation. [Scale: X -axis: 1 div = 20 V, Y -axis: 1 div = 2 s], (c) balancing of the dc link capacitor voltages after the controller is disabled for small interval, outer layer operation [Scale: X -axis: 1 div = 20 V, Y -axis: 1 div = 1 s].

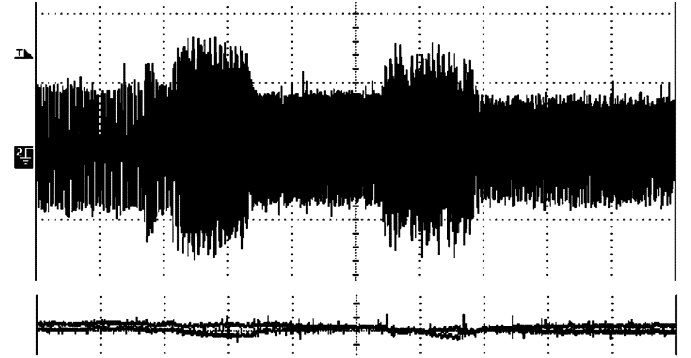


Fig. 11. DC link voltages and machine phase current under machine, operating in inner layer, is accelerated to outer-layer and then to over-modulation. Top Traces: V_{C1} and V_{C2} , bottom trace: Phase current. [Scale: X -axis: 1 div = 20 V (bottom trace), Y -axis: 1 div = 2 A (top trace) 2 A, Y -axis: 1 div = 2 s].

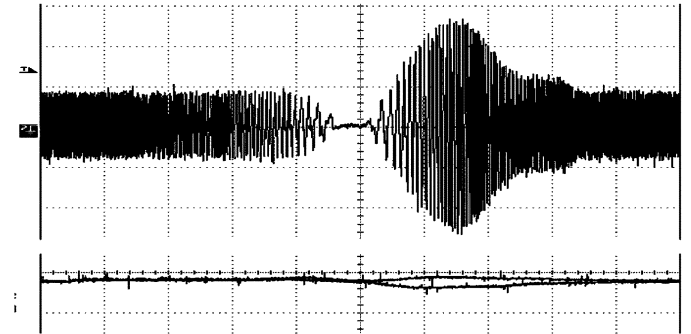


Fig. 12. DC link voltages and machine phase current under while machine operating in inner layer is subjected to speed reversal. Top Trace: Phase current, bottom trace: v_{C1} and v_{C2} [Scale: Y -axis: 1 div = 20 V (bottom trace), Y -axis: 1 div = 2 A (top trace), X -axis: 1 div = 2 s].

IX. CONCLUSION

A three-level inverter fed induction motor drive scheme with zero common mode voltage in pole voltage as well as in the

phase voltage with dc link capacitor voltage balancing is proposed in this paper. An open end winding induction motor drive, fed by three-level inverters from both sides, is used for the proposed scheme. The three-level structure is realized by cascading the conventional two two-level inverters, resulting into simple power bus structure for the proposed scheme. Thus, the proposed inverter structure does not require any clamping diodes which are required in NPC inverter topology. The proposed scheme has more multiplicity in the inverter voltage vector locations as compared to conventional single inverter fed drive which are effectively used to balance the dc link capacitor voltages without disturbing the SVPWM modulation. Thus, a single front-end rectifier of rating nearly half to that of a conventional two-level inverter can be used, with two capacitors for splitting the dc link voltage. The proposed capacitor voltage balancing scheme is based on altering the switching combinations of the inverter voltage vectors, having exactly opposite effect on the capacitor voltages, for consecutive sampling durations. A simple closed loop hysteresis controller is used to balance the dc link capacitor voltages throughout the modulation range of the drive.

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