Design for Non-Linearity Improvement of Current Steering Digital to Analog Convertor for Biomedical Applications

A Thesis Submitted to

Nirma University

In Partial Fulfilment of the Requirements for

The Degree of

Doctor of Philosophy

in

Technology & Engineering

By

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December, 2022

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CERTIFICATE

This is to certify that the thesis entitled **Design for Non-Linearity Improvement of Current Steering Digital to Analog Convertor for biomedical applications** has been prepared by **Mr. Jayeshkumar J Patel (13EXTPHDE107)** under my supervision and guidance. The thesis is his own original work completed after careful research and investigation. The work of the thesis is of the standard expected of a candidate for Ph.D. Programme in **Electronics and Communication Engineering** and I recommend that it be sent for evaluation.

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This is to certify that the thesis entitled Design for Non-Linearity Improvement of Current Steering Digital to Analog Converter for Biomedical Applications has been prepared by me, under the supervision and guidance of Dr. Amisha Naik. The thesis is my own original work completed after careful research and investigation. The work of the thesis is of the standard expected of a candidate for Ph.D. Programme. The final hard bound copy of the thesis is submitted after incorporating all the suggestions / corrections suggested by the referees.

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ACKNOWLEDGEMENTS

During my journey of research work starting from preparation for getting to be registered for Ph. D till proofing of each and every line of report, many persons are there for me with right spirit to help me, to support me, to guide me, to motivate me, to direct me as per their individual's best capacity. Because of group of such people, I could manage the even if many up and downs. I would like to take the opportunity to convey my gratitude.

First of all, I would like to express my deepest gratitude to GOD for his blessing with me throughout my life and specifically during the tenure of my research work phase.

I am thankful the Management of University, Institute of Technology and Department of Electronics and Communication Engineering for providing me the opportunity and permission for Ph. D work and more specifically for no. of extensions.

I take this opportunity to express a sense of gratitude to my Ph. D guide Dr. Amisha Naik, Associate Professor, Institute of Technology, Nirma University, Ahmedabad for her continuous guidance, motivation, valuable suggestions, and all kind of support in form of technical as well as moral during the each and every day & phase of Ph. D study. I am very much grateful to my research progress committee members Dr. Rajesh Thakkar, former Principal, Government Eng. College, Rajkot and Dr. N. M. Devashrayee, Eminent Professor- Institute of Technology, Nirma University for providing valuable and rewarding feedback/inputs/comments throughout my research work.

My sincere gratitude to Dr. R N. Patel, Director, Institute of Technology, Nirma University for his support and co-operation. I would like to thank Dr. Usha Mehta HOD, Department of Electronics and Communication Engineering for the encouragement and support. Big thanks to Dr D. K. Kothari, former HOD-EC for administrative support at various phase of my work. My special mention to Dr. Dhaval Pujara former HOD-EC here for all kind of support and specifically for encouraging me to give qualitative time for research work.

Thanks from bottom of my heart are for my friends cum colleagues Dr. Vijay Savani, Dr. Piyush Bhatasana, Dr. Akash Mecwan, Dr. Dhaval Shah, Dr. Bhupendra Fataniya, Prof. Hardik Joshi, Dr. Rutul Patel, Dr Manish Patel, Dr Bhaveshbhai, Mr Upendrabhai, Mr Gunjan and other colleagues of the department and institute. Thanks to students like Arya and Yash to say always- " Yes sir, You can do it".

I am very much thankful to my father, my wife Sheela, my daughter Dr. Aakanksha and son Nirmay for their motivation, love, support and patiently wait for years to see the completion of my Ph. D work.

There are many more who contributed in terms of moral support, motivation, thought sharing, help during simulation, guidance for research paper publication, providing impactful inputs for report writing etc. It might be little from their side but having significant impact during this journey. I personally convey lots of thanks to all well-wishers without mentioning their name here.

I thank one and all, who are with me directly or indirectly to keep me motivated and for moral support.

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LIST OF ABBREVIATIONS

AC	Alternating current
A/D	Analog-to-digital
ADC	Analog-to-digital converter
bit	Binary digit
CMOS	Complementary metal-oxide semiconductor
CS	Current Steering
D/A	Digital-to-analog
DAC	Digital-to-analog converter
dB	Decibel
DC	Direct current
DNL	Differential Non-Linearity
ENOB	Effective number of bits
FFT	Fast Fourier transform
FS	Full scale
HD	Harmonic distortion
HDL	High-level description language
HDTV	High-definition television
INL	Integrated Non-Linearity
I/O	Input / output
ISDN	Integrated services digital network
LSB	Least significant bit
LSI	Large-scale integration
MOS	Metal-oxide semiconductor
MOSFET	Metal-oxide semiconductor field effect transistor
MSB	Most significant bit
NMOS	N-channel metal-oxide semi-conductor
OSADC	Oversampled A/D converter
OSDAC	Oversampled D/A converter
PCB	Printed circuit board
PLL	Phase-locked loop

PMOS	P-channel metal-oxide semi-conductor
RAM	Random access memory
ROM	Read-only memory
SC	Switched capacitor
S/H	Sample-and-hold
SFDR	Spurious-free dynamic range
SNR	Signal-to-noise ratio
ULSI	Ultra-high large-scale integration
VLSI	Very high large-scale integration

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ABSTRACT

A Digital to Analog Converter find its applications in almost all the fields where the data is to be measured and to be monitored at various places /systems including human body. For biomedical portable devices which are used to measure and control parameters like ECG/EEG and in case of artificial retina implantations, there is a great demand of high-speed high-resolution Digital-to-Analog converters (DAC) designs which offers good linearity characteristics. In addition, it is expected that such design/devices dissipate minimum power.

In this work mainly the focuses are given for designing current steering DAC with good linearity characteristics using different Switching devices with variety of current sources for Improving Integral and differential Non linearity characteristics. For getting the advantages of binary weighted DAC and unary weighted current DAC, the concept of segmented DAC has been adopted with various kinds of combinations. To optimize the performance in terms of linearity and power the Current Steering DACs are designed using different types of switches like NMOS, Transmission Gates and differential switches and combining the use of binary and unary weighted DACs. For all the proposed designs, the simulations are carried out in CMOS 180nm process results using standard design tools were obtained and compared with state of art results.

Based on the results of the designed DACs, it can be said that segmented approach in current steering DAC with appropriate combination of no. of binary sources and no. of Unary current sources at USB side and/or LSB side play an important role in non-linearity. Differential switch offers due advantages comparted to NMOS switches and Transmission Gate switch as a switching element.

The most appropriate Design of current steering DAC for biomedical application is segmented Current DAC designed DAC with differential switches. DNL and INL are 0.12 and 0.152 LSB with power consumption of 3.8uW, DNL is reduced by the factor of **7.58**, INL is reduced by the factor of **8.09** and Power dissipation is increased by the factor of **2.375**. Cadence virtuoso tool has been used for simulation in 180nm CMOS technology with 1.8V supply voltage.

CHAPTER-1

INTRODUCTION

For a long back, data converters circuits are in huge demand as they are a must kind of block in almost all DSP processors chips and are successfully found useful in the various filed of engineering as well as non-engineering. They have tremendous usage or applications in areas including biomedical instrumentation, Communication systems, robotics, Data distribution systems, Aero Space, and Marine Engineering. Analog to Digital Converter (ADC) and Digital Analog Converter (DAC) are key blocks for interfacing-link between two domains: Analog and Digital. ADC is used as an input block for the processor/controller which converts Analog signal (which is continuous in the time domain) to digital (which is discrete in the Amplitude and time domain). While DAC is used as an output block and converts the signal from the Digital domain to the Analog domain. DAC may be an integral part of some of the ADC circuits as well. Specifically, DAC is used for Audio amplifiers, Video encoders, Display electronics, Calibration, Motor control, data distribution systems, Digital potentiometers, software radios, Biomedical applications, etc.

DACs are classified based on implementation mode: Resistor string DAC, R-2R Ladder DAC, Current steering DAC, and Charge Redistribution DAC. Current steering DAC is widely used because of its speed and the need for a buffer for resistive load.

There are many performance measures for a DAC. They can be divided into static measures, dynamic measures, and frequency-domain measures. The static performance measures describe the working of a DAC when single input words are applied. They are the offset and gain error, the integral nonlinearity (INL) error, and

the differential nonlinearity (DNL) error. The dynamic performance describes the working of the DAC when the input word makes transitions between different values. The major dynamic measures are settling time which decides the speed of the DAC, and glitches at the output. Other parameters are Resolution, Full-scale voltage, Power dissipation, Dynamic range, etc.

Integral nonlinearity (INL) error and differential nonlinearity (DNL) error plays an important role in any DAC. If the maximum DNL error is less than 1 LSB it is said that the DAC is guaranteed to be monotonic. Monotonicity can also be guaranteed if the maximum INL error is less than 0.5 LSB. If a DAC is monotonic, then the output always increases as the input increases. Nonlinearity error is more dominant for higher resolution DAC. It must be as less as possible so even in a noisy environment DAC generates error-free output. DAC used in the field of biomedical must have desirable INL and DNL. INL and DNL represent the accuracy of DAC. Accuracy is mainly influenced by the glitches and switching transients during the operation of DAC.

In this research work, the approach of segmented DAC (a combination of binary-weighted DAC and Unary weighted DAC) has been used to minimize the glitches. A novel approach of the differential switch is used to get the desired accuracy.

1.1 MOTIVATION

DACs (Digital to Analog Converters) play a vital role in various fields like biomedical instrumentation, Communication systems, Robotic, etc. Typically, the DACs are incorporated in most digital systems when real-world signals. Real-world signals like pressure signals, sound waves, temperature readings, or images are converted into digital form by means of analog-to-digital converters (ADCs). After processing, such signals are converted back to analog signals using DAC. DAC is an uncompromised requirement of the circuits that drive devices ranging from audio–video applications, DC, AC, or servo motor control to radio frequency transceivers or a variety of industrial temperature controllers.

DAC exist for a long back and lots of research and development have been carried out with a good rate of work. It is known as the circuit of all seasons. The advancement and progress of Technology may lead to a result in terms of possible better resolution. DAC having applications in the field of Communication and

Biomedical are more prone to Noise. For higher resolution DAC, other parameters like INL, and DNL will be deuterated. Hence output may not be monotonous. Under the influence of Noise, there will be no desired output for the given inputs. Hence nonlinearity errors i.e INL and DNL are very challenging for higher-resolution DAC.

Modern VLSI technology enables miniaturized and fully implantable neurostimulator circuits while simultaneously allowing the designer to integrate extremely large numbers of channels, and also allows increased functionality. Increased functionality empowers the designer to achieve higher stimulation efficacy without compromising the device size.

The current steering DAC enables high power performance as the current sources transistors involved in stimulation are required to be switched on. In the case of a splitter, the entire circuit draws the current regardless of the selected node. However, in the case of the splitter, the area increases linearly with an increase in the number of bits, which is not the case in the weighted arrays, where the area increases exponentially with the number of bits. The larger the number of bits in the weighted arrays higher the area required.

The motivation behind this research work is to design a Digital to Analog Converter having an application in the Biomedical filed where INL and DNL are crucial. It must offer less INL and DNL for higher resolution without compromising the area and power consumption.

1.2 RESEARCH OBJECTIVES

Very-large-scale integration (VLSI) implementations of neural and fuzzy systems usually have an array-type structure: the same cell is repeated in a large two-dimensional array for massively parallel processing, and some additional circuitry is available at the periphery for additional processing and/or out-of-chip communications. For optimum area efficiency, it is desired to simplify the cell as much as possible at the expense of complicating the periphery. However, many times one would like to improve the precision in the cells even if this requires some extra cell area. One simple way to provide such precision would be using some very compact and low-power mini digital-to-analog converters (mini-DACs).

A main source of nonlinearity originates because of glitches in the current cell. More no. of transitions results in more no. of changes in the states of switches say on to off or vice versa. In the case of a 4-bit binary-weighted DAC, when the input changes from 0011 to 0100, a big glitch is observed because of 3 transitions. Similarly, when the input changes from 0111 to 1000, even a big glitch will be there because of 4 transitions. In the case of unary weighted DAC, there is only a 1-bit transition so there is no glitch but it needs more no. of current sources; for 4-bit unary current steering DAC, 15 current sources having the same value are required. A thermometer code is used to control the switches. Additional hardware is required to convert binary code into thermometer codes. Characteristics of the switch also play an important role there are various options for the same: NMOS, PMOS, and Transmission gates One of the crucial parameters for DAC is Dynamic Nonlinearity which includes DNL and INL. Differential nonlinearity (acronym DNL) represents a deviation of actual step size with reference to ideal step size, where step size is a difference of analog outputs for adjacent input values.

Mathematically DNL for DAC is represented as follows:

$$\frac{V_{out}(i+1) - V_{out}(i)}{ideal\ LSB\ step\ width} - 1$$

Integral nonlinearity (acronym INL) represents a deviation of the actual analog output of DAC with reference to the expected ideal value for a given digital input value. It is also expressed in terms of DNL also.

It is as follows INL (n) = $\sum DNL(k)$

This research is expected to offer advantages over the existing Current steering Digital to analog Converter designs in the literature. The main objective is to minimize Nonlinearity say INL and DNL of DAC for biomedical applications using new types of switches and the concept of segmented DAC.

The Main objectives of this research work are as follows.

- To understand the various architecture of Current steering DAC which includes binarily weighted, unary weighted, and segmented DAC.
- Based on a selection of one architecture, various possibilities are to be explored for the betterment of Nonlinearity error say INL and DNL.
- To propose a design of a 10-bit Current steering DAC for biomedical applications like artificial retina prosthesis ECG/EEG devices.

1.3 STATE OF ART AND PROBLEM STATEMENT

By reviewing, implementing, and comparing the results of the various topologies from the literature as discussed earlier, it can be said that there is always a trade-off between resolution, conversion speed, power dissipation, and non-linear accuracy for DAC so it is very challenging to optimize these performance parameters.

In addition to this, the performance metric for INL and DNL errors plays a crucial role while designing the current steering DAC for the analog front-end of biomedical applications.

After careful study of different topologies, it is found that there is a need to design a Segmented current steering DAC with the following specification for portable devices, wearable electronics, and healthcare devices.

- Low noise
- Low power
- Low INL and DNL error

1.4 DESIGN METHODOLOGY

Based on a detailed literature study, following the road map is adopted to develop a segmented current steering DAC for biomedical applications.

1. Literature survey of DAC Architectures, switching elements, and current steering DAC architectures
2. Measurement setups for Nonlinearity errors in Current steering DAC
3. Problem definition and specification of the proposed design
4. Simulation of possible variants of current steering DAC
5. Result from analysis of proposed designs.
6. Comparison of proposed work with state of art reported from the literature
7. Important Findings

1.5 LIMITATIONS AND SCOPE OF IMPROVEMENTS

There is always a requirement for healthcare devices which includes ADC and DAC in the biomedical field. It is expected to have the best performance of DAC in the form of low power for good battery life, high speed for better diagnosis, and lower value of INL and DNL to offer effective performance in a noisy environment as

well. Digital to Analog Circuit for biomedical applications to be designed with proper specifications. But there are some limitations which to be considered to improve the design further.

- There is a need to find architecture for better Nonlinearity error in form of DNL and INL.
- There is a need to design a novel architecture for DAC which can offer better INL and DNL without compromising area and power consumption.
- The process and temperature variations further degrade the performance and hence yield.

1.6 TOOLS AND TECHNOLOGY

The design of the current steering DAC was done at the schematic level. Cadence Tool is used for transistor-level design and its simulation.

Here mainly the pre and post-layout simulations are carried out using circuit-level simulators like Cadence tools like Virtuoso, ADE L, ADE XL, and Spectre. In addition to that GPDK spice model files for 180 nm are used for simulation.

In this work, the proposed design of a 10-bit Current steering DAC for biomedical applications has been designed using 180nm GPDK technology. The design procedure is also verified using experimental results and it is also compared to recently reported designs from the literature. To obtain parametric variation Monte Carlo analysis is carried out using 180 nm CMOS technology using Cadence.

1.7 CONTRIBUTIONS OF THE THESIS

The major contribution of the thesis is mentioned below:

- Detailed review of different challenges for designing low noise and low glitch witches with focus for better Non linearity error.
- Proposed designs of various types of switches, including (i) NMOS switch, (ii) PMOS switch, (iii) Transmission Gate switch and (iv) Differential switch,
- Approach of Segmented DAC with various combinations like (i) MSBs to be realized using Unary weighted and LSBs using Binary

weighted with various combinations of no of bits in the groups of MSBs and LSBs and (ii) LSBs to be realized using Unary weighted and MSBs using Binary weighted with various combinations of no of bits in the groups of MSBs and LSBs.

1.8 THESIS ORGANIZATION

The organization of the thesis is as follow

In Chapter 1, the Introduction with basics of DACs, Motivation, have been presented. The objectives and the contributions of the research are also outlined briefly.

Chapter 2 (Literature Survey) presents the fundamentals of DAC, various types and its architectures. Evaluation parameters and their significance have been briefly explained in the chapter. Various design methodologies of Digital to Analog Converter have been discussed. The theories and mathematical analysis of INL and DNL is presented in the chapter. State of the art in the field of DAC and specifically current steering DAC reported in the literature are discussed in this chapter as well.

Chapter 3 presents the various possible ways to address the issues regarding DAC. The concept of Segmented DAC has been presented in the said chapter. One more possible option of Fibonacci DAC is also represented and compared with segmented and binary weighted DAC. The concept of Differential switch is also a part of this chapter. The issues with the design of segmented current steering DAC are presented. The pros and cons of the proposed Design are also presented.

Chapter 4 presents the proposed 10-bit current steering DAC design. Detailed analysis of the same is also presented in this chapter. The effect of linearity improvement of the DAC is discussed. The design details and the corresponding results of the proposed current steering DAC summarized in this chapter.

Chapter 5 presents the result and discussions about the proposed DAC. Analysis of the same in terms of pre layout and Post layout are also presented in this chapter. Monte Carlo analysis for Process and Mismatch

variations for the proposed DAC are also presented in this chapter. Performance comparison of the designed DAC is carried out with reference to existing DACs.

Finally, the summary of work, important conclusions based on the research work are presented in Chapter 6. Future scope of the research in this domain is also shared in this Chapter.

CHAPTER-2

LITERATURE SURVEY

2.1 INTRODUCTION

This chapter discusses about basic DAC architectures application-wise implementation requirements and literature survey in current steering DAC reported in the last decade. In addition, it also includes the merits and demerits of basic DAC architectures along with all necessary details. An N-bit DAC takes an input of an N-bit digital word and converts the digital input signal into an analog output signal in the form of voltage or current. A block-level representation for generic DAC is depicted in figure 2.1

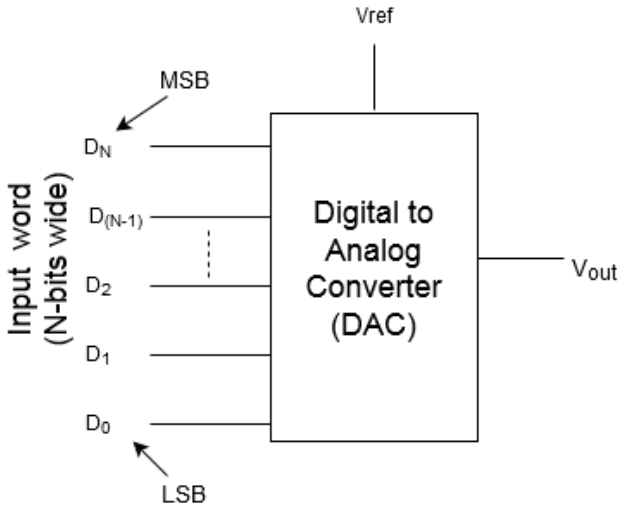


Figure 2.1 N-bit DAC representation

Here, an input N-bit digital word (D_0, D_1….D_{N-1}) is processed through the circuit and the respective output value in form of voltage or current is obtained. If the output is in form of voltage, for N-bit DAC, the output is expressed as follows:

$$V_{OUT} = \left(D_{N-1}\,2^{N-1} + \ldots + D_0\,2^0\right)\frac{V_{REF}}{2^N}$$

$$V_{OUT,\max} = \frac{2^{N-1}}{2^N}\cdot V_{REF}$$

D_0 represents LSB (Least significant bit) and D_{N-1} as MSB (Most Significant bit). Based on Implementation, there are mainly three major types available.

1. Voltage mode
2. Charge scaling based
3. Current mode

In the case of voltage mode, the output is available in form of voltages. With charge redistribution DAC, elements are given by capacitor values and the operation of the DAC is given by a switched-capacitor technique. In the case of the current mode, the output is in form of current.

2.2 CLASSIFICATION OF DAC

Based on circuits there are major types of DAC as below

- Weighted Resistor
- Resistor String
- R-2R ladder
- Charge redistribution
- Current Steering

2.2.1 WEIGHTED RESISTOR DAC

This is of voltage type of DAC, the output is in form Voltage, It consists of no. of resistors having different values in order of power of 2 i. e 1k, 2k, 4k , 8k, etc.. total no. of resistors is 2N. Here each branch based on the input bit value (either 1 or 0) generates weighted currents which are added at the input of current to the voltage converter to generate the final analog output. The formula is given by the following expression.

$$Vo = \{ R_F/(2^{N-1}*R)\}* \{2^{N-1}*V_{N-1} + 2^{N-2}*V_{N-2} + ... + 2^1*V_1 + 2^0*V_2 \}$$

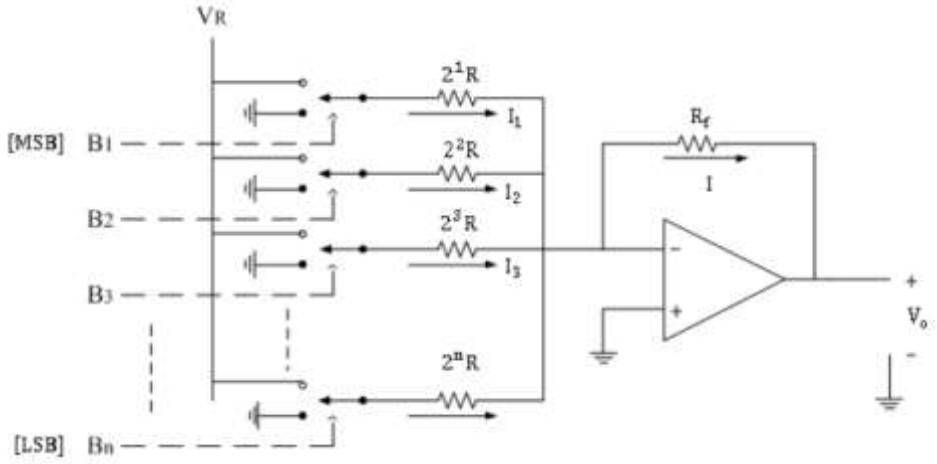


Figure 2.2 Weighted R DAC

Advantages:

• The architecture is very simple.

• It offers high speed conversion.

Disadvantages:

• It requires high precision weighted resistors.

• It needs high speed transistors.

• The resulting implementation will be costly.

2.2.2 RESISTOR STRING DAC

The Resistor string DAC referred to as Kelvin-Varley divider, is one of the simplest types used to implement analog conversion. In its simplest form, the string DAC is just a series of equal-value resistors with a tap point between each resistor. As shown in figure 2.3 for each input bit there is pair of switches (controlled by digital input bits) either of one is on at a time based on the bit is 1 D_0 is on else D_0 bar switch is on. Hence the digital code given at the input of the DAC will set the switches on or off, which gives the single voltage value as the output. This limited switch movement results in very low glitch generated, in turn, improves the noise performance. Ideally, each resistor will generate a voltage drop from the reference equal to 1 LSB.

This is one type of Voltage mode DAC, Output is in form of Voltage, here we have a string of equal resistors (the number. of resistors is 2*N), and there is something voltage divider kind of mechanism as shown in the figure. Here no. of switches is

$2*(2^N-1)$. Variations in the value of Resistors and unequal value of delay of switches lead to non-linear error in the generated output.

Advantages:

- Takes full advantage of the availability of almost perfect switches in MOS technologies
- Simple, fast for 10bits
- Inherently monotonic
- Compatible with purely digital technologies

Disadvantages:

- 2B resistors & ~2x2B switches for B bits hence large component count & large are and power dissipation for resolution>10bits
- High settling time required for high-resolution DACs

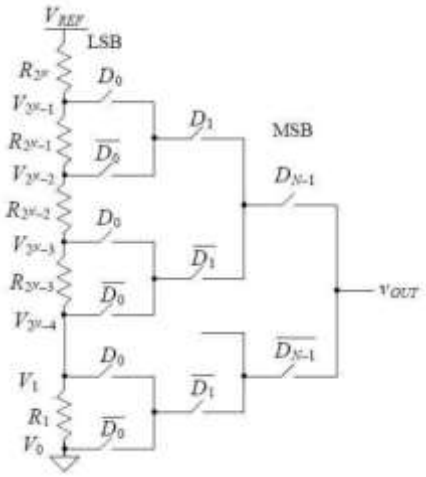


Figure 2.3 Register string DAC

2.2.3 R-2R LADDER DAC

The main limitation of the Resistor string DAC is nonlinearity associated with tolerance of Resistance and switch delays hence it is very difficult for the designer to maintain linearity while designing the DAC. The number of resistors required for the string DAC increases exponentially as resolution increases unless clever design tricks are implemented like cascaded resistor strings or interpolating amplifiers.

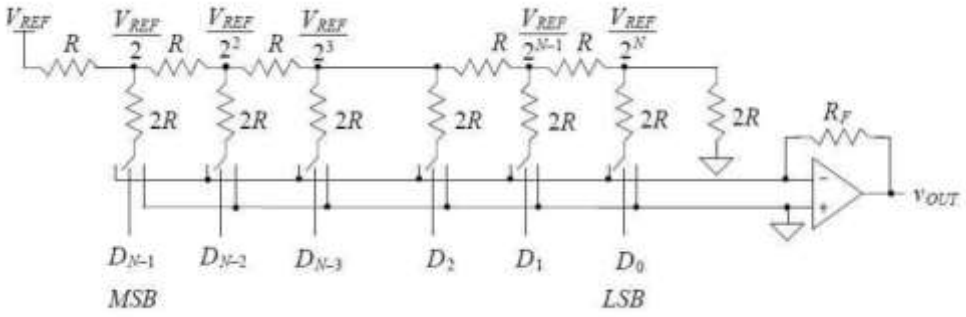


Figure 2.4 R-2R ladder DAC

The R-2R architecture resolves this problem by using binary-weighted resistors in the ladder arrangement.

Advantages:

- There are only two resistor values used in this type of architecture.
- It does not require precise resistors like Binary weighted architecture.
- It is low-cost and easy to Implement.

Disadvantages:

- The Resulting architecture is very slow.

  For a given N-bit DAC if the number of quantization levels is 2^N and the Number of Steps is $2^N - 1$ the resolution or step size of the DAC is given as the following expression.

  - Analog output/Number of steps = $V_{out} / (2^N - 1)$
  - % Resolution = (Step Size/Full scale output) x 100 %

2.2.4 DELTA-SIGMA ARCHITECTURE

The Sigma Delta DAC uses sigma-delta modulators for generating differential samples by comparing present and previous samples. Sigma–delta modulator (SDM) has become a popular method to implement high-resolution digital-to-analog converter (DAC); this method uses oversampling along with noise shaping for the suppression of quantization noise in the signal frequency band. The main benefits of SDM are their good linearity performance along with robust overall implementation [1].

These above-mentioned features of the SDM make it very attractive for a number of applications these architectures are based on oversampling concept. They are often used where the linearity of the circuit is given more priority compared to the

bandwidth of the circuit. It offers a very high resolution of 12 to 32 bits and is used in biomedical applications.

The block diagram of Sigma Delta DAC consists of a sigma-delta modulator, a digital interpolation filter, and a 1-bit converter. The input data stream is fed slowly to the interpolation filter. It adds zeros into the input bit string which increases the number of words in a given time interval, which further enhances the sampling rate of the converter. The filter assigns values to the input words to shift the noise in the output spectrum toward the high-frequency side. This will remove noise from the signal band which reduces the in-band noise of the information signal with increasing the resolution of the resulting DAC.

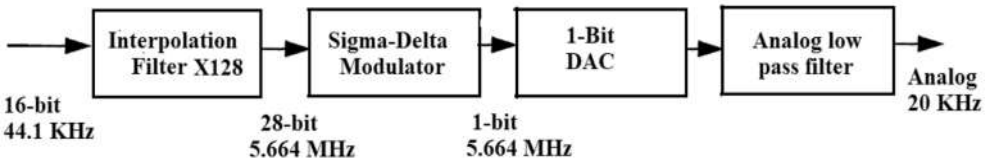


Figure 2.5 Delta Sigma DAC

2.3 CURRENT STEERING DAC

Current steering-based analog converters are the most fabricated on-chip for biomedical wearable devices including retina prostheses to neural stimulator ASICs. These DACs are very popular due to their small size and simplicity. They suffer from errors due to matching between various current sources and also due to switching noise and delays. Now designers can come up with newer applications easily by making use of the design scalability of CMOS circuits previously designed and developing the chips or applications very fast as per the user's demands and wishes. In addition, ASIC Fabrication is widely adopted in the literature to develop such biomedical instruments or wearable devices due to high linearity and low area -power with reasonable accuracy. This is why integration technology uses this type of Converter in their work.

In place of using Resistors for generating weighted voltage levels, the current steering DAC uses weighted current sources to convert the digital input bit pattern to the corresponding analog voltage output. The final generate voltage is the addition of all input bit place value-based current given to the circuit which is all added at

the input node and generates the single value analog output. Here the contrast is in signal definition as well as implementation. The current is being steered within the circuit according to the digital input given. There are three possibilities in the resulting architectures of the current steering converters: unary, binary (weighted place value), and segmented (a hybrid of the first two).

- Unary, uses double the number of current sources for input word length.
- Binary, uses same the number of current sources for input word length.
- Segmented, which is a mixture of the above two types.

Another important requirement is high-speed switches to insert the input bit at a fast rate which should offer low noise distortion and propagation delays. The switches must be operated quite fast to steer current in the output according to the given digital input word. In these designs, to further enhance the accuracy of conversion different methods of generating current sources like a simple current mirror, cascode current mirror, Wilson current mirror, or Regulated cascode current mirrors can be adopted. A block diagram of a Current Steering based converter is represented in figures 2.6 and 2.7. There are basically three types of current steering DAC used for the purpose.

Based on the type of architecture of the current sources used, the Current Steering data converters are mainly classified in two different ways namely Binary weighted and Unary weighted Current Steering converters. A 4-bit binary-weighted converter is depicted below shown in Figure 2.6 which is designed for 4-bit input. The advantage is it needs fewer numbers of current sources and generates significant glitches due to major transitions of bits.[3][5][10]

In unary DAC, 2^N-1 current sources are required to convert the N bit into an analog signal. Each current source is having the same current value in this case. A 4-bit unary and binary-weighted DAC is represented as shown in Figures 2.6 and 2.7. In this case, the advantage is - as there is only a one-bit change, there will be no glitches. But need a greater number of current sources which results in more area. A concept of segmented DAC can be used to optimize the Static performance of DAC as well as area and power requirements.

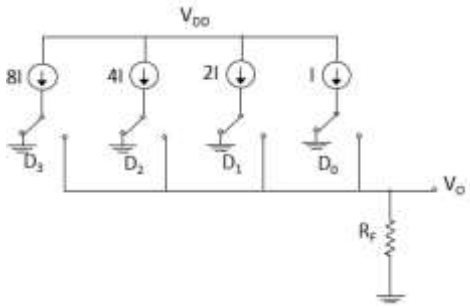


Figure 2.6 Binary representation of current steering structure.

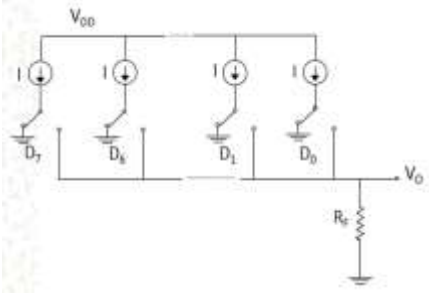


Figure 2.7 Unary representation of current steering structure

2.4 SEGMENTED CURRENT STEERING DAC

As discussed in the previous section unary sources do not require weighted sources and hence, they are free from error due to accuracy in weighting but use 2b sources for b-bit resolution which in turn increases power and area requirements and also needs an additional block known as a thermometer to the binary code converter increase the power- area needs, on the contrary, weighted binary sources-based realizations save the resource like power area as no need of thermometer decoder.

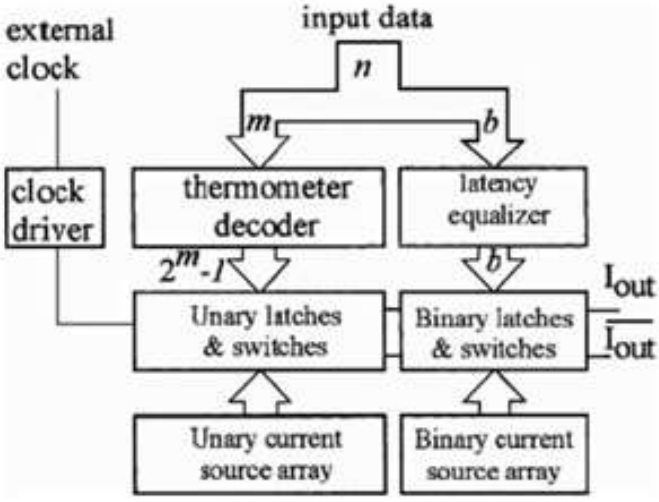


Figure 2.8 Basic block diagram of segmented current steering DAC

The Integral and Differential Nonlinearity errors mainly depend on the glitches produced by the current cell due to the non-linearity produced by drain voltages. The amount and magnitude of the glitches that appear at output depend on the no. of transitions the binary inputs make at a time. The increase in the number of transitions leads to an increase in the switching noise produced due to glitches at a time. In the case of 4-bit binary-weighted DAC, when input changes from 0111 to

1000, a severe glitch is observed because of transitions either from 1 to 0 or 0 to one at all bit positions.[3]. In the case of unary weighted DAC, there is only a 1-bit transition at a time so there is no glitch but it needs more no. of current sources. In case of 4-bit unary current steering DAC, 15 ideal current sources are required. A thermometer code is used to operate the switches. Here additional hardware is required for binary to thermometer code conversion. One such binary to thermometer code conversion is shown in Table 2.1.

Table 2.1 Binary to thermometer code representation

Binary code	Thermometer code		Binary code	Thermometer code
0000	000000000000000		1000	000000011111111
0001	000000000000001		1001	000000111111111
0010	000000000000011		1010	000001111111111
0011	000000000000111		1011	000011111111111
0100	000000000001111		1100	000111111111111
0101	000000000011111		1101	001111111111111
0110	000000000111111		1110	011111111111111
0111	000000001111111		1111	111111111111111

To get the benefits of both the binary-weighted and unary-weighted DAC, the concept of segmented DAC is explored in the proposed work. For DAC having N inputs, M bits have been implemented using unary weighted DAC while (N-M) bits are to be implemented using binarily weighted.

The differential nonlinearity (acronym DNL) is a measure of the error in DAC by comparing the response of ideal and practical DAC step width. It is defined as the deviation between two analog values corresponding to adjacent input digital values. The following equation determines dynamic non linearity error for a given DAC [1][3].

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{ideal\ LSB\ step\ width} - 1$$

The Integral nonlinearity (acronym INL) can be evaluated similarly as discussed above by comparing ideal and practical DAC responses. It represents a deviation of the actual analog output of DAC with reference to the expected ideal value for a

given digital input value. It is also expressed in terms of DNL. The mathematical expression is as follows.[3]

$$\text{INL (n)} = \sum_{k=0}^{n} DNL(k)$$

2.5 SWITCHING ELEMENTS

For the current steering DAC, the type of switch used and its noise delay performance characteristics contribute a lot to nonlinearity errors known as integral and differential non-linearity performance. These errors arise from propagation delay of "on" channel resistance, "off" resistance, "on to off" resistance ratio, and a parasitic capacitance at the output. The proposed work uses various types of switches like nMOS, pMOS, transmission gates, and differential switches. The nMOS and pMOS switches are typical and widely used approaches not only for digital to analog converters but for almost every implementation of digital logic device. The input digital word operates the switches "on" or "off". The pMOS-based implementation occupies more area compared to an nMOS-based implementation. For better resistance characteristics, a transmission gate is a good option. It is the parallel combination of nMOS and pMOS devices. Here additional complementary control inputs are needed to control the transmission Gate.

2.5.1 DIFFERENTIAL SWITCH

The current-switching structure like nMOS, pMOS, and others suffer from dynamic errors due to device mismatching. The device mismatching leads to changes in drain-source voltage variations leading to nonlinear variations in generated current. Here when a switch is turned off, the terminal voltage of its corresponding current source collapses to zero. Thus, the next time when this branch is enabled, the (nonlinear) capacitance at this terminal must charge up to VDD, drawing a significant transient current from the output node. Moreover, the switching actions also bring variations in value of the total current carried by the array, subsequently the ground voltage experiences large fluctuations in the presence of parasitic series inductances, such as those due to bond wires.

Both of these effects can be greatly suppressed through the use of the current steering technique. Here, the tail current is steered to one or both sides in each differential pair, causing only a small voltage excursion at the output.

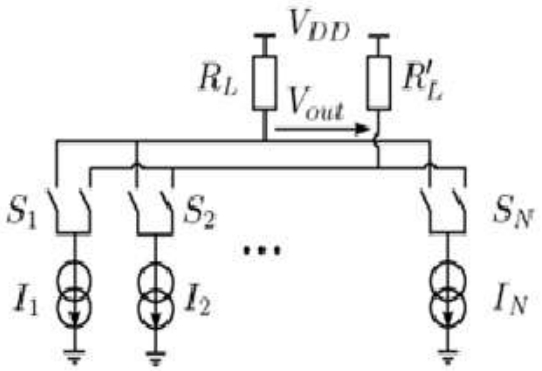


Figure:2.8 Differential switch used for current steering DAC

Also, since the total array current is mostly constant, the ground bounce is much smaller in value. In addition, another advantage of this configuration is it generates differential outputs. For proper matching among the current sources, here the unit cell is first designed using a simple current source with a differential switch which is repeatedly used to build the whole arrangement for n-bit resolution. That is, cell number i consists of 2i-1-unit cells in parallel, and the entire data converter contains 2*2n - unit cells.

The only drawback of current-steering conversion is their limited output voltage compliance. In this implementation, the differential-pair transistors must operate in saturation (as explained below), and, therefore, at least two drain-source voltages are subtracted from the supply and V_{DD}. Another difficulty in the design is the choice of digital input voltage logic level values.

The most convenient are rail-to-rail swings, but, such a choice 1) limits the analog output voltage range V_{max} to one transistor threshold if the transistor must maintain the saturation condition and 2) leads to large dips in node voltage during the transitions of S2 and Sn switches input. In other words, we would prefer only a moderate swing for the digital inputs, with a maximum level less than V_{DD} so as to allow a greater V_{max}. Such swings need another differential pair switch hence substantial power consumption.

2.6 CURRENT MODE DACS ASIC IN CMOS TECHNOLOGY

Submicron Integration technologies have become a very popular option for designing high sample rate switched current-based digital to single analog value converter designs [1–9]. The Switching speeds of submicron gate length MOS transistors have allowed oversampling rates of the few hundred mega samples easily and at the extreme beyond a giga-sample-per-second. The resolutions from 8 to 16 bits are achieved in two-step methods where MSBs and LSBs are separately converted is the most popular approach for almost all types of wearable ASIC designs. The MSB is always made from unit-weighted elements and is thermometer-coded. The number of bits in the MSB segment can vary from as few as 4 bits to as many as 8 bits, with 5 and 6 bits being the slightly more common choice. The rest of the bits may be binary-coded but are often further segmented into a thermometer-coded intermediate significant bit (ISB) section and an LSB binary-coded section.

Unlike switched capacitor circuits used in many data converter applications, which require mixed-signal process variants with high-quality poly-poly or metal-metal capacitors, switched current converters can make use of the standard fabrication technologies. The designs have been downscaled from 0.8 to 0.18 μm gate length devices and beyond in the last decade. The general block diagram of one such bio-medical ASIC reported in literature is shown in figure 2.9 below.

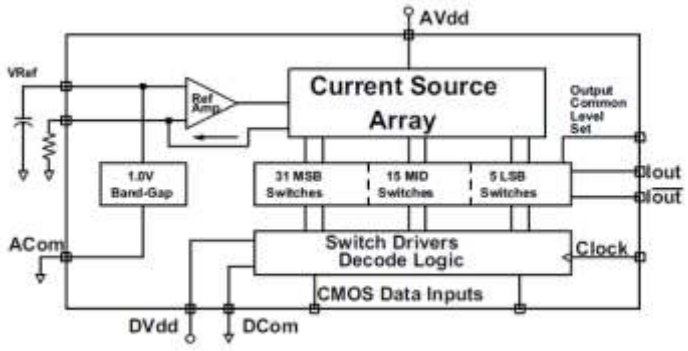


Figure 2.9 current modes in DAC [1,8]

The structure depicted in Figure 2.9 is the basic structure of a typical CMOS DAC [1,8]. This implemented converter offers 14 bits of overall resolution. The five MSBs are composed of 31 unit-weighted elements and are thermometer-coded. Each unit element consists of a cascaded pMOS current source and a pMOS differential current switch pair. The remaining nine bits of the DAC are segmented into four thermometer-decoded intermediate bits with the five LSBs being binary-

coded. Because just five of the MSBs are thermometer-coded, leaving 9 bits remaining, the inclusion of the thermometer coding for the 4 intermediate bits helps insure these 9 bits have sufficient INL and DNL accuracy for the overall resolution of the DAC.

2.7 CURRENT STEERING DAC FOR BIOMEDICAL APPLICATIONS

As discussed in earlier sections at the architecture level, current steering digital to analog converters is further categorized as unary, binary, and segmented architectures. The unary architecture consists of an array of matched current sources that need low area power. In addition, the structure has better differential non-linearity specification and if designed carefully, it has a better dynamic performance. However, as the number of bits increases, decoder complexity grows exponentially along with a significant increase in digital noise contribution. The architecture needs a more careful layout design which improves matching and also requires the largest silicon area among all architectures presently used. [2] The binary-weighted architecture [3,4] consists of binary-weighted current cells and hence the architecture requires the least hardware complexity, area, power, and design time. High glitch areas at major code transitions and strict current cell matching requirements are major limitations of this architecture.

An intermediate architecture that utilizes the advantage of both architectures is segmented architecture [5]. In this least significant bit (LSB) is a binary-weighted and the most significant bit (MSB) has unary weighted architecture. The segmented architecture has less complexity than unary weighted architecture for the same DNL specifications. On an increasing number of bits, the complexity of the decoder increases, and the timing skew of the decoder output introduces glitches at the output, thus limiting its dynamic performance. Several such types of Implementations are reported in the literature and the list is quite long but a few significant are mentioned below.

1. Recently in May 2022, a 12-bit partial segmented current steering digital to analog converter (DAC) with low glitch area, power consumption, and integral nonlinearity error is designed by Abhishek Kumar et al [10]. This paper discusses the causes of glitch energy in detail with possible solutions. In this implementation, the current-mode logic-based latch is used which reduces the

output swing from V_{DD} to Vth used at the input to the differential switch to reduce the glitch energy in terms of pico volts. It also helps to reduce the allowable minimum voltage headroom as compared to a double cascode structure as a switching device hence reducing the power dissipation to around 9.1 mili Watts operating at 200 MHz. The design and simulation of the current steering DAC are performed in a 0.18-micron standard CMOS technology library using the Cadence Virtuoso tool with a supply voltage of 1.8 V.

2. An 8-channel current steerable, multi-phasic neural stimulator with on-chip current digital to analog converter with calibration and residue nulling for precise charge balancing [11] is reported for neuro simulator applications that offer the differential non-linearity within ±0.3 LSB.
3. A Tripolar Current-Steering Stimulator ASIC for Field Shaping in Deep Brain Stimulation applications [12] was reported and fabricated using a 350nm CMOS process. In this work, a 4-bit multi-bias DAC is designed which controls the ratio of currents flowing in various anodic branches. The overall architecture occupies a reasonable silicon area.

It uses four voltage-to-current converters blocks, each controlling a 4-bit current-steering DAC. A 4-bit multi-bias DAC is used to control the ratio of the current flowing through the anodic branches. A circuit is used to generate exponential decay at the end of each pulse for anodal blocking. A control signal is used to switch the VIC inputs from the 4-bit DAC to the circuit. The switching at the output network is monitored by a timing control signal that regulates the anodic and cathodic portion of each stimulation cycle, which changes the direction of the currents through the electrodes.

Two types of DACs are found one is 4-bit Current steering and another is a multi-bias current steering DAC. They are simulated which results in a minimum range of integral nonlinear error achieved was 0.19 LSBs to 0.59 LSB and a maximum range of dynamic nonlinearity was 0.32 LSBs and 0.71 LSBs. Part of the nonlinearity of the multi-bias DAC is due to the fact that the transfer characteristic of a transistor biased in the triode region is logarithmic.

4. Further the author found several implementations reported from the literature which are mainly focused on the design of low-resolution low-power current steering digital-to-analog converters for use in large arrays of neural-type cells. Some of them used ultra-low-size MOS devices that are biased in weak inversion

regions to yield small currents and low power dissipations when building large-size arrays. The only drawback of operating the device in weak inversion resulting in poor matching between the transistors. The resulting effective precision of a fabricated array of a few tens of stacks of such DACs generates a transistor mismatch error of 47% (1.1 bits).

5. Further lots of work focused on segmented and binary-weighted architectures referred to as pseudo-segmented architecture [6-10]. It does not require encoders and decoders, thereby reducing timing skew and digital noise for higher-resolution DACs. The architecture requires a smaller number of well-matched weighted current cells as in segmented architecture.

While carrying out the literature survey the author found that the Pseudo-segmented architecture is the most accepted design for applications demanding high-speed and high-resolution performance. Apart from the architectural modification of DAC, currently, a lot of work is being reported on calibration and Dynamic Element Matching (DEM), which is another way found to improve the linearity of the current cells. Further, it also reduces the effect of transistor mismatch dynamically. In this type of designs the glitch area is also significantly reduced, but it adds circuit complexity in terms of level shifters, rotators, multiplexers, etc. [6–10].

To achieve higher operating frequency, glitch area reduction plays a major role while designing any application-specific DAC. A large glitch area increases settling time and hence reduces the maximum allowable operating frequency. Meng-hung Shen et al. [10-19] have reported the glitch area reduction method by using Dynamic Element Matching (DEM) and proved it by implementing a 6-bit DAC. Shu-Chung Yi [12] has implemented 10-bit by using binary to abacus encoder and decoder for all 10 bits. However, they use complex logic circuits and barrel rotator which adds digital noise to output and is not ideal for low power.

Besides, the glitch area is more severe for higher-resolution DACs. Jurgen De Veugele et al. [13] proposed a 10-bit binary-weighted DAC with a glitched area of 2.64 pico volts but do not focus on methods for its reduction. Fang-Ting Chou et al. [14] consider the glitch area due to delay-dependent output. They have used partial and full compensation of output capacitance to reduce input code dependent delay and increase the capacitance at the output node which in turn increases settling time and limits its maximum allowable operating frequency.

2.8 GENERAL APPLICATIONS AREAS

Apart from applications discussed in earlier sections DACs are also found useful for many general-purpose digital signal processing applications. Some of the important applications are discussed below.

Audio Amplifier: DACs are used to produce DC voltage gain with Microcontroller commands. Often, the DAC will be incorporated into an entire audio codec which includes signal processing features.

Video Encoder: The video encoder system will process a video signal and send digital signals to a variety of DACs to produce analog video signals of various formats, along with optimizing of output levels. As with audio codecs, these ICs may have integrated DACs.

Display Electronics: The graphic controller will typically use a lookup table to generate data signals sent to a video DAC for analog outputs such as Red, Green, Blue (RGB) signals to drive a display.

Data Acquisition Systems: Data to be measured is digitized by an Analog-to-Digital Converter (ADC) and then sent to a processor. The data acquisition will also include a process control end, in which the processor sends feedback data to a DAC for converting to analog signals.

Calibration: The DAC provides dynamic calibration for gain and voltage offset for accuracy in test and measurement systems.

Data Distribution System: Many industrial and factory lines require multiple programmable voltage sources, and this can be generated by a bank of DACs that are multiplexed. The use of a DAC allows the dynamic change of voltages during operation of a system.

Digital Potentiometer: Almost all digital potentiometers are based on the string DAC architecture. With some reorganization of the resistor/switch array, and the addition of an I2C-compatible interface, a fully digital potentiometer can be implemented.

CHAPTER-3

CURRENT STEERING DAC VARIANTS

3.1 INTRODUCTION

This chapter mainly discusses specifications and applications related to current steering DAC including various biomedical and wireless application requirements. It includes retina prosthesis and neural simulator-based ASICs which widely uses high speed highly linear and low power area needs with all the necessary details. Selection of the appropriate DAC architecture depends on the application needs and also specifications requirements. But for general purpose applications, it is expected to have good performance of DAC in form of linearity error i.e. INL & DNL, gain error, offset error. Dynamic performance is affected by non-linearity such as glitches and time skew [6].

Based on the binary inputs, DAC produces a single analog voltage or current output. The signal which is continuous in amplitude and time domain is obtained from the signal which is discrete in both the said domains with the reference input voltage applied to the data converters. The Current steering DAC among various types of DACs are popular because of the fact that these data converters provide high-speed conversion with higher resolution using lower consumption of power [2],[7].

Digital-to-Analog Converter employing Current Steering topology has a higher speed of conversion and also supports increased resolution. To improve the matching precision of the current sources the Current Steering DAC is typically employed.

3.2 HIGH-SPEED CURRENT STEERING DAC FOR BIOMEDICAL APPLICATION.

The matter of the retinal prostheses is represented in Fig. 3.1. The external camera is used to capture the image. The image information is converted into an associated analog signal. The chip is implanted in the retina, converted signal is fed to the chip by wireless media. The chip offers artificial vision by the process of stimulation and the same is available to retinal cells. Various Experiments have been carried out with different laboratory settings & Patients. So far, blind patients can read large fonts using prostheses. However, the perceptual resolution of current systems is quite low.

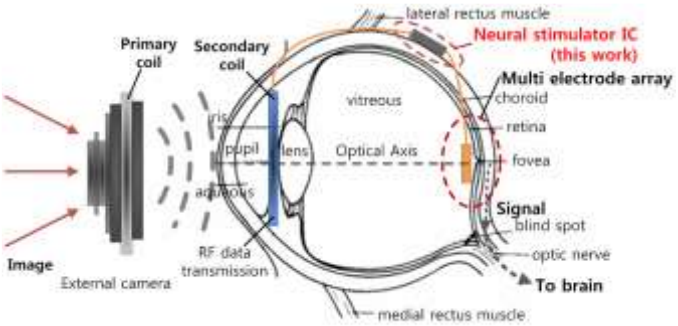


Figure 3.1(a) Application of Neural Stimulator IC for retinal Prosthesis

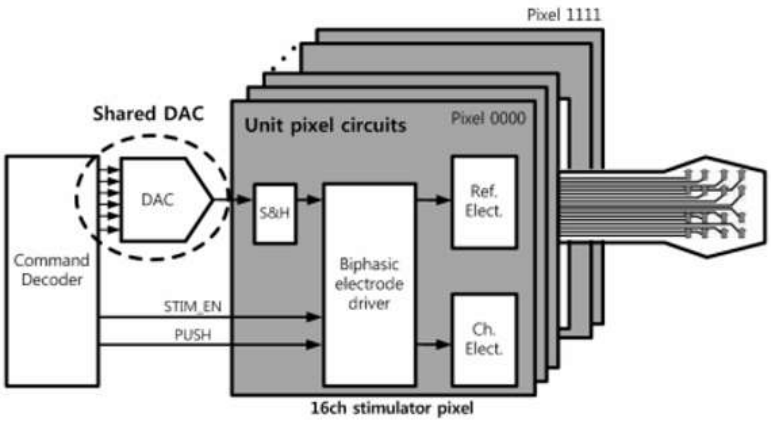


Figure 3.1(b) Neural Stimulator IC

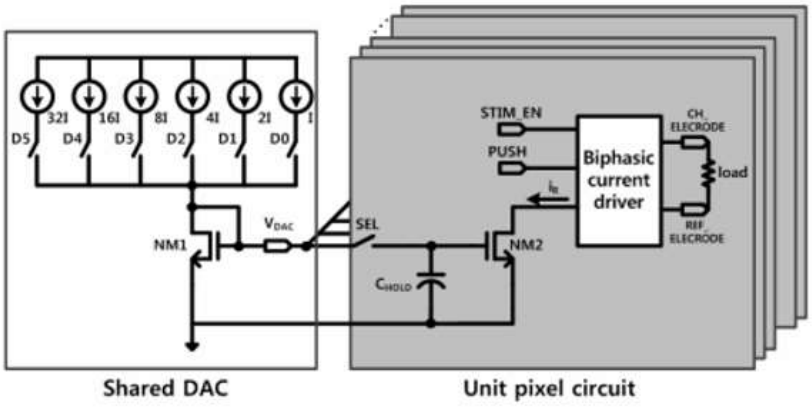


Figure 3.1(c) DAC Sharing Scheme

Figure 3.1. Concept of artificial retinal prostheses.[4]

1. Neural stimulators have been employed in the visual prostheses system based on functional electrical stimulation (FES). Due to the size limitation of the implantable device, the smaller area of the unit current driver pixel is highly desired for a higher-resolution current stimulation system. This paper presents a 16-channel compact current-mode neural stimulator IC with a digital-to-analog converter (DAC) sharing scheme for artificial retinal prostheses. The individual pixel circuits in the stimulator IC share a single 6-bit DAC using the sample-and-hold scheme. The DAC sharing scheme enables simultaneous stimulation on multiple active pixels with a single DAC while maintaining a small size and low power. The layout size of the stimulator circuit with the DAC sharing scheme is reduced to 51.98 %, compared to the conventional scheme. The stimulator IC is designed using a standard 0.18 μm 1P6M process. The chip size except for the I/O cells is 437 μm ´ 501 μm.

3.3 EFFECT OF DIFFERENTIAL SWITCH ON PERFORMANCE OF CURRENT STEERING DAC

Since switching actions change the total current carried by the array, the ground voltage experiences large fluctuations in the presence of parasitic series inductances, such as those due to bond wires. Both of these effects can be greatly suppressed through the use of current steering (Figure 3.2). Here, the tail current is steered to

the left or the right by each differential pair, causing only a small voltage excursion at node –X. Also, since the total array current is relatively constant,

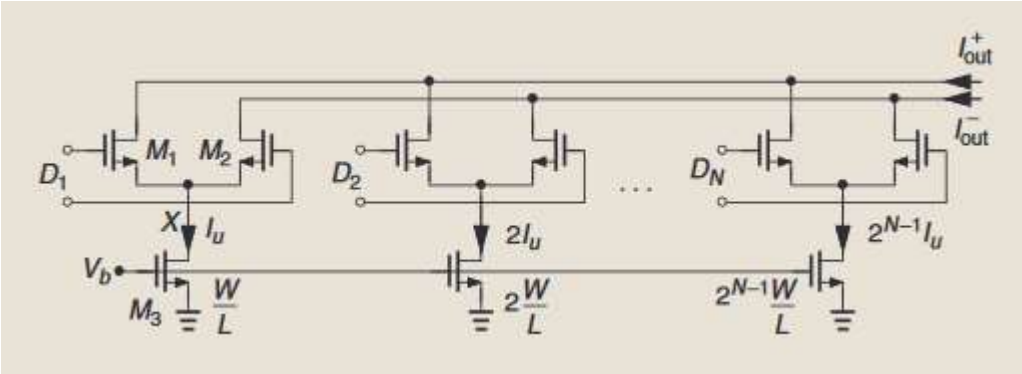


Figure 3.2 A binary-weighted current-steering DAC using a differential switch [5]

the ground bounce is much smaller. Of course, another advantage of this configuration is that it naturally provides differential outputs. [5]

3.4 EFFECT OF SEGMENTATION ON CURRENT STEERING DAC.

For the majority of communication circuits, the most commonly used high-speed DACs are based on current-steering architecture. Typically, an N-bit current-steering DAC is designed using a segmented structure in which input bits are divided into two groups with B less significant bits switching binary coded current sources and (N–B) most significant bits switching thermometer coded unary current sources (Fig. 1). A layout-dependent switching sequence that minimizes the systematic errors of such architecture is presented in [3]. Using the results in [4] as a basis, a new cost-oriented approach to optimize the design area is developed. The optimum design can be obtained by reducing the area of the current source transistors. The corresponding DAC could feature a smaller size in comparison to equivalent subsystems reported in the literature. In order to achieve high linearity and Spurious Free Dynamic Range (SFDR), a large degree of segmentation has been used in [5] for a 12-bit 320- Mega Sample/s current-steering D/A converter in 0.18-lm CMOS, with the seven most significant bits (MSBs) being implemented as equally weighted current sources. A ‘‘design-for-layout’’ approach has allowed limiting the device area to just 0.44 mm2. The increased switching noise associated with a high degree of segmentation has been reduced by a new latch architecture. The block diagram of the current steering DAC is shown below in figure 3.3

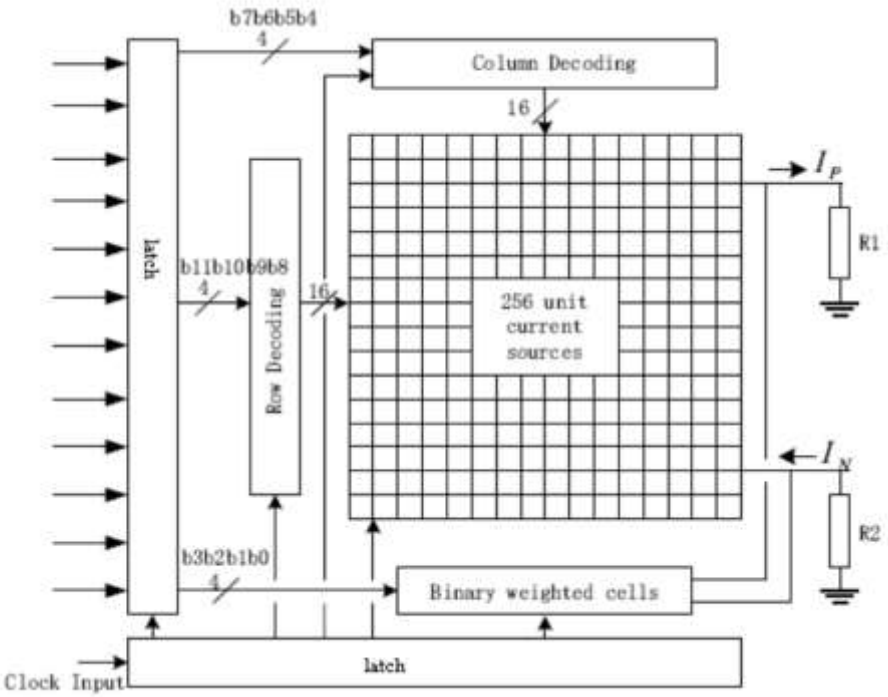


Figure 3.3. Block diagram of segmentation in Current steering DAC [13]

To get the benefits of both say binary weighted and unary weighted DAC, the concept of segmented DAC is explored. For DAC having N inputs, M bits have been implemented using unary weighted DAC while (N-M) bits are to be implemented using binarily weighted. The representation is as below shown in Figure 3.4

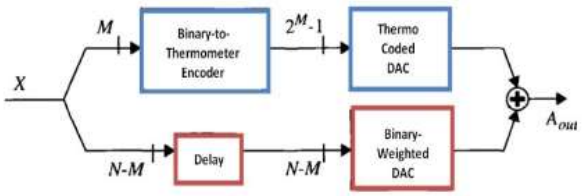


Figure 3.4 Logic and Concept of Segmented DAC

3.5 COMPARATIVE ANALYSIS OF CURRENT STEERING DAC.

The amount of INL and DNL depends on the type of architecture say binarily weighted, unary weighted, or segmented DAC. Types of switching also have a great impact on the INL and DNL. This article presents the design and implementation of segmented DAC using various switches like NMOS, PMOS, Transmission Gate, and differential switch. The concept of segmented offered the advantage in form of a reduction in glitches compared to binary-weighted DAC. Looking at the

comparison of all, the Results of DAC using a differential switch offered an advantage in form of uniform step size on output. Eventually those results in form of better INL and DNL. In order to simulate the design, a cadence virtuoso tool with 180 nm MOS technology is used.

Table 3.1 Comparative analysis of reported Current steering DAC

Parameters	[7]	[9]	[5]	[4]	[6]
Resolution (bits)	10	6	8	4	6
Technology (nm)	65	90	65	65	500
Supply voltage (V)	3.3 V	1.2/1 V	1	1.2	3
Power (mW)	76	17.7	0.54	30	3.1
Area (mm^2)	0.135	0.038	0.01	-	-
DNL (LSB)	0.4	0.06	0.47	0.12	0.17
INL (LSB)	0.55	0.09	1.58	0.16	0.33
SFDR (dB)	74	37.2	-	23.3	-
frequency	122 MHz	-	1Mhz	-	-
Conversion rate	500Mhz	3.1 Gs/S	-	10Ghz	-
Segmentation	Yes	No	No	No	Yes

3.6 SPECIFICATION FOR PROPOSED DESIGN.

The parameters of the proposed DAC are shown in Table 3.2

Table 3.2: specifications of proposed DAC

Parameters	**Proposed value**		**Parameters**	**Proposed value**
Technology	180		INL (Max)	0.34 LSB
Resolution	10 bits		DNL (Max)	0.36 LSB
Approach	Segmented		Power (Max)	20mW
Supply voltage	1.5-3.3 V		Frequency	200 Mhz

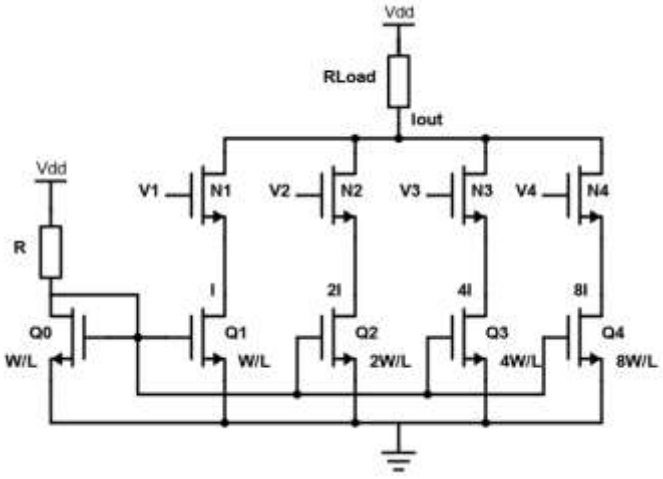
The proposed structure of the current steering offered a significant improvement in INL and DNL. The same will have a good application in the field of medicine. It is observed that the Static error in the output current of the DAC mostly depends on the type of switch, speed of switching, and combination of segmentation. The proposed segmented DAC offers better static performance in form of INL and DNL. The result of DAC shows a reduction in glitches which results in an improvement in INL and DNL values. Total DC power dissipation is 22 milli Watts at 1.8V. The proposed DAC offers a desirable performance in form of DNL and INL which is in the range of $\pm$0.5 LSB.

CHAPTER-4

PROPOSED CURRENT STEERING DAC

4.1 PERFORMANCE ANALYSIS OF UNARY AND BINARY DAC ARCHITECTURE

The architecture of 4-bit binary weighted Current steering DAC using NMOS switches is represented in Figure 4.1. Here, transistors Q_1 , Q_2, Q_3 and Q_4 are part of current mirror circuit. They are responsible for the generation of weighted currents I, 2*I, 4*I and 8*I. The additional transistors N_1, N_2, N_3 and N_4 are used as a switching element. Figure 4.2 shows analog output current for given binary inputs. Here, major glitches are observed when input changes from 01111 to 10000. Secondly, the output current does not show linear increase for increase in binary inputs.



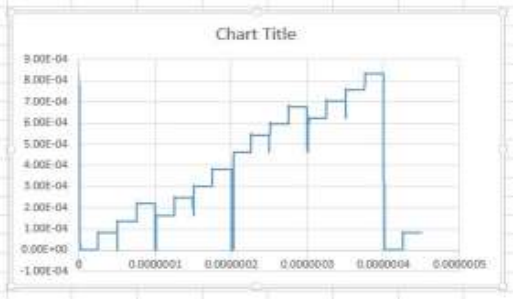


Figure 4.2 Output 4-bit binary weighted DAC using NMOS switches

Figure 4.1 Architecture of 4-bit binary weighted DAC using NMOS switches.

4.2 DESIGNING HIGH SPEED DAC FOR RATINA PROSTHESIS

The proposed 5-bit segmented current steering DAC is implemented in cadence virtuoso 180 nm technology. The DAC is simulated with supply voltage of 1.8 V and 200 MHz of the maximum sample rate. The simulated design consumes power of 20mW at sampling rate of 200 MHz. The simulated DNL and INL observed are ±0.36 LSB and ±0.34LSB, respectively.

Figure 4.3 and Figure 4.4. shows the simulated results and output of proposed segmented DAC with compared to Binary weighted DAC.

Figure 4.4 shows output in form of current for binary inputs. Major glitches are observed when input changes from 01111 to 10000.

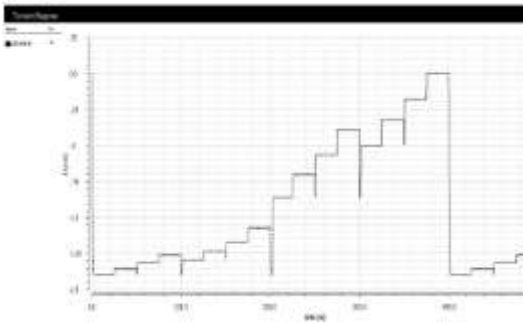


Figure 4.3 Current output of binary weighted DAC with NMOS switches

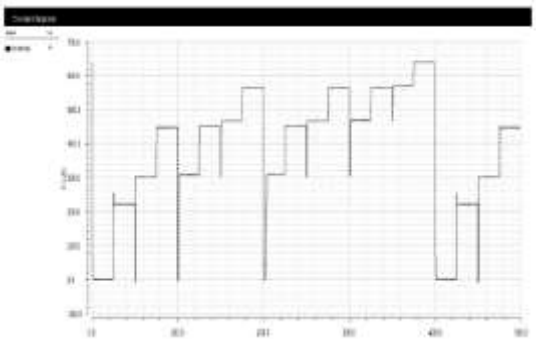


Figure 4.4. Current output of binary weighted DAC with PMOS switches

4.3 EFFECT OF SWITCHES ON PERFORMANCE OF CURRENT STEERING.

4-bit Current steering DAC were implemented using various kind of switches and results are compared. the results are summarised in Table 4.1. It has been observed Differential switch approach offers better INL and DNL.

Segmented approach is also covered with differential switch. In case of of segmented approach, 2 MSBs are realized with unary while 2LSBs with binary weighted one.

Table 4.1 Comparison table for different type of switches

Parameters	Simulated Value			
	NMOS Switch	PMOS Switch	Transmission Gate switch	Differential switch
Technology	180	180	180	180
Resolution	4 bit	4 bit	4 bit	4 bit
Approach	Binary weighted	Binary weighted	Binary weighted	**Segmented**
Supply voltage	1.8 V	1.8 V	1.8 V	1.8 V
INL (Max)	0.63 LSB	0.7 LSB	0.54 LSB	**0.34 LSB**
DNL (Max)	0.56 LSB	0.72LSB	0.43 LSB	**0.36 LSB**
Power (Max)	14mW	18mW	26mW	20mW
Frequency	200 Mhz	200 Mhz	200 Mhz	200 Mhz

4.4 VARIANTS OF SEGMENTD CURRENT STEERING DAC.

To address the problem of glitches, the concept of Segmented DAC is used here. Here Differential switches have been used There are two options are explored (a.) LSBs are implemented using Unary current sources and MSBs are implemented using Binary current sources. Current output of the same is represented in Figure 4.5 LSBs are implemented using Binary current sources and MSBs are implemented using Unary current sources. Current output of the same is represented in Figure 4.6

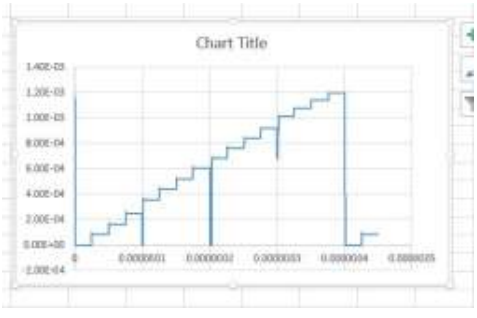


Figure 4.5 Output of segmented DAC using Differential switches (LSBs are Unary and MSBs are Binary sources)

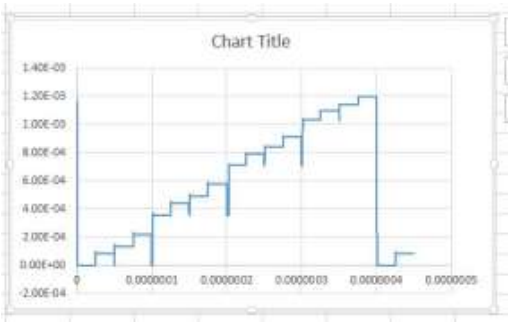


Figure 4.6 Output of segmented DAC using Differential switches (LSBs are Binary and MSBs are Unary sources)

4.5 COMPARISION OF PROPOSED WORK WITH LITERATURE.

Based on literature survey, it was decided to design highly linear DAC which consumes low power and offers high speed of conversion as the major focus was given to biomedical applications. To observe the linearity of DAC, ideal and practical DAC responses in terms of hight and width needs to be compared. The comparison between ideal and practical responses of DAC is referred as a Integral and differential non linearity error.

In the proposed work, three types of current steering DAC architectures are designed and simulated. They are 1. Binary weighted 2. Unary 3. Segmented (hybrid structure of binary and unary). The amount of INL and DNL observed depends on the type of architecture used. Secondly, it depends on types of switching device used.

Further, to add merits of binary and unary known as segmented architecture with all possible combinations have been explored to optimize INL and DNL performance this work presents design and implementation of segmented DAC using various switches like NMOS, PMOS, Transmission Gate and differential switch. The concept of segmented offered the advantage in form of reduction in glitches compared to binary weighted DAC.

A binary weighted 4-bit current-mode digital to Analog converter (DAC) Suitable for neural stimulator based artificial retinal prostheses is designed and simulated using 180nm CMOS Process. In this implementation INL, DNL have been calculated using switching devices like PMOS and Transmission Gate. Based on comparison, Transmission gate offers better performance in form of INL and DNL. The measured values of DNL and INL errors are 0.38 LSB and 0.34 LSB respectively. The measured power consumption is 22mW.

The proposed 5-bit segmented current steering DAC is implemented in cadence virtuoso 180 nm technology. It is observed that the Static error in the output current of the DAC mostly depends on type of switch, speed of switching and combination of segmentation. The proposed segmented DAC offers better static performance in form of INL and DNL. The result of DAC shows reduction in glitches which results in improvement in INL and DNL values. The DAC is simulated with supply voltage

of 1.8 V and 200 MHz of the maximum sample rate. The simulated design consumes power of 20mW at sampling rate of 200 MHz. The simulated DNL and INL observed are ±0.36 LSB and ±0.34LSB, respectively.

The novel architecture of segmented current steering DAC for neural simulator is designed and simulated. It is observed that the Static error in the output current of the DAC mostly depends on type of switch, speed of switching and combination of segmentation. The proposed segmented DAC offers better static performance in form of INL and DNL. The result of DAC shows reduction in glitches which results in improvement in INL and DNL values. The proposed DAC offers a desirable performance in form of DNL and INL which is in the range of $\pm$0.5 LSB.

4.6 Design of Segmented CS DAC for Neural Stimulation Application

A multi-phasic neural stimulator using current steering Digital to Analog Converter with low resolution is in great demand to ameliorate symptoms of Parkinson's disease and disorders of consciousness. Here a 5-bit segmented DAC is designed for such applications. In order to simulate the design, a cadence virtuoso tool with 180 nm MOS technology is used. The results are obtained after simulation which offers $\pm$0.34 LSB INL and $\pm$0.36 LSB value for DNL. For the input of 200 MSPS, the power dissipation is about 22 mW when working with 1.8 V of the supply voltage.

The common targets for stimulations of neural tissues lie within the center as well as at the peripheral nervous system (PNS). The CNS, central nervous system, is mainly concerned with the proper functioning of the neurons' population. The stimulation of the same is carried out for probing the said populations. The stimulation also provides sensory feedback to its users utilizing the periprosthetic device. Clinically, to ameliorate symptoms of Parkinson's disease and epilepsy, CNS stimulations are used. Similarly, for the sensory feedback of the prosthetic devices, peripheral nervous system (PNS) stimulations are also useful [1,20]. In recent advancements, such simulations are applied to the treatment of hypertension and inflammatory disorders [2,20]. The block diagram of a neural stimulator that utilizes multiple DACs in a single channel is shown in figure 1. DAC topology selection depends upon various parameters like chip area, amount of power required, and accuracy of performance. Current steering DAC with a Current source array of binary or unary weights and R – 2R ladders are part of a famous topology that is utilized for the design of neurostimulators.

4.7 PROPOSED SEGMENTED APPROACH

The current steering DAC enables high power performance as the current sources transistors those involved in stimulation are required to be switched on. In case of a splitter, the entire circuit draws the current regardless of the selected node. However, in case of splitter the area increases linearly with increase in number of bits, which is not the case in the weighted arrays, where the area increases exponentially with the number of bits. Larger the number of bits in the weighted arrays higher the area required. For DAC having N inputs, M bits have been implemented using unary weighted DAC while (N-M) bits to be implemented using binary weighted. The segmentation scheme and corresponding transistor level representation is as below shown in Figure 4.7 and Figure 4.8.

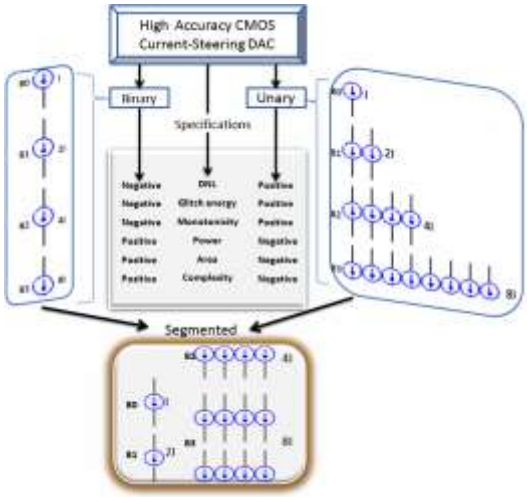


Figure 4.7 Block diagram illustrating Segmentation approach [8]

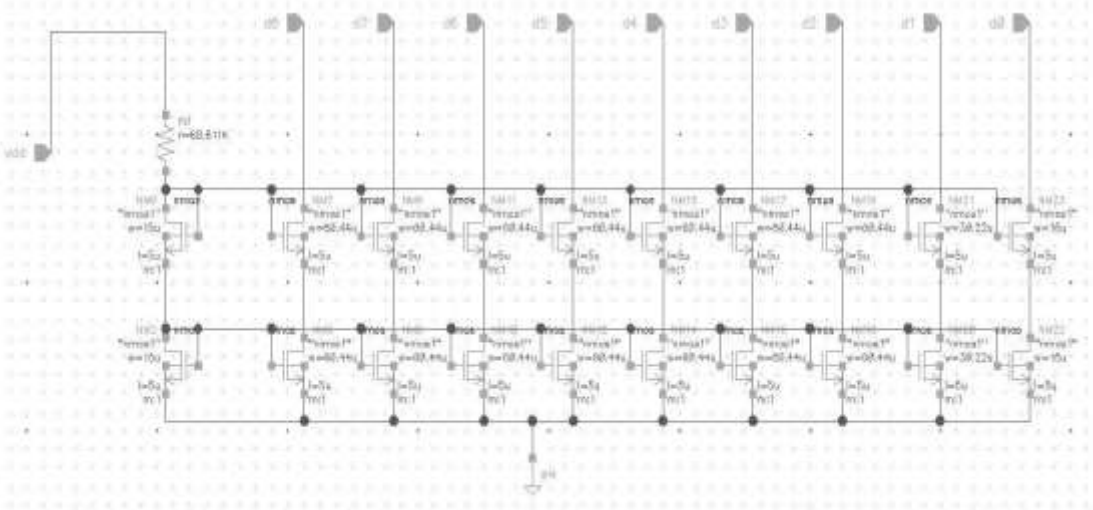


Figure 4.8 Implementation of Segmented DAC using Cadence

A main source of nonlinearity originates because of glitches in the current cell. More no. of transitions results in more no. of changes in the states of switches say on to off or vice versa. In the case of a 5-bit binary-weighted DAC, when input changes from 00111 to 01000, a big glitch is observed because of 4 transitions. Similarly, when the input changes from 01111 to 10000, even a big glitch will be there because of 5 transitions. In the case of unary weighted DAC, there is only a 1-bit transition so there is no glitch but it needs more no. of current sources; for 5-bit unary current steering DAC, 31 current sources having the same value are required. A thermometer code is used to control the switches. Additional hardware is required to convert binary code into thermometer codes. Binary to thermometer code conversion for 3 – bit was shown in Table 2.1.

4.8 Binary to thermometer code representation and Implementation

There are two approaches; in the first approach, MSBs are implemented using unary weighted: for 5- bit DAC, if M=3, the total no. of current sources is 7+2=9 (7 having the same value of current ($4I_o$) while 2 are binary weighted say $2I_o$ & I_o), if M=2, total no. of current sources are 3+3=6 (3 having the same value of current ($8I_o$) while 3 are binary weighted $4I_o$, $2I_o$ & I_o). In the second approach, MSBs are implemented using Binary weighted: for 5- bit DAC, if M=3, the total no. of current sources is 2+7=9 (7 having the same value of current (I_o) while 2 are binary weighted say $16I_o$ & $8I_o$), if M=2, total no. of current sources are 3+3=6 (3 having the same value of current (I_o) while 3 are binary weighted $16I_o$, $8I_o$ & $4I_o$).

4.9 5-Bit Segmented Current steering DAC

The proposed 5-bit segmented current steering DAC is implemented in cadence virtuoso 180 nm technology. The DAC is simulated with a supply voltage of 1.8 V and 200 MHz of the maximum sample rate. The simulated design consumes power of 20mW at a sampling rate of 200 MHz. The simulated DNL and INL observed are ±0.36 LSB and ±0.34LSB, respectively.

Figure 4.9 shows output in form of currency for binary inputs. Major glitches are observed when the input changes from 01111 to 10000.

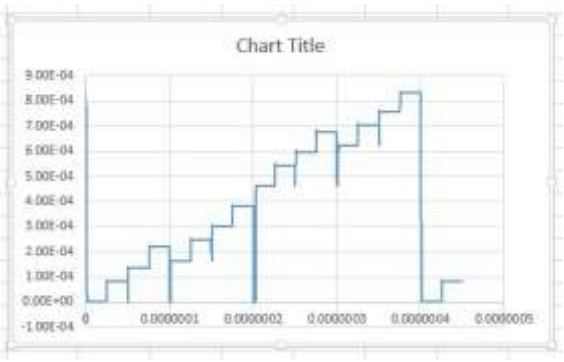


Figure 4.9: Output of binary weighted DAC

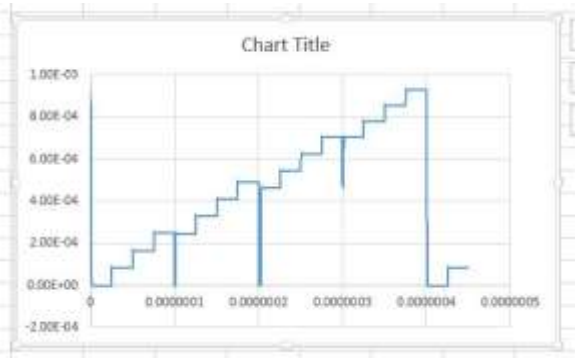


Fig.4.10: Current output of proposed DAC with lower weighted binary bits

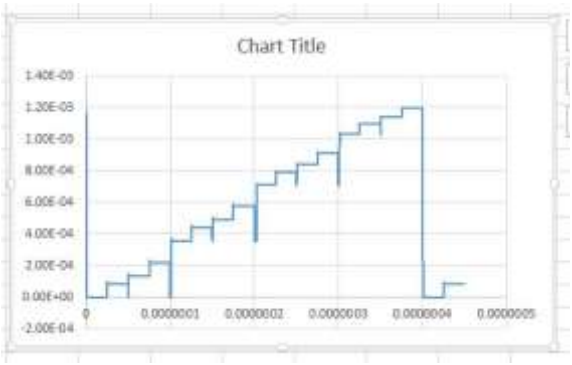


Fig.4.11: Current output of segmented DAC with lower weighted unary bits

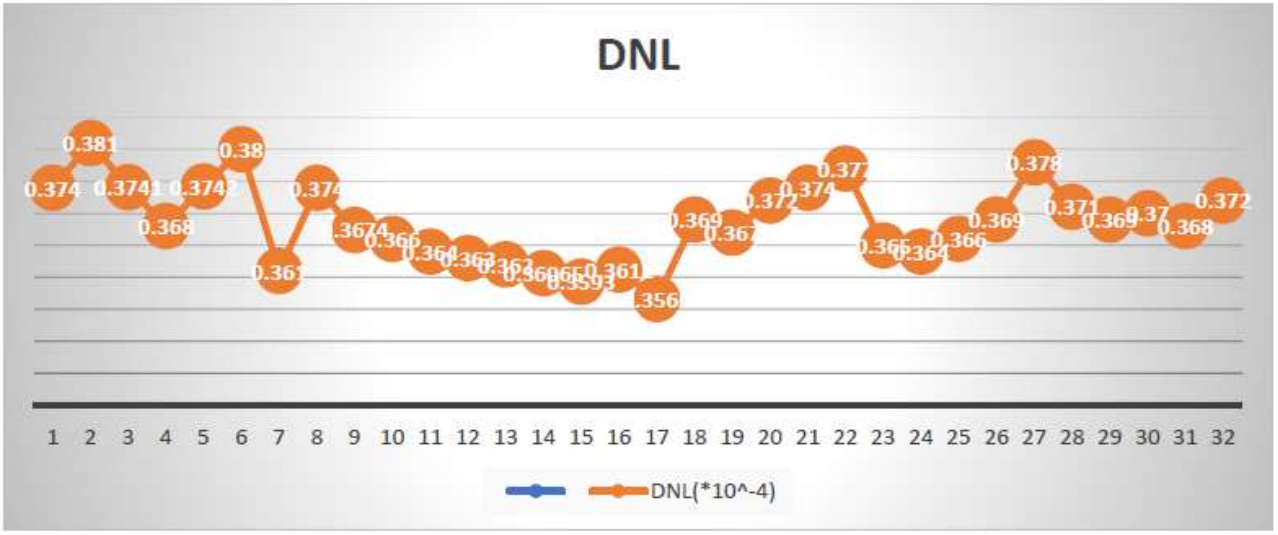


Figure 4.12: DNL graph of proposed segmented DAC

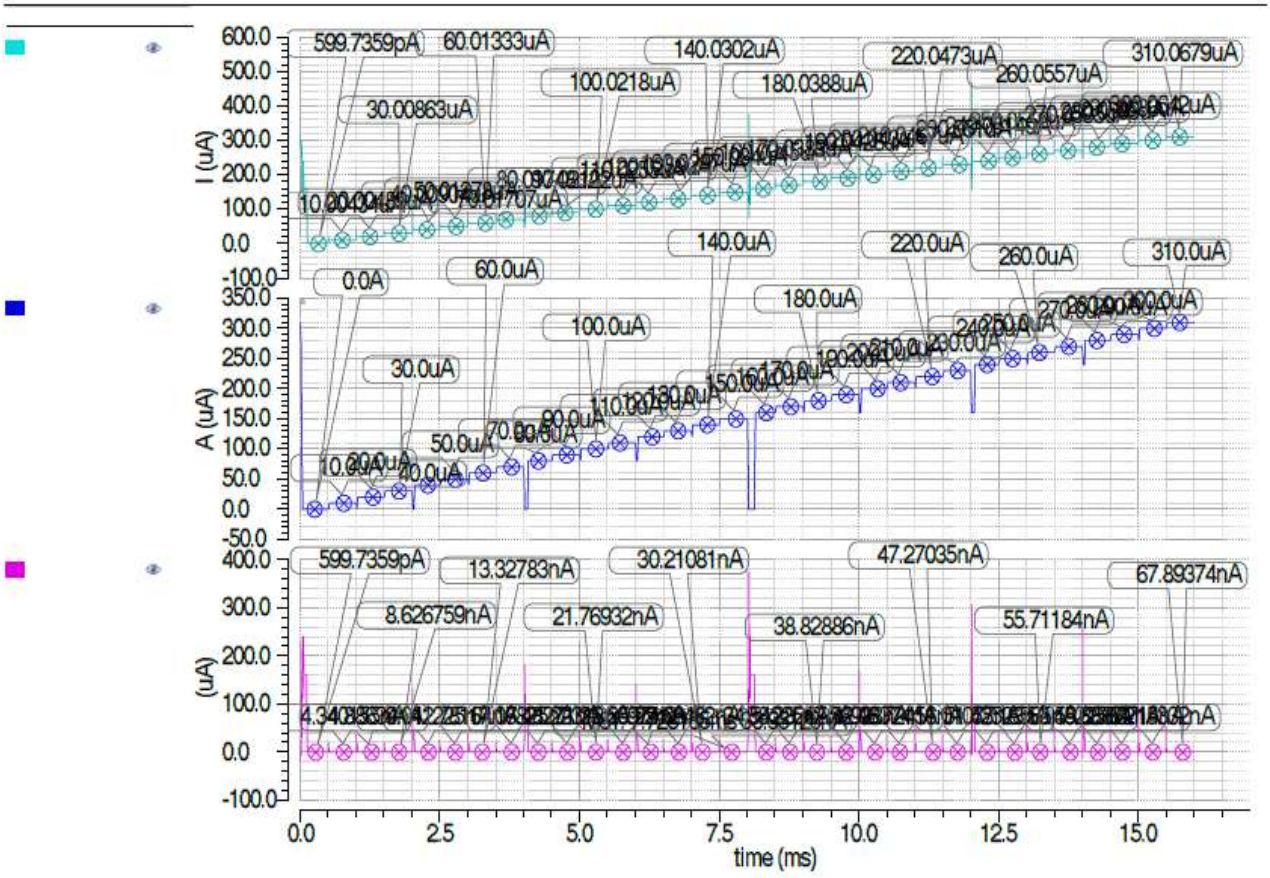


Figure 4.13: Plot of INL for proposed DAC

It has been observed that Glitches have been reduced in the case of segmented DAC. The same is represented in Figure 4.12 and Figure 4.13 in form of INL and DNL.

The novel architecture of the current steering DAC for neural stimulation application is presented. It is observed that the Static error in the output current of the DAC mostly depends on the type of switch, speed of switching, and combination of segmentation. The proposed segmented DAC offers better static performance in form of INL and DNL. The result of DAC shows a reduction in glitches which results in an improvement in INL and DNL values. Total DC power dissipation is 22 mW at 1.8V. The proposed DAC offers a desirable performance in form of DNL and INL which is in the range of $\pm$0.5 LSB.

4.10 DIFFERENTIAL SWITCH

The current-switching structure using NMOS, PMOS or Transmission Gate suffers from dynamic errors. When a switch turns off, the top terminal voltage of its corresponding current source collapses to zero. Thus, the next time that this branch

is enabled, the (nonlinear) capacitance at this terminal must charge up, drawing a significant transient current from the output node. Here at the current source a pair of two NMOS transistors are used and controlled by complementary inputs. Hence at a time one stich remains connected to the current source. There will be less effect in from of change in voltage at the output node so dynamic error is less. The ground bounce is much smaller. Of course, one more advantage of this configuration is that it naturally provides differential outputs.

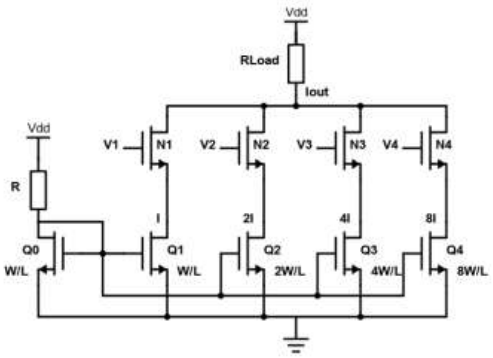


Figure 4.14 Architecture of 4-bit binary weighted DAC using NMOS switches.

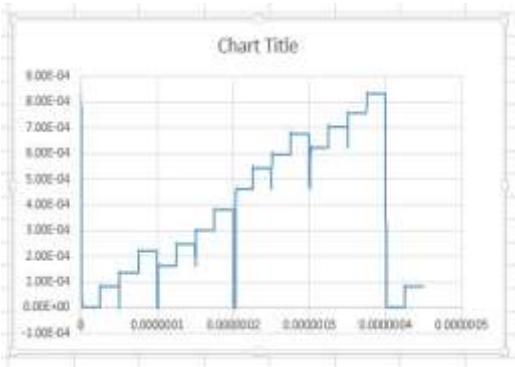


Figure 4.15 Output 4-bit binary weighted DAC using NMOS switches

By keeping current source parts the same as in the case of DAC having NMOS switches, NMOS transistors (N1. N2, N3, and N4) used as switches are replaced with PMOS switches MP1, MP2, MP3, and MP4 as shown in Figure 4.16. Figure 4.17 shows an out of the same DAC in form of current. It does not offer any advantages in form of INL and DNL.

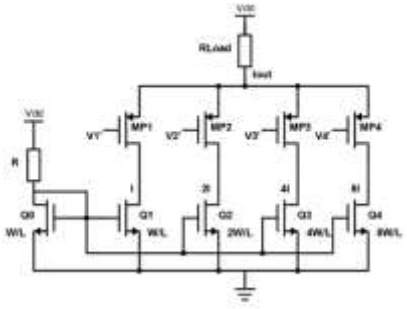


Figure 4.16 Architecture of 4-bit binary-weighted DAC using PMOS switches.

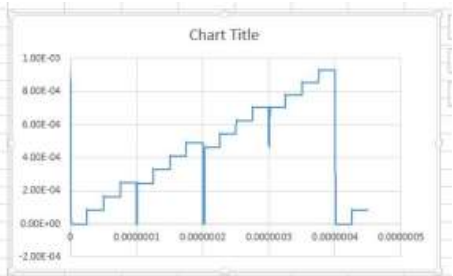


Figure 4.17 Output of 4-bit binary-weighted DAC using PMOS switches

One more architecture is explored by having Transmission Gate (TG) as a switching element having the characteristics of constant resistance. It is made of a parallel

combination of NMOS and PMOS. It consumes relatively more area compared to options of NMOS and PMOS. The 4-bit current steering DAC using TG switches is shown in Figure 4.18 and its simulated current output is shown in Figure 4.19. It has been observed that glitches are there but output increase is relatively more uniform compared to previous both cases.

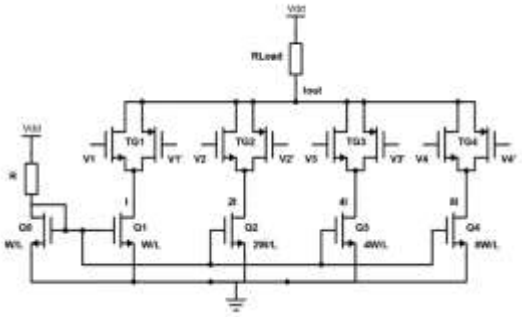


Figure 4.18 Architecture of 4-bit binary weighted DAC using Transmission gate switches.

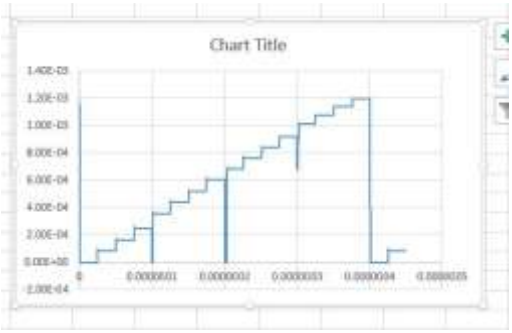


Figure 4.19 Output of 4-bit binary weighted DAC using Transmission Gate switches

Architecture of 4-bit binary weighted Current steering DAC using Differential switches is represented in Figure 10. Current mirror is same as in previous case. Differential switch (each pair consists of two NMOS transistors) DS1, DS2, DS3 and N4 are used as a switching element. Figure 11 shows output in form of current for binary inputs. Major glitches are still observed here but more uniform rise in output is observed dislike in case of NMOS, PMOS and Transmission Gate switch cases.

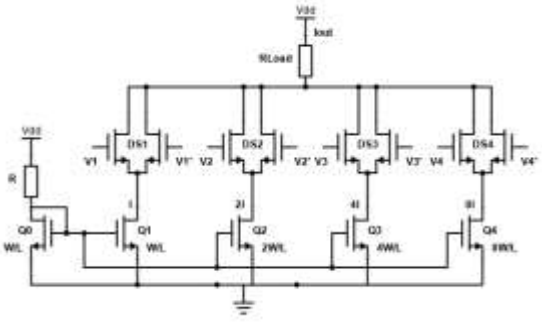


Figure 4.20 Architecture of 4-bit binary-weighted DAC using Differential switches.

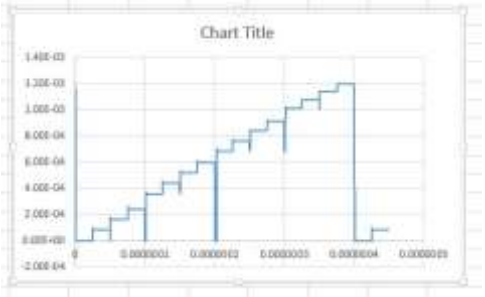


Figure 4.21 Output of 4-bit binary-weighted DAC using Differential switches.

To address the problem of glitches, the concept of Segmented DAC is used here. Here Differential switches have been used There are two options explored (a.) LSBs are implemented using Unary current sources and MSBs are implemented using Binary current sources. The current output of the same is represented in Figure 4.22. (b) LSBs are implemented using Binary current sources and MSBs are implemented using Unary current sources. The current output of the same is represented in Figure 4.23.

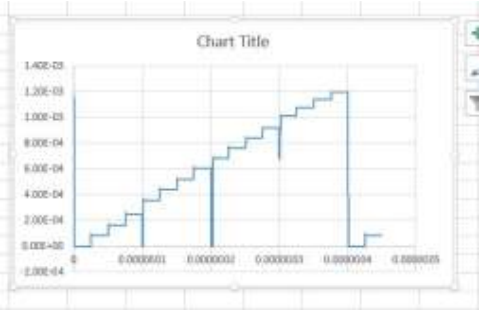


Figure 4.22 Output of segmented DAC using Differential switches (LSBs are Unary and MSBs are Binary sources)

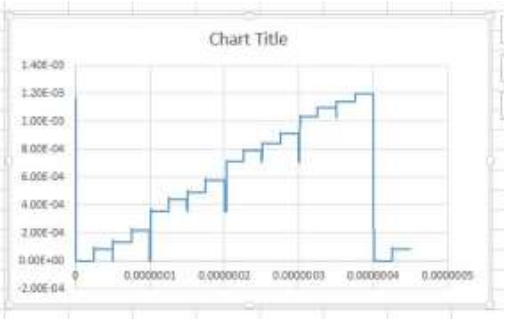


Figure 4.23 Output of segmented DAC using Differential switches (LSBs are Binary and MSBs are Unary sources)

Here it is observed that Differential switches with Segmented DAC offer advantages in form of a reduction in glitches and a uniform rise in output which results in a reduction of non-linearity error (INL and DNL).

4.11 DESIGN FOR IMPROVING NON-LINEARITY ERROR FOR CURRENT STEERING DAC

A compact current-mode Digital-to-Analog converter (DAC) suitable for neural stimulator-based artificial retinal prostheses is represented in this paper. The designed DAC is binarily weighted in 180nm CMOS technology with a 1.8V supply voltage. In this implementation, the authors have calculated for DAC having various types of switches: NMOS, PMOS switch, and Transmission Gate. The implemented DAC uses lower area and power compared to unary architecture due to the absence of digital decoders. The desired value of Integrated nonlinearity (INL) and Differential nonlinearity (DNL) for DAC for Artificial Retinal Prostheses are +0.5LSB. The result obtained in this works for INL and DNL is +0.34LSB and +0.38 LSB respectively with 22mW power dissipation.

Here for 4-bit converter, the 4 weighted current sources are used, those are represented as: I_o, $2I_o$, $4I_o$ and $8I_o$. The main advantage of this architecture is number of current cells required will be reduced hence this architecture is most suitable for higher resolution implementations. The disadvantage with this architecture is it produces higher amount of glitches (unwanted signal) on the contrary the unary architecture offers higher accuracy with greater linearity at the cost of chip area and power overhead.

DAC is a crucial part of the retinal Prostheses. Parameters like non linearity error which includes INL & DNL, power dissipation, conversion time etc. play an important role. Characteristics of switching elements are one of the prominent factors for such parameters.

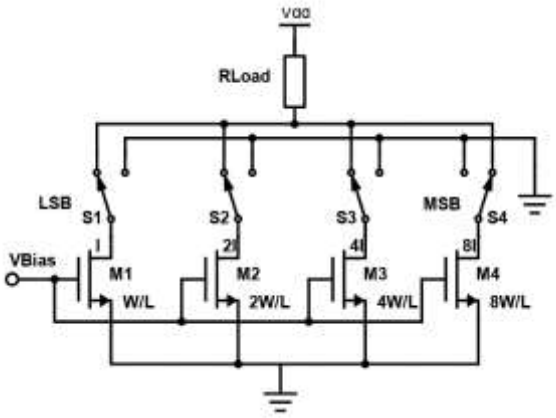


Figure 4.24 4-bit binary weighted current steering DAC

The present work is focused to provide following merits over the existing designs reported in last decade. The design objective is to minimize DNL and INL without too much compromising power consumption and chip area for the application in Bio medical field. After carrying out thorough literature survey, simulations and analysis, following modifications are done to bring novelty in proposed DAC

For the proposed design and simulation, cadence tool is used with 180 nm CMOS technology. The proposed current steering DAC offers desired INL and DNL with rated power consumption.

4.12 SIMULATION RESULTS AND DISCUSSIONS

The proposed 4-bit segmented current steering DAC is implemented using cadence virtuoso in CMOS 180 nm technology. This converter developed and simulated in a 180 nm CMOS technology with supply voltage of 1.8 V. and the maximum sample rate was 200 MHz under simulation. DNL and INL for proposed DAC were observed as ±0.42 LSB and ±0.4LSB, respectively. With the operating frequency of 200 Mhz, simulated power consumption was 20 mW.

Figure 5 to Figure 10 shows the simulated results and output of proposed segmented DAC using various kinds of switches say NMOS, PMOS and transmission gate.

Here in case of PMOS switch, same kind of observations are there as observed in case of NMOS switches. As digital input increase, output should increase. It is not always observed in case of NMOS and PMOS kinds of switches.

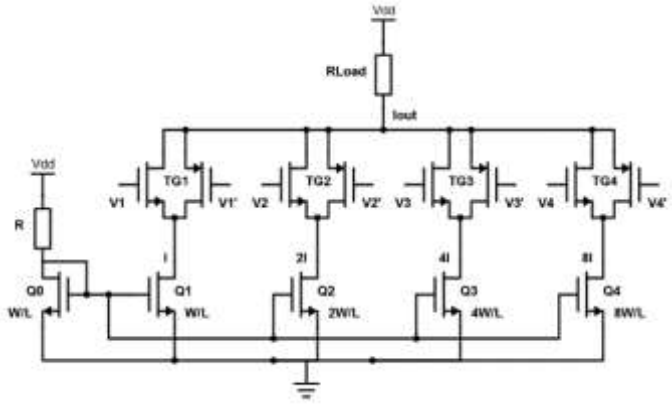


Figure 4.25 Architecture of binary weighted DAC with Transmission Gate switches

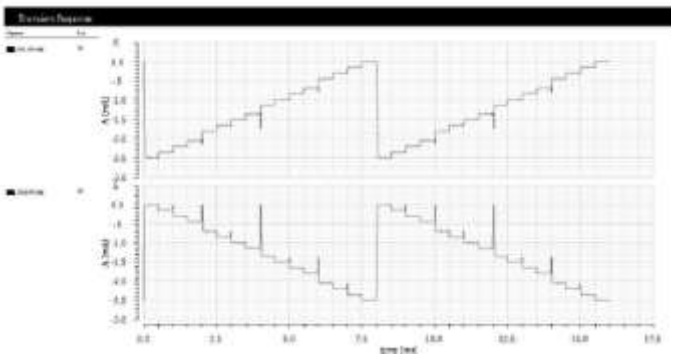


Figure 4.26 Current output of binary weighted DAC with Transmission Gate switches

Transmission gate is one good option as a switch. Architecture having transmission gate offers a big advantage in form of reduction of glitches as well as continuous rise of current as desired which makes lesser value of INL and DNL.

Hence in proposed Current steering DAC, Transmission gate is used a switching element.

4.13 10-bit CURRENT STEERING DAC FOR BIOMEDICAL APPLICATION

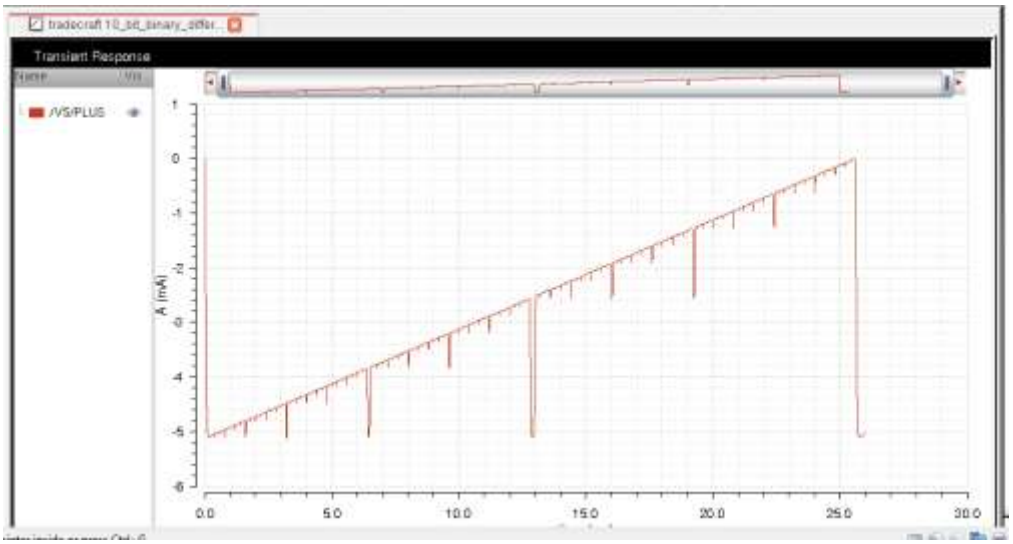


Figure 4.27 Current output of 10-bit binary weighted DAC using differential switch

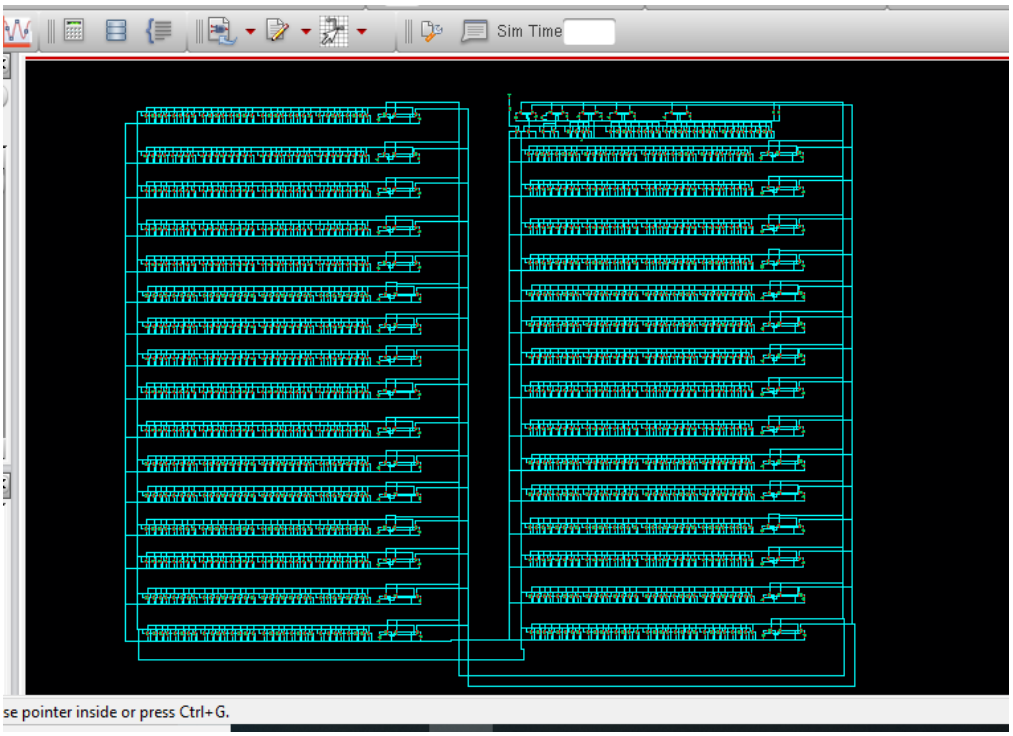


Figure 4.28 Architecture of 10-bit segmented DAC using differential switch for biomedical application

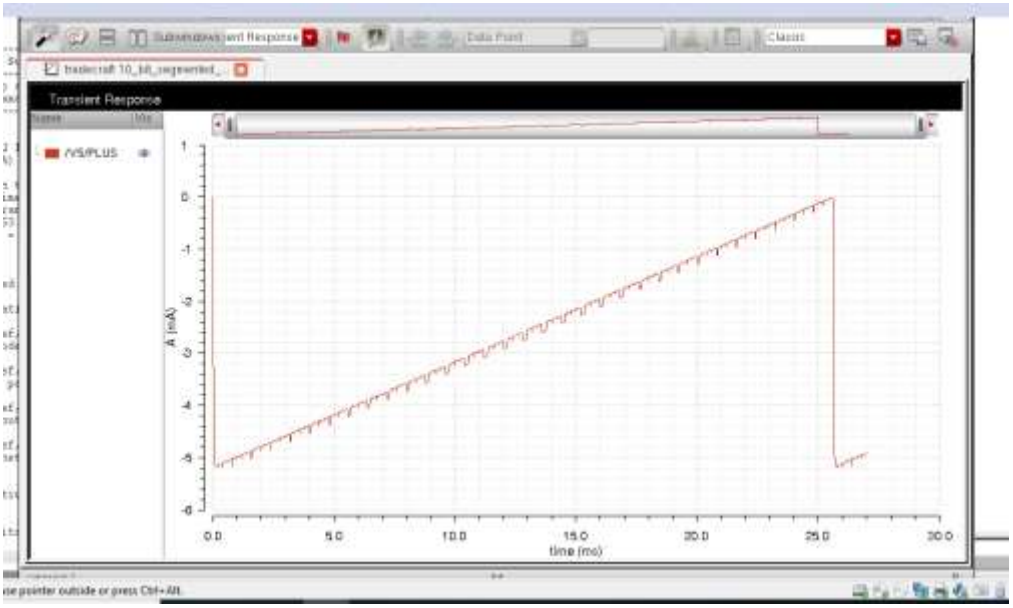


Figure 4.29 Output of 10-bit segmented DAC using differential switch for biomedical application

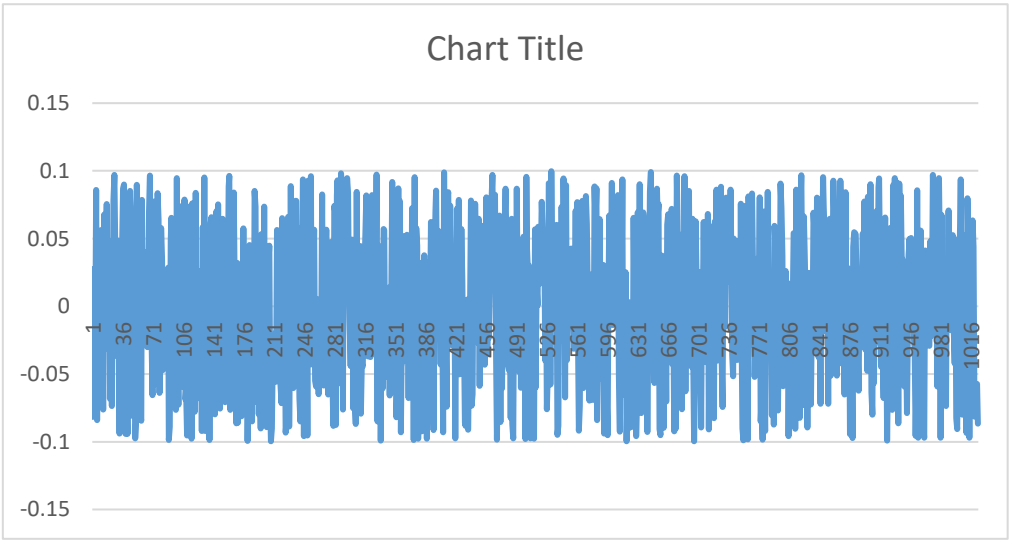


Figure 4.30 DNL graph of 10-bit CS DAC for Biomedical application

Simulation results in form of DNL and INL for proposed 10-bit current steering segmented DAC are represented in Figure 4.30 and Figure 4. 31 respectively.

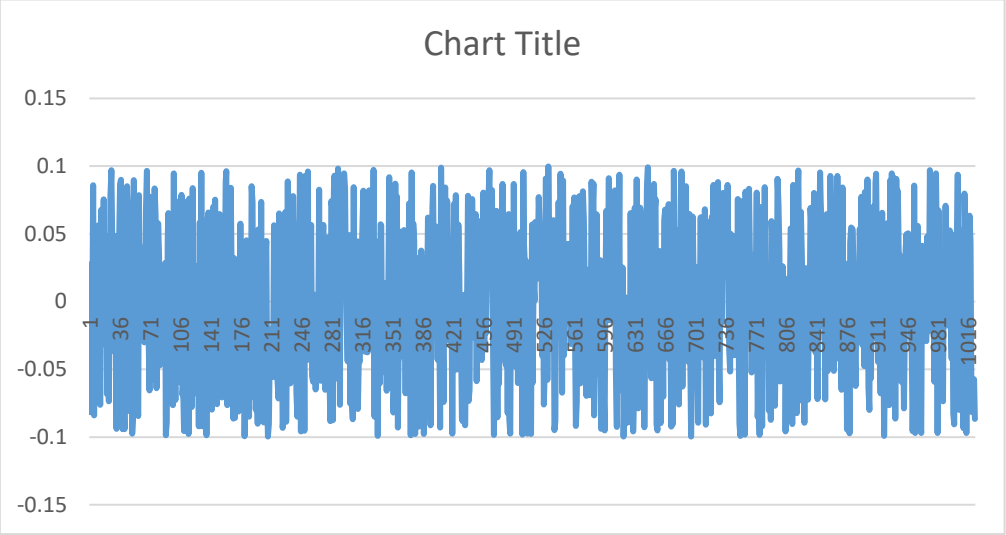


Figure 4.31 INL graph of 10-bit CS DAC for Biomedical application

Result obtained in this work is compared with state of arts in form of table based on various parameters are represented in Table 4.2.

Table 4.2 Comparison of result with state of Arts

Parameters	**[7]**	**[2]**	**[5]**	**[4]**	**[1]**	**[3]**	**This work**	
Month and Year of publication	Jan 2016	Feb 2016	Mar 2016	Jan 2017	Oct 2017	Aug 2014	2020	
Resolution (bits)	10	6	8	4	6	10	10	10
Technology (nm)	65	90	65	65	500	180	180	180
Supply voltage (V)	3.3 V	1.2/1 V	1	1.2	3	1.5	1.8	1.8
Power (mW)	76	17.7	0.54	30	3.1	**0.0016**	**0.0028**	**0.0038**
Area (mm^2)	0.135	0.038	0.01	-	-	-	-	-
DNL (LSB)	0.4	0.06	0.47	0.12	0.17	**0.92**	**0.24**	**0.12**
INL (LSB)	0.55	0.09	1.58	0.16	0.33	**1.23**	**0.36**	**0.152**
Frequency (Mhz)	122	-	1	-	-	0.0395	0.04	0.04
Conversion rate (MS/s)	500	3100	-	10000	-	0.110	0.12	0.12
Segmentation	Yes	No	No	No	Yes	No	No	Yes

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PUBLICATIONS RELATED TO THE THESIS WORK

Jayesh Patel, Amisha Naik. “Comparative Study of Current steering DAC based on Implementation using various types of Switches” International Journal of Advanced Research in Engineering and Technology, 11.4 (2020):452-460.

Jayesh Patel, Amisha Naik. “A Low Voltage High Speed Segmented Current Steering DAC for Neural Stimulation Application”. International Journal of Recent Technology and Engineering, 2020.

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Jayesh Patel, Amisha Naik. “Design and Implementation of 4-bit Binary weighted Current Steering DAC”. International Journal of Electrical and Computer Engineering, Vol. 10, No. 6, (2020), pp. 5642-5649.

Design for Non-Linearity Improvement of Current Steering Digital to Analog Convertor for Biomedical Applications

A Thesis Submitted to
Nirma University
In Partial Fulfilment of the Requirements for
The Degree of
Doctor of Philosophy
in
Technology & Engineering

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December, 2022

CONCLUSION

In this research, the main objective was to explore the design of current steering DAC for biomedical applications with improved Nonlinearity error i.e integral and differential nonlinear error.

The salient points related to the proposed design are summarized below:

Design and analysis of a Current steering DAC were carried out using various types of switches i.e NMOS, PMOS, Transmission Gate, and Differential switches. The concept of segmented DAC was used which offers an advantage over Binary weighted DAC and Unary weighted DAC looking at the complexity and Nonlinearity.

Various combinations were explored for design goals area power and INL DNL errors which are mentioned below.

- 4bit binary (USB side) + 6-bit unary (LSB side),
- 5bit binary (USB side) + 5-bit unary (LSB side),
- 6bit binary (USB s4-bit+ 4-bit unary (LSB side),
- 4bit binary (LSB side) + 6-bit unary (USB side),
- 5bit binary (LSB side) + 5-bit unary (USB side) and
- 6bit binary (LSB side) + 4-bit unary (USB side).

From the designs of different switches and combinations of segmented DAC, the following general conclusions are drawn for the proposed 10-bit current steering DAC for biomedical applications:

- Implementation of 10 –bit current steering DAC with differential switch with segmented approach offered DNL and INL are 0.12 and 0.152 LSB with a power consumption of 3.8uW
- DNL is reduced by a factor of **7.58**
- INL is reduced by a factor of **8.09**
- Power dissipation is increased by a factor of **2.375**

FUTURE SCOPE OF WORK

The Segmented current steering DAC is currently in high demand for biomedical ASIC implementations due to high-speed operation, simplicity of design, reasonable INL, and DNL performance.

The reported work can be explored in the following directions.

- The INL and DNL errors can be further optimized by improving the matching of current mirrors using matching techniques already reported in the literature.
- Newer devices like FinFETs-based switches can be used to improve the errors.
- Different current mirror topologies like cascode, Wilson, or regulated cascode can be used in place of the simple current mirror to improve the performance of DAC.
- It can be designed with Higher resolution with power reduction using some power reduction techniques.
- Based on the requirement of application, It can be explored to design for other fields as well.