Three-Level Inverter Scheme with Common Mode Voltage Elimination and DC-Link Capacitor Voltage Balancing for an Open End Winding Induction Motor Drive

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***Abstract*- A DC Link capacitor voltage balancing scheme for an three-level inverter with open end winding induction motor drive is proposed in this paper. The multiplicity of the switching combinations of the inverter voltage locations is best exploited to arrive at the capacitor balancing criterion. All the inverter vector locations, which has unbalancing effect on the capacitor voltages, exhibits greater multiplicity than the conventional neutral point clamped three-level inverter. These switching combinations can be used properly to balance the capacitor voltages. The effect of various switching combinations on the capacitor voltages is established and then a closed loop hysteresis controller based capacitor voltage balancing scheme is proposed. The performance of the proposed scheme for various operating conditions is demonstrated through simulation and experimental results. A 1.5 kW induction motor with open end windings is used for experimental verification of the proposed scheme.**

I. INTRODUCTION

Since introduced in 1981 [1], the multi-level inverters have been established themselves as the industry choice for the medium voltage, high power variable speed applications. Out of the various multi-level inverter configurations proposed in the literature, the conventional three-level neutral point clamped topology is the most favored one. The three-level neutral point clamped inverters require two separate DC link power supplies of half the voltage ratings as compared to the two-level inverters. The better solution is to use the single power supply of the same voltage rating along with a pair of capacitors to split the DC Link. The load current drawn from the mid point of the DC rail leads to the charging/discharging of the DC link capacitors [2]. The phase voltage generated across the machine phase with unbalanced DC links contains even harmonics, which may cause damaging effects to the machine because of current harmonics, torque pulsations and increased machine losses [2]. During the unbalanced load conditions or dynamic conditions, the neutral point voltage may deviate from the normal balanced state and in the worst case, one capacitor may get fully charged to full DC link voltage. This doubles the stress on the switching devices (which are rated only for half the DC Link Voltage), and it may result in permanent damage to the switching device. The neutral-point voltage-balancing problem is discussed at length in the literature [2]-[9]. Different control schemes are presented and their operation has been demonstrated during steady state as well as dynamic conditions of the load (Induction Motor) connected to the inverter. The dependence of the neural point voltage variation on the system parameters like load currents, load power factor, DC Link capacitors etc., have been extensively studied for three-level NPC inverter [3] - [6]. The effect of the zero sequence voltage on the neutral point variation is established in [3] and the theoretical minimum capacity of the capacitors required for neutral point balancing is also studied [3]. The neutral point balancing schemes, for the three-level neutral point clamped inverter, are based on effective use of the redundant switching states of the inverter voltage vectors. The redundant switching states are used alternately such that the neutral point voltage unbalance caused by the first switching state combination is compensated by another state, thus, bringing the total unbalance, in one switching cycle, to zero [2] [5] [8]. But only few inverter voltage vectors have redundancy of the switching combinations and thus limits the neutral point balancing capability of the three-level NPC inverter [3][5] [6]. A neutral point voltage control scheme is presented in [5], where a DC offset voltage is added to the modulating signals before comparing with the carriers. Adding the DC offset in such manner does not change the effective voltage across the machine phases, but results in the change in the average current drawn from middle rail of the DC Link. A control strategy is proposed to maintain this average current to minimum, which results in minimum deviation in the neutral point potential [5]. The neutral point balancing scheme is presented in [9], where the time durations of the various inverter vectors in the switching interval is determined such that the total error in the capacitor voltages is less than the threshold limit. The time intervals for initial and end inverter switching vectors are thus not equal and the PWM implemented in this way is no longer a SVPWM.

This paper presents a DC Link capacitor voltage balancing scheme for a three–level inverter configuration with common mode voltage elimination for open end winding induction motor. An open end winding induction motor is fed from two three-level inverters from either side [11], where each three-level inverter is a cascaded combination of two two-level inverters [12]. The resultant voltage space vectors of the inverter configuration are equivalent to a conventional five-level inverter [11]. The individual two-level inverters are fed from separate DC links, isolated from each other, to avoid the flow of common mode currents in the phase windings [11]. When only those inverter voltage vectors, which do not generate common mode voltage across motor phase, are used for inverter switching, the resultant voltage vectors are similar to a three-level inverter [14]. The DC links of each three-level inverter can be then connected together, and it requires only two isolated power supplies. The proposed inverter generates zero common mode voltage in the machine phase voltage as well as inverter pole voltages [14]. The inverter voltage vectors of the proposed three-level inverter drive have more redundant switching combinations as compared to the NPC three-level inverter. There exist redundant switching

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combinations for the inverter voltage vectors which have unbalancing effect on the capacitor voltages. These switching combinations have exactly opposite effects on the capacitor voltages and thus alternate use of these switching combinations can be used to maintain the capacitor voltages. The redundancy offered by the inverter voltage vectors makes the proposed three-level inverter ideal for DC Link capacitor voltage balancing. Thus the two power supplies can be replaced by a single power supply, along with two capacitors to split the DC Link and the DC link can be balanced by a voltage balancing scheme based on the alternate switching of the redundant states of the inverter voltage vectors. The dependence of the DC link capacitor voltage deviations on the motor current and inverter switching states is established for the proposed three-level inverter drive. The relationship between the DC link capacitor voltage deviations, the motor phase current and inverter switching states is established for the proposed three-level inverter drive. The simplicity of DC link capacitor voltage balancing is demonstrated with open loop as well as closed loop hysteresis controllers. The simulation studies are carried out and response of the controller is demonstrated for steady state as well as for dynamic state. A hysteresis controller based closed loop voltage-balancing scheme is presented, which can balance the capacitor voltage under various operating conditions. A simple three-level inverter PWM algorithm is used for PWM generation, which is based only on the instantaneous amplitudes of reference phase voltages [13]. The experimental studies are carried out on a laboratory prototype with 1.5 kW open-end windings induction motor drive and the experimental results are presented.

II. THE THREE-LEVEL INVERTER SCHEME WITH COMMON – MODE VOLTAGE ELIMINATION FOR AN OPEN-END WINDING INDUCTION MOTOR

Fig. 1 shows the proposed three-level inverter configuration. An induction motor with open-end windings is fed from both ends using two three-level inverters. The individual three-level inverters are formed by cascading two two-level inverters [14]. The combinations of switching states from the three-level inverters, with zero common mode voltage, for the proposed drive are shown in Fig. 2 [14]. The first switching state in each pair corresponds to switching state of inverter-A, while second one corresponds to switching state of inverter-B (Fig 2). Thus appropriate selection of switching states of individual three-level inverters, results into the common mode voltage totally eliminated from the inverter pole voltages, and the phase windings of the induction motor.

III. ANALYSIS OF DC-LINK CAPACITOR VOLTAGE UNBALANCE FOR PROPOSED THREE-LEVEL INVERTER CONFIGURATION

As long as the motor current is supplied from top or bottom rail of the DC link, the capacitor voltage remains balanced. Any tendency of the loads to draw the current through the mid-point of DC link will result in the unbalance of the capacitor voltage. The voltage across the bottom and top DC link capacitors is referred as v_{C1} and v_{C2}. Under the balanced condition, $v_{C1} = v_{C2} = V_{DC}/2$

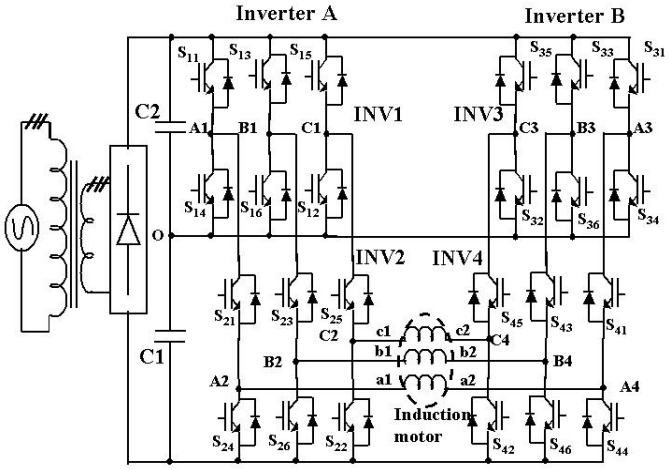


Fig. 1: Schematic of the proposed three-level inverter fed from single converter.

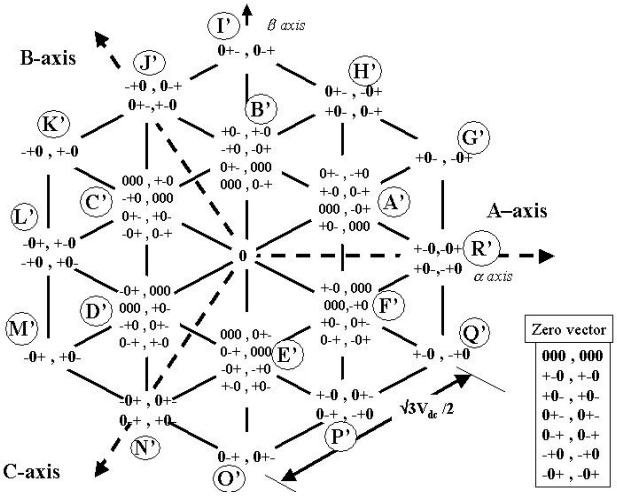


Fig. 2: The switching combinations for three-level inverter with common mode voltage elimination

Each leg of individual three-level inverter can modeled as a three pole switch, connected to negative, mid-point and positive bus of the DC link respectively, as shown in Fig. 3a. The equivalent switch can assume values equal to 1, 2 or 3, which means that the pole of the switch is connected to bottom, middle or top DC link respectively. The motor currents are denoted as i_a, i_b and i_c while the total current drawn by the inverter from the bottom, middle and top rails of the DC link are denoted as i_1, i_2 and i_3 respectively. The Inverter-A input currents are referred as i_{1A}, i_{2A}, i_{3A} and inverter-B input currents are referred as i_{1B}, i_{2B}, i_{3B}, as shown in Fig. 3b. The inverter pole voltage with respect to negative DC rail, for inverter-A, can be expressed in terms of capacitor voltages as

$$
\begin{aligned}
v_{a1}(S_a) &= \delta(S_a-1)v_{C1} + \delta(S_a-2)(v_{C1}+v_{C2}) \\
v_{b1}(S_b) &= \delta(S_b-1)v_{C1} + \delta(S_b-2)(V_{C1}+v_{C2}) \\
v_{c1}(S_c) &= \delta(S_c-1)v_{C1} + \delta(S_c-2)(v_{C1}+v_{C2})
\end{aligned} \tag{1}
$$

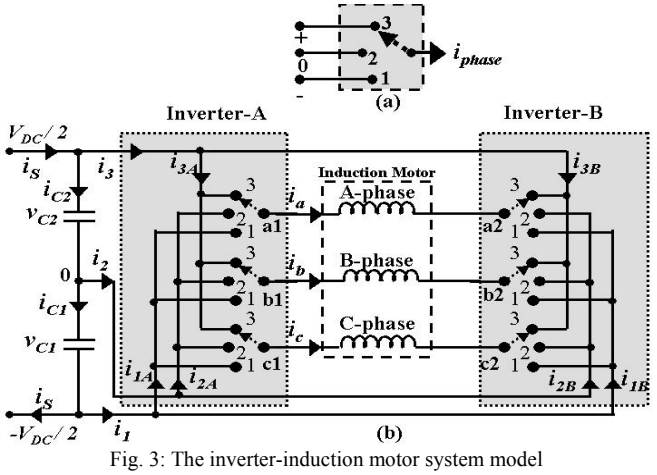


Fig. 3: The inverter-induction motor system model

Similarly expression can be written for pole voltages of inverter-B,

$$
\begin{aligned}
v_{a2}(S'_a) &= \delta(S'_a-1)v_{C1} + \delta(S'_a-2)(v_{C1}+v_{C2}) \\
v_{b2}(S'_b) &= \delta(S'_b-1)v_{C1} + \delta(S'_b-2)(v_{C1}+v_{C2}) \\
v_{c2}(S'_c) &= \delta(S'_c-1)v_{C1} + \delta(S'_c-2)(v_{C1}+v_{C2})
\end{aligned} \tag{2}
$$

where v_{a1}, v_{b1}, v_{c1} and v_{a2}, v_{b2}, v_{c2} are the pole voltages of inverter-A and inverter-B respectively with respect to lower DC link bus. In (1) and (2), $\delta(.)$ is the Dirac-Delta function and $S_a, S_b, S_c, S'_a, S'_b, S'_c$ are the switching functions defined for poles of inverter-A and inverter-B respectively and can take any value from 1, 2 or 3 [10]. The currents drawn from the DC Link nodes can be represented in terms of the motor currents as shown in (3) for inverter-A and in (4) for inverter-B respectively.

$$
\begin{bmatrix} i_{1A} \\ i_{2A} \\ i_{3A} \end{bmatrix} = \begin{bmatrix} \delta(S_a-1) & \delta(S_b-1) & \delta(S_c-1) \\ \delta(S_a-2) & \delta(S_b-2) & \delta(S_c-2) \\ \delta(S_a-3) & \delta(S_b-3) & \delta(S_c-3) \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3}
$$

$$
\begin{bmatrix} i_{1B} \\ i_{2B} \\ i_{3B} \end{bmatrix} = -\begin{bmatrix} \delta(S'_a-1) & \delta(S'_b-1) & \delta(S'_c-1) \\ \delta(S'_a-2) & \delta(S'_b-2) & \delta(S'_c-2) \\ \delta(S'_a-3) & \delta(S'_b-3) & \delta(S'_c-3) \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{4}
$$

Now the total current drawn from the DC link is the sum of the two inverter currents. Therefore,

$$
\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} \delta(S_a-1) & \delta(S_b-1) & \delta(S_c-1) \\ \delta(S_a-2) & \delta(S_b-2) & \delta(S_c-2) \\ \delta(S_a-3) & \delta(S_b-3) & \delta(S_c-3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} \delta(S'_a-1) & \delta(S'_b-1) & \delta(S'_c-1) \\ \delta(S'_a-2) & \delta(S'_b-2) & \delta(S'_c-2) \\ \delta(S'_a-3) & \delta(S'_b-3) & \delta(S'_c-3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{5}
$$

For a three wire load,

$$
i_a + i_b + i_c = 0 \tag{6}
$$

$$
\text{Similarly, } i_1 + i_2 + i_3 = 0 \tag{7}
$$

Thus substituting $i_c = -(i_a + i_b)$ and removing the dependent variable i_3, (5) gets reduced to

$$
\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} [\delta(S_a-1)-\delta(S_c-1)]-[\delta(S'_a-1)-\delta(S'_c-1)] & [\delta(S_b-1)-\delta(S_c-1)]-[\delta(S'_b-1)-\delta(S'_c-1)] \\ [\delta(S_a-2)-\delta(S_c-2)]-[\delta(S'_a-2)-\delta(S'_c-2)] & [\delta(S_b-2)-\delta(S_c-2)]-[\delta(S'_b-2)-\delta(S'_c-2)] \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{8}
$$

The current flowing through the capacitors is given by

$$
i_{C2} = i_S - i_3 = i_S - (-i_2 - i_1) \quad = i_S + i_2 + i_1 \tag{9}
$$

$$
i_{C1} = i_S + i_1 \tag{10}
$$

$$
\therefore \begin{bmatrix} i_{C2} \\ i_{C1} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_S \\ i_2 \\ i_1 \end{bmatrix} \tag{11}
$$

The currents flowing through capacitors is directly related to the voltage across the devices and the relationship is given by

$$
\begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} = \frac{1}{C}\int \left\{ \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{C2} \\ i_{C1} \end{bmatrix} dt \right\} = \frac{1}{C}\int \left\{ \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_S \\ i_2 \\ i_1 \end{bmatrix} dt \right\} \tag{12}
$$

Let Δv_C be the change in the capacitor voltage,

$$
\Delta v_C = v_{C2} - v_{C1} \tag{13}
$$

Substituting from (12) into(13), results in

$$
\Delta v_C = \frac{1}{C}\int i_2 \, dt \tag{14}
$$

Thus the load current drawn from the middle node of the DC link is responsible for the variation in the capacitor voltages. Whenever switching functions $S_a, S_b, S_c, S'_a, S'_b$ and S'_c assume value equal to 2, there exists a tendency of capacitor voltage unbalancing. The different switching combinations, for the same inverter voltage vector location, have different effect on the capacitor voltages. This effect of the various switching combinations on the capacitor voltages is discussed in the next section.

IV. SPACE VECTOR COMBINATIONS AND THEIR EFFECT ON DC LINK CAPACITOR VOLTAGES

The inverter voltage vector locations are divided into four main groups (Fig. 2) [2]. The central voltage location being referred as *zero voltage vector* (ZV), the voltage vector locations at the periphery of inner hexagon are referred as *small voltage vectors* (SV), the intermediate voltage vectors on outer periphery are referred as m*iddle voltage vectors* (MV), while the largest voltage vectors on outer periphery are referred as l*arge voltage vectors* (LV). The s*mall voltage vectors* are again classified in to three sub-groups (Fig. 4). The sm*all voltage vectors* combinations, in which each capacitor has one winding connected across it, are referred as

n*ormal small voltage vector* (NSV). The s*mall voltage vectors* combinations, in which two windings are connected across the top capacitor C2, are referred as u*pper small voltage vectors* (USV). The s*mall voltage vectors* combinations, in which any two out of three phase windings are connected across bottom DC link capacitor C1 are referred as l*ower small voltage vectors* (LSV) (Fig. 4).

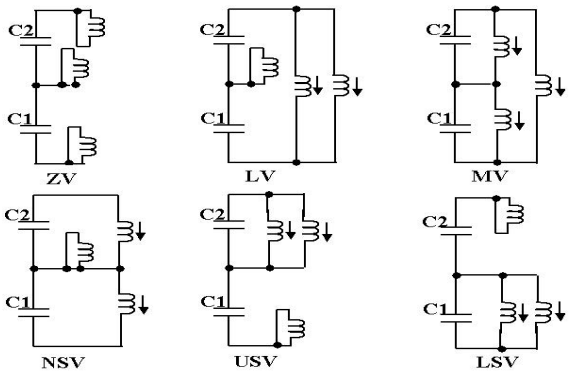


Fig. 4: The phase winding connections to the DC Link capacitors for various vector groups

Each voltage vector combination has a charging/discharging effect on the DC link capacitors C1 and C2 as summarized in Table 1.

TABLE 1: EFFECT OF DIFFERENT VECTOR GROUPS ON CAPACITOR VOLTAGES

Inverter voltage Vector Group	Capacitor C1	Capacitor C2
ZV	No effect	No effect
NSV	Less charging or discharging effect	Less charging or discharging effect
USV	Discharging	Charging
LSV	Charging	Discharging
MV	Less charging or discharging effect	Less charging or discharging effect
LV	No effect	No effect

The inverter vector belonging to USV and LSV groups have large effect on the DC link capacitor voltage balance as the current drawn from the middle node of the DC link is significant. The inverter voltage vectors belonging to USV group have charging effect on bottom DC link capacitor-C1 and discharging effect of top DC Link capacitor. On the contrary, inverter voltage vectors belonging to LSV group have charging effect on top DC link capacitor-C2 and discharging effect of bottom DC link capacitor-C1. Comparatively, when the NSV vectors are used for inverter switching, only the difference between the current, drawn by the phase connected to top capacitor and the current drawn by the phase connected to bottom capacitor, will be drawn from middle node of the DC Link. Thus NSV vectors will have less effect on the capacitor voltage balance as compared to USV and LSV vectors. Each *middle voltage vector* locations (Fig. 2) have two different combinations of three-level inverter voltage vectors (Fig. 2). There exists a similarity between the *middle voltage vectors* (MV) and *normal small voltage vectors* (NSV). In both, one phase winding is connected across the each DC link capacitor. While both differ in the way, the third winding is connected to the DC Link capacitors. In *middle voltage vectors* (MV) the third winding is directly connected across the DC link while in *normal small voltage vectors* (NSV) the third winding is short circuited at mid-point of DC link and thus does not have any effect on the capacitor voltages. The *middle voltage vectors* (MV) have same effect as the inverter vectors belonging to *normal small voltage vectors* (NSV) group. The *large voltage vector* group is characterized by connection of any two phase winding across the DC link while the third winding is short circuited at DC link mid-point. As the phase windings are directly connected across the DC link, this inverter voltage vectors belonging to this group has no effect on the capacitor voltages.

V. DC LINK CAPACITOR VOLTAGE BALANCING SCHEME

The inverter voltage vectors belonging to ZV, NSV, MV and LV can be used effectively to maintain the voltage balance across the DC Link capacitors. The input to the voltage-balancing scheme can be either the difference in the capacitor voltages, Δv_C or the load current drawn from middle node, i_2 as the voltage unbalance can be determined from the i_2, given by (14). Thus, a single front-end rectifier can be used, with two capacitors for splitting the DC link. The power schematic of the overall system is shown in Fig. 1.

A. Open loop DC Link capacitor balancing scheme

Each inverter vector locations from groups NSV and MV have two switching combinations. The basic difference in each of these two combinations is that, the phase winding which is connected across top capacitor in one switching combination, gets connected across bottom capacitor, for the other switching combination (Fig. 5).

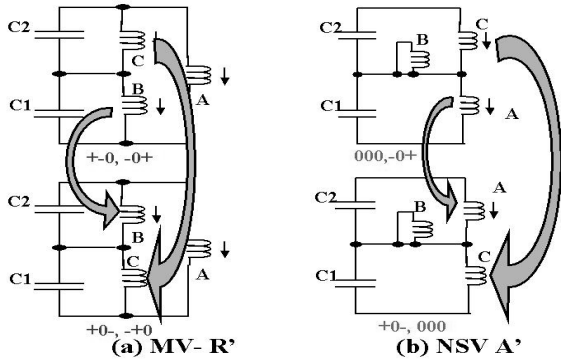


Fig. 5: Phase winding connections to the DC Link capacitor voltages for NSV and MV groups

Thus for the same inverter vector location, if the switching combinations are switched alternately, the capacitor voltage unbalance caused by first switching combination is nullified by the second switching combination. The controller thus switches alternate switching combinations for inverter vectors from NSV and MV group while the inverter vectors from ZV

and LV are switched in the normal way. In this manner, the average voltage unbalance caused in one switching interval is nullified in the next switching interval. Typical switching combinations selected for various inverter vectors, when the reference voltage vector is in sector, formed by inverter voltage vector combinations at A'-G'-R' locations (Fig. 2), are shown in Fig. 6(a) (Table-2).

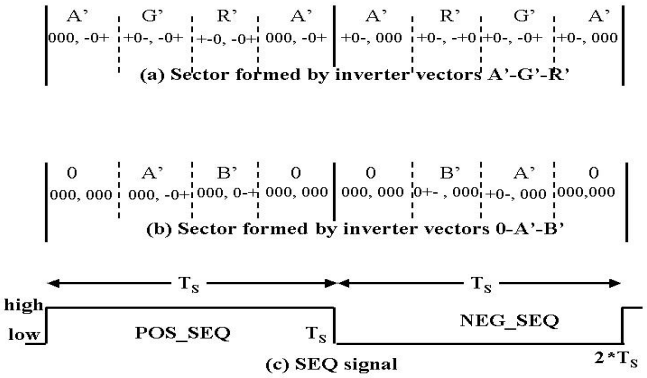


Fig. 6: The sequence of various switching combinations during POS_SEQ and NEG_SEQ

Similarly the inverter switching combinations can be selected for inner sectors also. For example, the inverter switching combinations selected for the sector, formed by inverter voltage vector combinations at 0-A'-B' locations (Fig. 2), are as shown in Fig. 6(b). Fig. 7 shows the simulation results when the test motor is running in steady state. The individual capacitor voltages as well as the total DC Link voltage are shown Fig. 7a while the phase voltage and phase current waveforms are shown in Fig. 7b. The capacitor voltage remains constant, and if the controller disables the voltage-balancing scheme, the capacitor voltages start deviating from their balanced values as shown in Fig. 8a. The phase voltage and phase current under the unbalanced voltage condition is shown in Fig. 8b. The phase voltage waveform gets distorted under the unbalanced capacitor voltages condition.

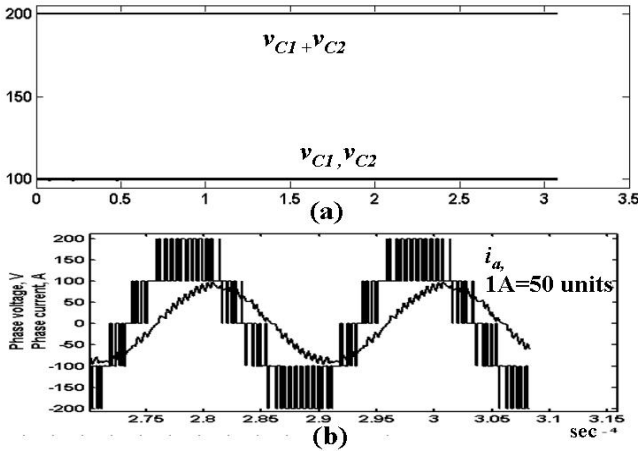


Fig. 7: Operation of the open loop DC Link balancing controller (Simulation results)

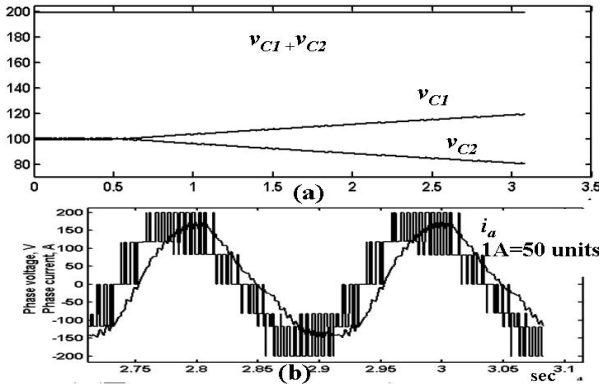


Fig. 8: Deviation in the capacitor voltages when the open loop DC Link balancing controller is turned off (simulation results)

Table 2: CLASSIFICATION OF SWITCHING COMBINATIONS CORRESPONDING TO VARIOUS INVERTER VOLTAGE VECTORS

VECTOR LOCATION	POS_SEQ	NEG_SEQ
0	000, 000	
A'	+0-, 000	000, -0+
B'	0+-, 000	000, 0-+
C'	-+0, 000	000, +-0
D'	-0+, 000	000, +0-
E'	0-+, 000	000, 0+-
F'	+-0, 000	000, -+0
G'	+0-, -0+	
H'	0+-, -0+	+0-, 0-+
I'	0+-, 0-+	
J'	0+-, +-0	-+0, 0-+
K'	-+0, +-0	
L'	-+0, +0-	-0+, +-0
M'	-0+, +0-	
N'	-0+, 0+-	0-+, +0-
O'	0-+, 0+-	
P'	0-+, -+0	+-0, 0+-
Q'	+-0, -+0	
R'	+-0, -0+	+0-, -+0

B. Hysteresis controller based closed loop DC Link voltage balancing scheme

The voltage-balancing scheme implemented in the above manner can balance the DC link capacitor voltage. Still a gradual deviation in the DC link voltages is observed. The possible reasons for this are, use of the asynchronous PWM, the unequal time durations of the MV and NSV inverter vectors in consecutive switching intervals, unbalanced load currents etc. As discussed in the pervious section, the switching combinations belonging to USV and LSV group have characteristic features of charging lower and upper capacitors respectively. The inverter vectors belonging to this group can be effectively used to charge the capacitor. Thus, if the difference in the DC Link voltage Δv_C is monitored, the switching combinations from USV or LSV groups can be selected to bring back the deviation in the capacitor voltage to zero. The overall block schematic of the hysteresis controller based closed loop voltage balancing scheme is shown in Fig. 9. A simple three-level inverter PWM algorithm is used for PWM generation, which is based only on the instantaneous

amplitudes of reference phase voltages [13]. The output of the hysteresis controller along with SEQ signal is used to select the appropriate value of signal 'state', an input signal to the digital logic. Depending upon the status of signal 'state', the inverter switching combinations to be switched for various inverter vector locations (generated by PWM modulator) are selected.

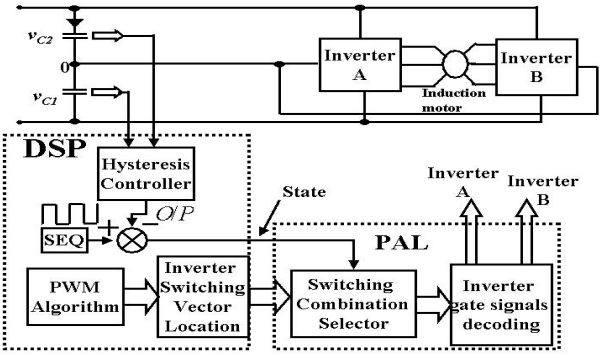


Fig. 9: Hysteresis controller based closed loop DC Link capacitor voltage balancing scheme

The simulation results with the closed loop DC Link capacitor voltage balancing scheme are shown in Fig. 10. Fig. 11 shows the simulation results when the DC link voltage balancing scheme is disabled while motor is operated in motoring mode. The DC link capacitor voltages start diverting from their normal value. The controller is again enabled and the DC link voltages are brought back to their normal values.

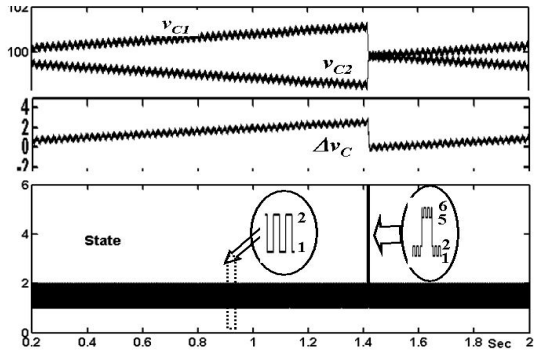


Fig. 10: Operation of closed loop controller for DC link balancing (Simulation results)

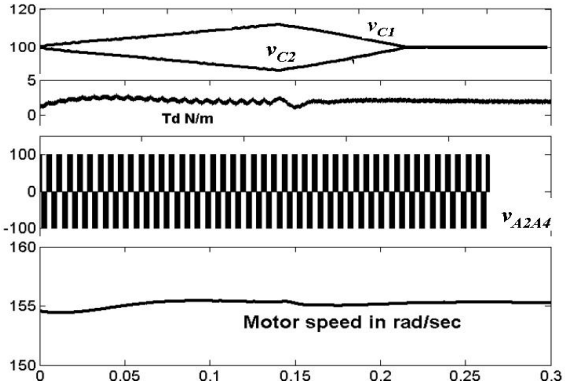


Fig. 11: The deviation in the capacitor voltages when the DC Link voltage-balancing scheme is turned off for a small interval

VI. DC LINK CAPACITOR VOLTAGE BALANCING IN OVER-MODULATION AND 12-STEP MODE

In over-modulation range, the capacitor voltage balance is entirely due to the MV vectors, and the SV vectors are switched for less time duration. Fig. 12 shows the simulation results when the system is driven in the over-modulation region. The extreme case is the 12-step operation, wherein the inverter vectors from the SV group are not switched at all. In 12-step mode, the controller cannot bring back the unbalanced system to steady state, as the SV vectors are not switched at all. Fig. 13 shows the simulation results when the command is increased to drive the system into 12-step mode. The capacitor voltage balancing scheme is disabled, and the capacitor voltages immediately gets disturbed and divert from normal balanced state. The only way to obtain the capacitor voltage balance is to reduce the modulation index momentarily. This allows the switching of the inverter vectors belonging to SV group and the DC link voltage is brought back the balanced state as shown in Fig. 13. The momentary reduction in modulation index can be allowed for small time interval rather than continuing to work with unbalanced DC link voltages.

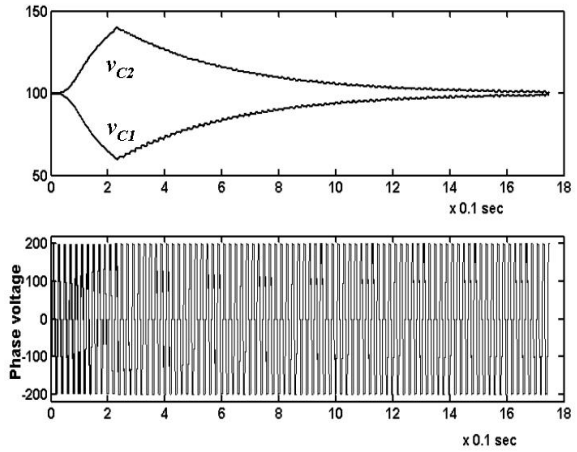


Fig. 12: The operation of the DC Link capacitor voltage balancing scheme in over-modulation

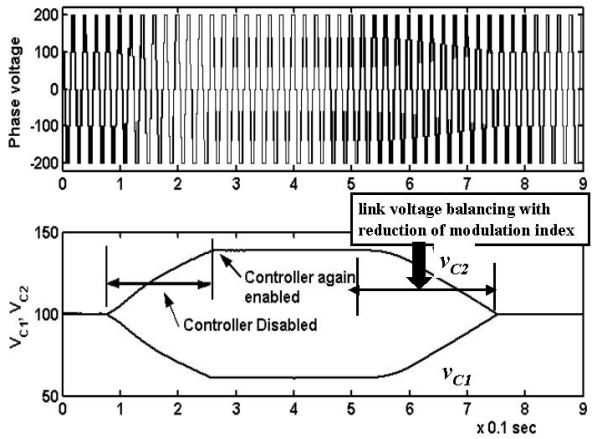
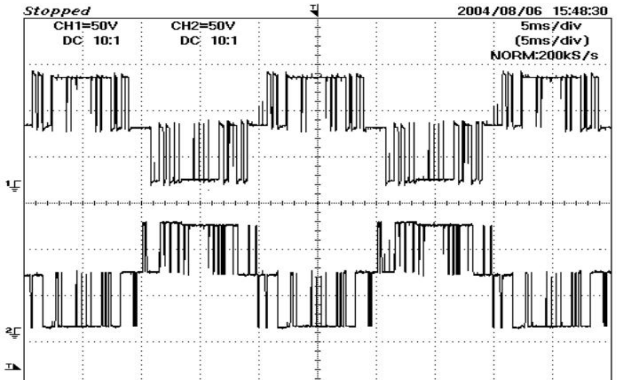


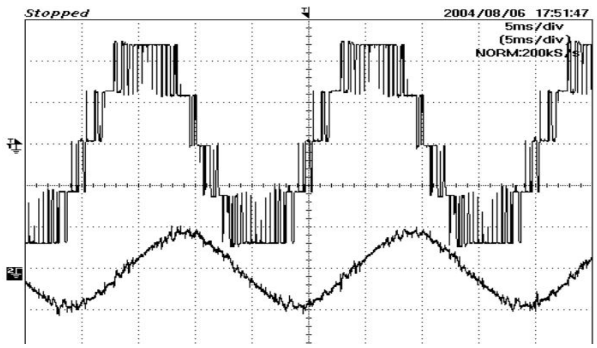
Fig. 13: DC Link balancing with momentary reduction in modulation index

VII. EXPERIMENTAL RESULTS AND DISCUSSION

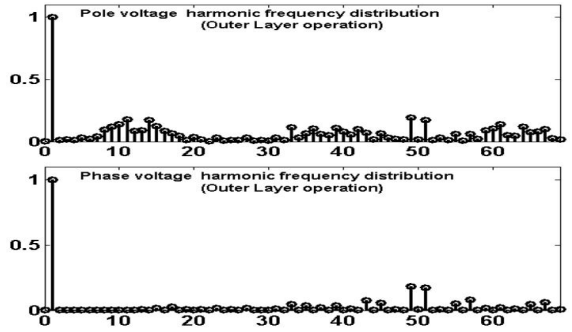
The proposed scheme is tested on a 1.5 KW three-phase induction motor drive with V/f control for different modulation indices covering the entire speed range. The hysteresis controller based closed loop DC link capacitor voltage balancing scheme is implemented using TMS320F24 processor and PALCE22V10 devices. The controller schematic is as shown in Fig. 9. The pole voltage, phase voltage and phase current waveforms for inverter operation in outer layer and in over-modulation is shown in Fig. 14 and Fig. 15, respectively. The pole voltages of the two inverter system are symmetric and are out of phase with each other. Both the pole voltage and the phase voltage show the absence of triplen voltage components. Fig. 15c, shows 5^{th} and 7^{th} harmonics in over-modulation range. The DC link voltage balancing with the induction motor running at constant speed are shown in Fig. 16. The DC link capacitor voltages are well within the voltage band of the hysteresis controller. With the reference voltage space vector in the outer layer (three-level operation), the capacitor voltage-balancing scheme is disabled for small interval (Fig. 17). The capacitor voltages are balanced immediately after the controller is enabled again. Fig. 18 shows the DC link voltages and the phase current during the acceleration of machine from inner layer operation to outer layer operation and again to the operation in over-modulation. The DC Link voltages are maintained within the control band.



(a) Pole voltages: Trace-1: V_{A20}, Trace-2: $V_{A40'}$, Trace 3: (Trace1-Trace2) X axis: 1div=10 ms, Y axis: 1 div = 100V

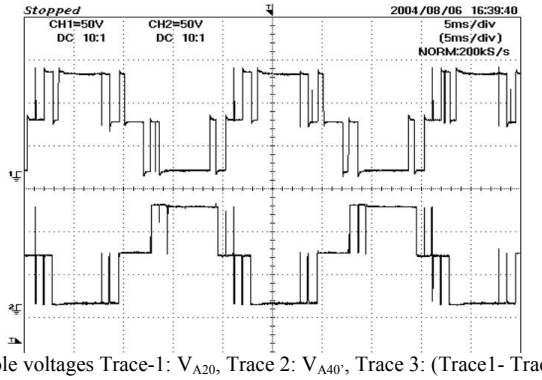


(b)Trace 1: Phase voltage V_{A2A4}X axis: 1div=10 ms, Y axis: 1 div = 100V
Trace 2: Phase current X axis: 1div=10 ms, Y axis: 1 div = 2A

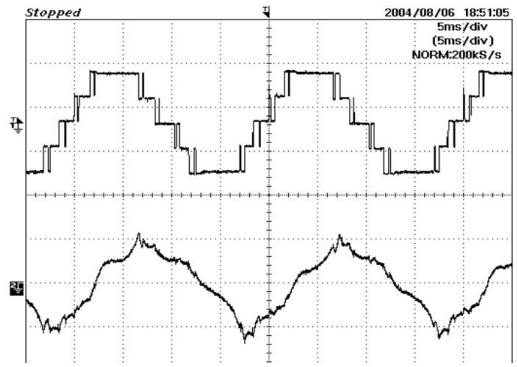


(c) Normalized harmonic spectrum for pole voltages and phase voltages

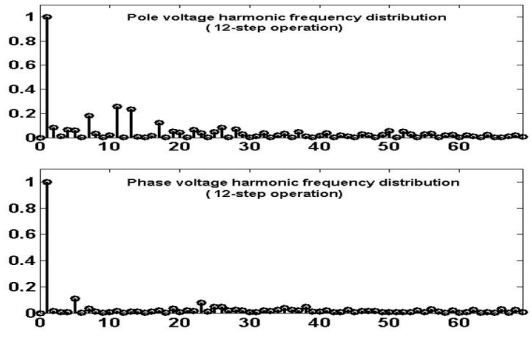
Fig. 14: The operation of three-level inverter in Layer-2 (Modulation index 0.48)



(a) Pole voltages Trace-1: V_{A20}, Trace 2: $V_{A40'}$, Trace 3: (Trace1- Trace2) X axis: div=20 ms, Y axis: 1 div = 100V



(b) Trace 1: Phase voltage V_{A2A4} X axis: 1div=20 ms, Y axis: 1 div = 100V, Trace 2: Phase current X axis: 1div=20 ms, Y axis: 1 div = 4A



(c) Normalized harmonic spectrum for pole voltages and phase voltages

Fig. 15: The operation of three-level inverter in 12 step mode (Modulation index 1.3)

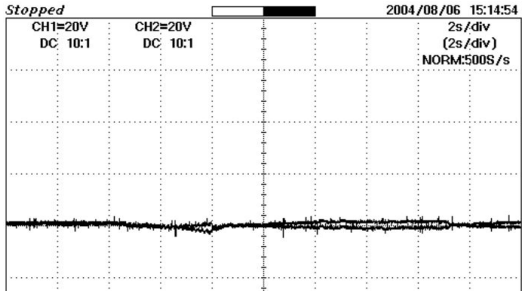


Fig. 16: Balancing of DC link capacitor voltages V_{C1} and V_{C2} during steady state operation [Scale: X-axis: 1 div= 20V, Y-axis:1 div= 2 s]

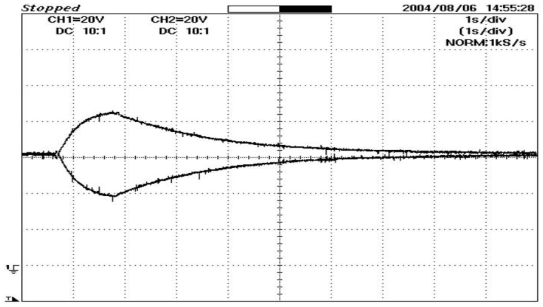


Fig. 17: Balancing of the DC Link capacitor voltages after the controller is disabled for small interval, outer layer operation Top Trace: V_{C1} , bottom trace: V_{C2} [Scale: X -axis: 1 div.= 20V, Y -axis: 1 div.= 1 s]

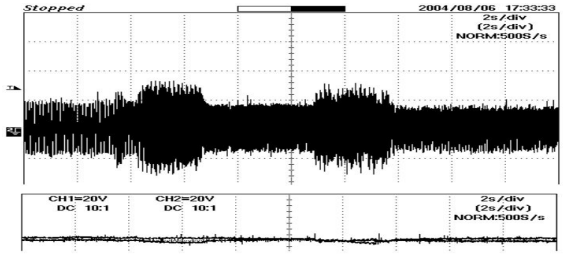


Fig. 18: The DC link voltages and machine phase current under while machine, operating in inner layer, is accelerated to outer-layer and then to over-modulation. Top Traces: V_{C1} and V_{C2} , bottom trace: Phase current. [Scale: X -axis: 1 div= 20V, 2A, Y-axis: 1 div= 2 s]

VIII. CONCLUSION

A three-level inverter scheme for an open end winding induction motor with zero common mode voltage in pole voltage as well as in the phase voltage with split capacitor DC link balancing is proposed in this paper. The availability of redundant switching combinations for all vector locations are used to balance the DC link voltages without disturbing the SVPWM modulation. Thus, a single front-end rectifier can be used, with two capacitors for splitting the DC link voltage. The proposed three-level inverter configuration has more multiplicity in the inverter voltage vector locations as compared to the conventional single three-level inverter. The proposed capacitor voltage balancing scheme is characterized by altering switching combinations of the inverter voltage vectors for consecutive switching time durations, without jeopardizing the SVPWM. The proposed capacitor voltage-balancing scheme is implemented without compromising on the SVPWM scheme and simple hysteresis controller is used to balance the DC link capacitor voltages.

APPENDIX 2: Induction motor parameters

3 phase, 1.5 kW, 50 Hz, 4 pole , 230 V, *Rs*= 2.08 ohms, *Rr*= 1.19 ohms, *Lr*=0.28 H, *Ls*= 0.28 H, *M*=0.272 H

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