A Review of Multi-Level Inverter Technology for High-Power Induction Motor Drives

P.N. Tekwani[1] and K. Gopakumar[2]

[1]Department of Electrical Engineering, Institute of Technology, Nirma University, Ahmedabad
[2]Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore

***Abstract*—Multi-level inverter technology has become a preferred solution for high-voltage high-power induction motor drive systems. This is because of the considerable inherent advantages offered by multi-level inverters compared to their two-level counter parts. Neutral-point-clamed, flying capacitors, cascaded H-bridge and dual inverter fed open-end winding induction motor configurations are amongst the most widely used multi-level inverter topologies as on today. This paper presents a review of multi-level inverter technology used for the high-power induction motor drive applications. Advantages and drawbacks of different multi-level inverter topologies are discussed with their comparative analysis for device rating, power-bus complexity and dc-link capacitor voltage balancing point of views.**

***Index Terms*—High-Power Induction Motor Drives, Multi-Level Inverter Technology.**

I. Introduction

The pulse width modulation (PWM) inverters provide easy and effective control of voltage and frequency in adjustable speed drives (ASD). The PWM inverter reduces the amplitudes of lower order harmonics in the motor terminal voltage by shifting the dominating harmonics towards higher frequencies. Even though, switching the PWM-VSI fed ASD at higher frequencies results in improvement in the overall performance of the drive, it causes significant amount of switching losses and generates conducted as well as radiated *electromagnetic interference* (EMI). As the two-level inverters have to switch between the two extreme levels of the dc-link voltages, they involve large voltage change rates (*dv/dt*) in every switching. This *dv/dt* effect can result in additional EMI and increased stress on the insulation of the machine windings. This large *dv/dt* also appears in the alternating common-mode voltage (CMV) generated by the PWM controlled two-level inverters and can cause the motor shaft voltages, flow of motor bearing currents and consequently increased ground leakage currents. Also, in a two-level inverter, each device has to be rated to block the entire dc-link voltage during its off time. So, when used for high-voltage and high-power drive applications, the conventional two-level inverters experience above mentioned limitations. Therefore, in practice, use of conventional two-level inverters employing PWM techniques is restricted to low and medium power applications.

For the high-voltage high-power industrial drives, PWM-VSIs operating at high switching frequencies are seldom preferred due to considerable switching losses. Thus, the task of reducing harmonic contents in the output voltage has to be addressed in a different way for PWM-VSI fed IM drives, especially for high-voltage high-power applications. This has been made possible by the use of different class of PWM inverters, termed as m*ulti-level inverters*. Multi-level inverters are realized from a number of smaller discrete voltage sources, and they generate the output voltage waveforms with more steps of smaller magnitudes. Significant inherent advantages offered by the multi-level inverters compared to their two-level counterparts (two-level inverters) are listed as follows [1]-[11]:

- It is possible to use power semiconductor devices of lower voltage ratings to realize high voltage levels at inverter output;
- It is possible to obtain refined output voltage waveforms and reduced *total harmonic distortion* (THD) in voltage with increased number of voltage levels (stepped output voltage waveforms);
- It is possible to obtain machine currents with reduced harmonics, resulting into reduced torque pulsations in the drive system;
- It is possible to reduce the EMI problems by reducing the switching *dv/dt*;
- Lower amplitudes of alternating CMV and hence lower bearing currents;
- Less stress on the insulation of machine phase windings;
- Inverter can be operated with the lower switching frequency and hence the switching losses are reduced.

Although designed initially to reduce the harmonic contents in the output voltage waveforms, the multi-level inverters have very quickly established themselves as a preferred option for realizing high-voltage high-power drives for industrial, marine, utility and traction applications, using power devices of lower voltage ratings. Today, multi-level inverters are extensively used in high-power drive applications for laminators, mills, conveyors, pumps, fans, blowers, compressors, etc. [11].

II. General Background of Multi-level Inverters

Multi-level inverters generate output voltage with stepped waveforms by using an array of power semiconductors and capacitor voltage sources. The commutation of switches

permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1 shows the schematic of one phase leg (pole-A) of inverters with different numbers of levels, for which the action of power semiconductors is represented by an ideal switch with several positions. As shown in Fig. 1(a), for two-level inverter, the position of the switch is represented by switching function s_A, which can attain any of the two distinct values 0 or 1. The point O in Fig. 1(a) is a fictitious neutral point (mid point of the dc-link) considered for the representation of the pole voltage v_{AO}. Thus, $v_{AO} = -V_{dc}/2$ when $s_A = 0$, and $v_{AO} = V_{dc}/2$ when $s_A = 1$. Similarly, the switching function for pole-B and pole-C are defined as s_B and s_C, respectively [1]-[11].

For a three-level inverter, as shown in Fig. 1(b), the pole voltage levels $-V_{dc}/2$, 0, and $V_{dc}/2$ can be attained with corresponding switching function values 0, 1, and 2, respectively. In a similar way, for a five-level inverter, the pole voltage levels $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$ and $V_{dc}/2$ can be attained with switching function values 0, 1, 2, 3, and 4, respectively (Fig. 1(c)). For a general *n*-level inverter, the switching function has a range from 0 to *n*-1, as shown in Fig. 1(d) [11].

The pole voltages of inverter are defined in terms of the switching functions as in (1), where *n* represents the number of levels of inverter. When an induction motor with Wye (Y) connected stator is connected at the output terminals of the inverter, the inverter pole voltage can be represented in terms of phase to motor neutral-point voltages and motor neutral to the inverter dc-link neutral (mid) point voltage, as given by (2). Considering balanced three-phase system (i.e., $v_{AN}+v_{BN}+v_{CN} = 0$), (2) can be rewritten as (3). The voltage v_{NO} is known as common-mode voltage (CMV). Using (2) and (3), phase to motor neutral-point voltages can be expressed in terms of the inverter pole voltages by (4). Similarly the motor line-to-line voltages can be written as in (5). The inverter pole voltages contain harmonics of third order and its multiples (triplen harmonics), which are absent (as they get cancelled) in the phase-to-motor neutral voltage and line-to-line voltage.

$$\begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} = \frac{V_{dc}}{(n-1)} \begin{bmatrix} s_A - \left((n-1)/2\right) \\ s_B - \left((n-1)/2\right) \\ s_C - \left((n-1)/2\right) \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} = \begin{bmatrix} v_{AN} + v_{NO} \\ v_{BN} + v_{NO} \\ v_{CN} + v_{NO} \end{bmatrix} \tag{2}$$

$$v_{NO} = \frac{1}{3}\left[v_{AO} + v_{BO} + v_{CO}\right] \tag{3}$$

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \tag{5}$$

The inverter voltage space phasor is represented in terms of the three pole voltages as in (6). It is evident from (2) and (3) that the phase voltages v_{AN}, v_{BN}, v_{CN} also result in the same voltage space phasor $\mathbf{V_S}$. Hence, the inverter voltage space phasor represents the combined information of all the three phase voltages. The space phasor $\mathbf{V_S}$ can be resolved into two rectangular components (along α and β axes) as shown in (7). The relationship between the components of $\mathbf{V_S}$ and the instantaneous phase voltages of motor is given by the conventional ABC-αβ transformation as in (8).

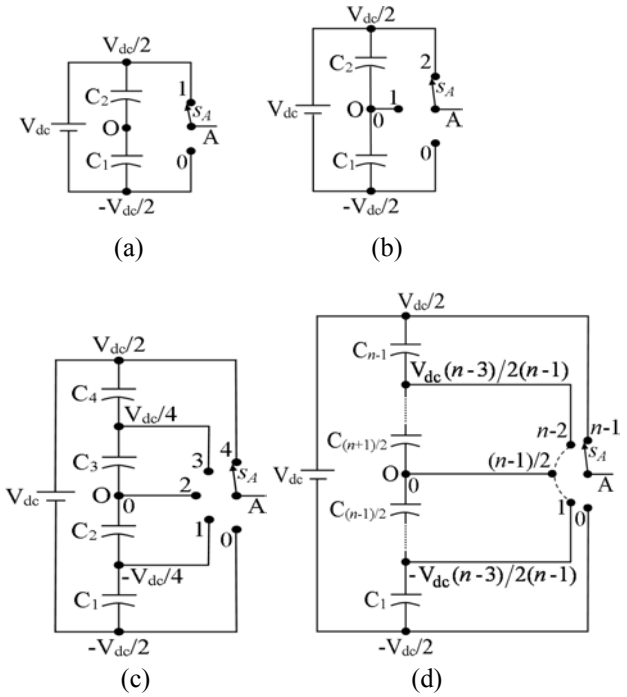


Fig. 1: Representation of one leg (pole) of an inverter: (a) two-level, (b) three-level, (c) five-level, and (d) general n-level

Similarly, the inverse transformation in (9) provides αβ-ABC conversion.

$$\mathbf{V_S} = v_{AO} + v_{BO}e^{j120^\circ} + v_{CO}e^{j240^\circ} \tag{6}$$

$$\mathbf{V_S} = V_{S(\alpha)} + jV_{S(\beta)} \tag{7}$$

$$\begin{bmatrix} V_{S(\alpha)} \\ V_{S(\beta)} \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \begin{bmatrix} 2/3 & 0 \\ -1/3 & 1/\sqrt{3} \\ -1/3 & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_{S(\alpha)} \\ V_{S(\beta)} \end{bmatrix} \quad (9)$$

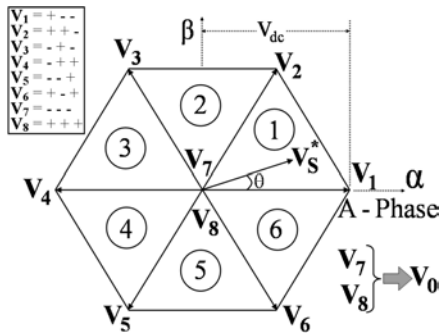
As shown in Fig. 1(a), each pole of the two-level inverter can attain two voltage levels, viz. $-V_{dc}/2$ and $V_{dc}/2$. Therefore the total number of switching states that a two-level inverter can generate is $2^3 = 8$. For each pole of the two-level inverter, if the voltage level $-V_{dc}/2$ is indicated by '-' (bottom switching device of the pole is "ON") and $V_{dc}/2$ is indicated by '+' (top switching device of the pole is "ON"), then the switching states of the inverter can be represented as (+--), (++-), (-+-), (-++), (--+), (+-+), (---), (+++). For every switching state, the signs inside the bracket represent the states of the switches (voltage level), of inverter pole A, B and C, respectively. The voltage space vectors corresponding to these eight switching states of the two-level inverter are defined as $\mathbf{V_1}$, $\mathbf{V_2}$, $\mathbf{V_3}$, $\mathbf{V_4}$, $\mathbf{V_5}$, $\mathbf{V_6}$, $\mathbf{V_7}$, and $\mathbf{V_8}$ respectively, as shown in the voltage space phasor structure in Fig. 2(a). The triangular sectors of inverter voltage space phasor structure are indicated by encircled numbers, 1 to 6, in Fig. 2(a). In case of voltage vectors $\mathbf{V_7}$ and $\mathbf{V_8}$, all the three poles of the inverter are connected to the same dc-bus (voltage level), effectively shorting the load and resulting no transfer of power between the dc-link and the load. Hence, $\mathbf{V_7}$ and $\mathbf{V_8}$, are known as *zero voltage vectors* ($\mathbf{V_0}$). In case of each of the remaining six vectors, power gets transferred between the dc-link and the load. Therefore, these voltage vectors ($\mathbf{V_1}$, $\mathbf{V_2}$, …, $\mathbf{V_6}$) are known as *active voltage vectors*.

For an *n*-level inverter, the number of switching states '*t*' generated by the inverter is given by (10) and the number of voltage vectors '*k*', generated by the inverter, is given by (11). The inverter space phasor locations for a three-level and a five-level inverter configuration are shown in Fig. 2(b) and Fig. 2(c), respectively. In Fig. 2(b) the pole voltage level 0 (Fig. 1(b)) is indicated by '0' in the switching states. Whereas, in Fig. 2(c), the pole voltage levels $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$, and $V_{dc}/2$ (Fig. 1(c)) are indicated by -2, -1, 0, 1, and 2 respectively in the switching states, for the sake of clarity [11].

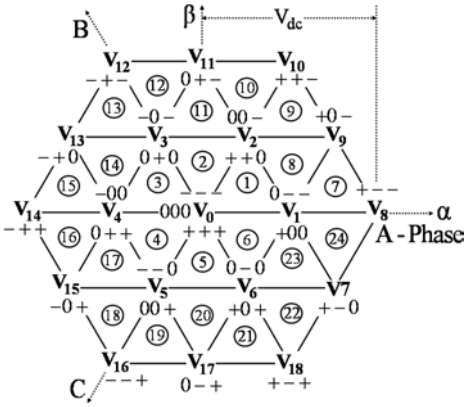
$$t = n^3 \quad (10)$$

$$k = 3(n)(n-1)+1 \quad (11)$$

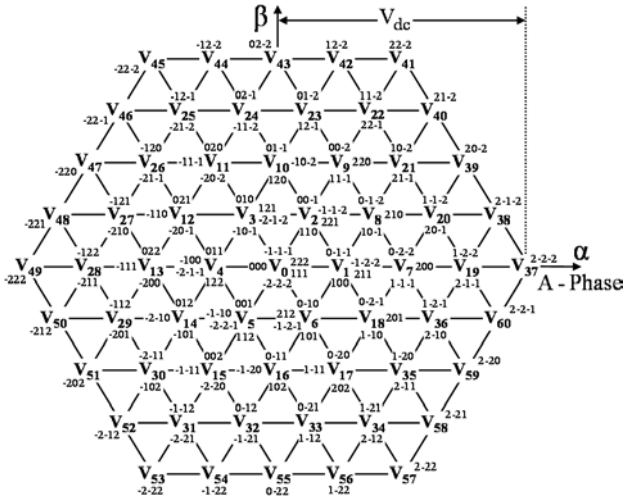
It is to be noted that the voltage vector $\mathbf{V_7}$ and $\mathbf{V_8}$ (Fig. 2(a)) effectively generate the same voltage vector location, hence the switching states (---) and (+++), which generate this zero voltage vectors, are known as redundant switching states of zero voltage vector ($\mathbf{V_0}$). Similarly, the switching states which generate the same inverter voltage vector are considered as redundant switching states of that voltage vector. In the voltage space phasor structures of Fig. 2, the central (zero) inverter vector has multiplicity of switching states (redundant switching states) of *n*. As evident in Fig. 2, the multiplicity of switching states for the inverter vectors goes on reducing as one moves towards the outer inverter voltage vector locations of the voltage space phasor structure, and the outer-most inverter vectors do not have any multiplicity.



(a)



(b)



(c)

Fig. 2: Voltage space phasor structure of an inverter: (a) two-level (7 voltage vectors, 6 triangular sectors, 8 switching states) (b) three-level (19 voltage vectors, 24 triangular sectors, 27 switching states), and (c) five-level (61 voltage vectors, 96 triangular sectors, 125 switching states)

In the PWM switching, the three nearest (adjacent) inverter vectors at the edges of the triangular sector, in which the tip of the reference vector ($\mathbf{V}_S^*$, Fig. 2(a)) lies, are selected for inverter switching. The distance between the reference voltage vector and the nearest inverter voltage vector directly determines the harmonic content in the output voltage waveform. As seen from Fig. 2, the inverter voltage vectors are placed very close to each other for higher level inverter configurations (for example, five-level inverter space vectors, Fig. 2(c)), which results in reduced harmonic contents in the output voltage and the current waveforms are more sinusoidal (with lower THD).

Various topologies of multi-level inverters are reported in the literature [1]-[52]. The most commonly used multi-level inverter configurations are neutral-point-clamped (NPC) (diode-clamped), flying capacitors (capacitor-clamped), cascaded H-bridge (cascaded multicell) and dual inverter fed open-end winding IM structure. Comparative studies have been carried out for these inverter topologies to judge their performance [5], [11], [18].

III. Different Multi-level Inverter Topologies

In the multi-level inverters based on the neutral-point clamped strategy, voltage across the series connected capacitors is assumed to be constant to achieve equal sharing of the dc-link voltages among the switches. But, these capacitor voltages can fluctuate over a fundamental cycle (depending on the load current drawn from the dc-link) and this means that devices are called upon to block higher voltages than the ideal condition where each device has to block only $V_{dc}/(n\text{-}1)$ for an n-level inverter [3]-[6], [8]-[11]. Fig. 3 shows power schematics of a multi-level NPC inverter.

The flying capacitor multi-level inverters do not need the clamping diodes but need a large number of bulky capacitors as floating sources to clamp the voltage. If capacitors with equal voltage rating ($V_{dc}/(n\text{-}1)$) as the main switches are used, an *n*-level inverter will need (*n*-1) x ((*n*-2)/2) capacitors per pole as floating sources [5], [11], [12] in addition to (*n*-1) main dc-bus capacitors. In inverters where the number of levels is high, the control also becomes complicated, as the voltages across a large number of capacitors have to be maintained by ensuring proper duty ratios in the switches [16], [17]. But the large amount of energy/voltage storage in the capacitors provides better ride-through capabilities to this class of inverters against the input supply interruptions. Fig. 4 shows basic building block (one leg) of power schematic of a five-level flying capacitor inverter.

Cascaded inverters have become popular in high-power drive applications because of their modular structure and simplicity of control [18]. They are particularly attractive for large electric drive applications where separate dc sources are available in large numbers in the form of batteries. The inverter structure is very simple as each inverter cell has identical structure and thus the extension to higher levels does not add any more power-bus complexity. Also the complicacies like, the capacitor voltage balancing, or clamping diodes/capacitors etc. are not required. The limitation of this topology is the requirement of large number of separate dc sources. Fig. 5 shows block schematic of cascaded H-bridge inverter, which results into a five-level voltage space phasor structure.

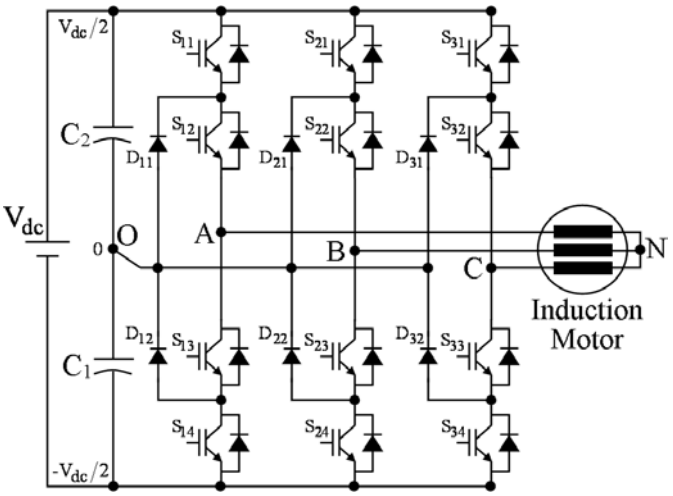


Fig. 3(a): Power schematic of a three-level neutral-point-clamped (NPC) inverter

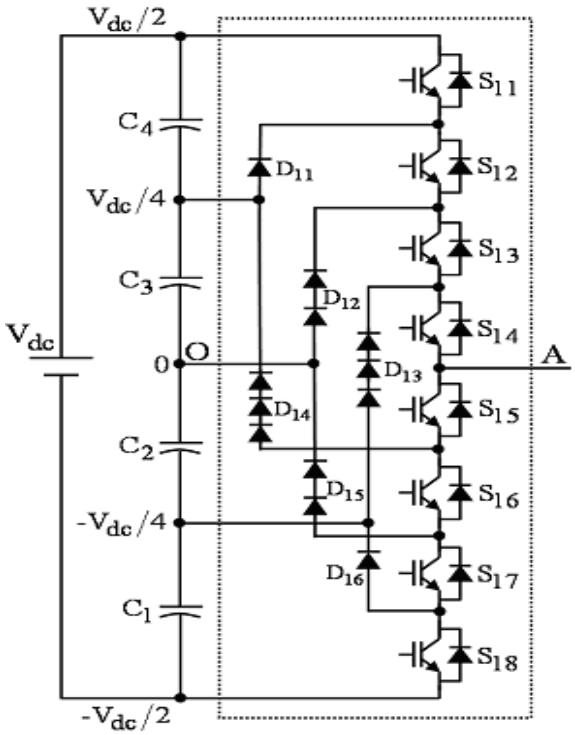


Fig. 3(b): Power schematic of one leg of a five-level neutral-point-clamped (NPC) inverter

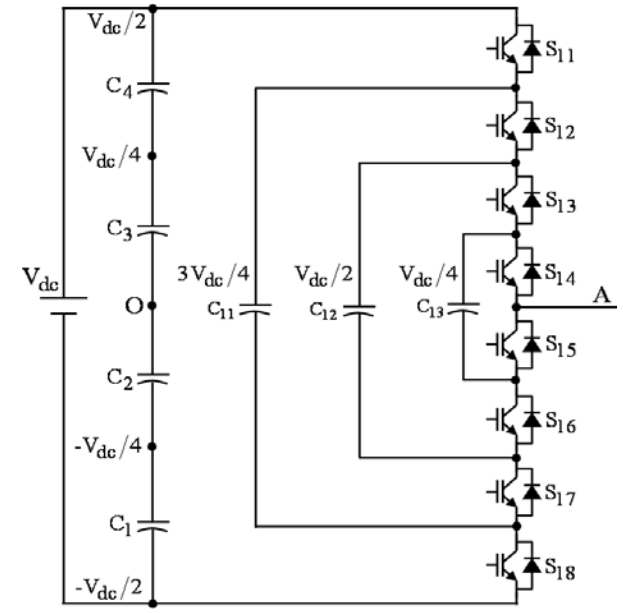


Fig. 4: Basic building block (one leg) of a five-level flying capacitor (capacitor-clamped) inverter configuration

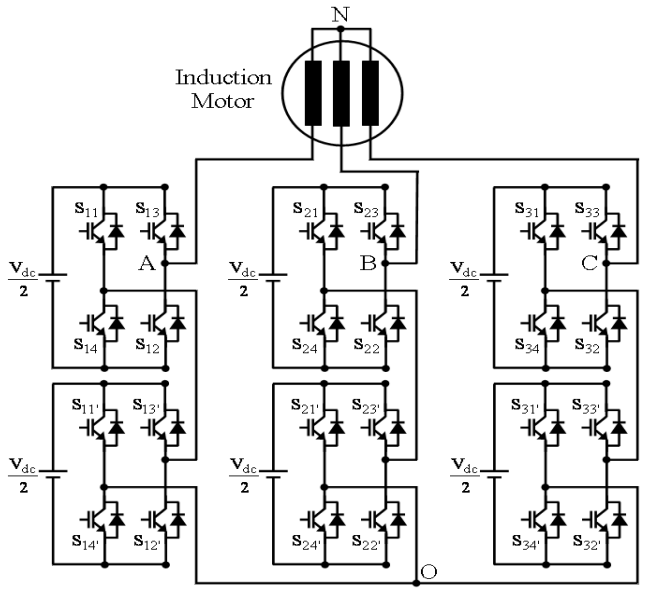


Fig. 5: Power schematic of cascaded H-bridge five-level inverter

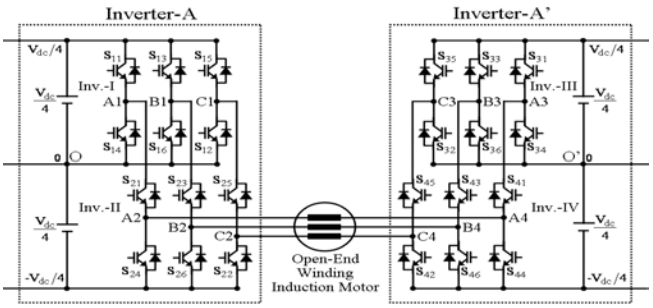


Fig. 6: Power schematic of dual three-level inverter fed open-end winding IM drive (capable of generating a five-level inverter voltage space phasor structure)

In dual two-level inverter fed open-end winding IM drive, the dc-link voltage of each inverter is half the dc-link voltage of single three-level inverter fed conventional IM drive. The added advantage is that the clamping diodes are not required and the drive does not have any neutral-point fluctuation. Also, here a total of 64 (8x8 of each of the two-level inverters) switching state combinations are possible compared to a total of 27 switching states for a single three-level inverter fed conventional IM drive [19]. This increased redundancy of switching states to generate the same number of voltage vectors turns out to be a very useful feature for achieving common-mode voltage elimination and dc-link capacitor voltage balancing in multi-level inverter fed drives with higher number of levels. Fig. 6 shows power schematic of a dual three-level inverter fed open-end winding IM drive. Here, each of the individual three-level inverters (Inverter-A and Inverter-A') is fabricated by cascading two conventional two-level inverters. The inverter scheme of Fig. 6 generates a five-level inverter voltage space phasor structure.

IV. Conclusion

Multi-level inverter technique is a preferred solution for high-power induction motor drives. Different multi-level inverter topologies are proposed in the literature. Selection of particular topology should be made as per the application requirements considering simplicity in power-bus structure, less device count, modularity of structure, reduced control complexity and dc-link capacitor voltage balancing capability. Also, for multi-level inverter technology, the issues of generation of alternating CMV in the drive system and voltage unbalance within various capacitors of the dc-link are to be taken care of by different means.

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