Multilevel inverter with 12-sided polygonal voltage space vector locations for induction motor drive

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Abstract: Multilevel inverters are preferred over two-level inverters in high-voltage, high-power applications mainly because low-switching-frequency PWM schemes can be implemented with power devices of low-voltage ratings. Common multilevel inverter structures such as NPC, H-bridge and flying capacitor will produce a hexagonal voltage space vector structure. In the over-modulation range a multilevel inverter with a hexagonal voltage space vector structure will produce high amplitude 5th and 7th harmonic voltages in the output voltages. The maximum phase peak fundamental voltage is 0.637 *Vdc* in six-step mode operation (where *Vdc* is the radii of the hexagonal voltage space vector structure). A 12-sided polygonal voltage space vector structure will have a maximum phase peak fundamental voltage of 0.64 *Vdc* in the linear modulation range itself (where *Vdc* is the radii of the 12-sided polygonal voltage space vector structure), which is more than the output in six-step operation in the over-modulation range for a conventional multilevel structure. Also with a 12-sided polygonal space vector structure, an additional boost of the fundamental phase voltage is possible in the 12-step operation with the elimination of the 5th- and 7th- order harmonics ($6n\pm1$, $n=1,3,5\ldots$ etc). A multilevel inverter structure with 12-sided polygonal voltage space vector structure is proposed for an induction motor drive. The proposed inverter structure is realised by cascading three conventional two-level inverters. This makes the power bus structure very simple.

1 Introduction

Ever since Nabae *et al.* proposed the NPC (neutral-point clamped) three-level inverter, multilevel inverters have established themselves as the industry choice for high-power drive applications [1]. As the multilevel inverters can be operated at lower switching frequencies, the very first advantage with multilevel inverters over conventional two-level counterparts is the reduced switching losses. Various inverter topologies, like NPC, cascaded H-bridge and flying capacitor based multilevel inverter topologies, have been proposed in the literature [2–5]. Another interesting multilevel inverter scheme has been proposed for IM drive with open-end winding configuration. But this calls for opening of machine neutral [6–8].

There have been varieties of modulation schemes proposed for multilevel inverter drives, of which SPWM and SVPWM are the most popular [9–12]. In conventional multilevel inverters, the SVPWM schemes are based on hexagonal voltage space vectors and the inverter vectors along the radii of the hexagon are selected for inverter switching. In the linear modulation range, high amplitude harmonic components are present at the switching frequency and its sidebands [14]. But in overmodulation, lower-order harmonics of order $6n\pm1$ ($n=1,2,3,\ldots$) are present in the output. Modulation schemes have been presented, in the past, for inverter-fed induction motor drives, to selectively eliminate or suppress $6n\pm1$, ($n=1,2,3,\ldots$) order harmonics from the machine phases [14]. The harmonic elimination scheme proposed in [14] involves the switching of inverter vectors from a 12-sided polygon. The complete elimination of $6n\pm1$, $n=1,3,5,\ldots$ harmonic components have been demonstrated in this scheme along with significant suppression of 11th- and 13th- order harmonic components. The realisation of a 12-sided polygonal inverter voltage vectors has been demonstrated with an open-end induction motor fed from two sides by two-level inverters of different DC-link voltages, which calls for opening of machine neutral.

In this paper, a 12-sided polygonal space vector generation scheme is proposed for IM drives. The 12-sided polygon is achieved with inverter structure formed by cascading three two-level inverters fed with asymmetric links. The induction motor can be fed from a single side with no alterations in the windings. The complete elimination of $6n\pm1$, $n=1,3,5,\ldots$ order harmonics is achieved with the proposed scheme throughout the modulation range. The linear range of modulation for the proposed inverter scheme is 0.64 *Vdc*, whereas it is 0.577 *Vdc* for the inverter schemes based on conventional schemes (*Vdc* is the radii of the voltage space vector polygon). Similarly, the maximum value of the fundamental component in the output phase voltage that can be generated from the proposed scheme is 0.658 *Vdc* (12-step mode operation, with the absence of 5th- and 7th- order harmonics) as compared to 0.637 *Vdc*, in a conventional six-step switching mode (high amplitude 5th and 7th harmonics are present). The inverter bus structure is simple as it is based on cascading two-level inverters and it does not call for opening of machine neutral. The proposed scheme has been simulated using MATLAB and experimentally verified

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using a 1.5 kW induction motor drive under V/f control, and the results are presented.

2 Power circuit of proposed inverter-fed IM drive configuration

A schematic of the power circuit of the proposed induction motor drive is shown in Fig. 1*a*. The overall configuration consists of cascaded combination of three two-level inverters, namely, INV1, INV2, INV3, fed from asymmetric DC links. INV1 and INV3 are supplied with voltage $0.366\,kV_{dc}$ whereas INV2 is fed with a DC link supply of $0.634\,kV_{dc}$ (the factor '*k*' can be appropriately selected such that the radii of the 12-sided voltage space vector polygon is the same as that of the conventional hexagonal voltage space vector structure). Each DC-link is supplied with isolated power supplies. The switches in each leg of the individual two-level inverters are operated complementary to each other. The state of the upper switch automatically determines the state of the lower switch in a leg. Let '0' represent the off state and '1' the on state of the switches. Each pole of the overall inverter configuration can realise different voltage levels depending on the condition of the switching devices in the respective leg. When S_{24}, S_{34} (Fig. 1*a*) are on, pole A of the overall inverter assumes a voltage level of zero and when S_{24}, S_{31} (Fig. 1*a*) are on, the inverter pole is at voltage $0.366\,kV_{dc}$. Similarly, the states of various switches and the resultant pole voltage are summarised in Table 1. The pole voltage levels for leg B and leg C can be determined in similar way from the switch states in the respective legs. Table 1 shows the switching states and the corresponding levels for the pole voltages. A '0/1' implies that the switch can be either on or off ('don't care'condition). Each phase is required to attain one of the four levels (0–3, Table 1), the levels being $0\,V_{dc}$, $0.366\,kV_{dc}$, $1.0\,kV_{dc}$ or $1.366\,kV_{dc}$. From Fig. 1*a* and Table 1 it can be noted that switches of INV1 and INV3 require a voltage blocking capacity of $0.366\,kV_{dc}$, while the switches in the middle inverter (INV2) require a voltage rating of $1.0\,kV_{dc}$. For example, for a pole voltage level of $1.366\,kV_{dc}$ for phase A, it can be noted from Fig. 1*a*, that the switches to be turned ON are S_{31} (INV3), S_{21} (INV2) and S_{11} (INV1). This will make the switch S_{24} of inverter 2 block a DC-link voltage of $1\,kV_{dc}$. Similarly, for a pole voltage of $0\,V_{dc}$ for phase A, the switches to be turned on are S_{14} (INV1), S_{24} (INV2) and S_{34} (INV3). In this mode switch S_{21} of inverter 2 has to block a DC-link voltage of $1\,kV_{dc}$. So inverter 2 switching voltage ratings will be 73% of the total DC-link voltage of the inverter systems.

3 Voltage space vectors of proposed scheme

The combined effect of the three pole voltages in the three 120° separated phase windings of the induction motor at any instant can be represented by an equivalent voltage

Table 1: Switching states to realise various voltage levels for one pole (leg A)

		A phase		
Pole voltage	Level	S_{11}	S_{21}	S_{31}
$1.366\,kV_{dc}$	3	1	1	0/1
$1.0\,V\,kV_{dc}$	2	0	1	0/1
$0.366\,kV_{dc}$	1	0/1	0	1
$0\,V_{dc}$	0	0/1	0	0

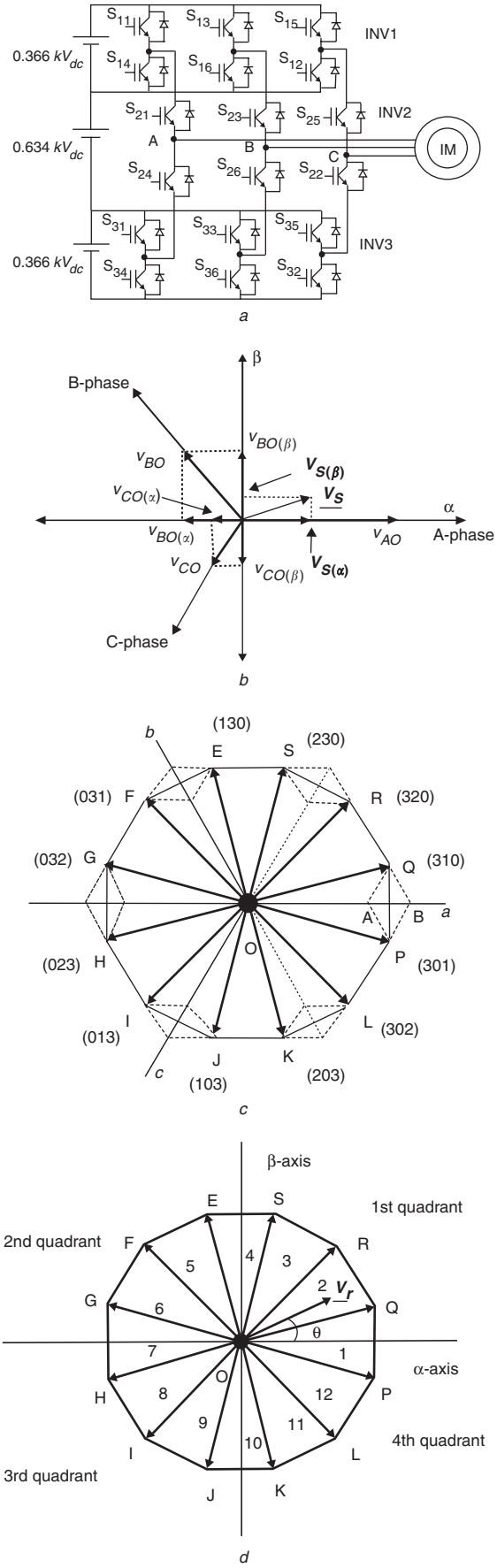


Fig. 1
a Power circuit
b Equivalent space vectors
c 12-sided polygonal voltage space vectors
d Sectors of 12-sided polygon

space vector $\boldsymbol{V_s}$ given by

$$\boldsymbol{V_s} = v_{AO} + v_{BO}e^{j\frac{2\pi}{3}} + v_{CO}e^{j\frac{4\pi}{3}} \quad (1)$$

This equivalent vector can be determined by resolving the phase voltages along two mutually perpendicular axes, α–β axes, of which α is along the A phase (Fig. 1*b*). The voltage space vector is then given by

$$\boldsymbol{V_s} = V_{s(\alpha)} + j\,V_{s(\beta)} \quad (2)$$

where $V_{s(\alpha)}$ is the sum of all components of v_{AO}, v_{BO} and v_{CO} along the α axis and $V_{s(\beta)}$ is the sum of the components of v_{AO}, v_{BO} and v_{CO} along the β axis:

$$V_{s(\alpha)} = v_{AO} - \frac{1}{2}v_{BO} - \frac{1}{2}v_{CO} \quad (3)$$

$$V_{s(\beta)} = \frac{\sqrt{3}}{2}v_{BO} - \frac{\sqrt{3}}{2}v_{CO} \quad (4)$$

Equation (3) can also be written in matrix form as:

$$\begin{bmatrix} V_{s(\alpha)} \\ V_{s(\beta)} \end{bmatrix} = \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \quad (5)$$

Figure 1*b* shows how the reference vector is generated from the components of the vectors along the three phases.

4 Generation of 12-sided polygonal voltage space vectors

Each pole of the proposed inverter scheme can take four levels of pole voltages independently in any three phases, depending on the condition of the inverter switches, as decided by the modulation scheme. When pole A of the proposed inverter configuration is at level '3' (represented as OB in Fig. 1*c*), pole B is at level '1' (represented as BQ in Fig. 1*c*) and pole C at level '0', the equivalent space vector $\boldsymbol{V_s}$ is represented by vector OQ as shown in Fig. 1*c*. This vector OQ is equivalently represented as '310' in Fig. 1*c*. Similarly, when pole A of the proposed inverter configuration is at level '3' (represented as OB in Fig. 1*c*), pole B is at level '0' and pole C at level '1' (represented as BP in Fig. 1*c*), the equivalent space vector $\boldsymbol{V_s}$ is represented by vector OP as shown in Fig. 1*c*. (the corresponding three-phase pole voltage level is '301'). In a similar way, a total of 12 active voltage space vectors, separated by 30° and one zero voltage space vector, can be realised with different voltage levels on pole A, pole B and pole C. These voltage space vectors and their combinations are as shown in Fig. 1*c* and Table 2. (In Table 2 k can be chosen in such a way that the radius of the 12-sided voltage space vector polygon is equal to V_{dc}, and is the same as the radius of a conventional hexagonal structure).

The zero voltage space vector is generated when all the pole voltages are at the same level. From Fig. 1, it can be noted that there are four combinations of pole voltages possible for the zero voltage space vector location. For the present study the zero pole voltage level (switching state '000') is used for the PWM implementation.

5 Space vector PWM with 12-sided polygon

Figure 1*c* shows the 12-sided polygonal voltage space vector locations. The 12 sectors formed are numbered from 1 to 12, as shown in Fig. 1*d*. A reference vector $\boldsymbol{V_r}$ is shown in sector 2. This reference vector is sampled with a time period T_S. Using the volt–second balance, the reference vector can be realised by switching OQ for time interval T_1 and

Table 2: Generation of active vectors from three phases

Vector	'A' phase	'B' phase	'C' phase	Combination
OP	1.366 kV_{dc}	0	0.366 kV_{dc}	301
OQ	1.366 kV_{dc}	0.366 kV_{dc}	0	310
OR	1.366 kV_{dc}	1.0 kV_{dc}	0	320
OS	1.0 kV_{dc}	1.366 kV_{dc}	0	230
OE	0.366 kV_{dc}	1.366 kV_{dc}	0	130
OF	0	1.366 kV_{dc}	0.366 kV_{dc}	031
OG	0	1.366 kV_{dc}	1.0 kV_{dc}	032
OH	0	1.0 kV_{dc}	1.366 kV_{dc}	023
OI	0	0.366 kV_{dc}	1.366 kV_{dc}	013
OJ	0.366 kV_{dc}	0	1.366 kV_{dc}	103
OK	1.0 kV_{dc}	0	1.366 kV_{dc}	203
OL	1.366 kV_{dc}	0	1.0 kV_{dc}	302

immediately followed by OR for time interval T_2. For the time interval $T_0 = T_S - T_1 - T_2$, zero voltage level is maintained in all the three pole voltages. As in the case of conventional hexagonal SVPWM signal generation, T_0 is split into two halves of $T_0/2$, one half is applied in the beginning of the time interval T_S and the other half at the end after the T_S sampling period. The same approach is employed for a reference voltage lying in the other sectors also. In sector 5, for example, vectors OE would be on for the T_1 period and OF would be on for the T_2 period. The time intervals T_1 and T_2 are found from the sampled reference phase amplitudes as derived below. The active vector switching periods T_1 and T_2 are functions of the sector number and the sampled reference phase amplitudes. The formula relating T_1 and T_2 to the phase voltage, sector number and T_S is derived using the volt–second balance method.

Let V be the magnitude of vectors OP, OQ etc., and 'm' be the sector number of the sector in which $\boldsymbol{V_r}$ lies. The volt–second balance equation in any sector for the sampled reference vector is as shown below:

$$T_1 V\angle((m-1)30^\circ - 15^\circ) + T_2 V\angle(m30^\circ - 15^\circ) = T_S(V_\alpha + jV_\beta) \quad (6)$$

The '15°' accounts for the first sector being bisected by the 'A' phase axis and being rotated by 15° from its normal (clock like) position (Fig. 1*d*). Simplifying further, (6) can be written as:

$$T_1 V\angle(m-1)30^\circ + T_2 \cdot V\angle m30^\circ = T_S(V_\alpha + jV_\beta)(\cos 15^\circ + j\sin 15^\circ) \quad (7)$$

On equating the real and imaginary parts, (7) can be separated as,

$$T_1 V\cos((m-1)30^\circ) + T_2 V\cos(m30^\circ) = T_S(V_\alpha \cos 15^\circ - V_\beta \sin 15^\circ) \quad (8)$$

$$T_1 V\sin((m-1)30^\circ) + T_2 V\sin(m30^\circ) = T_S(V_\alpha \sin 15^\circ + V_\beta \cos 15^\circ) \quad (9)$$

From (8) and (9),

$$\begin{pmatrix} T_1 \\ T_2 \end{pmatrix} = \frac{T_S}{V}\begin{pmatrix} \cos((m-1)30^\circ) & \cos(m30^\circ) \\ \sin((m-1)30^\circ) & \sin(m30^\circ) \end{pmatrix}^{-1} \times \begin{pmatrix} (V_\alpha \cos 15^\circ - V_\beta \sin 15^\circ) \\ (V_\alpha \sin 15^\circ + V_\beta \cos 15^\circ) \end{pmatrix} \quad (10)$$

On expansion and simplifying (10) we get the following:

$$T_1 = \frac{2T_S}{V}\left[V_\alpha \sin(m \cdot 30^\circ - 15^\circ) - V_\beta \cos(m30^\circ - 15^\circ)\right] \tag{11}$$

$$T_2 = \frac{2T_S}{V}[-V_\alpha \sin((m-1)30^\circ - 15^\circ) + V_\beta \cos((m-1)30^\circ - 15^\circ)] \tag{12}$$

From (11) and (12), T_1 and T_2 in terms of V_α and V_β, can also be represented in terms of the sampled reference phase amplitudes v_A, v_B and v_C:

$$V_\alpha = \frac{3}{2}v_A = -\frac{3}{2}(v_B + v_C) \tag{13}$$

$$V_\beta = \frac{\sqrt{3}}{2}(v_B - v_C) \tag{14}$$

The resulting T_1 and T_2 equations are as shown below:

$$T_1 = \frac{2\sqrt{3}T_S}{V}[-v_B \sin(m30^\circ + 15^\circ) + v_C \cos(m30^\circ + 45^\circ)] \tag{15}$$

$$T_2 = \frac{2\sqrt{3}T_S}{V}[v_B \sin((m-1)30^\circ + 15^\circ) - v_C \cos((m-1)30^\circ + 45^\circ)] \tag{16}$$

The values of $\sin(m30^\circ + 15^\circ)$ and $\cos(m30^\circ + 45^\circ)$ are precalculated and stored in lookup tables for sector 'm' varying from 0 to 12. Note that T_1 and T_2 cannot be negative, and to ensure this the correct value of 'm' is required.

6 Space vector PWM signal generation with 12-sided polygonal voltage space vectors

A simple V/f scheme is used for the present inverter-fed IM motor study. This V/f scheme is shown in Fig. 2*a*. The drive scheme is first simulated using Matlab and then experimentally verified on a 1.5 kW induction motor drive.

The three-phase reference phase voltages v_A, v_B, and v_C generated by the V/f controller is sampled at regular intervals of time (T_S), in a sector. For different modulation range, different samples are used in a sector. The number of samples of the reference vector taken in a sector is chosen so that the overall switching frequency is limited (<1000 Hz) in order to keep switching losses low, while maintaining sufficient resolution.

6.1 Number of samples in sector for different speed ranges

0–15 Hz: 4 samples per sector

15–30 Hz: 3 samples per sector

30–45 Hz: 2 samples per sector

45–50 Hz: 1 sample per sector.

In every sector the first sample is always taken at the start of a sector, in order to obtain the maximum output fundamental voltage from the PWM scheme.

6.2 Sector identification

The sector in which the reference vector lies is found using the following method. The 12-sided polygonal voltage space vector structure of Fig. 1*d* is divided into four quadrants. The four quadrants can be identified from the sampled reference phase amplitudes as shown below:

'v_A' positive, and '$(v_B - v_C)$' positive: 1st quadrant

'v_A' negative, and '$(v_B - v_C)$' positive: 2nd quadrant

'v_A' negative, '$(v_B - v_C)$' negative: 3rd quadrant

'v_A' positive, '$(v_B - v_C)$' negative: 4th quadrant.

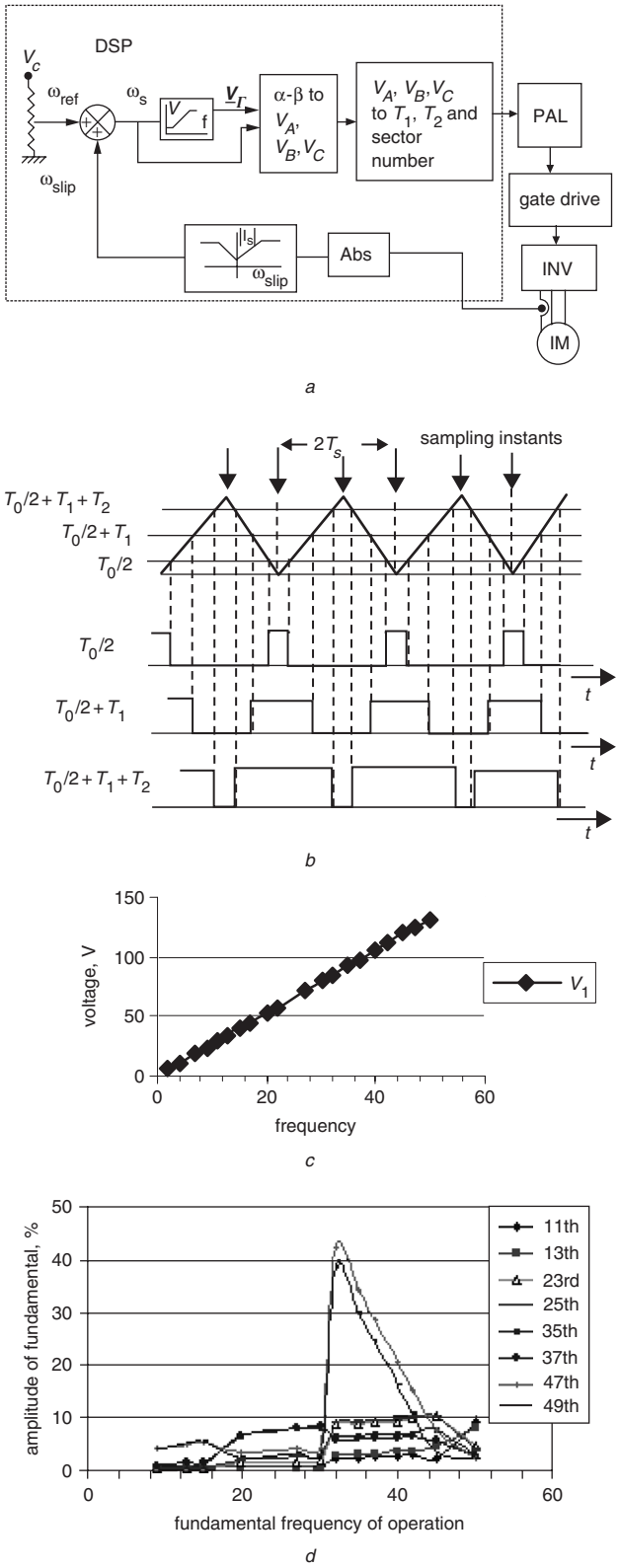


Fig. 2
a V/f scheme for proposed induction motor drive
b Comparison for obtaining time durations
c Amplitude of fundamental voltage against frequency of operation
d Harmonics at various frequencies of operation

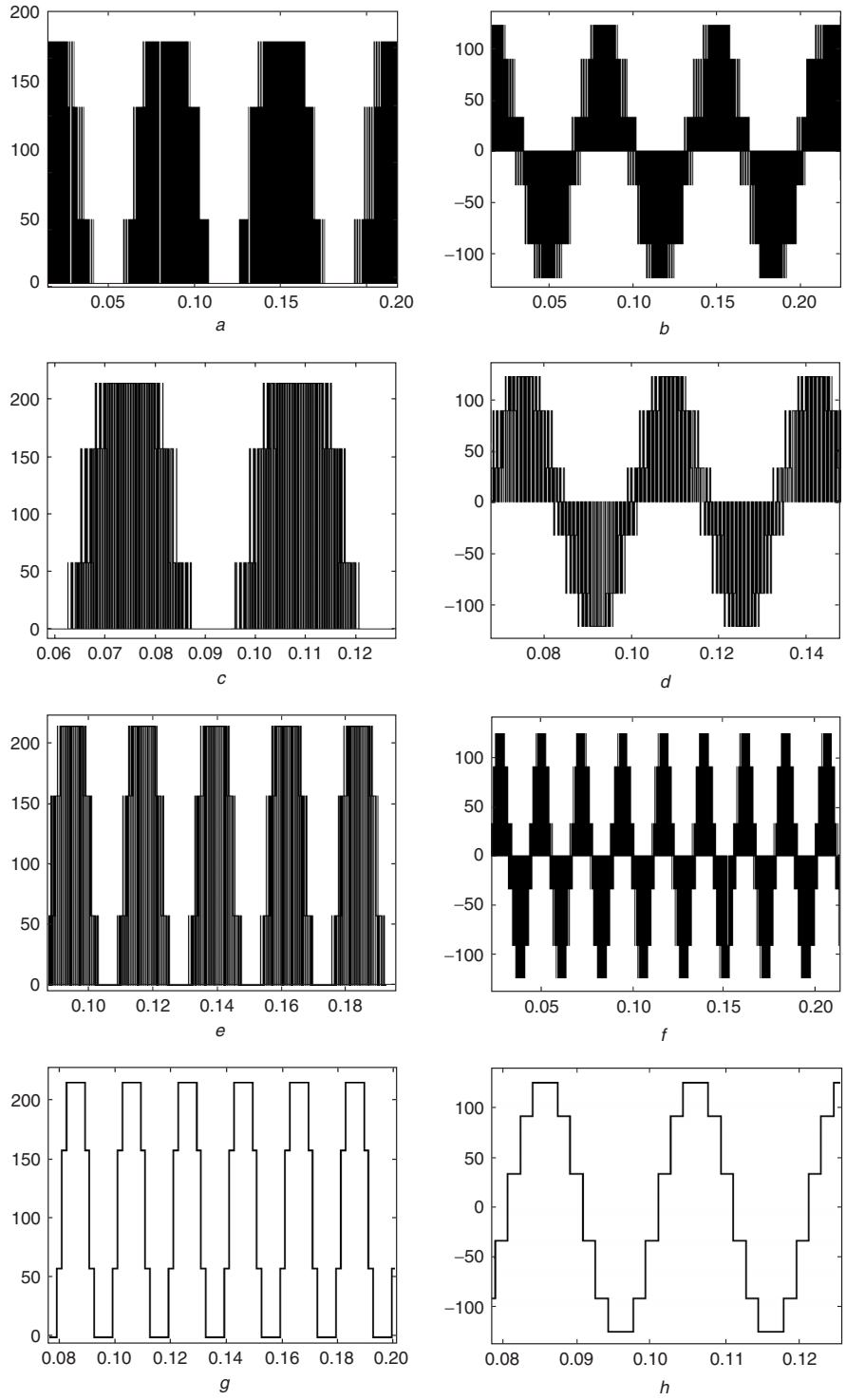


Fig. 3
a Pole voltage at 15 Hz
x-axis: 1div. = 50 ms, *y*-axis: 1div. = 50 V
b Phase voltage at 15 Hz
x-axis: 1div. = 50 ms, *y*-axis: 1div. = 50 V
c Pole voltage at 30 Hz
x-axis: 1div. = 10 ms, *y*-axis: 1div. = 50 V
d Phase voltage at 30 Hz
x-axis: 1div. = 20 ms, *y*-axis: 1div. = 50 V
e Pole voltage at 45 Hz
x-axis: 1div. = 20 ms, *y*-axis: 1div. = 50 V
f Phase voltage at 45 Hz
x-axis: 1div. = 50 ms, *y*-axis: 1div. = 50 V
g: Pole voltage at 50 Hz
x-axis: 1div. = 20 ms, *y*-axis: 1div. = 50 V
h Phase voltage at 50 Hz
x-axis: 1div. = 10 ms, *y*-axis: 1div. = 50 V

Once the quadrant is found, the sector in which the reference vector lies can be found using the following method:

If in quadrant 1:

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 15^\circ$ then sector 1

else

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 45^\circ$ then sector 2

else

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 75^\circ$ then sector 3

else sector 4.

In quadrant 2:

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 15^\circ$ then sector 7

else

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 45^\circ$ then sector 6

else

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 75^\circ$ then sector 5

else sector 4.

In quadrant 3:

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 15^\circ$ then sector 7

else

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 45^\circ$ then sector 8

else

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 75^\circ$ then sector 9

else sector 10.

In quadrant 4:

If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 15^\circ$ then sector 1

else

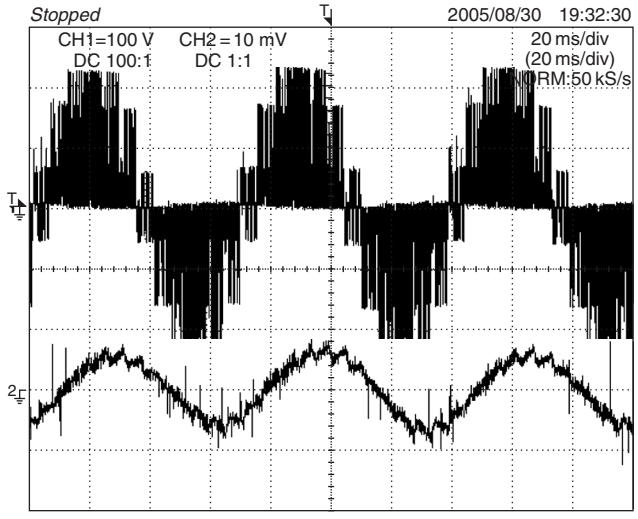
If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 45^\circ$ then sector 12

else

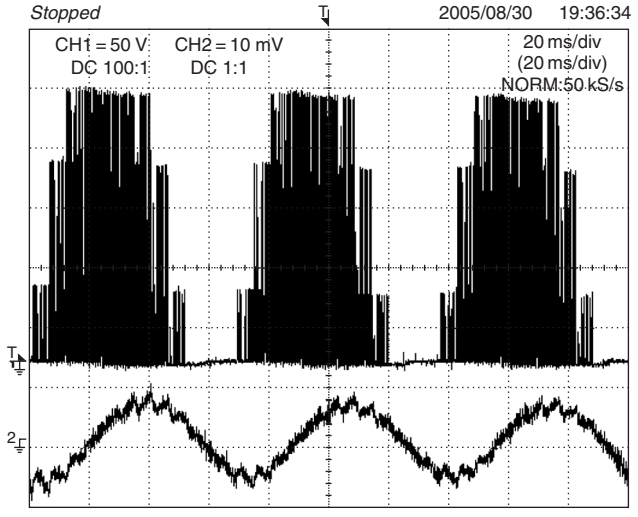
If $|v_B - v_C| \leq |v_A|\sqrt{3}\tan 75^\circ$ then sector 11

else sector 10.

For sampled v_A, v_B, and v_C the sector check for only one quadrant is always done in a sampling period, and thus the method is fast.

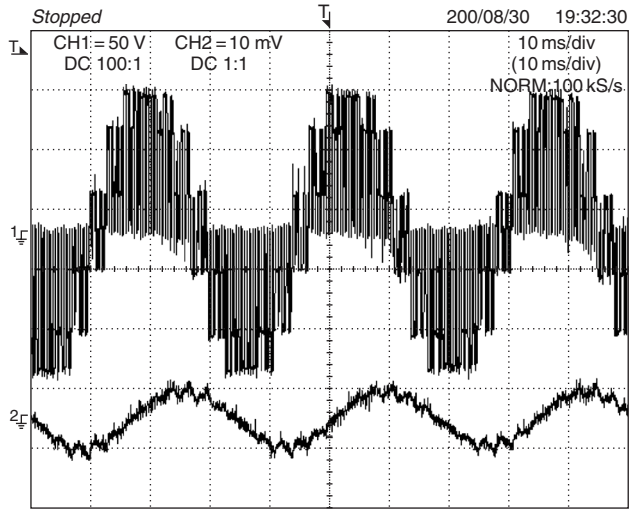


a

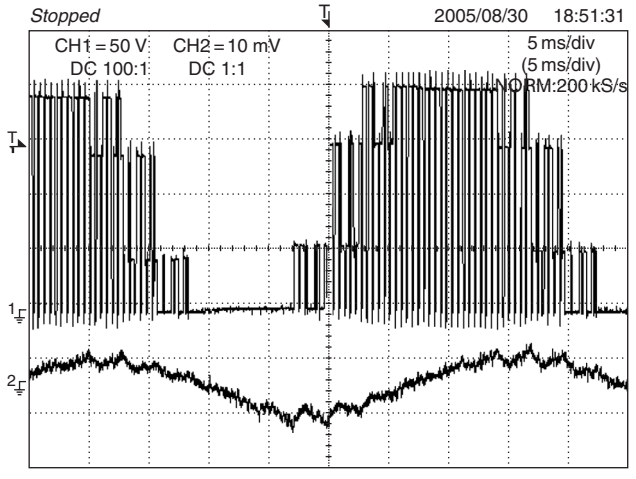


b

Fig. 4
a Phase voltage and motor current at 15 Hz
x-axis: 1div. = 20 ms, *y*-axis: upper trace: 1div. = 100 V, lower trace: 1div. = 1.5 A
b Pole voltage at 15 Hz
x-axis: 1div. = 20 ms, *y*-axis: upper trace: 1div. = 50 V, lower trace: 1div. = 1.5 A



a



b

Fig. 5
a Phase voltage and motor current at 30 Hz
x-axis: 1div. = 10 ms, *y*-axis: upper trace: 1div. = 50 V, lower trace: 1div. = 2 A
b Pole voltage and motor current at 30 Hz
x-axis: 1div. = 5 ms, *y*-axis: upper trace: 1div. = 50 V, lower trace: 1div. = 2 A

6.3 Computation of T_1 and T_2

Once the sector is identified, the computation of T_1 and T_2 are done using the (15) and (16). The gating signals for the inverters are generated by comparing the T_0, $T_0/2 + T_1$ and the $T_0/2 + T_1 + T_2$ with a triangular waveform (Fig. 2*b*). The frequency of the triangular waveform is adjusted based on the number of samples needed in a sector, depending on the output fundamental frequency.

7 Simulation results

The proposed inverter scheme has been simulated using Matlab. A total DC-link voltage of 215 V is used for the present study. The drive scheme is simulated for different speed ranges. Figures 3*a* and *b* shows the inverter pole voltage and phase voltage, respectively, for 15 Hz operation. Figures 3*c* and *d* show the pole voltage and phase voltage, respectively for 30 Hz. From the simulation study it can be noted that each leg is not switched on all the time but clamped to the zero state for 30% of the duration in a fundamental period. This can also be verified from the pole voltage levels of Fig. 1*c*. This will also reduce the inverter switching losses when compared to a conventional scheme with hexagonal voltage space vector structure. Figures 3*g* and *h* shows pole voltage and the phase voltage waveform from the proposed drive scheme for 12-step mode operation (50 Hz operation). The V/f drive scheme is run and the FFT of the waveforms taken and plotted to see the various harmonics present in the phase voltage at different fundamental frequencies of operation. The proposed inverter scheme has been studied for the fundamental component and its harmonic content for the full modulation range with various sampling periods (depending on the output fundamental frequency) as mentioned in Section 6. A linear modulation range is observed up to the 50 Hz operation (Fig. 2*c*). The relative amplitudes of various harmonic orders up to the 49th are computed for different modulation ranges (Fig. 2*d*). Note from Fig. 2*d* that the 5th

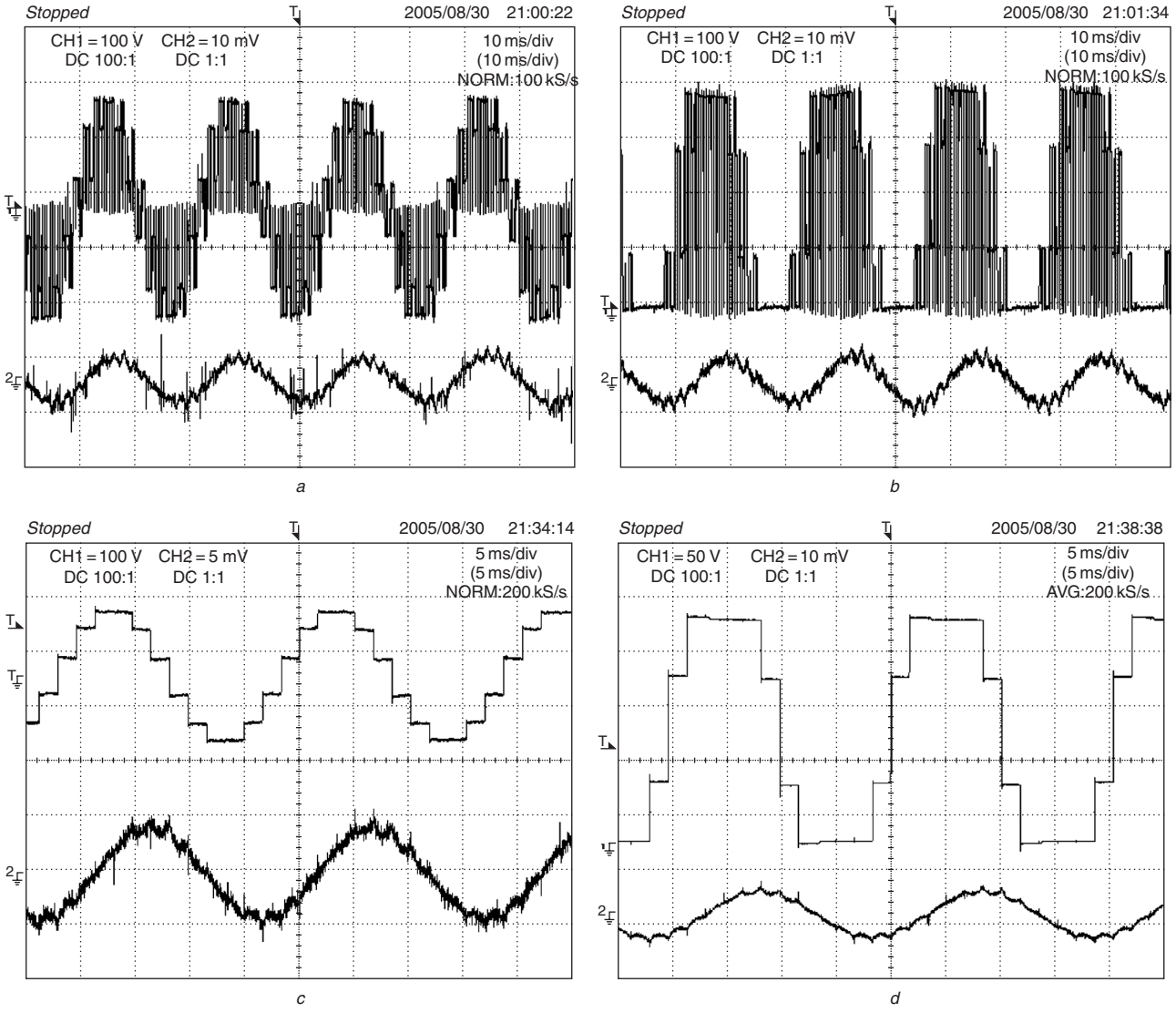


Fig. 6

a Phase voltage and motor current at 45 Hz
x-axis: 1div. = 10 ms, *y*-axis: upper trace: 1div. = 100 V, lower trace: 1div. = 2 A
b: Pole voltage and motor current at 45 Hz
x-axis: 1div. = 10 ms, *y*-axis: upper trace: 1div. = 50 V, lower trace: 1div. = 2 A
c Phase voltage and motor current at 50 Hz
x-axis: 1div. = 5 ms, *y*-axis: upper trace: 1div. = 100 V, lower trace: 1div. = 1 A
d Pole voltage at 50 Hz
x-axis: 1div. = 5 ms, *y*-axis: upper trace: 1div. = 50 V, lower trace: 1div. = 2 A

and 7th order harmonics ($6n \pm 1$, $n = 1, 3, 5 \ldots$) are absent throughout the modulation range up to 12-step mode operation (50Hz). The low-order harmonic content (11, 13, 23, 27, 35 and 37) is less than 10% of the fundamental amplitude, and the 47th and 49th order harmonics are boosted up in the output frequency range from 30 Hz to 45 Hz operation, for the present sampling technique presented in Section 6.

8 Experimental verification and discussion

The proposed scheme has been experimentally verified for a 1.5 kW induction motor drive. The space vector PWM is generated using the TMS320LF2407 digital signal processor. The output of the DSP is the sector number and signals '$T_0/2$', '$T_0/2 + T_1$' and '$T_0/2 + T_1 + T_2$'; the required gating signal for the inverter is generated using logic gates in a PAL (Fig. 2*a*). The drive scheme is operated for different modulation range under V/f control. A total DC-link voltage of 215 V is used for the experimental study. Figures 4*a* and *b* show the motor phase voltage waveform and the pole voltage waveform, respectively, along with phase current waveform for 15 Hz operation. As in the simulation study, it can be noted from the pole voltage waveform, that the inverter leg is not switched for 30% of the fundamental period of operation. The corresponding waveforms (pole voltage and phase voltage) for 30, 45 and 50 Hz (12-step mode) operation are shown in Figs. 5*a*, *b*, 6*a*, *b*, *c* and *d*, respectively. The experimental waveforms are in agreement with the simulation study. Figures 7*a–d* show the harmonic spectrum of the motor phase voltage for 15, 30, 45 and 50 Hz operation. The harmonic spectrum shows that the 5th and 7th harmonic orders ($6n \pm 1$, ($n = 1, 3, 5, \ldots$) are totally absent in the complete modulation range. So by properly selecting the number of samples in the different modulation ranges, the inverter switching frequency can be limited to within 1 kHz operation and, at the same time, low-frequency harmonic amplitudes can be highly suppressed with the total elimination of $6n \pm 1$ ($n = 1, 3, 5 \ldots$) order harmonics from the drive system.

The proposed drive gives increased modulation range (for the same voltage space vector amplitude), when compared to a conventional hexagonal voltage space vector structure. If V_{dc} is the radii of the proposed 12-sided polygonal and the conventional hexagonal voltage space vector structure, a maximum phase peak fundamental of 0.658 V_{dc} is possible from the present scheme, with the total elimination of 5th and 7th order harmonics. This can be done by finding the A phase amplitude by taking the projection of the vectors in Fig. 1*d* and computing the Fourier component. For the conventional hexagonal structure the maximum phase peak fundamental is only 0.637 V_{dc}, with high-amplitude 5th and 7th harmonic voltages.

9 Conclusions

A multilevel inverter structure with 12-sided polygonal voltage space vector structure has been proposed. The proposed inverter structure is realised by cascading conventional two-level inverters only. This will make the power bus structure simple to fabricate. An increased modulation range is possible from the proposed multilevel inverter scheme when compared to a conventional multilevel scheme, with the same DC-link voltage, for the inverter structure. A simple PWM scheme is proposed such that the modulation scheme can be realised up to 12-step mode operation. The proposed 12-sided polygonal space vector PWM scheme gives highly suppressed low-order harmonics with total elimination of the $6n \pm 1$ ($n = 1, 3, 5 \ldots$) order harmonics for the full modulation

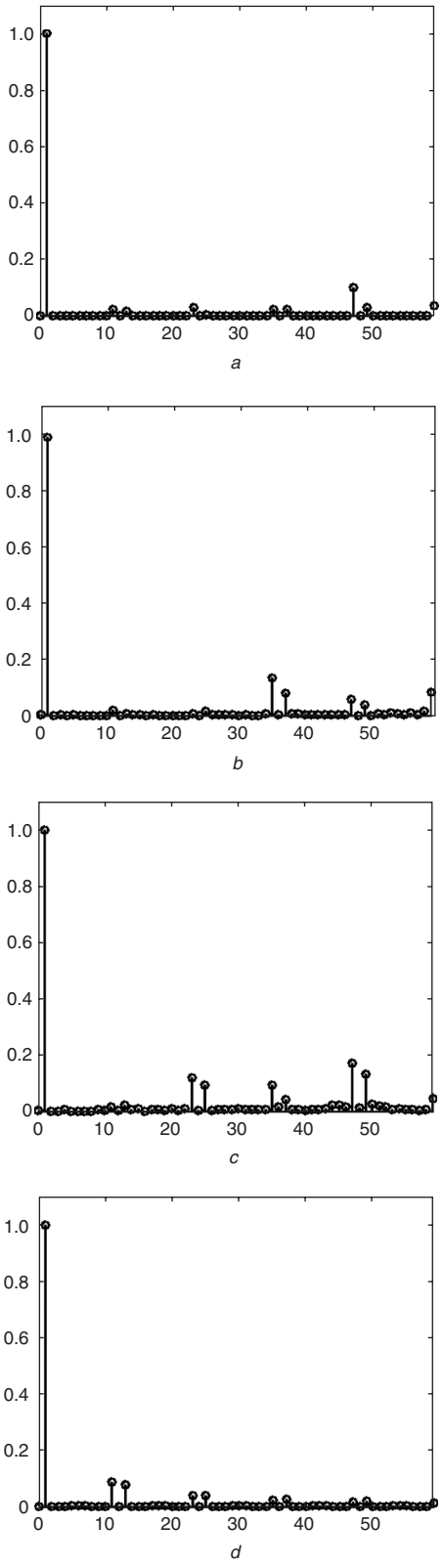


Fig. 7
a Harmonics at 15 Hz operation
x-axis: *n*th harmonic, *y*-axis: relative amplitude
b Harmonics in 30 Hz operation
x-axis: *n*th harmonic, *y*-axis: relative amplitude
c Harmonics in 45 Hz operation
x-axis: *n*th harmonic, *y*-axis: relative amplitude
d Harmonics in 50 Hz operation
x-axis: *n*th harmonic, *y*-axis: relative amplitude

range. With the highly suppressed low-frequency harmonic order, a low-frequency PWM switching can be implemented with the proposed multilevel structure (with increased modulation range), when compared to hexagonal voltage space vector based conventional multilevel inverter schemes. The present PWM scheme also ensures that the inverter pole voltages of the proposed drive scheme are not switched for 30% of the fundamental period. This will also improve the overall efficiency of the proposed multilevel inverter scheme when compared to any conventional scheme. So the proposed scheme can be considered for low-voltage and medium-voltage inverter-fed IM drive schemes for high-power applications.

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12 Appendix

Induction motor parameters: three- phase, 50 Hz, 1.5 kW

M: Magnetising inductance: 0.272 H

L_{ss}: Total stator inductance: 0.28 H

L_{rr}: Total rotor inductance: 0.28 H

R_s: Stator resistance: 2.08 Ω

R_r: Rotor resistance: 4.19 Ω

P: Number of poles: 4