"STUDY AND IMPLEMENTATION OF CMOS IO's FOR SUB MICRON VLSI CIRCUITS"

A Major Project Report

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In

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(VLSI Design)

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CERTIFICATE

This is to certify that the M.Tech. Dissertation Report entitled **"Study and implementation of CMOS I/O's for sub micron VLSI circuit"** submitted by **Tripti Bhargava (Roll no. 04MEC004)** towards the partial fulfillment of the requirements for Semester III-IV of **Master of Technology (Electronics and Communication Engineering)** in the field of **VLSI Design** of **Nirma University of Science and Technology, Ahmedabad** at **STMicroelectronics, G.Noida** is the record of the work carried out by them under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this Dissertation-Project work to the best of our knowledge have not been submitted to any other University or Institute for award of any degree or diploma.

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ABSTRACT

The objective of the work carried out is to design and implement the 2.5v IO in the 90nm technology according to the specifications required by the end user which act as an interface between the core and the off chip environment. If package is consider as one of the protective layer, then the IO frame is the second protective layer to the core Any external hazards such as electrostatic discharge (ESD) and noises should be filtered out before propagating to the internal circuit for their protection.

My work concentrates on the designing and the implementation of the output buffer as per the specification required by the end user. On the broader sense an output buffer mainly consist of the Testpin and predriver, Level shifter, Slew rate controller and the 2mAmp driver.To have the complete control over the slew rate against the varied PVT condition compensation codes from the compensation block is used .Implementation of compensation block is out of scope of thesis as it is the property of company STMicroelectronics.In the work carried out various aspects from designing to layout (taking into consideration the latch up issue) to validation have been considered. The design is basically for 90nm technology.

 The design quality of I/Os is a critical factor, which is again governed by process corners, voltage and temperature. MOSFET suffer from substantial parameter variations from wafer to wafer and from lot to lot.

Basically four corners have been defined N-fast and P-slow, N-slow and P-slow, N-fast and P-slow, P-fast and N-slow. Besides these four process corners one more process corner has been considered i.e. N-typical and P-typical which may lie some where between fast and slow. Apart from the processes, there may be change in voltage as well as temperature. So for a particular technology high value, typical value and low value of the voltages are decided on which the I/Os as well as core has to operate. Similarly the temperature range has been defined in the range of -40^oC to 25^oC to 125^oC i.e. minimum, typical and maximum respectively.

Besides designing more of the importance has been given to layouts as that is the real system which is going to operate in real world. Certain checks like design rule checks, electrical rule checks and specially latch up prevention has been kept in mind while drawing the layouts as latch up alone can kill whole design by drawing large amount of currents and hence power consumption, which is some thing the deciding factor of a good design and of course for the end user.

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COMPANY PROFILE

History

The ST group was formed in June 1987 as a result of the merger between SGS Microelettronica of Italy and Thomson Semiconducteurs of France. In May 1998, the company changed its name from SGS-THOMSON Microelectronics to ST Microelectronics. The group totals more than

- 50,000 employees.
- 16 advanced research and development units.
- 39 design and application centers.
- 17 main manufacturing sites.
- 88 sales offices in 31 countries.

STMicroelectronics is a global independent semiconductor company and is a leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications. An unrivalled combination of silicon and system expertise, manufacturing strength, Intellectual Property (IP) portfolio and strategic partners positions the Company at the forefront of System-on-Chip (SOC) technology and its products play a key role in enabling today's convergence trends.

- Corporate Headquarters, as well as the headquarters for Europe and for Emerging Markets, are in Geneva.
- The Company's U.S. Headquarters are in Carrollton (Dallas, Texas);
- Those for Asia/Pacific are based in Singapore; and Japanese operations are head quartered in Tokyo.

ST is one of the world's largest semiconductor companies

- In 2003, ST's net revenues were US$7.2 billion and net earnings were US$253 million.
- ST is also the world's leading supplier of analog ICs, MPEG-2 decoder ICs, and ASICs/ASSPs overall.
- Additionally, in the memory market, ST is ranked fourth in NOR Flash ICs.
- ST is number one for ICs in set-top boxes.

- At number two in smart cards, in hard disk drives, and also in xDSL chips.
- At number three in wireless semiconductors and also in automotive.

The Company's products are manufactured and designed using a broad range of fabrication processes and proprietary design methods. To complement this depth and diversity of process and design technology, the Company also possesses a broad intellectual property portfolio that it has used to enter into cross-licensing agreements with many other leading semiconductor manufacturers.

ST has developed a worldwide network of strategic alliances, including product development with key customers, technology development with customers and other semiconductor manufacturers, and equipment and CAD development alliances with major suppliers. By augmenting its rich portfolio of proprietary technologies and core competencies with complementary expertise from a variety of carefully chosen strategic partners, ST has developed an unsurpassed capability to offer leading-edge solutions to customers in all segments of the electronics industry. The Company currently offers over 3,000 main types of products to more than 1,500 customers.

- Customers: Alcatel, Bosch, DaimlerChrysler, Ford, Hewlett-Packard, IBM, Motorola, Nokia, Nortel Networks, Philips, Seagate Technology, Siemens, Sony, Thomson and Western Digital.

Approximately two-thirds of ST's revenue is derived from differentiated products, a combination of dedicated, semi-custom and programmable products designed to suit a specific customer or a specific application and therefore having high system content. This result reflects ST's exceptionally early recognition of the importance of system-on-chip technology, which is the key for addressing the fast growing market for convergence products, and the success of the strategies it developed to ensure its leading position in this key emerging field.

ST's commitment to environmental responsibility has resulted in substantial reductions in the consumption of energy, water, paper and hazardous chemicals, increased recycling of waste products and a significant cut in CO_2 emissions.

In 1999, ST received the United States Environmental Protection Agency's Climate Protection Award for its outstanding accomplishments in protecting the Earth's climate. In 2000, ST was ranked first in environmental management among 14 semiconductor

companies by Innovest Strategic Value Advisors and received the only AAA ranking in eco-efficiency. Also in 2002, ST received the Seal of Sustainability from the Sustainable Business Institute and ST's back-end Malta plant received the Management Award for Sustainable Development as part of the European Awards for the Environment 2002, organized by the European Commission Directorate-General Environment. And most recently, ST was awarded the 'Best Industrial Renewable Energy Partnership' as part of the European Commission's Campaign for Take-Off for Renewable Energy Awards 2003.

Chapter 1

INTRODUCTION

1.1 What are I/O's?

I/O is the specially designed element, which acts as an interface between core signal and off chip environment. A chip can be divided into two main parts:

1) Core

2) I/O's

Any input signal, which comes from off chip device, has to be checked by the I/O for any discrepancy in its behavior other than the defined for the core and if it finds any characteristic of the signal, which can damage the core, it either modifies the signal or simply rejects it. It also checks the signal going from core to the outside world. So I/Os are responsible for proper functioning of the entire chip and guard the core. Thus however efficient the core design may be, it is the I/O, which determines the efficiency of the chip. It is necessary for the designer to analyze the designed I/O under the practical conditions to verify the deriving strength of the chip, delay in signal, power etc. as they all are heavily dependent on the I/O irrespective of whether the core is compliant with the specifications or not. Because even a minor difference in the performance of the I/O than the desired one can damage the whole circuit or even can cause problems to the off chip circuit, it is the responsibility of the I/O to limit the outgoing signal in all respects like amplitude, frequency, delay etc. (under the specified range), for proper functioning.

Today the I/O structures probably require the most amount of circuit design expertise along with detailed process knowledge [6]. A system designer cannot afford to contemplate I/O pad design and hence has been established the importance of a well characterized I/O library for the process being utilized Any I/P signal which comes from off-chip environment (external voltage are at a typical voltage Vdde level of 2.5V, 3.3V or 5V) into the chip, must be checked by I/O for any discrepancy. I/O acts as protection

device for the core. I/O also scans the signal which is going from core to off-chip world. Typically I/Os are placed at the periphery of the core logic i.e. on the sides of the core logic, except on the corners of the cell. They are placed parallel to one another (abutted together using filler cells) and vertical to the enclosure containing the core. Also corner cells are used. This helps in maintaining the power ring continuity throughout the cell, which is very important for uniform distribution of the power to all the I/O inside the chip. [23]
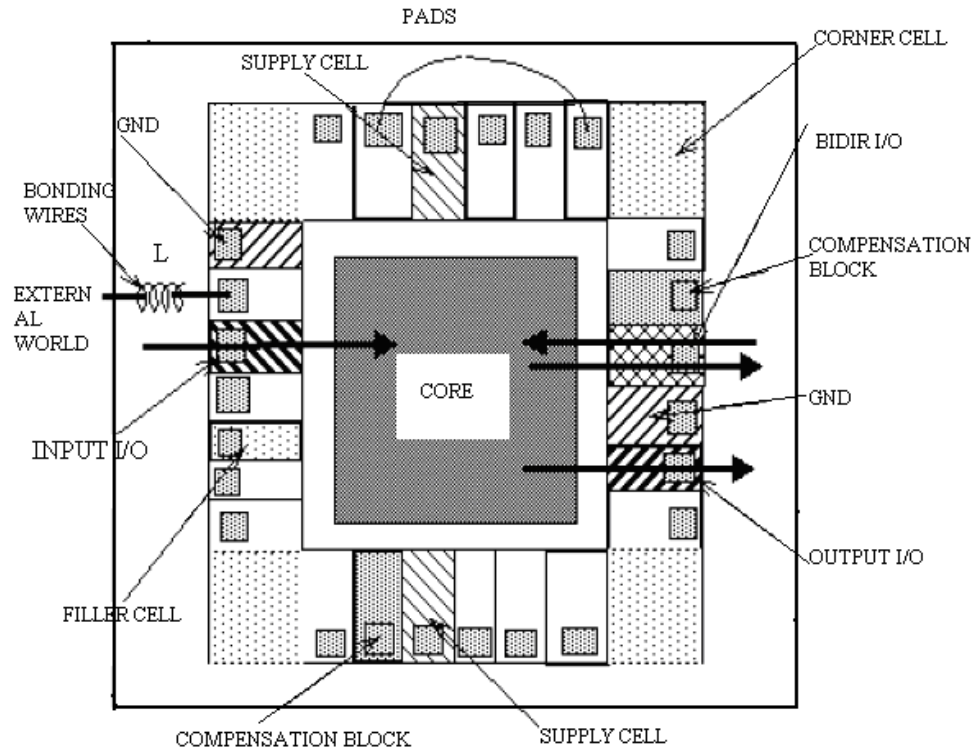
Figure 1.1 Input/Output and core in a chip

Uniform distribution of power is necessary, as the I/Os are placed all over the periphery and due to large distances between them there is high chance of the power getting degraded, which means I/Os will get power in a broader range than the required one. For e.g. the actual voltage received by one buffer could be 2V and for another one 2.5V

Here in CR&D G.NOIDA, general purpose I/O's are designed which can be used for a wide range of applications if they are meeting the required specifications.

Chapter 2

STANDARD I/O LIBRARY

A Standard I/O library consists of the following components:

- Input Buffers
- Output Buffers
- Bidirectional Buffers
- Compensation cell (If the library contains the active slew rate control buffers)
- Supply cells
- Voltage reference generators
- Leaf cells that constitute above cells

2.1 INPUT BUFFERS

An input buffer couples the external off chip signal to the core elements of the chip. Since the external signal can have voltage ranges much beyond the normal CMOS operating voltages, an input ESD protection is required for these buffers. The non-destructive breakdown of diodes is utilized to clamp the voltage between Vdd and Vss.The resistor tends to decrease the current reaching the gate of devices. The only disadvantage is the introduced RC delay (each diode introducing a capacitance) to the input of the circuit. The design has to be optimized if used in high-speed circuits. ESD protection for buffers today has a major role to play in the efficient chip design. After passing through the ESD block, the signal is applied to the I/P buffer. A typical I/P buffer may be divided into three main stages as represented by the block diagram

```
From ──▶ ┌──────────┐  Signal at  ┌──────────┐  Signal at  ┌──────────┐
Pad      │ Schmitt  │ ──────────▶ │  Level   │ ──────────▶ │ Buffer To│
         │ Trigger  │  Vdde level │  Shifter │  Vdd level  │ Set Drive│
         └──────────┘             └──────────┘             └──────────┘
                                                                │
                                                         To core signal
                                                                ▼
```
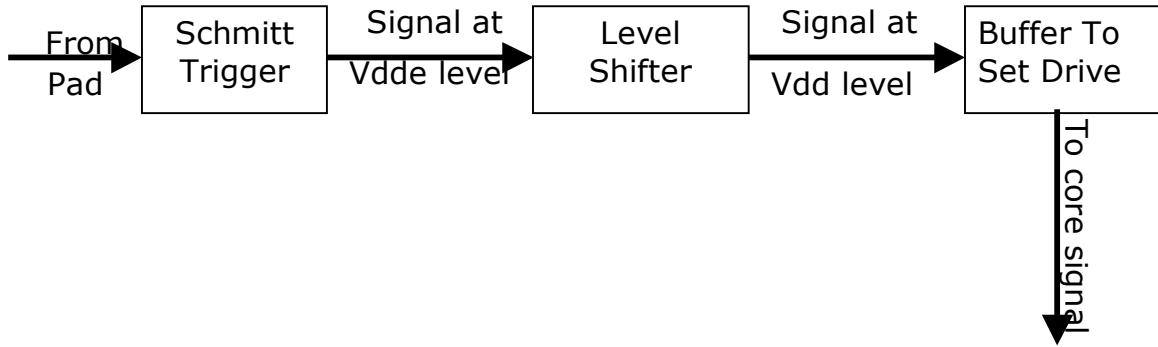
Figure 2.1 Block Diagram of Input Buffer

2.1.1 ELECTRO STATIC DISCHARGE (ESD)

Electrostatic Discharge, in short ESD, protection is very important to save the chip from unwanted voltage which gets developed at the pin due to some source coming in contact with the pin. These large accumulated charges can destroy the transistor, so a mechanism is needed which can effectively and quickly discharge this unwanted accumulated charge [17]. And here again the importance of metal rings comes into picture as they discharge accumulated charges and protects the chip. Care should be taken that there are no acute angles in the metal layers as they could be a potential areas of hotspots.

An I/P buffer couples the external off chip signal to the core elements of the chip.

Since the external signal can have voltage ranges much beyond the normal CMOS operating voltages, an I/P ESD protection is required for these buffers. Non-Destructive break down of diodes is utilized to clamp the voltages between VDD and VSS. The resistor tends to decrease the current reaching gate. But this block introduces RC delay; hence the design has to be optimized, if used in high-speed circuits.

There are 3 types of ESD stress models [19]

1. Human Body model:

When a charged person touches packaged device, it results in discharge of the charges accumulated at pins when his finger comes in contact with pin, with peak current in Amps of about 100ns duration.

For HBM following factors are important:

Human body capacitance (= 100pf)

- Charging potential (2KV)

- Finger resistance (which limits current in circuit) = 1.5Kohm

2. Machine model:

When a machine, which could be a solder iron, bonding machine etc. comes in contact with the pin, charges from the tip of the machine gets transfer to the pin, which results in large current.

In this model, resistance which limits peak current through circuit is much lower (25ohm) so RC time constant is small which leads to higher peak current (3-4 amp) as compared to HBM.

3. Charged device model (CDM):

In this, ESD event occurs when electro statically charged device (i.e. charge is stored in DUT, Device under Test, itself) is abruptly discharged to ground. CDM pulse has very fast rise time so protection device should turn on fast. Only thermal damage occurs in CDM while both thermal damage & oxide rupture occur in HBM & MM.

Reason for thermal damage:

Flow of high current through circuit results in energy dissipation, which leads to thermal damage.

NMOS ESD Phenomena:

For ESD protection, NMOS transistor is used whose drain is connected to PAD. Now if ESD event occurs, it injects minority carrier (holes) in the drain, which leads to substrate current by avalanche phenomena. There is parasitic bipolar with drain as collector, substrate as base, source as emitter. Initially the leakage current flows from drain to bulk via P well, which offers some resistance. The drop across this P well resistance is nothing but voltage across base and emitter of the NPN. As soon as it becomes more than threshold voltage of BJT, the parasitic bipolar turns on. In VI curve it is indicated by snapback region, which starts at (V_{t1}, I_{t1}) and is followed by second breakdown point $(V_{t2}.I_{t2})$ where thermal damage occurs. I_{t2} depends on following parameters:

- Heating at drain junction

- Junction depth

- Substrate resistance

- Channel length & finger width

For ESD protection another simple circuit which we use is a diode with one terminal at the pad and other at vdde i.e. the IO cell operating voltage, say 3V3. Under normal condition this diode is reversed biased but if there is some ESD activity the diode will become forward biased and will provide this spike a least resistance path to another very large dimensioned MOSSWI to ground.
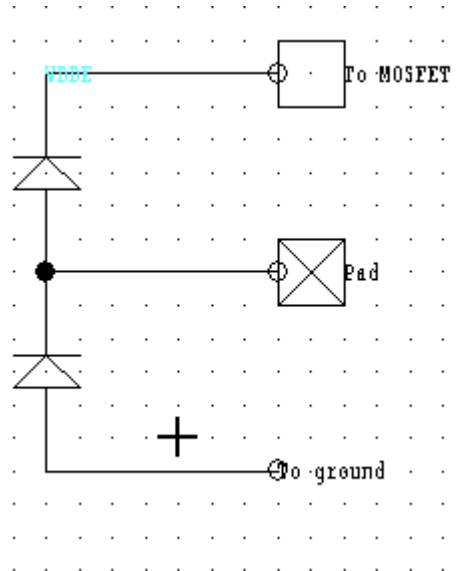
Figure 2.2 ESD protection circuit

In the layout we have these diodes as close to the pad as possible. Even the output driver section made of NMOS and PMOS transistors are also close to the PAD. We have two types of diodes in fabrication DP and DN.

> • DP diodes are diodes in which we have an outer N-well ring and a P+ inside it.

> • DN diodes we have P+ as the outer ring and N+ inside it.

Though these diodes are in no way different from the functioning point of view,it is just the fabrication difference. The diode used by the 5V tolerant library for ESD protection leads to formation of these parasitic transistors, which cause latch-up. The IO buffers will work on a supply of 3.3V (+/-10%), but capable of withstanding standard 5V (+/- 10%) signals at the pad.

Effect of Higher voltages on transistors

When 5V on the PAD, the following effects occur: [19]

- **For NMOS:**

  - **Hot electron effect:** When 5V on the drain of NMOS, the electron coming from the source may acquire such high energy that they can penetrate the insulting layer of SiO_2 (i.e. they cross the potential barrier of SiO_2 layer) which will affect the threshold voltage of transistor, in other words will change the characteristics of transistor.

  - **Gate -oxide stress potential**: When 5V comes on the PAD, the V_{ds} of NMOS will be 5V, which cross the stress limit (=4V) so transistor becomes stress.

- **For PMOS:**

  - **Flow of substrate current:** In case of 5V on the PAD, the diode formed between the p+ of PMOS and the substrate n+ of PMOS becomes forward biased so there will be flow of substrate current pad, without damaging the input/output MOSFETS. For ESD protection of FT libraries, we have this diode when the n-type substrate is at floating potential i.e. VDD5 so if there is a spike greater than 5V on the PAD the diode will be forward biased and will provide a discharge path through MOSSWI which is a very big transistor and provides the ground path.

2.1.2 FILLER AND CORNER CELLS (P&R CELLS)

These cells are used for continuity of metal rings which is responsible for uniform distribution of power, ESD protection, and N well closing to prevent latch up. Latch up may be prevented into two basic ways:

1.*latch up resistant CMOS process* – in this method, the substrate is doped with varying degree of doping, bottom is highly doped where as the upper portion is lightly doped compared to bottom. This reduces the parasitic resistance offered by the n well and the substrate; hence reduce the gain of the O/P.

2. *Layout technique* – in this method, P+ substrate of NMOS transistor is surrounded by the N well of the PMOS transistor by collecting minority carriers and preventing them from being injected into the respective bases.

2.1.3 PADS

Pads are basically a sandwich of various metal layers used in the design. The pad consists of pins and metal connections on all sides to provide the power connection to both the core and I/O elements. Multiple power pads are often used to reduce the noise. The internal elements of the I/O circuit being connected to one power pad while the external elements, the circuit part which will have interface with the off chip elements being connected to a different power pad. A metal layer at the bonding pad finally shorts all the power pads. The noisier power pads, the one connected to the O/P transistor are separated from the substrate to prevent the noise coupling through the substrate.

2.1.4 SCHMITT TRIGGER

This circuit is used to generate clean pulses from a noisy input signal by providing hysteresis. The basic principle employed for such circuit is the different switching thresholds signals going from 'LOW' to 'HIGH' and 'HIGH' to 'LOW'
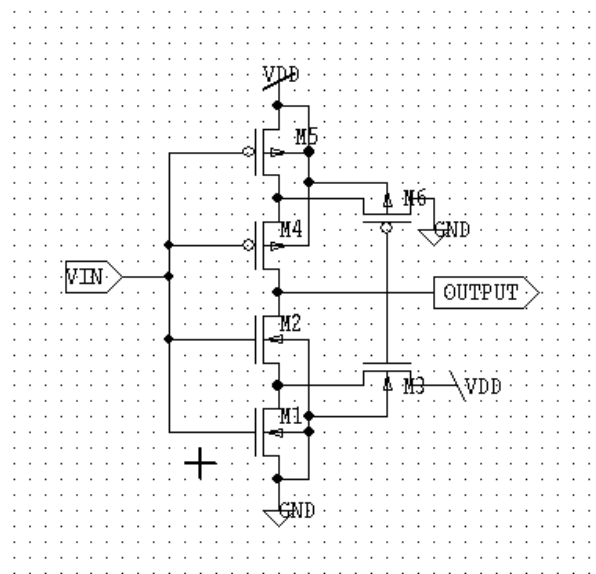
Figure 2.3(a) Standard Hysteresis Circuit

WORKING:

We can divide the circuit into two parts, depending on whether the output is high or low. If the output is low then M6 is on and M3 is off and we are concerned with the p-channel portion when calculating the switching point voltages, while if the output is high, M3 is on and M6 is off and we are concerned with the n channel portion. Also if the output is high, M4 and M5 are on, providing a DC path to VDD. [16]

Lets begin our analysis of this circuit, assuming that the output is high (=VDD) and the input is low (=0V). MOSFETs M1 and M2 are off while M3 is on. The source of M3 floats to VDD-Vt,n. With Vin less than the threshold voltage of M1, source of M3 remains at approximately VDD-Vt,n. As Vin is increased further, M1 begins to turn on and the voltage, source of M3 starts to fall towards ground. As M2 starts to turn on, the output starts to move towards ground, causing M3 to start turning off. This in turn causes the source of M3 to fall further, turning M2 on even more. This continues until M3 is totally off and M2 and M1 are on. This positive feedback causes the switching point voltage to be very well defined. The curve characteristic of the Schmitt is shown in figure 2.3(b).

2.1.5 - LEVEL SHIFTER

Core circuit works at a voltage of 1.2V (typical) whereas the signals come at higher voltage levels so in order to apply these signals to core we need to lower the voltage level with the help of level shifters.

Working

When input is high Nmos-1 (as shown in figure 2.4) will be on and will try to pull down the gate of transistor 4,hence turning it on and simultaneously transistor 2 will be off so the potential at out1 is high and hence transistor 3 is off and as transistor 1 is on, potential at OUT2 is low.
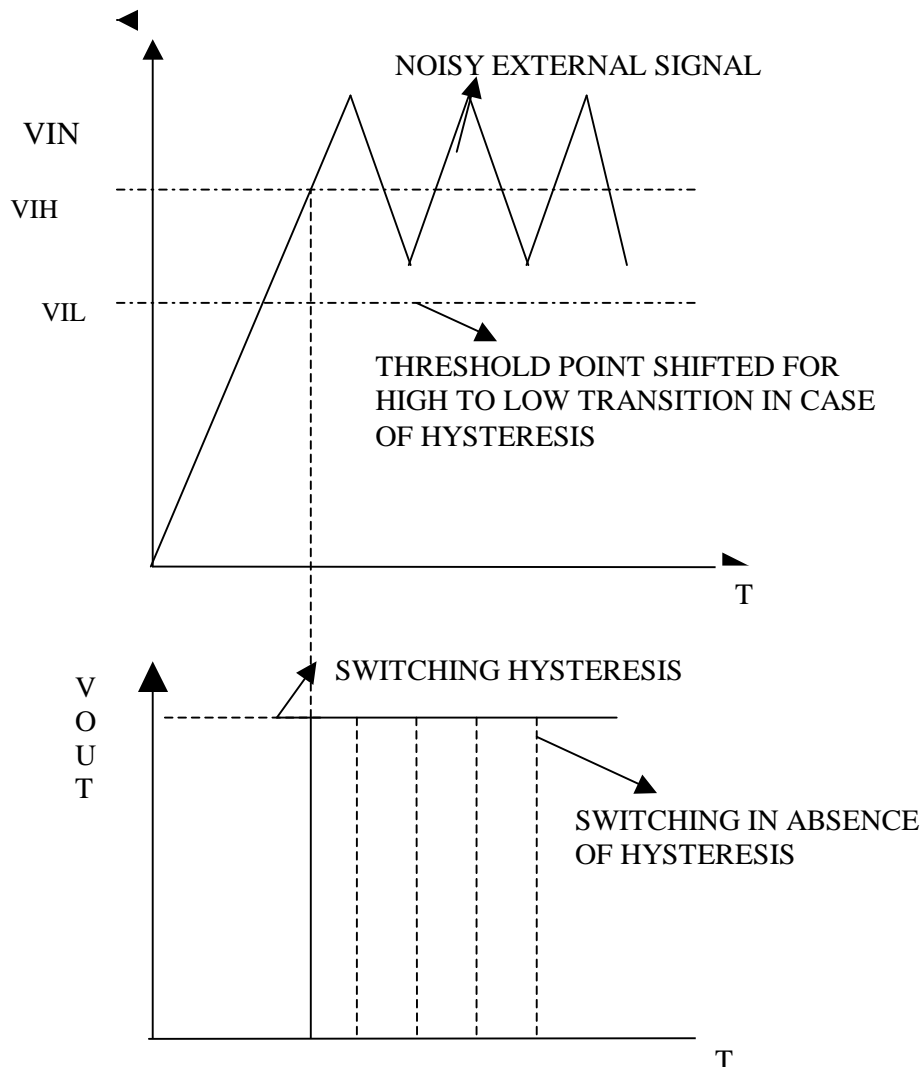
Figure 2.3(b) Demonstration of Noise Decoupling With Hysteresis
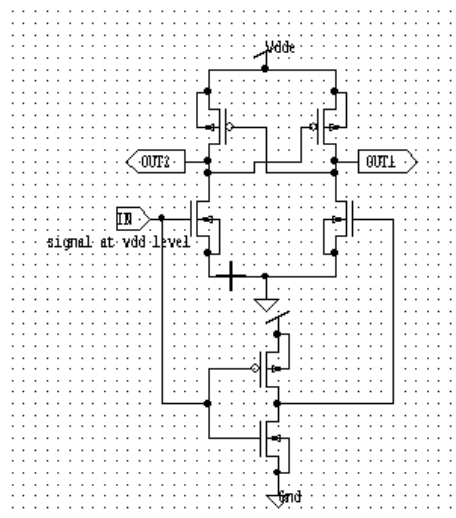
Figure 2.4 level shifter

2.1.6 - INPUT DRIVER

It is used to set drive i.e. the current capability to charge the load capacitor to the desired value in given time. Circuit is designed in such a way that the aspect ratio (W/L) which is inversely proportional to resistance, of the transistors used in input drive section, has a value which in turn returns the required time constant. Input buffers are available with two possible drives towards the core

- Normal drive which is equivalent to an X4 drive in the standard digital library. These cells are characterized with internal loads up to 80 standard loads i.e. 0.72pF.

- High drive which is equivalent to an X16 drive in the standard digital library. They are characterized with loads up to 316 standard loads i.e.2.84pF.

2.2 OUTPUT BUFFER

These interface the outgoing signals from the core to the off chip environment. Hence these are used to drive large capacitive loads which arise from long interconnect lines such as clock distribution networks, high capacitance fan out and high off chip loads. The drive capability of such a buffer should be such as to achieve the requisite rise and fall times into a given capacitive load. Normally the drive capability of I/O buffers is as high as 8 mA. By driving capability, it means that the output buffer can source or sink the specified amount of current in the worst case.
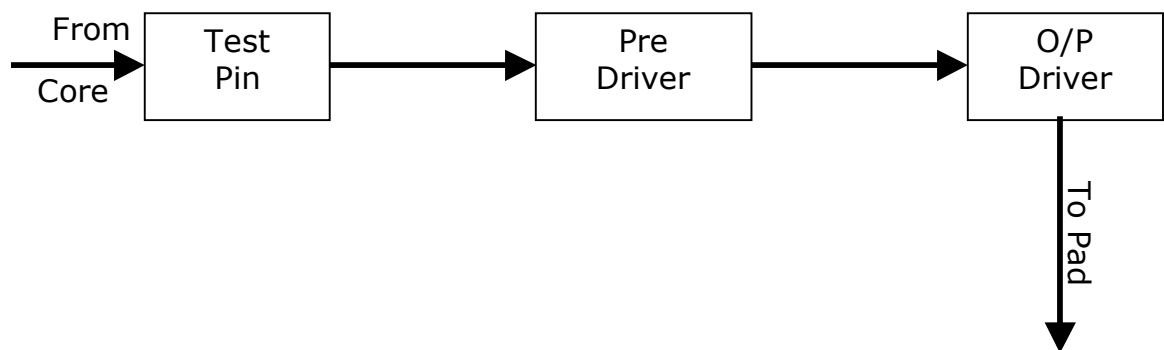
Figure 2.5 Block diagram of output buffer

2.2.1 TESTPIN & PREDRIVER

This is connected between the core and Slew Rate Controller. It is basically comprised of multiplexer and chain of inverters It works in two modes test mode and basic operating mode. And multiplexer is there to select test or basic operating mode. The multiplexer is followed by the series of inverter to generate two signals NIN and PIN for slew rate control. Signal at NIN rises faster than PIN signal and signal at PIN falls faster than NIN signal. This is done to ensure that the O/P drivers transistors should not have large dynamic current
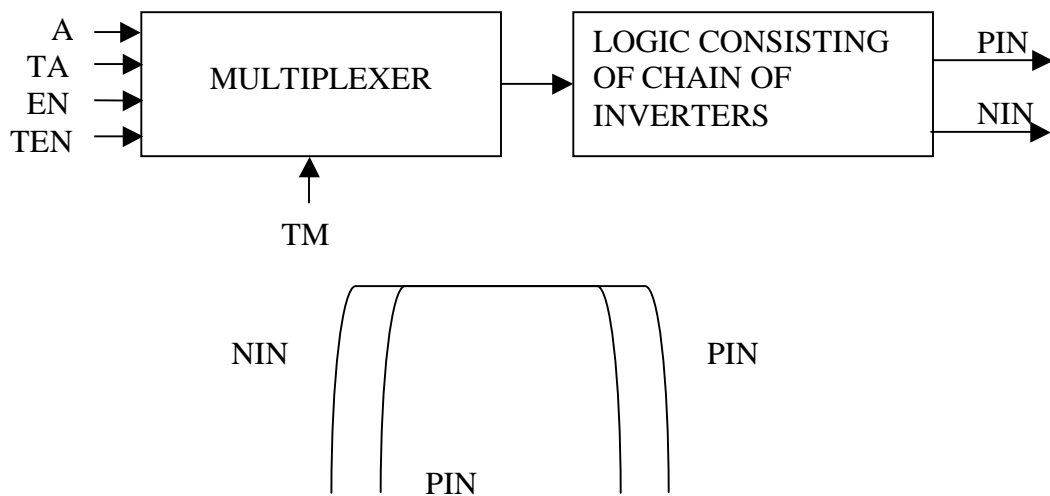
Figure 2.6 – Block diagram demonstrating Test pin and pre driver

TM =1, buffer goes in test mode

TM =0, Normal operation

A: input data coming from the core and is transmitted to PAD

EN: input enable pin to enable the O/P section

TA: input test mode data pin

TEN: input enable pin, to enable the O/P section when it is in test mode.

Mode	TM	TEN	en	TA	A	NIN	PIN
NORMAL O/P MODE	0	X	0	X	A	A	A
NORMAL I/P MODE	0	X	1	X	X	VDD	0
TEST MODE FOR O/P BUFFER	1	0	X	TA	X	TA	TA
TEST MODE FOR I/P BUFFER	1	1	X	X	X	VDD	0

Table2.1 - Functionality of Test Pin Block

2.2.2 SLEW RATE CONTROLLER

Inductance introduced by the package pins and transmission wires introduce noise, which is the inductive voltage, in the signal. A fast transition of the signal at the output pad tends to introduce frequencies in UHF range into the off chip load.

To reduce noise, we generally control the switching which reduces the rate of change of current at the output *e=Ldi/dt, e* = inductive voltage, *L* = inductance of pins and wires, *di/dt = rate of change of current.* Slew rate control circuits thus artificially limit the rate of current. One way to achieve this is by breaking the output driving transistors into a series of parallel transistors and switch the stages sequentially one after the other with some delay [18]. The slew rate control circuit consists of a series of NAND and nor gates which are driven by PIN and NIN signals respectively. As there is sequential delay in both NAND and NOR chain, thus they drive the series of output transistors sequentially. This results in total controllability over the rate of change of output current and hence slew rate can be controlled. These slew rate controllers are hard coded so they are unable to counter PVT variations in slew. So to compensate for the change in slew rate in changing PVT conditions, codes are fed through a compensation block which generates the code according to the conditions. Compensation block has only an enable pin and the output pins. This block senses the change and generates a common code for the entire slew rate controlling devices. If in special cases we require different slew rate for different I/O some modification is done at the cell level by adding special circuitry, which modifies the code generated by the compensation block.
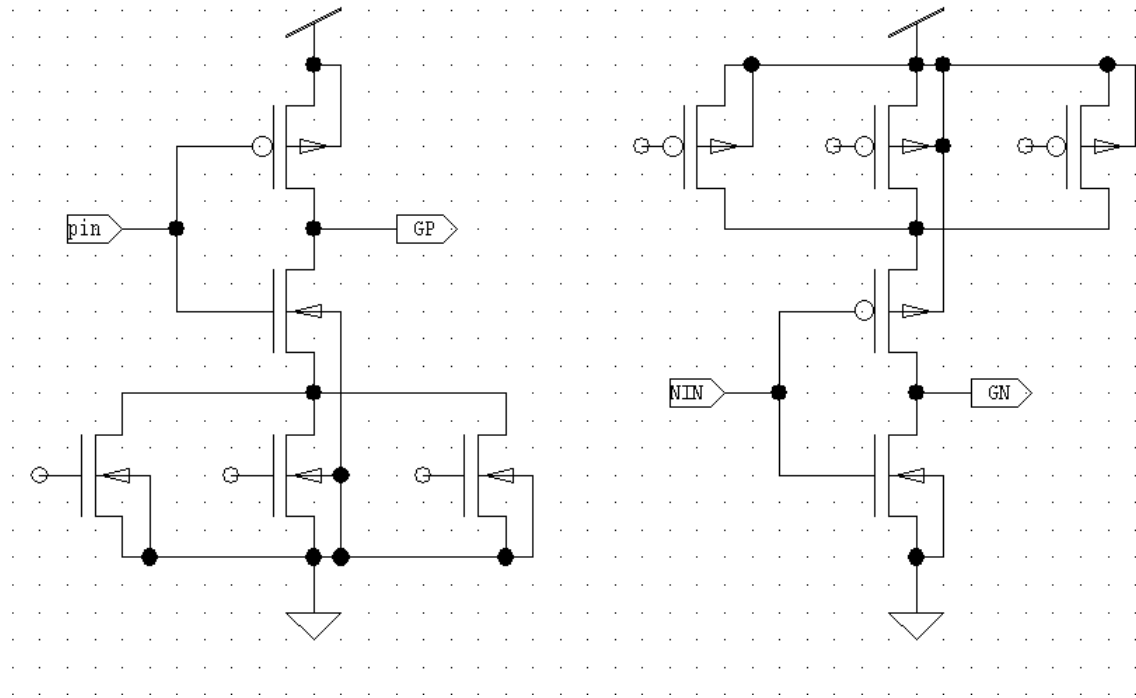
Figure 2.7 Slew Control Block

GP and GN are signals, which are connected to the gate of PMOS and NMOS of O/P drivers respectively. So to control the rate current signal at the O/P pad, we control the switching of these O/P transistors i.e. conditional GP and GN signals. Since GP is connected to PMOS so the falling edge of GP is made slow which implies that rising edge of PIN signal has to be controlled i.e. made slow, so NMOS of driver in the slew block is made weak (increasing the length of NMOS) by connecting NMOS in series, similarly to control the GN connected to the NMOS of O/P driver, PMOS is connected in series with PMOS of driver in the slew block (increasing the length of PMOS) to control the rising edge of GN signal.

In most applications, slew gets affected due to change in PVT's condition, than a series of NMOS and PMOS is connected in parallel instead of one NMOS and PMOS. The gates of those transistors are controlled by the codes generated by compensation block. Depending upon the PVT condition, compensation block generate codes which decides the number of parallel connected transistors to turn on, then these combined transistors condition the signal connected to the gate of O/P transistors of drivers which in turn controls the rise and fall of the voltage/current at the O/P pad.

2.2.3 - OUTPUT DRIVER

An output buffer must have sufficient drive capability to achieve adequate rise and fall times into a given capacitive load. Drivers are nothing but series of inverter, which sink or source current. Their size depends upon the desired drive strength [3].

The O/P drivers are divided into N inverters, the gate of which is permanently tied to the signal coming from the slew control block, thus this driver decides the current sourcing/sinking capability in best conditions. The gates of other inverters are connected to the signal coming from the slew block through the pass gates, which are controlled by TSASRC codes, which are generated, by the compensation cell. Depending upon PVT condition, compensation will generate the TSASRC codes and these codes select the number of drivers connected in parallel i.e. depending upon PVT condition the driver size are changed which control the falling edge of current at the pad.

To achieve the specified functionality of the output buffer, different types of output stages are used.

1. Push-Pull Stage

A push pull stage consists of p and n transistors at the output pad for sourcing and sinking respectively where each of transistors is controlled through a different chain of tapered inverters fed after buffering. This has two advantages:

        1) No direct gate contacts of the two output driver transistors

        2) Static and short circuit power dissipation can be avoided by bifurcating the inverter chain in such a way such that while sourcing current at the O/P pad, NMOS driver is made off before PMOS is on and vice versa.

2. Open Drain Output Stage

This has an advantage over the push pull, and that is, it has just one driver stage. Such configuration avoids gate source-drain capacitance, thus making it faster than push pull. But this configuration can either sink or source current at a time, which limits its usage. The output state of the pad can also be driven to tristate and can be connected to buses where high impedance state is required for data transfer. This is mainly used in buses.

3. Push Up/down Stage

Often the tristated output is put to a particular logic level instead of letting the bus float. Either logic low or high can be made at the output using the pull up or pull down

transistors Normally the NMOS transistor is used for pull down and PMOS transistor for pull up. But the strength of the transistor is so chosen that when a logic level appears at the output from core, it must overcome the pulling up or pulling down action.
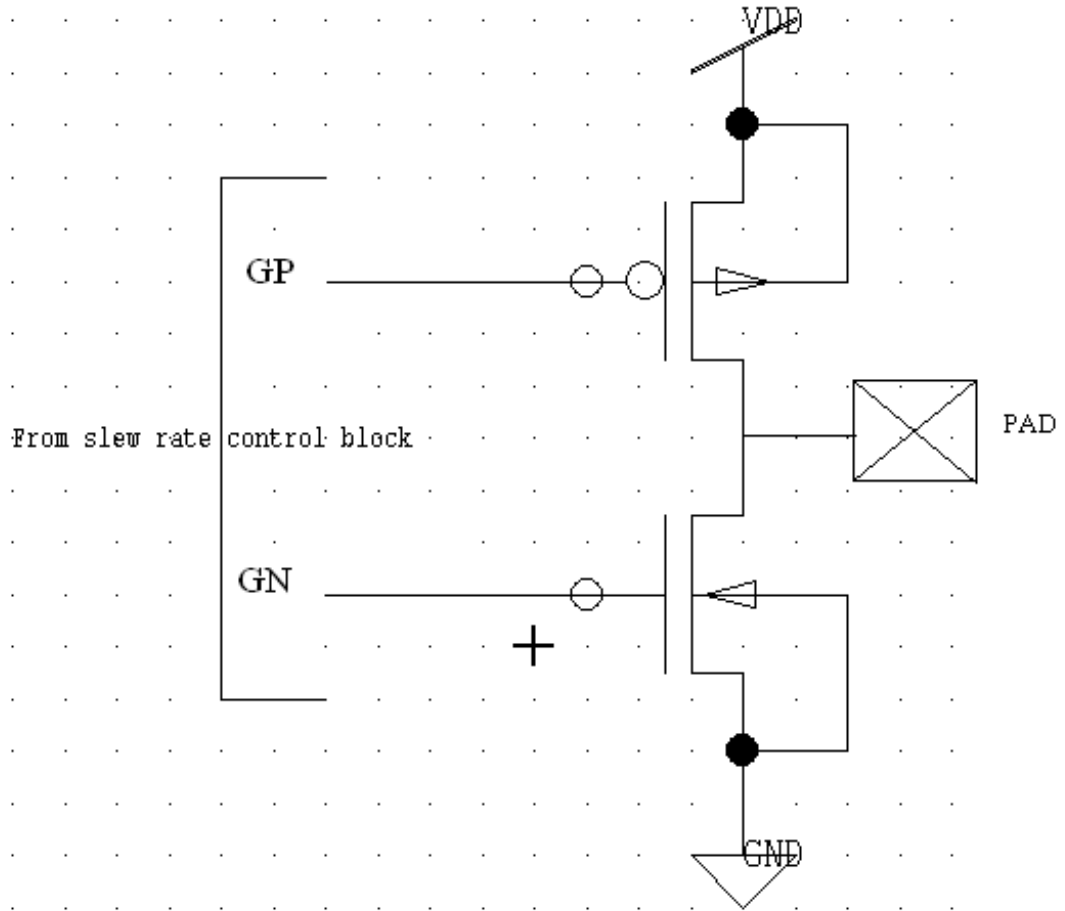
Figure 2.8 Output Drivers

2.3 - BIDIRECTIONAL BUFFER

This contains both input and output buffers and signal can enter as well as leave the core as shown in figure 2.9.

Advantage of input buffers or output buffers over bidirectional buffers is that due to smaller circuitry in them there is less leakage current.

In standard libraries, the end user is provided with both so that it can be used as per the requirement.
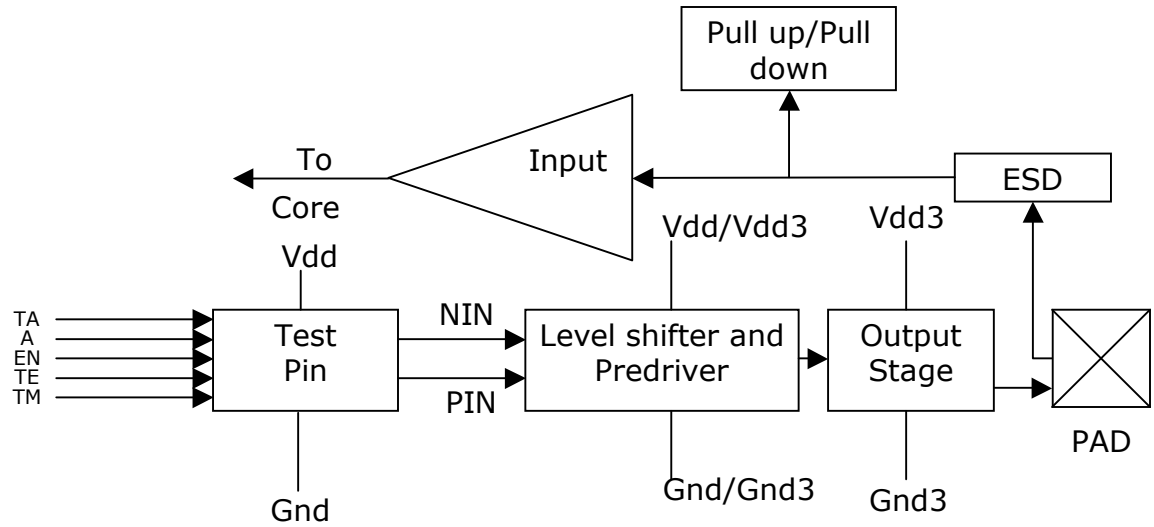
Figure 2.9 Block Diagram of Input Output Buffer

2.4 ABOUT I/O LIBRARIES

A standard library contains the above-explained cells. Each of the above mentioned categories might have different number of cells each pertaining to different specifications.

Each of the I/O libraries is identified by its nomenclature. Input buffers, output buffers and bidirectional buffers have got their own way of nomenclature as mentioned in table 2.2. [23]

INPUT BUFFER		OUTPUT BUFFER		BIDIRECTIONAL BUFFER	
IBUF	CMOS I/P buffer	B	Push pull O/P buffer	BD	Bidirectional buffers
TLCHT	TTL for I/P buffer	BT	Tri state O/P buffer	1st suffix	Drive capability in mA
SCHMT	I/P Buffer with Hysteresis			2nd suffix	H for high drive I/P stage
1st suffix	T for TTL levels, C for CMOS levels	1st suffix	Drive capability in mA	3rd suffix	ZI for tri state I/P stage, AI for gated I/P stage
				4th suffix	S for schmitt trigger on I/P
2nd suffix	H for high drive I/P stage	2nd suffix	C for CMOS (Absence of C=TTL)	5th suffix	T for TTL levels, C for CMOS levels
3rd suffix	AI for gated I/P	3rd suffix	R for slew rate control, AR for active slew rate control	6th suffix	R for slew rate control, AR for active slew rate control
4th suffix	U for active pull up	4th suffix	OD for open drain	7th suffix	OD for open drain O/P
	D for active pull down			8th suffix	U for active pullup, D for active pull down
5th suffix	Q for switch on pull-up down	5th suffix	P for test functions	9th suffix	Q for switch on pullup/down
6th suffix	_TC for x V capable	6th suffix	_TC for x V capable	10th suffix	P for test functions
	_FT for y V tolerant		_FT for y V tolerant	11th suffix	_TC for x V capable _FT for y V tolerant
7th suffix	ISO for isolated from substrate	7th suffix	_ISO for isolated from substrate	12th suffix	_ISO for isolated from substrate

Table 2.2- Nomenclature of Buffers

z

Chapter 3

DESIGN STRATEGY

3.1 Design of I/O elements

In the design of Input/output buffers, there are some critical aspects, which have to be taken into consideration at various design levels. Main focus will be on designing the circuit for hysteresis, ESD protection circuit, Driver (simple inverter) and Current buffer with Xma driving capability (where X is any number in suitable range) and certain aspects regarding active slew rate control will also be discussed.

3.1.1 Hysteresis

Hysteresis is often required in input buffers to decouple the noisy external signal from the core circuitry of the chip [4]. For a noisy external signal we desire that the buffer doesn't switch it's state due to noise. We should have a margin for the noise considerations as shown in the figure 3.1. As long as the signal doesn't go below Vilhyst the o/p doesn't change. So you have a margin of Vihhyst - Vilhyst. Normally, without hystersis it will start changing as soon as the voltage goes below Vihhyst (in this case).

The basic principle employed for such circuit is the different switching thresholds for input signals from low to high and high to low transtions ie, when we apply low voltage to the i/p and ramp it up to the high level the threshold point comes say at a point Vin = Vilhhyst. Simmiliarly when we apply a high voltage at the i/p and decrease it the threshold point comes at point Vin = Vihlhyst . We need these points to be different such

that   Vilhhyst>Vihlhyst   as   shown   in   the   figure   3.1   below.
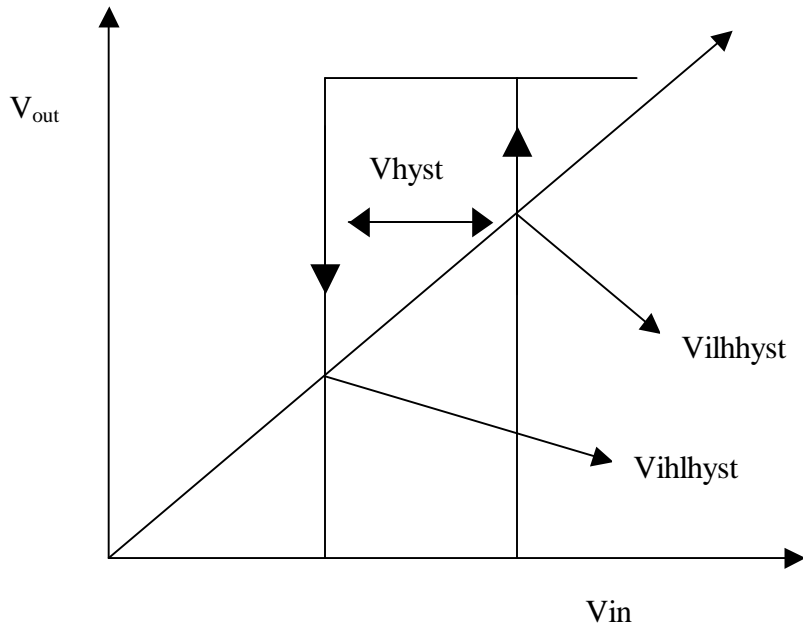
Figure 3.1-Hysteresis Characteristics

3.1.1.1 CIRCUIT DESIGN

As mentioned above the idea is to achieve different threshold points.

3.1.1.1.1 Standard hysteresis circuit

Figure 3.2 shows a very commonly used Hysteresis circuit. Here the different threshold voltages of n-channel and p-channel transistors are used as advantage. The Schmitt trigger proper consists of three p-channel devices M1 to M3 and three n-channel devices M4 to M6.

Functioning

For the dc voltage sweep from low to high at the input ,though M5 turns ON after Vin > Vtn5 ,M4 does not turn ON as Vt4 (threshold voltage of M4) is shifted due to body affect. Hence output voltage remains at high level .The source of M4 is initially at a voltage of VDD -Vt6 (body affected).But after Vin> Vtn5, the voltage at node N1 begins to fall. Here M6 and M5 form an inverter pair, having a feedback effect with M6 acting as a resistive load. As soon as VGS4 > Vt4 (body affected), M4 gets ON and output node

is immediately pulled to the ground. Also the drive strength of nMOS M4 and M5 is more compared to the pMOS M2 and M1.This explains the sharp transition characteristics of the circuit. The value of Vihhyst depends primarily on W/L of M6 and M5 for a given technology (Vtn fixed). Keeping M6 fixed, greater is the W/L of M5, and faster is the rate at which the node N1 is pulled down. This pulls up the switching threshold Vihhyst to a lower value towards left in figure 3.1.A similar explanation ensues for the input. Going high to low and feedback transistor M1 and M2 forming the inverter pair with M3 as a resistive load. Here the switching threshold Vilhyst depends primarily on W/L of M1.The difference in the two logic thresholds is achieved by a different pMOS and nMOS body affected threshold voltages.
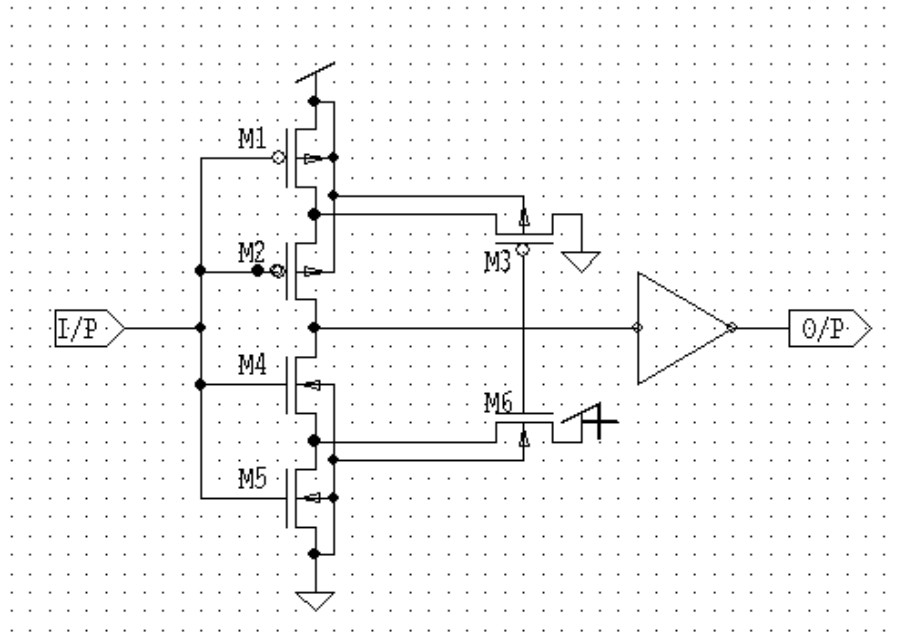
Figure 3.2 Standard Schmitt trigger

Approximate values of Vilhyst and Vihhyst can be obtained using [1]

k5/k6=((Vdd-Vihhyst)/(Vihhyst-Vtn))2………………………. (eq1)

k1/k3 = ((Vilhyst)/(Vdd-Vilhyst-|Vtp|))2………………………(eq2)

Advantages/Disadvantages

The driving transistors M2 and M4 show racing conditions when the transition begins. The switching points of the circuit cannot be defined precisely because the circuit is

based on a rationed operation. The NMOS inverter M5, M6 and the PMOS inverter M1, M3 are rationed circuits.

Transistor	Change	Rising threshold Vihhyst	Falling threshold Vilhyst
M3	W increases	No change	Decreases
M6	W increases	increases	No change
M1	W increases	increases	increases
M5	W increases	Decreases	Decreases
M2	W decreases	Decreases	Decreases
M4	W decreases	increases	increases

Table 3.1- Functioning of Schmitt trigger

3.1.2 Drive strength

"Drive Strength" of an input buffer is the capacity of the buffer to "drive" the specified load inside the CORE as shown in the figure 3.3
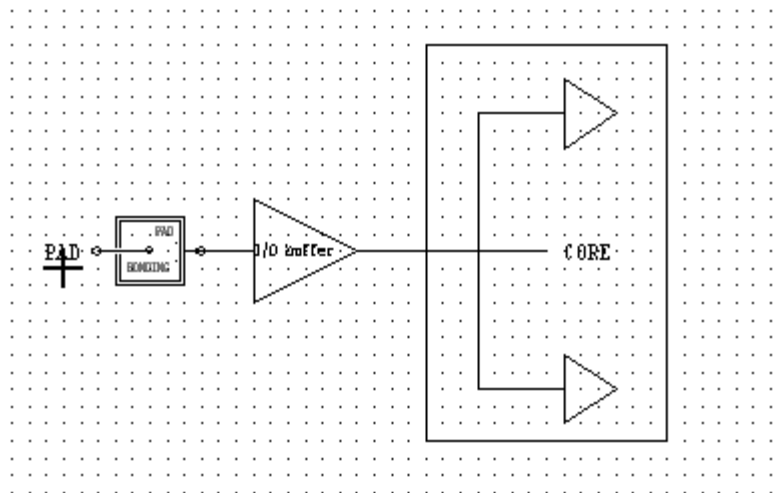
Figure 3.3- I/P buffer driving the core

The "Drive Strength" of the Buffer is primarily decided by the size of the last stage transistor. The bigger the size the greater is its drive capability. As expected the PMOS transistor decides its current sourcing capacity whereas the NMOS decides its sinking capacity.

Till a certain point we gain in terms of speed of buffer as the drive capability of the transistor is increasing after which greater area and the capacitance effect at the internal node takes over which slows down the buffer in terms of the slopes and delays. Also this may increase to such extend that previous stage may not be able to drive the large capacitance of the last stage. Tapering of buffers may be required which may result in layout area increase. Smaller the sizes of the transistor may result in very less drive capability, which may prevent the buffer to drive the required number of gates in the CORE.

3.1.3 BASIC DESIGN (Simple inverter)

Mostly the last stage would be a simple inverter whose PMOS and NMOS transistor Width's decide the drive strength. The last stage could also be cascoded transistors as shown in the figure 3.4(a). Here The Widths should be calculated accordingly. The supply should be of the same level as the one driving the CORE
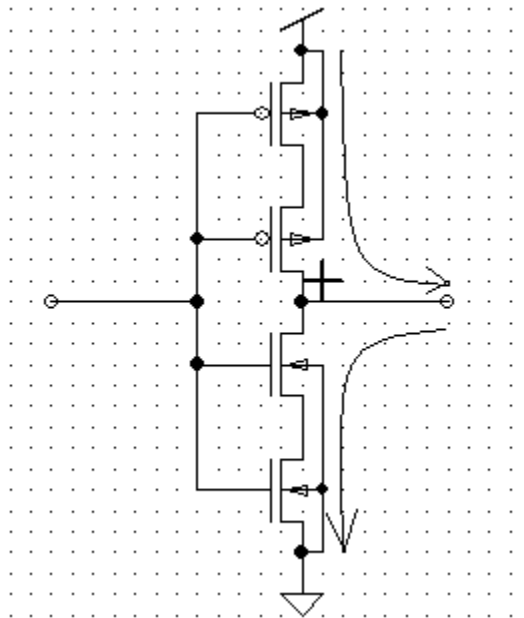
Figure 3.4(a) - Basic inverter circuit

ANY OTHER

Some times the last stage may not exactly be an inverter like in a tristate circuit. But the principle remains the same. The PMOS, when ON, should be able to drive the desired load maintaining the slope requirements and similarly the NMOS ON should be able to do the same as shown in the Figure 3.4(b). The last stage is not exactly an inverter. Supply should be of the same level as the one in the CORE.
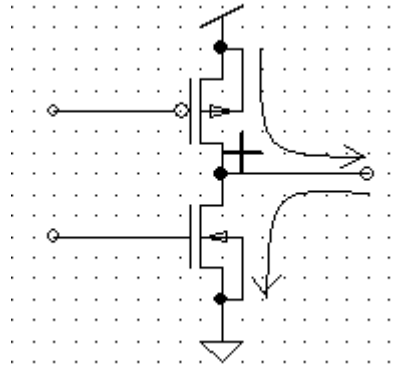
Figure 3.4(b) - Last stage in case of tristate circuit

GUIDELINES FOR CIRCUIT TUNING

The Standard drive Widths for CORELIB are calculated by seeing Power*Delay Product, Rise times, fall times and Delays v/s Wp/Wn of an inverter [21], whereas for the IOLIBs we try to keep the threshold point very close to the center of the swing (vdd/2). This is generally very close the value of the CORELIB cell.

TECHNOLOGICAL CONSTRAINTS

The Considerations with the technology generally will include

- Finding the corresponding Wp/Wn ratio.
- The minimum Width technology constraints.
- The Number of transistors minimum sized inverter can drive.
- Accordingly we decide on the drive strength.

3.1.4 Electrostatic Discharge

ESD is the discharge of large amounts of electrostatic charges on to the chip causing irreversible damage to the chip like gate oxide breakdown, snap-back, gate drain shorts

etc. Various reasons could be touching the chip with bare hands, touching with charged instruments etc. This has today become a major study area since a lot of chips are damaged due to these phenomena.

Optimization of ESD protections in IC is a task to be addressed at two different levels:

1. Elementary protection structures
2. Device protection network

Elementary protection structures

- Components suitable to accomplish a localized and effective energy discharge path.
- Are annexed to pad circuitry
- Can be active elements of the device
- ESD failure modes are related to the pad architecture and the discharge model.
- ESD protection devices should be chosen and optimized to fit the requirements of different pads.
- These structures should have minimum impact on the functional behavior of the device
- Protection architecture should be full consistent with the process flow

Device protection network

- The set of elementary protection structures (e.g. power supply protections) and "passive" elements (metal bus, substrate taps, guard rings) involved in any possible discharge path.
- Optimized elementary protections are necessary but not sufficient to achieve ESD immunity.
- In actual devices it is not possible to implement an elementary protection between any pair of pads.
- Taking advantage of existing metal bus, substrate taps, and guard rings. It is possible to organize the protections in a network providing a safe discharge path for each ESD configuration.

Typical ESD failures:

- Oxide damage at the drain/gate overlap in n - channel with drain directly connected to the supply lines

- $V_{ESD} > V_{bkd}$ (OX)

- Drain contact /junction damage in the n-channel biased in snap - back by the ESD pulse.

What is snap - back?

- A parasitic lateral NPN bipolar is associated to any n - channel transistor

- Turning -on this bipolar is termed as the snap - back.

- Irreversible damage is caused by the snap-back in not optimized structures.

- Junction avalanche inducted by the ESD can turn on this bipolar causing snap - back.

- It is possible to rely on snap-back to develop an optimized MOS protection structure

What should the protection devices protect?

CMOS INPUTS	Gate oxide breakdown
	Gate to Vcc protection
	Input diffusion to nearby diffusions
CMOS output buffers	Damage to the drain/substrate junctions
	Damage to the drain contacts
	Drain gate filament damage
	Drain source melt filaments
POWER pins	Damage to the internal circuits
	Increase in the post ESD I_{dd} leakage

Table 3.2- ESD protection

What should the protection devices do?

Input/Output/Supply Pins

- Clamp the ESD voltage to shunt the ESD Stress Current

- Turn on Fast (Less than 1 ns)

- Carry Large Currents of 2 Amps or more for 150ns

- Have Low on-resistance

- Occupy minimum area at the Bond pad

- Have minimum capacitance

- Introduce Minimum series resistance

- Be immune to Process Drifts

- Be robust for numerous pulses

- Offer protection for various ESD stress models

- Not interface with the IC's functional testing

- Not cause increased Vcc or I/O leakage

- Survive the burn-in tests.

Main requirements for ESD protection

Triggering voltage: Vcc < Vtrig < Vbkd (ox)

- higher than operating voltage i.e. no interference with the device functionality

- lower than failure thresholds

- gate oxide breakdown voltage (input /power supply)

- snap back voltage of the pull down (output)

Lateral NPN as the ESD device

Reverse biased collector junction collects minority carriers

- Collector junction avalanches holes are injected in the substrate.

  Avalanche is the process in which highly energized particles cause the formation of holes electron pairs.

- Excess holes forward bias the emitter junction because of the potential increase in the substrate. Current begins to flow in the base region.

- Electrons flow from forward biased junction to depletion region. Holes flow in the opposite direction.

- Positive feedback quickly focuses current into the base region; device is now operating as a bipolar.

Advantages of NPN as ESD device

- Triggering and sustaining voltage higher than power supply and lower than oxide breakdown
- high impedence when the device is ON in operating conditions
- low impedence when the device is OFF and ESD is applied
- Low dynamic resistance (~10 Ohms range)
- Structure consistent with the CMOS process.

Drawback of NPN as ESD device

- Bipolar action is induced by the collector avalanche. The mechanism is a potential cause of failure
- Large size is required to reduce ESD current density below the 2nd breakdown threshold
- Uniform current distribution is necessary but not easily obtained
- Not suitable for very fast ESD models (CDM)*.

    *CDM – Charge Device Model

3.1.5 Output Pad buffers

CMOS output pad Buffers are used to drive large capacitive loads which arise from long global interconnect lines such as clock distribution networks, high capacitance fan out and high off chip loads. The drive capability of such a buffer should be such as to achieve the requisite rise and fall times into a given capacitive load. Normally the drive capability of I/O buffers as high as 24mA [1] and as low as 0.8mA is available. Conventionally a XmA buffer would mean to source or sink XmA while fulfilling the worst case CMOS/TTL dc levels at the output of the sourcing/sinking transistor. The following section would help explain the meaning of an XmA buffer and gives the analytical design equations for designing such an output transistor drivers.

Design of a XmA Buffer:

Consider a push pull stage at the output of the buffer where both p and n transistors are driven by different set of controlled signals through a chain of inverters. The p transistor would apparently source the current while n would sink the current. All the simulations are performed at the worst conditions. This considers the inductive voltage drop in the power pads (due to the packaging lead inductance).Typically a drop of 0.4 V is used for the equations and eldo simulations here.
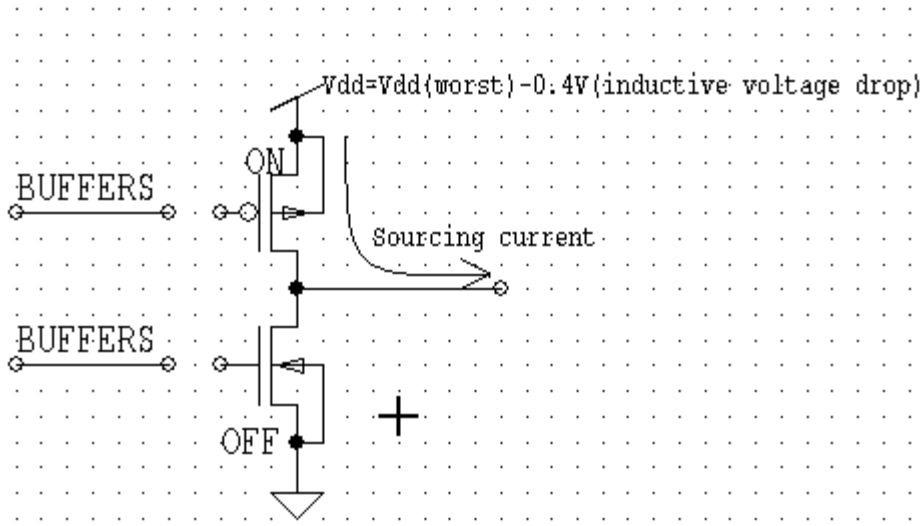
Figure 3.5(a) - PMOS sourcing current in X mA Buffer

$I_{DS}=\beta[(V_{GS}-VTP)VDS-V_{DS}^{2}/2]$ 2]...............1(a)

where β is given as

$\beta=\mu_{p}\varepsilon/t_{ox}.(W/L)_{p}$ ....1(b)

$(W/L)_{p} = [X . 10_{-3}]. [(-4.1 + |Vtp|)0.4 - 0.08]^{-1} [t_{ox}/\propto_{p}.\Sigma]$...................2

t_{ox} is the oxide thickness $\propto_{p}$ the hole mobility and Σ the relative permittivity of the Silicon dioxide.

The aspect ratio(W/L)$_{p}$ of the pMOS driver is designed such that I$_{DS}$=XmA.Thus for a CMOS output buffer (W/L) of the p driver for a XmA Buffer is given as in equation in 2.

With appropriate value of $\propto_{p}$ the hole mobility which is a highly sensitive parameter, aspect ratio values of the driver close to that obtained by ELDO simulations are obtained. The normal procedure for finding the driver sizes still is by performing ELDO / SPICE simulation on an isolated transistor under requisite dc levels and worst case supply voltages.
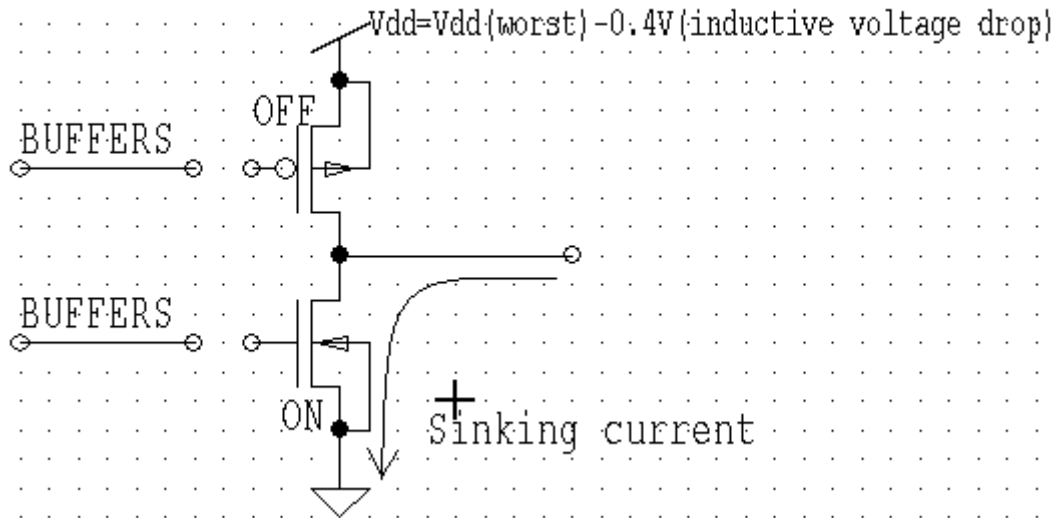
Figure 3.5(b) - NMOS sinking XmA of current

$XmA = \mu n * e/t_{ox} (W/L)n [(5-Vtn)*4-0.08]$

Where μn=electron mobility

Similarly the n transistor figure 3.5(b) will sink current while meeting CMOS / TTL output dc conditions. A rise fall time of 12 ns is achieved for the all buffers while driving a maximum load of 25 pf (determined conventionally) under nominal conditions.

Tapering of Buffers

Frequently the output stage transistors are preceded by a string of scaled inverters typically three in stage to scale the internal on chip gate signal to a drive level capable of quickly switching the large external capacitance. This prevents the degradation of signal paths by placing too large a capacitive load on previous stages.

The optimization to be achieved in such scaling is to minimize the delay between the input and output while maintaining the area and the power dissipation. A basic derivation of tapering factor in [2] has shown the factor to vary between 3 to 10.A series of advanced works has appeared recently in journals. The work in [3] gives an accurate expression of this factor taking into account the short circuit current power consumption. Design of tapered buffers for gate arrays and standard cell circuits is presented in [4].

While a variable stage ratio approach as a means of reducing the area of cascoded inverters in Buffers is presented in [5].

Undoubtedly the tapering of buffers for optimization to meet constraints such as area, power and speed has come to occupy a degree of importance in Buffer design. An extensive deal on this topic is certainly out of scope of the present work

Different output stages

Often a plain inverter stage at the output of buffers is avoided. The miller capacitance formed between the gates and the source-drain diffusion [2] of p and n transistors can result in oscillations at the output in series with the lead inductance. Also the self-bootstrapping causes additional delays. The short circuit power dissipation is highly possible in such a configuration. These limitations have given rise to several types of output stages. Below is explained some of the widely used configurations with their relative merits.

PUSH-PULL STAGE:

A push pull stage consists of p and n transistors at the output pad for sourcing and sinking respectively, where each of the gates of transistors is controlled through a different chain of tapered inverters fed after buffering (as shown in figure 3.6)**.** Such a stage has the advantage of doing away with the miller capacitance and hence bootstrapping (by avoiding direct gate contacts of the two output driver transistors.). Also static and short circuit power dissipation can be avoided by bifurcating the inverter chain in a way such that while sourcing current at the output pad, NMOS driver is made OFF before PMOS is on and vice versa. This prevents a short path at any moment of operation.
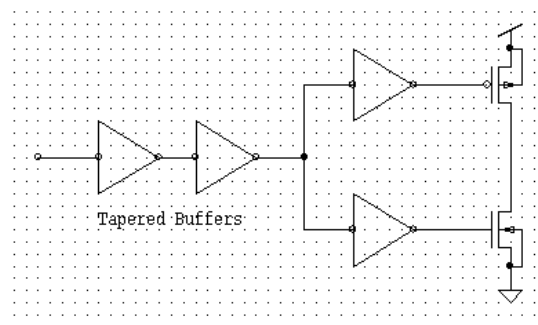
Figure 3.6- Push pull output stage

OPEN DRAIN OUTPUT STAGE:

An open drain stage is superior to push pull stage in that it has just one driver transistor. Such a configuration obviously avoids even the source -drain diffusion capacitance apart from doing away with miller capacitance. Thus open drain is faster than a push pull stage pad. The limitation of such a driver is that it can either source or sink current at a time. The two possible configurations are shown below in figure 3.7. The output state of the pad can also be driven to tristate and can be connected to buses where high impedance state is required for data transfer.

I/P	O/P
H	H
L	Z

I/P	O/P
H	H
L	Z
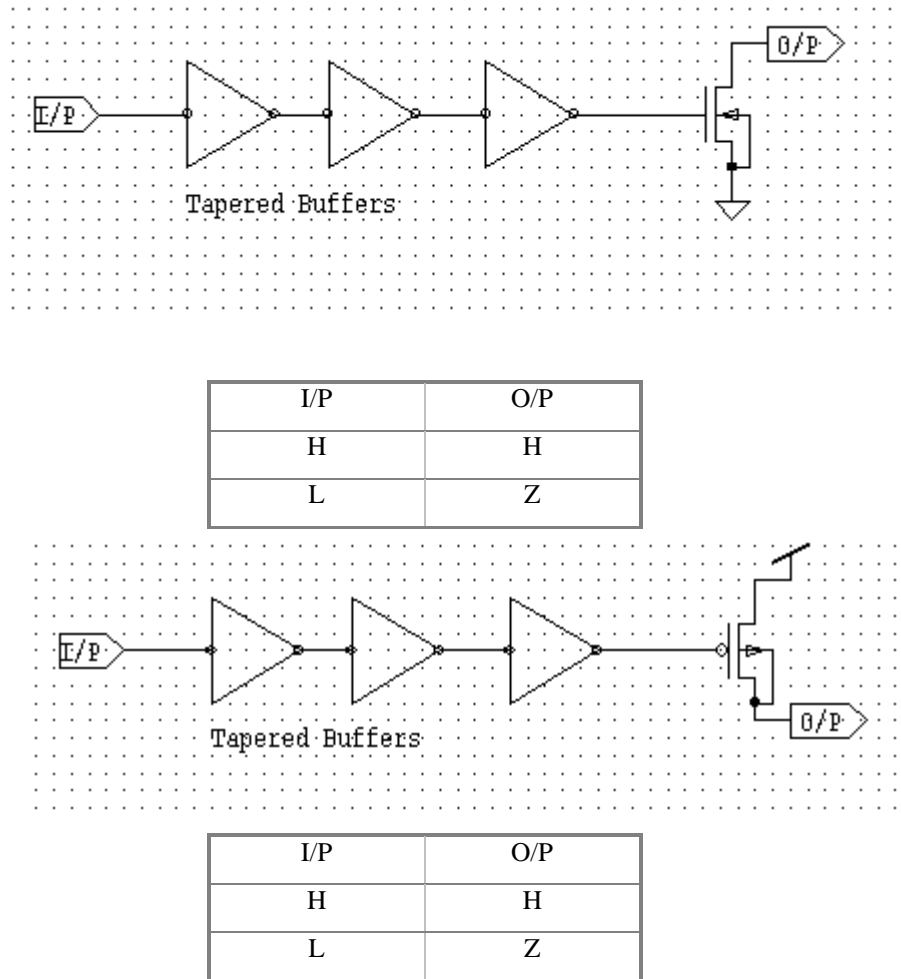
Figure 3.7 - Open Drain output stage

TRISTATE PADS:

A high impedance state, which is the state when no current flows at the output, is required when data is to be transferred from the bus [14]. This state is achieved when both the p and n output transistors go into cutoff region of operation. A simple logic for enabling such a state with a particular dc level at an input pin is shown in the figure 3.8(a) and figure 3.8(b).Thus when input pin EN is high, both p and n transistors at the output is OFF and tristate is achieved. Open Drain output stages can also be tristated by appropriate signal at the input.
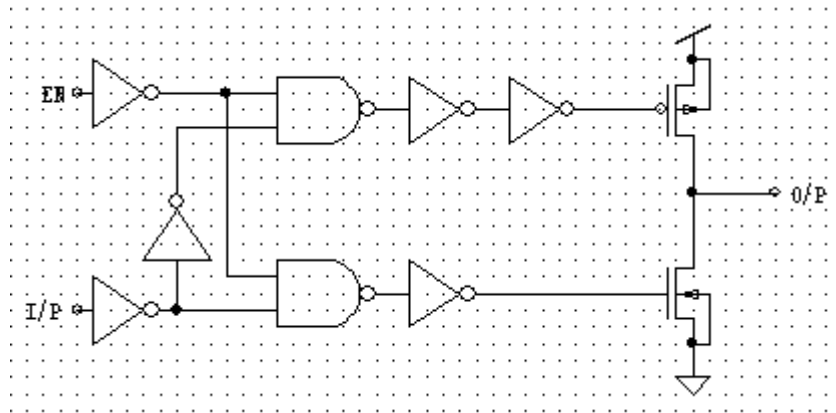
Figure 3.8(a) - Tri stated pads Using NAND gate

EN – Active Low
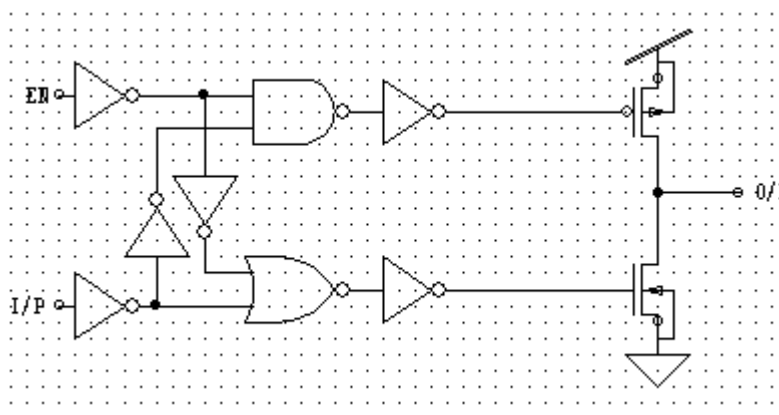
EN – H, Z – Tristated

Figure 3.8(b) - Tri stated pads Using NAND and NOR gate

EN – Active Low

EN – H, Z – Tristated

PULL UP/DOWN STAGES:

Often the tristated output is put to a particular logic level instead of letting the bus float [22]. Either logic low or high can be made at the output using the pull up or pull down transistors. Normally the NMOS is used for pulling down and PMOS is used for pull up, configured as shown in Fig 3.9.The design specifications [6] for the pull up /down stages specify the equivalent resistance and the pull up/down current allowed. The design of such transistors is such as to allow the least static power consumption though quickly pulling up/down the tristated bus to the required logic. The pull up/down stages can also
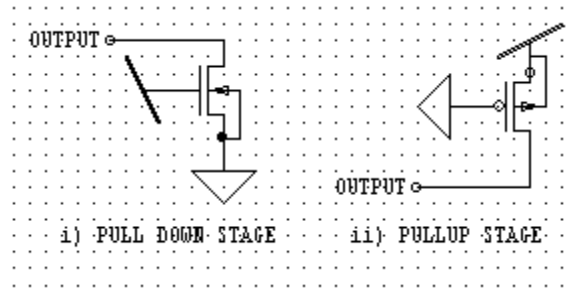
Figure 3.9- Output/Input pull-up pull-down transistors

Be used at the input of input buffers to keep them from floating.

3.2 Slew Rate Control

A fast transition of the signal at the output pad tends to introduce frequencies in UHF range into the off chip load being fed. Sometimes this becomes undesirable in applications such as if the signal is fed to a Television chip, cellular phones, radios etc. The signals in the UHF range then appear as noise. Thus many a time's controlled switching of current signal at the output pad is required, achieved by slew rate control circuits. A controlled switching also results in reduced dI/dt power supply noise. The source of this noise is the inductive voltage drop $V = L (dI/dt)$ at the power rails where inductance is introduced by the package pins.

Other methods to reduce this noise would be to use the lowest inductance package pins (usually the center pins) for power and ground or reducing the off chip load being driven. Slew rate control circuits thus artificially limit the rate of current switching thereby limiting the UHF interference. A very basic work on what exactly slew control would mean has been presented by Parthasarthy in [7].

The basic approach for achieving slew rate is to break the output driving transistors in different parallel transistors and switch the stages sequentially one after the other with some delay. Below is explained the working of a Slew rate controlled circuit used with Pad limited I/O design. The slew rate action is basically achieved through the circuit shown in figure 3.10(a).

A predriver consisting of inverters is designed in such a way so that the signal at NIN rises faster than PIN while signal at PIN falls faster than NIN (simple jugglery with W/L of predriver inverter can achieve this.). The signals are shown in figure 3.10(b). For illustration sake let the signal at NIN and PIN fall. (Which is when the input signal goes low). Since PIN goes low first, the output of all the NAND gates PD1 -PD4 go high at the same time This results in all the output p transistor, shown in figure 3.10(d) go OFF at the same time. While NIN goes low from high state later than the PIN, the output of the first NOR gate ND1 switches to high later. Further ND2, ND3 and ND4 would switch high sequentially as the signal is propagated through the NOR-NOT set of gates. The switching of ND1-ND4 is as shown in figure 3.10(c).Thereby a controlled switching at the output is apparently concluded by applying the signals ND1-ND4 to the output driver n -transistors stages [15]. A reverse case of output going high, while sourcing current is explained as above with faster transition at NIN than PIN.
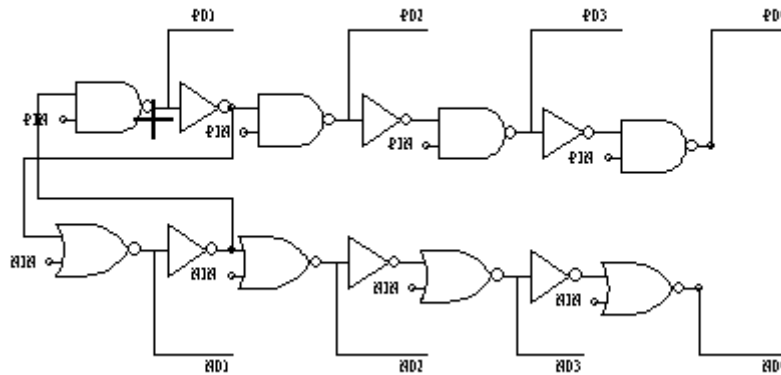
Figure 3.10(a) - Slew rate control circuit

The rate of switching is controlled by the amount of delay offered to the propagation of signals by the set of NAND-NOT and NOR-NOT set of gates. Greater is the delay offered to a particular transition of switching, more controlled is the current switching and hence more is the slew rate control. A set of modifications can be made to the basic

circuit of slew rate control to have a balance of slew rate control, area and power constraints.
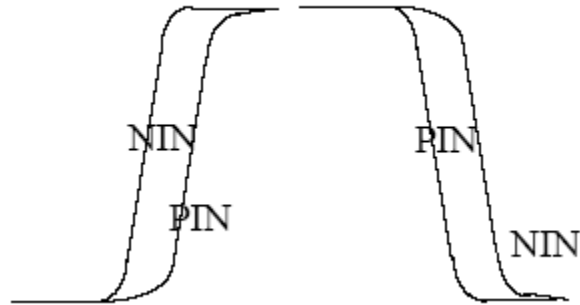
Figure 3.10(b) - Signals from Pre-Driver stages
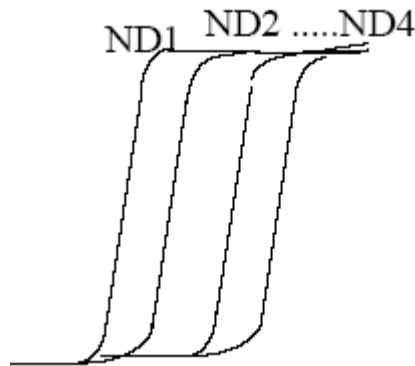
Figure 3.10(c) - Switched signal at the NMOS driver I/P
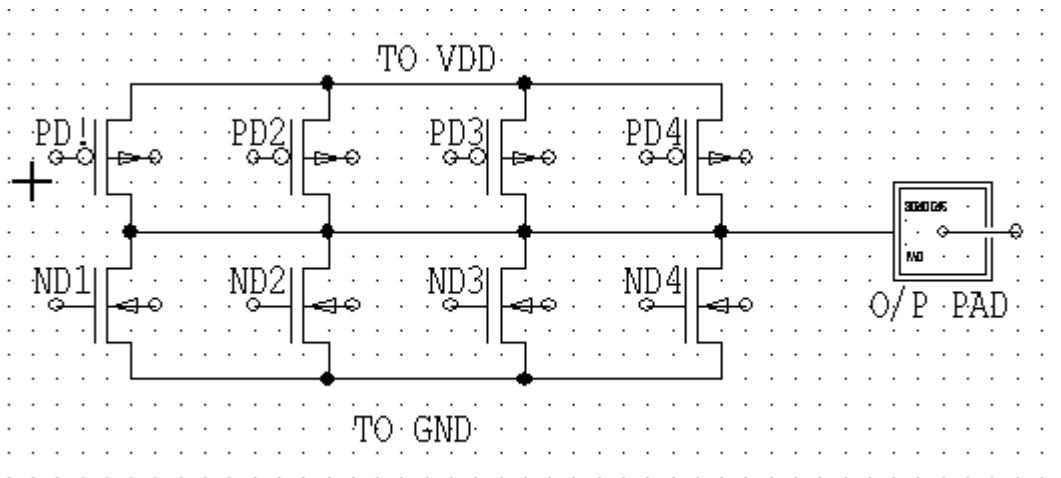
Figure 3.10(d) - Multi stage O/P driver

3.2.1 Active Slew Rate Control

Although, Active slew rate control and design of compensation Block is beyond the scope of the current work, but to understand I/O's as a whole, it is necessary to have a brief overview of the compensation block. The necessity of the slew rate control has been explained in the earlier part of the work.

What is active slew rate control?

Normally the designing of an I/O is done in the worst-case conditions i.e. meeting the timing constraints etc. Worst-case design is used so that the data can be transferred from one circuit to another within a given time period. It is under these conditions that the slew is measured but unfortunately the worst-case condition for the slew lies on the other end usually referred to as the "best conditions". Therefore as we move from towards the best conditions slew increases and degrades the noise performance. Active slew rate control is the way to compensate for this change of slew with the PVT conditions so as to able to keep relatively constant slew over all conditions.

How is it achieved?

An electronic circuit is designed to provide digital compensating information to a CMOS output buffer or to a number of CMOS output buffers. This circuit is usually called the COMPENSATION BLOCK. This compensating information is used in the buffer to ensure that the CMOS buffer will operate quickly during "worst case" conditions but will not operate too quickly under "best case" conditions.

The digital information from the compensation block is fed to the transistors. The code is such that for best case fewer transistors are on (lesser current) and for the worst more transistors are on (larger current).

Compensation Block

This circuit, as we know now give the digital code for the buffers used to offset the process changes. The basic principle behind the design of this block is to have three sub blocks. As shown in the figure 3.11

- A Block which gives o/p proportional to the changes in PVT
- A Block which gives o/p independent of the changes in PVT
- A Block, which compares the o/p of two blocks to give the desired digital code.

```
┌─────────────────────┐
│                     │
│  Proportional to    │
│  changes in PVT     │              ┌──────────────────────┐
│                     │              │                      │
└─────────────────────┘              │  Compares and gives  │
                                     │  a digital output    │
┌─────────────────────┐              │                      │
│                     │              └──────────────────────┘
│  Independent to     │
│  changes in PVT     │
│                     │
│                     │
└─────────────────────┘
```
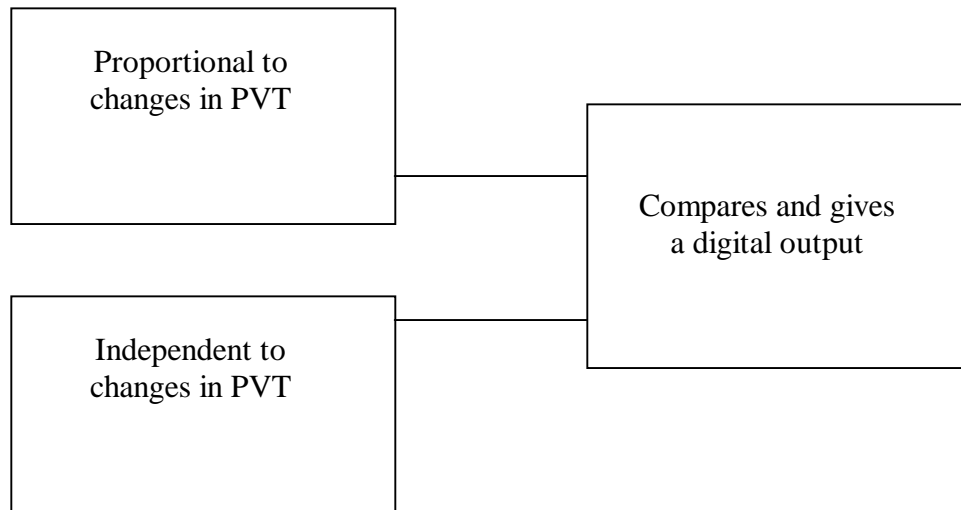
Figure 3.11-Compensation Block

The COMPENSATION cell controls the value of the current slew rate of the output signal delivered by the I/O Cell and also its output impedance, and maintains them in a specific range. The cell is designed to provide digital information depending on the current temperature, process, and supply levels to a CMOS output buffer or indeed a number of CMOS output buffers. Due to the termination configuration, a DC current flowing through the output buffer causes the current slew rate to be controlled during switch-on and switch-off of each N and PMOS driver.14 bits are dedicated to IO for this control. The compensating information allows CMOS buffers to operate fast enough, but not too fast, whatever their PVT environment (Process, Voltage, and Temperature). The code is continuously updated as the PVT conditions vary.

The user has to connect the codes, which are going to be used in IOs to their corresponding rail. Unlike the previous designs, the compensation cell provides 14 output bits .In earlier designs these 14 bits are averaged to provide a 7-bit code. But this 7 bit code had a weak point .It couldn't account for the conditions when PMOS was fast but NMOS was slow and vice versa. This design provides 7 separate bits for PMOS as well as NMOS to overcome this problem. Another difference from the previous designs is the use of Band gap reference generator to generate the reference voltage. An external

resistor is used to convert the band gap reference voltage to current. Use of external Resistor minimizes the variation in current because of the very low tolerance (1% compared to 20% for the internally fabricated one). The output current of this cell is much more stable than output of the PTAT current generator that was used in previous designs.

3.3 Low power design considerations

A majority of power consumed by the output buffers is by the dynamic switching of high capacitive loads at the output. Obvious means of reducing dynamic dissipation is operation of the circuit at lower frequencies, reducing supply voltages and voltage signal swing on the high capacitive interconnects or even at the output (for e.g. ECL compatible levels). Such low swing CMOS buffers have been reported [8] specially designed for applications where the interconnect capacitance is high such as in gate array design where the floor planning may require the buffers to be placed in different array of cells or in different functional blocks. Such buffers need both the driver -receiver configuration, drivers to pull down the signal swing on interconnects and receiver to pull up the signal to full swing CMOS logic. A system level design for driving and receiving the terminated low voltage swing signals between CMOS chips is presented in [9]. The ECL level compatible buffer automatically measures the impedance of the external lines being driven and match the I/O pads driver to reduce the reflections.

Static and short circuit power consumption [10] though not constituting a major contributor to overall power consumption, is a factor easily controlled through simple design changes. A properly designed push pull stage at the output of the buffers can prevent shorts between power rails (as explained earlier). An open drain stage further saves power with just one driver transistor. Static power saving is also made by using proper receiving stages, in case of low swing voltages. [11]

3.4 Input Buffers

An input buffer couples the external off chip signal to the core elements of the chip. Since the external signal can have voltage ranges much beyond the normal CMOS

operating voltages, an input ESD protection is required for these buffers. The non-destructive breakdown of diodes is utilized to clamp the voltage between Vdd and Vss. The resistor tends to decrease the current reaching the gate of devices. Figure 3.12 shows the circuit to achieve the diode clamping. The only disadvantage is the introduced RC delay (each diode introducing a capacitance) to the input of the circuit. The design has to be optimized if used in high-speed circuits. ESD protection for buffers today has a major role to play in the efficient chip design. A full level discussion on this issue has been left out of the present work for terseness sake and as a course for future work.
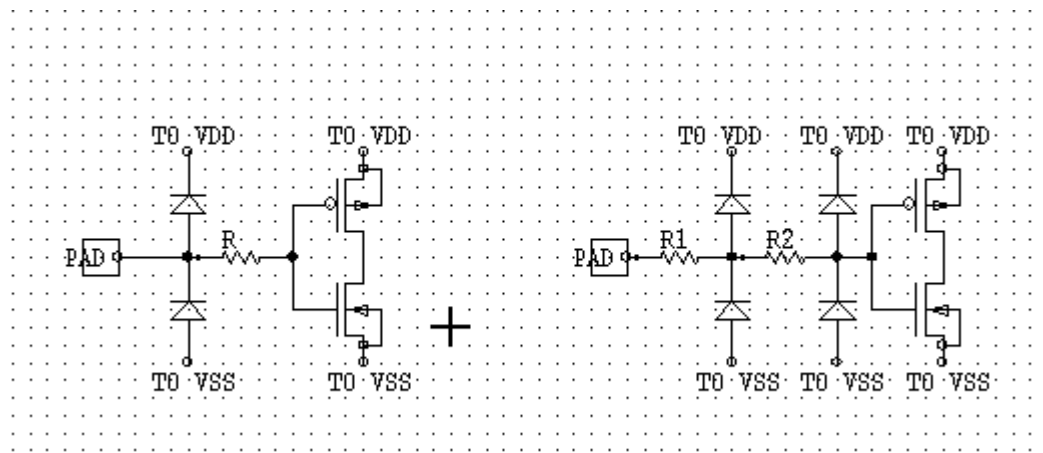
Figure 3.12 - Input ESD protection circuits

CMOS AND TTL BUFFERS

An external signal may be either CMOS or TTL. Normally the design of input buffers consists of cascaded CMOS inverter chain sufficient to drive the internal load [13]. A CMOS to CMOS buffer design is very simple, having two inverters as shown in figure 3.13. The gate length of first stage inverter is greater than the normal gate lengths to prevent early avalanche breakdown with high input gate voltages.
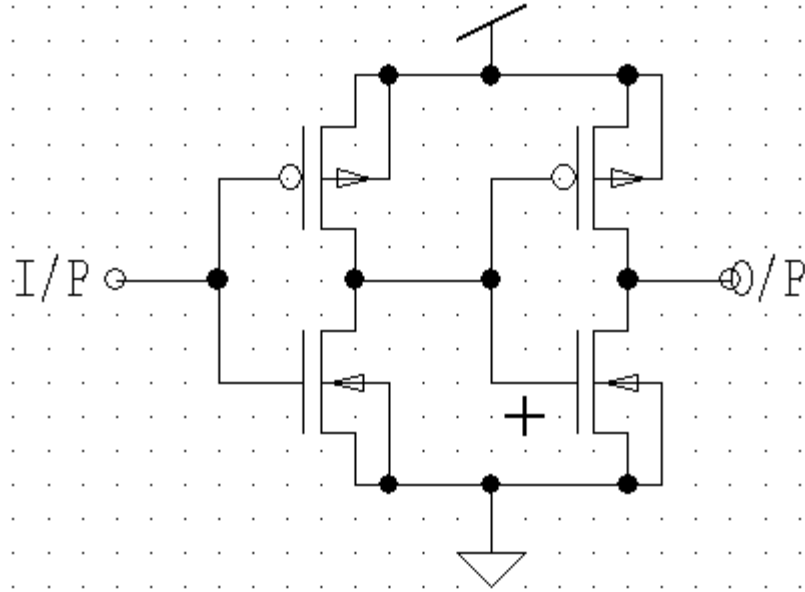
Figure 3.13 - Input Buffer

Many systems still use TTL or ECL interface for compatibility with existing systems or for high-speed interchip communication. So input buffers, which convert TTL logic to CMOS are necessary for the design. Design of such buffers is very easy with a pair of CMOS inverters where the size of first inverter has been scaled down to switch between the TTL logic thresholds V_{il} of 0.8V and V_{ih} of 2.0V.Thus to locate the switching logic threshold around 1.4V, the PMOS and NMOS size of first inverter has to be scaled down. Such configurations have patently high static power consumption .For example when the input is TTL high of 2.4V, both PMOS and NMOS is on and hence a through current from supply to ground, resulting in standby power dissipation. [12]

CHAPTER 4

DESIGN AND SPECIFICATIONS OF BIDIRECTIONAL BUFFER

The design strategy of designing the bi-directional buffer has been discussed in previous chapters. Keeping those design strategies into mind following BIDIR has been designed

BIDIR name: BD2SCARDQP_2V5_LIN

4.1 NAMING CONVENTION

BD Bi-directional buffer.

1st suffix -   Drive capability in mA.

2nd suffix - S for Schmitt trigger on input.

3rd suffix - C for CMOS levels.

5th suffix - R for slew rate control

AR for active slew rate control.

D for active pull down.

8th suffix - Q for switch on pull-up/down.

9th suffix - P for test functions.

10th suffix - _2V5 for 2.5V.

11th suffix - _LIN for Linear views.

4.2 ELECTRICAL SPECIFICATIONS

	Parameter	Minimum	Typical	Maximum	Unit
V_{dd}	Core power supply voltage	0.9	1.0	1.1	V
Vdde2v5	2.5V IO power supply voltage	2.2	2.5	2.7	V
Tj	Operating junction temperature	-40	25	125	^{o}C

Table 4.1 – Electrical specifications of the bi-directional buffer

4.3 IO SPECIFICATIONS FOR 2.5V BIDIR

The 2.5V IOs comply with the JEDEC standard JESD8b. [23]

	Parameter	Minimum	Maximum	Unit
Vil	Low level input voltage		0.7	V
Vih	High level input voltage	1.7		V
Vhyst	Schmitt trigger hysteresis	300	600	mV

Table 4.2 - DC input specification (2.2V<vdde2v5<2.7V)

	Parameter	Min.	Max	Unit
Vol	Low level O/P voltage		0.2	V
Voh	High level O/P voltage	Vdde2v5-0.2		V

Table 4.3 - DC output specifications (2.2V<vdde2v5<2.7V)

	Parameter	Minimum	Maximum	Unit
Ipu	Pull up current	27	85	uA
Ipd	Pull down current	20	99	uA
Rpu	Pull up resistance	32	81	Kohm
Rpd	Pull down resistance	27	110	Kohm

Table 4.4 - Pull-up and Pull down Characteristics

4.4 BUFFERS DESCRIPTION (FUNCTIONALITY)

4.4.1 BIDIRECTIONAL buffers

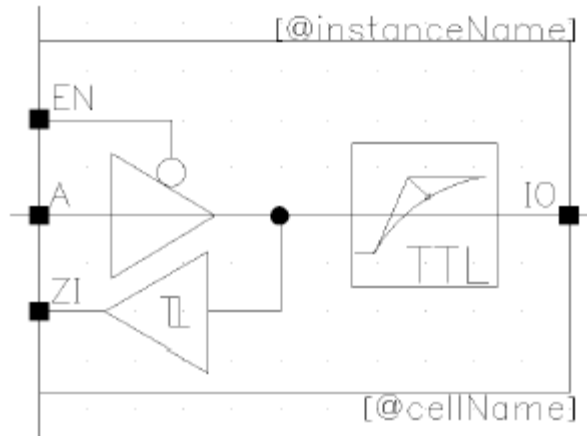Bi-directional buffers are tri-state output buffers associated with an input buffer.

Figure 4.1 - Bi-Directional IO

EN	Function
0	Output buffer plus copy of A on ZI. The I/P signal arrives on A, the cell drives IO and ZI with IO=ZI=A
1	Input buffer. The input signal arrives on IO, the cell drives ZI with ZI=IO.A is not used

Table 4.5 - Modes of operation of a normal Bi-directional Buffer

4.4.2 OUTPUT STAGE:

- The rating of output buffers, which is 2mA, is a DC specification. This is the current a buffer can source/sink within VOH and VOL specifications, in worst-case conditions. The maximum output current, during output switching, is much higher.

- The primary goal of the slew rate control circuitry is to reduce the SLOPE of the CURRENT flowing to/from the load. Furthermore, this library includes only buffers with "active" slew rate control, which have "AR" in their names. Their output current slew rate, dI/dT, is relatively constant over the temperature, power supply and process variations.

4.4.3 MODES OF OPERATION FOR 2.5V I/O

Normal operation (NORMAL INPUT/OUTPUT MODE)

- If the pin **EN** is LOW for a Bi-directional buffer then the buffer is in Output mode, and can drive out a 2.5V signal.

- If the pin **EN** is HIGH (1.0V) for a Bi-directional buffer then the buffer is in Input mode, and can receive a 2.5V signal.

IDDQ test

- For IDDQ test there should be no dissipation in IOs.

1.0V Core supply power down (COREOFF MODE)

- A feature for 2.5V Capable IOs is that if the 1.0V core supply (VDD) is powered down, whilst there is external activity at the 2.5V interfaces the Output transistors do not turn-on and no dc power is consumed. In other words external 2.5V activity doesn't have impact on the IOs, but signals cannot be received or transmitted. This is **COREOFF MODE.**

- During COREOFF MODE, the internal DC current remains very low, and the buffer remains in tri-state mode.

IOOFF MODE

- Some applications for 2.5V Capable IOs require that the 2.5V periphery supply (vdde2V5) be powered down, whilst the core (1.0V) supply is still active. This

might happen during power up/down sequences, for example. Clearly if the 2.5V supply (vdde2V5) is powered down, external activity at the 2.5V interfaces cannot be allowed, either at 2.5V or at 1.0V signal levels, since in either case the junction diodes of the output pmos devices would be forward biased collapsing the signal. Therefore, such a mode supports the presence of the 1.0V supply whilst the 2.5V supply is powered down, but doesn't allow activity at the external interface to the pad. This is **IOOFF MODE.**

Chapter 5

LAYOUT STRATEGY

5.1 HIERARCHY

The use of hierarchy involves dividing a module into sub modules and then repeating this operation on the sub modules until the complexity of the sub modules is at an appropriate level of detail This is similar to software application program where large program are split into smaller and smaller sections until simple subroutines, with well defined functions and interfaces can be written. Although we can have module at single level but the picture of the module will not be clear and easily perceivable. In case of hierarchical approach, if some error occurs in the functionality, then it is easier to focus on the problem and can be corrected with ease.

5.1.1 INSTANTIATION AND HIERARCHY

Many times in a circuit, certain leaf cell is used many times in the same cell, and that cell may exist in some library. There are three ways in which that leaf cell can be placed in the cell i.e.

- Either by designing the leaf cell from scratch
- By copying the cell from the library and the placing it at the required place
- By just instantiating the leaf cell in the cell. The last method has one major advantage over the first two, as it reduces redundancy.

By instantiating a cell or leaf cell inside a circuit we just refer that the action to be performed on the signal at that instance has to be preformed by the cell or leaf cell present in some library. It helps in DRC and LVS as the cell or leaf cell is already DRC and LVS clean. So when we run the DRC or LVS we perform these tasks in HIERARCHIAL mode. Hierarchy is nothing but the action performed on the circuit in top to bottom fashion. By top to bottom fashion we mean that the task is first performed on the top level, i.e. if some cells are instantiated in the circuit the direction of flow of action is directed to the instantiated cell and if again some cells are instantiated in the

instantiated cell in the main circuit, then it goes to the cell instantiated in the instantiated cell. Again if we want to go to the bottom most instantiated cell we can descend into the cell only in hierarchical way.

5.1.2 CALIBRE

CALIBRE is the Mentor Graphics batch layout verification toolset, which works on GDSII and CIF (CalTech Intermediate Format) data, as well as data generated from IC station. Layout verification is required to check the validity of the layout in context of Process and actual gate level design prior to their testing on silicon. The layout verification is divided into the following four tasks:

Design Rule Check (DRC) verifies that the physical design rules have been met for every object in the design. These rules are technology dependent and they require updating as the technology changes.

Layout Versus Schematic (LVS) verifies that the layout matches the schematic or net list.

Parasitic Extraction (PEX) presents layout information about parasitic resistance and parasitic capacitance and back annotating them to corresponding objects in the schematic, for more accurate simulation. With this information, you can see where to change the layout to improve chip performance.

Electrical Rule Check (ERC) performs connectivity related checks.

GDS Format For calibre DRC and Calibre LVS verification; it is required to generate a netlist of the layout in GDS format. This format converts the geometrical information of the gate level logic into a netlist file which sets different codes for different layers used in the layout, along with its geometrical shape, in the layout, in the form of coordinates. During Calibre DRC, it basically picks the layer codes and the coordinates for different layers and compares it with its design rule file drc.ctrl file. This drc.ctrl file contains the defined set of rules for layers spacing and their minimum geometrical shape. Calibre DRC is a fast, high capacity, and complete design rule check system.

CDL Format This is a format in which the information about the connectivity of different devices, pins, and components in a circuit is stored. This netlist is slightly

different form Spice netlist so during LVS verification the tool picks the information about the connectivity of different layers and their pin configuration and compares it with the schematic netlist which is in CDL format which actually has the connectivity information about the circuit form schematic

5.2 HIERARCHY IN LAYOUTS

In a layout of an I/O, there are two types of cells:

Base cell consists of active, poly, and transistor. Usually for one library, all the I/Os have same base cell irrespective of whether its an input, output or bi-directional with few exceptions where some modification at the base level is necessary to achieve some important characteristic which is otherwise not possible in the chip. Base cell has defined boundaries within itself for different blocks, which are needed to design a buffer. And in these defined space, transistors with active and poly for that particular block is present in floating state i.e. they are not connected together, or some other leaf cell is instantiated.

Leaf Cell can be of two types:

- One having only the information about the connectivity of transistors with their pin information at top level or at the instantiated cell level. They have different metal rails, vias and pins in their cell view.

- The other type contains active and poly forming the transistor along with some metal rails used in the cell, which is same for all the cells in the library. These cells are actually instantiated at the base level and can be instantiated inside other leaf cell or they can instantiate some other leaf cells inside them. They are generally lower in hierarchy to base cell.

5.2.1 LAYOUT EXTRACTION

Once a layout has been constructed, then it is required to generate its extracted view. Layout extractors examine the interrelationship of mask layers to infer the existence of transistors and other components .As metal layers are used to connect different components, to provide path for the signal to flow, in the process parasitic resistances and parasitic capacitances are added to the original circuit. They affect the functionality of the chip apart from degrading the quality of the signal. So an extractor basically calculates
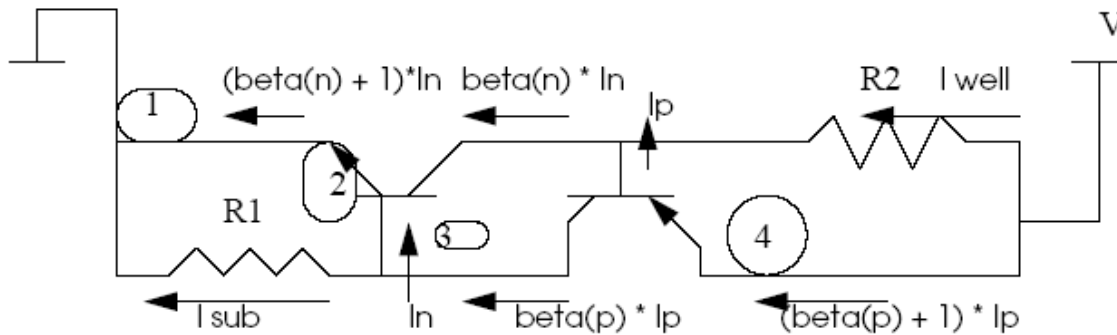
the parasitic resistances and capacitances at each node and adds this information in the extracted view. It is necessary to check the functionality and performance of the signal taking into account all the parasitic effects. This is accomplished either by simulating the generated netlist from the extracted view or back annotating the parasitic effects at their respective nodes in the schematic and simulating the new schematic view. First approach is quite easy .The output given indicates the actual response of the circuit on silicon. This helps in making modification in layout view to reduce parasitic effects to restore the specified functionality and characteristic of the circuit .

5.3 LATCHUP

The device structures that are present in the standard CMOS technology inherently comprise a pn-pn sandwich of layers as shown in figure 5.1(a) and figure 5.1(b).

Figure 5.1(a) – NMOS and PMOS transistors

Figure 5.1(b) – Effect of latchup

The sandwich can be thought of as a connection between a parasitic pnp and a parasitic npn transistor. The source of the n-channel transistor forms the emitter of a parasitic lateral npn transistor, the p -substrate forms the base and the n-well forms the collector. Also the source of the p-channel transistor forms the emitter of a parasitic pnp transistor, n -substrate as the base and the p-substrate as the collector. Thus the resulting circuit is formed.

In the normal mode of operation both the junctions are reversed biased. Problem occurs when due to some reason one of the two transistors go into the active region. Then a positive feedback is formed and large currents flows causing breakdown in the cmos. This phenomenon is called latch up [20].

The transistor can go into the active region for a variety of reasons like

  ▪ application of voltage which is greater than power supply voltage to an i/p or o/p terminal
  ▪ improper sequencing of power supplies
  ▪ presence of large dc currents in substrates
  ▪ flows of displacement currents in the substrate due to fast changing internal nodes

Latch up chances increase when the substrate or well concentration is made lighter, as the well is made thinner and as the device geometries are made thinner. This is because it increases the resistances and increases the beta of transistors.

Latch up can be prevented by include special protection structure at i/p and o/p pads so that the excessive currents flowing can be effectively shunted and inclusion of low

impedance diffused "guard rings" surrounding the wells. The latter are formed by using the source/drain diffusion and provide a low-resistance, equipotent ring in the substrate and well to lower series resistance.

5.3.1 TENTATIVE LATCH UP DESIGN RULES

Definitions

IO: Input / Output. Power pads are not considered as IO pads.

Emission site: all active regions (OD) directly (or via a maximum resistance of 5kW) tied to an IO pad as well as all junctions which can be forward biased are considered as potential emission sites, and must be protected against latch up.

Well tie: a well tie is an OD active used to connect the wells. P+/OD inside a Pwell as well as an N+/OD inside an N well are considered as well ties.

Majority guard ring: a majority guard ring is a well tie which completely surrounds an emission site of majority carriers. It aims at collecting majority carriers, and decreasing the well resistance.

Minority guard ring: a minority guard ring is usually formed by an N+ OD / Nwell (with or without Deep N well) connected to a high potential (vdd). It completely surrounds an emission site of minority carriers (by eg: N+/P well or N well/P well junctions) and aims at collecting them.

Ring series resistance: it corresponds to the maximum resistance from any point of the guard ring to the PAD where the ring is connected (generally Vdd for N+ OD / Nw guard ring and Vss for P+ OD Pw guard ring). It includes metal bus and contact resistances as well as silicided OD resistance. The value provided in this document can be applied only if all other rules concerning guard rings are fully applied (continuous silicided OD surrounding an emission site).

Critical IP: All IPs having active regions directly (or via a maximum resistance of 5kW) tied to an IO pad are considered as critical from a latchup point of view (ex: IO cells).

Critical Nwell: All Nwells having a P+ OD (or an isolated Pwell) emission site are considered as critical Nwells.

Maximal voltage difference: the voltage difference must be calculated in all application modes of the IP. The highest voltage difference is then used for Nwell distance rules.
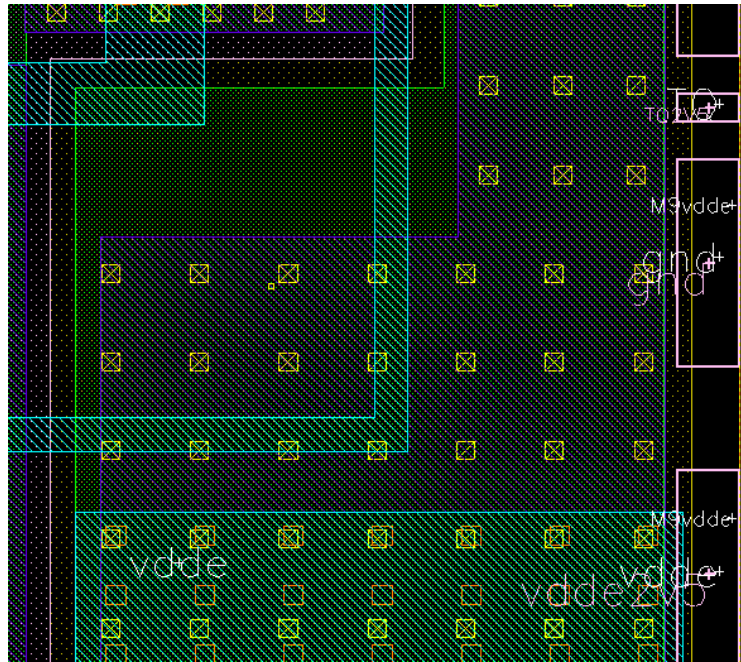
Figure 5.2(a) Measure to avoid latch up

In the figure 5.2(a) shown above the green color shown is OD (active region). In this particular case OD is working as a guard ring. This active area has got a lot of resistance, which aids in latch up problem. So to minimize the resistance of the OD metal1 (blue) is placed over it having as many contacts as can be possible. The metal1 will come in parallel with OD and hence minimizing the resistance.

In figure 5.2(b) one of the method called strapping has been done in order to avoid latch up problem. In this case the n substrate or p substrate are tied to VDD or ground respectively as either the case may be for PMOS and NMOS. The figure below shows the strapping with vdd i.e. n substrate with the help of vias and different metal layers.
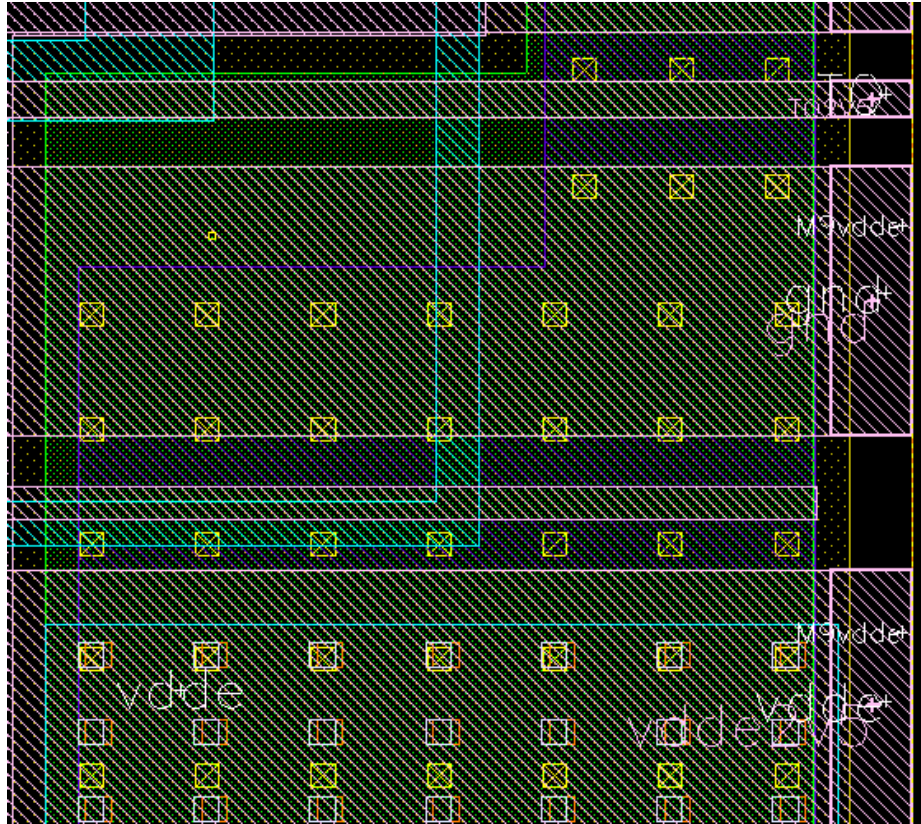
Figure 5.2(b) Measure to avoid latch up

5.3.2 Metal thickness rule

Metal thickness rule to be followed while forming the layout at different temperatures

Tj=105°C

Metal Level	Idc(mA)	Irms(mA)	Ipeak-DC(mA)
M1	3.036(W-0.02)	Sqrt[93.83(W-0.02)^2+0.484]	16.45 Idc
M2	4.026(W-0.02)	Sqrt[30.08(W-0.02)^2+0.654]	8.07 Idc
M3	4.026(W-0.02)	Sqrt[15.77(W-0.02)^2+1.248]	8.07 Idc
M4	4.026(W-0.02)	Sqrt[10.68(W-0.02)^2+1.842]	8.07 Idc
M5	4.026(W-0.02)	Sqrt[8.08(W-0.02)^2+2.436]	8.07 Idc
M6	4.026(W-0.02)	Sqrt[6.49(W-0.02)^2+3.030]	8.07 Idc
M7	4.026(W-0.02)	Sqrt[5.43(W-0.02)^2+3.624]	8.07 Idc

Table 5.1 – Metal thickness rule at T=105°C

$Tj=110^oC$

Metal Level	Idc(mA)	Irms(mA)	Ipeak-DC(mA)
M1	2.116(W-0.02)	Sqrt[92.55(W-0.02)^2+0.484]	23.58 Idc
M2	2.806(W-0.02)	Sqrt[29.68(W-0.02)^2+0.484]	11.57 Idc
M3	2.806 (W-0.02)	Sqrt[15.55(W-0.02)^2+0.484]	11.57 Idc
M4	2.806 (W-0.02)	Sqrt[10.54(W-0.02)^2+0.484]	11.57 Idc
M5	2.806 (W-0.02)	Sqrt[7.97(W-0.02)^2+0.484]	11.57 Idc
M6	2.806 (W-0.02)	Sqrt[6.41(W-0.02)^2+0.484]	11.57 Idc
M7	2.806 (W-0.02)	Sqrt[5.36(W-0.02)^2+0.484]	11.57 Idc

Table 5.2 – Metal thickness rule at T=110°C

$Tj=125^oC$

Metal Level	Idc(mA)	Irms(mA)	Ipeak-DC(mA)
M1	0.759(W-0.02)	Sqrt[88.93(W-0.02)^2+0.484]	65.79 Idc
M2	1.007(W-0.02)	Sqrt[28.51(W-0.02)^2+0.484]	32.23 Idc
M3	1.007 (W-0.02)	Sqrt[14.94(W-0.02)^2+0.484]	32.23 Idc
M4	1.007 (W-0.02)	Sqrt[10.13(W-0.02)^2+0.484]	32.23 Idc
M5	1.007 (W-0.02)	Sqrt[7.66(W-0.02)^2+0.484]	32.23 Idc
M6	1.007 (W-0.02)	Sqrt[6.16(W-0.02)^2+0.484]	32.23 Idc
M7	1.007 (W-0.02)	Sqrt[5.15(W-0.02)^2+0.484]	32.23 Idc

Table 5.3 – Metal thickness rule at T=125°C
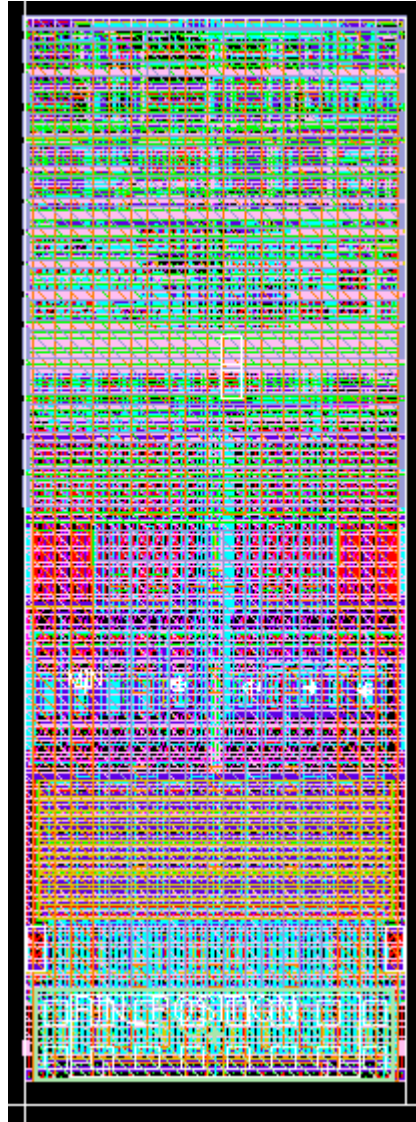
Figure 5.3 - layout view corresponding to BD2SCARDQP_2V5_LIN

Layout of the leaf cells that constituted the above mentioned top cell has been placed in the **APPENDIX I**

Chapter 6

VALIDATION FLOW AND ANALYSIS OF RESULTS

Usually an I/O library consists of

- Level converter
- Schmitt trigger
- Multiplexer
- Slew rate controller

There may be other blocks to which may be designed as per according to specifications and their necessity.

After the completion of design, there is a necessity of SPICE regression of that particular library. Regression is nothing but to simulate the library to check the parameters of the circuit are within in specifications or not.

Before discussing the regression of the library, let's discuss the flow of tools, which are used in regression of libraries.

6.1 Flow for simulation of library

- A particular library is given which has to be regressed.
- As per according to the library requirement, a particular version of design kit (DK) is chosen i.e. a compatible DK
- Various tools which are compatible with the DK are sourced in the directory namely
  - ➢ UNIOPUS
  - ➢ Calibre
  - ➢ Artist kit
  - ➢ AMS
  - ➢ Unicad utilities

Above mentioned tools are from CADENCE, MENTOR GRAPHICS and ST MICROELECTRONICS

- ▪ The library is launched in OPUS from where GDSII file is extracted. GDSII file is extracted from layout of the circuit.
- ▪ Next CDL file is extracted which is the netlist of the schematic view.

A schematic contains the information about the design, various transistors, their parameters like aspect ratio and some passive elements. Schematic is just a symbolic representation of the circuit in design. Actual physical data that goes into Chip is layout. Virtuoso Layout Editor (Opus) is used to make layouts. The schematic contains all the information and simulations are run on the netlist to check whether the results are in desired range. With the help of the schematic layouts are designed.

- ▪ After extracting CDL file and GDS file, post layout netlist is extracted for post layout simulation (PLS). This netlist includes all the parasitic capacitances whether they are of wires or of any nodes and any other parasitic if present including the connectivity of all the components.
- ▪ A particular directory structure is made for running out the simulation as shown below
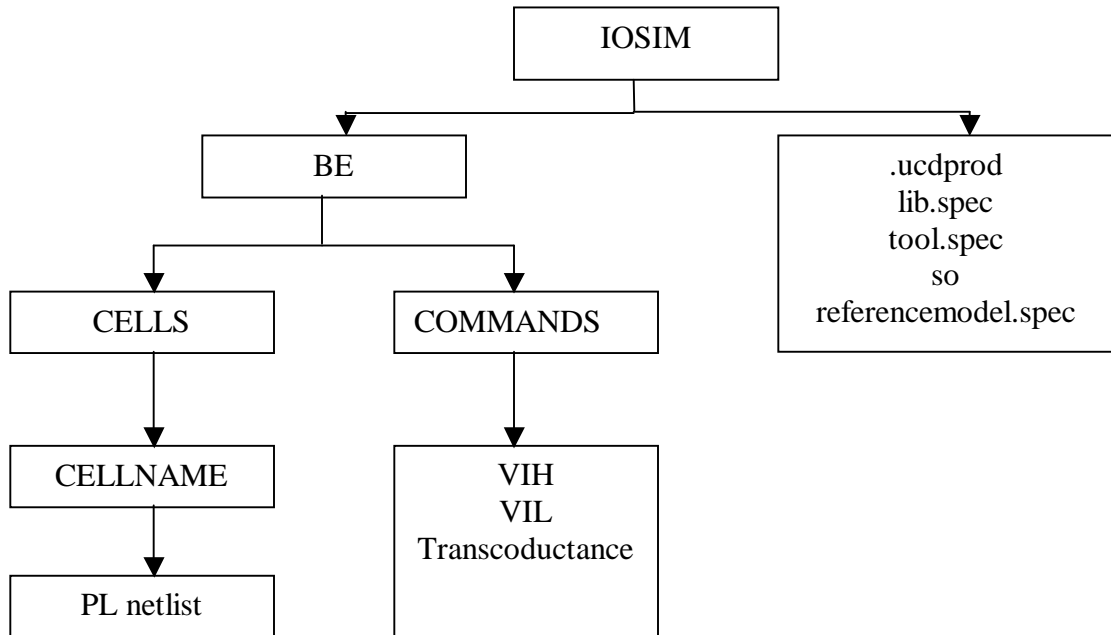
Figure 6.1 Directory structure for simulation

IOSIM is a tool used for running out the simulation at different process corners, voltage and temperature (PVT conditions). Different process corners i.e. nfps, nspf, nsps, nfpf,

different operating voltages and different temperatures are considered for simulation. These process corners are defined in the file *lib.spec,* this file refers to *referencemodel.spec* from where the path of all process corners is set. In *netlist*, post layout netlist which was extracted earlier is placed in *netlist.*

Finally a command is run

Iosim simu –command VIH –cell CELLNAME –netlist netlist –measure lib.spec

This command is going to execute which will extract required electrical parameters from the command file. Command file for various parameters are written in SPICE code. These commands files vary from circuit to circuit.

For detailed schematic views refer **Appendix III**
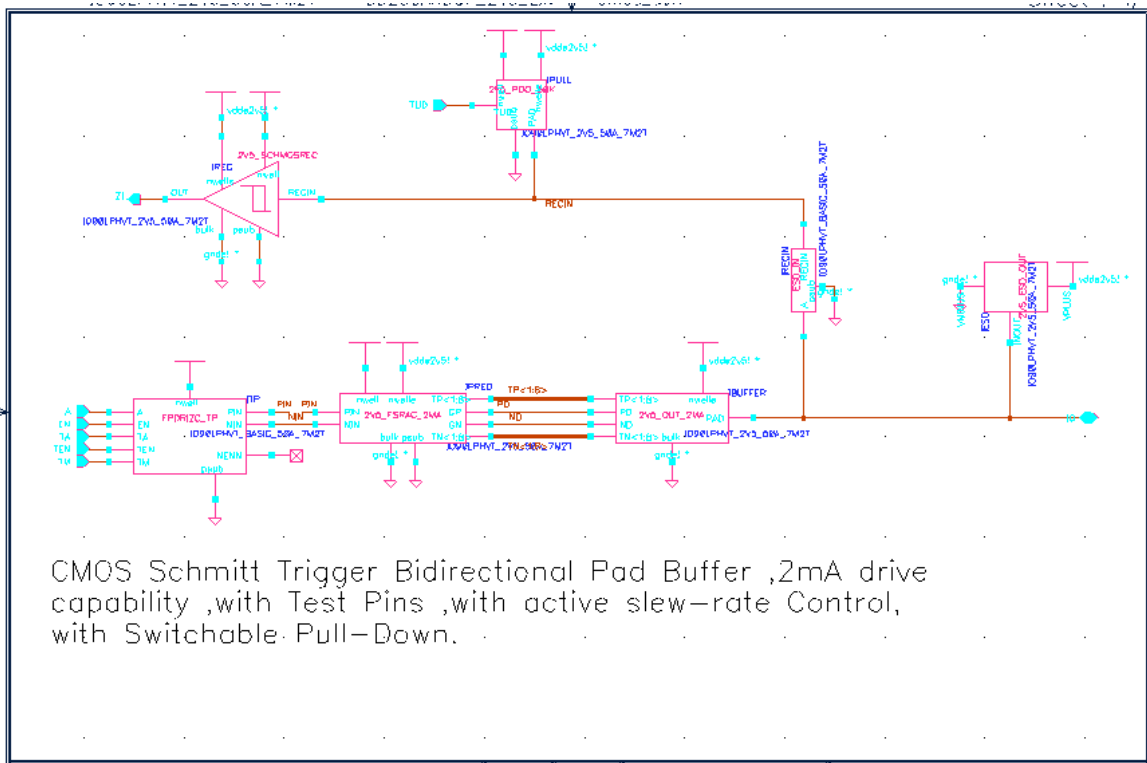
Figure 6.2 - Block diagram of BD2SCARDQP_2V5_LIN

6.1.1 Eldo simulations and effect of changing W/L

Symbols and notations used in the tables

Wp - P Transistor Width

Wn - N Transistor Width

PW - Pulse Width

Rd - Rise Delay

Fd - Fall Delay

Rt - Rise Time

Ft - Fall Time

VM - Maximum Output Voltage

vm - Minimum Output Voltage

Isr - Current Sourcing Capability

Isn - Current Sinking Capability

Sf - Falling Edge Slew Rate

Sr - Rising Edge Slew Rate

+ - Increase in the value

++ - Large Increase in the value

- Decrease in the value

- - Large decrease in the value

* - No change in the value

< - Slight decrease in the value

> - Slight increase in the value

Observed values at different widths of transistors are compared with values obtained at the normal width of transistors

Wp	Wn	PW	Rd	Fd	Rt	Ft	VM	vm	Isr	Isn	Sf	Sr
+	*	+	-	<	-	>	+	>	+	*	*	+
++	*	++	--	<	--	>	+	>	++	*	*	++
*	+	-	*	-	*	-	*	>	*	+	+	*
*	++	--	*	--	*	--	*	-	*	++	++	*
+	+	<	-	-	-	--	+	-	+	+	+	+
++	++	<	--	--	--	--	+	--	++	++	++	++

Table 6.1 - Results obtained while changing the width of transistors in the 2V5_OUT_2MA block of the bi-directional buffer BD2SCARDQP_2V5

Conclusion

- When width of only p transistors are increased pulse width, rising edge slew rate, max output voltage and current sourcing capability of the buffer increases while rise delay and rise time decreases.

- When width of only n transistors are increased current sinking capacity and falling edge slew rate increases but pulse width, fall delay, fall time and minimum output voltage decreases.

- When width of both p and n are increased, the output response has mixed characteristics of above both cases as pulse width, fall and rise delay, fall and rise time and voltage minimum all goes down whereas current sourcing and sinking, rising and falling slew rate, voltage maximum all sees large hike in their values except pulse width which gets a slight up shift in its value.

Explanation

- Number of carriers in a transistor depends upon the width of the transistor. By increasing the width of transistor, we actually increase the number of carriers and thereby reducing the resistance offered by the channel. This results in high current

sourcing capacity of the transistor in case of p transistors. When high current flows through the circuit, time for charging goes down, which means reduction in rise time and this forces the circuit to attain a high value of voltage within the same time period and consequently reducing the delay. Again as the charging current is high and the rise time is low therefore the rate of change of current, which is nothing but the rising edge slew rate, increases. Due to reduction in time taken for charging, the positive edge delay of the output signal goes down and the width of the output increases.

- When the width of n transistor is increased we actually introduce more number of free electrons in the transistor and this increase in charge reduces the resistance. Now this time the current sinking capacity of the circuit goes up and due to reduction in resistance offered by the channel, the discharging time decreases, which means the output is pull down to ground in less time, thereby decreasing the fall time and the falling edge delay. As the circuit has to discharge large amount of charge in less time, the rate of change of sinking current increase in the circuit and that's why we observed that when we had increased the width of n transistor, the falling edge slew rate was increased. A major difference between the action of the present case and the previous case on the width of the output signal is, the pulse width increases in case of p transistors and decreases in case of n transistors and the reason for this behavior is that in both the cases, the rising and falling edge gets a shift towards the reference axis and when only the n transistor is made large, only the falling edge gets a shift which means decrease in the time difference between falling and rising edge.

- When the width of both n and p transistor is increased, the number of holes and electrons in p and n transistor is increased respectively. Consequently a large amount of current can now be sinked or sourced from the transistor. This lowers the time taken by the circuit to charge or discharge the circuit thereby reducing rising and falling time, rising and falling edge delay. Both the slew rates get a up shift in their value. There is a shift in the value of maximum output voltage and minimum output voltage because the circuit can be charged or discharged more quickly within the time period.

Wp	Wn	PW	Rd	Fd	Rt	Ft	VM	vm	Isr	Isn	Sf	Sr
+	*	-	*	-	*	>	*	*	*	+	+	*
++	*	--	*	--	*	-	*	*	*	++	++	*
*	+	+	-	<	>	>	<	>	+	*	*	+
*	++	++	--	<	-	>	+	-	++	*	*	++
+	+	+	-	-	>	-	+	>	+	+	+	+
++	++	+	--	--	-	-	+	-	++	++	++	++

Table 6.2 - Results obtained while changing the width of transistors in the 2V5_FSRAC_2MA block of the bi-directional buffer

Conclusion

The FSRAC block is used to control the slew rate of the buffer. From the table one can draw conclusions that as we increase the width of p transistors in the circuit keeping the width of n transistors constant, the buffer gives an output with higher values of falling edge slew rate and sinking current but lower values of pulse width, fall delay and fall time .The changes has no effect on rise delay, rise time, maximum and minimum output voltage, sourcing current capacity and rising edge slew rate.

- A different set of changes can be seen in the output response when the n width of transistors is increased. Pulse width, rising slew rate, and sourcing current all shoots up whereas the effect on rise delay, rise time, fall time, minimum voltage is opposite, and no effect on sinking current and falling slew rate.

- An increase in values of sourcing and sinking current, rising and falling slew rate, maximum output voltage and pulse width is seen when both n and p transistors are made large. The same change has opposite effect on rising and falling delay, rising and falling time, and minimum voltage.

Explanation

- In the first case, only the width of p transistor is increased, and therefore the resistance in that path is decreased. We see the FSRAC block; NIN and PIN signal is applied to the two different inverters, which has an extra p and n transistor connected respectively to their inverters. Basically by changing the width of n and p transistors we are changing the width of these extra-connected transistors. The output from inverter connected to NIN, drives the n transistor in output section of the buffer. This inverter has an extra p transistor, connected between VDD and p transistor of the inverter, when the width increases, the resistance in charging path decreases and as the two p transistors are in series, the output is a smooth curve. By controlling the characteristics, that is the smoothness of the output, we actually control the Vgs of the n transistors in output section. Consequently the strength of the sinking current increases, which increases the falling edge slew rate of the buffer. The other effects are also due to increase in the sinking current strength.

- When the width of n transistor increases, resistance in the discharging path of the FSRAC block decreases. This controls the output characteristics of the inverter connected to PIN signal. The output has a smooth curve which drives the p transistors to the output section .By changing the characteristics of the output of the inverter connected to PIN signal, we actually change the characteristic of the applied voltage at gate of p transistors. Therefore the current sourcing capability of the buffer increases and hence the rising edge slew rate increases.

- By increasing the width of both n and p transistors in the FSRFC block, the gate voltage of n and p transistors in the output section smoothens and thereby the sourcing and sinking capability of the output section increases but in continuous manner due to smooth change in Vgs. This results in higher sinking and sourcing current and therefore increase in rising and falling edge slew rate at the output.

6.1.2 Simulation results for the Bi-directional Buffer (refer to Appendix III)

DC I/P threshold

	Parameter	Minimum	Maximum	Unit
VIH	Input high voltage	1.322	1.622	V
VIL	Input low voltage	0.876318	1.168	V
VHYST	Hysteresis	0.393727	0.562903	V

Table 6.3 – DC I/P threshold

Figure 6.3 – VIH minimum

Figsure 6.4 – VIH maximum
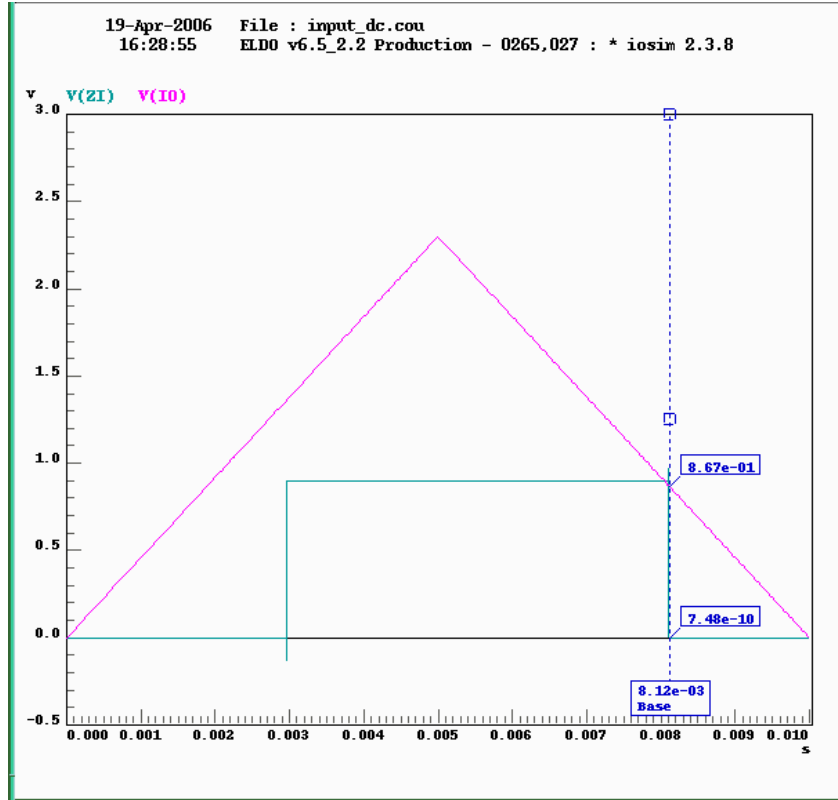
Figure 6.5 – VIL minimum

Figure 6.6 – VIL maximum

Figure 6.7 – Minimum hysteresis

Figure 6.8 – Maximum hysteresis

INPUT TRANSIENTS at 100MHz

PARAMETER	MINIMUM	MAXIMUM	UNIT
Delay fall	0.421	1.4702	ns
Delay rise	0.363	0.9641	ns
Duty cycle	49.206	56.874	%
Fall time	4.514	6.1473	ns
Rise time	0.44812	1.3849	ns

Table 6.4 – Input transients
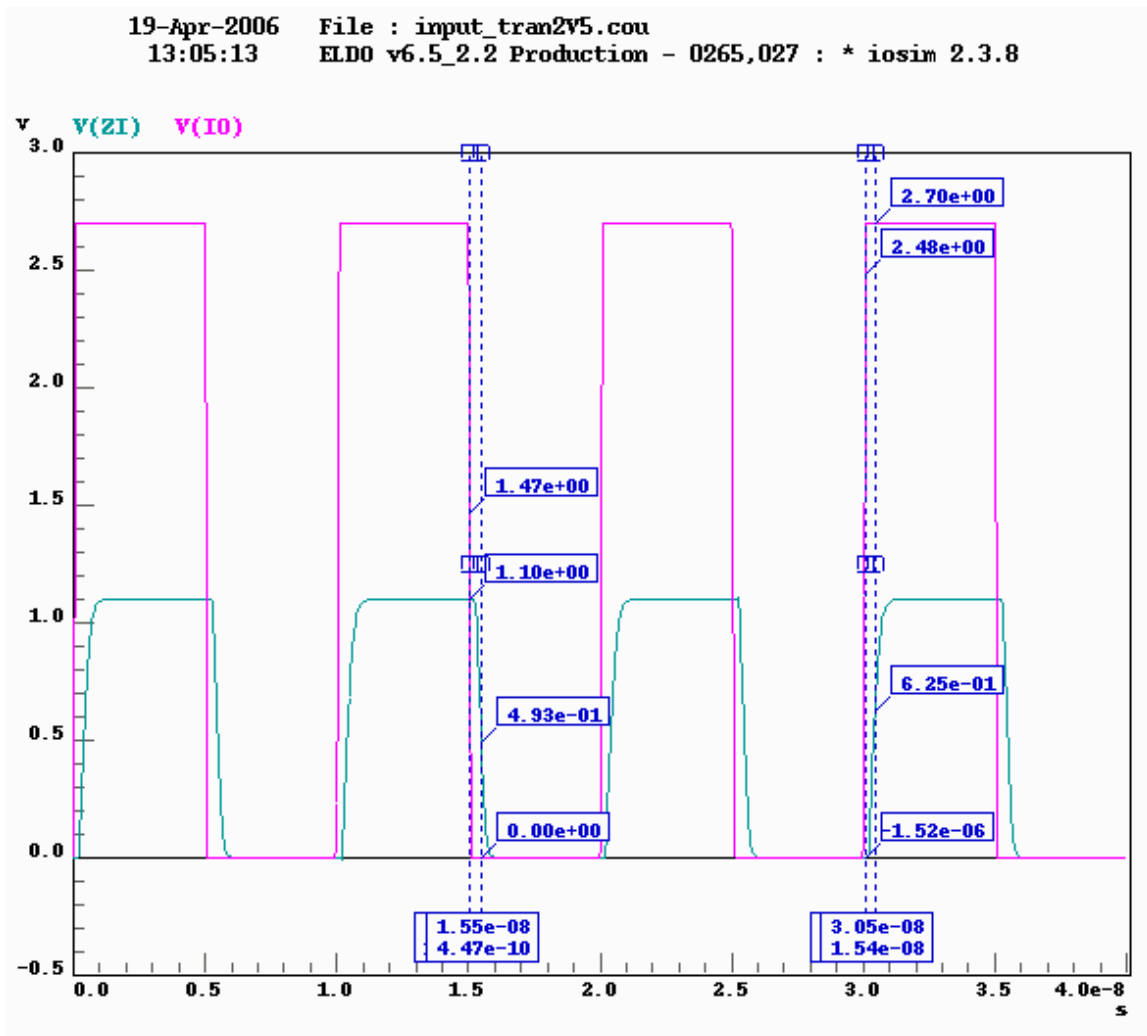
Figure 6.9 – Minimum Delayfall and Delayrise time in O/P w.r.t. I/P in I/P buffer
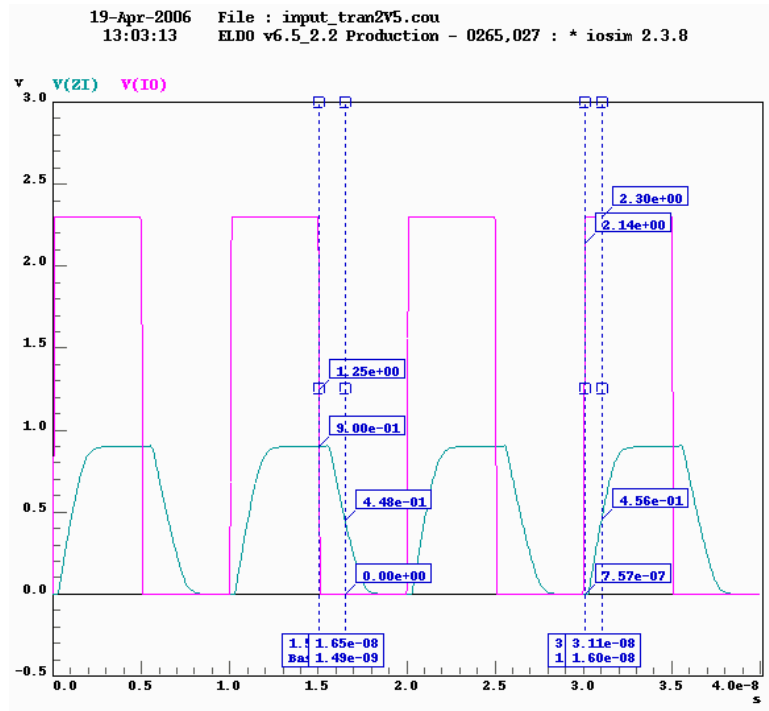
Figure 6.10 - Maximum Delayfall and Delayrise time in O/P w.r.t. I/P in I/P buffer
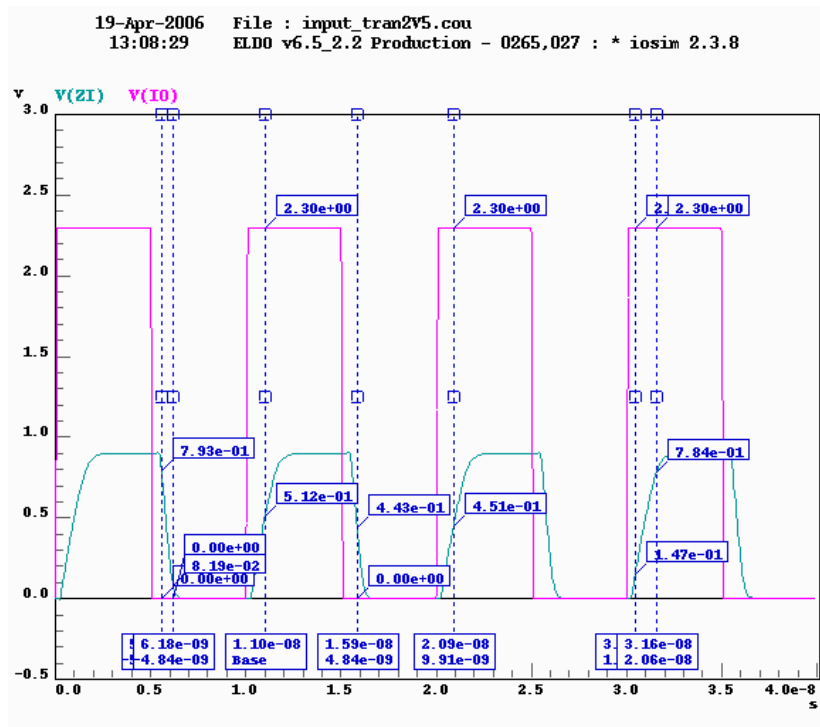
Figure 6.11 – Minimum Duty cycle and fall time in I/P buffer
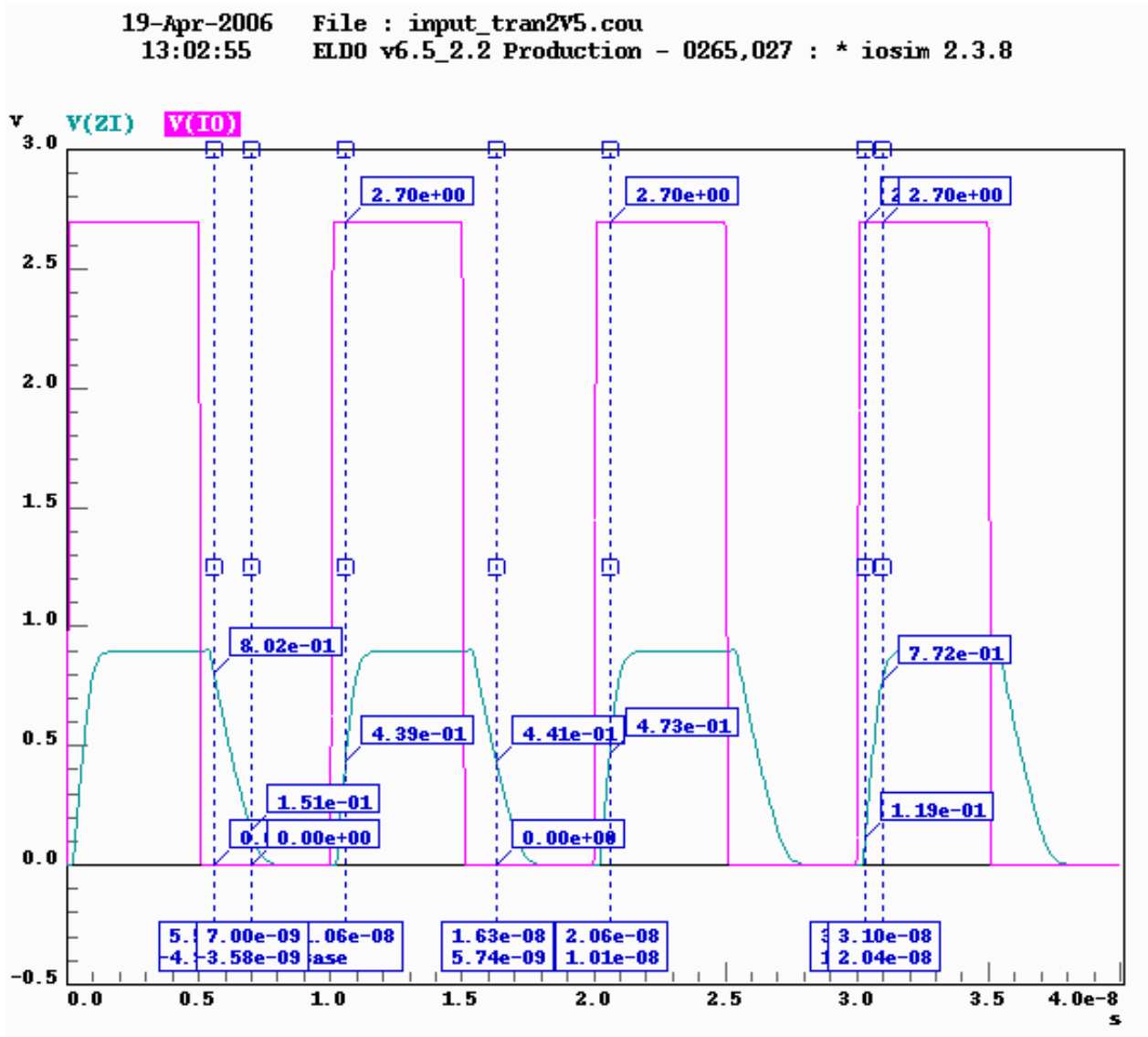
Figure 6.12 – Maximum duty cycle and fall time in I/P buffer
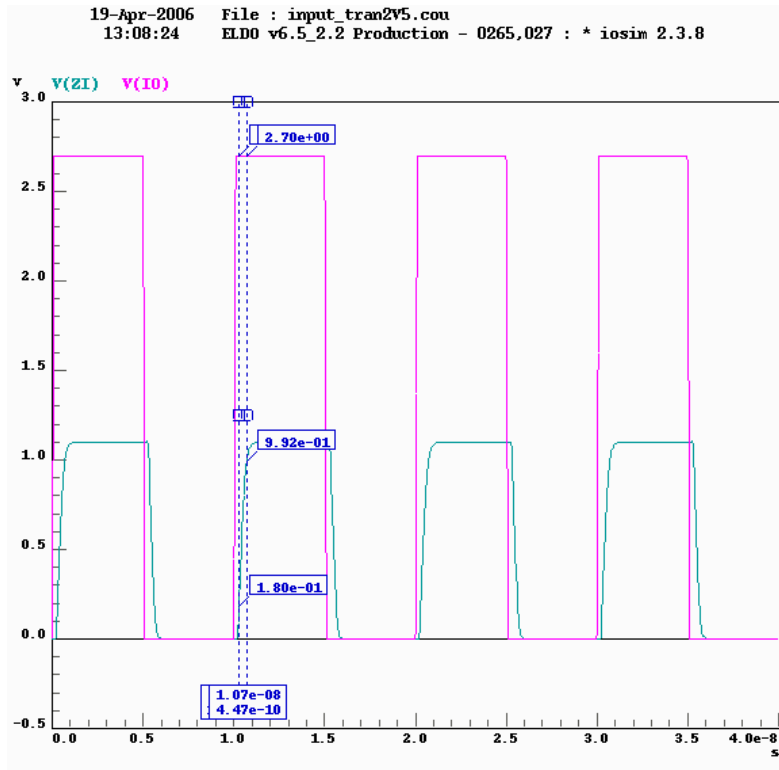
Figure 6.13 – Minimum rise time in I/P buffer
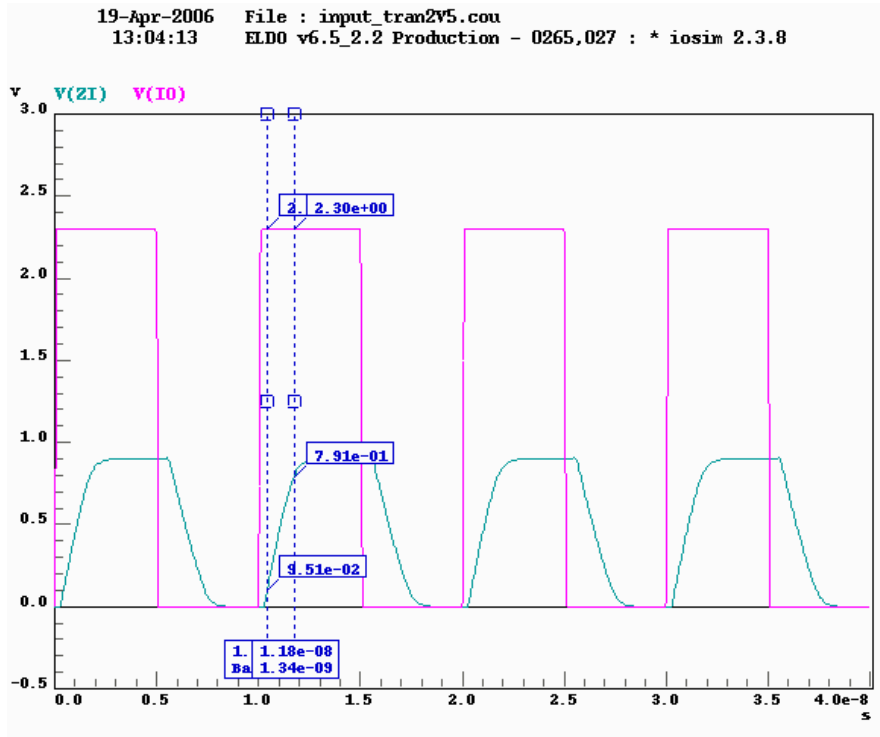
Figure 6.14 – Maximum Rise time in I/P buffer

PARAMETER	MINIMUM	MAXIMUM	UNIT
PULL DOWN CURRENT	29.47	95.924	uA
PULL DOWN RESISTANCE	78.045	28.147	Kohm

Table 6.5 – Pull down current and pull down resistance
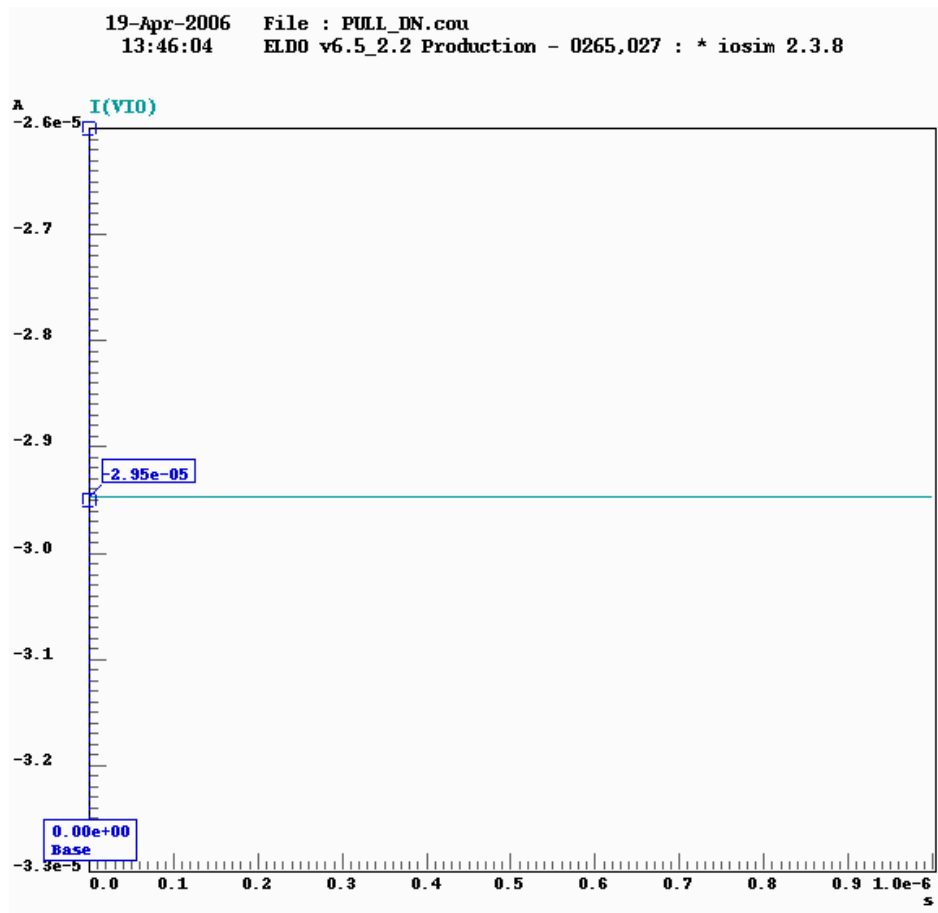
Figure 6.15 – Minimum pull down current

```
         19-Apr-2006    File : PULL_DN.cou
         13:46:19       ELDO v6.5_2.2 Production - 0265,027 : * iosim 2.3.8
```
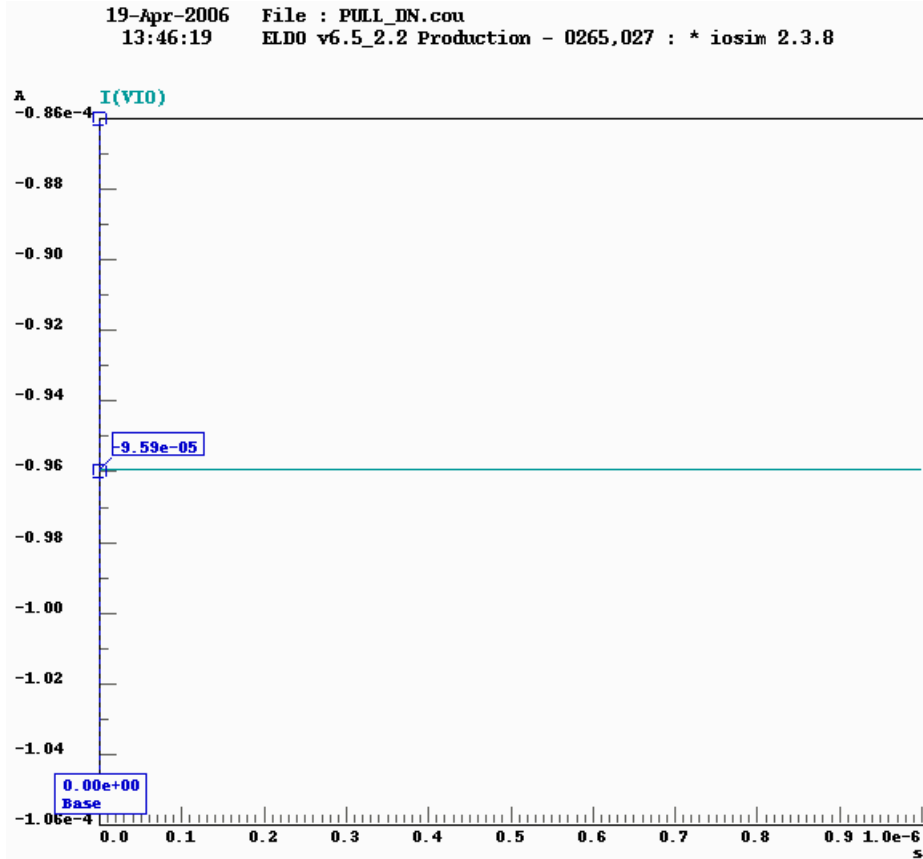

Figure 6.16 – Maximum pull down current

O/P SECTION   (DRIVE STRENGTH)

PARAMETER	MINIMUM	MAXIMUM	UNIT
Sink Current	2.682	4.8117	MA
Source current	2.6924	3.8919	MA

Table 6.6 – Sink current and source current

O/P TRANSIENTS (Load = 10pf), Maximum operating Frequency=100MHz

PARAMETER	MINIMUM	MAXIMUM	UNIT
Delay fall	2.6651	4.1959	Ns
Delay rise	2.2628	3.7206	Ns
Duty cycle	50.613	59.875	%
Fall time	2.0991	3.3113	Ns
Rise time	2.2193	3.4506	Ns

Table 6.7 – Output transients
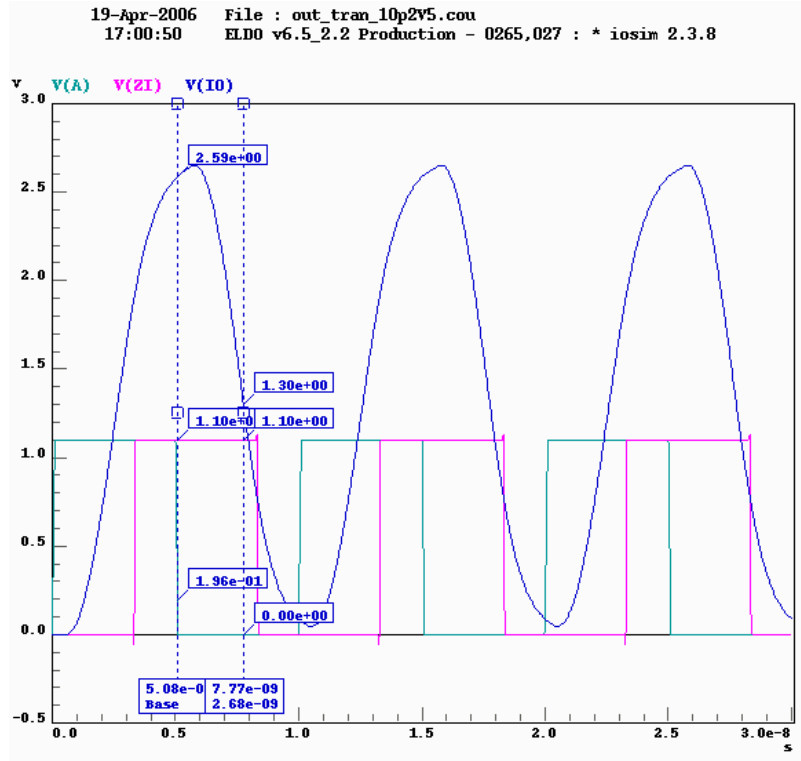
Figure 6.17 – Minimum fall time in O/P wrt input in O/P buffer
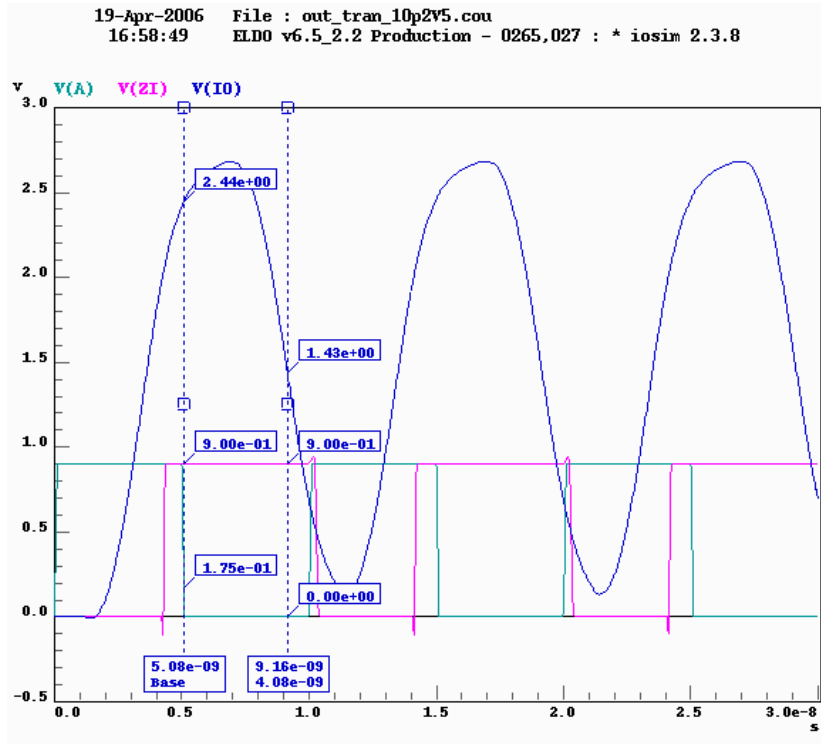
Figure 6.18 – Maximum Fall time in O/P wrt input in O/P buffer
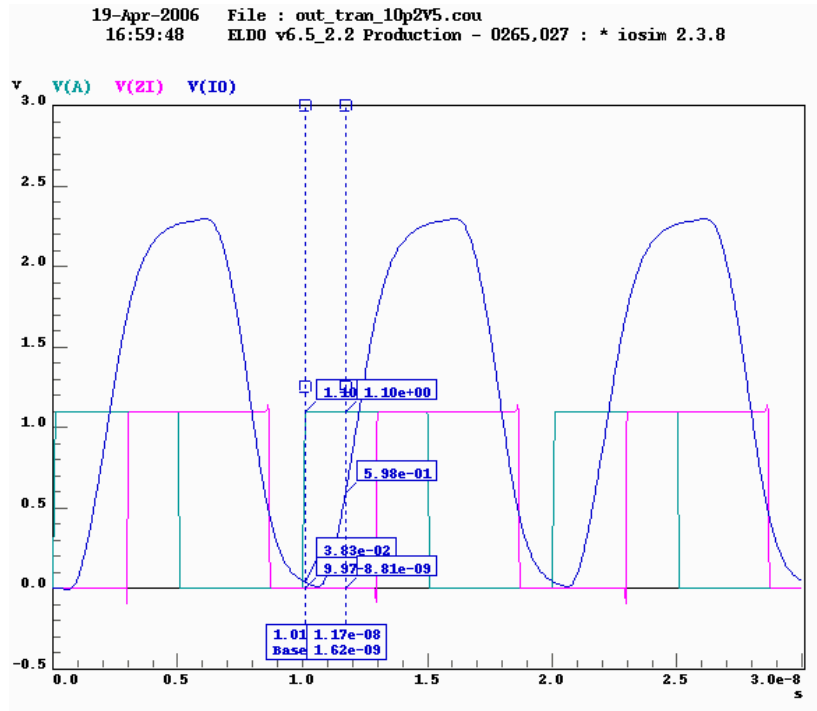
Figure 6.19 – Minimum rise time in O/P wrt input in O/P buffer
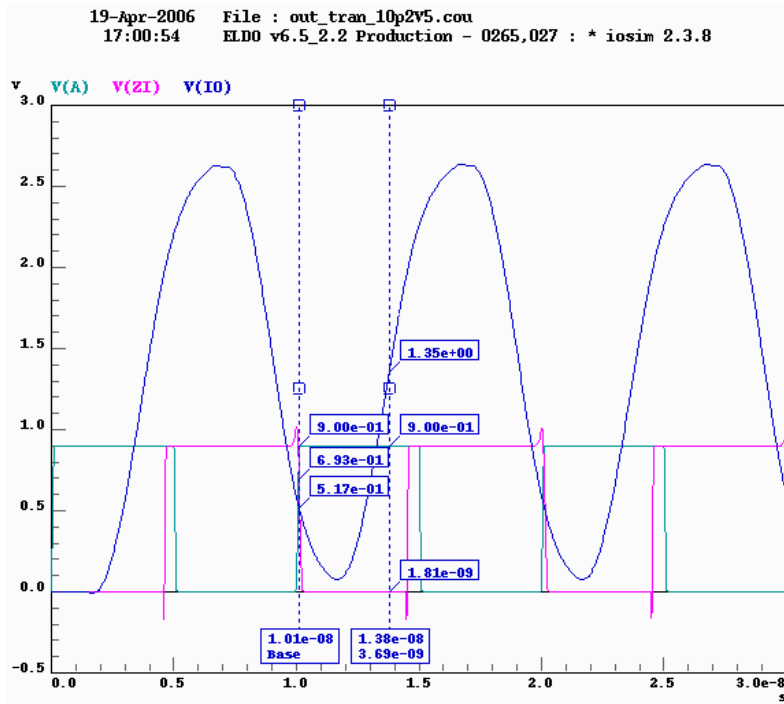
Figure 6.20 – Maximum rise time in O/P wrt to input in O/P buffer
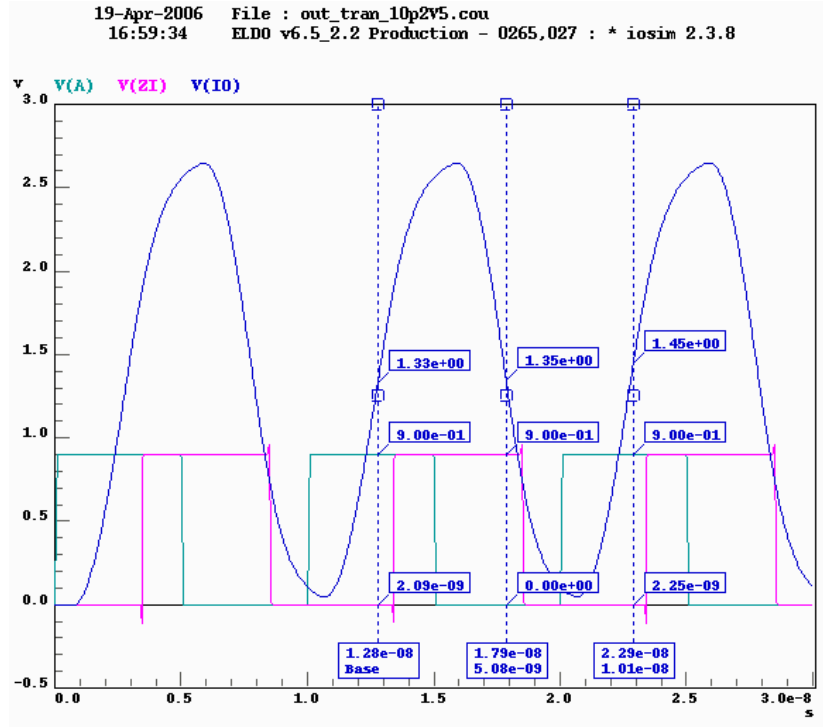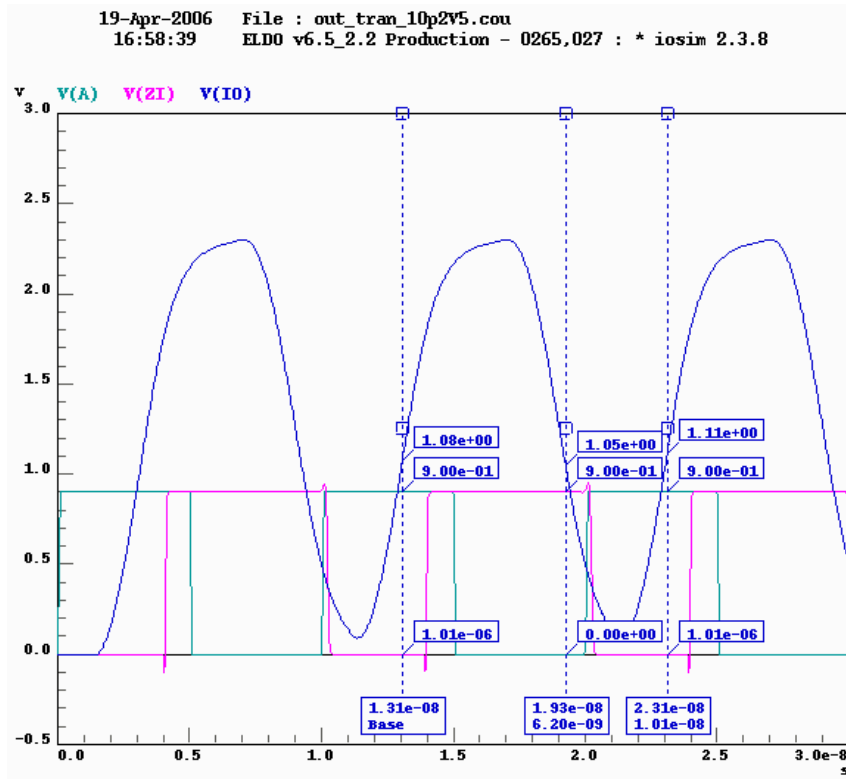
Figure 6.21 – Minimum Duty cycle in O/P buffer

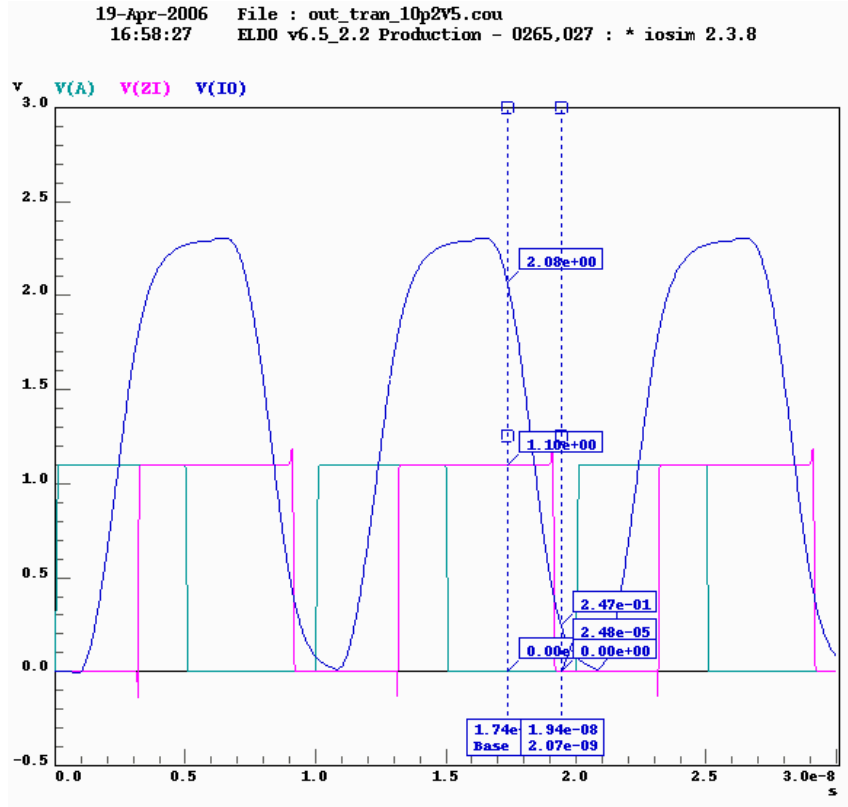**Figure 6.22 – Maximum Duty cycle in O/P buffer**
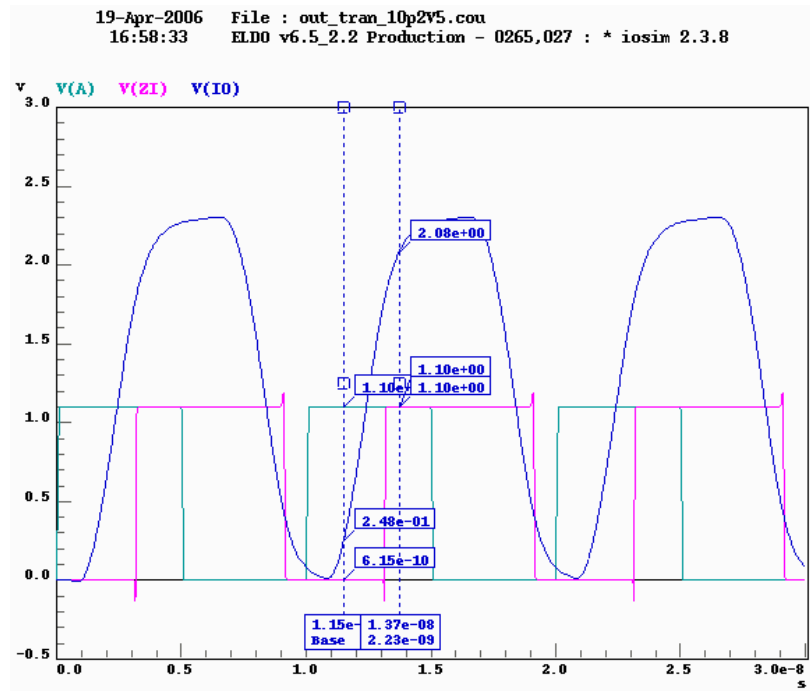
Figure 6.23 – Minimum fall Time in O/P buffer
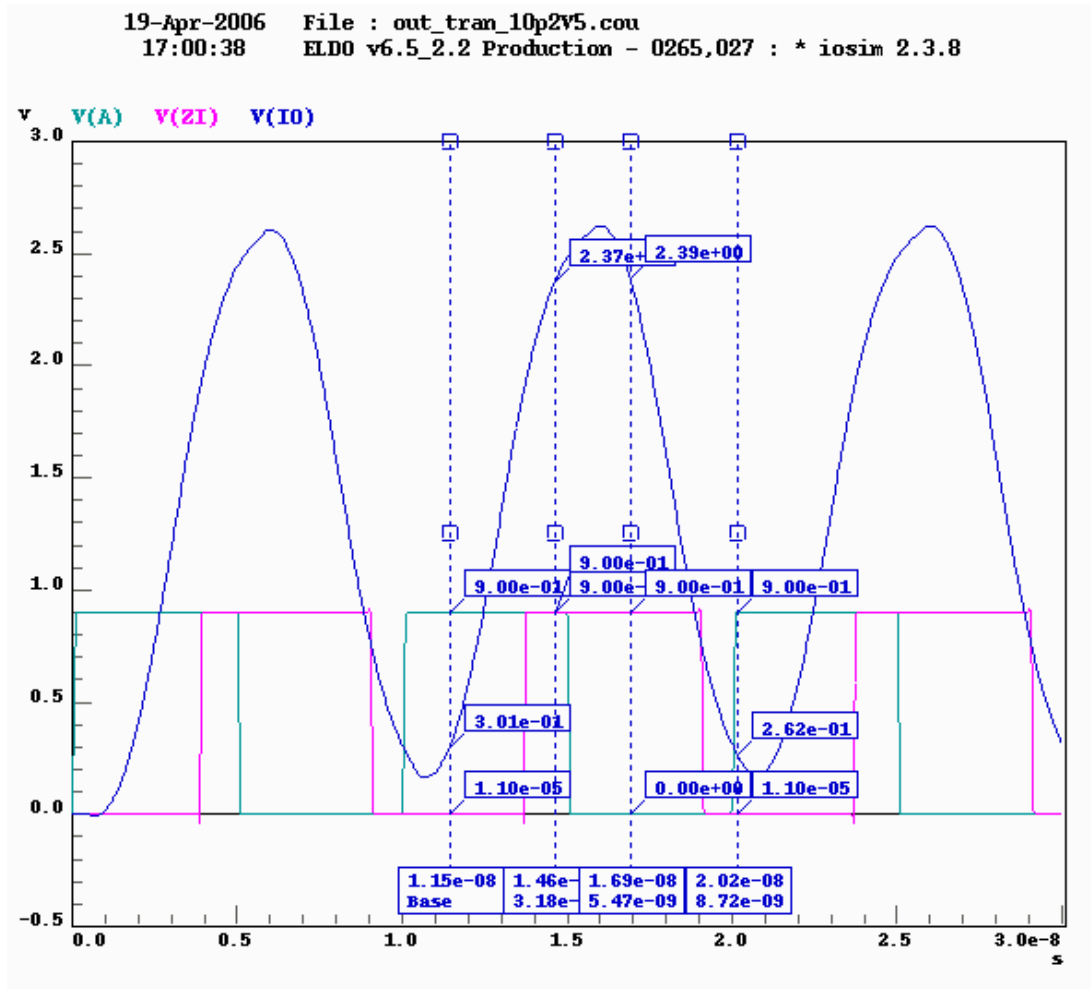

Figure 6.24 – Minimum rise time in O/P buffer

Figure 6.25 – Maximum fall time and rise time in O/P buffer

CURRENT CONSUMPTION IN BIDIRECTIONAL BUFFERS

	Parameter	-40°C		125°C		Unit
		Minimum	Maximum	Minimum	Maximum	
2 mA output	I(VDDE)	0.52e-3	0.90e-3	0.247	5.58	UA
mode	I(VDD)	63e-6	0.001	0.012	0.57	UA
2 mA input mode	I(VDDE)	0.79e-3	s0.79e-3	0.06	3.22	UA
	I(VDD)	0.60e-3	0.60e-3	0.022	0.74	UA

Table 6.8 – current consumption in bi-directional buffer

FUTURE SCOPE

The regression of libraries has been done with spice v1.4 and there is a regular updating in spice versions. As the version of spice increases, MOS model improve .As a result the design is much more near to the silicon i.e. the results which come after validation show much more same behavior as that on the silicon.

The bi-directional buffer designed above can be designed according to new specifications i.e. the latest spice versions, as with the latest spice versions, it is possible that on some corner cases the design may fail, which may need to be redesigned.

Considering the layout, although much care was taken to make the design latch up free, yet an efficient layout can be made considering all the design rule checks and latch up checks, which may result in lesser power dissipation.

The above design has been made for 90nm technology, but the technology is scaling day by day, so this design could be implemented in 65nm technology, which would be a greater challenge, as more and more defects will come into consideration as we go down further decreasing the technology.

CONCLUSION

Designing and implementation of the 2.5V IO as per the specification of the end user has been successfully achieved in the 90nm technology. Pre-layout and post-layout simulations are carried out using the BSIM4 models and are matched within the tolerance. Within the area constraint, layout has been made using the entire recommended latch up rules in the 90nm technology. And the post-layout latch-up simulation result shows that no latch rules are violated. The total chip area occupied by this IO is $7.0263*10^{-3}$ mm^2.

A comprehensive account of the I/O library elements has been presented in this work. The emphasis is on the circuit design of the several I/O cells and a basic understanding of the purpose and functionality of the library elements. Circuit and design issues relating to hysteresis and Slew rate control has also been presented. Appropriate references for topics which need a detailed analysis has been given along with for interested readers.

An I/O design today is much more than the circuit designs. The circuit limitations can be well addressed by an efficient layout of the I/O cell. Moreover it is in the intelligent layout that I/O latch up (high current through I/O make them doubly susceptible to latch up) can be prevented.

Similarly ESD protection through circuits and technological modifications has also assumed importance in an I/O design. These issues form a separate topic in themselves and hence have been left out of the present work.

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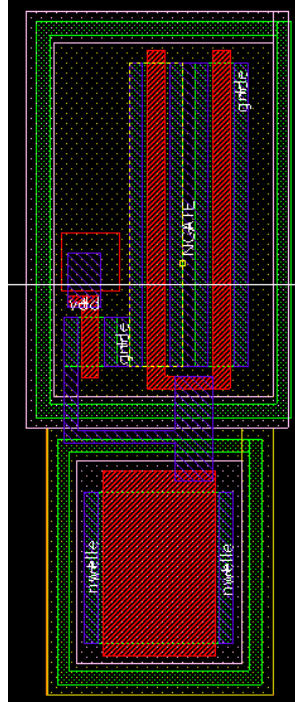[23.] Documents prepared by ST Microelectronics and JEDEC organization.

Appendix I

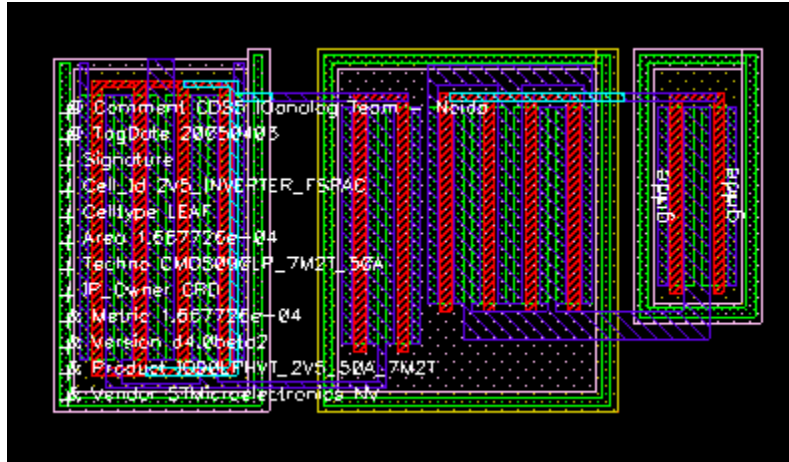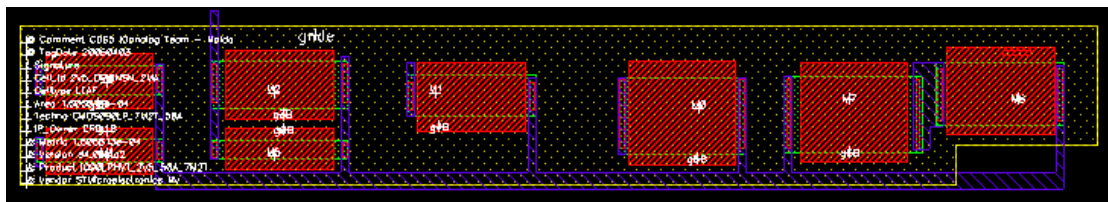**2V5_SCHMOSREC**

2V5_ESD_REC
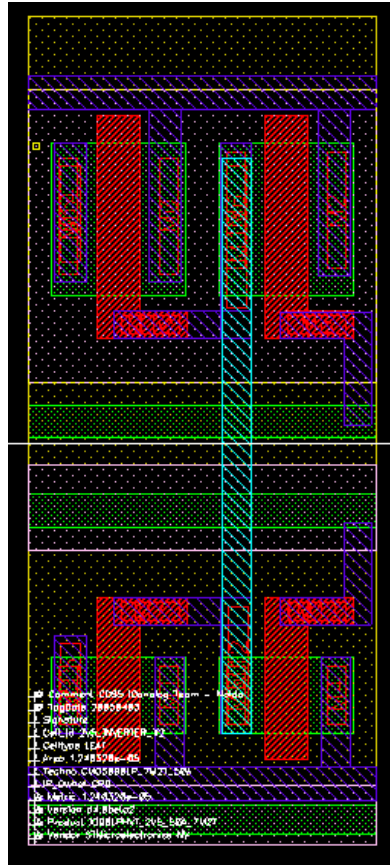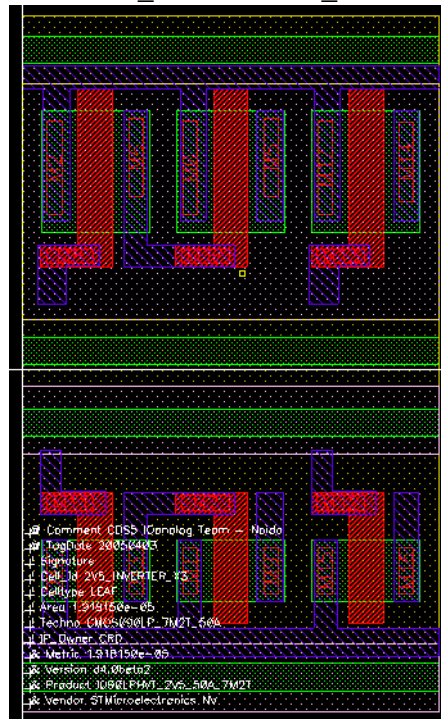
2V5_INVERTER_X2

2V5_INVERTER_X3
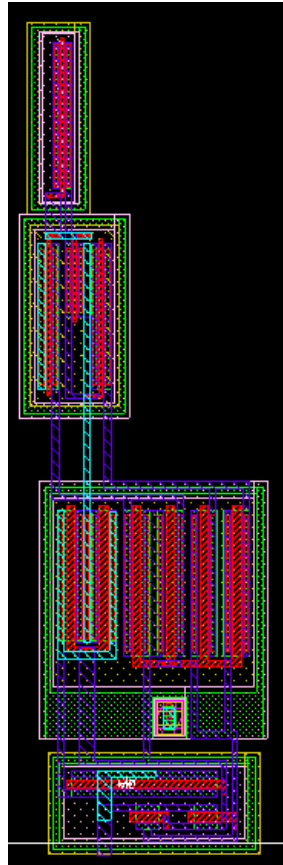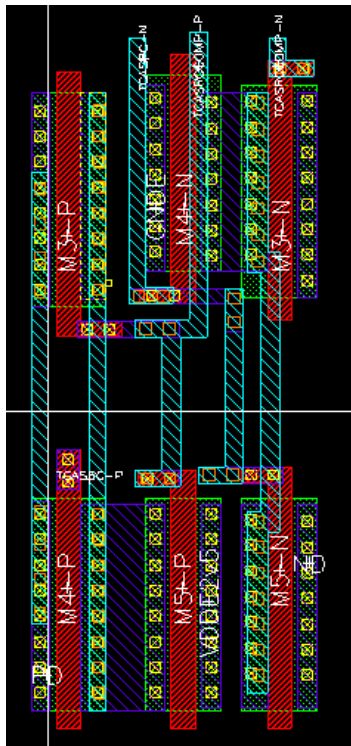
2V5_LEVELSHIFTER

2V5_NMOS_KEEPOFF

2V5_INVERTER_FSRAC
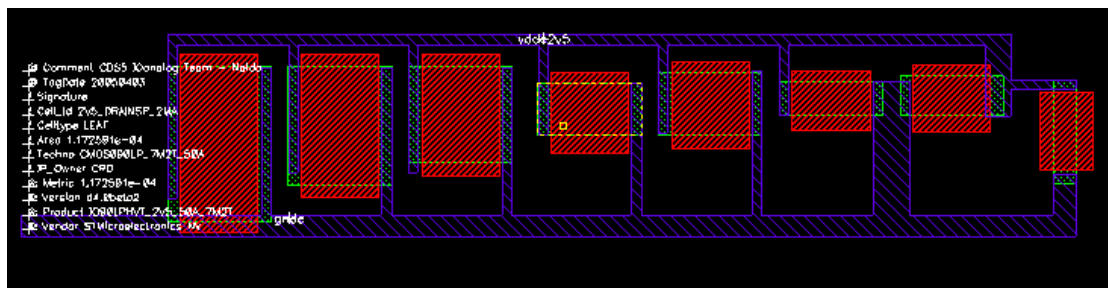
2V5_DRAINSN_2MA
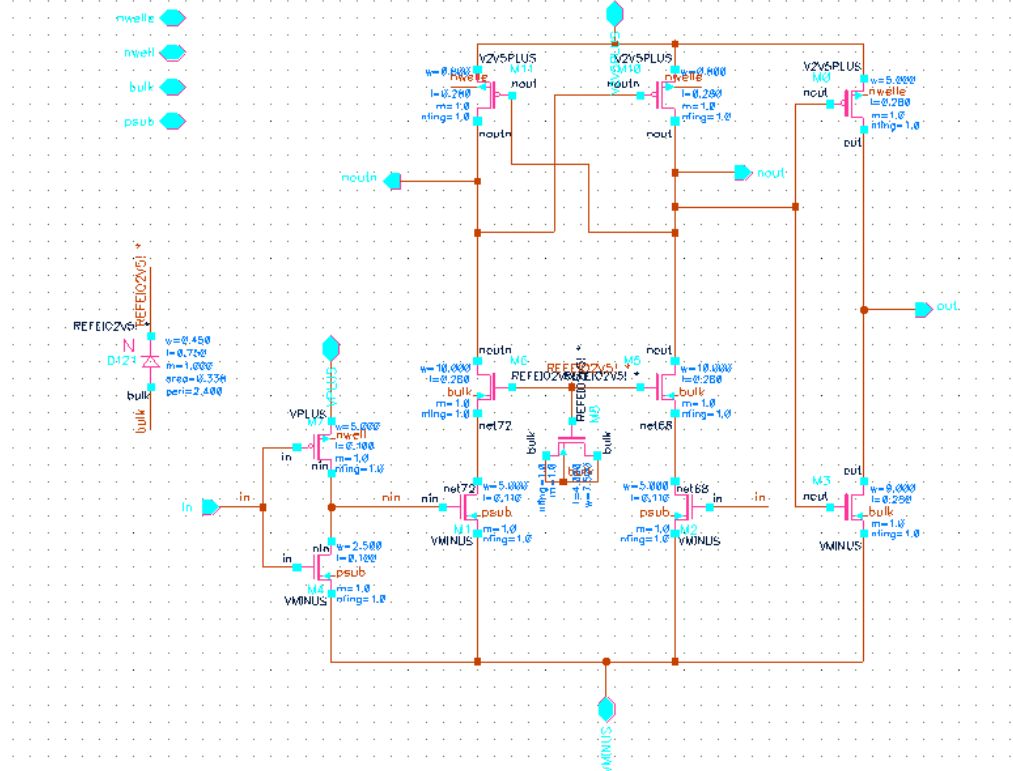

2V5_DRAINSP_2MA
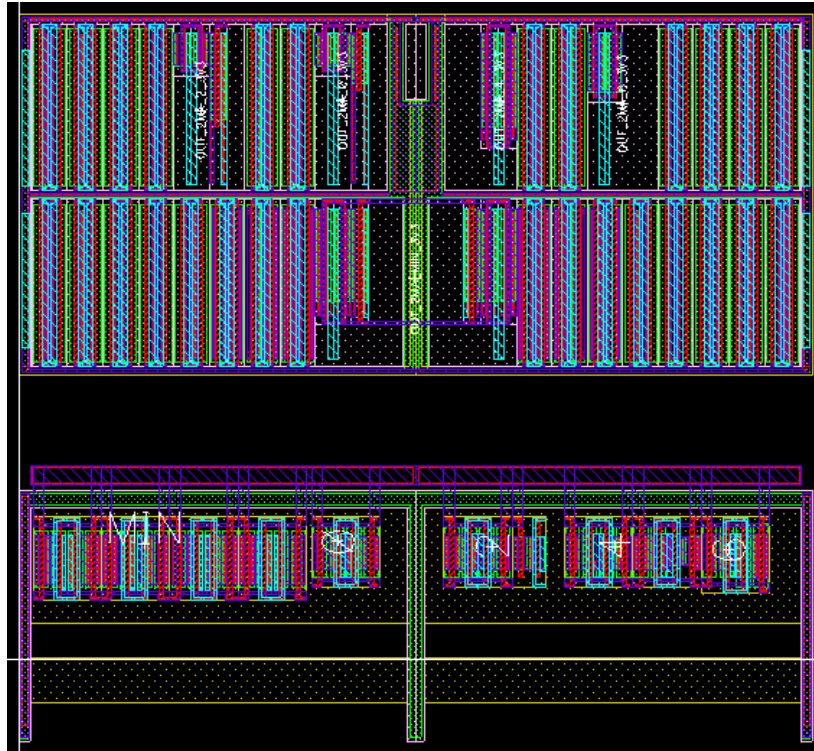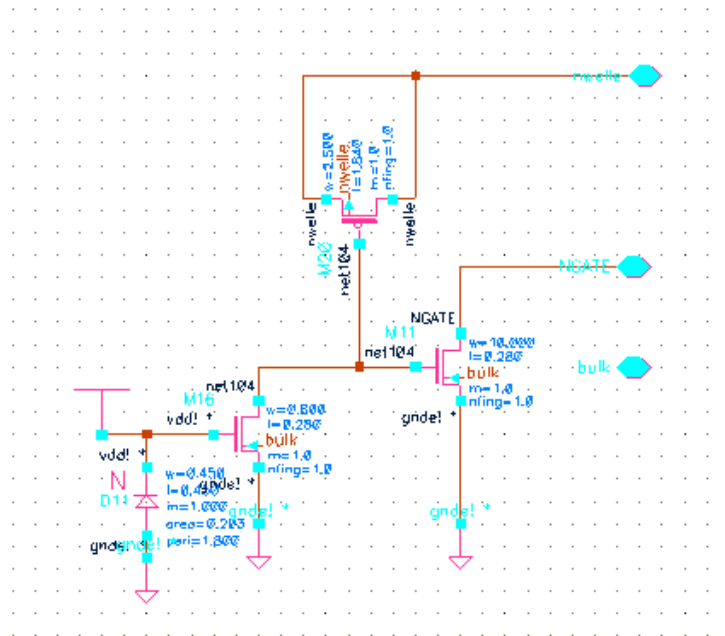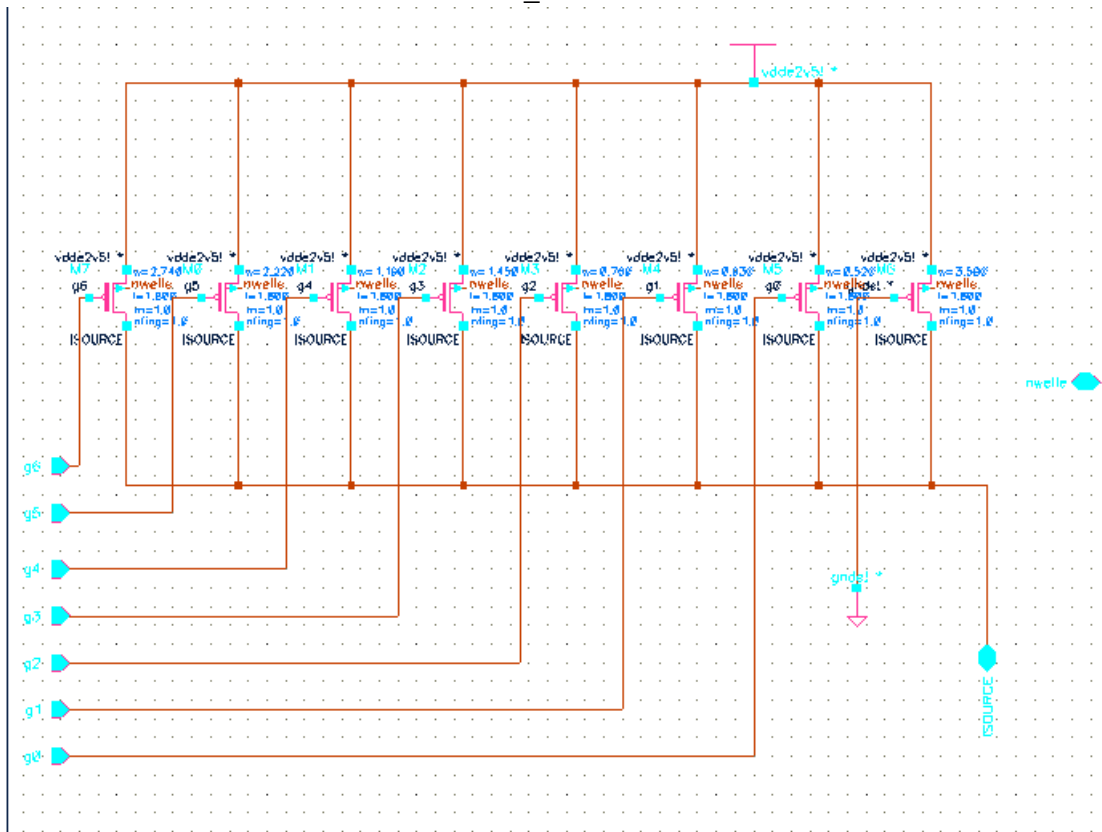
2V5_DRIVERS_2MA

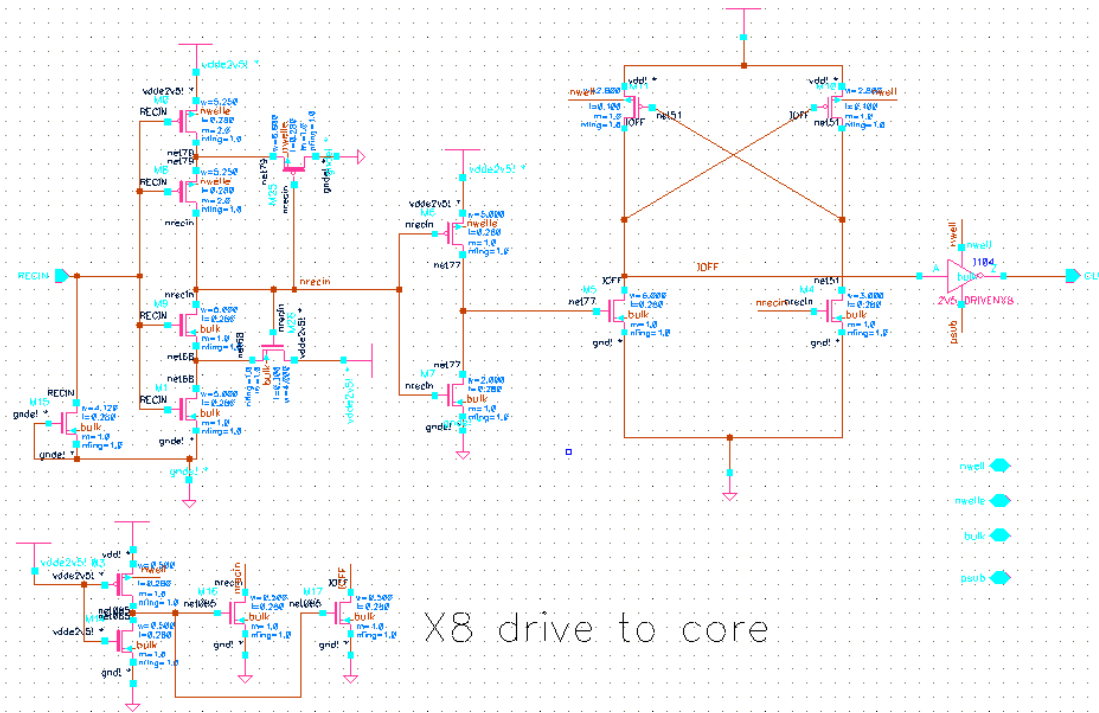**2V5_PDQ_50K**

APPENDIX II
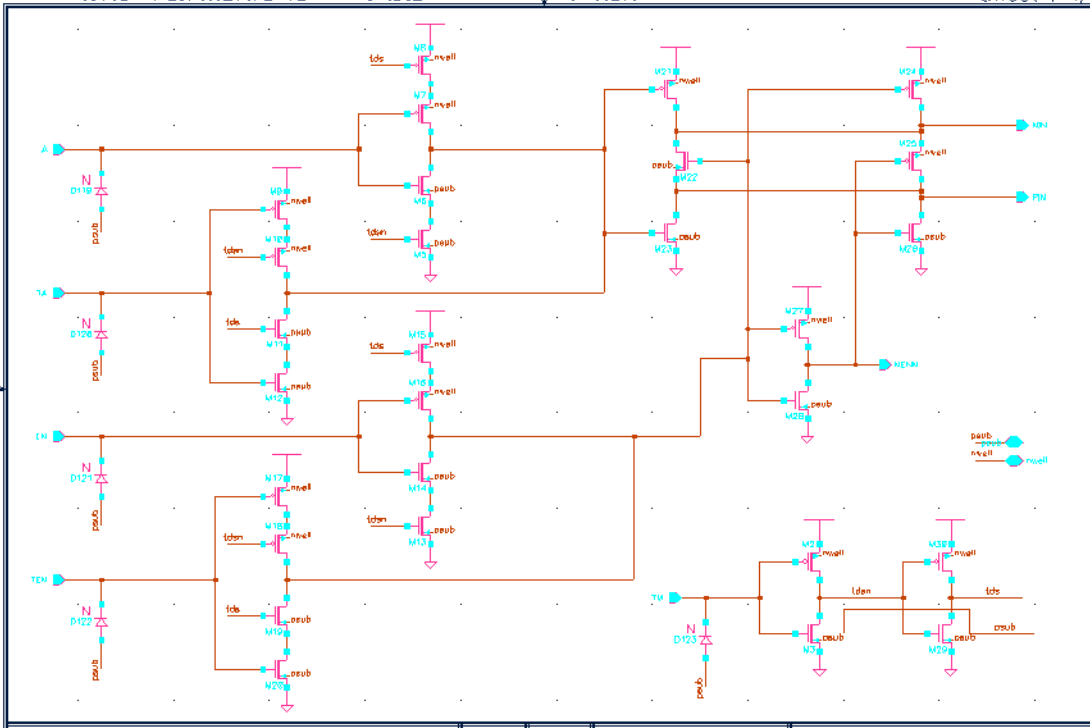
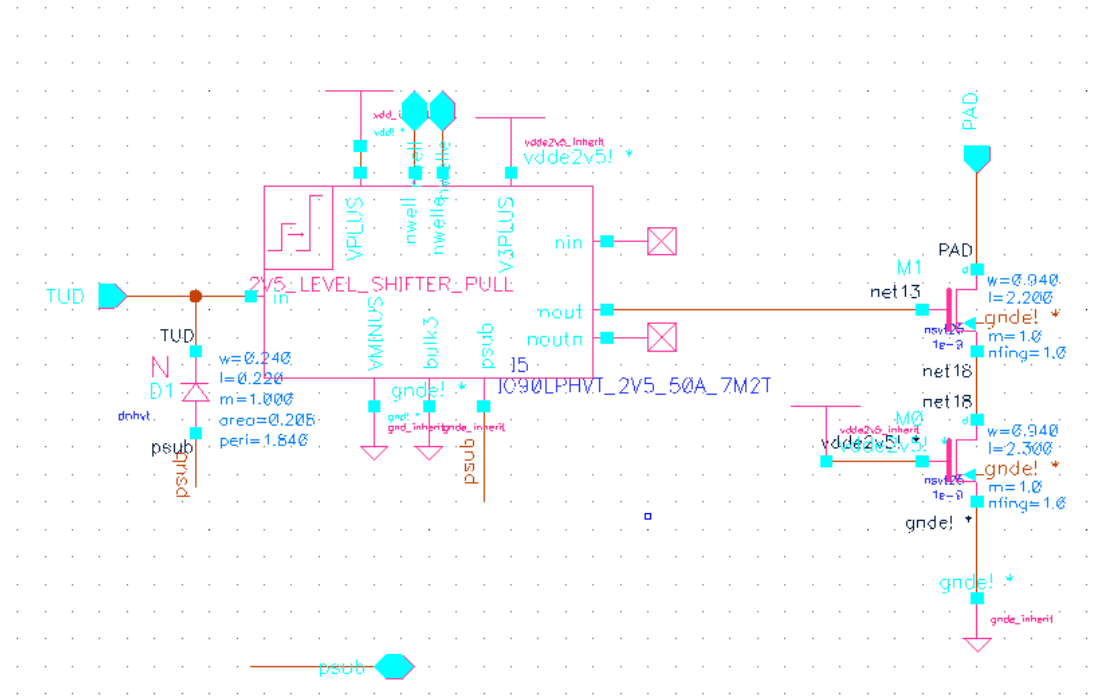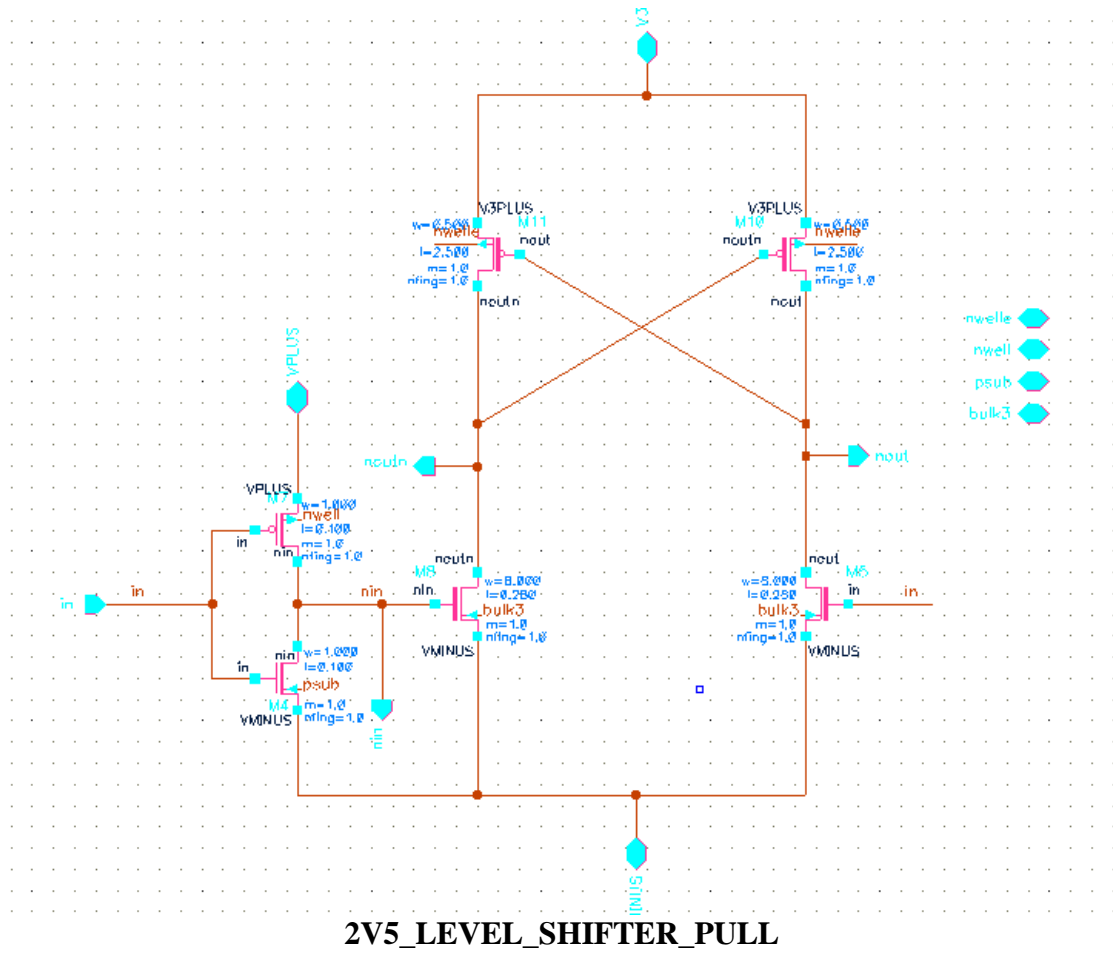**Tri state pre-driver with Test path**

LEVEL SHIFTER

NMOS_KEEPOFF

DRAINSP_2MA

DRAINSN_2MA

BASIC INVERTER

2V5_PGPD

2V5_PGND

2V5_SCHMOSREC

X8 drive to core

2V5_PDQ_50K

2V5_LEVEL_SHIFTER_PULL

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APPENDIX III
The following commands were executed in IOSIM in order to get simulation results

```
************************************
** OPTION COMMANDS**
************************************
.option limprobe=5000 XA = 3.400000e-07
.option eps=1e-8 itol=1e-12 reltol=1e-8 vntol=1e-8
.option notrc reduce nomod noascii nojwdb cou nowarn=240
.option be extmksa AEX
.param RPOLYN_DEV = 0
.param RPOLYP_DEV = 0

********* SUPPLY SIGNALS**************
VVDDE2V5 VDDE2V5 gnd dc VDDE
VVDD VDD gnd dc VDDH
.connect gnd 0
.connect gnde 0

**********MACRO SIGNALS****************************
VREFEIO2V5 REFEIO2V5 0 V7
VA6SRC2V5 A6SRC2V5 GND V6
VA5SRC2V5 A5SRC2V5 GND V5
VA4SRC2V5 A4SRC2V5 GND V4
VA3SRC2V5 A3SRC2V5 GND V3
VA2SRC2V5 A2SRC2V5 GND V2
VA1SRC2V5 A1SRC2V5 GND V1
VA0SRC2V5 A0SRC2V5 GND V0
```

DC INPUT THRESHOLD

```
**********CORE SIGNALS****************************
VM TM 0 0
VEN EN 0 vddh
VTEN TEN 0 0
VTA TA 0 0
VTUD TUD 0 0
VA A 0 vddh
VIO IO GNDE vdde

.tran 0 1u

************EXTRACTION AND PLOT*******************

.EXTRACT label = IPDN -(i(VIO))
.EXTRACT label = RPDN abs(V(VDDE2V5)/I(VIO))
```

.plot I(VIO)
.end

INPUT TRANSIENTS

**********CORE SIGNALS*****************************
VM TM 0 0
VEN EN 0 VDDH
VTEN TEN 0 0
VTA TA 0 0
VTUD TUD 0 VDDH
VA A GND 0
CZI ZI 0 1pf
VIO IO 0 pulse 0 VDDE 0 0.1n 0.1n 4.9n 10n
.tran 0 20n

.extract LABEL=DELAYRISE (xup(V(ZI),vddh*0.5,2)-xup(V(IO),vdde*0.5,2))
.extract LABEL=DELAYFALL (xdown(V(ZI),vddh*0.5,2)-xdown(V(IO),vdde*0.5,2))
.extract label=TRISE (xup(V(ZI),vddh*0.9,2)-xup(V(ZI),vddh*0.1,2))
.extract label=TFALL (xdown(V(ZI),vddh*0.1,2)-xup(V(ZI),vddh*0.9,2))
.extract LABEL=DUTY_CYCLE (xdown(v(ZI),vddh/2,2)-
+xup(v(ZI),vddh/2,2))/(xup(v(ZI),vddh/2,2)-xup(v(ZI),vddh/2,3))
.extract label = peak1 (0.95*vddh)-max(v(ZI),0n,20n)
.extract label = valley1 min(v(ZI),15n,20n)-(0.05*vddh)
.extract label = peak2 (0.90*vddh)-max(v(ZI),0n,20n)
.extract label = valley2 min(v(ZI),15n,20n)-(0.10*vddh)
.PLOT V(ZI) V(IO)
.probe v
.probe i
.op
.end

N drive

**********CORE SIGNALS*****************************
VM TM 0 0
VEN EN 0 vddh
VTEN TEN 0 0
VTA TA 0 0
VTUD TUD 0 0
VA A 0 vddh
VIO IO GNDE vdde

.tran 0 1u

************EXTRACTION AND PLOT*******************

.EXTRACT label = IPDN -(i(VIO))
.EXTRACT label = RPDN abs(V(VDDE2V5)/I(VIO))
.plot I(VIO)
.end

P DRIVE

**********CORE SIGNALS*****************************
VM TM 0 0
VEN EN 0 vddh
VTEN TEN 0 0
VTA TA 0 0
VTUD TUD 0 0
VA A 0 vddh
VIO IO GNDE vdde

.tran 0 1u

************EXTRACTION AND PLOT*******************

.EXTRACT label = IPDN -(i(VIO))
.EXTRACT label = RPDN abs(V(VDDE2V5)/I(VIO))
.plot I(VIO)
.end

PULL DOWN

**********CORE SIGNALS*****************************
VM TM 0 0
VEN EN 0 vddh
VTEN TEN 0 0
VTA TA 0 0
VTUD TUD 0 0
VA A 0 vddh
VIO IO GNDE vdde

.tran 0 1u

************EXTRACTION AND PLOT*******************

.EXTRACT label = IPDN -(i(VIO))
.EXTRACT label = RPDN abs(V(VDDE2V5)/I(VIO))
.plot I(VIO)
.end

O/P TRANSIENTS

**********CORE SIGNALS*****************************
VTM TM 0 0
VEN EN 0 0
VTUD TUD 0 0
CIO IO 0 10p
VA A 0 pulse 0 VDDH 0 0.1n 0.1n 4.9n 10n
.tran 0 30n

.extract LABEL=DELAYRISE (xup(V(IO),VDDE*0.5,2)-xup(V(A),VDDH*0.5,2))
.extract LABEL=DELAYFALL (xdown(V(IO),VDDE*0.5,2)-
+xdown(V(A),VDDH*0.5,2))
.extract LABEL=TRISE (xup(V(IO),VDDE*0.9,2)-xup(V(IO),VDDE*0.1,2))
.extract LABEL=TFALL (xdown(V(IO),VDDE*0.1,2)-xdown(V(IO),VDDE*0.9,2))
.extract LABEL=DUTY_CYCLE   (xdown(v(IO),VDDE/2,2)-
+xup(v(IO),VDDE/2,2))/(xup(v(IO),VDDE/2,2)-xup(v(IO),VDDE/2,3))
.extract label = peak1 (0.95*VDDE)-max(v(IO),0n,20n)
.extract label = valley1 min(v(IO),15n,20n)-(0.05*VDDE)
.extract label = peak2 (0.90*VDDE)-max(v(IO),0n,20n)
.extract label = valley2 min(v(IO),15n,20n)-(0.10*VDDE)

.PLOT V(A) V(ZI) V(IO)

.end