Design, Analysis and Performance based Evaluation of DLL (Delay Locked Loop) in DSM Technology

Major Project Report

Submitted in partial fulfillment of the requirements

For the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Khyati Vinaychandra Bhatt

(08MEC001)

Department of Electronics & Communication Engineering

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Ahmedabad-382 481

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Declaration

This is to certify that

i) The thesis comprises my original work towards the Degree of Master of Technology in Electronics & Communication Engineering (VLSI Design) at Nirma University and has not been submitted elsewhere for a degree.

ii) Due acknowledgement has been made in the text to all other material used.

Khyati Vinaychandra Bhatt

Certificate

This is to certify that the Major Project entitled **"Design, Analysis and Performance based Evaluation of DLL(Delay Locked Loop) in DSM Technology"** submitted by **Bhatt Khyati Vinaychandra (08MEC001)**, towards the partial fulfillment of the requirements for the degree of Master of Technology in Electronics & Communication Engineering(VLSI Design) of Nirma University, Ahmedabad is the record of work carried out by her under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree.

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Abstract

Currently, CMOS VLSI is progressing at fast rate for decades and dominating most of markets in digital circuit areas. In a constant voltage scaling, the vertical and later electric fields are increased, which reduced to oxide reliability. Low power supply voltage is required necessarily. For the design of CMOS VLSI systems using low power supply voltage, the implementation of chips is directly limited by processing technology and devices. The objective is to demonstrate the useful techniques in the designing of logic level and system building blocks in low-voltage CMOS VLSI technology.

Generation and distribution of clock signals inside the VLSI systems is one of the most important problems in the design of VLSI systems. Because of the process variations and interconnect parasitic, clock signals delays vary for different paths. The clock signals should have zero clock skew, that is to say all the clock signals should arrive at the inputs of registers at the same time. Otherwise latches and flip-flops' get clock signal at different time instances. In order to circuit to operate correctly these differences should be eliminated, ideally to zero. However it is not possible practically and 10 percentage of the clock cycle is expended in order to compensate for clock skew.

Delay Locked Loops (DLL) are widely employed in microprocessors, memory, and communication ICs in order to reduce on chip clock buffering delays and improve I/O timing margins. A DLL is a digital circuit similar to a phase-locked loop, with the main difference being the absence of an internal oscillator. A DLL can be used to change the phase of a clock signal.

Abberviation

BSIM	Barkley Short Channel Insulated Gate MOSFET
CMOS	Complementary Semiconductor Metal Oxide
CP	Charge Pump
CDR	Clock and Data Recovery Circuit
DSM	Deep Sub Micron
DLL	Delay Locked Loop
FSM	Finite State Machine
IC	Integrated Circuit
ICMR	Input Common Mode Range
LPF	Low Pass Filter
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Filed Effect Transistor
PD	Power Dissipation
PVT	Process,Voltage,Temperature
PLL	Phase Locked Loop
PFD	Phase Frequency Detector
SOC	System On Chip
SPICE	Simulation Program for Integrated Circuit Emphasis
SNDR	Signal to Noise Density Ratio
TSMC	Taiwan Semiconductor Manufacturing Company
VLSI	Very Large Scale Integration
VCDL	Voltage Controlled Delay Line
VCO	Voltage Controlled OScillator

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Chapter 1

Introduction

Generation and distribution of clock signals inside the VLSI systems is one of the most important problems in the design of VLSI systems. Because of the process variations and interconnect parasitic, clock signals delays vary for different paths. The clock signals should have zero clock skew, that is to say all the clock signals should arrive at the inputs of registers at the same time. Otherwise latches and flip-flops' get clock signal at different time instances. In order to circuit to operate correctly these differences should be eliminated, ideally to zero. However it is not possible practically and 10 percentage of the clock cycle is expended in order to compensate for clock skew. To handle this problem, several solutions are proposed. One of which is usage of H-tree clock networks, in which configuration the distance to all circuit blocks is same thus the clock delay would be same. But this technique is hard to implement since the different fan-out requirements for different blocks and routing constraints. Currently, CMOS VLSI is progressing at fast rate for decades and dominating most of markets in digital circuit areas. In a constant voltage scaling, the vertical and later electric fields are increased, which reduced to oxide reliability. Low power supply voltage is required necessarily. For the design of CMOS VLSI systems using low power supply voltage, the implementation of chips is directly limited by processing technology and devices. The objective is to demonstrate the useful techniques in the designing of logic level and system building blocks in low-voltage CMOS VLSI technology.

The sub-micrometer CMOS process is the technology for current and future semiconductor systems and applications due to its low-cost. Technology constraints and battery-powered operation require that low-voltage analog circuits be designed. Whereas low-voltage operation is associated with many advantages for digital circuits, it generally complicates the design of analog circuits. When the supply voltage is lowered ,not only does it become increasingly difficult to maintain the same (high) level of SNDR performance, but also even the functionality of the circuit may be hard to preserve.

The continued scaling of CMOS technology together with progress in the design of high-frequency analog and mixed-signal CMOS circuits has enabled the designers to implement many functions onto a single chip. One of the greatest challenges in the design of such systems is a need to put broadband analog circuits on the same die that the large complex digital signal processing components are placed. Due to the high-level of interactions between the noisy digital blocks with the noise sensitive analog parts through various propagation mechanisms it is highly possible that the large-signal switching transients of the digital circuits corrupt the performance of the analog sub-blocks. Crosstalk from digital circuits on analog components is mostly via substrates and thus named the substrate noise. Such noise degrades analog signal integrity in mixed-signal integrated circuit design. Substrates comprised of a lightly doped epitaxial layer grown on a heavily doped substrate will exhibit a good performance in minimizing the latch-up phenomenon, and as a result these types of substrates are widely used in system-on-chip (SOC).

However, there is an increasing trend to use silicon-on-insulator technology to due its superior power dissipation performance. In general, the substrate noise propagation through the silicon bulk is a complicated phenomenon and strongly depends on the Substrate doping profiles. However, since the resistivity of the heavily doped p+ substrate in a low epitaxial layer is quite low, such substrates are generally modeled as a single node. Thus, the substrate propagation is approximately uniform throughout the heavily doped substrate. The building blocks that are exposed to the substrate

noise are clearly the ones that provide the communication interface between the digital part and the analog part, namely analog-to-digital (A/D) and digital-to-analog (D/A) converters, as well as the clock generator of the digital synchronous circuit.

Delay-locked loops (DLLs) are widely utilized as on-chip clock frequency generators to synthesize a low skew and higher internal frequency clock from an external lower frequency signal and also as clock and data recovery circuits (CDR) in broadband communications systems, The random temporal variation of the phase, or jitter, is a critical performance parameter in the design of DLL circuits. A Delay-Locked Loop circuitry exhibits a better noise performance than a phase-locked loop (PLL), and therefore it is widely used as a clock generator in a mixed-signal integrated circuit where the noisy digital circuits will severely affect the analog portion through the noise being injected through the silicon substrate.

The reduction of clock skew is one of the important problems in the VLSI design. Passive Techniques such as clock network optimization techniques cannot completely reduce the clock skew. Phase-locked loops and Delay Locked Loops (DLL) are extensively used in VLSI circuits in order to decrease clock screw in the clock networks. DLL is a first order loop that compares it's input with a reference signal, than delay it' s output so that it can synchronize with the reference signal in a feedback fashion.

Delay-locked loop (DLL) is a critical circuit component widely used in many timing applications.

1.1 Literature Survey

DLLs are widely employed in microprocessors, memory, and communication ICs in order to reduce on chip clock buffering delays and improve I/O timing margins. The essential function of a DLL is to achieve phase alignment between the input clock and the output clock from the final stage of the VCDL. After the phase alignment is achieved, each VCDL delay stage is able to provide a stable clock signal which is phase shifted from the input clock. However, the rising clock speeds and integration levels of

digital circuits have made the phase alignment task increasingly difficult. The rising demand for high-speed I/O has created an increasingly noisy environment in which DLL's must function. This noise, typically in the form of supply and substrate noise, tends to cause the output clocks of DLL's to jitter from their ideal timing. With a shrinking tolerance for jitter in the decreasing period of the output clock, the design of low jitter DLL's has become very challenging .Thus, a detailed study of prior work in DLL design and analysis is needed for us to achieve the design goals of wide lock range, low jitter, and fast locking.

1.2 Introduction Of DLL

Delay locked loops (DLL's) and phase-locked loops (PLL's) are often used in the I/O interfaces of digital integrated circuits in order to hide clock distribution delays and to improve overall system timing. In these applications, DLL's and PLL's must closely track the input clock. However, the rising demand for high-speed I/O has created an increasingly noisy environment in which DLL's and PLL's must function. This noise, typically in the form of supply and substrate noise, tends to cause the output clocks of DLL's and PLL's to jitter from their ideal timing. With a shrinking tolerance for jitter in the decreasing period of the output clock, the design of low jitter DLL's and PLL's has become very challenging. Achieving low jitter in PLL and DLL designs can be difficult due to a number of design tradeoffs. Consider a typical PLL which is based on a voltage controlled oscillator (VCO). The amount of input tracking jitter produced as a result of supply and substrate noise is directly related to how quickly the PLL can correct the output frequency. To reduce the jitter, the loop bandwidth should be set as high as possible.

Unfortunately, the loop bandwidth is affected by many process technology factors and is constrained to be well below the lowest operating frequency for stability. These constraints can cause the PLL to have a narrow operating frequency range and poor jitter performance. Although a typical DLL is based on a delay line and thus simpler from a control perspective, it can have a limited delay range which leads to a set of problems similar to that of the PLL.

Growing demand for high-speed IFO on digital ICs creates an increasingly noisy environment in which phase-locked loops (PLLs), delay-locked loops (DLLs), and other clock generating blocks must function. This noise, typically in the form of supply noise and substrate noise, makes design of low-jitter PLLs and DLLs challenging. Self biasing leads to a number of desirable properties that include IC process independence, fixed damping factor, fixed bandwidth-to-operating-frequency ratio, broad frequency range, input phase offset cancellation, and, most importantly, low input tracking jitter.

As silicon fabrication technology develops, the chip size gets bigger and bigger, and number of logic gates and chip operating frequency increase, clock skew becomes more and more important in ensuring proper functioning of VLSI chips. With a synchronous communication protocol, it is impossible to further increase the communication clock speed without reducing the clock skew on chip. The clock skew is caused by different RC delay of clock interconnects along different clock signal paths and different delays of clock buffers due to process variations, temperature differences on the same chip, and power supply differences due to power rail IR drop. To reduce clock skew, the clock distribution network should be carefully designed. In addition, circuit techniques such as Phase Locked Loop (PLL) and Delay Locked Loop (DLL) may become necessary to reduce the total clock skew by employing them in several critical places of the clock distribution structure. DLL has advantage over PLL for low-voltage applications where it is difficult to obtain acceptable noise-induced jitter performance as supply voltage drops. In addition, acquisition time is often larger in PLL than in DLL due to the time PLL takes to drive the VCO to the correct

frequency.

Delay and Phase Locked Loops are integral components of contemporary digital and mixed signals ICs. Integrating these semi-analog blocks in the environment of a large IC requires dealing effectively with the unavoidable supply and substrate noise. To address this issue, designers usually employ differential delay elements combined with some form of high bandwidth biasing scheme. However, decreasing supply-to-threshold voltage ratios, have also led to the adoption of buffers based on variants of static CMOS gates with regulated supply which acts also as the control voltage.The advantages of CMOS based delay buffers are their simple and portable design and their relaxed supply headroom requirements.

Their main disadvantage, however, is their high control-voltage to delay gain; typically 1 percent of delay per 1 percent of regulated supply control-voltage. This high gain does not directly affect the buffer noise sensitivity in a well regulated environment. However, in order to compensate for high gain, designers are forced to reduce the loop bandwidth - typically regulated supply PLLs and DLLs achieve loop bandwidths that are 1-2 orders of magnitude lower than their theoretical maximum (1/10th of the reference clock frequency). This low bandwidth results in loops with long acquisition times, high phase error accumulation, and limited operating range. The proposed Delay and Phase Locked Loops exhibit wide bandwidth, low noise sensitivity, short acquisition times, and large operating range.

As the speed performance of VLSI systems increases rapidly, more emphasis is placed on suppressing skew and jitter in the clocks. Phase-locked loops (PLL's) and delay-locked loops (DLL's) have been typically employed in microprocessors, memory interfaces, and communication IC's for the generation of on-chip clocks. However, it becomes increasingly difficult to reduce the clock skew and jitter, whether they are inherent or result from substrate and supply noise, as the clock speed and circuit integration levels are increased. While the phase error of PLL's is accumulated and persists for a long time in a noisy environment, that of DLL's is not accumulated ,and thus, the clock generated from DLL's has lower jitter. Therefore, DLL's offer a good

alternative to PLL's in cases where the reference clock comes from a low-jitter source, although their usage is excluded in applications where frequency tracking is required, such as frequency synthesis and clock recovery from an input signal. However, the main problem of conventional DLL's is that they are very difficult to design to work over process, voltage, and temperature (PVT) variations .Since DLL's adjust only phase, not frequency, the operating frequency range is severely limited. We propose a new DLL architecture that operates in a wide frequency range while keeping the low-jitter performance. Various wide-range DLL architectures, with similar motivations, have been developed, which can be classified in to three categories: analog type, digital type and dual-loop type while a conventional analog DLL uses a voltage-controlled delay line (VCDL), the wide-range analog DLL uses phase mixers for wide-range operation. However, because of its relatively high analog complexity, the analog DLL requires a process-specific implementation, making it relatively difficult to port across multiple processes Thus, digital DLL's have been proposed for better process portability. However, skew error and jitter are increased due to continuous change of phase selections among quantized delay times with supply and temperature variations. To overcome these problems, dual-loop architectures have been proposed. In a PLL is added to make the core DLL lock to a reference frequency, and a phase mixer interpolates two intermediate clocks in the core DLL and produces the final output clock. or almost continuous phase is obtained with addition of a fine delay line or a phase interpolator to a digital DLL. However, additional chip area and power consumption of these wide-range DLL's are excessive, and furthermore, their jitter performance gets worse compared with conventional DLL's since the number of delay cells or gates in the clock propagation paths becomes larger. We propose a new DLL architecture that achieves a large operating range by attaching a replica delay line in parallel with a conventional analog DLL. Since, the replica delay line. Occupies one-fourth the area of the core DLL, it incurs only a small increase in chip area and power consumption. Since the replica delay line is out of the clock propagation path, it does not do any harm on low-jitter performance. While other wide-range DLL's use

phase mixers or phase selections to generate a single output, the proposed DLL uses a similar multistage analog VCDL to what conventional analog DLL's use. Therefore, the proposed DLL can generate multiphase clocks without using excessive amount of hardware. Furthermore, by incorporating a dynamic phase detection circuit and cell-level duty cycle correction method, the multiphase clocks are equally spaced even in high-frequency operations. A prototype DLL designed for eight-phase clocks can be used in applications such as gigabit serial interfaces.

Chapter 2

Clock Distribution Network

In present day VLSI ICs, intra-die processing variations are becoming harder to control, resulting in a large skew in the clock signals at the end of the clock distribution network. We describe a buffered H-tree technique to distribute the clock signal and to de-skew a clock network. The clock shielding wires (which are connected to GND in normal operation) are, in de-skewing mode, used to selectively return the clock signal for de-skewing, and for serial communication with the clock distribution sites for skew adjustment. Our forward and return clock networks are buffered, with identically sized and co-located wires and buffers. This results in both these networks exhibiting identical delay characteristics in the presence of intra-die process variations. Unlike existing approaches, our method utilizes a single phase detection circuit, and can achieve a very low maximum chip-level clock skew. This skew value is not dependent on the resolution of the phase detector. Further, our technique can be applied dynamically, either at boot time or periodically during the operation of the IC, as necessary. Additionally, our buffered H-tree enables us to implement efficient clock gating by allowing the user to turn off clocks in the distribution network itself, thus disabling entire sections of the clock network. We demonstrate the utility of our technique on a 6-level H-tree clock distribution network. In a clock distribution network which is initially skewed by up to 300ps, our technique can de-skew signals to within 4ps of each other. We show that the total wiring area of our clock distribution

and de-skewing methodology is about 35 percentage higher than a traditional H-tree (which does not have a deskewing functionality), while the active logic area overhead is about 25 percentage. The power consumption of our network is 5 percentage lower than that of a traditional H-tree network with no de-skewing functionality

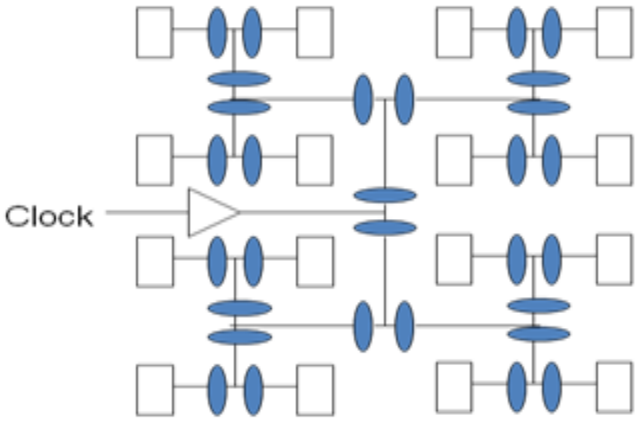

Figure 2.1: H Tree Topology

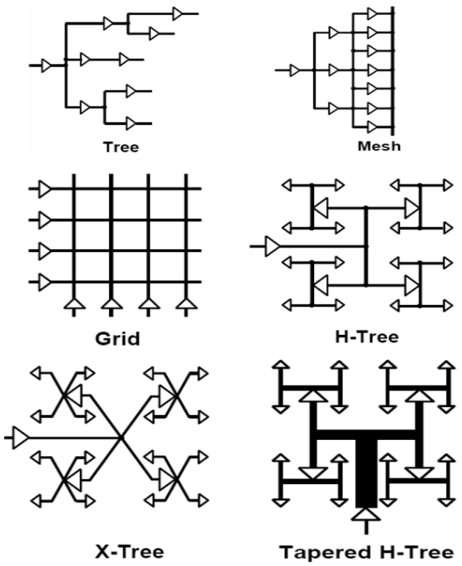

Figure 2.2: Clock Distribution Network

2.1 Other Clock Distribution Networks

Clock signals are typically loaded with the greatest fanout and operate at the highest speeds of any signal, either control or data, within the entire synchronous system. Since the data signals are provided with a temporal reference by the clock signals, the clock waveform must be particularly clean and sharp. Furthermore, these clock signals are particularly affected by technology scaling (Moore's law), in that long global interconnect lines become significantly more resistive as line dimensions are decreased. This increased line resistance is one of the primary reasons for the increasing significance of clock distribution on synchronous performance. Finally, the control of any differences and uncertainty in the arrival times of the clock signals can severely limit the maximum performance of the entire system and create catastrophic race condition which an incorrect data signal may latch within a register.

2.2 Clock Skew

Differences in clock signal arrival times across the chip are called clock skew. It is a fundamental design principle that inputs to registers timing must be guaranteed to satisfy register setup and hold time requirements. Both data propagation delay and clock skew are important in guaranteeing these parameters. Clocking sequentially-adjacent registers on the same edge of a high-skew clock can cause timing violations or functional failure in designs. Figure 2.3 shows an example of sequentially-adjacent registers, where a regular routing resource has been used to route the clock signal; it is highly likely that clock skew will be noticeable.

Skew is the variation of propagation delay differences between output signals. Minimizing output skew is a key design criterion in today's high-speed clocked systems. Excessive skew, especially for clock signals, can cause race conditions and other

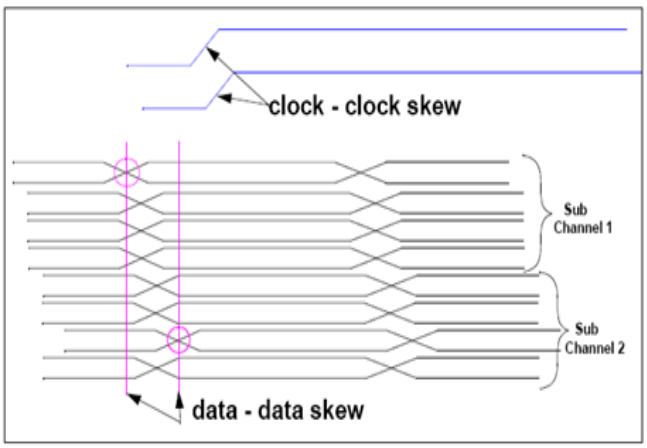

Figure 2.3: Clock Skew

timing errors that result in system data faults. At the very least, poor skew will force a slower maximum system speed, and this, in turn, will limit system performance.

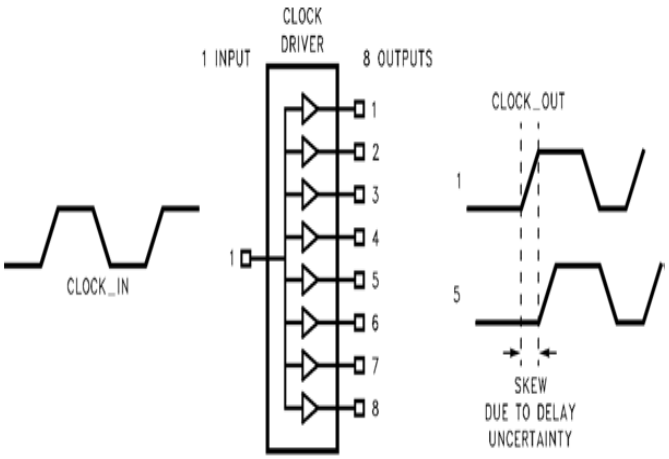

Figure 2.4: Clock Driver showing output skew

2.2.1 Sources of Clock Skew

With a perfectly balanced distribution, device mismatch is the largest contributor to the clock skew.

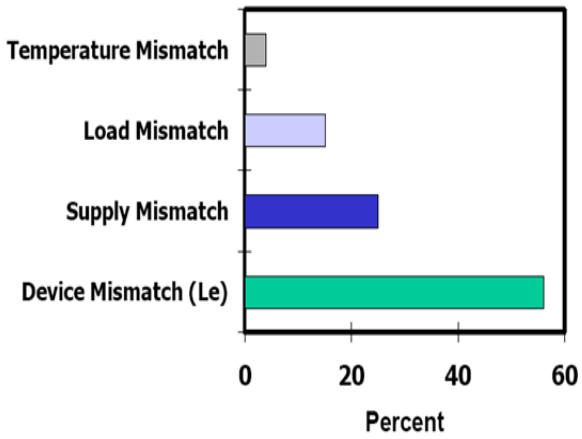

Figure 2.5: Sources of Clock Skew

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of devices. Extrinsic skew is defined as the differences in trace delays and loading conditions. If the trace delays are poorly matched the result will be an increase in signal-to-signal skew.

2.2.2 Positive Clock Skew

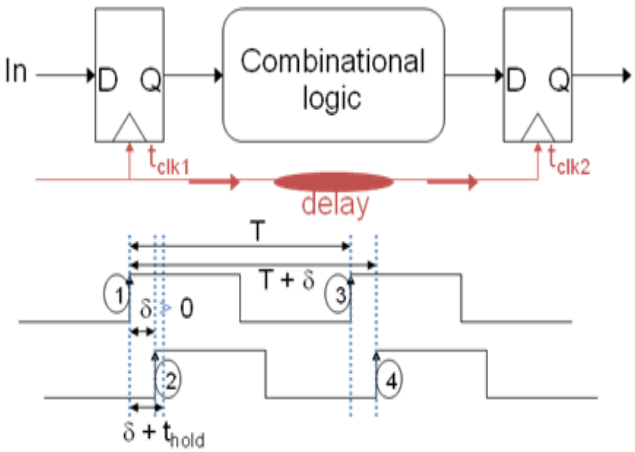

Figure 2.6: Positive Clock Skew

2.2.3 Negative Clock Skew

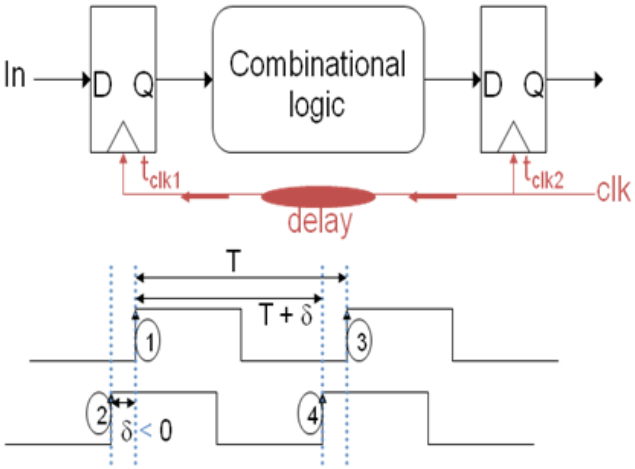

Figure 2.7: Negative Clock Skew

2.3 Jitter

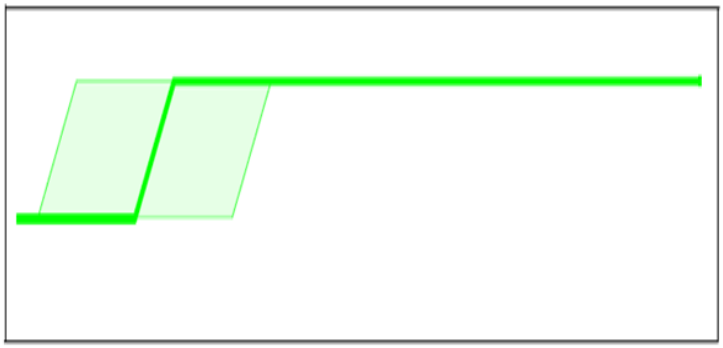

Figure 2.8: Timing Displacement from nominal timing characteristic

Magnitude and offset of timing displacement could depend on: previous signal state(s), current signal state(s), supply voltage level(s), crosstalk, and variations in

thermal characteristics. Jitter is movement of signal edges from their ideal position in time. This movement can lead or lag the ideal positions, and, as system speeds increase, these edge deviations present a significant problem for system signal integrity, causing skew, race conditions, and other timing problems. Jitter is generally classified into three types: cycle-to-cycle jitter, period jitter, and phase jitter. Cycle-to-cycle jitter is the change in an output's transition in time in relation to the transition during the previous cycle. Period jitter is the maximum change in a signal transition from the ideal position in time. Phase jitter, also called long-term jitter, in the maximum change in an output signal transition from its ideal position over many cycles (typically 10 to 20 microseconds).

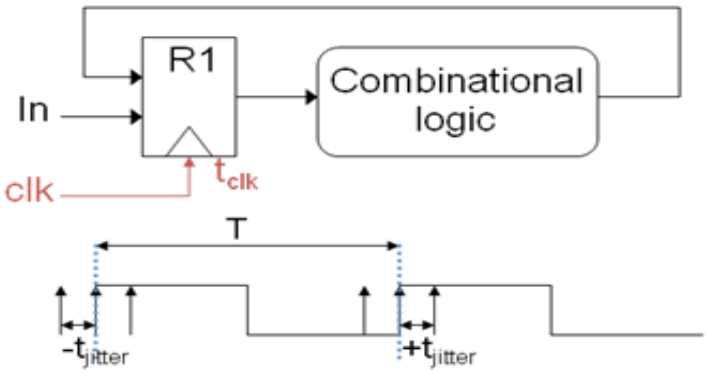

Figure 2.9: Clock Jitter

The causes of jitter are grouped into two general categories: deterministic jitter and random jitter. Deterministic jitter is caused by power supply fluctuations, cross-talk, and duty cycle distortion (e.g., asymmetric rising and falling edges). Random jitter is caused primarily by device thermal noise. Although system designers have little control over the causes of random jitter, they can reduce the effects of deterministic jitter by minimizing cross-talk and duty cycle distortion and by ensuring the power network is adequate for system needs.

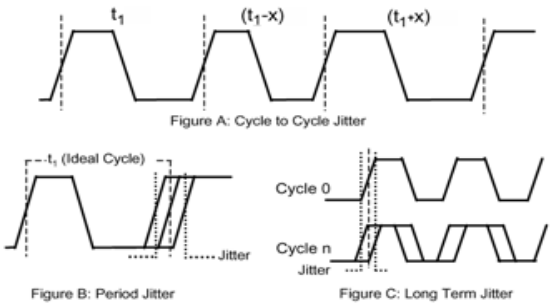

Figure 2.10: Types Of Jitter

2.4 Substrate Noise

Substrate noise is the major source of performance limitation in mixed-signal integrated circuits. This paper studies substrate noise effects on the performance of delay-locked loops (DLLs). Due to their robust noise performance, the delay-locked-loops are widely used as click generators of microprocessors. Although exploiting advanced circuit techniques reduces the timing jitter induced by the substrate noise to a large extent, the hostile noisy digital section in mixed-signal VLSI circuit can still cause a large substrate noise and hence a non-negligible timing jitter in DLL clock generators.

Chapter 3

DLL Architecture

Correct timing is necessary for proper operation of high performance digital and mixed-signal circuits. As the size and operating frequency of VLSI systems increase, designing of clock distribution system poses numerous challenges. In general, the quality of clock pulses is determined by several factors such as frequency, phase, duty-cycle, jitter, and clock skew. A good design solution is one that minimizes all previously mentioned negative effects issues .Delay Locked Loops (DLLs) and Phase Locked Loops (PLLs) are used in synchronous digital systems in order to improve timings, i.e. to minimize negative effects of skew and jitter in the clock distribution network. we propose an efficient DLL architecture implemented with linear delay element.

Traditionally, PLLs are used for high-frequency clock synthesis. When frequency multiplication is not required, a DLLs offer better performance in respect to PLLs, since its design is easier, and immunity to on-chip noise and stability is better. DLL with installed first-order loop filter is more stable then higher-order PLL. In addition, jitter accumulation makes PLLs more susceptible to power-supply and substrate noise in respect to DLLs.

3.1 Different DLL Architectures

According to the principle of phase shift generation DLL architectures can be classified into three classes: analog digital and hybrid, usually referred as dual loop.

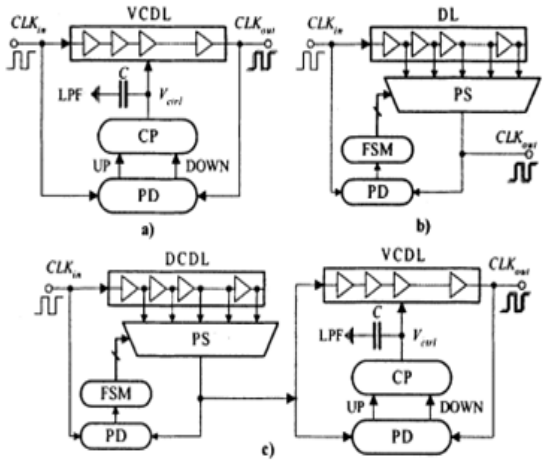

Figure 3.1: Three DLL Architectures

Constituents of the analog DLL, pictured in Fig. 3.1(a), are: Voltage Controlled Delay Line (VCDL), Phase Detector (PD), Charge Pump (CP), and first order Low-Pass Filter (LPF). The VCDL is composed of several variable delay elements connected in cascade. The reference clock CLK-in, drives the input of VCDL. In order to determine the phase alignment error, the PD compares the rising edges of CLK-in and CLK-out. Composition of CP and LPF act as an integrator, and generates a control voltage, Vctrl. Under normal condition, the DLL forces to align a phase difference between CLK-out and CLK-in. When correctly locked, the total delay of VCDL should be equal to one period of the reference clock, CLK, Analog DLLs are suitable for fine-grain delay variation. They are efficient in applications where small, accurate, and precise amount of delay is necessary to achieve.

The digital DLL shown in Fig.3.1(b) consists of: Digitally Controlled Delay Line (DCDL), Phase Selector (PS), Phase Detector (PD) and Finite State Machine (FSM).

DCDL is implemented as a delay elements chain of variable length. The number of elements in a chain determines the amount of the delay. The PS is realized as a multiplexer. At its output pulse of defined phase-shift (delay) is selected . FSM's output defines the amount of a delay. Delay elements, in DCDL, provide fixed and quantized time delays, and they are used for coarse-grain delay variation in a wide range of regulation. This means that the digital DLL quantizes the clock signal into several coarse-grain discrete delay steps.

The dual-loop DLL, sketched in Fig 3.1(c), is composed as a series of digital and analog DLL In general, the dual-loop DLL provides a wide operating phase-shift range. Jitter performance is not good enough, because clock propagation patha includes two lops with large number of delay elements. Hardware complexity and power consumption of Dual loop DLL are high.

3.2 DLL Architecture

DLLs are widely employed in microprocessors, memory, and communication ICs in order to reduce on chip clock buffering delays and improve I/O timing margins. They can also be used to generate multiple clock signals on chip. The essential function of a DLL is to achieve phase alignment between the input clock and the output clock from the final stage of the VCDL. After the phase alignment is achieved, each VCDL delay stage is able to provide a stable clock signal which is phase shifted from the input clock. However, the rising clock speeds and integration levels of digital circuits have made the phase alignment task increasingly difficult. For example, power supply and substrate noise resulting from the switching of digital circuits affects the operation of DLL and leads to output clock jitter. Thus, a detailed study of prior work in DLL design and analysis is needed for us to achieve the design goals of wide lock range, low jitter, and fast locking.

A conventional DLL is typically composed of three components: a PD, a CP, and a VCDL. Conventional DLLs can be categorized as either analog or digital. Generally

speaking, a digital DLL has the advantage of being more robust, enabling better process portability, requiring lower supply voltage, and being simpler design. On the other hand, an analog DLL has the advantages of higher power and substrate noise rejection, smaller area and power consumption, and finer phase resolution.

3.3 DLL Operation Principle

A DLL is essentially a nonlinear negative feedback system. However, it is a common practice to characterize a DLL by linear analysis. Although linear analysis is not able to produce a very accurate result, it can still serve as a reasonable first-order approximation and can lead to some useful insights into a DLL's operation. In a DLL, the input clock signal propagates through the VCDL and develops phase shift (or time delay) at every delay stage of the VCDL. The phase shift of each delay stage is controlled by the voltage of a loop filter. The output is taken from one of the delay stages. The phase of the output signal is compared with the phase of the input clock in the PD. The phase error information generated by the PD (usually in the form of a voltage or a current) is then transferred to the CP. The CP uses the phase error information to adjust the voltage of the loop filter and thus to change the delay of the VCDL. Owing to such a negative feedback mechanism, the phase error is gradually reduced until it finally becomes zero. At that time, the delay of the whole VCDL line becomes equal to one clock period, and the voltage of the loop filter is stabilized, which indicates that a locked state has been established.

3.4 Analog DLL

Since analog DLLs architectures and their components vary significantly from one to the other, the following sections will first discuss the implementations of the three basic building blocks: the PD, the CP, and the VCDL.

DLL consists of 4 units:-

1 phase Detector

2 Charge Pump

3 Filter

4 Voltage Controlled Delay Line (VCDL)

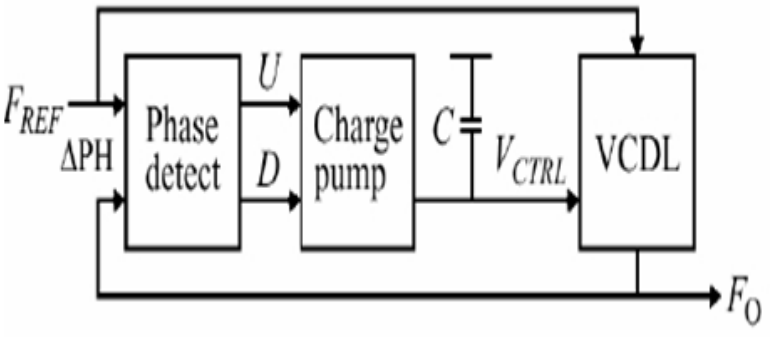

Figure 3.2: Block diagram of DLL

It's working principle is as follows: First, phase detect block compares the reference clock signal with the output signal, depending on the difference , if reference signal is leading the output Up (U) signal, else if the reference signal lagging the output signal Down (D) signal is asserted, and thus controls the delay line appropriately. VCDL adjusts the phase of the output signal proportional to the difference between reference signal until the output signal is high

3.4.1 Phase Detector

The PD is one of the most critical components within a DLL. One of the structural differences between an analog and a digital DLL is that the inputs to the PD are

different. Both an analog DLL's PD and a digital DLL's PD take the input reference clock as one input. For the other input to the PD, a digital DLL usually uses the output of a digital tap whose phase is the closest to the input reference signal, and this tap is not necessarily the last tap of the VCDL. While for an analog DLL, since the delay of the entire VCDL must be one clock cycle in the locked state, the other input to the PD is directly taken from the end of the VCDL.

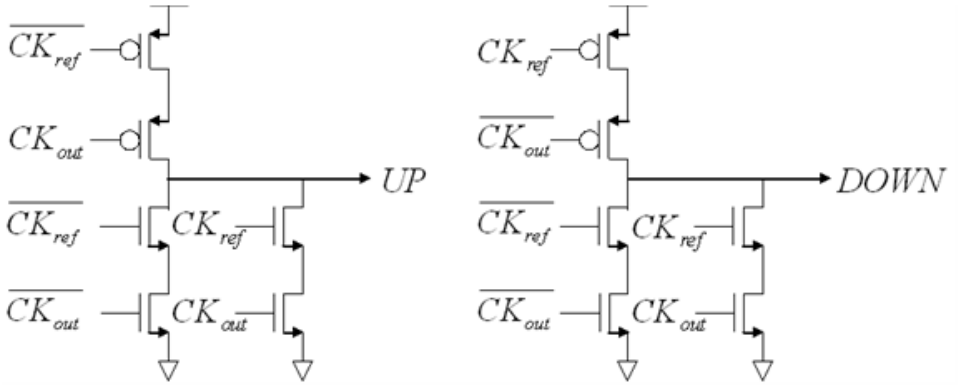

Figure 3.3: PD based on XOR gate

In an XOR PD, the dc value of the PD output signal is linearly proportional to the phase difference of the two input signals. In addition, the average output signal becomes zero when the two inputs are 90 degree out of phase. As a result, an XOR PD is often used in quadrature locking where the two input signals to the PD are 90 degree out of phase in the locked state. The simple XOR PD suffers from several drawbacks. Firstly, there is only one output from the XOR PD, which makes it difficult to interface with the subsequent CP circuit.

Secondly, an XOR gate is essentially a signal level detector, i.e., the output of an XOR gate is dependent upon the duty cycle of the two input signals. Consequently,

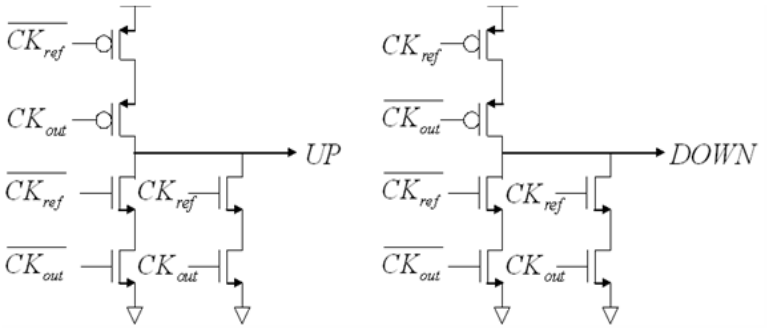

Figure 3.4: Modified PD that provides two output

XOR PD may generate incorrect phase error information unless duty cycle correction circuits are used .

An improved PD is based on flip-flops. Since flip-flops offer edge detection, the duty cycle dependence problem with the XOR gate PD can be avoided. Figure 3.5 shows a commonly used flip-flop based linear PD, which consists of two flip-flops and one NAND gate.

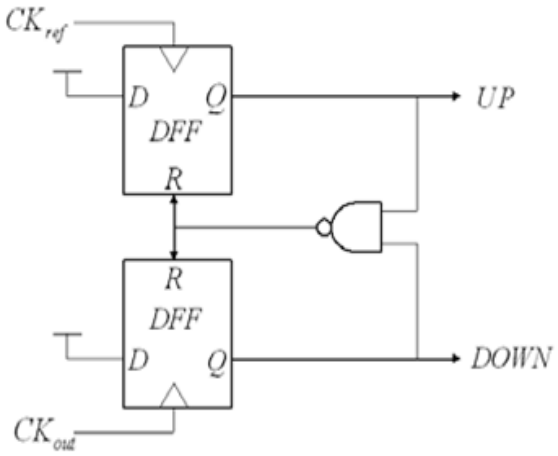

Figure 3.5: PD based on flipflops

The flip-flop based PD is capable of detecting both the phase and the frequency difference, which helps to increase the acquisition range and the locking speed. The disadvantage about the flip-flop based PD is that the reset time may limit the speed

of the PD, which may further limit the operating frequency and the acquisition speed of the DLL.

A third type of PD, which is widely used recently in high-speed DLL designs, is a dynamic PD. The basic structure of a dynamic PD includes two blocks, which are used to generate the UP signal and the DOWN signal, respectively. The two blocks have exactly the same design, except that the two input signals are switched in position. Each block consists of two cascaded stages with a pre-charge PMOS in each stage. The pre-charge activity of the second stage is often controlled by the output of the first stage, as shown in Figure. The dynamic PD eliminates flip-flops and has the advantages of simple structure and a fast transition time. However, dynamic PD needs to be carefully designed in order to minimize the dead zone.

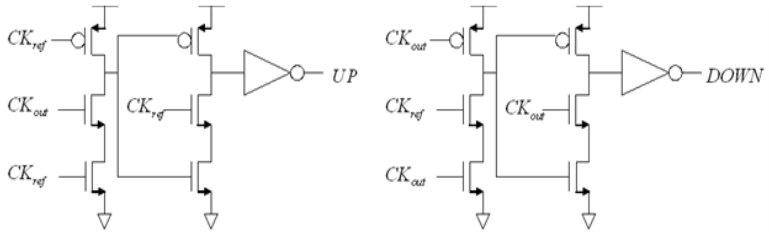

Figure 3.6: A dynamic PD

In order to skew the clock, first of all the skew must be known. This skew can be detected by the phase detectors. Its function is to detect the phase difference between reference clock signal with the input clock signal. It takes these clock signals as input and produces an output that is proportional to the phase difference. Phase detectors can be analog or digital. The first phase detectors used in locked-loops was the linear multiplier phase detector, but as the PLLs became to implemented by digital components, digital phase detectors become popular. Simplest digital detector is an XOR gate, of which output is zero if the two inputs have same phase and one as long as they are not equal. Phase detectors can be implemented digitally by J-K flip flops.

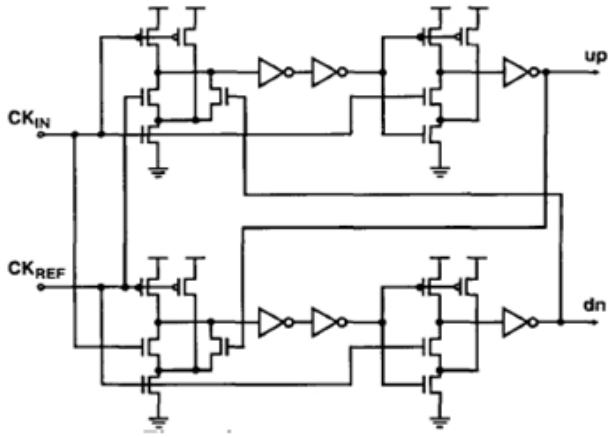

Figure 3.7: Phase Detector

3.4.2 Charge Pump

The charge-pump circuit is an important component in a phase-locked loop (DLL). The charge-pump converts Up and Down signals from the phase/frequency detector (PFD) into current. A conventional CMOS charge-pump circuit consists of two switched current sources that pump charge into or out of the loop filter according to two logical inputs. The mismatch between the charging current and the discharging current causes phase offset and reference spurs in a DLL.

In a DLL, the phase error between the input reference clock and the VCDL output clock is sensed by the PD and transferred to the CP in the form of voltage pulses or current pulses. The CP performs the function of adjusting the voltage of the loop filter and thereby altering the VCDL delay according to the phase error information from the PD. In principle, the CP simply consists of two controlled switches, one current source, and one current sink.

The two switches are controlled by the UP pulses and the DOWN pulses, respectively. Once the switch is closed, the current source or sink will start adding charge

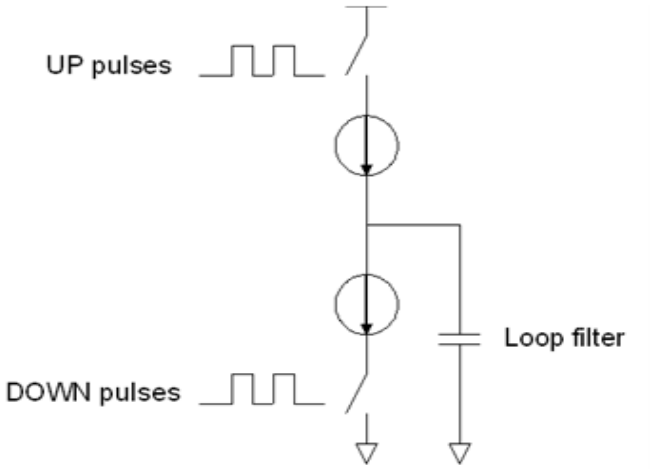

Figure 3.8: Simple Charge pump

onto or removing charge from the loop filter (capacitor). This charging or discharging process will continue until lock is achieved. In the locked state, the voltage (charge) of the loop filter is kept constant. It is possible that equal charging and discharging will still happen in the locked state. In fact, it is desired to have such activities to minimize jitter. However, the charging and discharging currents must be identical as well as very narrow so that the voltage of the loop filter will not be disturbed.

There are three basic configurations for a single-ended CP: switching in the source, switching in the drain, and switching in the gate . These three topologies are illustrated in below Figure 3.9.

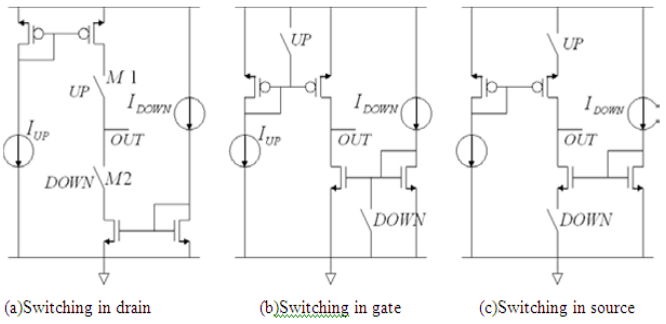

Figure 3.9: Three Single-ended CP configurations

Among the three configurations, switching in source is preferred due to its simpler structure, lower power dissipation and faster switching time Furthermore, studies show that in CMOS circuits, current switching provides a faster switching speed than voltage switching, if all the other conditions are the same . In addition, several new techniques are proposed to further improve the three basic CP structures. The configuration in figure suffers from the charge sharing between the common drain of M1 and M2 and the loop filter when the switch is on (closed). A structure with an active unity-gain amplifier was proposed in to solve this problem. Another enhancement to the basic CP is the adding of two additional current steering switches which greatly improve the switching speed. The third proposed technique is to use only NMOS switches to avoid the mismatch between NMOS and PMOS.

A high-performance CP that combines several of the above techniques was proposed in this structure, the mismatch problems are avoided by redesigning the NMOS and PMOS switches. Cascode current mirrors are used at the output to increase the output resistance so that the charging or discharging current are not be significantly disturbed.

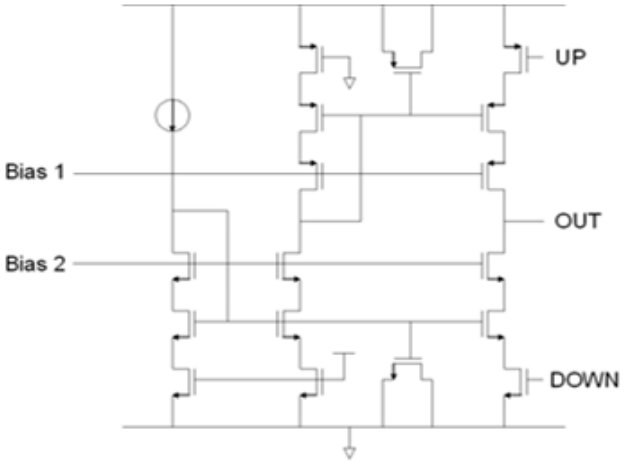

Figure 3.10: A high performance single ended CP

Fully differential CP consists of a set of NMOS switches, a set of PMOS switches, two loop filters, and some common-mode feedback circuitry. Although differential CPs are not as widely used as single-ended CPs, they do possess several unique advantages. Firstly, the fully differential structure offers better noise immunity to common-mode noise sources such as supply and substrate noise. Secondly, mismatch between the PMOS and NMOS switches in single-ended CPs does not exist in fully differential CPs. Lastly, the output voltage range can be doubled if the voltages of both loop filters are used. These advantages are achieved at the expense of double chip area and higher power dissipation.

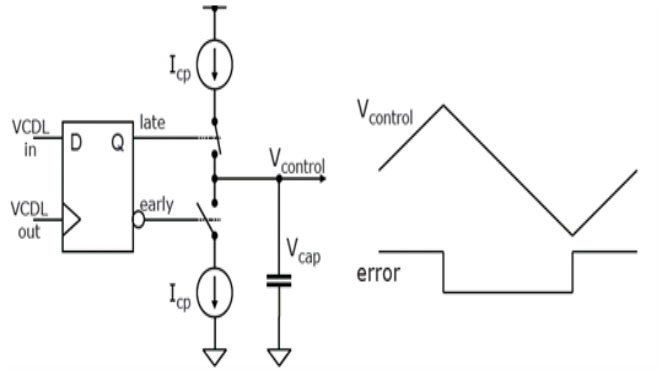

Figure 3.11: Active loop Filter– charge pump and capacitor

A charge pump and capacitor is used a loop filter to convert the output of the phase detector into the control voltage to control VCDL delay. A PD charge pump assembly is shown in figure.

This phase comparator injects, subtracts or leaves alone the charge stored across a capacitor, depending on the output of the phase detector circuit. When the late signal is asserted, the current flows into the capacitor, increasing the control voltage to the VCDL and when the early signal is asserted, the capacitor discharges decreasing the control signal to the VCDL.

3.4.3 Voltage Controlled Delay Line

Besides the PD and the CP, the VCDL is also considered to be one of the most critical blocks within a DLL because the output signal of the DLL is directly taken from the VCDL. The VCDL.s performance considerably affects the jitter of the output signal and the stability of the DLL.

A VCDL typically consists of a number of delay stages (cells) which are connected in series. A VCDL is an open loop configuration by itself, so it does not oscillate and thereby is different from the voltage-controlled oscillator (VCO) in a PLL.

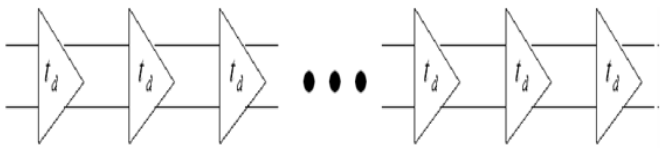

Figure 3.12: A typical VCDL configuration

For analog DLLs, the total delay of the VCDL must be equal to one clock period REF T (or a phase shift of 360) in the locked state. Theoretically, all the delay stages in the VCDL are identical. Therefore, each delay stage contributes a time delay of T n REF (or a phase shift of 360o n) for an n stage VCDL. Using more stages increases the phase resolution, but also increases the minimum VCDL delay. The design parameters of individual delay cells include output signal swing and delay range.

As usual, the delay cells in analog DLLs can be divided into single-ended types and differential types. Unlike digital DLLs that typically use basic inverters as the delay cells, analog DLLs employ many different configurations for their delay cells. Typical single-ended configurations include a current starved inverter and an RC delay stage.

The VCDL takes the reference clock as an input and delays it by some amount. The amount of delay introduced is a function of the control voltage. A starved inverter, whose delay is controlled by the NMOS and PMOS charging currents during high to low and low to high transitions at the output, is used as the delay cell. When the current source is controlled by a control voltage, the delay introduced becomes a function of the control voltage. Such a voltage controlled single-ended delay cell is shown in figure below.

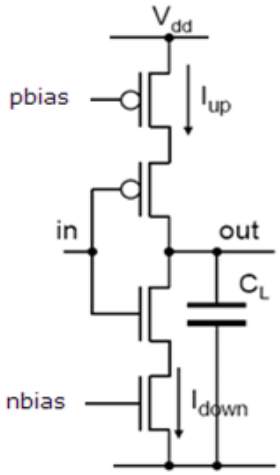

Figure 3.13: Voltage Controlled delay cell

A VCDL consists of a series of such voltage controlled delay cells, which introduce the delay required to align the phases of the input and the output clocks. The number of delay stages is decided by the delay required and the voltage range of the low pass filtered phase detector output.

The voltage controlled delay line consists of multiple stages of single ended starved inverter delay cells. Delay cells exploit the concept of intrinsic delay in CMOS circuits. Consider an NMOS transistor connected to an output load capacitance. The time the capacitance takes to charge or discharge introduces a delay in the response of the circuit. The same is the reason for the delay observed in an inverter. The PMOS

transistor can only pull up the o/p capacitor, while the NMOS transistor provides the pull-down path for the capacitor. The current sourced into or sinked in from the capacitor determines the amount of delay introduced.

In a current starved inverter, the current through the inverter is controlled by two current sources, which in turn are controlled by the bias voltages to the current source devices. The amount of delay introduced is given by.

For Pull-up,

$$\Delta t_{up} = \frac{C}{I_{up}} \frac{V_{dd}}{2} \tag{3.1}$$

For Pull-down,

$$\Delta t_{down} = \frac{C}{I_{down}} \frac{V_{dd}}{2} \tag{3.2}$$

Hence, controlling Iup controls the charging time and controlling Idown, controls the discharging time. Note that the devices are sized in such a way that the switching transistors do not limit the currents.

The delay introduced is a function of two main parameters:

- The sizing of the current source devices which controls the charging or discharging current

- The sizing of the switching transistors which affect the amount of load capacitance seen by the current and the previous stage when cascaded to form a delay line.

The following equation depicts the above relationships:

$$\Delta t = \frac{C}{I_{down}} \frac{V_{dd}}{2} \approx \frac{C}{\mu C_{ox} V_{dd}} \frac{L}{W} \tag{3.3}$$

3.4.4 Bias Generator

The bias generator provides the bias voltages required for the current sources in a current starved inverted delay cell. The bias generator essentially generates the nbias voltage (bias voltage for the NMOS current source - Idown), from the pbias voltage (bias voltage for the PMOS current source - Iup). The circuit of a bias generator is shown in figure 3.14.

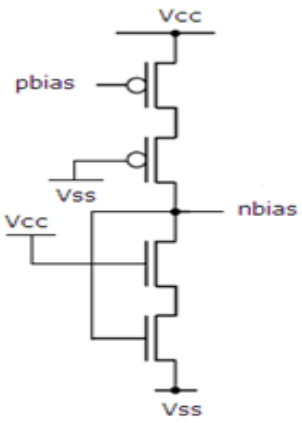

Figure 3.14: Bias Generator

The bias generator implements a PMOS device whose current is controlled by the value of pbias. This current goes through the NMOS device whose VGS is controlled by the magnitude of the current flowing through it. The VGS of the NMOS device provides the nbias voltage required for the down current source of the delay cell.

The most essential characteristic of a bias generator is the linearity between pbias and nbias voltage values. It is essential that the nbias voltage tracks the pbias voltage value linearly in order to match the up and down charging currents of the delay cell, to match the rise and fall time delays introduced.

3.4.5 Filter

In the history of the PLLs the first phase detector was the linear multiplier phase detector. This multiply filters simply multiply the two inputs, and the desired result is reached by eliminating the higher frequency terms (odd -harmonics) in the product. This elimination, or filtering, is done by a low pass filter. In DLLs there is no need to include a low pass filter, instead a capacitor is used in order to integrate the phase error mainly, and thus increasing control voltage appropriately. So filter block is simply a capacitor. Increasing capacitor increases the lock time while decreases the bandwidth and the ripples on the control voltage, and decreasing it decreases lock time and increases the ripples.

Chapter 4

Charge Pump

Charge pumps have been used to generate high voltages for many applications, such as EEPROMs and Flash memories for programming and erasing of the floating gate . In general, a charge pump is a closed loop system because the pump output is usually regulated at a predetermined level. To achieve the regulation, the pump needs to be kept turned on, as long as the output voltage is lower than the regulation level. If the pump output level reaches or exceeds the regulation level, the extra charge from pump output must be shunted away or the pump must be completely shut off.

A basic block diagram of the charge pump's operation is shown in figure. Assuming the pump output voltage is starting from zero at the beginning operation, the output of the regulator is high, Feedback signal from the regulator would enable pumping clocks to be applied to the charge pump .charge is transferred from stage to stage and potential energy of the charge pump will start to ramp up once the charge reaches the output. During this time the regulator is enabled to constantly sample the output voltage and compare it with the reference voltage. When the output reaches the regulation level, the regulator sense it and deactivates the pumping clock. The charge pump is shut off.

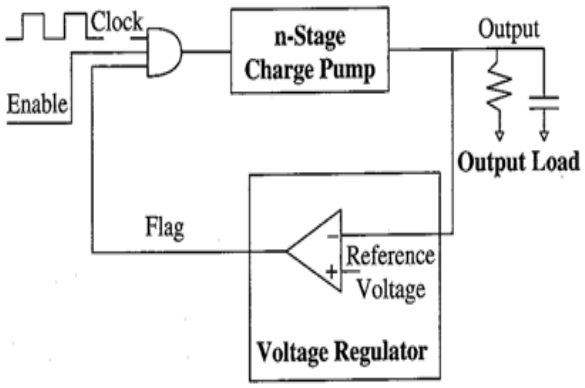

Figure 4.1: Block Diagram of charge pump

If the output load is purely capacitive in nature, the pump output voltage should remain unchanged for long period of time and in principle the pump does not need to be turned on again once regulation level is reached. In reality, though, this scenario seldom happens. Capacitive coupling from nearby signals, he DC current attributing from different output leakage.

Components will obviously cause the output of the charge pump to be discharged over time. Depending upon the pump's feedback response time and other implementations, the regulator will eventually detect the deviation of output voltage from the regulation level and enable the charge pump. since the output is closer to the original preset level, the pump should be able to replenish the lost charges faster and reach regulation level only in short amount of time. As shown in figure This process will introduce output voltage overshoot and undershoots near regulation level.If the amplitude of noise is large, it may be detrimental to the functionality and device -related reliability of the circuit.

The operation-dependent power balancing between pump and output load scheme relies on matching pump output strength with the loading circuit power consumption at all time. The charge pump may have different output power specifications in many different operations. Even within the same operation the loading circuit may have different current loads over time. Noise occurs if there is mismatch between the

delivered power from the pump and the consumed power from the load. If pump strength can be adjusted based on operation, then the output noise can be minimized. Pump strength can be adjusted as required by varying clock frequency, pump clock amplitude, sizing of effective boosting capacitance, etc., the second approach used a voltage-controlled oscillator instead of a steady clock generator. The clock frequency of the VCO will be high when the pump is initially starting up. Then this clock frequency will slowly decrease in an almost linear fashion as the output voltage approaches the regulation level and will almost stop when the value is reached. The latter approach is more complex to implement and not suitable for all applications.

At the end of the high-voltage operations, it is required to shut off the charge pump, discharge the high-voltage potential at the output and all internal nodes, and bring them down to normal chip supply levels. This shut-off and discharging process should be carefully managed. If the pump circuit, including the regulator, is shut off before discharging, it may create unwarranted high-voltage stress on some circuits. Further, discharging the high voltage to internal chip supplies may create high-ground bounce or high-Vcc bounce without careful timing controls. The noise could create problems for other circuits still in operation. In general, it is better to discharge the internal high-voltage nodes during a pre-defined period for high-voltage recovery purposes only.

4.1 Basic Concept - The Bucket Capacitor Model

Charge pumps are circuits that generate a voltage level higher than the chip supply voltage from which they operate. To see how this is possible, consider the simple circuit shown in Figure 4.2. which consists of a single capacitor and three switches.

During clock phase, ϕ, switches S1 and S3 are closed and the capacitor is charged to the supply voltage, VDD. Next, in the second clock phase, ϕb, switches S1 and S3 are opened and switch is closed. The bottom plate of the capacitor assumes a potential of VDD, while the capacitor maintains its charge of Q = C * VDD from

the previous phase.

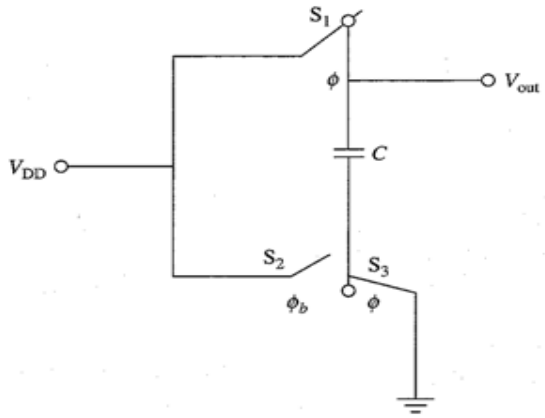

Figure 4.2: Simple voltage doubler

Thus, in the absence of a DC load, an output voltage can be generated that is twice the input supply voltage. In order to accommodate a load at the output, the circuit should be modified by adding an output capacitance, as shown in figure 4.2.

In this case, the ideal output voltage is given by,

$$V_{out} = \frac{C}{C + 2C_{out}V_{dd}} \tag{4.1}$$

Needless to say, the presence of the output capacitor Cout will reduce the output voltage, depending on the output load capacitor. If a load, RL, is present, a ripple voltage, VR, will also generate at the output.

The ripple voltage can be reduced by making Cout sufficiently large so that VR is negligible compared to Vout, but in doing so the output voltage will also be reduced. It is important to note that the switches mentioned in this circuit can actually be implemented using n-type MOSFETs or p-type MOSFETs, and the capacitor can be

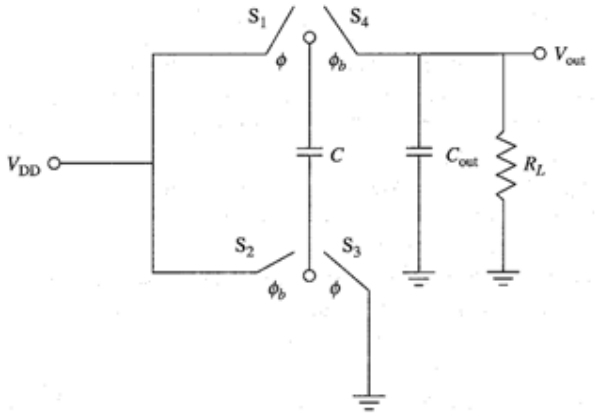

Figure 4.3: Voltage doubler with Load

standard metal-metal capacitance or realized using the gate oxide of the MOSFET, with its source-drain substrate connected together to form one and the gate forming the other end. It is also important to pay considerable attention to the type of MOSFETs used in circuits involving high voltages.

4.2 Charge Pump Design Criteria

A charge pump is a common system, the construction of which is based upon simple CMOS transistors and capacitors. Relying on charge conservation theory and the capacitive coupling method, the charge pump generated the final output voltage, which can be either higher or lower than the given chip supply voltages.

Many criteria should be considered before the actual design work can start. Normally designers should consider at least two things: the available technology and the product specification. Technology involves the wafer processing for the chips. Models and parameters such as capacitance, sheet resistance, interconnection, and transistors are set by the technology and are used by designers in circuit design. The product specification contains the requirements the final product must achieve. Specifications such as power-consumption requirements, the pump-regulation level, the power efficiency of the design and die size, and so on, are the targets the circuit

design has to meet on silicon.

- Technology
  - Supply voltage
  - Silicon dixide
  - Resistor
  - Transistor Specification
- Specification
  - Output Load characteristic
  - Pump Output current
  - Ripple on Regulated Output Voltage
  - Pump Regulation
  - Capacitive Devider
  - Resistive Devider
  - MOSFET biased type regulator
- Resistor
- Transistor Specification

4.3 Implemented Charge Pump

Figure 4.4 shows the charge pump circuit with a loop filter When the M1 and M2 current source devices are connected to the output node, the output voltage is isolated from any switching noise resulting from the overlap capacitance of the M3 and M4 switch devices.

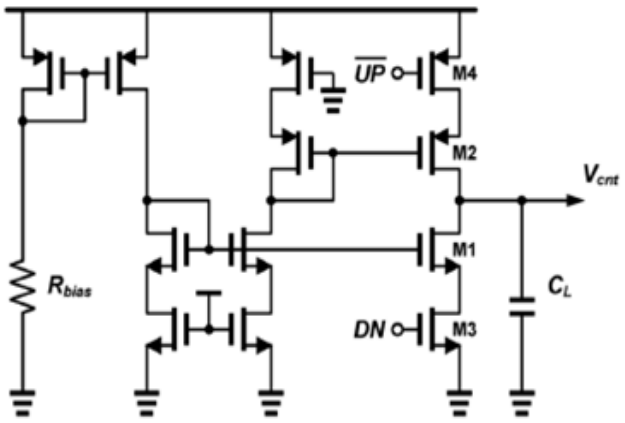

Figure 4.4: Charge Pump Circuit with Filter

Since both of the NMOS and PMOS current sources are always turned on in each cycle, any charge injection will be canceled out to the first order with equal device sizes of the current source. To minimize the diffusion capacitance, the layout for the current source and switch devices contain no diffusion contact between the two gates. The two switch devices are folded together for matching and layout constraints, creating two unconnected intermediate nodes.

Chapter 5

Phase Frequency Detector

A number of different circuits can be used as PDs. In earlier days, people used multiplier, exclusive-OR gate and JK-flip-flop for phase detection. Auxiliary circuits were often needed to assist the acquisition of frequency locking. A second class of PD, the tri-state PD or phase-frequency detector (PFD), provides both phase and frequency-detection capability, which is favorably (if not exclusively) used in most Delay-locked loops.

The characteristics of a PD have great impact on the performance of DLLs. Several dynamic-logic PFDs are analyzed that more or less demonstrate certain drawbacks such as large dead-zone or blind-zone.

5.1 EX-OR gate

The operation of an exclusive-OR gate used as a PD is shown in Figure When the two input square-wave signals are 90 out of phase, the output will have a 50 percentage duty cycle, giving an average value of zero. When the phase difference deviates from 90, the output duty cycle is no longer 50 percentage, and the average value of the output is proportional to the phase difference. The monotonic detection range in this case is $(0, \Pi)$. If the waveforms of the input signals are not symmetrical, the detection range may be significantly reduced.

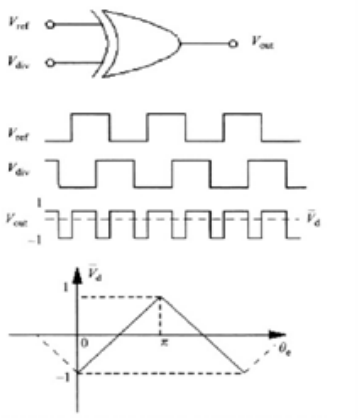

Figure 5.1: Exclusive OR Phase Detector and its phase characteristic

This can be illustrated by considering an extreme situation when both the inputs have a small duty cycle, for example, 1 percentage. In this case, the average output is clipped to a value close to zero and the whole detection range is 2Π /100 only. This PD is not frequency sensitive.

5.2 Flip-Flop based PD

5.2.1 J-K Flip-Flop

An edge-triggered JK-flip-flop can be used as a PD, as shown in Figure 5.2 In this device, a positive edge at the J input triggers the output to "high" and a positive edge at the K input triggers the output to "low". Note that the average of the output reaches zero when the two input signals are at opposite phase. The average output reaches maximum when there is a 360 phase difference, and reaches minimum when the two signals are in phase. So the phase-detection range of this PD is twice that of the previous two PDs. In addition, because this PD is edge triggered, the waveforms of the inputs do not need to be symmetrical. Similar to the exclusive-OR gate PD, the JK-flip-flop is not capable of frequency detection.

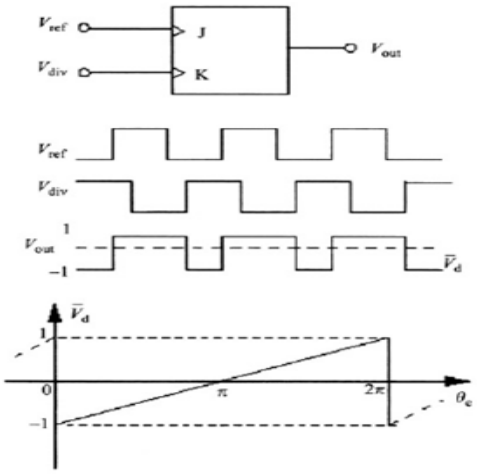

Figure 5.2: J-K Filp-Flop based PFD

5.3 Tri state phase detector

A tri-state PD, or PFD, is shown in Figure 5.3. It is composed of two D-flip-flops and an AND-gate, and has two output terminals UP and DN. At any time, the two outputs of the PFD, UP and DN, will be at one of four states: 00, 01, 10, 11, with UP = high, DN = low represented by state 10, etc. The fourth state is an unstable state (at state 11, the AND-gate will reset the D-flip-flops). In general, the tri-state PFD is implemented together with a charge pump, as illustrated in the dashed-line box in Figure 5.3. In this simple illustration, the charge pump is composed of a P current source and an N current source. The two current sources are controlled by the two outputs of the PFD. An active signal at UP (UP = 1) will turn on the P current source, allowing a positive current to flow into the output node (node and make the output voltage to rise. Similarly, an active signal at DN (DN = 1) will turn on the N current source, which pulls current from the output node, causing the voltage at the output node to reduce. When both UP and DN are not active (UP = 0, DN = 0), both current sources are turned off from the output node, then the voltage at node will remain unchanged.

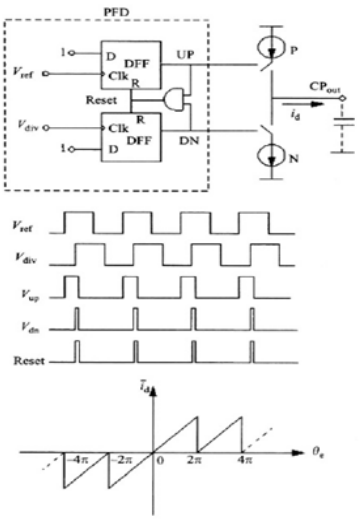

Figure 5.3: A Tri State PFD with Charge Pump and its ideal phase Characteristic

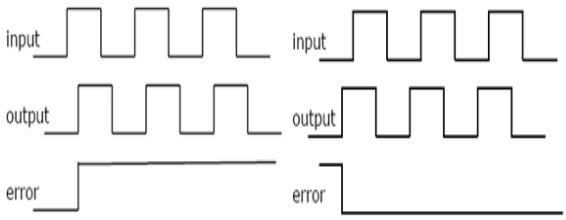

Figure 5.4: Lead and lag outputs of a Phase Detector

The operation of the PFD is illustrated in Figure 5.3 as well. A positive transition in the REF signal causes the UP terminal to transit to "high". Similarly, a positive transition in the DIV signal causes the DN terminal to transit to "high". When both UP and DN are "high", the PFD is reset, which brings UP and DN to "low". The average output of the PFD is given in Figure 5.3. This time, the output is expressed in current instead of voltage, since our interest is the average current flowing in and out of node It turns out that the ideal linear phase-detection range of this PFD is which

is twice that of the JK-flip-flop PD's detection range. Beyond this range, the phase characteristic curve is periodic with a period of. To look at the extra frequency-detection feature provided by this device, we assume that the REF frequency is higher than the DIV frequency. Notice that now the REF signal will have more positive transitions than the DIV signal, as such the UP terminal will have more chances to stay at "high" than the DN terminal. This means more current will flow into node causing the voltage to increase. We conclude that the tri-state PD has superior performance than other PD in terms of phase-detection range and frequency sensitivity. Up to now, our focus is on the ideal behavior of PDs.

5.4 Design Issues in Phase-Frequency Detectors

5.4.1 Dead-Zone

Instead of using complex reset D-flip-flops, a tri-state PFD is often implemented in the form of Figure 5.5. Note that the reset signal is generated from intermediate signals instead of from the UP and DN outputs directly. If the phase difference of the input signals is small, a positive transition at UP or DN will be closely followed by a reset operation. If the propagation delay at UP and DN is large enough, it is possible that UP or DN may be pulled to low by the reset operation before it completes a positive transition. Consequently, the charge pump output voltage will keep intact at a small phase difference. This phenomenon is called "dead-zone", and is shown in Figure 5.7, with the dead-zone exaggerated. In a DLL, if the input phase error is within the deadzone, it will have little influence on the VCDL control voltage. A delay cell is usually inserted in the reset path such that the reset pulse is wide enough to allow the PFD outputs become effective before they are reset (Figure 5.5). By doing so, the UP and DN outputs are given enough time to make a positive transition, and thus dead-zone can be reduced. Nevertheless, the maximum operating frequency of the device will be limited by the total delay of the reset path. Since the

maximum operating frequency happens when REF and DIV are in opposite phase, an approximate estimation of the operating frequency is given as follows.

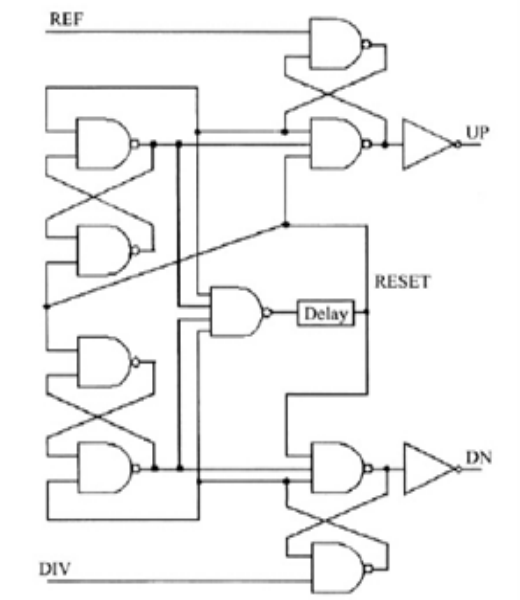

Figure 5.5: J-K Filp-Flop based PFD

Assume equal gate delay tg for the internal gates and tG for the driving gates of UP/DN nodes in Figure 5.5. Also, denote the delay time of the delay element as td. It follows that the minimum RESET pulse width is 3tg+td and the delay time from the input (REF or DIV) to RESET is 2tg+td . Any transition edge in REF and DIV will be ignored during the reset operation (RESET = 1), and this is considered abnormal. To avoid such a situation, a transition in REF or DIV should happen after the reset operation. The maximum operating frequency is therefore given by,

$$f_{max} = \frac{1}{2(5t_g + 2t_d)} \tag{5.1}$$

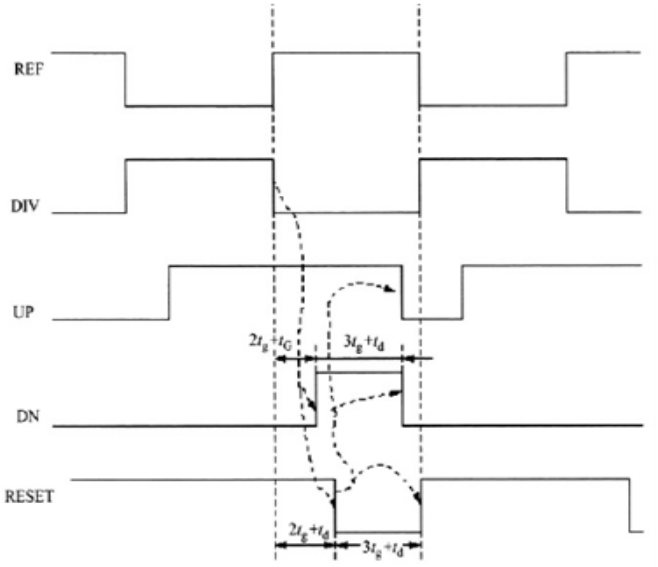

Figure 5.6: Maximum Frequency Estimation

5.4.2 Blind-Zone

The PFD output characteristic curve in Figure 5.7 rises monotonically with phase error. When the phase error approaches, The curve changes to the opposite sign abruptly. The cause of the abrupt polarity change can be explained through timing analysis. In Figure 5.8 , the occurrence of a REF rising edge coincides with a reset operation (RESET = 1) and, therefore, does not have any impact on the PFD output. This situation is depicted in Figure 5.8 by the dotted area. Consequently, the leading REF signal is incorrectly indicated by the PFD as lagged (DN is wider than UP) in a subsequent cycle. As long as a PFD is in reset mode, it will be blind, that is, any input transition will not be seen by the PFD.

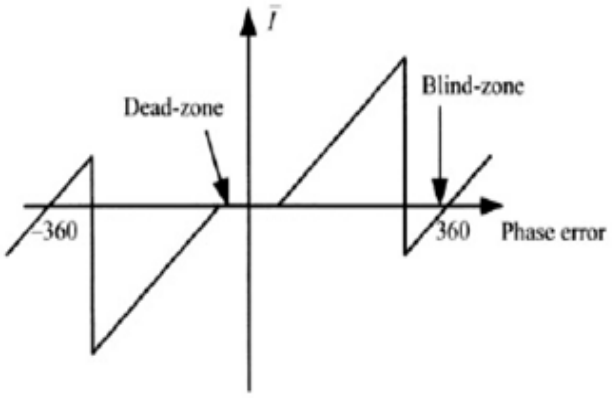

Figure 5.7: Dead Zone and Blind Zone

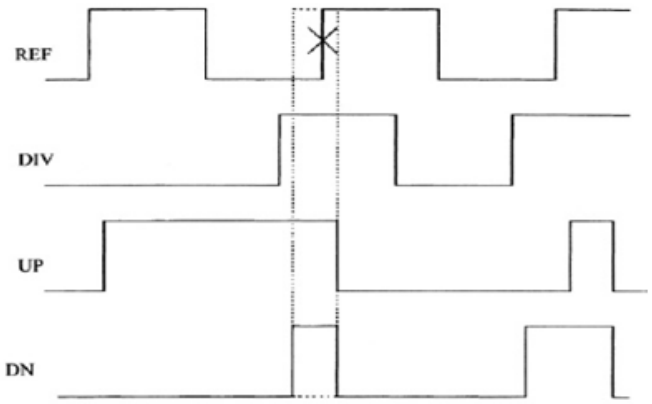

Figure 5.8: Timing analysis of blind Zone

5.5 Convectional Precharged PFD

The conventional Precharged PFD shown in below figure is designed to overcome the speed limitation and to reduce the dead zone. The dead-zone occurs when the loop is in a lock mode and the output of the charge pump does not change for small changes in the input signals at the PFD. An improved Precharged PFD is used in this DLL design. The Precharged PFD is a modified version of the conventional type to reduce the jitter of the DLL.

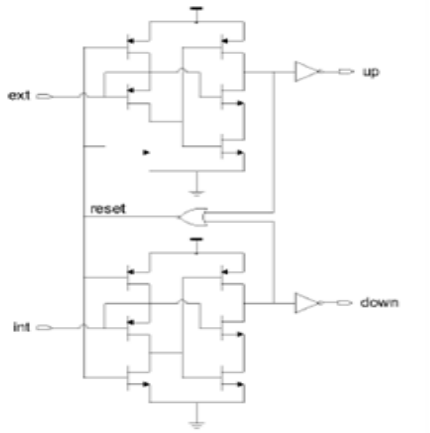

Figure 5.9: Convectional Precharged PFD

In conventional Precharged PFD, when the clock is in phase, one-shot pulse will be produced. This pulse is consists of both the up and down output. For in-phase inputs of ext and int, the up charge pump will see both up and down pulse for the same short period of time. This one-shot pulse is produced due to the dynamic behavior of the TSPC DFF. Whenever ext and int goes high, the circuit would need to send a reset pulse to reset the circuit. The amount of delay time to reset all internal nodes determines the circuit speed. The one-shot pulse is reset required to eliminate the dead zone of the PFD. The optimum one-shot pulse is the one which can produce just enough pulse width to enable the charge pump to pump current into the loop filter.

However, unnecessary long one-shot pulse will reduce operating frequency of the PFD and the additional charges that are introduced to the charge pump can cause jitter at the output. up This jitter is caused by the up and down current mismatch in ext the charge pump. Therefore, it is undesirable for the width of this signal to be too large.

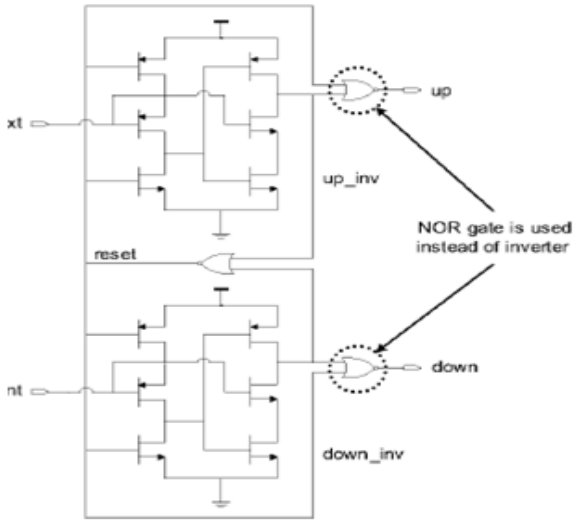

Figure 5.10: Implemented PFD

The proposed PFD is designed in a way to minimize this signal to reduce the jitter cause by the up and down mismatch in the charge pump. By knowing the part of the one-shot pulse when that the reset signal is HIGH is not reset X necessary, we can eliminate the additional pulse width by replacing the inverter before the output of the conventional Precharged PFD with a NOR gate. The input to the NOR gate is the output signal of the TSPC DFF and the reset signal.

5.6 A High Performance Dynamic Logic Phase Frequency Detector

Dynamic CMOS logic circuits and especially domino-logic have been used in high-performance designs due to their faster operating speed and potential saving in power.

A pioneer dynamic-logic (domino-logic) PFD is shown in Figure 5.11 In this circuit, the outputs are reset almost immediately following a positive transition at one of the inputs if initially a positive transition has occurred at the other input. As a result, the circuit experiences dead-zone problem. In this design, dead-zone cannot be effectively reduced by adding an extra delay in the reset path as given in Figure

5.5 . Furthermore, the detection range of this circuit is only $(-\Pi, \Pi)$. To see this problem, consider a situation that a positive transition in REF occurs when DIV = 1: in a normal tri-state PFD, following the rising edge of REF, UP should be pulled to "high". In this circuit, UP will stay at "low" instead. This is because node U1 is discharged and node U2 is charged immediately after the rising edge of REF. UP gets no time to transit to high.

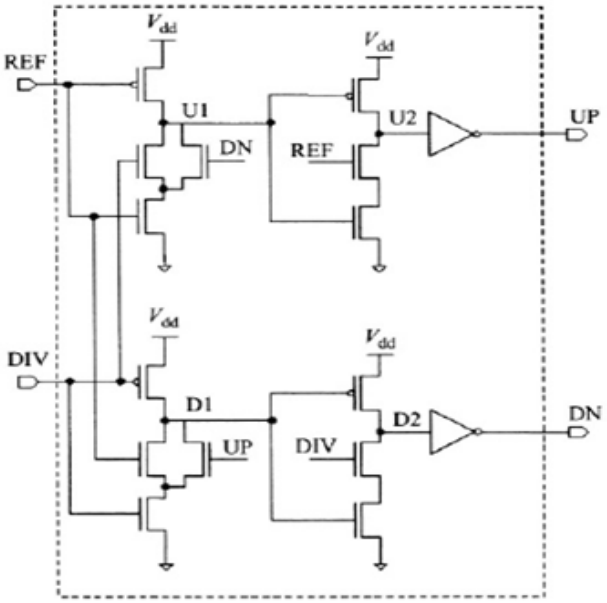

Figure 5.11: Dynamic Logic PFD

The dead-zone problem in the above design was partially improved in (Figure 5.12). This is accomplished by the three inverters and two NMOS transistors at the REF (or DIV) input, which basically form a pulse generator to create a delay for the discharge of node U1 (and U2) such that UP and DN can become effective for a certain amount of time. A defect in this circuit is that a DC path might be formed from the power supply to the ground through node U1 or U2. For instance, if DIV is transiting from 0 to 1 while REF = 0, a DC path is formed through node

U1. Depending on whether the voltage at node U1 is low enough to be below the threshold of the following PMOS transistor, the UP signal may or may not be reset. Because of this, this circuit also has a limited linear detection range of $(-\Pi, \Pi)$.

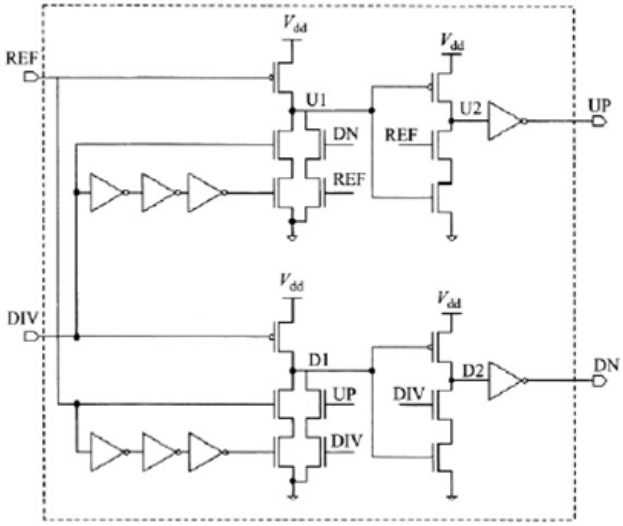

Figure 5.12: A Dynamic logic PFD with reduced Dead Zone

Shown in Figure 5.13 is another dynamic PFD circuit. Unlike the two .dynamic PFDs discussed above, in this design, the reset action is initiated solely by the PFD outputs. This means that a reset process will not happen until UP and DN become effective. For this reason, dead-zone is not visible in this design. There also exists a defect in this circuit: assume a rising edge of REF has caused a positive transition at UP, and soon after REF returns to 0.Subsequently, if a rising edge of DIV causes a positive transition at DN, a DC path will be formed between the power supply and the ground via node U1 since REF = 0, UP = 1, and DN = 1. This situation is very similar to the short-circuit problem found in Figure 5.12. The linear detection range of this circuit is only $(-\Pi, \Pi)$ as well.

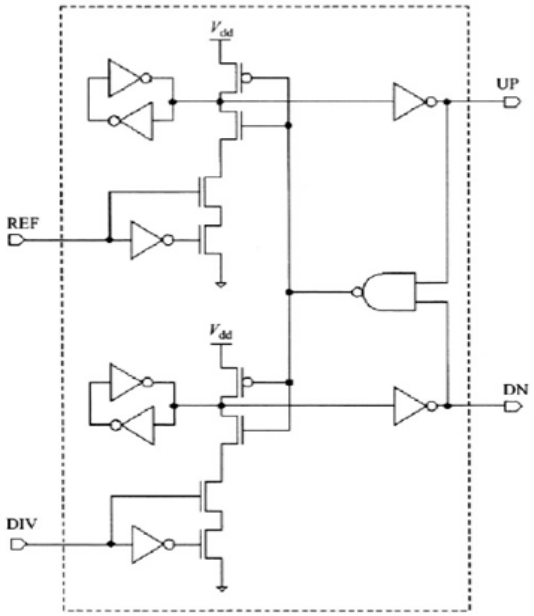

Figure 5.13: A Dynamic PFD without Dead Zone

A common problem in the above three dynamic PFDs is that they are not purely edge sensitive, and especially, the two circuits in Figures 5.12 and 5.13 violate the operation integrity of domino circuits, although they seem to perform better in terms of dead-zone. By using two pulse generators (similar to that used in Figure 5.12), a dynamic-logic PFD disclosed in (Figure 5.14) is made to be purely edge sensitive. The device then functions in the same way as demonstrated by the original tri-state PFD (Figure 5.3). Ideally, the phase-detection range will approach Yet, according to our analysis on blind-zone, a blind-zone of approximately three gate-delays exists in this circuit. This circuit is relatively very simple, but requires a careful control of the delay of the pulse generators in order to reduce dead-zone. Extra latches are used (the cross-connected inverters) in this circuit to ensure proper operation, which also slows down its operating speed.

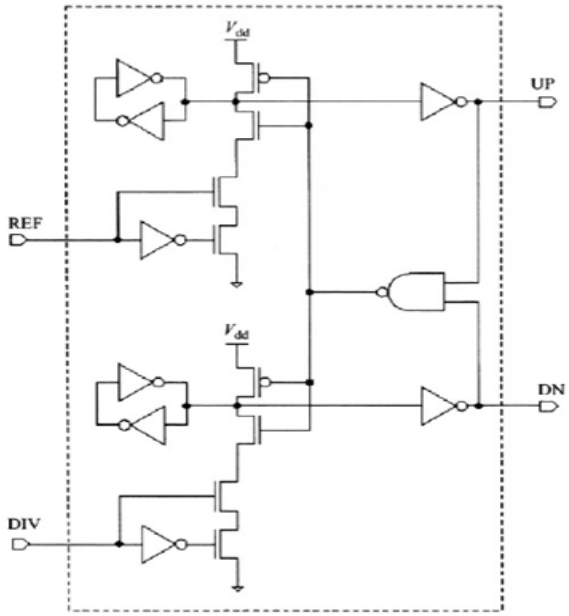

Figure 5.14: A Dynamic PFD with reduced blind Zone

5.7 A Novel Dynamic-Logic Phase-Frequency Detector

In an effort to design a PFD capable of working at gigahertz frequency with minimum dead-zone, minimum phase offset and reduced blind-zone, we have proposed a new domino-logic PFD. Our design goals are accomplished by overcoming the drawbacks existing in previous dynamic PFDs. Circuit integrity is maintained in this design.

The new PFD is shown in Figure 5.15 . MU2-3 and MD2-3 form two inverter structures in the precharge stage that basically prevent the device from being short-circuited as happened in Figures 5.12 and 5.13. It should become obvious that the circuit will be fully operational with a permutation of MU1 and MU2, MU3 and MU4 (also MD1 and MD2, MD3 and MD4).

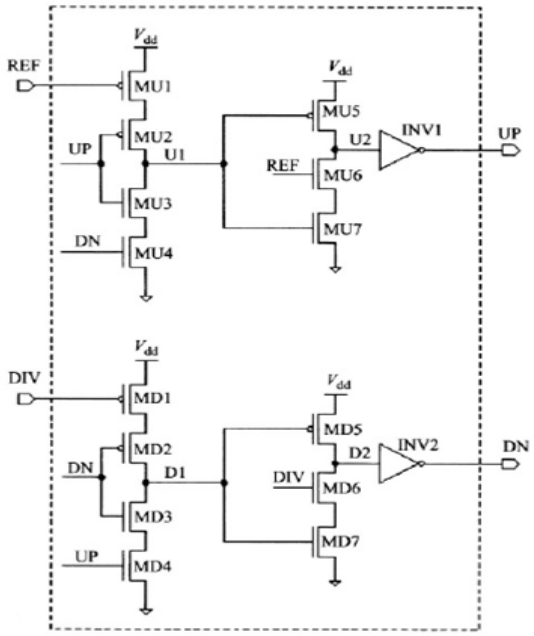

Figure 5.15: The Proposed Dynamic PFD

5.7.1 Circuit Operation

To inspect the behavior of this PFD more closely, we have shown a finite-state diagram of the PFD with all its four possible states included (Figure 5.16). In the diagram, each state transition is accompanied by its corresponding transition condition, which is basically the positive transition of REF or DIV, denoted by and respectively. Two simultaneously occurring positive transitions are simply denoted by (REF,DIV).

The operation of the circuit can be explained according to the charging and discharging behavior of typical dynamic circuits. Assuming initially UP and DN are both low (state = 00) and REF and DIV are low, nodes U1 and D1 are pre-charged to high through transistor MU1-2 and MD1-2 respectively. At the rising edge of REF, MU6-7 are turned on, node U2 is pulled to low, which drives UP too high. Similarly, a rising edge of DIV will drive DN to high. If the rising edge of REF comes first, the state will transit from 00 to 10, and then transit from 10 to 11 upon the arrival of a rising edge of DIV. If the rising edge of DIV comes first, the state transition will be

from 00 to 01 and then to 11. In the case that the rising edges of REF and DIV come simultaneously, the state will transit from 00 to 11 directly. State 11 is an unstable state, as identified by the dashed circle. At state 11, UP and DN will turn on MU3-4 and MD3-4, nodes U1 and D1 are discharged accordingly, and nodes U2 and D2 will be charged to high through MU5 and MD5, respectively. This returns the circuit to state 00.

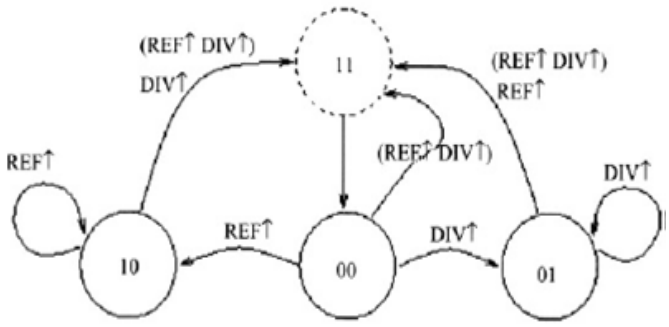

Figure 5.16: Finite State Diagram of PFD operation

Indeed, all the tri-state PFDs operate in the above manner, that is, a rising edge of REF drives UP to high, and a rising edge of DIV drives DN to high. When both UP and DN are high, the circuit is reset, returning UP and DN to low. This general statement may disguise the truth. As we have carefully inspected all the previously mentioned dynamic PFDs, when the phase error is beyond some of the dynamic PFDs behave differently from expected. For this reason, we examine the operation of our PFD cautiously as below. Assume REF is leading DIV by more than 180: initially, a leading rising edge of REF drives the device to state 10 as before. Now, upon a DIV rising edge, DN will be pulled to "low". At this moment, REF is "low", but UP is driven "high". So, the path formed by MU1-2 is shut off and no charge is injected from to node U1 during the time when U1 is being pulled to "low" through path

MU3-4. UP is therefore reset to low normally. This clarifies that the detector indeed operates correctly when phase error lies between $(\Pi, 2\Pi)$.

Chapter 6

Simulation Results

6.1 Inverter characterization

The most important component of a DLL is the delay cell, which is actually a current starved inverter. Hence, as a pre-cursor to starting the DLL simulation, the characterization of the inverter with the devices to be used in the delay cell was done. Multiple simulations were carried out with the inverter, to characterize the sizing required to match the drives of the PMOS and NMOS devices owing to their mobility differences and the VT of the devices used.

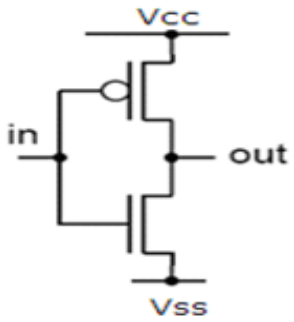

Figure 6.1: Inveter

The sizing ratio of the PMOS to NMOS devices was determined for which the output waveform had equal rise and fall times for an ideal input signal. Figure 6.1 below shows the simulated waveform of an inverter - input/output, and Figure 6.2 shows simulated waveform ,which involve delay and duty cycle measurement.

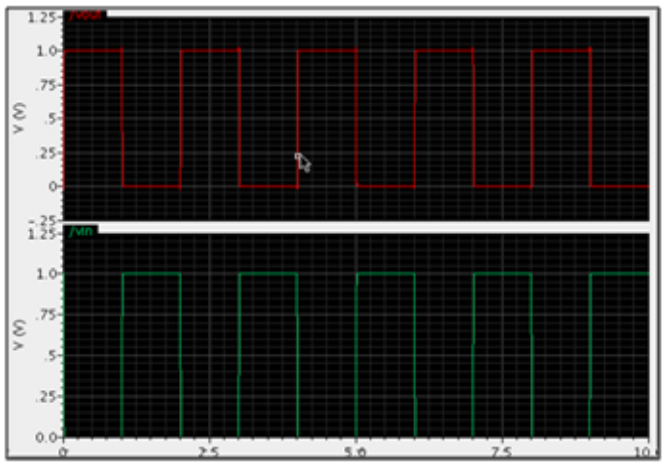

Figure 6.2: Transiant Analysis of Inverter

6.2 DLL Block Diagram

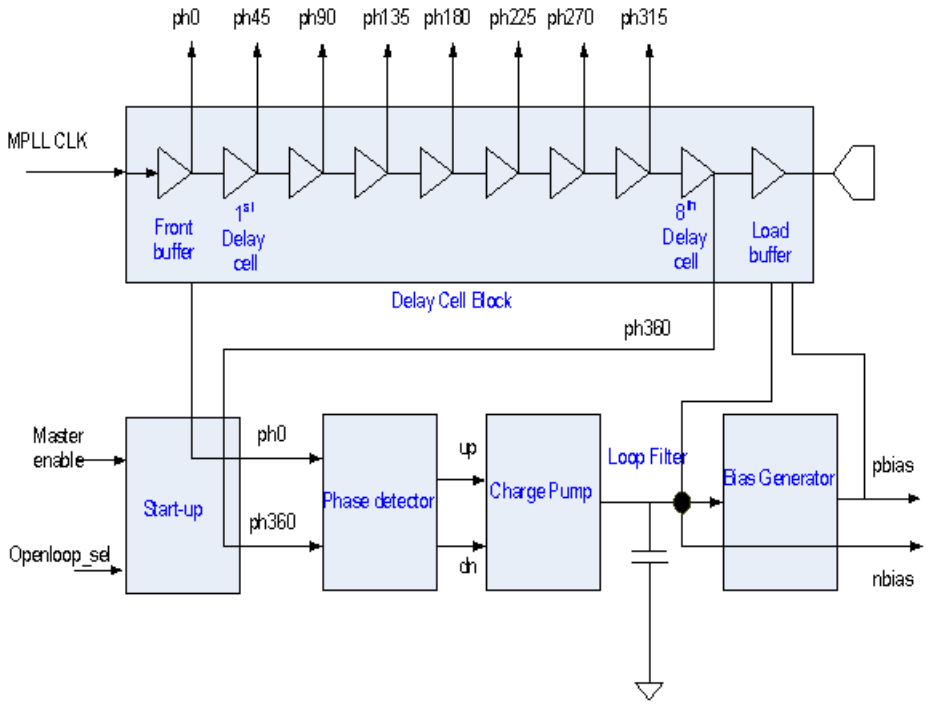

Figure 6.3: DLL Block Diagram

6.2.1 Bias generator

The bias generator provides the bias voltages required for the current sources in a current starved inverted delay cell. The bias generator essentially generates the nbias voltage (bias voltage for the NMOS current source - I down), from the pbias voltage (bias voltage for the PMOS current source Iup).

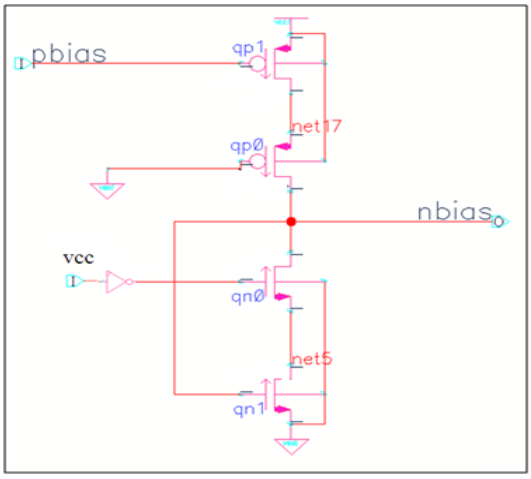

Figure 6.4: Bias Generator Block Diagram

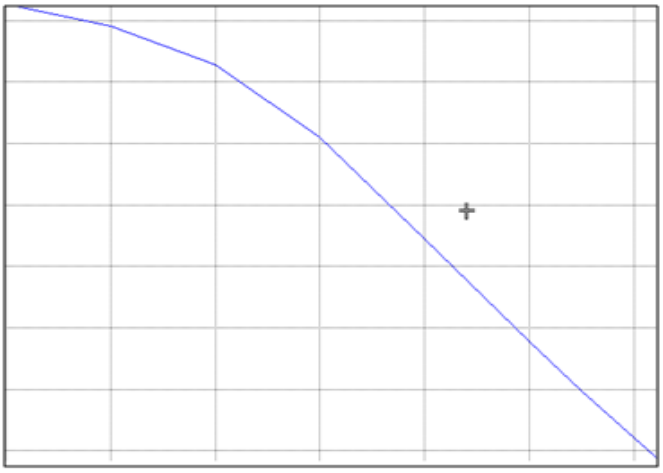

Figure 6.5: Bias Generator Characteristic (Pbias Vs nbias)

As we observe from the graph, the relationship between nbias and pbias voltage values are linear for a pbias voltage. The bias generator circuit was also tested with sudden rise in pbias values to ensure that the circuit did not result in oscillations.

6.2.2 Delay Cell

Single Ended Delay cell:-

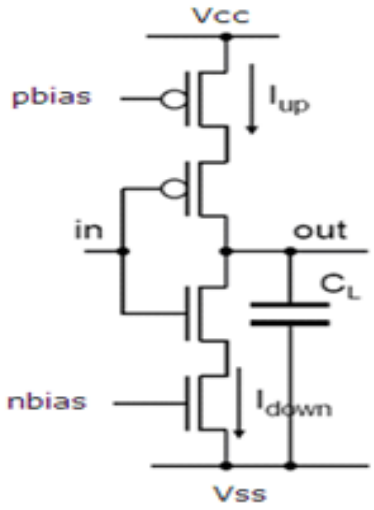

Figure 6.6: Single Ended Delay Cell

Delay cells exploit the concept of intrinsic delay in CMOS circuits. Consider an NMOS transistor connected to an output load capacitance. The time the capacitance takes to charge or discharge introduces a delay in the response of the circuit. The same is the reason for the delay observed in an inverter. The PMOS transistor can only pull up the o/p capacitor, while the NMOS transistor provides the pull-down path for the capacitor. The current sourced into or sinked in from the capacitor determines the amount of delay introduced. The schematic of a single stage starved inverter delay cell is depicted in figure 6.6.

Single Delay Cell Schematic:-

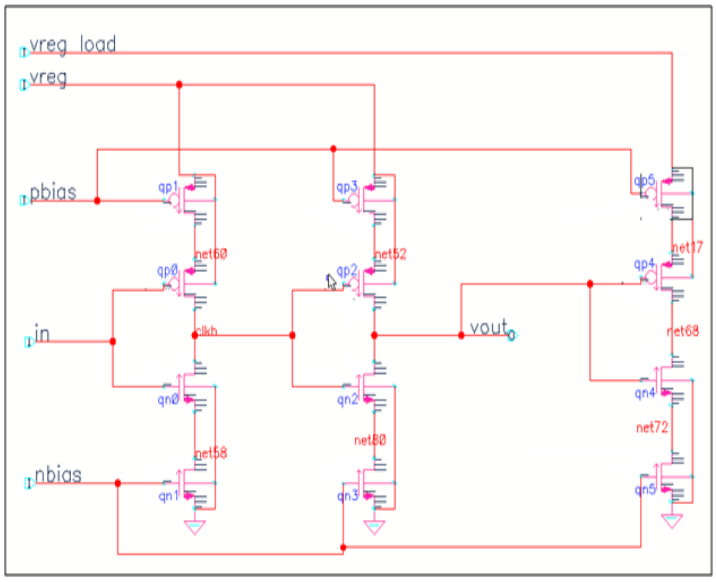

Figure 6.7: Delay Cell (Two Inverters connected back to back)

Delay between input and output (Two inverter Delay):-

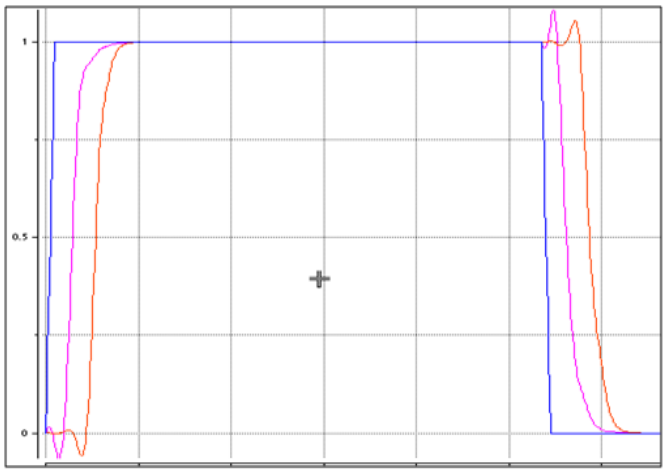

Figure 6.8: Delay between two Inverters

Bias Generator Schematic:-

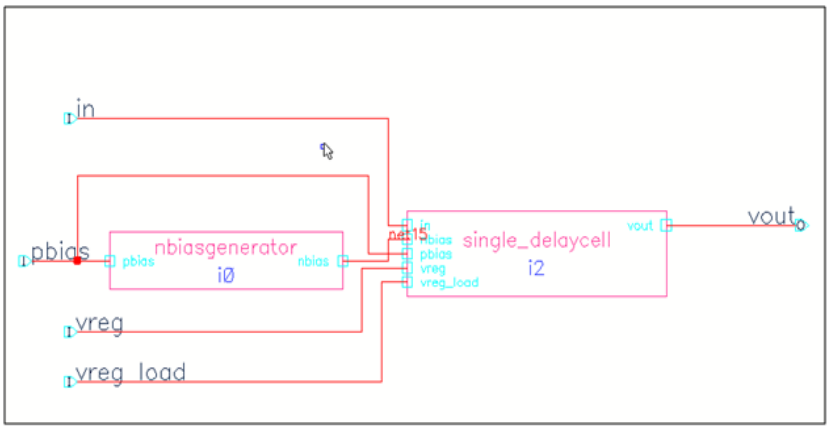

Figure 6.9: Single Delay Cell with Bias Generator

Delay Cell Characteristic:-

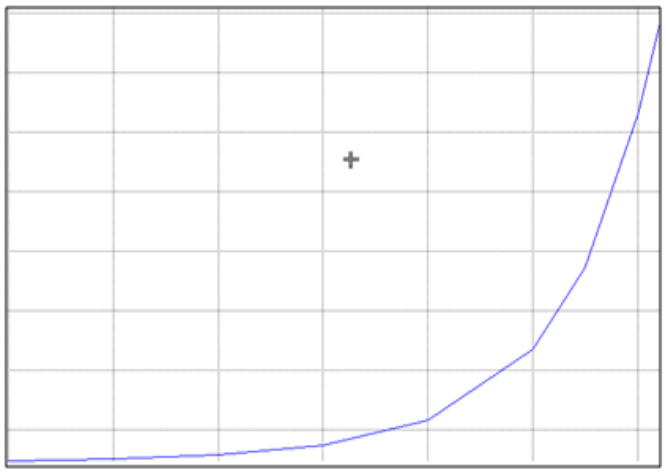

Figure 6.10: Delay Vs Pbias

6.2.3 Charge Pump

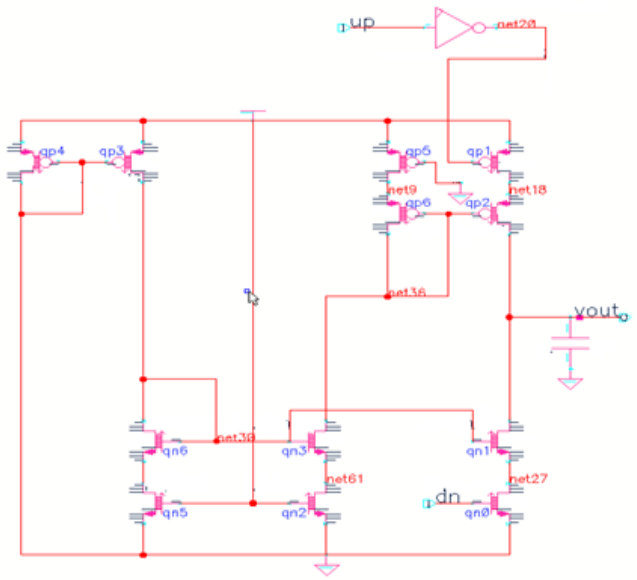

Figure 6.11: Charge Pump

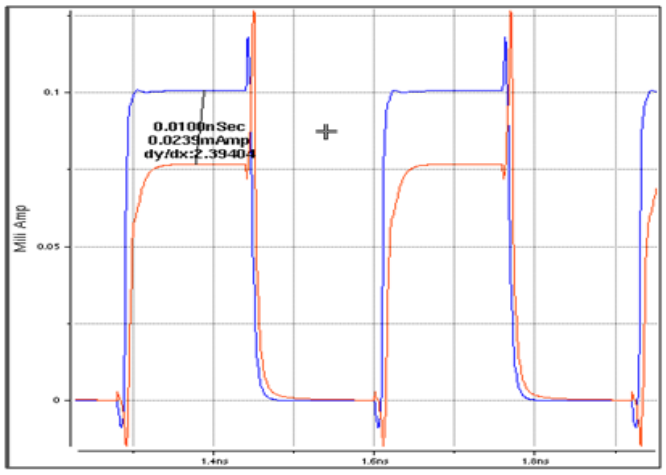

Figure 6.12: Offset Current (23uA)

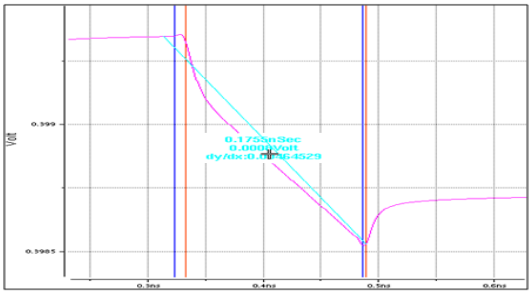

Figure 6.13: Output Voltage 0.8 mv

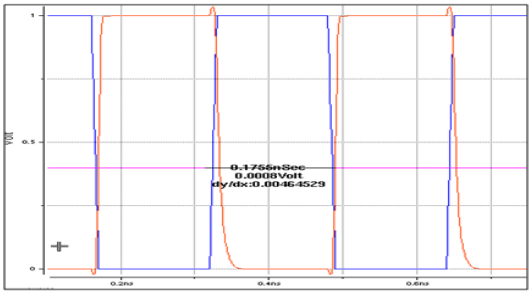

Figure 6.14: Output Voltage (Up and Down inputs simultaneously)

Down signal is applied as input:-

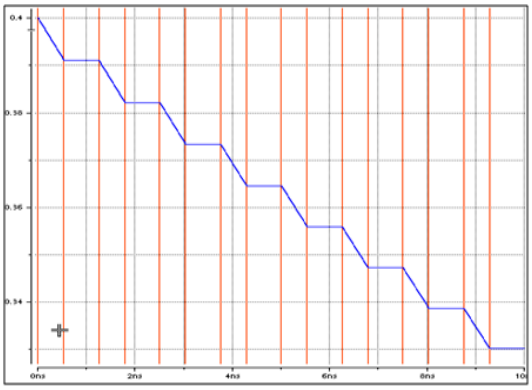

Figure 6.15: Vout (Discharging of Cap)

UP signal is applied as input:-

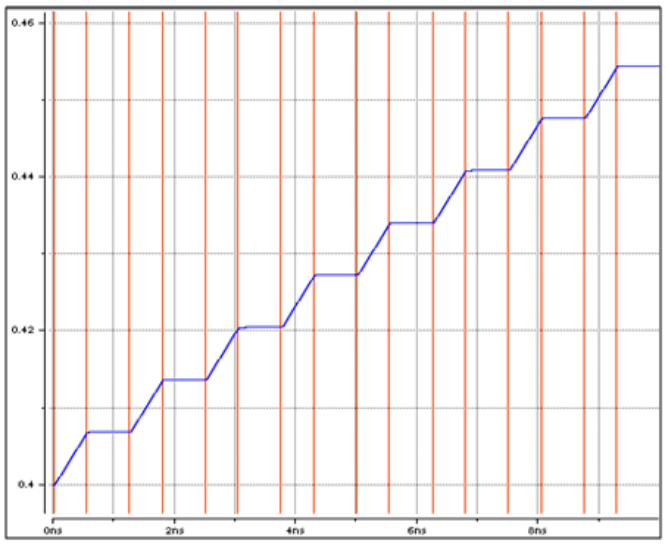

Figure 6.16: Vout (Charging of Cap)

Source and Sink Current:-

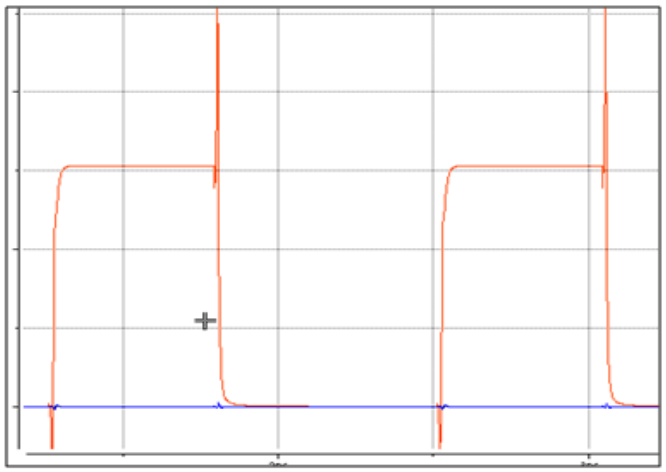

Figure 6.17: Source Current

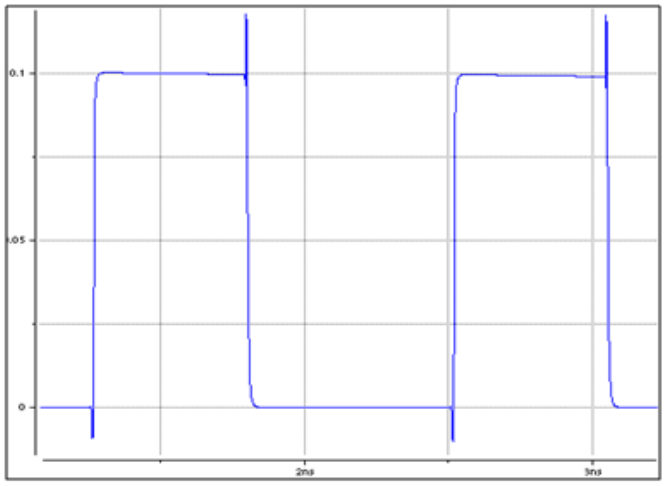

Figure 6.18: Sink Current

6.2.4 Phase Frequency Detector

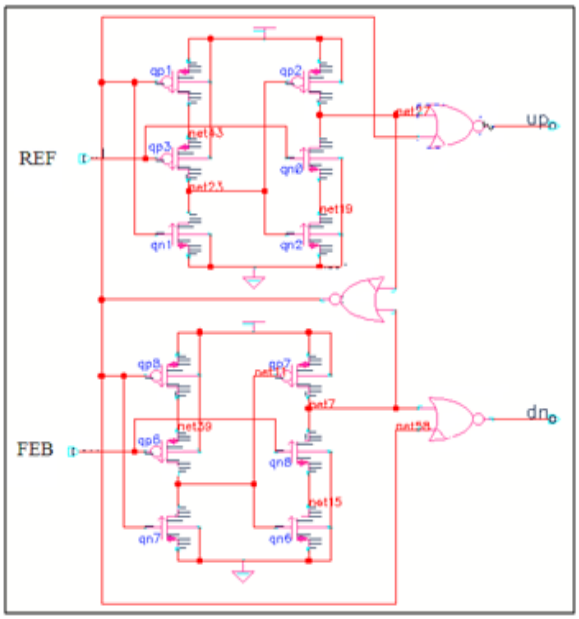

Figure 6.19: Implemented PFD

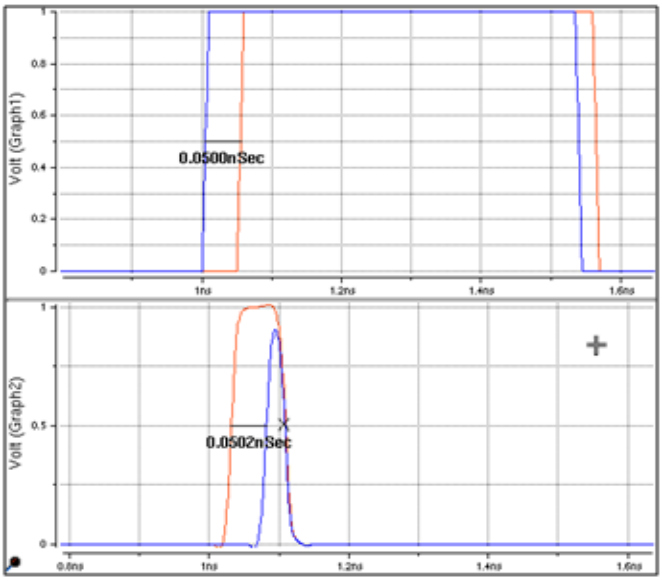

Figure 6.20: Up and Dn Signal

Dynamic Logic PFD:-

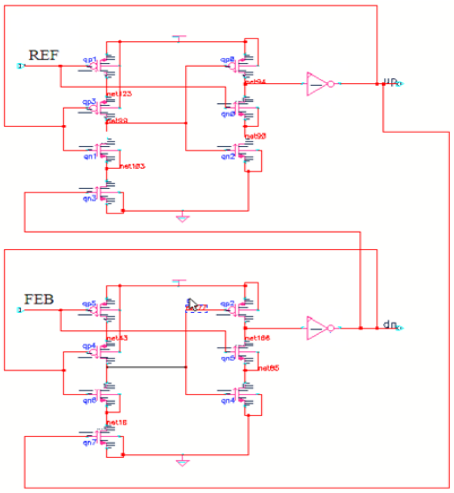

Figure 6.21: Dynamic Logic PFD

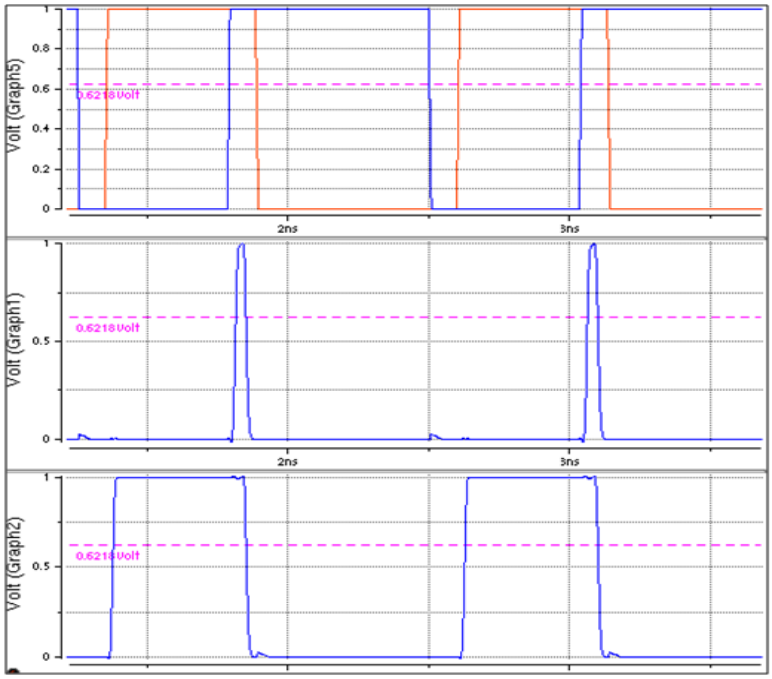

Figure 6.22: Simulation Result of Dynamic Logic PFD

6.2.5 DLL Closed Loop Simulations

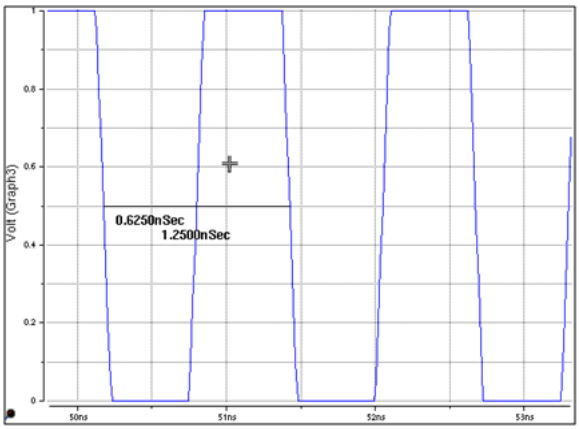

Figure 6.23: Input Clk

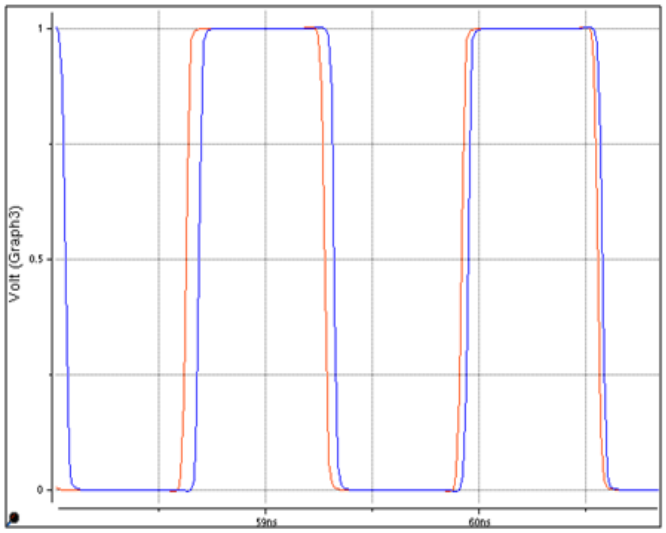

Figure 6.24: REF,FB Clk (Before Locked)

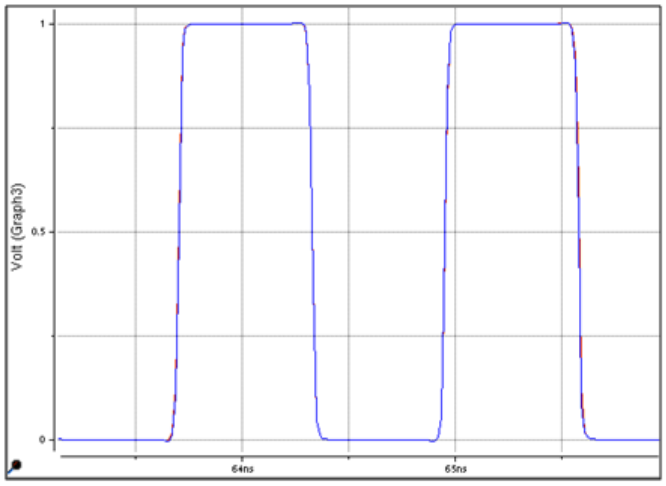

Figure 6.25: REF,FB Clk (After Locked)

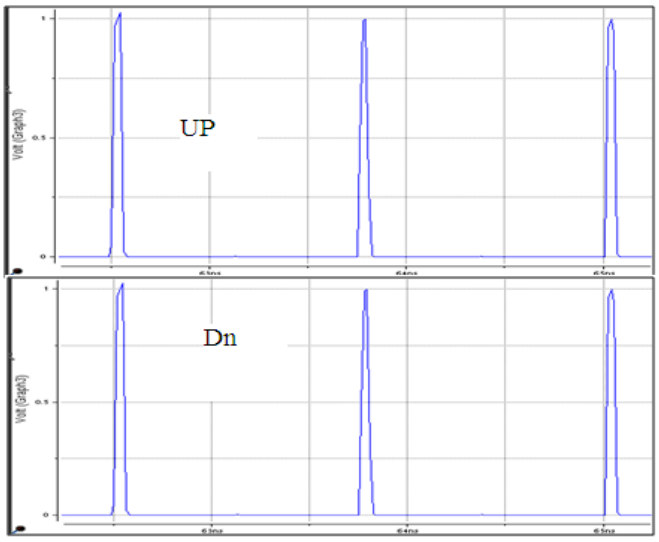

Figure 6.26: Up and Dn Signal

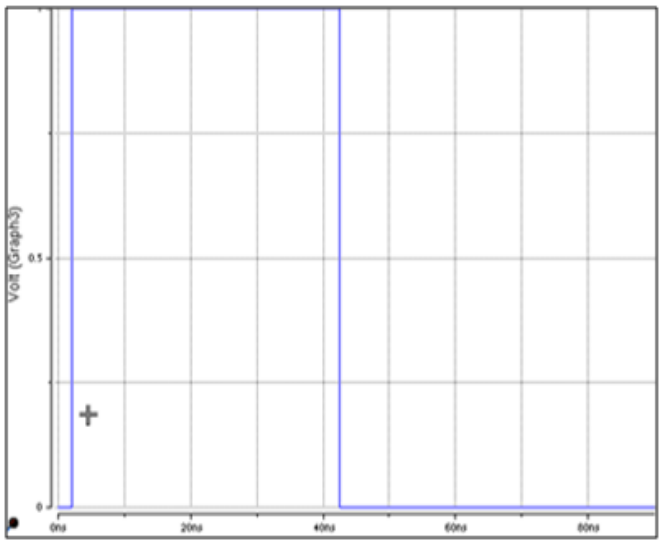

Figure 6.27: Start up Signal

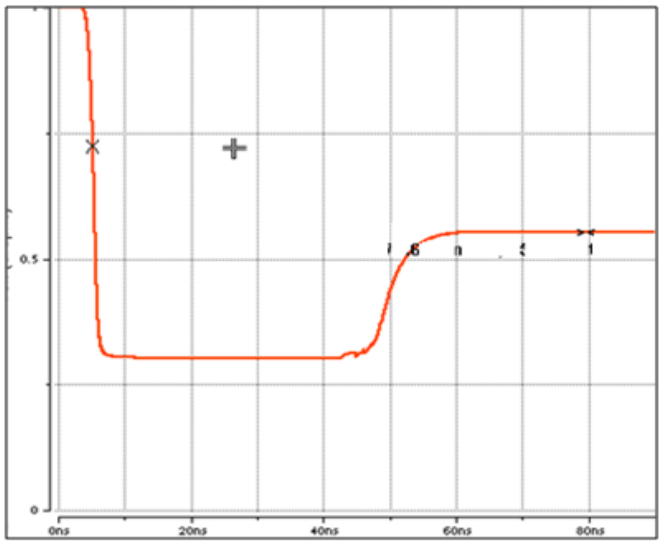

Figure 6.28: CP bias

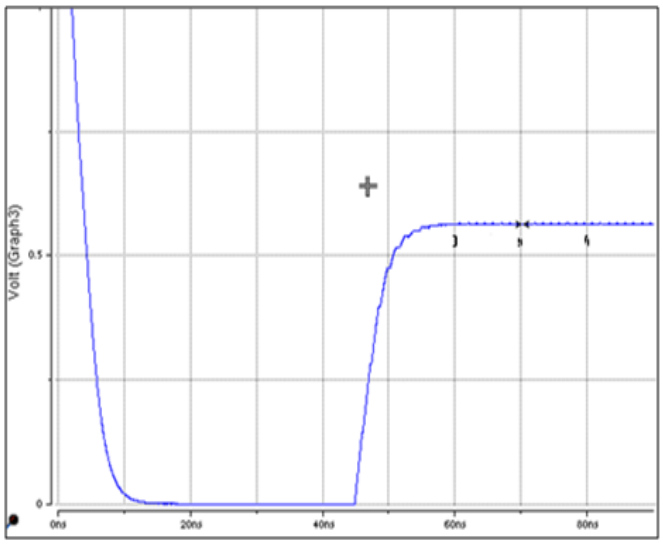

Figure 6.29: CP Out

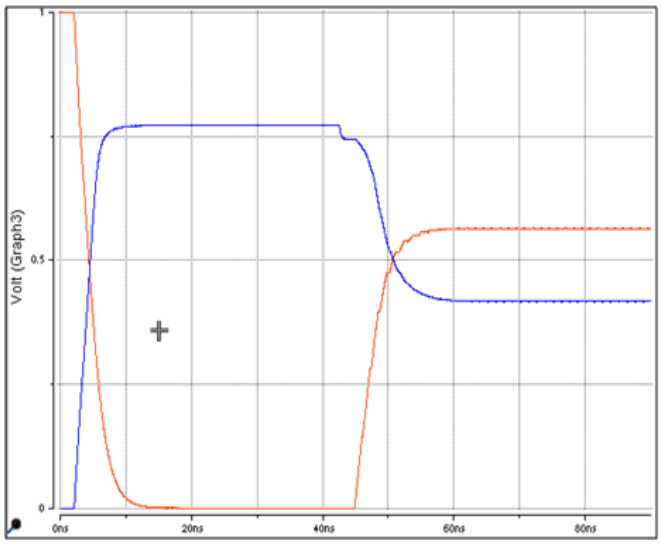

Figure 6.30: Pbias,nbias

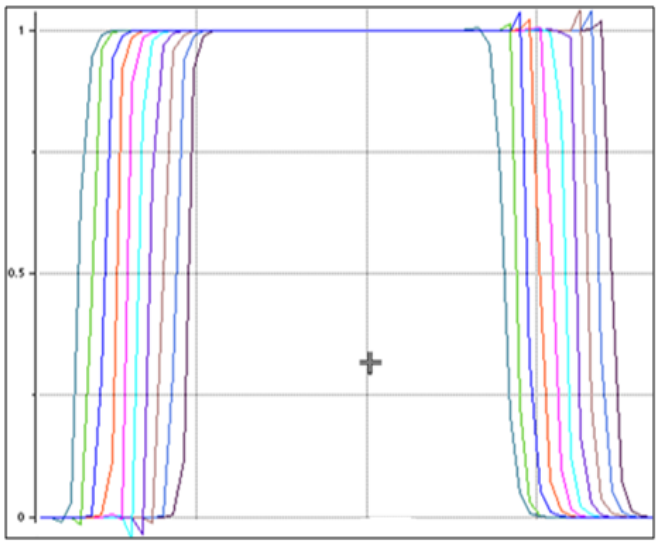

Figure 6.31: CLK0-CLK7

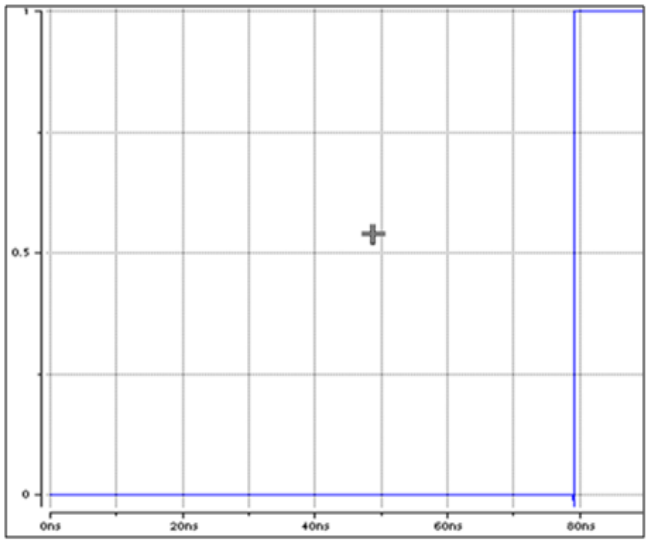

Figure 6.32: DLL Locked Signal

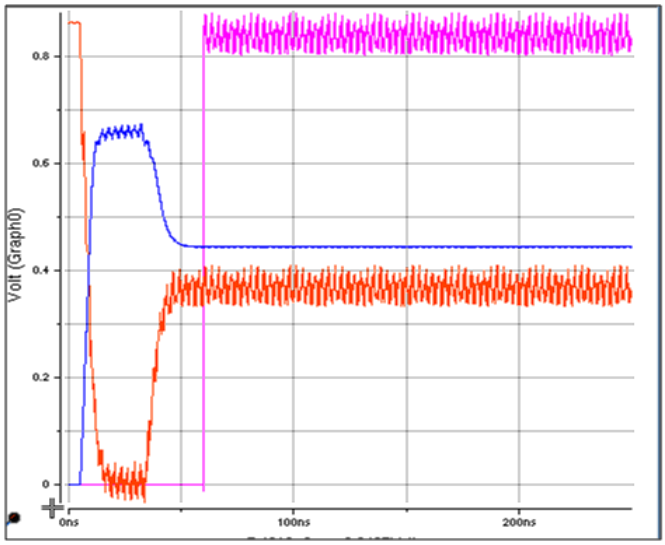

Figure 6.33: Pbias,nbias DLL Locked Signal

6.2.6 Voltage Controlled Delay Line

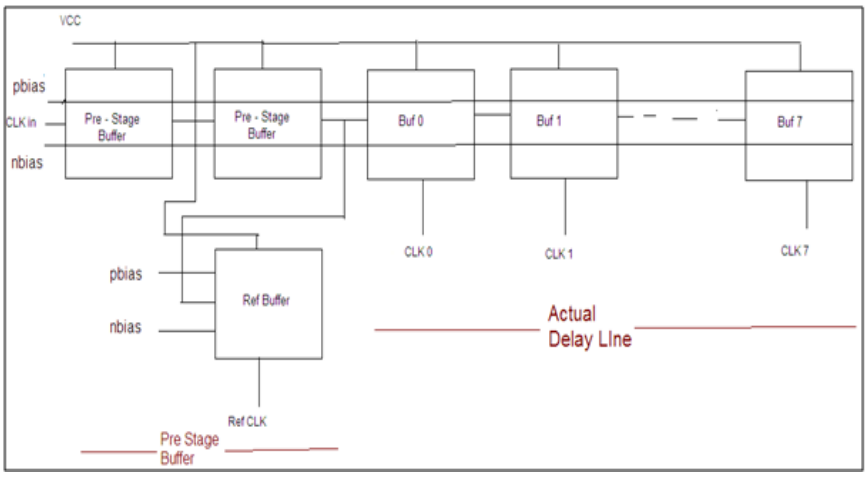

Figure 6.34: Block Diagram of VCDL

Parameters to be measured for Delay line:-

1 Input Clock

2 Rise/Fall Time

3 Duty Cycle

4 Delay

5 Jitter

6 Current

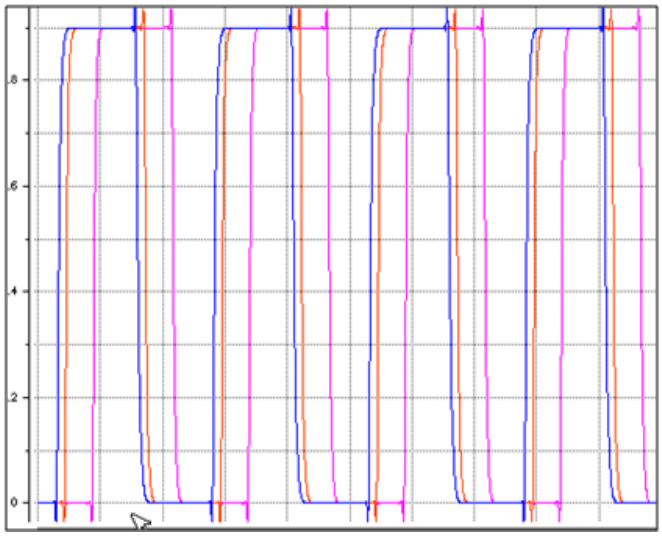

Figure 6.35: Input Clk Clk-0 Clk-7

Modified Block (After removing first stage):-

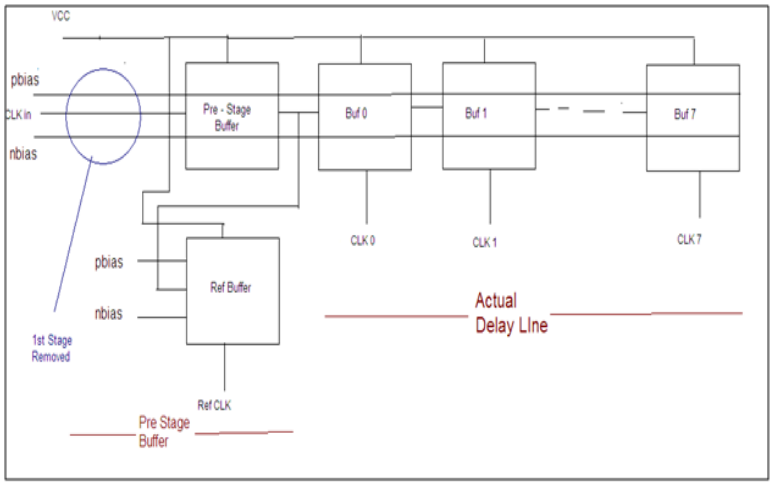

Figure 6.36: Modified Block (After removing first stage)

Comparison Of both Design:-

1 Delay

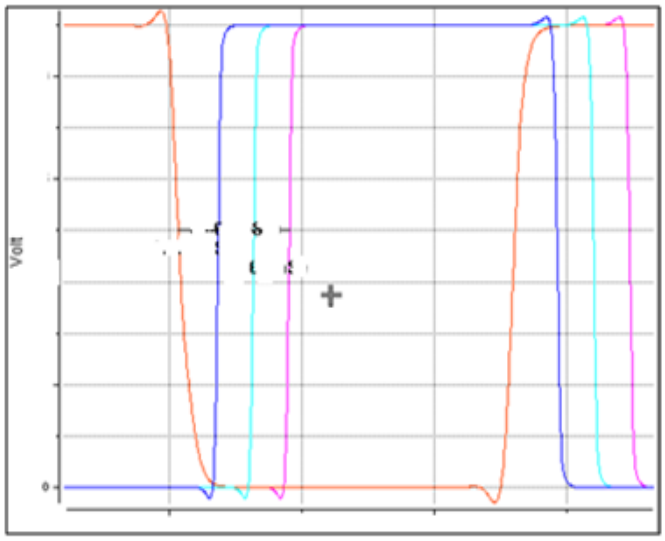

Figure 6.37: Original Block

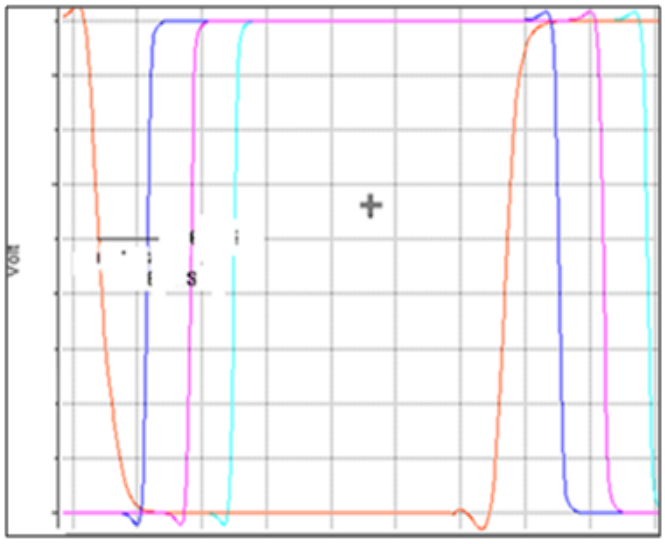

Figure 6.38: Modified Block

2 Rise/Fall Time

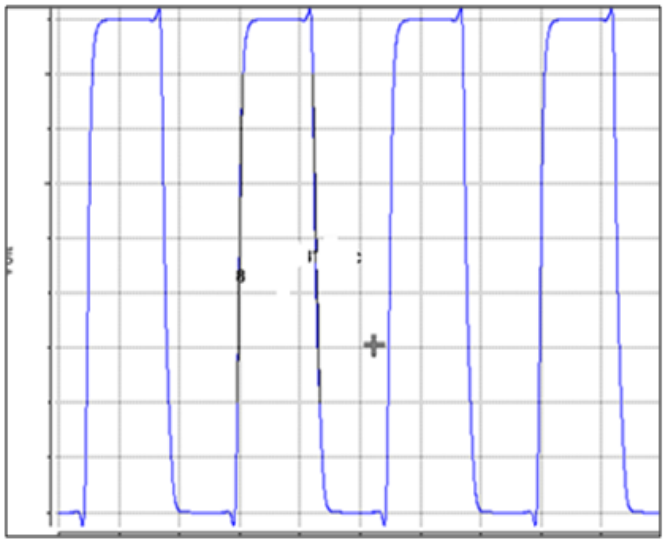

Figure 6.39: original Block

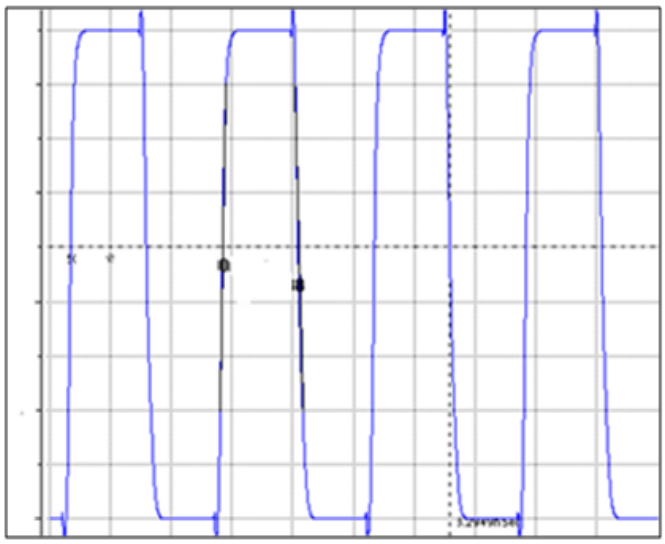

Figure 6.40: Modified Block

3 Duty Cycle

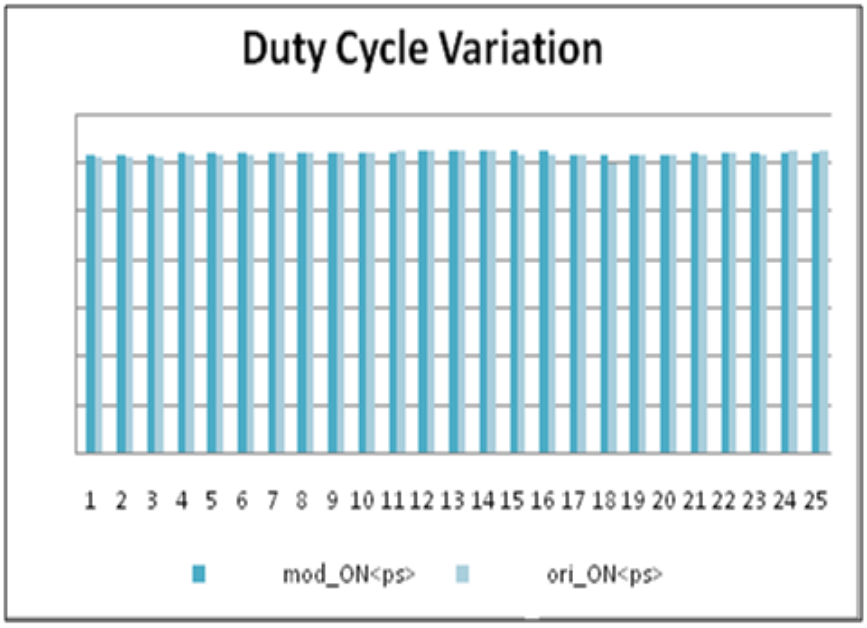

Figure 6.41: Duty Cycle Variation in both cases

Summary Table

Table 6.1: Summary Table.

Sr. No	Parameters	% Difference
1	Delay	Mostly same 0%
2	Rise /Fall Time	Mostly same 0%
3	Duty Cycle	Increase 1%
4	Current/Power	Decrease
5	Area	Decrease

Chapter 7

Summary

The Phase Detector (PD), Charge Pump (CP), and Voltage-Controlled Delay Line (VCDL) are the three most important blocks in a DLL. The PD serves the purpose of detecting the phase difference between the input reference signal and the output signal from the last stage of the VCDL. The phase difference information from the PD is provided to the CP so that the corresponding charging or discharging current can be activated to control the voltage of the loop filter. The phase resolution of the PD and the switching speed of CP directly affect the perlformance of the DLL. By using this structure, a fast switching speed and good matching between charging and discharging currents can be achieved.

A new domino-logic PFD with extended phase-detection range and no visible dead-zone is designed to operate at high frequency and low power consumption. The new PFD has the simplest form and uses only 18 MOS transistors.

The proposed charge pump allows the use of low-voltage transistors, which help obtaining fast switching times and have lower on resistance. It is, therefore, possible to use higher clock frequencies.

Chapter 8

Referances

1 "Design of Analog CMOS Integrated Circuits" - Behzad Razavi

2 "CMOS Analog Circuit Design"- Allen and Holberg,Oxford-2003

3 "CMOS analog Circuit Design, Layout and Simulation"- Jacob Baker, PHI-2005

4 "Charge pump circuit design" - Feng pan and samaddar

5 Soh Lip-Kai, Mohd- Shahiman Sulaiman, and Zubaida Yusoff " Fast-Lock Dual Charge Pump Analog DLL using Improved Phase Frequency Detector", IEEE-2007

6 Jae Hyung Noh, and Hang Geun Jeong, "Charge-Pump with a Regulated Cascode Circuit for Reducing Current Mismatch in PLLs", World Academy of Science, Engineering and Technology 31, 2007

7 Kyung-Soo Ha and Lee-Sup Kim," Charge-pump reducing current mismatch in DLLs and PLLs", IEEE-2006

8 Robert , Hou-Ming Chen, and Po-Jen Huang, "A Multiphase-Output Delay-Locked Loop With a Novel Start-Controlled Phase/Frequency Detector",IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS, VOL. 55, NO. 9, OCTOBER 2008

9 Christopher Lam and Behzad Razavi, " A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4um CMOS Technology", Member, IEEE-2000

10 Y. Moon et al, "An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance", IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 377-384, Mar. 2000

11 Shenggao Li and Mohammed Ismail, "A High performance Dynamis Logic Phase Frequncy Detector", Analog VLSI Lab, The Ohio-state University, Wireless PAN Operations, Intel Corporation

12 John G Maneatis,"Low Jitter Process-Independent DLL and PLL Based on Self-Biased Techniquies" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NO. 11, NOVEMBER 1996 1723

13 Stefanos Sidiropoulos, Dean Liu, Jaeha Kim, Guyeon Wei, Mark Horowitz , "Adaptive Bandwidth DLLs and PLls using Regulated Supply CMOS Buffers" 2000 Symposium on VLSl Circuits Digest of Technical Papers.

14 Yongsam Moon, Student Member, IEEE, Jongsang Choi, Kyeongho Lee, Member, IEEE,Deog-Kyoon Jeong, Member, IEEE, and Min-Kyu Kim, "An All-Analog Multiphase Delay-Locked Loop Usinga Replica Delay Line for Wide-Range Operation andLow-Jitter Performance" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 3, MARCH 2000,377

15 Goran Jovanovi?, Mile Stoj?ev, Dragia Krsti? "Delay Locked Loop with Linear Delay Element" IEEE 2005

16 Yong -Bin Kim,tom Chen, "A CMOS Delayed Locked Loop(DLL) for reducing Clock Skew To Under 500Ps" IEEE-1997

17 Payam Heydari, "Analysis of DLL Jitter due to Substrate noise"IEEE-2000.

Appendix A

Used Terms

- **Rise Time:-**

  Rise Time is the difference between the time when the signal crosses a low threshold to the time when the signal crosses the high threshold. It can be absolute or percent.

- **Fall Time:-**

  Fall Time is the difference between the time when the signal crosses a high threshold to the time when the signal crosses the low threshold. It can be absolute or percent.

- **Duty Cycle:-**

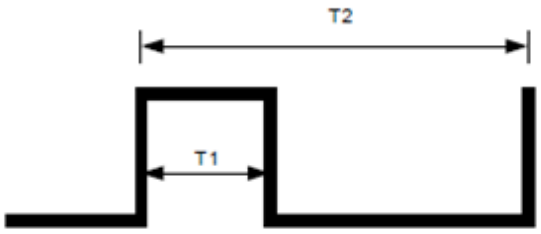

Figure A.1: Duty Cycle

For example, in an ideal pulse train (one having rectangular pulses), the duty cycle is the pulse duration divided by the pulse period.

- **Skew:-**

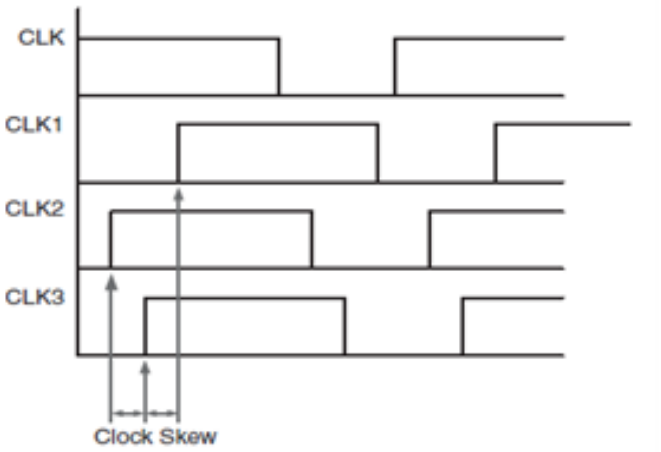

Figure A.2: Skew

- **Jitter:-**

Jitter is movement of signal edges from their ideal position in time. The period frequency displacement of the signal from its ideal location.The deviation can be in terms of amplitude, phase timing, or the width of the signal pulse.

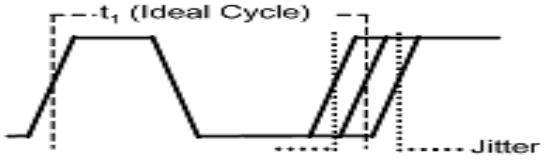

Figure A.3: Jitter

- **Lock Range:-**

  Lock range refers to the maximum and minimum delays of the VCDL, which set the range in which the delay of the VCDL can be varied. A DLL is able to achieve lock only in this range.

- **Lock Time:-**

  Lock time is defined as the time it takes for the DLL to lock to the input variations. The lock time can be optimized by decreasing the loop-capacitor or increasing the charging current and VCDL loop gain. A large charging current is required during lock acquisition when a large change in the phase of the input clock takes place to improve the lock time

- **Loop Bandwidth:-**

  Loop bandwidth defines the frequency range over which a DLL can lock to variations in the input clock. The DLL bandwidth will be one or two orders of magnitude lower that the operating frequency. It is a measure of the maximum rate of change of input period the DLL can track.

- **Dead Zone:-**

  If the propagation delay at UP and DN is large enough, it is possible that UP or DN may be pulled to low by the reset operation before it completes a positive transition. Consequently, the charge pump output voltage will keep intact at a small phase difference. This phenomenon is called "dead-zone".

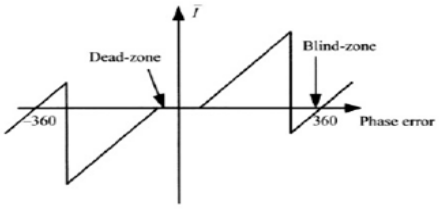

Figure A.4: Dead Zone