"MULTILEVEL INVERTER"

A Major Project Report

Submitted in Partial Fulfillment of the Requirements

for Degree of

MASTER OF TECHNOLOGY
IN
ELECTRICAL ENGINEERING

(POWER APPARATUS & SYSTEMS)

By

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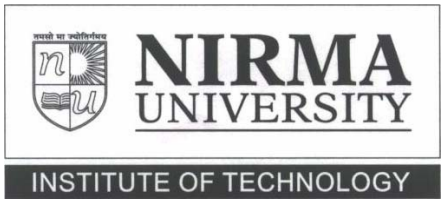

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Certificate

This is to certify that the Major Project Report entitled **"MULTILEVEL INVERTER"** submitted by **Mr. Rachit Shah (04MEE014)**, towards the partial fulfillment of the requirements for Degree of Master of Technology (Electrical Engineering) in the field of Power Apparatus & Systems of **Nirma University of Science and Technology** is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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Abstract

For high power applications, voltages and currents must be pushed up. Hence, maximum ratings of power semiconductors become a real handicap. Multilevel Inverter can overcome this limitation.

The report covers and gives an idea of different topologies available in Multilevel Inverters. Main two modulation topologies - Sinusoidal PWM and Space Vector PWM, used in Multilevel Inverter are also explained in this report.

To get the deep-through to Three-Level Diode-Clamped Inverter topology, firstly the Sinusoidal PWM topology is explained. The SPWM topology clearly explains the switching used in Three-Level Diode-clamped Inverter and its basics.

This report also provides one with a new and simple algorithm for Space-Vector PWM. This algorithm takes the advantage of symmetry in the space-vector diagram in order to reduce the switching losses of the IGBT's. The biggest problem of diode-clamped inverter of neutral point voltage unbalanced is overcome by the use of the effective space-vector algorithm. Simulation results are provided to validate the effectiveness of the algorithm, for different reference speeds.

The H-Bridge Inverter topology is also studied in deep and the simulation results for Nine-Level Inverter are also provided. The simulation result comparison shows that the H-Bridge Inverter is quit simple and advantageous in comparison with Diode-Clamped Inverter topology, because of simple switching techniques and improved quality of the output voltage and current and improved source current. The THD of the source current is 5-6% and output phase voltage THD is 8-9%. Other advantage of H-Bridge Inverter is easy commercialization and easy to increase the number of CELLS and hence voltage levels.

The simulation results are supported with the experimental results. For preparing the prototype, different PCB's are prepared. The gate pulses are generated by the use of DSP 'TMS320F2811', which are then further given to the IGBT driver board via multilevel interface board.

A single-phase 3-level prototype model for CELL is also prepared. The experimental results are also shown.

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1. INTRODUCTION

1.1 Harmonics in Electrical Systems

One of the biggest problems in power quality aspects is the harmonic contents in the electrical system. Generally, harmonics may be divided into two types:

1) Voltage harmonics, and

2) Current harmonics.

Current harmonics is usually generated by harmonics contained in voltage supply and depends on the type of load such as resistive load, capacitive load, and inductive load. Both harmonics can be generated by either the source or the load side. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas discharge lighting devices, etc. Load harmonics can cause the overheating of the magnetic cores of transformer and motors. On the other hand, source harmonics are mainly generated by power supply with non-sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives. Any periodic waveform can be shown to be the superposition of a fundamental and a set of harmonic components. By applying Fourier transformation, these components can be extracted. The frequency of each harmonic component is an integral multiple of its fundamental. The method used to determine harmonic content commonly used is Total Harmonic Distortion (THD), which is defined in terms of the amplitudes of the harmonics, Hn, at frequency $n\omega o$, where ωo is frequency of the fundamental component whose amplitude of $H1$ and n is integer. The THD is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}{}^2}}{H_1}$$

1.2 Conventional Two-Level and Three-Level Voltage Source Inverter

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three-phase ac systems. A half-bridge is the simplest topology, which is used to produce a two-level square-wave output waveform. The full-bridge topology is used to synthesize a three-level square-wave output waveform. The half-bridge and full-bridge configurations of the single-phase voltage source inverter are shown in Fig.1.2.1 and 1.2.2, respectively.

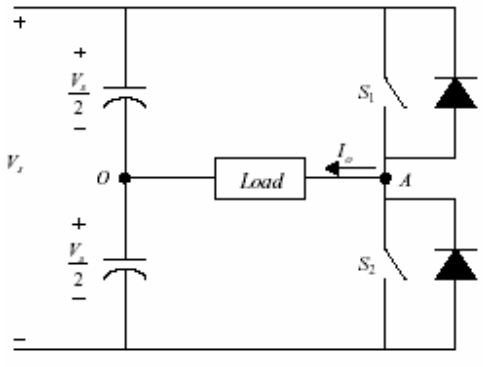


Fig. 1.2.1 : Half-bridge configuration.

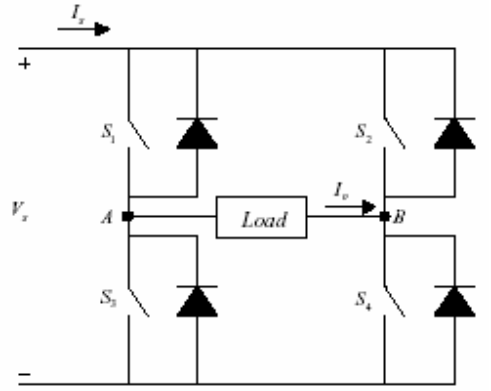


Fig. 1.2.2 : Full-bridge configuration.

Fig. 1.2.3 and 1.2.4 respectively shows the output waveform of a Half-bridge and Full-bridge configuration.

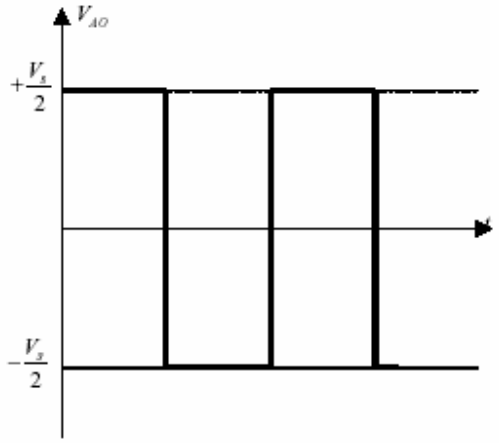


Fig. 1.2.3 : Output waveform of Half-Bridge configuration.

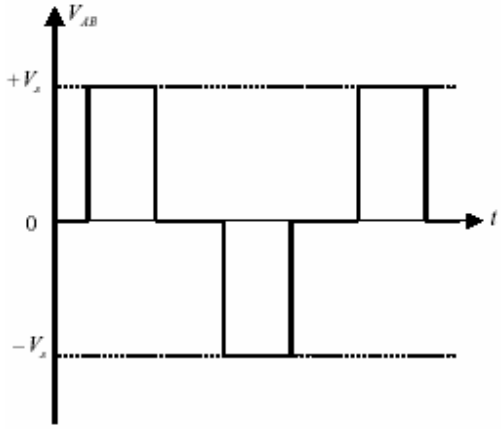


Fig. 1.2.4 : Output waveform of Full-Bridge configuration.

1.3 Multilevel Voltage Source Inverter

For high power applications, voltages and currents must be pushed up. Hence, maximum ratings of power semiconductors become a real handicap. Paralleling devices, subsystems or systems leads to higher current levels. On the other hand, given a chain of devices connected in series, achieving static and dynamic voltage sharing among switches becomes a problem. The best method for stabilizing voltages applied to the devices is by clamping those using DC voltage sources; or large capacitors, which transitorily behave as voltage sources. Multilevel topologies are based on this principle, and therefore, the voltages applied to the devices can be controlled and limited.

Advantages offered by the multilevel approach compared to two-level topology include:

► Good power quality, due to greater availability of voltage levels,

► Good electromagnetic compatibility (EMC),

► Low switching losses, as switching frequencies of the devices can be reduced,

► Filters with smaller reactive components,

► Ratings of the components used reduces.

These all benefits, together with the ability to deal with high voltage levels, confer on multilevel converters a very important role in the field of high power applications.

In 1980, early interest in multilevel power conversion technology was triggered by the work of Nabae, et al., who introduced the neutral-point-clamped (NPC) inverter topology. It was immediately realized that this new inverter had many advantages over the more conventional two-level inverter. Subsequently, in the early nineties the concept of the three-level inverter was extended further and some new multilevel topologies were proposed.

2. MULTILEVEL INVERTER TOPOLOGIES

At the present time, the majority of research and development effort seems to concentrate on the development of four classes of inverters:

1. The diode-clamped (neutral-point-clamped) multilevel inverter.
2. The flying capacitor inverter.
3. The multilevel inverter with cascaded and parallel H-bridge inverters.
4. Modified H-bridge inverters.

2.1 Diode-Clamped Multilevel Inverter

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three-level. Because of industrial developments over the past several years, the three-level inverter is now used extensively in industry applications. Although most applications are medium-voltage, a three-level inverter for 480V is also in the market.

Fig. 2.1.1 shows the topology of the three-level diode-clamped inverter. Although the structure is more complicated than the two-level inverter, the operation is straightforward. Each phase node (*a*, *b* or *c*) can be connected to any node in the capacitor bank (d_0, d_1 or d_2). Connection of the *a*-phase to junctions d_0 and d_2 can be accomplished by switching transistors T_{a1} and T_{a2} both OFF or both ON respectively. These states are the same as the two-level inverter yielding a line-to-ground voltage of zero or the dc voltage. Connection to the junction d_1 is accomplished by gating T_{a1} OFF and T_{a2} ON. In this representation, the labels T_{a1} and T_{a2} are used to identify the transistors as well as the transistor logic (1=ON and 0=OFF). Since the transistors are always switched in pairs, the complement are labeled $\overline{T}_{a1}$ and $\overline{T}_{a2}$ accordingly. In a practical implementation, some dead time is

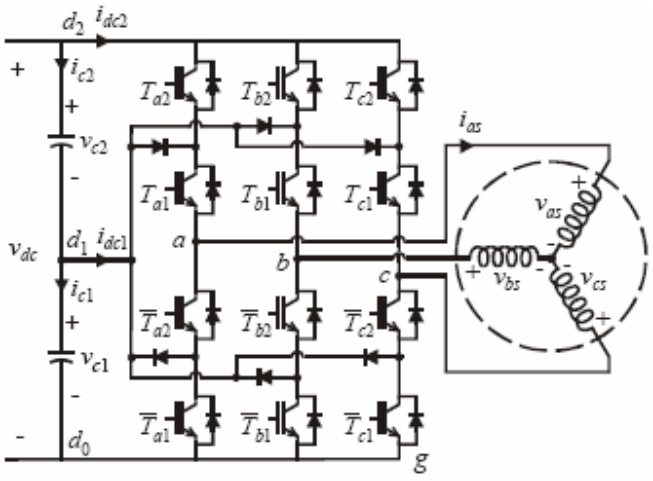


Fig. 2.1.1 : Three-level diode-clamped inverter topology.

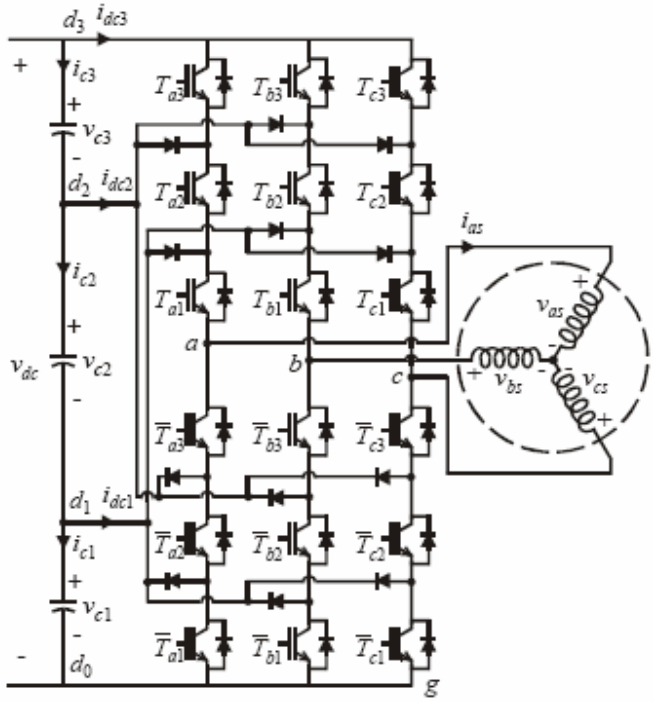


Fig. 2.1.2 : Four-level diode-clamped inverter topology.

inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition. From Fig. 2.1.1, it can be seen that, with this switching state, the *a*-phase current i_{as} will flow into the junction through diode D_{a1} if it is negative or out of

the junction through diode D_{a2} if the current is positive. According to this description, the inverter relationships for the *a*-phase are presented in Table -2.1.1.

Table – 2.1.1. Three-level inverter relationships.

S_a	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}
0	0	0	0	0	0
1	0	1	v_{c1}	i_{as}	0
2	1	1	$v_{c1} + v_{c2}$	0	i_{as}

The dc currents i_{adc1} and i_{adc2} are the *a*-phase components to the junction currents i_{dc1} and i_{dc2} in Fig. 2.1.1 respectively.

Extending the diode-clamped concept to four levels results in the topology shown in Fig. 2.1.2. A pair of diodes is added in each phase for each of the two junctions. The operation is similar to the three-level inverter with the relationships described in Table -2.1.2.

Table – 2.1.2. Four-level inverter relationships.

S_a	T_{a3}	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}	i_{adc3}
0	0	0	0	0	0	0	0
1	0	0	1	v_{c1}	i_{as}	0	0
2	0	1	1	$v_{c1} + v_{c2}$	0	i_{as}	0
3	1	1	1	$v_{c1} + v_{c2} + v_{c3}$	0	0	i_{as}

The **advantages** of diode-clamped multilevel inverter are:

- Voltages across the switches are only half of the dc-link voltage.
- The first group of voltage harmonics is centered around twice the switching frequency.
- This topology can be generalized, and the principles used in the basic three-level topology can be extended for use in topologies with any number of levels.

However, practical experience with this topology revealed several **technical difficulties** that complicate its application for-high power inverters. These are as follows:

- This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress.
- For topologies with more than three levels the clamping diodes are subject to increased voltage stress equal to $V_{pn}.(n-1)/n$. Therefore, series connection of diodes might be required. This complicates the design and raises reliability and cost concerns.
- The issue of maintaining the charge balance of the capacitors is still an open issue for NPC topologies with more than three-levels. Although the three-level NPC topology works well with high power factor loads, NPC topologies with more than three levels are mostly used for Static VAR Compensation circuits.

2.2 Flying Capacitor Multilevel Inverter

Another fundamental multilevel topology, the flying capacitor, involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase which can be used to balance the flying capacitors so that only one dc source is needed.

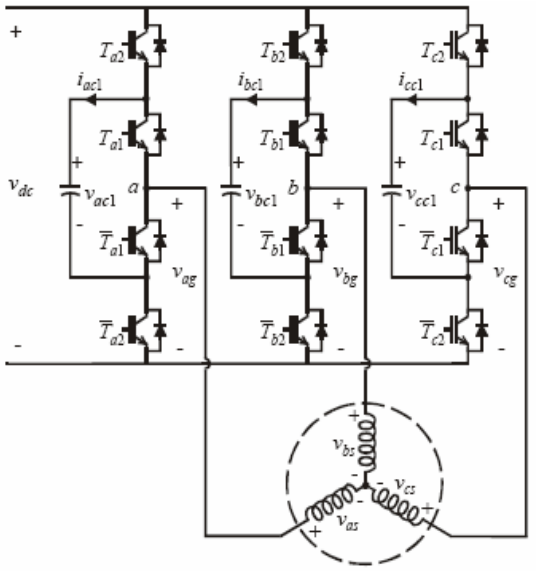


Fig. 2.2.1 : Three-level flying capacitor topology.

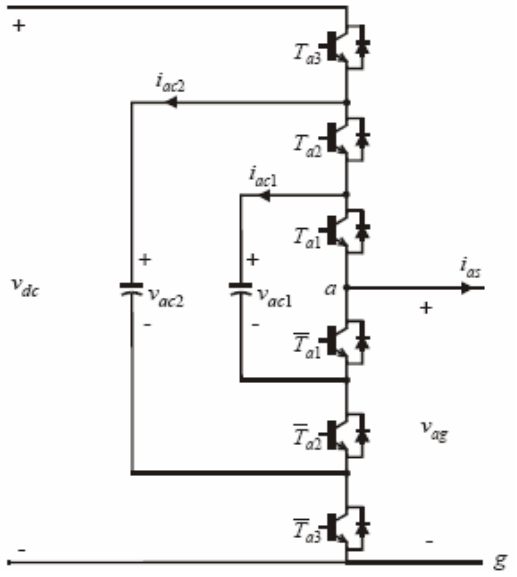


Fig. 2.2.2 : Four-level flying capacitor topology.

Fig. 2.2.1 shows the three-level flying capacitor inverter. The general concept of operation is that each flying capacitor is charged to one-half of the dc voltage and can be connected in series with the phase to add or subtract this voltage. Table -2.2.1 shows the relationships for the *a*-phase.

In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states which make up the level $S_a = 1$. Considering the direction of the *a*-phase flying capacitor current i_{ac1} for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. In

Table-2.2.1, the current i_{adc} is the *a*-phase component of the dc current. The total dc current can be calculated by summing the components for all phases.

Table – 2.2.1. Three-level flying capacitor relationships.

S_a	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{adc}
0	0	0	0	0	0
1	0	1	v_{ac1}	$-i_{as}$	0
	1	0	$v_{dc} - v_{ac1}$	i_{as}	i_{as}
2	1	1	v_{dc}	0	i_{as}

Fig.2.2.2 shows the structure for the *a*-phase of the four-level flying capacitor inverter. For this inverter, the capacitors v_{ac1} and v_{ac2} are ideally charged to one-third and two-thirds of the dc voltage respectively. The four voltage levels are obtained by the relationships shown in Table -2.2.2.

Table – 2.2.2. Four-level flying capacitor relationships.

S_a	T_{a2}	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{ac2}	i_{adc}
0	0	0	0	0	0	0	0
1	0	0	1	v_{ac1}	$-i_{as}$	0	0
	0	1	0	$v_{ac2} - v_{ac1}$	i_{as}	$-i_{as}$	0
	1	0	0	$v_{dc} - v_{ac2}$	0	i_{as}	i_{as}
2	0	1	1	v_{ac2}	0	$-i_{as}$	0
	1	1	0	$v_{dc} - v_{ac1}$	i_{as}	0	i_{as}
	1	0	1	$v_{dc} - v_{ac2+} v_{ac1}$	$-i_{as}$	i_{as}	i_{as}
3	1	1	1	v_d	0	0	i_{as}

The **advantages** of Flying Capacitor topology are :

- This topology naturally limits the dV/dt stress across the devices.
- Introduces additional switching states that can be used to help maintain the charge balance in the capacitors.

At the present time it seems that this topology has few **disadvantages**.

- The dc-link capacitor charge controller adds complexity to the control of the whole circuit.
- The flying capacitor topology might require more capacitance than the equivalent diode clamped topology. In addition, it is obvious that rather large RMS currents will flow through these capacitors.

2.3 H-Bridge Inverters

2.3.1 Cascaded H-Bridge Inverters

The series H-bridge inverter appeared in 1975, and several patents have been obtained for this topology. Since this topology consist of series power conversion cells, the voltage and power level may be easily scaled. One of the earlier applications of this topology was for plasma stabilization; it was then extended for three-phase applications.

A two-cell series H-bridge inverter is shown in Fig. 2.3.1. The inverter consist of familiar H-bridge (sometimes referred to as full-bridge) cells in a cascade connection. Since each cell can provide three voltage levels (zero, positive dc voltage, and negative dc voltage), the cells are themselves multilevel inverters. Taking the *a*-phase for example, the relationship for a particular cell can be expressed as in Table -2.3.1.

Table – 2.3.1. H-bridge cell relationships.

S_{aHi}	T_{aLi}	T_{aRi}	v_{agi}	i_{adci}
-1	0	1	$-v_{adci}$	$-i_{as}$
0	0	0	0	0
	1	1	0	0
1	1	0	v_{adci}	i_{as}

* Where i = No. of Cell. *i.e.* i^{th} Cell.

2.3.2 Parallel H-Bridge Inverter Topology

Since nearly all multilevel inverters involve effective series connection of transistor devices, parallel connection of inverter poles through inter-phase reactors is sometimes overlooked or not recognized as a multilevel solution. However, the multilevel features and redundancy were noted by researchers some time ago. One advantage of parallel connection is that the devices share current and this topology is good for high current loads.

Fig.2.3.2 shows a three-phase three-level inverter made from parallel two-level poles. The inter-phase reactor is similar to a typical transformer with the exception that an air-gap exists in the core to ensure linearity and the windings are such that the resistance and leakage inductances are small. With these assumptions, the reactor will have equal

voltages on each half meaning that the line-to-ground voltage is the average of that of each of the two-level poles. Then the general relationships for the *a*-phase can be listed as in Table -2.3.2.

Table – 2.3.2. Parallel inverter relationships.

S_a	T_{aL}	T_{aR}	v_{ag}	i_{adc}
0	0	1	0	0
1	0	1	$v_{dc} / 2$	i_{asR}
	1	0	$v_{dc} / 2$	i_{asL}
2	1	1	v_{dc}	i_{as}

A primary **advantage** of H-bridge topology is that it provides the flexibility to increase the number of levels without introducing complexity into the power stage. Also, this topology requires the same number of primary switches as the diode-clamped topology, but does not require the clamping diode.

The H-bridge **configuration uses** multiple dedicated dc-busses and often a complicated and expensive line transformer, which makes this a rather expensive solution. However, the cells can be supplied by phase-shifted transformers in medium-voltage systems in order to provide high power quality at the utility connection.

2.3.3 Modified H-Bridge Inverter Topology

The conventional H-bridge topology for n-cells connected in series gives 2n+1 output waveform levels. While in case of modified H-bridge topology for n cells connected in series we get 2^{n+1}-1 level of output waveform. In case of conventional topology the DC voltage at each cell are equal and in case of modified topology the DC voltage at each cell increases in binary pattern *i.e.,* in 2^{n-1} format. For example, 2Vdc, 4Vdc, 8Vdc …. 2^{n-1}.

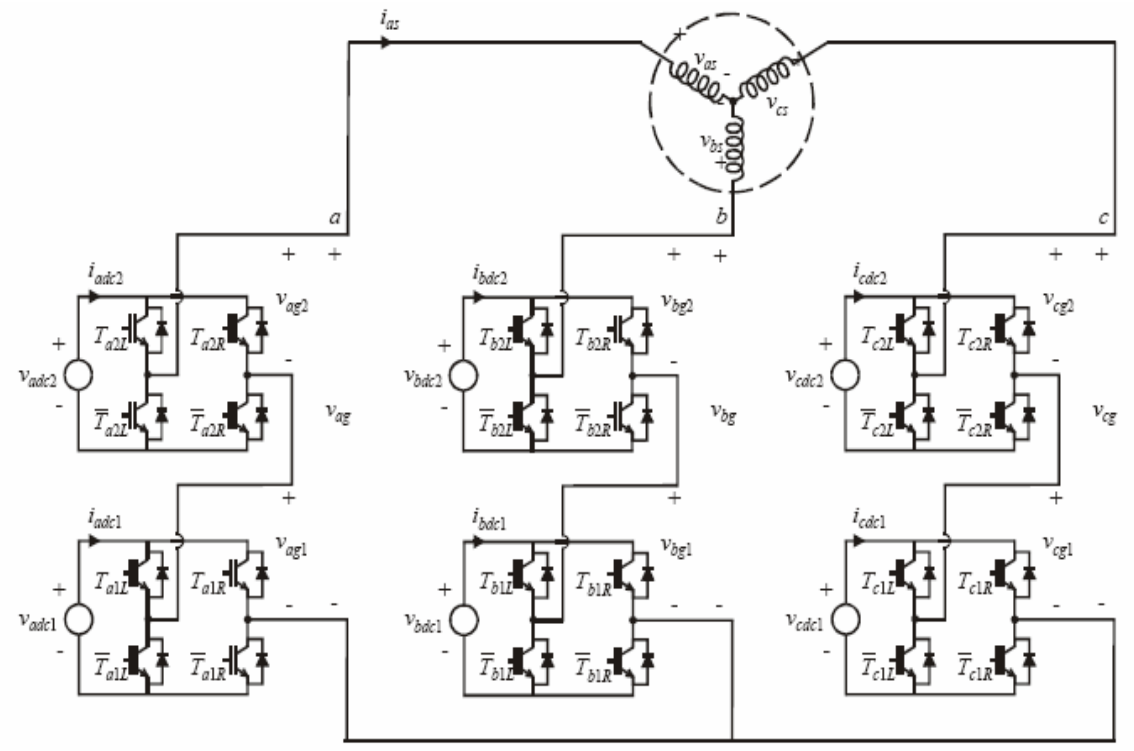


Fig. 2.3.1 : The Two-cell Cascaded H-bridge drive.

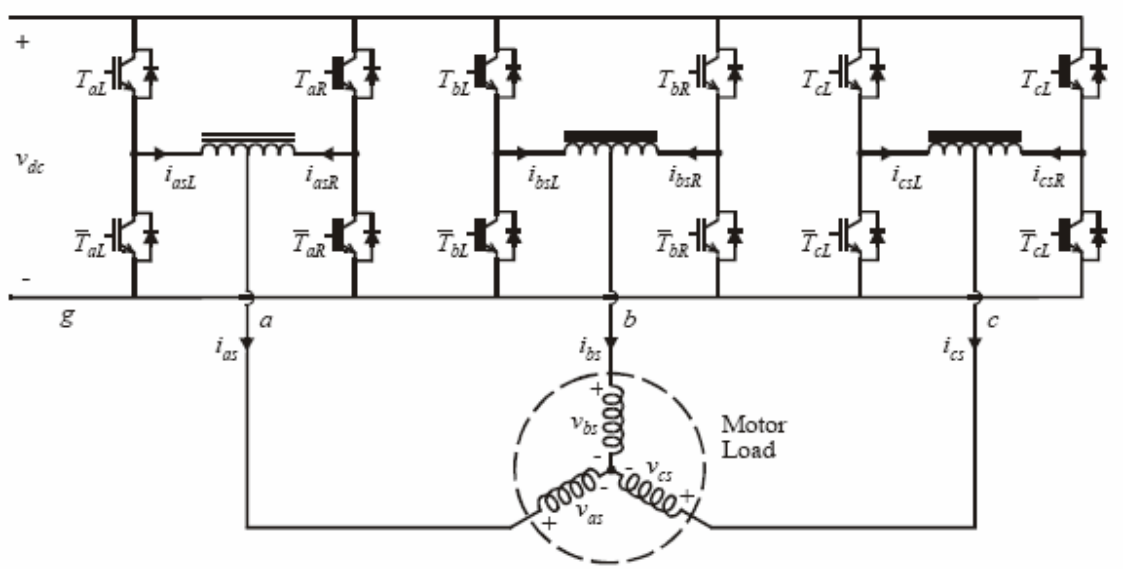


Fig. 2.3.2 : Parallel phase inverter.

Table – 2.4. Comparison of Topologies For Multilevel Inverters.

Topology	Level	a	b	c	d	e
Diode Clamped	n	$6(n-1)$	$6(n-1)$	$n-1$	$n-1$	$2n-1$
Flying Capacitor	n	$6(n-1)$	0	$3n-5$	$(n-1)^2+3\sum_{i=1}^{n=2} i^2$	$2n-1$
Conventional H-bridge	n	$6(n-1)$	0	(Even) $3n/2-1.5$ (Odd) $3n/2-2$	(Even) $3n/2-1.5$ (Odd) $3n/2-2$	$2n-1$
Modified H-bridge	$m=2^n-1$	$12(n-1)$	0	(Odd) $3n/2+1.5$ (Even) $3n/2+3$	(Odd) $3n/2+1.5$ (Even) $3n/2+3$	$2m-1$

a : switches (with free-wheeling diodes).

b : independent diodes (with different reverse voltages possible).

c : capacitors (with different voltages possible).

d : real number of capacitors (series and parallel connections for the same voltage distribution and capacitance).

e : line-to-line output voltage levels.

3. MODULATION TOPOLOGIES FOR MULTILEVEL INVERTER

It is generally accepted that the performance of an inverter, with any switching strategies, can be related to the harmonic contents of its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms. In multilevel technology, the well-known modulation topologies are as follows:

1) Sinusoidal Pulse Width Modulation (SPWM).

2) Space Vector Pulse Width Modulation (SVPWM).

3.1 Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. These methods have been extensively studied and are among the most popular in industrial applications. These methods involve a comparison of the reference signal with a triangular carrier waveform and the detection of cross-over instances to determine switching events. The variations of these methods are essentially in the polarity and shape of the carrier waveforms.

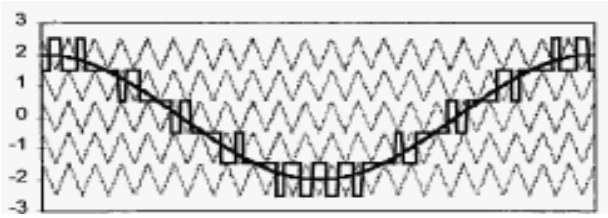


Fig. 3.1.1 : 6 – Level Inverter SPWM

For an n-level inverter, n-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference, or modulation, waveform has peak-to-peak amplitude A_m and frequency f_m, and it is centered in the middle of the carrier set.

The three cases of triangular wave disposition are :

1) Alternative phase opposition disposition, where each carrier band is shifted by 180^o from the adjacent bands,
2) Phase opposition disposition, where the carriers above the zero reference are in phase, but shifted by 180^o from those carriers below the zero reference and
3) In-phase disposition, where all the carriers are in phase.

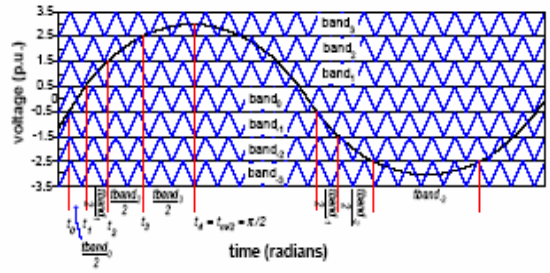


Fig. 3.1.2 : n = Even

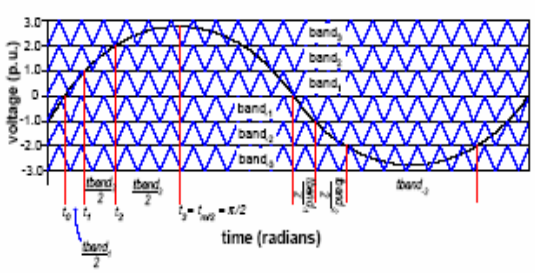


Fig. 3.1.3 : n = odd

Fig. 3.1.2 and 3.1.3 shows the SPWM for number of output levels even and odd respectively.

Variable frequency carrier band is another topology used in multilevel sinusoidal PWM. In this topology, as shown in Fig. 3.1.4, the frequency of the carrier band decreases as we go from zero-level to upper bands and lower bands.

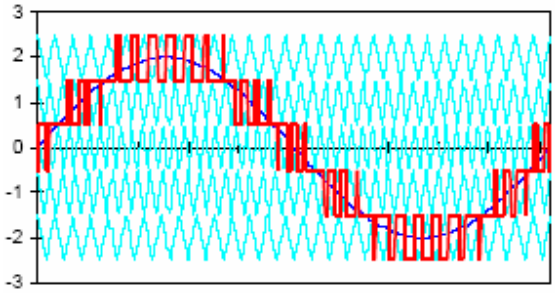


Fig. 3.1.4 Variable Frequency Carrier Band.

3.2 Space Vector Pulse Width Modulation (SVPWM)

The space-vector PWM method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications still known. Because of its superior performance characteristics, it has been finding widespread application in recent years.

It can be shown that the space vector $\overline{V}$ with magnitude V_m rotates in a circular orbit at angular velocity ω, where the direction of rotation depends on the phase sequence of the voltages. With the sinusoidal three-phase command voltages, composite PWM fabrication at the inverter output should be such that the average voltages follow these command voltages with a minimum amount of harmonic distortion.

The space vector modulation uses averaging technique, as it uses the voltage vector such that their average value is equal to the instantaneous output voltage required. For averaging the value, the first step is identifying the nearest three voltage vectors and using the redundancy. After identification the next step is to estimate the on-time period for each voltage vector. The final step is to determine the sequence of switching of each voltage vector. The SVM can be implemented by the help of fast DSP's.

3.2.1 Space Vector PWM For a Three-Level Diode Clamped Inverter

In case of a two-level inverter there are total of 8-vectors (6-non zero vectors and 2-zero vectors). The number of vectors for a n-level inverter is given by

$$\text{No. of space vector} = n^3$$

Hence in case of a three-level inverter there are 27 vectors and among them, there are 3-zero vectors and 24-non zero vectors. Similarly, five-level inverter shall have 125 vectors. Each switching state, or combination of phase-leg switches, produces a defined set of three-phase voltages, which can be represented in a hexagon form as shown in figure 3.2.1.1.

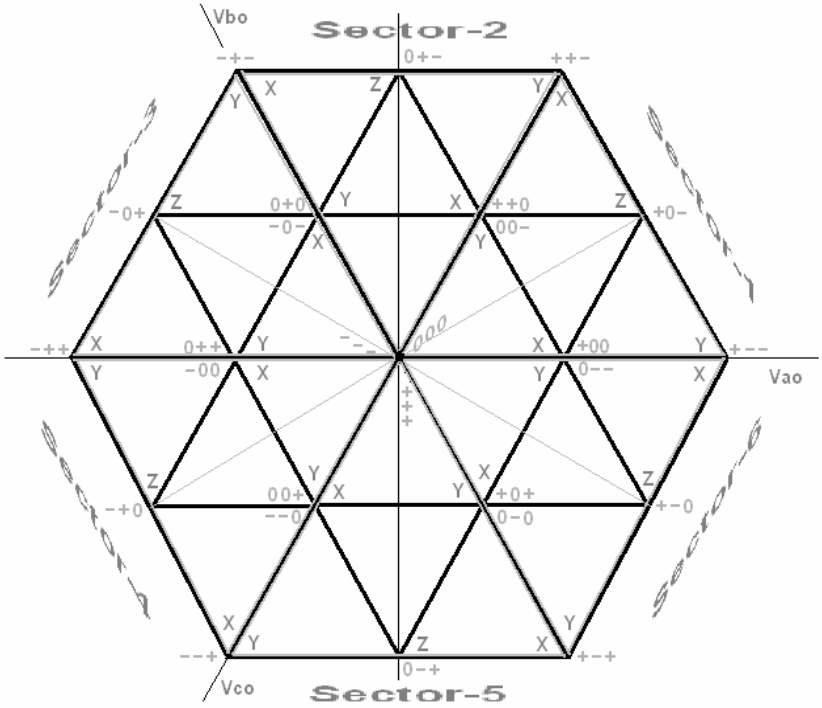


Fig. 3.2.1.1 : Space - Vector Diagram for Three-Level Inverter.

Suitable vectors from the space-vector (SV) diagram should be chosen for each modulation cycle in order to generate the reference vector (m_i). The vectors nearest to m_i are the most appropriate selections in terms of their ability to minimize the switching frequencies of the power devices, improve the quality of the output voltage spectra, and the electromagnetic interference (EMI).

In figure 3.2.1.1, the SV diagram of the three-level inverter is divided into six sextants, and each sextant is then divided into four triangular regions in order to show the vectors nearest to the reference.

Figure 3.2.1.2 represents the simplified model of the three-level diode clamped inverter, where Vc1 and Vc2 are the voltages across the lower and the upper capacitors voltages respectively.

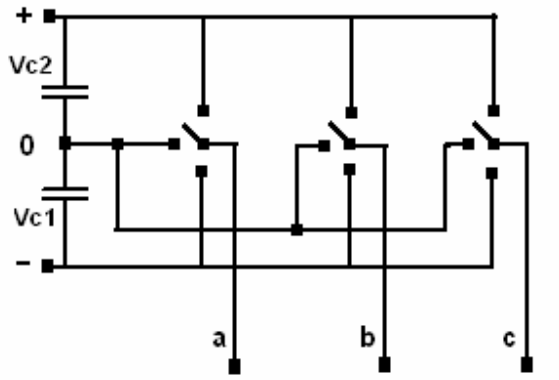


Fig. 3.1.1.2 : Simplified Model of Three-Level Diode Clamped Inverter.

Each leg has the following three-states, which are utilized to generate the required voltage :

State '+' : Upper switches ON.

State '0' : Auxiliary switches ON.

State '-' : Lower switches ON.

Four groups of vectors can be distinguished in this SV diagram, as described in the following:

(1) The "large vectors" ('+--', '++-', '-+-', '-++', '--+' and '+-+') assign the output voltages of the inverter to either the highest or the lowest DC voltages levels. As they do not connect any output to the NP, they do not affect the voltage balance of the capacitors. These vectors can generate the highest AC voltage amplitudes because they have the greatest lengths. In fact, these six vectors are equivalent to the active ones of the two-level inverter.

(2) The "medium vectors" ('+0-', '0+-', '-+0', '-0+', '0-+' and '+-0') connect each output to a different DC-link voltage level. Under balanced conditions, their tip end in the middle of the segments that join two consecutive large vectors. The

length of the medium vectors defines the maximum amplitude of the reference vector for linear modulation and steady-state conditions, which is $\sqrt{3}/2$ the length of the large vectors. Since one output is always connected to the NP, the corresponding output current will define the NP current. This connection produces voltage imbalances in the capacitors, and these must be compensated.

(3) The "short vectors" ('0--/+00', '00-/++0', '-0-/0+0', '-00/0++', '--0/00+' and '0-0/+0+') connect the AC outputs to two consecutive DC-link voltage levels. Their length is half the length of the large vectors. They are double vectors, which means that two states of the converter can generate the same voltage vector. As they affect the NP current in opposite ways, proper utilization of these vectors will help the NP voltage to achieve balance.

(4) The "zero vectors" ('---', '000' and '+++') are in the origin of the diagram. They connect all of the outputs of the converter to the same DC-link voltage level, and therefore, they do not produce any current in the DC side.

3.2.2 Simplified Calculation of Duty Cycles

Taking into account the symmetry of all the sextants, it is interesting to reflect the reference vector into the first sextant in order to reduce the number of relevant regions. Also, the amplitude of the reference vector must be normalized to fit into a diagram in which the triangular regions have unity lengths.

The theoretical maximum length of the normalized reference vector (m_i) is the two-unity value. However, in steady-state conditions, its length is limited to $\sqrt{3}$ due to the fact that longer lengths of this vector will be outside of the vector-diagram hexagon (figure 3.2.2.1), and thus cannot be generated by modulation. Over modulation is produced if the normalized reference vector assumes lengths longer than $\sqrt{3}$ for some positions of this vector, but it can never be outside of the hexagon.

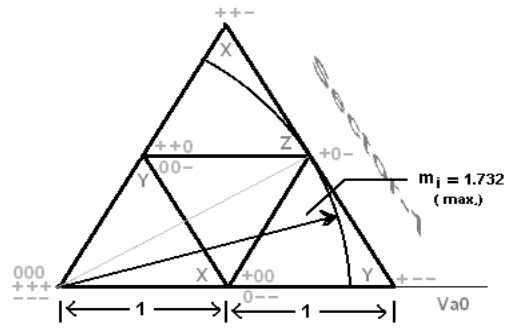


Fig. 3.2.2.1 : Max. length of the normalized reference vector in steady-state conditions.

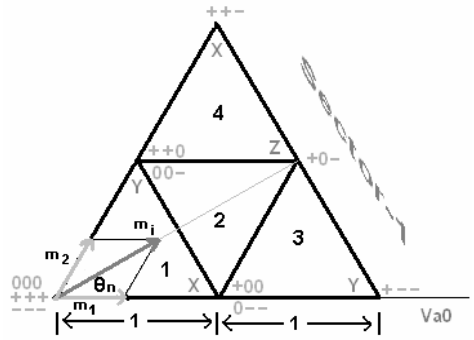


Fig. 3.2.2.2 : Projections of the normalized reference vector in the first sextant.

In figure 3.2.2.2, the normalized reference vector is decomposed into the axes located at zero and sixty degrees, obtaining projections m_1 and m_2, respectively.

The lengths of the new vectors are determined as follows :

$$m_1 = \left(\sqrt{3}\right) * \left[\cos\theta_n - \frac{\sin\theta_n}{\sqrt{3}}\right] \quad \text{and} \quad m_2 = 2 * \sqrt{3} * \frac{\sin\theta_n}{\sqrt{3}}$$

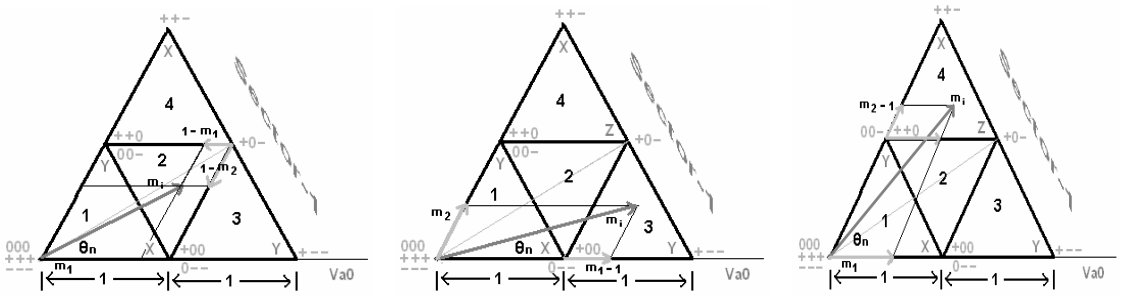
In general, these values are the direct duty ratios of the vectors, as in the following :

$d_{0--/+00} = m_1$,

$d_{00-/++0} = m_2$ and

$d_{+++/000/---} = 1 - m_1 - m_2$.

The cases for which the normalized reference vector is located in Regions 2, 3 and 4 are shown in figure 3.2.2.3-(a,b,c).



(a.) Region-2. (b.)Region-3. (c.) Region-4.

Fig. 3.2.2.3 : Projections for Region – 2, 3 and 4.

Table-3.2.1 summarizes the information needed to ascertain the region where the reference vector lies and the duty cycles of the nearest vectors in the first sextant.

Table-3.2.1: Summary of information for the SVPWM.

Case	Region	Duty Cycles
$m_1 \le 1$ $m_2 \le 1$ $m_1 + m_2 \le 1$	**1**	$d_{0--/+00} = m_1$ $d_{00-/++0} = m_2$ $d_{+++/000/---} = 1 - m_1 - m_2$
$m_1 \le 1$ $m_2 \le 1$ $m_1 + m_2 > 1$	**2**	$d_{0--/+00} = 1 - m_2$ $d_{00-/++0} = 1 - m_1$ $d_{+0-} = m_1 + m_2 - 1$
$m_1 > 1$	**3**	$d_{+--} = m_1 - 1$ $d_{+0-} = m_2$ $d_{0--/+00} = 2 - m_1 - m_2$
$m_2 > 1$	**4**	$d_{+0-} = m_1$ $d_{++-} = m_2 - 1$ $d_{00-/++0} = 2 - m_1 - m_2$

For all cases, it is assumed that the sum of m_1 and m_2 is not greater than 2; otherwise, the reference vector would be outside of the hexagon, and thus could not be reproduced by modulation.

3.2.3 Symmetric Modulation

In this method the nearest vectors in the given sextant are used for getting the required output voltage. The vectors must be selected such that the DC-link capacitors voltages are balanced. The NP current must be positive in order to discharge the lower capacitor, and must be negative to charge it. For example, vector '0--' will discharge the lower capacitor ($i_1 = i_a > 0$), and vector '+00' will charge it ($i_1 = i_b + i_c = -i_a < 0$).

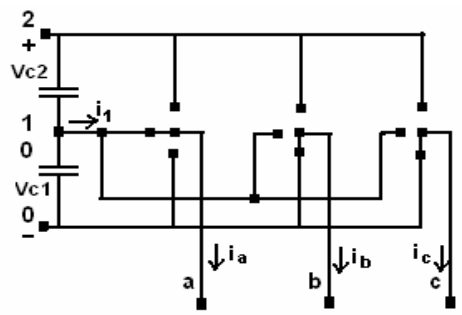


Fig. 3.2.3.1 : State Vector is '0--'.

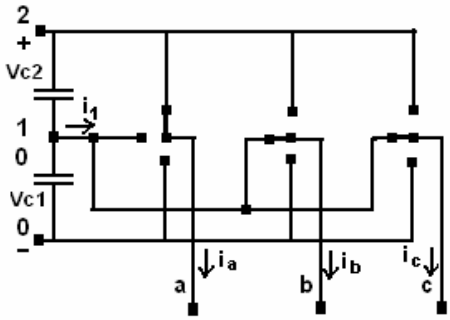


Fig. 3.2.3.2 : State Vector is '+00'.

The switching sequence used in first sector and its different regions is as shown in Table-3.2.2.

Table-3.2.2: Sequence of switching in Sector-1.

Sector		Region - 1	Region - 2	Region - 3	Region - 4
1	V_a	- 0 0 0 + + +	0 + + +	0 0 + + +	0 + + +
	V_b	- - 0 0 0 + +	- - 0 0	- 0 0 0 +	0 0 + +
	V_c	- - - 0 0 0 +	- - - 0	- - - 0 0	- - - 0

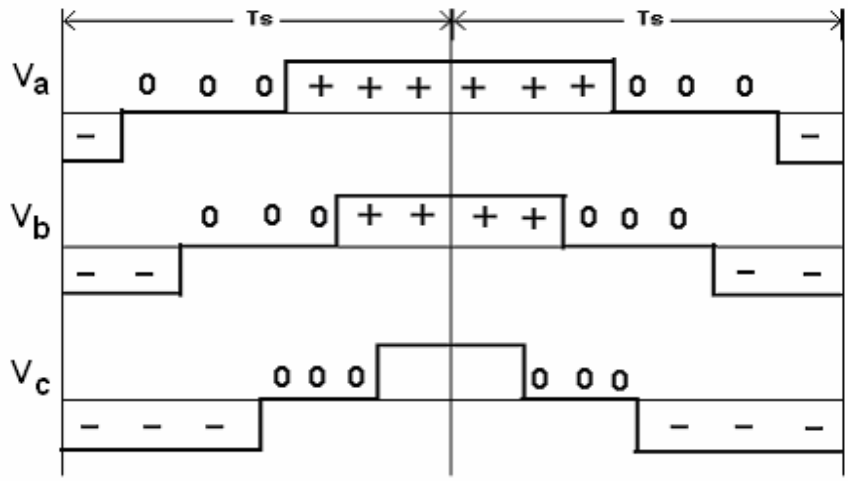


Fig. 3.2.2.3 : Waveforms showing sequence of switching in Sector-1 & Region-1.

4. SIMULATION MODEL OF THREE-LEVEL DIODE CLAMPED INVERTER

4.1 Sinusoidal PWM With Two DC Source

The simulation of the proposed scheme is done by the help of the PSIM v 6.0 Simulation package.

Figure – 4.1 shows the model of a Three-Level Diode-Clamped Inverter with DC sources, in PSIM v 6.0. For initial understanding of the topology proposed, two DC sources of 80 Volts and Resistive and Inductive load with value 10 ohm and 0.03 Henry respectively are used. Twelve IGBT's (with anti-parallel diodes) are used as the switching devices.

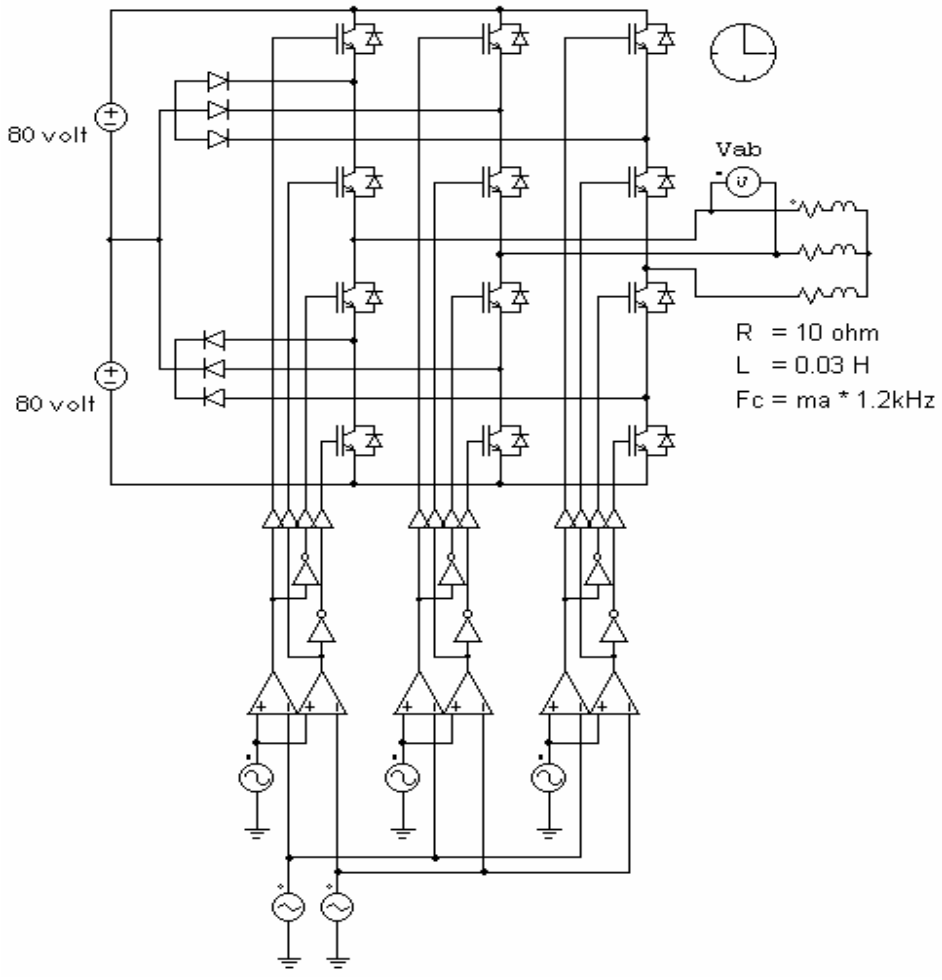


Fig. 4.1 : Three-Level Diode-Clamped Inverter With Sinusoidal PWM With Two DC Source.

4.1.1 Simulation Results For Triangular Waves With Phase-Disposition

In this case the carrier triangular waves (upper wave and lower wave) are phase disposed by 180^{o}. The load used over here is resistive load of value R = 10 ohms. The simulation is done over here is with modulation index $m_a = 1$, $m_a = 0.8$ and $m_a = 0.4$. The frequency of carrier waves used is $Fc = m_a * 1.2$ kHz. The figures below shows the output phase voltage V_{ab}, phase voltage V_{an} and the fast fourier transform of voltage V_{ab}.

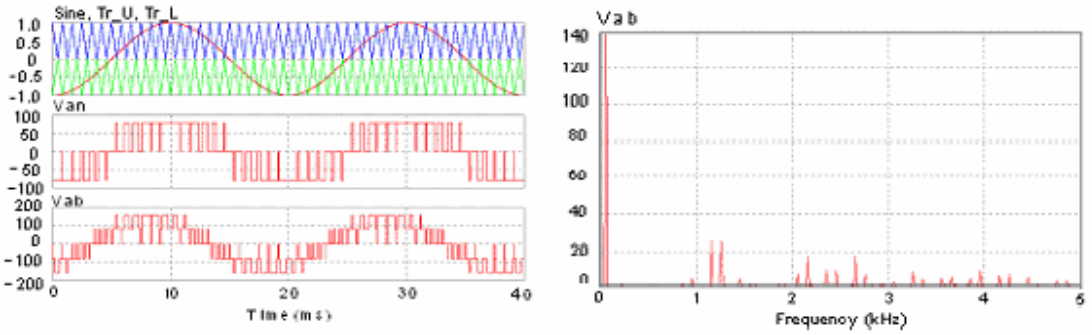


Fig. 4.1.1.1.a : $m_a = 1$.

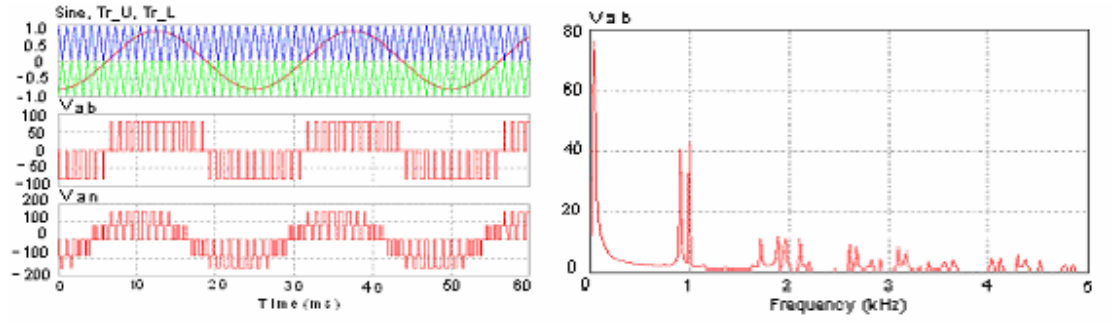


Fig. 4.1.1.1.b : $m_a = 0.8$.

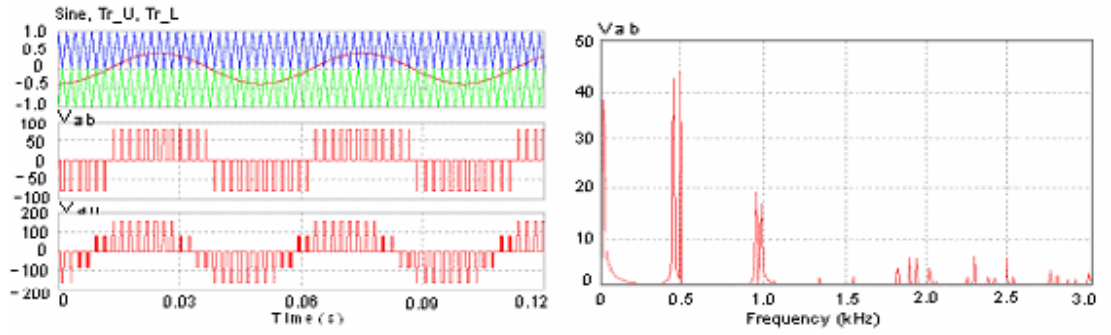


Fig. 4.1.1.1.c : $m_a = 0.4$.

The simulation shown below is for the load R = 10 ohms and L = 0.03H with $m_a = 1$ and $m_a = 0.4$.

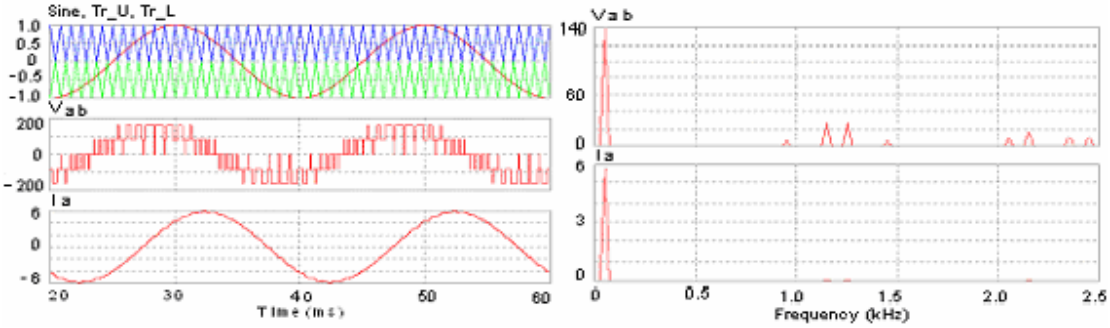


Fig. 4.1.1.2.a : $m_a = 1$.

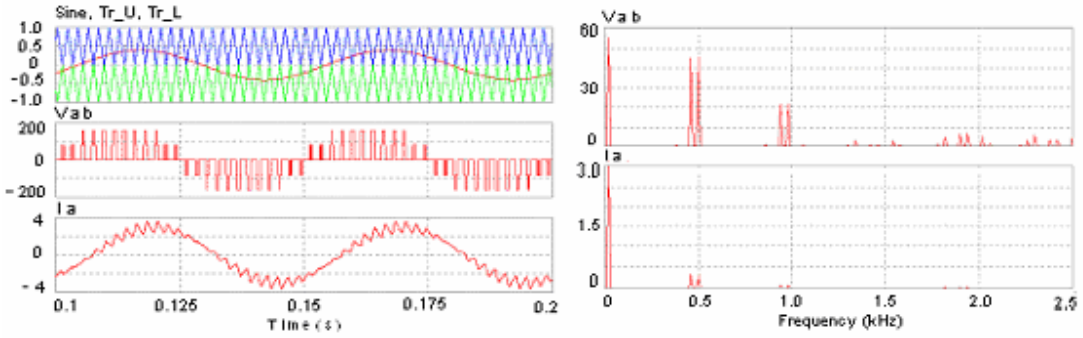


Fig. 4.1.1.2.b : $m_a = 0.4$.

4.1.2 Simulation Results For Triangular Waves With No Phase-Disposition

The simulation shown below is for the load R = 10 ohms and m_a = 1. Here the upper and lower carrier waves have 0^o phase shift as shown in figure 4.1.2.1.

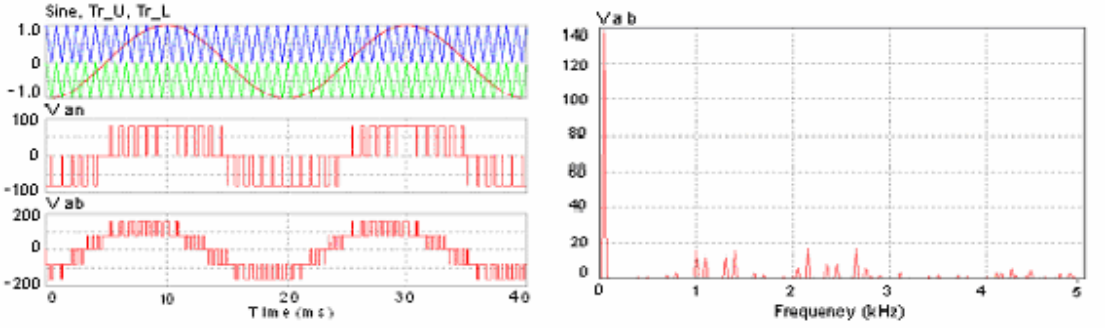


Fig. 4.1.2.1 : m_a = 1.

The simulation shown below is for the load R = 10 ohms and L = 0.03H.

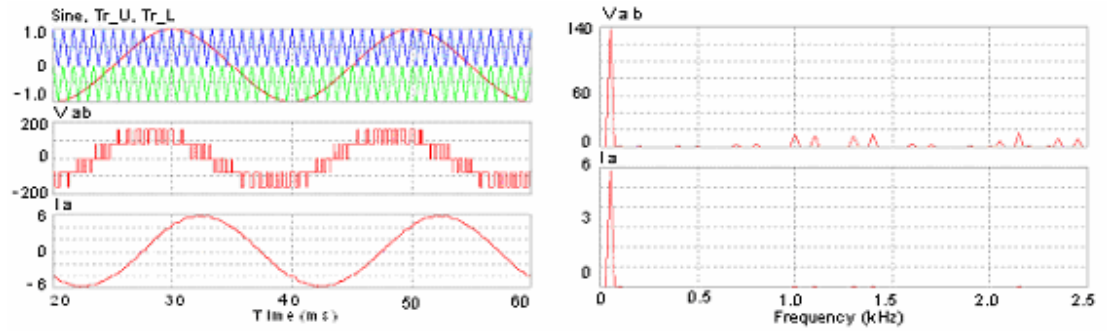


Fig. 4.1.2.2.a : m_a = 1.

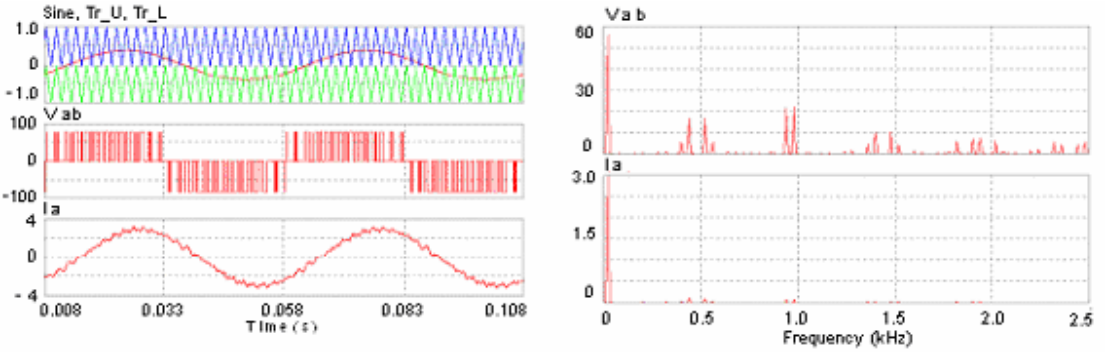


Fig. 4.1.2.2.b : m_a = 0.4.

4.2 Sinusoidal PWM With Two Capacitors & Single DC Source

Figure – 4.2 shows the model of a Three-Level Diode-Clamped Inverter with DC source, in PSIM. Here single DC source with 160 Volts and two series capacitor with C = 220uF and Resistive and Inductive load with value 10 ohm and 0.03 Henry respectively are used.

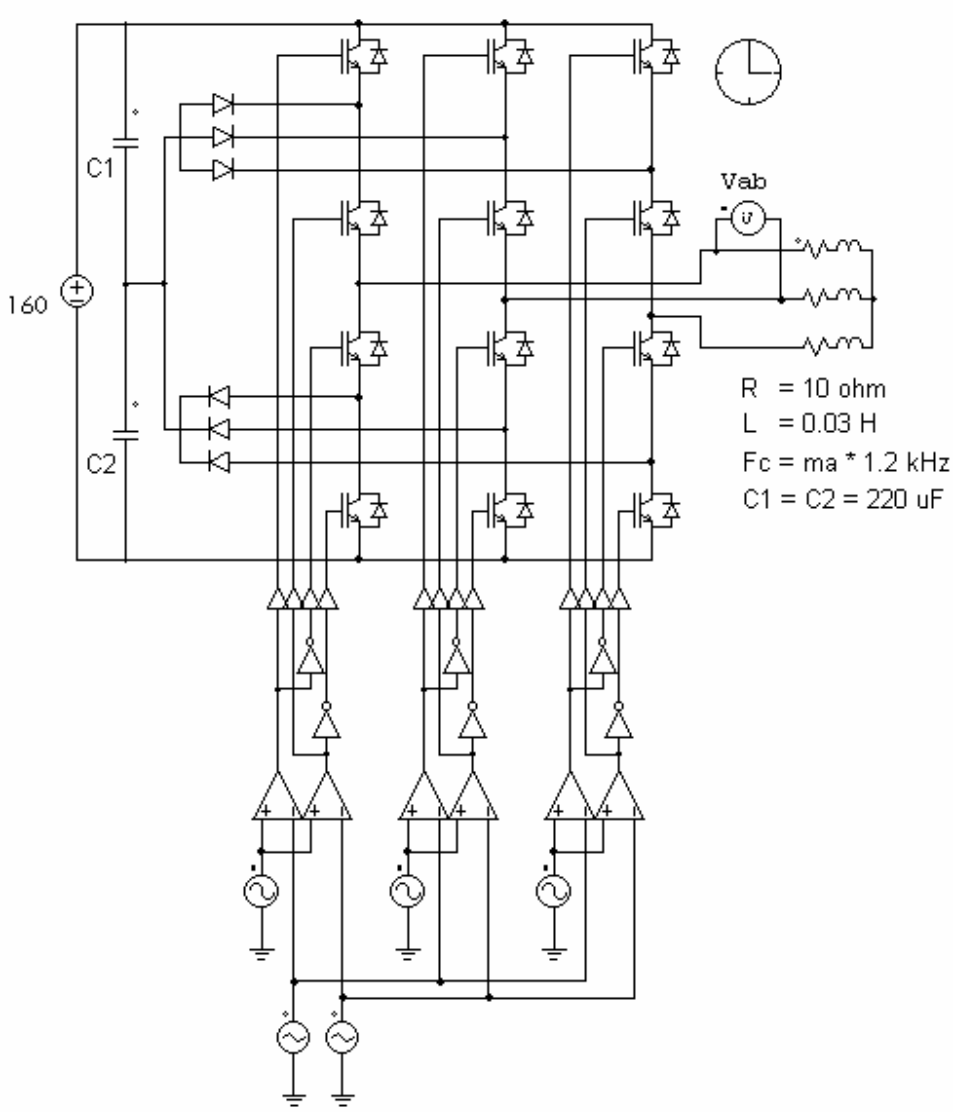


Fig. 4.2 : Three-Level Diode-Clamped Inverter With Sinusoidal PWM With Single DC Source.

The value of the capacitor is selected on the basis of the thumb rule used in industries, i.e., for 1 ampere rms output current (at rated condition) 40uF to 60uF capacitance is selected.

4.2.1 Simulation Results For Triangular Waves With Phase-Disposition

The simulation shown below is for the load R = 10 ohms and L = 0.03H with $m_a = 1$ and $m_a = 0.4$.

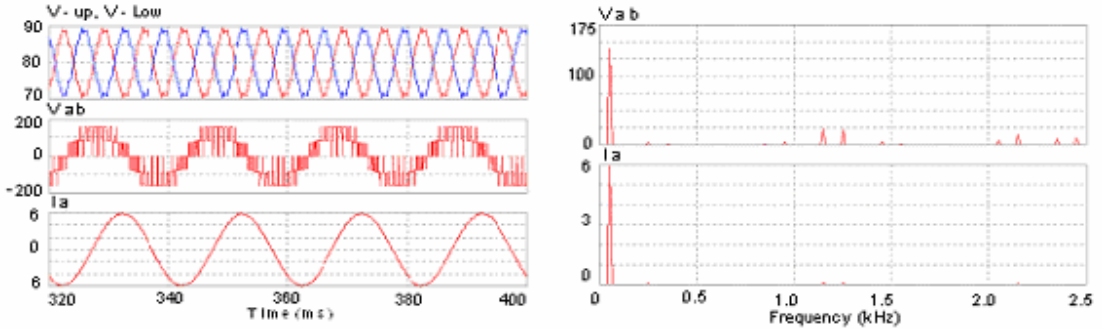


Fig. 4.2.1.a : $m_a = 1$.

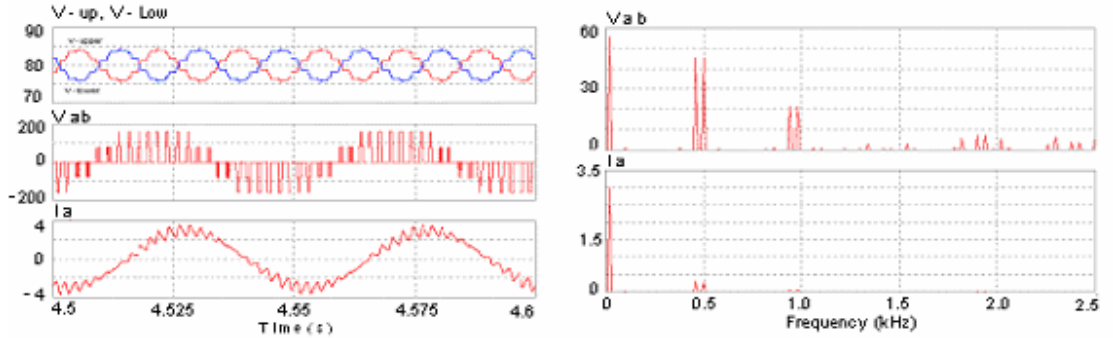


Fig. 4.2.1.b : $m_a = 0.4$.

4.2.2 Simulation Results For Triangular Waves With No Phase-Disposition

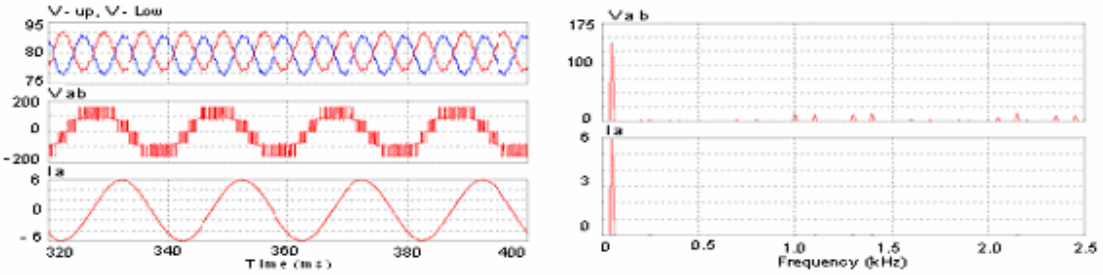


Fig. 4.2.2.a : $m_a = 1$.

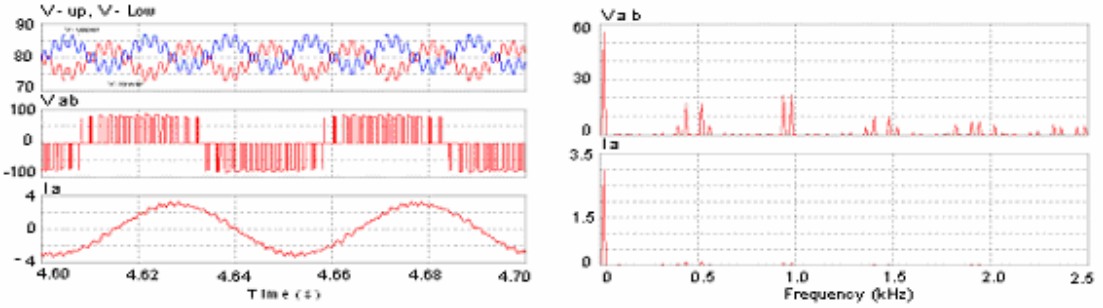


Fig. 4.2.2.b : $m_a = 0.4$.

The first set of output line voltage harmonics are centered around the switching frequency of the carrier wave, as it can be seen from the fast fourier transform analysis of the output line voltage. The other set of harmonics are centered around the multiple of the switching frequency of the carrier wave as seen above. The total harmonic distortion is considerably low in case of the topology with carrier waves in no phase disposition state. The main problem in case of SPWM is the use of the redundant switching states, which are used in a proper manner in case of SVPWM to balance the average neutral point current to zero and balance the neutral point voltage with upper and lower capacitor voltages equal.

4.3 Simulation Model With Space-Vector PWM

Simulation of the proposed model in done in the PSIM v 6.0 package. The programming for the sector identification, time calculations and all other calculations are done in the Visual Basic v 6.0. Figure 4.3.a shows the PSIM model.

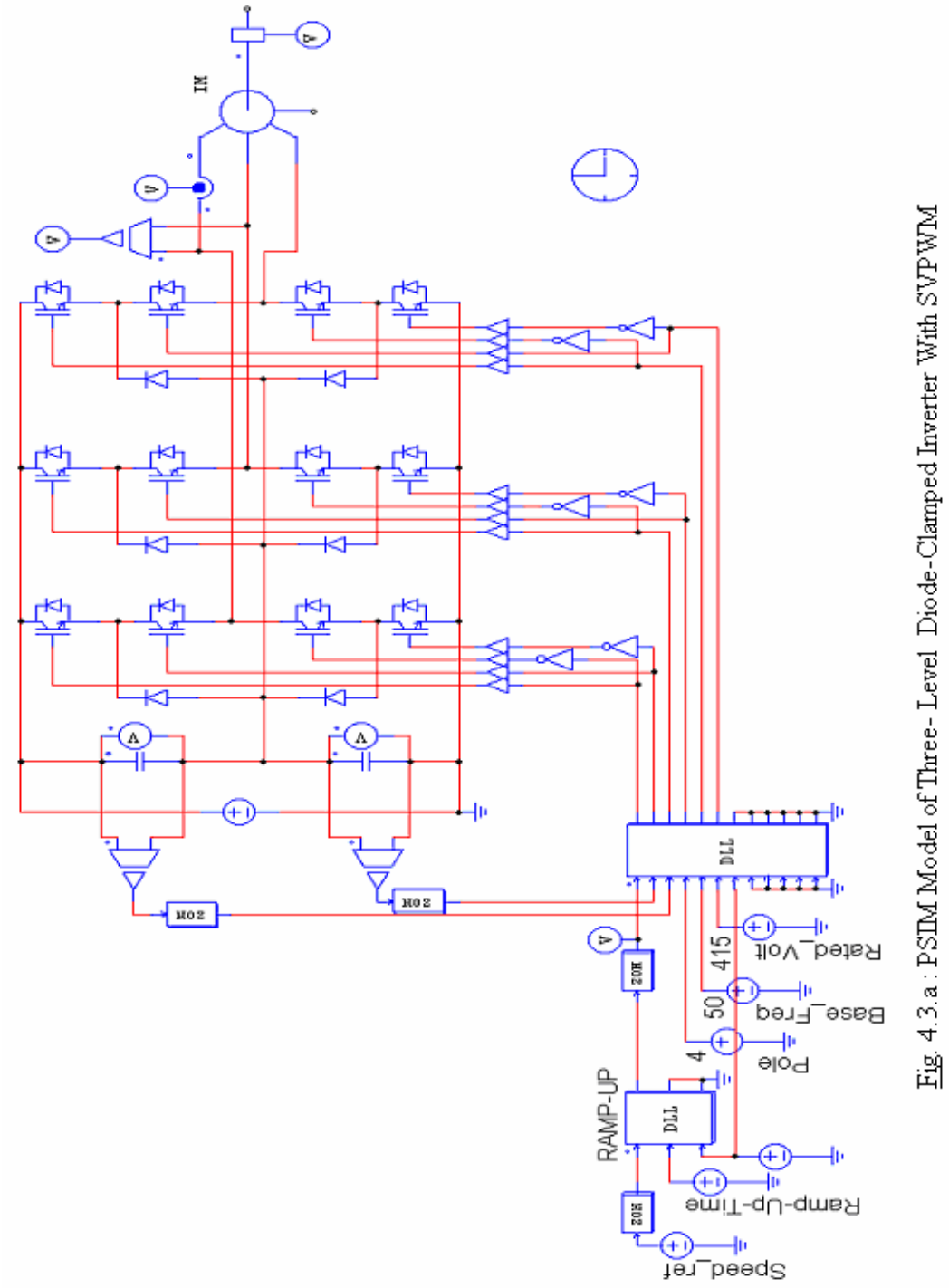


Fig. 4.3.a : PSIM Model of Three- Level Diode-Clamped Inverter With SVPWM

Flowchart of The Program:

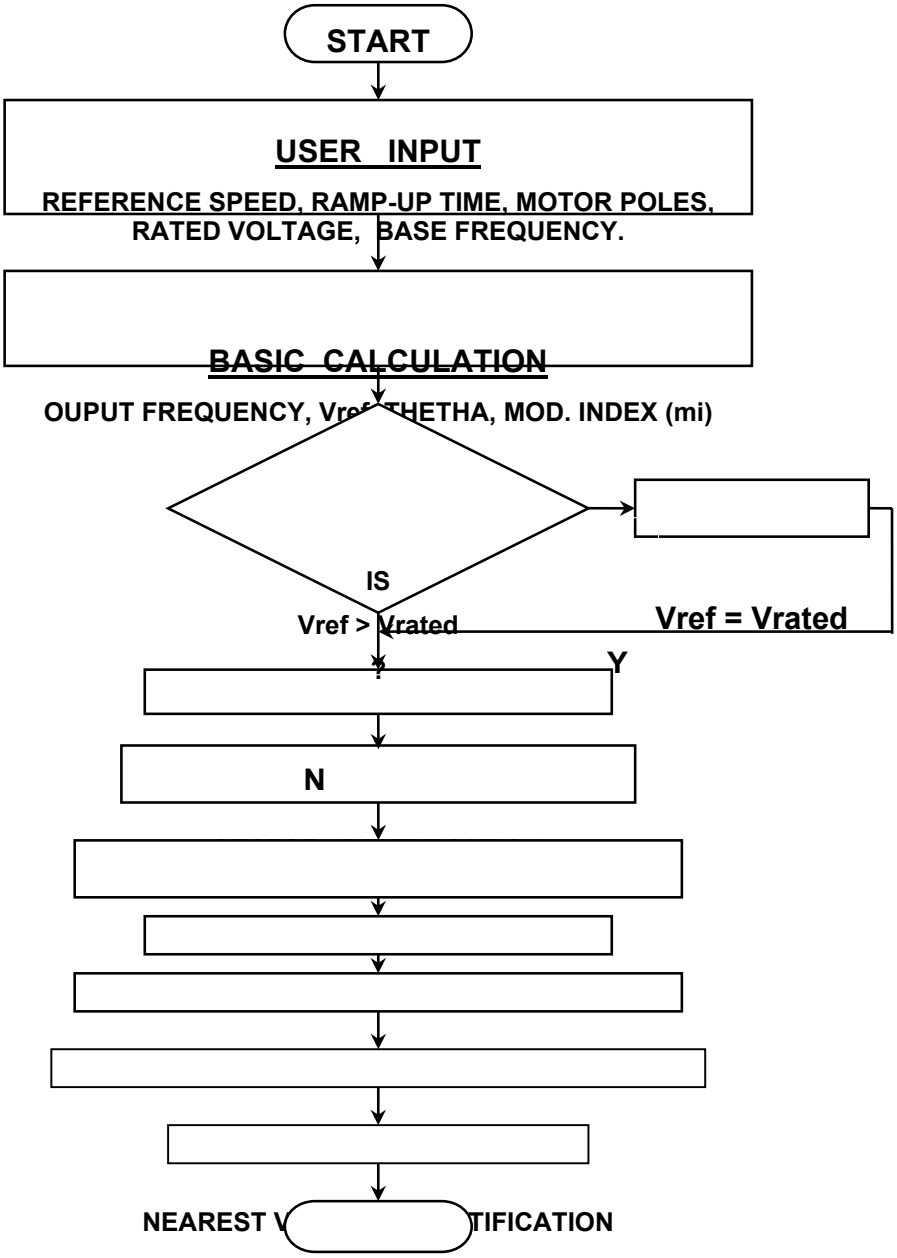
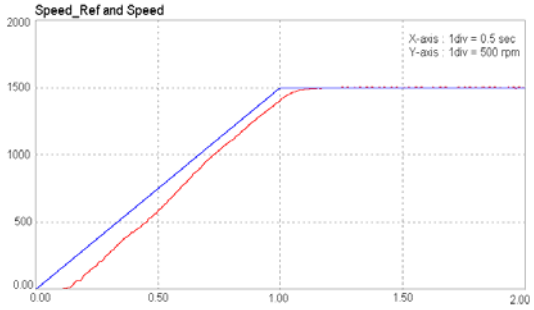
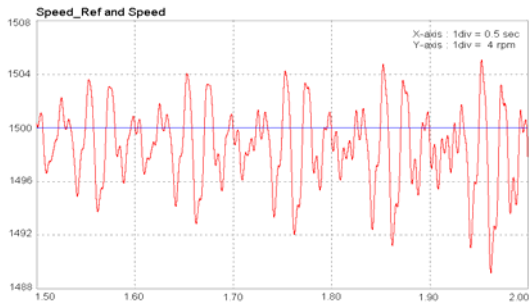


Fig. 4.3.b : Flowchart of the proposed model.

4.4 Simulation Results of SVPWM.

4.4.1 Speed reference = 1500 rpm.





(a.) (b.)

Fig. 4.4.1.1 : (a.) Speed Reference and Motor Speed. (b.) Expanded View.

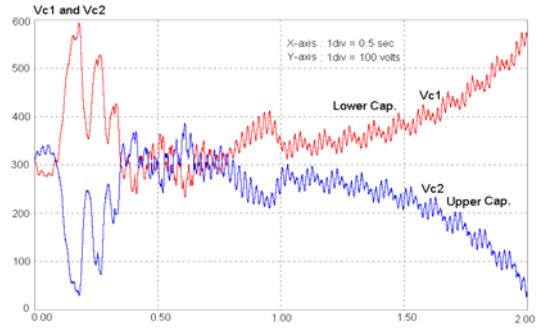


Fig. 4.4.1.2 : Capacitor Voltages.

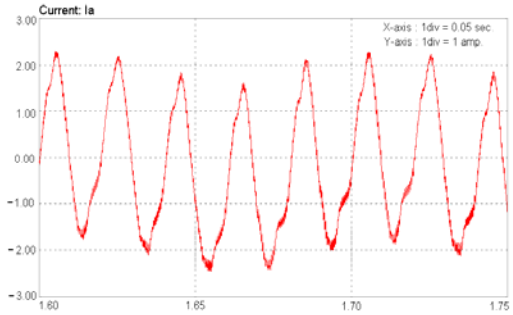


Fig. 4.4.1.3 : Motor Current.

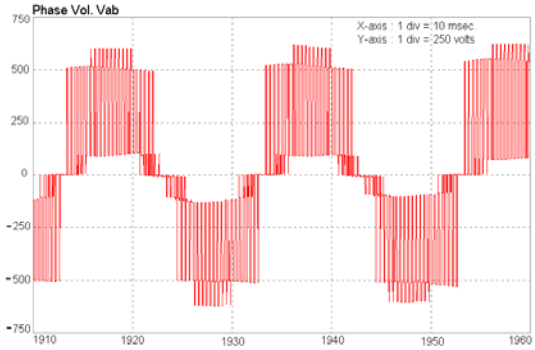


Fig. 4.4.1.4 : Phase Voltage Vab.

The problem in Diode-Clamped Inverter is the voltage unbalance in the upper and lower capacitors, which can be seen from the Figure 4.4.1.2. This problem needs to be overcome.

The problem of the unbalanced capacitor voltages is overcome by adjusting the counter value according to the change in reference speed value and the ramp-up. The simulation results are shown in the following section with different speed references.

4.4.2 Speed reference = 1500 rpm.

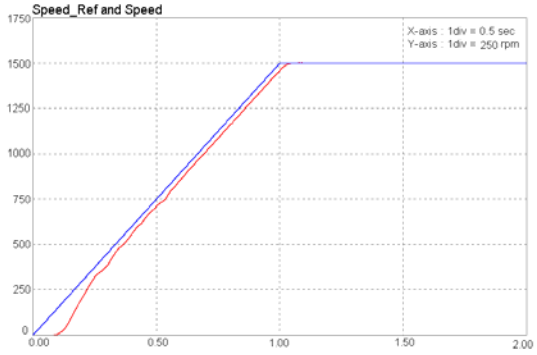


Fig. 4.4.2.1 : Speed ref. & Motor speed.

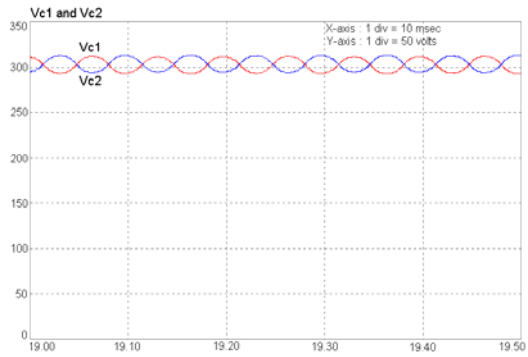
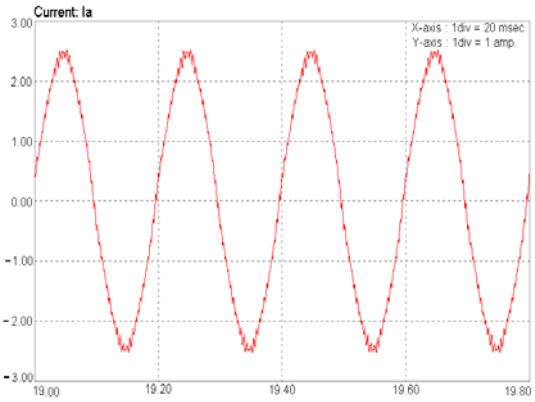
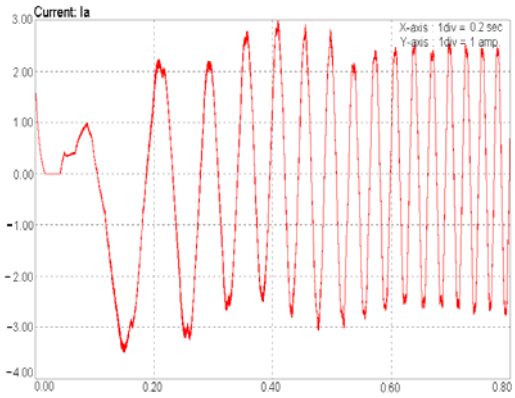


Fig. 4.4.2.2 : Capacitor Voltages.



(a.)



(b.)

Fig. 4.4.2.3 : Motor Current Ia (a.) Ref. speed and (b.) Starting.

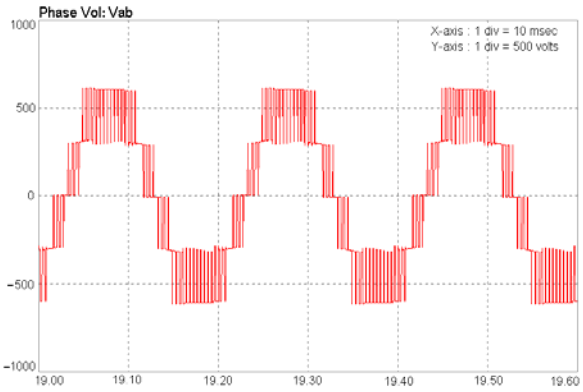


Fig. 4.4.2.4 : Phase Voltage Vab.

4.4.3 Speed reference = 1200 rpm.

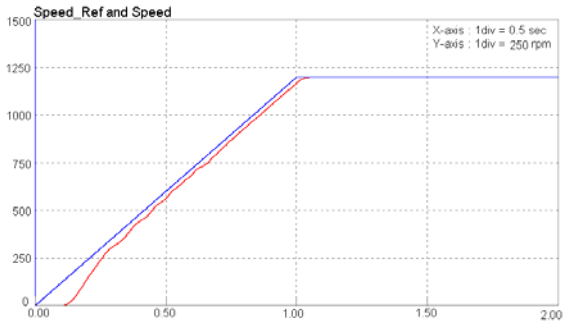


Fig. 4.4.3.1 : Speed ref. & Motor speed.

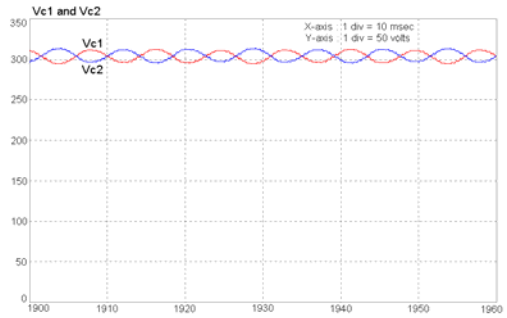


Fig. 4.4.3.2 : Capacitor Voltages.

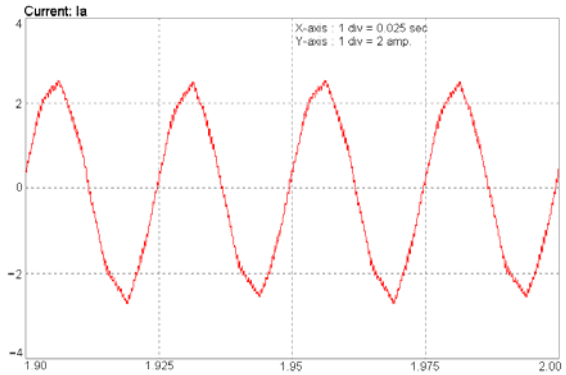


Fig. 4.4.3.3 : Motor Current Ia.

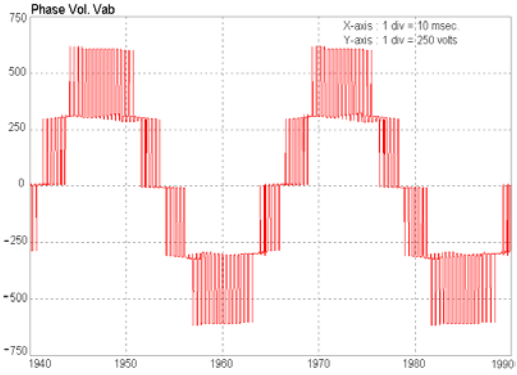


Fig. 4.4.3.4 : Phase Voltage Vab.

4.4.4 Speed reference = 400 rpm.

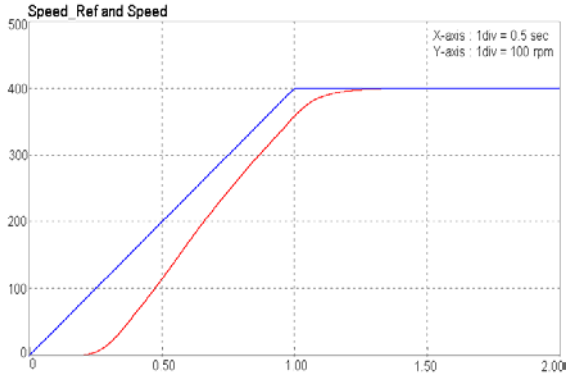


Fig. 4.4.4.1 : Speed ref. & Motor speed.

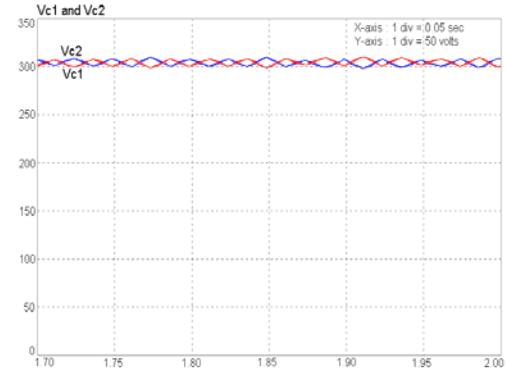


Fig. 4.4.4.2 : Capacitor Voltages.

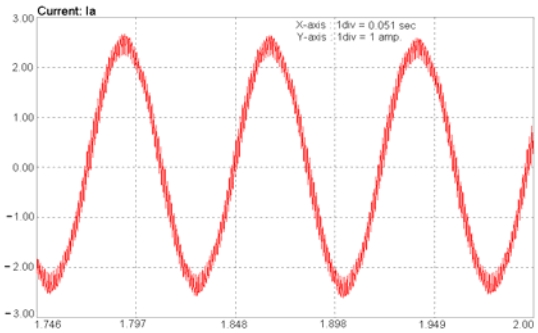


Fig. 4.4.4.3 : Motor Current Ia.

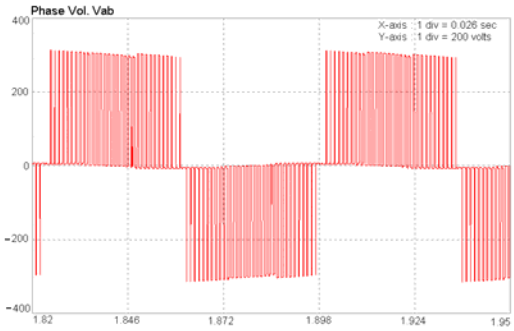


Fig. 4.4.4.4 : Phase Voltage Vab.

4.4.5 Speed reference = 1500rpm to -1500rpm to 400 rpm.

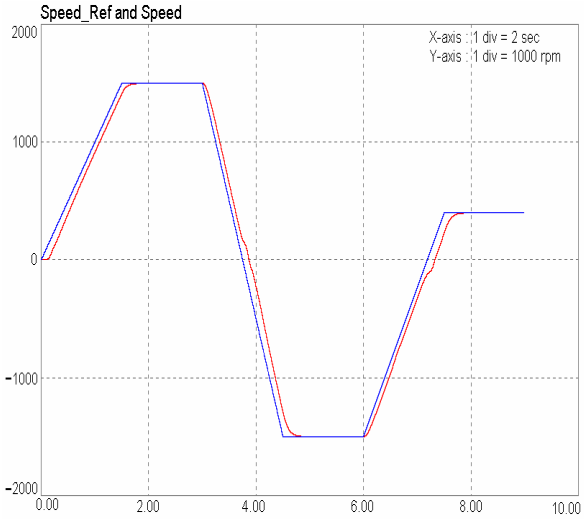


Fig. 4.4.5.1 : Speed ref. & Motor speed.

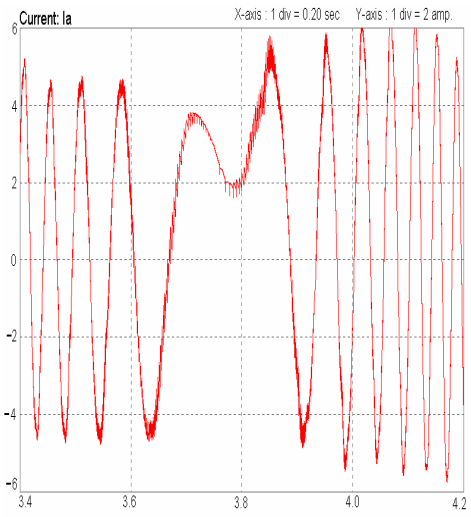


Fig. 4.4.5.2 : Motor Current (Ia).

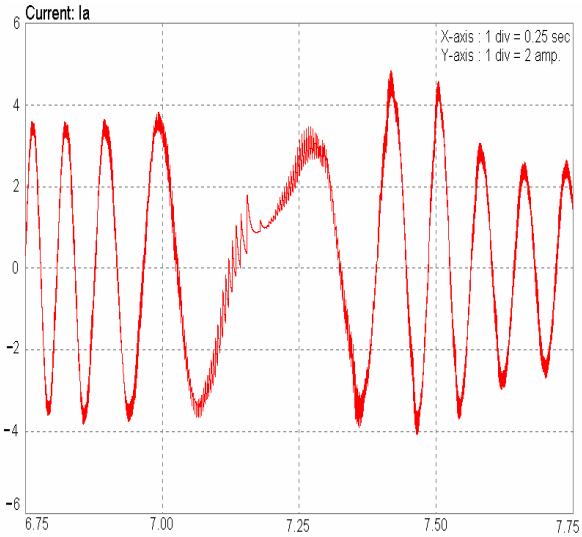


Fig. 4.4.5.3 : Motor Current (Ia).

The ramp-up time for the 4.4.1 ~ 4.4.4 is kept to be as 1.0 second and for the 4.4.5, ramp-up time is 1.5 second as seen from the figures. After the modification made for the counter value to change in respect to the reference speed, the capacitor voltages are balanced. As a result of which the motor does not hunt, which was the case before the modification. The motor phase current (Ia) is too balanced. As seen from the figure 4.4.2.3.(b.), the motor current at the time of starting does not exceed the rated current value and get a soft-starter like operation. As a result of the balanced neutral point current and voltages, the output voltages and the currents have reduced order of harmonics.

From the case 4.4.5, it can be seen that as the speed-reference is varied from 1500 rpm to -1500 rpm and lastly to 400 rpm, there is a smooth variation in the speed as well as the current during the time of the change over of speed from forward motoring to reverse motoring and vice versa. Figure 4.4.5.2 shows the variation of current when there is speed transaction from forward motoring to reverse motoring. Figure 4.4.5.3 shows the variation of current during the speed transaction from reverse motoring to forward motoring.

5. SIMULATION MODEL OF NINE-LEVEL H-BRIGE INVERTER

5.1 Firing Topology-I

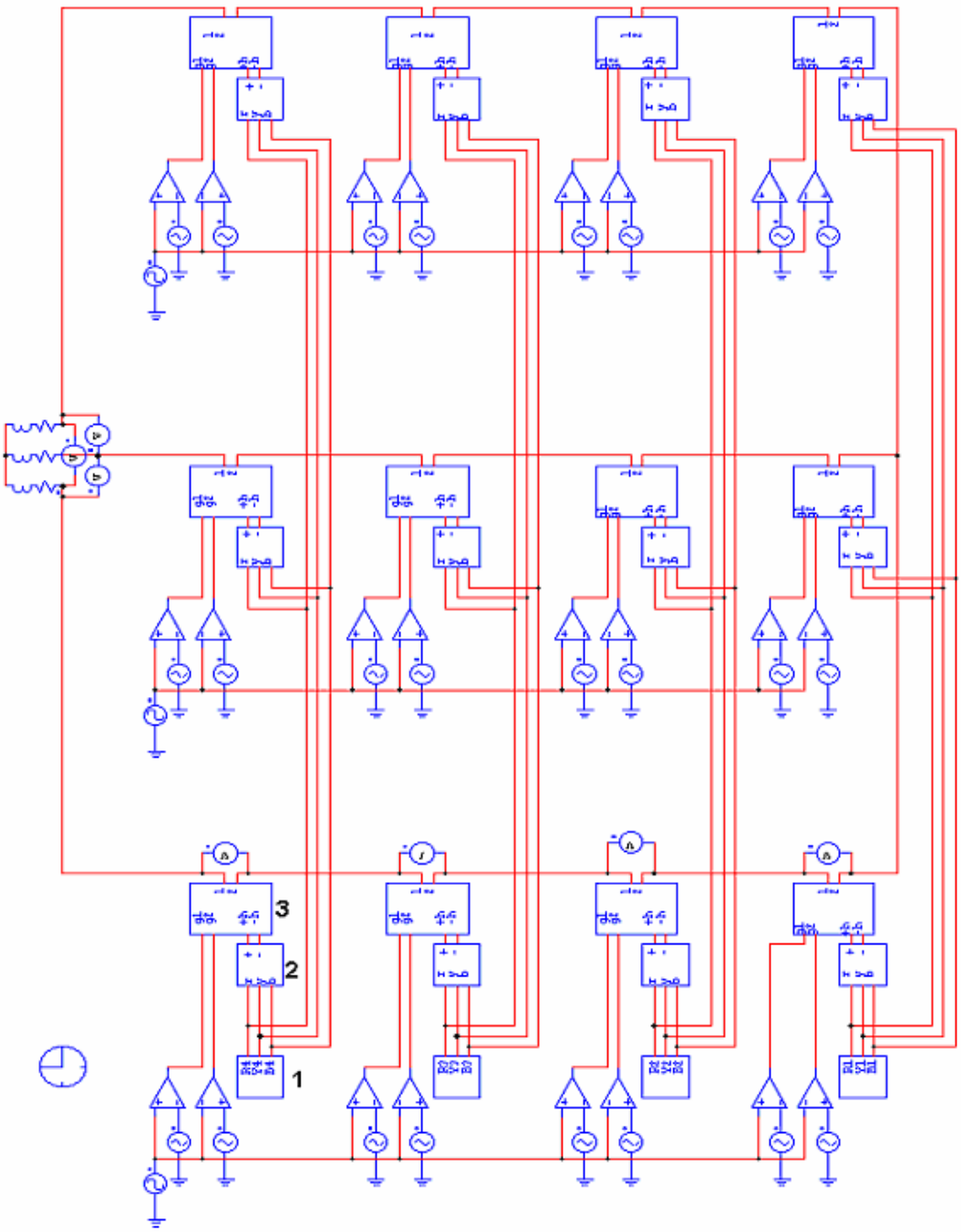


Fig 5.1.1: H-Bridge Multilevel Topology (Firing Scheme - I)

Figure 5.1.1 shows a basic 9-level H-bridge inverter topology with a basic firing scheme topology-I. The load used for the simulation purpose is R = 17 Ohms and L = 0.05 Henry. The blocks marked by '1', '2' and '3' are represented in following figures. Block-1 represents a 3-Phase source with line reactors. For simulation purpose to produce a effect of a 24-pulse transformer (12-secondaries), the 3-Phase sources are each shifted by 0^0, 15^0, 30^0, 45^0. Block-2 represents a transformer rectifier set with DC-Choke and capacitor. While Block-3 represents an H-Bridge Module. There are such 12 modules known as CELL, with four Cells cascaded as shown in figure 5.1.1 for each phase.

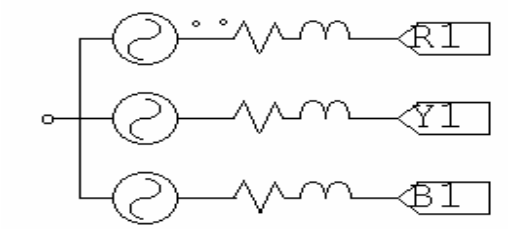


Fig. 5.1.2 : Three-Phase Source (Block-1)

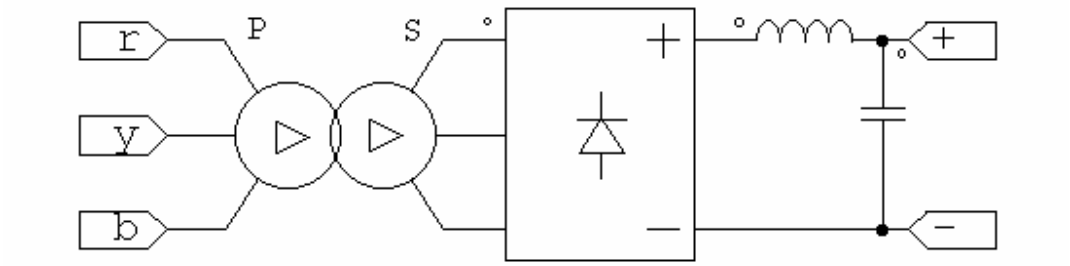


Fig. 5.1.3 : Transformer & Rectifier With DC-Choke and DC-Link Cap. (Block-2)

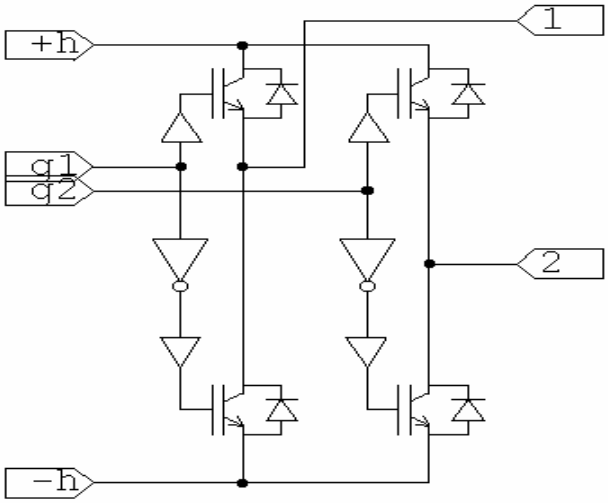
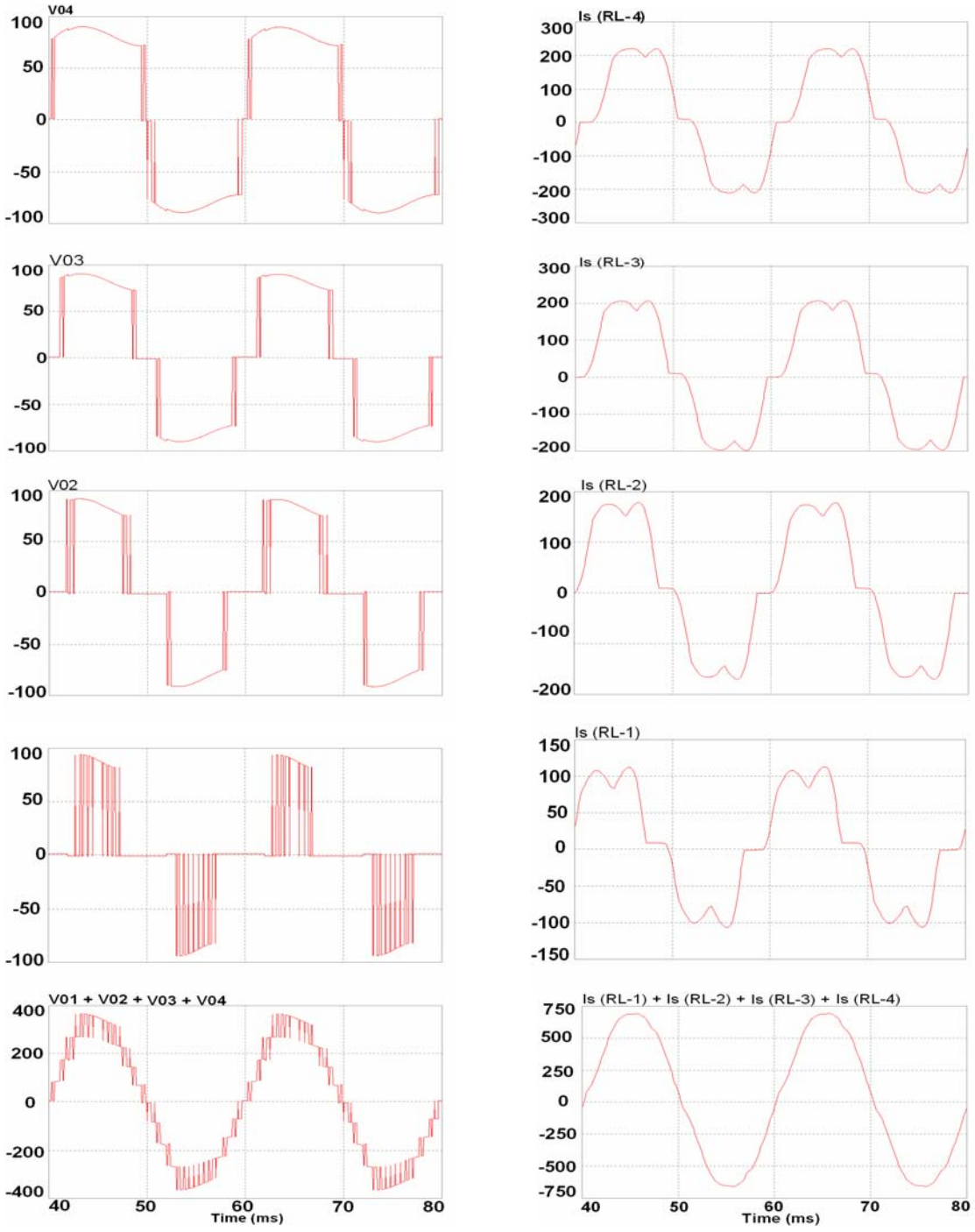


Fig. 5.1.4 : H-Bridge Module (Block-3)

5.1.1 Simulation Results For Firing Topology-I



(a.) **(b.)**

Fig. 5.1.1.(a.) Top to bottom, Voltages across Cells from top to bottom & bottom-most Phase-Voltage.
(b.) Current in Transformers of R-Phase & total source current.

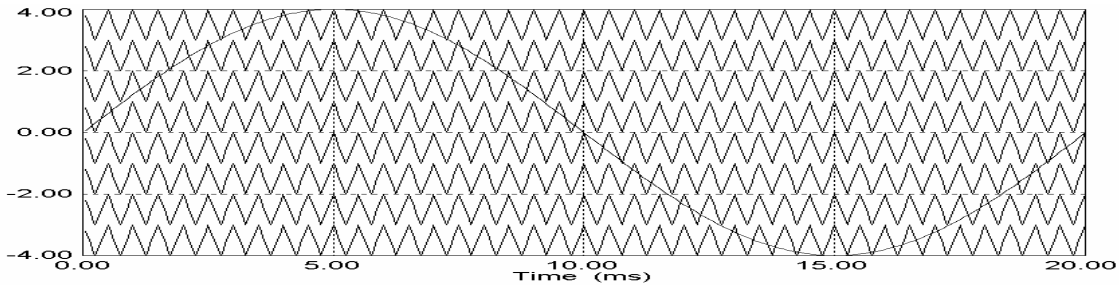


Fig. 5.1.1.1 : Sine-Triangular Comparison.

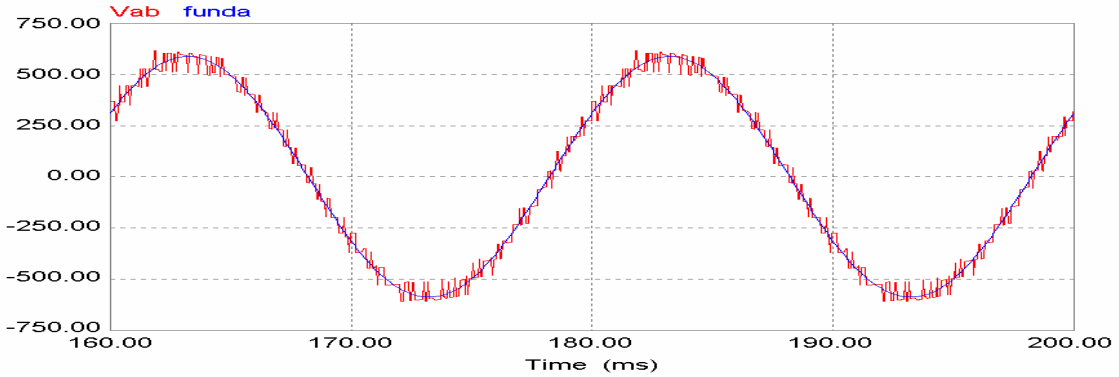


Fig. 5.1.1.2 : Line Voltage (416 Volts RMS.)

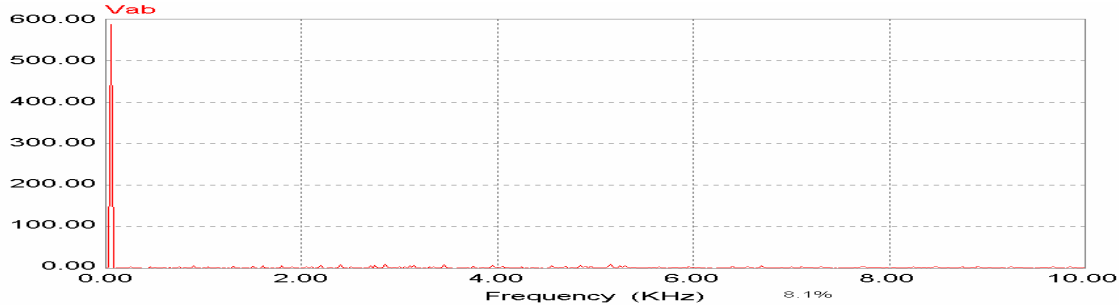


Fig. 5.1.1.3 : Line Voltage FFT.

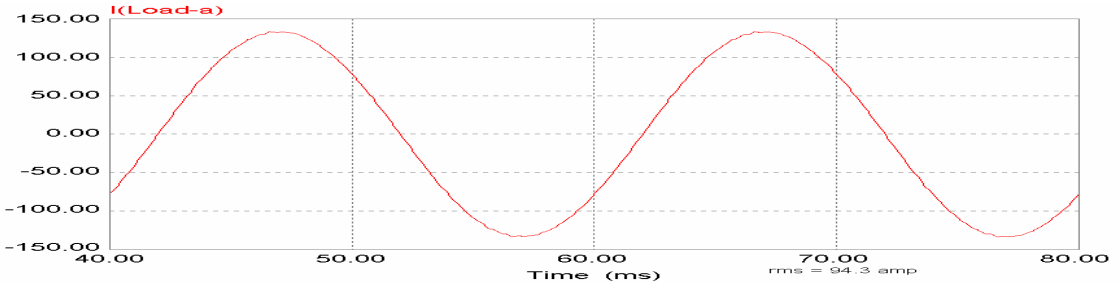


Fig. 5.1.1.4 : Load Current (98 Amps RMS.)

5.2 Firing Topology-II

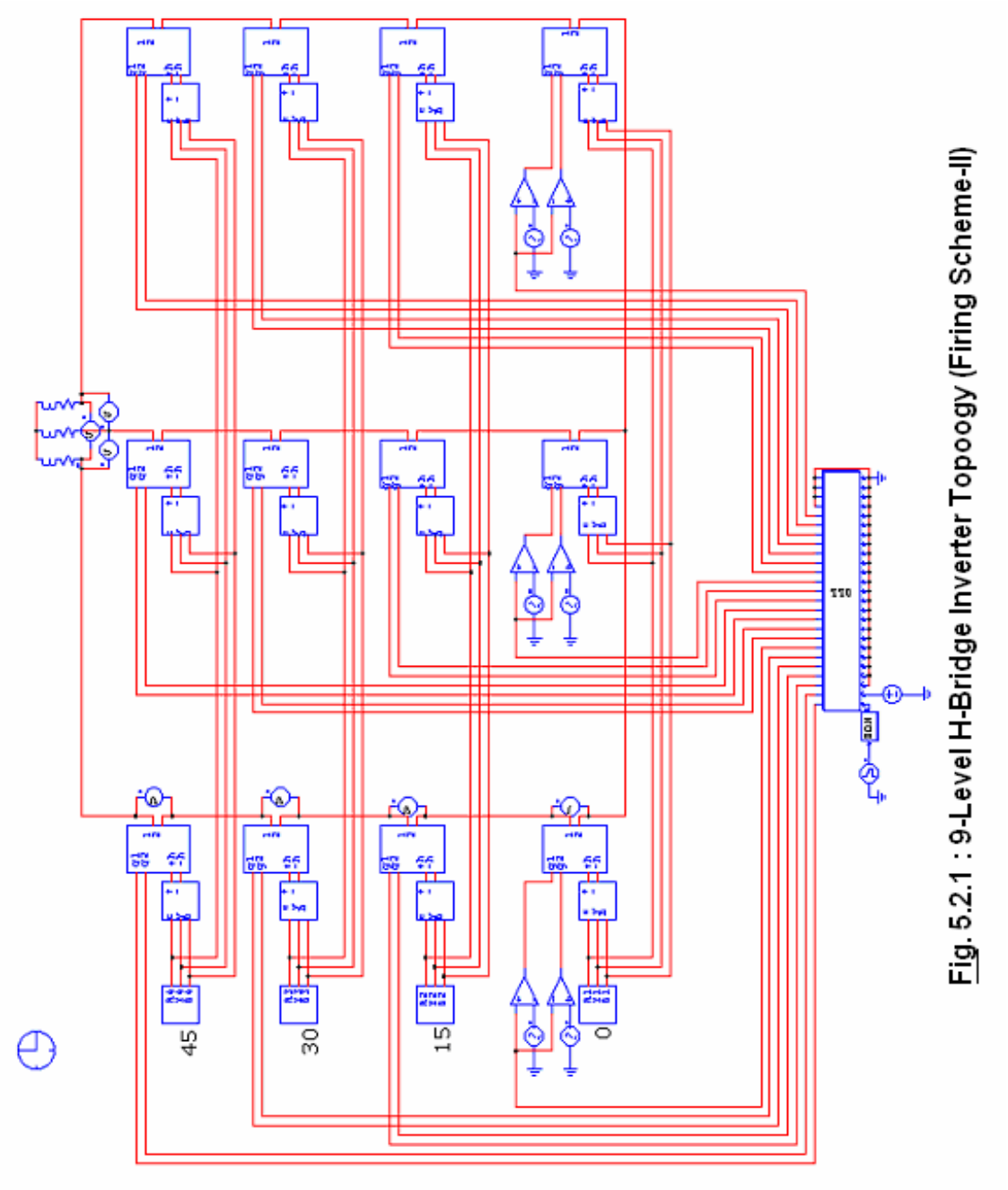
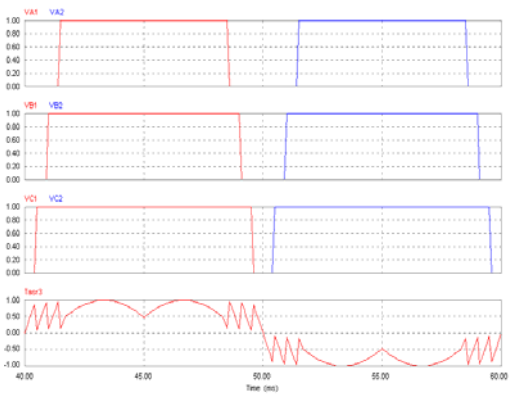


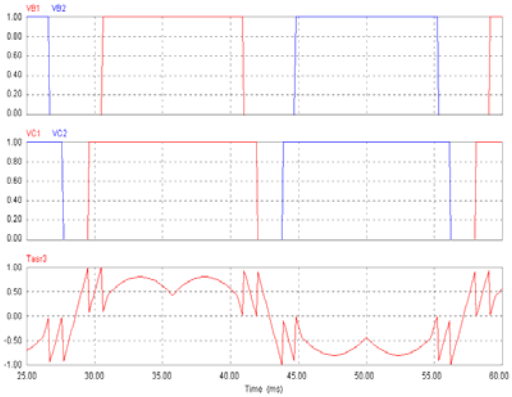
Fig. 5.2.1 : 9-Level H-Bridge Inverter Topoogy (Firing Scheme-II)

The power supply, transformer-rectifier and H-Bridge Cell blocks are same as explained in previous section.

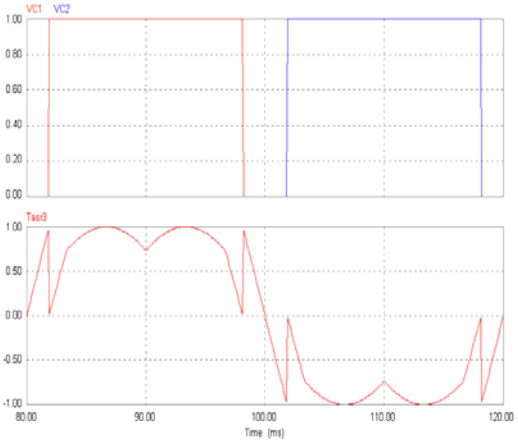
5.2.1 Simulation Results For Firing Topology-II



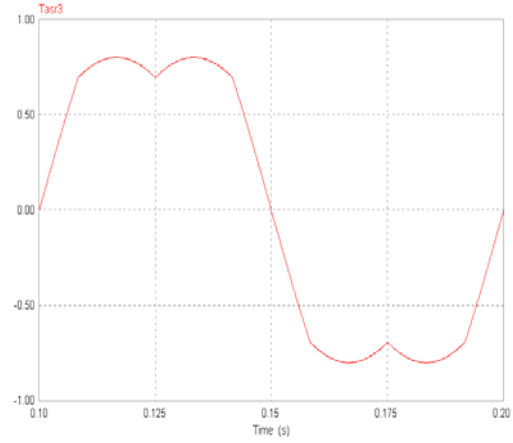
Mod. Index = 1



Mod. Index = 0.7



Mod. Index = 0.5



Mod. Index = 0.2

Fig. 5.2.2 : Gate Pulses for Cell-2,3,4 and Reference Wave for Cell-1.

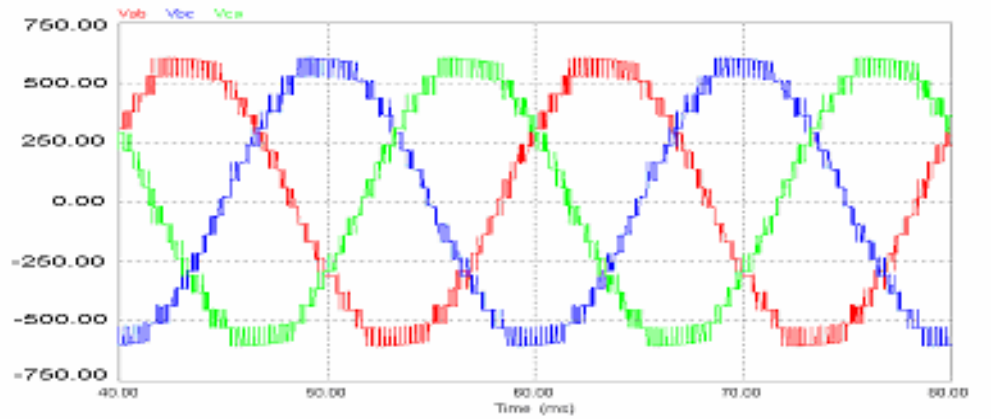


Fig. 5.2.3 : Line Voltages (440Volts RMS)

6. HARDWARE DESCRIPTION

6.1 Control Circuit & Driver Circuit

The total system for control circuit and driver circuit is divided into four PCB's. The four PCB's used are:

1.) Display/Keypad Card (PCA-2003B).

2.) Control Signal Board (PCA-2004A).

3.) Multi-Level Interface Board (PCA-2007).

4.) MV Driver Board (PCA-1019).

6.1.1 Display/Keypad Card

The display cum keypad is used to enter the different parameters such as Reference Frequency, V/f Curve Shapes, Jog Frequency, etc. The same card is equipped with LCD which shows the different parameters to the user. For the testing purpose, the same program used in Expert Eazy Drive is installed in the Card for Multi-level inverter. The program is transferred to the Card through an JTAG at RS-485 port.

6.1.2 Control Signal Board

The main heart of the control signal board PCA-2004A is DSP 'TMS320F2811'. The block diagram of the Control Signal Board PCA-2004A is shown in Fig. 6.1.2. The same card is used in the EXPERT EAZY Drive and DC Drive. The main concern with this card for the prototype making of Multi-Level Inverter is with the DSP, its programming and the interfacing of the card with the Interface Board (PCA-2007). The power supply to the PCA-2004A is provided through an SMPS with voltage input of 230VAC and output dc of '+24V/0.5Amp', '+15V/2.2Amp', '+5V/1Amp', '0V/COM' and '-15V/0.5Amp'. The '3.3V/1.9V' supply voltage for the DSP 'TMS320F2811' is regulated from IC-TPS76701 with '+5V' input from SMPS.

The programming for the DSP 'TMS320F2811' is done in the Code Composer Studio. The program is written in the 'C-Language'. The main problem with the programming was to use an existing program for the AC Drive and availability of 12-pins only for the generation of 48 Gate-Signals for 48-IGBT's in an 9-Level Inverter system. The problem

was then solved by the complex and logical programming. The program is transferred from PC to DSP 'TMS320F2811' from an 'Emulator' through an 'JTAG'.

Table – 6.1. DSP Pins Usage For Signal Generation.

SR.NO.	DSP PIN	DSP PIN FUNCTION	INITIALISE AS	CIRCUIT FUNCTION
1	68	GPIOA0/PWM1	PWM	R-PHASE PWM CELL-1
2	69	GPIOA1/PWM2	GPIO	R-PHASE DIRECTION, 1 = -Ve Half & 0 = +Ve Half
3	70	GPIOA2/PWM3	PWM	Y-PHASE PWM CELL-1
4	71	GPIOA3/PWM4	GPIO	Y-PHASE DIRECTION, 1 = -Ve Half & 0 = +Ve Half
5	72	GPIOA4/PWM5	PWM	B-PHASE PWM CELL-1
6	75	GPIOA5/PWM6	GPIO	B-PHASE DIRECTION, 1 = -Ve Half & 0 = +Ve Half
7	33	GPIOB0/PWM7	GPIO	Gate Signal for CELL-2. Active High
8	34	GPIOB1/PWM8	GPIO	Gate Signal for CELL-3. Active High
9	35	GPIOB2/PWM9	GPIO	Gate Signal for CELL-4. Active High
10	36	GPIOB3/PWM10	GPIO	R-Phase chip select for CELL-2,3,4. Active High
11	37	GPIOB4/PWM11	GPIO	Y-Phase chip select for CELL-2,3,4. Active High
12	38	GPIOB5/PWM12	GPIO	B-Phase chip select for CELL-2,3,4. Active High
13	81	PDPINTA	PDPINT	OVER CURRENT FROM CELL
14	60	GPIOD5/PBPINTB	GPIO	ENABLE for all gate pulse, in case of fault : LOW

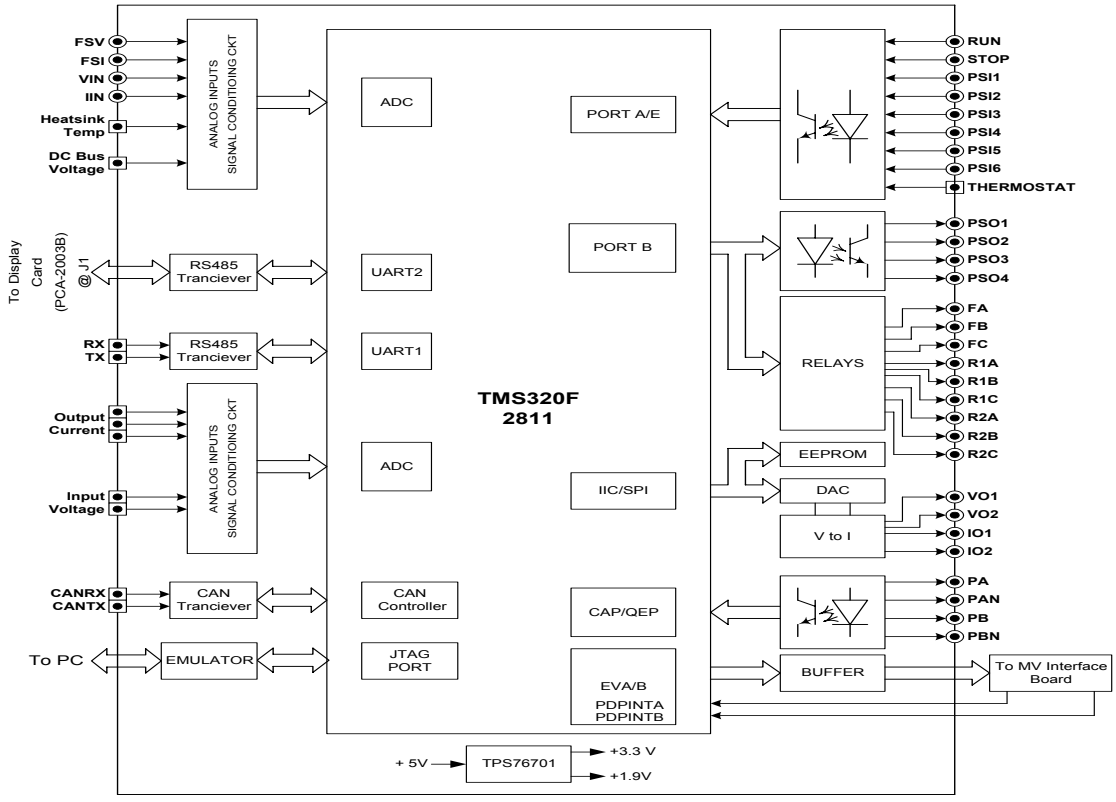


Fig. 6.1.2 : Block Diagram Representation of Control Signal Board

6.1.3 Multi-Level Interface Board

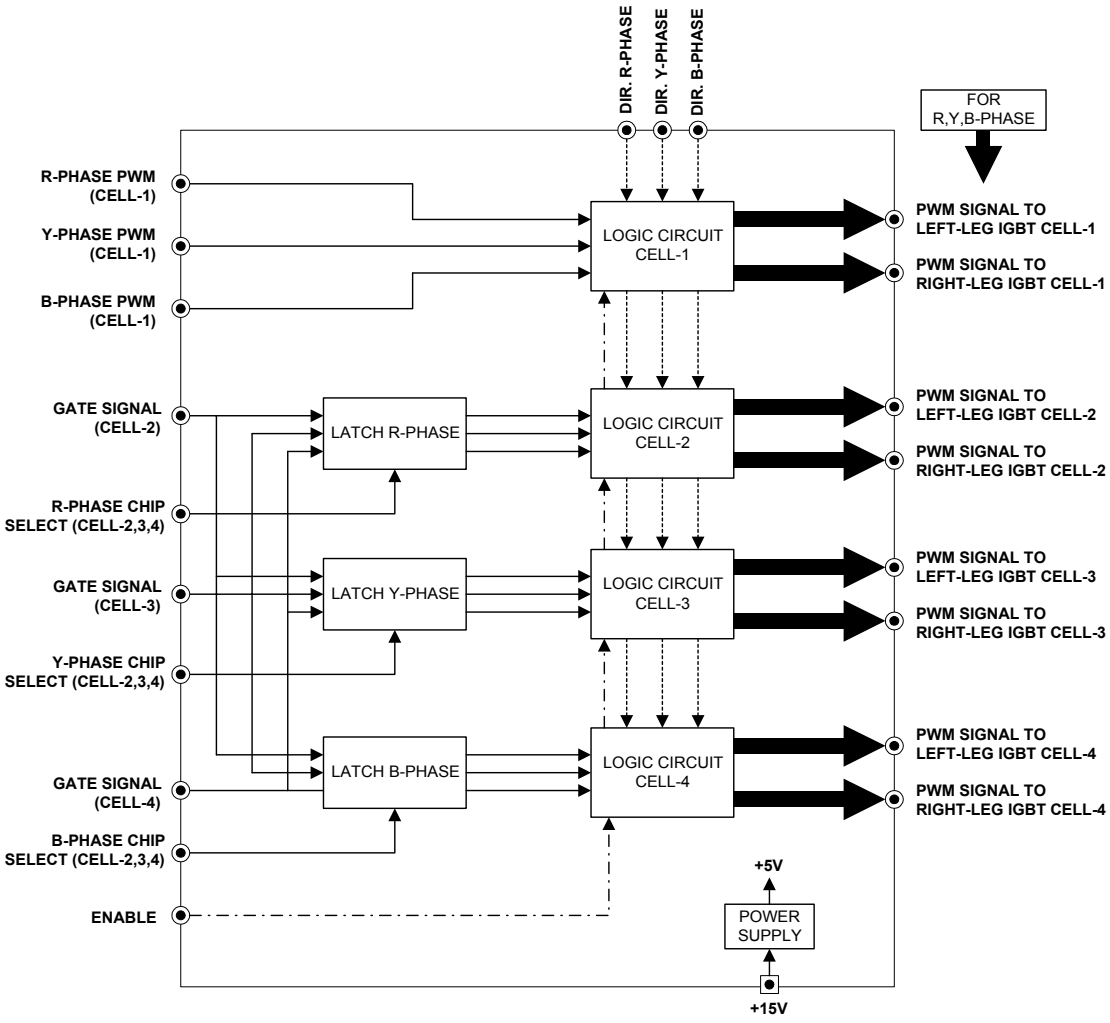


Fig. 6.1.3 : Block Diagram Representation of Multi-Level Interface Board

Features And Functions Of The Multi-Level Interface Board:

1.) Fiber Optic Transceivers, which provides isolation between the Control Circuit and High-Voltage Power Circuit.

2.) Enable/Disable signal seizes the Gate Signals in case of any fault.

3.) Twelve signals are converted to 24 Gate Signals.

Circuit Description:

The twelve signals generated from Control Signal Board (PCA-2004A), is transferred to Multi-Level Interface Board through FRC cables. The circuitry of Interface Board (PCA-2007) is developed such that 24-Gate Pulses required for the 9-Level H-Bridge Inverter are generated here from 6-Gate Pulses and 6-Control Signals derived from the Control Signal Board.

The three direction signals 'DIR' for R-Phase, Y-Phase and B-Phase are used to differentiate the Gate Pulses for the Right-Leg IGBT's and Left-Leg IGBT's used in each CELL.

The 'Chip Select' or 'Latch Enable' signals for R-Phase, Y-Phase and B-Phase are utilized over here to fetch the Gate-Signals for 'CELL-2', 'CELL-3' and 'CELL-4' respectively for R-Phase, Y-Phase and B-Phase, which were multiplexed in DSP.

The PWM Gate Pulses for R-Phase, Y-Phase and B-Phase are directly transferred to the Logic Circuit, as shown in Figure 6.1.3.

The Logic Circuit complies of NOR logic which used 'DIR' and 'Gate-Signals' to finally generate 24 Gate Signals. An Enable/Disable Signal instantly seizes Gate Signals to MV Driver Board (PCB-1019), as soon as an fault is detected.

The voltage requirement for all the IC's used in this board is +5 Volts, which is obtained through an SMPS Voltage of +15 Volts using IC LM2595. The 24 Gate-Signals generated through this board are transmitted to 12 MV Driver Board (PCB-1019), via fiber optic cables for isolation between high-voltage power circuit and low-voltage control circuit.

6.1.4 MV Driver Board

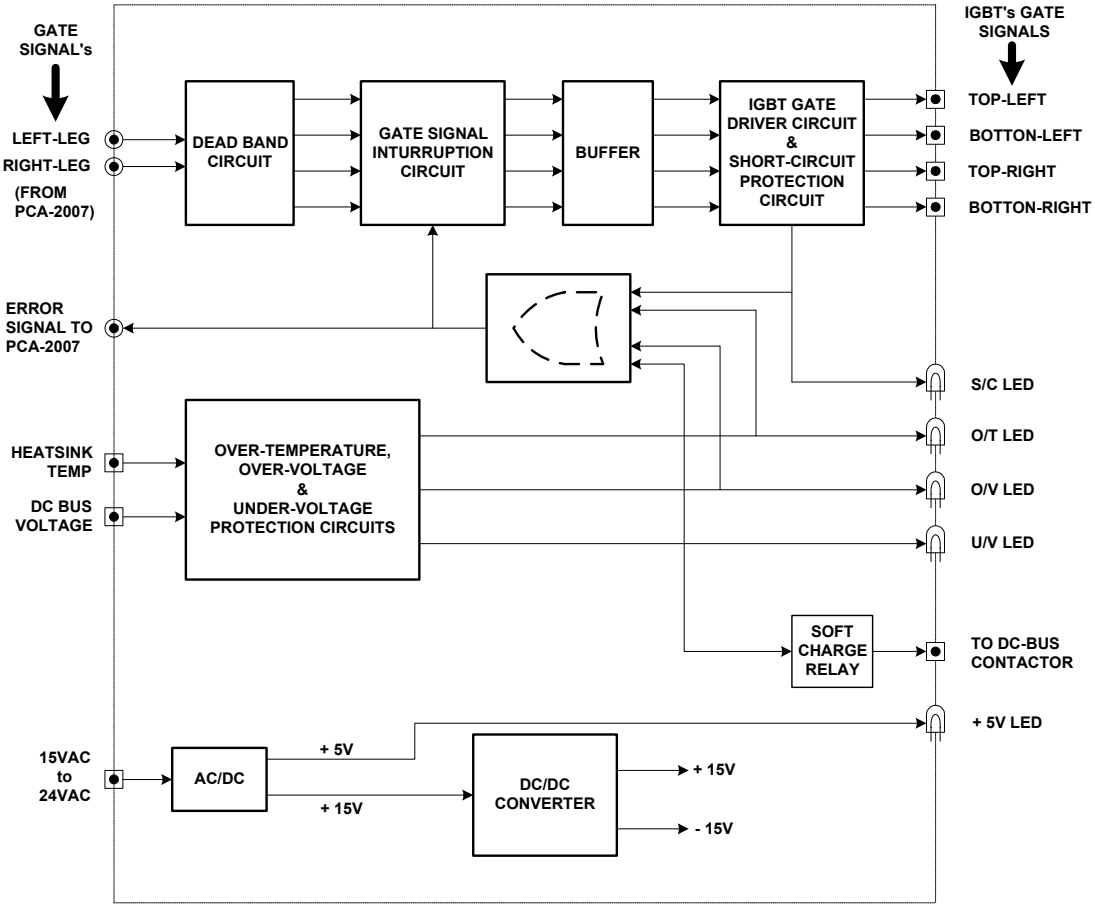


Fig. 6.1.4 : Block Diagram Representation of MV Driver Board.

Features And Functions Of The MV Driver Board:

1. Integrated DC/DC Converter with high galvanic isolation (2.5KV) ensures that the user is protected from the high voltage at the secondary side. So, the power supply for the driver remains the same as used in the control board (0/+15V) without the requirement of the isolation. Regulating pulse width modulator UC3525 is used for this purpose.
2. All information that is transmitted between input and output uses proper isolation (optocoupler and ferrite transformer).

3. A high frequency (52KHz) DC/DC Converter provides required isolated power supplies for the four sections. For this, four isolated ferrite transformers are connected in parallel in push-pull configuration.
4. The nominal voltage of the power supply Vs is +15V. Its variation is from 14.5V to 15.2V. The current requirement is lower than 300 mA.
5. Short circuit protection is provided by measuring the collector-emitter voltage with a Vce monitoring circuit. The driver (PC929) detects the short and after a delay (determined by C) and decreases the turn-off speed of the IGBT. Soft Turn-Off under fault conditions is necessary as it reduces the voltage overshoot and allows for a faster Turn-Off during normal operation. In case of the fault both the IGBT's are Turned-Off immediately and an error signal is fed to the control circuit.
6. Two control signals are transmitted to each PCA-1019 from PCA-2007 through Fiber Optics transmitter.
7. Four switching signals for the H-Bridge Cell are generated, with required dead-band time of 4μsec, from this two control signals.
8. The IGBT's are Turned-On by applying a positive gate voltage of +15V and Turned-Off by applying a negative voltage.
9. This MV Driver Board has additional advantages such as Over-Voltage Protection, Under-Voltage Protection and Over-Temperature Protection.
10. In case of any fault, a 555 timer acts as a mono-shot and it blocks the switching signals to IGBT's.
11. In case of any fault is detected, an error signal is transmitted through fiber optic to PCA-2007 board, which blocks control signals transmitted to board PCA-1019. In return an error signal is send to control board PCA-2004A, which gives a reset signal and blinks an FAULT Signal.

Circuit Description:

The MVD board can be divided into five sections:

(i) Power supply (+15V, +5V),

(ii) DC/DC Converter (+15V, -15V),

(iii) Hybrid IGBT Driver,

(iv) Fault Protection Circuit,

(v) Dead-Band Circuit.

(i) POWER SUPPLY :

The +15V supply voltage required for DC/DC Converter, LM339 Comparator IC, TL084 OP-AMP and Buffer ULN2003 is generated by Adjustable Voltage Switching Regulator LM2576. The unregulated vol. to LM2576 is given from a rectifier bridge. The +5V supply required for Fiber-Optic Transceivers and Hex Schmitt-Trigger Inverter IC is generated by Linear Voltage Regulator LM7805.

(ii) DC/DC CONVERTER :

Isolated power supplies required for the TOP and BOTTOM sections are provided by an integrated DC/DC Converter. It receives regulated +15V from the control board at primary side and works in the push-pull configuration to provide +VE (+15V) and –VE (-6.6V) supply at secondary side required for IGBT switching. UC3525 generates the PWM signals for DC/DC Converter. Ferrite transformer is used to transfer the required energy at the output. MOSFET Q1 and Q2 are used for switching. The Toroidal transformer and the rectifier diodes are mounted on PCA-521. The entire assembly is called as ARL-04. The negative supply (-15V) required for TL084 is generated from PCA-521.

(iii) IGBT DRIVER PC929 :

The PC929 Driver from SHARP is used to drive the IGBT. It is designed to convert logic level control signals into optimal IGBT gate drive. Input signals are isolated from the IGBT. It also provides a short-circuit protection by monitoring the collector-emitter voltage Vce of the IGBT. A collector feedback is taken for this purpose. The

driver initiates a controlled slow turn-off and generates a fault signal when a short is detected. The slow turn-off helps to control dangerous transient voltages that can occur when high short circuit currents are interrupted. The output of the driver will remain disabled and the fault signal will remain active for minimum 20 μsec after a short circuit is detected. The input signal of the driver must be in its off state in order for the fault signal to be reset. In order to achieve efficient and reliable operation of high current, high voltage IGBT modules, a gate drive with high pulse current capability and low output impedance is required. The output booster stage is used for this purpose.

(iv) FAULT PROTECTION CIRCUIT :

The fault protection circuit includes Over-Voltage Protection, Under-Voltage Protection, Over-Temperature Protection and Short-Circuit Protection. In case the DC link voltage goes above 788V, an over-voltage fault is initiated; while if the DC link voltage falls below 452V, an under-voltage fault is initiated. The over-temperature fault is active when the temperature goes above 88 ^{0}C. It also provides a short-circuit protection by monitoring the collector-emitter voltage Vce of the IGBT, as explained above. In case detection of any above fault, a low signal is given to Trigger Pin of 555-timer which acts as mono-shot, giving 1 sec pulse and it blocks the switching signals to the ULN2003 and hence to IGBT's. In return, an error signal is transmitted through fiber optic to PCA-2007 board, which blocks control signals transmitted to board PCA-1019.

(v) DEAD-BAND CIRCUIT :

The two control signals from PCA-2007, for left and right leg of H-Bridge are inverted to make four switching signals for four IGBT's of H-Bridge. The inverted switching signals generated have a dead-band time of approximately 4 μsec, which is generated by use of comparators and RC network.

6.2. H-Bridge CELL

Figure 6.2 shows the structural representation of an H-Bridge CELL. The CELL can be divided into four sections :

(i) Diode Bridge Rectifier,
(ii) Soft-Charge Contactor & Resistor,
(iii) DC-link Capacitors and
(iv) H-Bridge IGBT's.

As shown in figure the input to diode bridge rectifier is 440VAC. The capacitor bank gets charged to the desired voltage level through an soft-charge resistor, to avoid large inrush current when capacitors are not charged. When the capacitor bank gets charged to 500Vdc, a soft-charge relay in PCB-1019 operates a soft-charge contactor and bypasses the soft-charge resistor. After the DC-link voltage reaches the desired level, 600Vdc for testing, IGBT gate signals are activated through an Keypad command. The output voltages at different frequencies for different CELL's are shown in the test results.
The testing is done for Single CELL Single-Phase unit for the approval and modification purpose. The test results shows the authentication of the gate pulses that are generated and various PCB's and their outputs. The test results shows the authentication of DSP programming, the Multilevel Interfacing PCB, the dead-band circuit in PCB-1019, Under/Over Voltage protection circuit, Over-temperature protection circuit, etc.

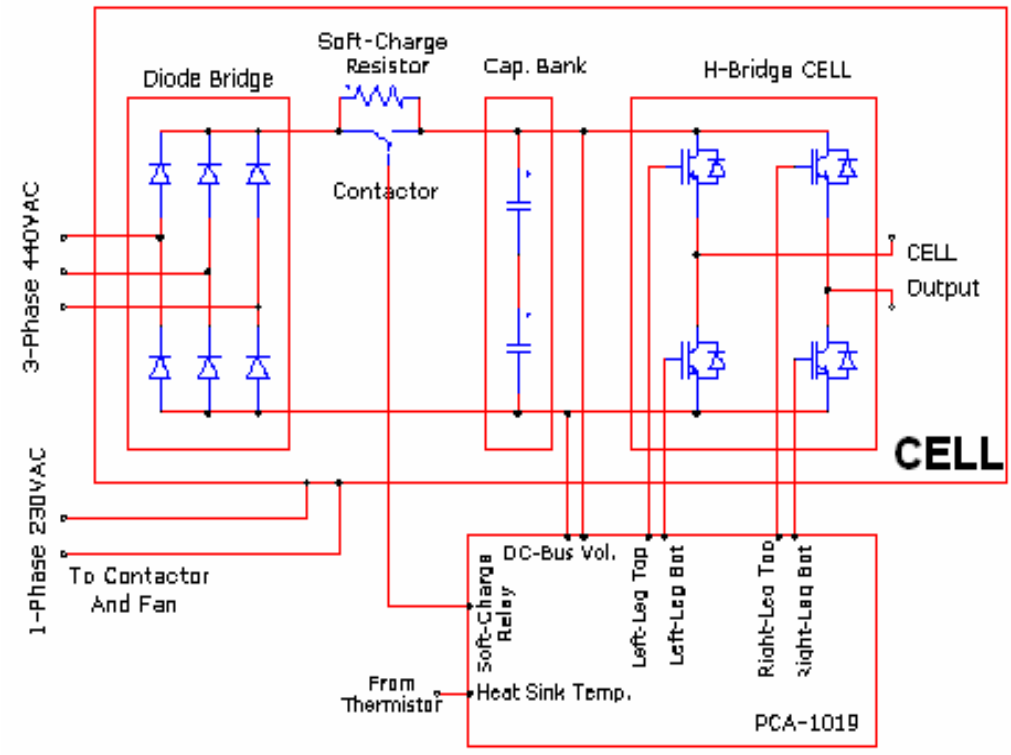


Fig. 6.2 : Representable View of Single CELL Structure

7. TEST RESULTS

7.1 Test Results for PCA-2004A

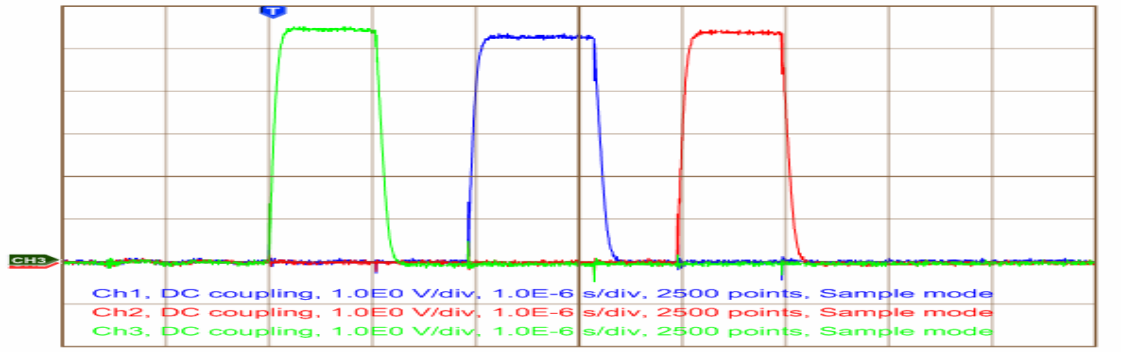


Fig. 7.1.1 : Chip-Select Signal For R-Phase, Y-Phase and B-Phase

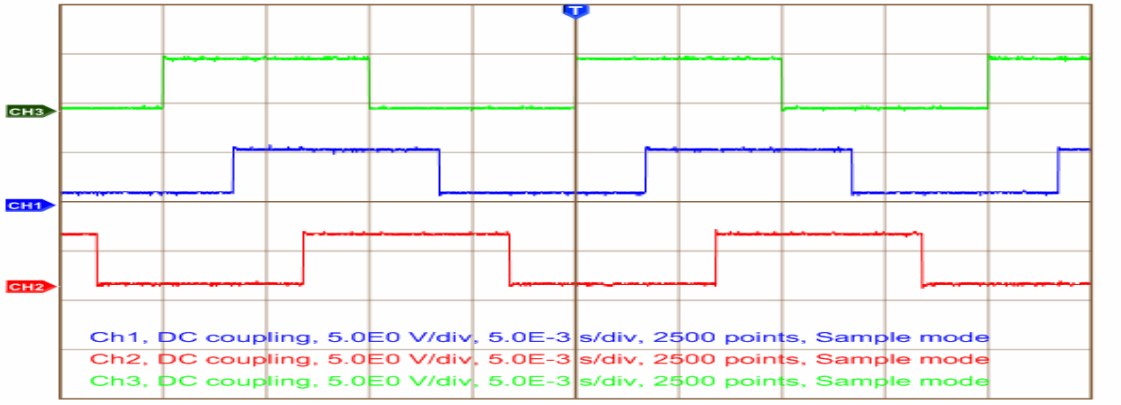
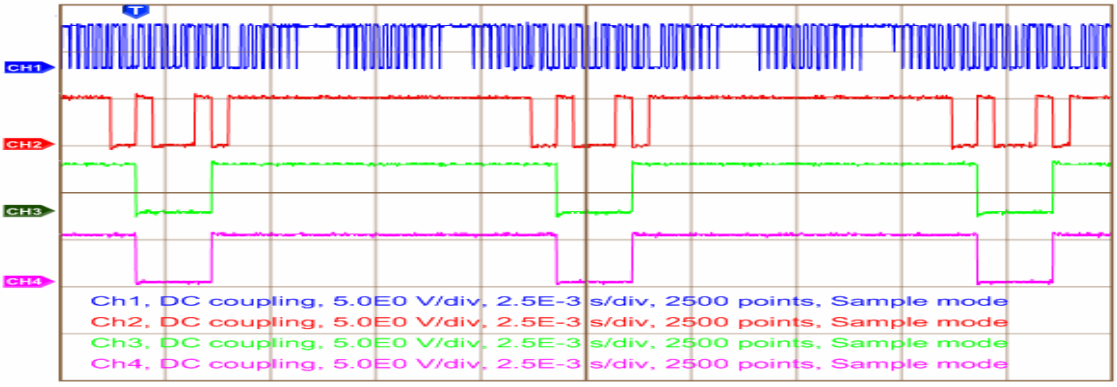


Fig. 7.1.2 : Direction Signals For R-Phase, Y-Phase and B-Phase

7.2 Test Results for PCA-2007



First: CELL-1, Second: CELL-2, Third: CELL-3, Fourth: CELL-4

Fig. 7.2.1 : Signals Generated At Output of Latch & PWM (R-Phase)

Fig. 7.2.2 : Signals Generated At Output of Logic Circuit @ 50 Hz (R-Phase)

Fig. 7.2.3 : Signals Generated At Output of Logic Circuit @ 40 Hz (R-Phase)

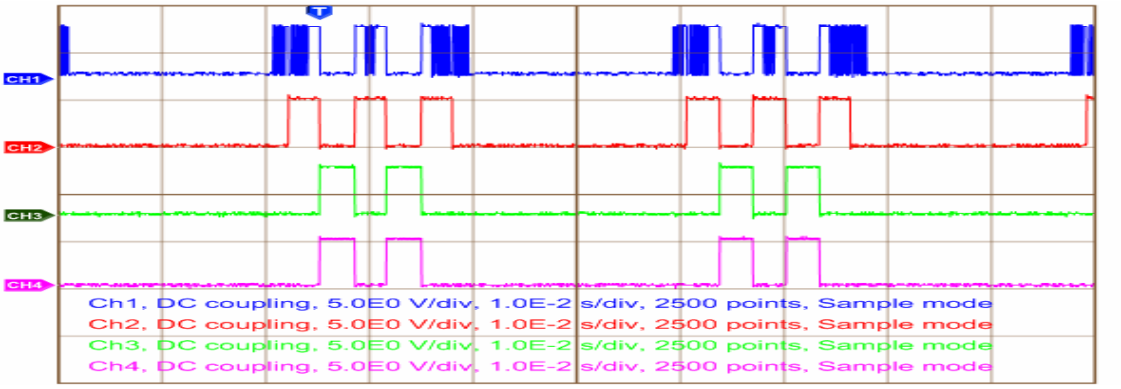


Fig. 7.2.4 : Signals Generated At Output of Logic Circuit @ 26 Hz (R-Phase)

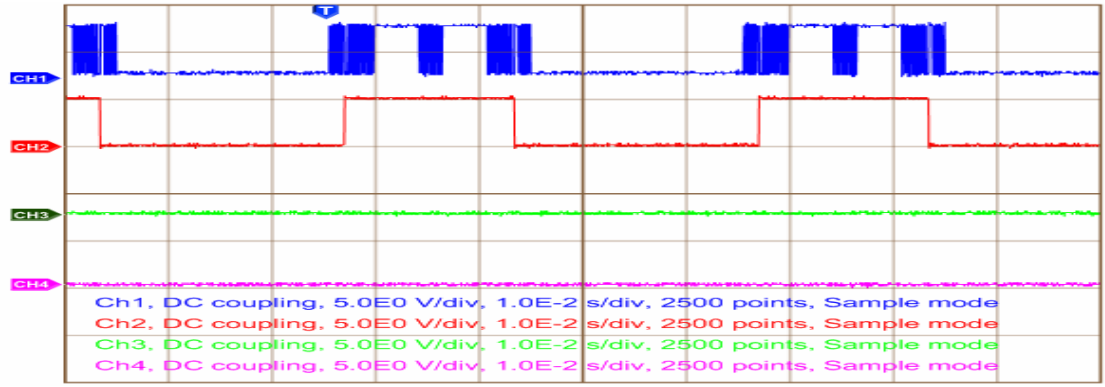


Fig. 7.2.5 : Signals Generated At Output of Logic Circuit @ 25 Hz (R-Phase)

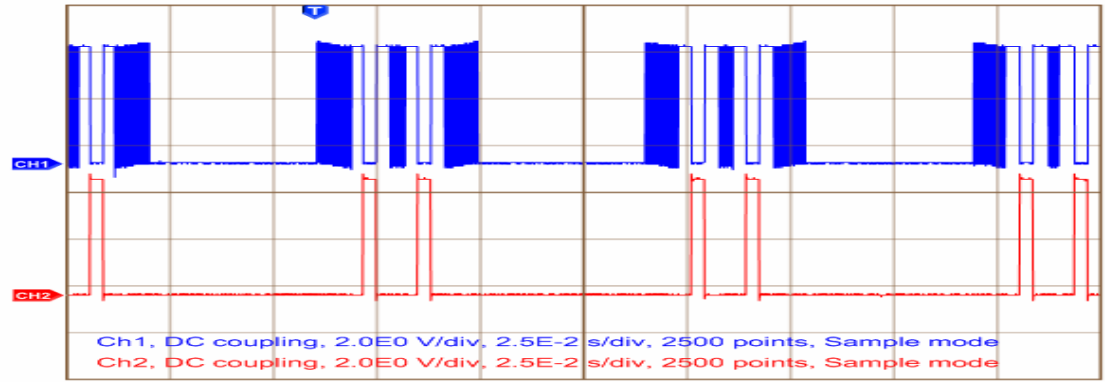


Fig. 7.2.6 : Signals Generated At Output of Logic Circuit @ 12.6 Hz (R-Phase)

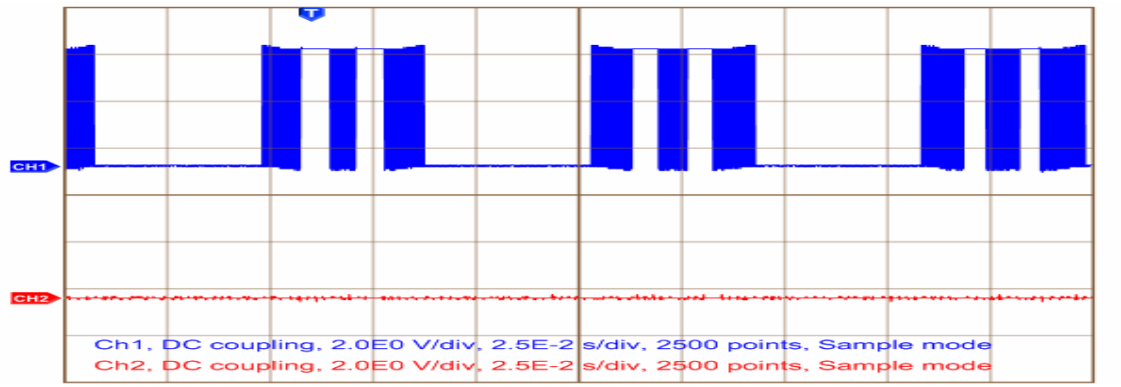
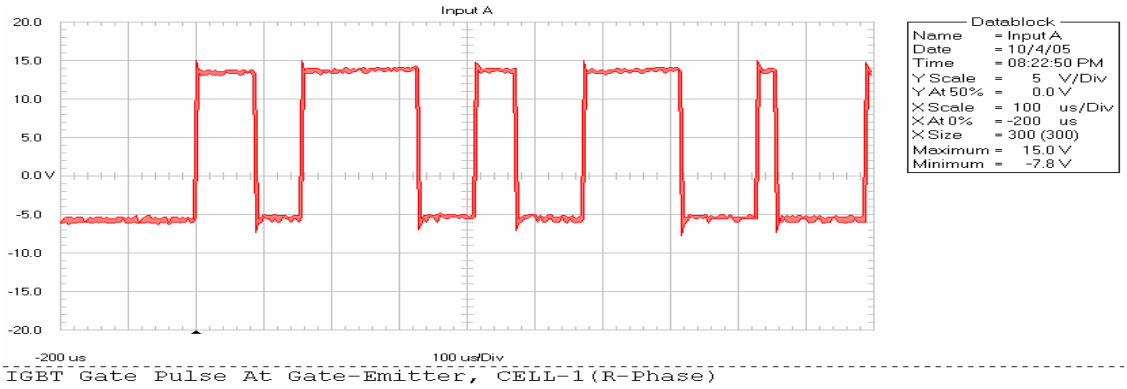
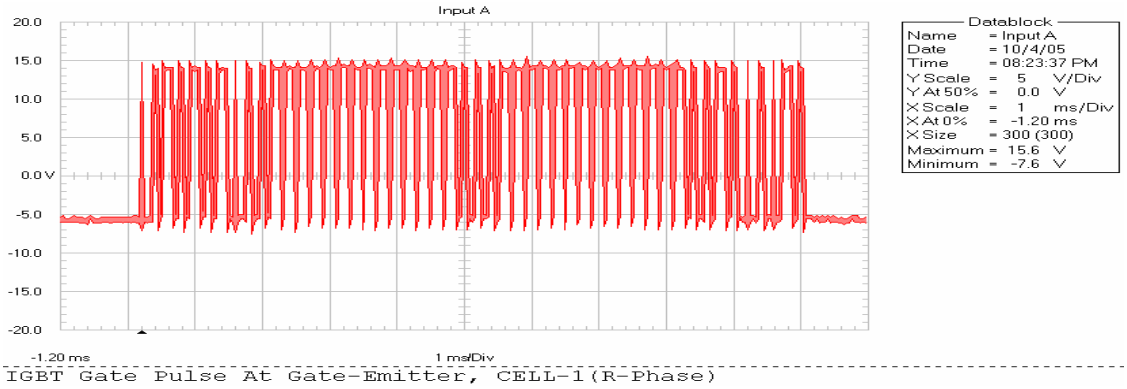


Fig. 7.2.7 : Signals Generated At Output of Logic Circuit @ 12.5 Hz (R-Phase)

7.3 Test Results for PCA-1019



(a.)



(b.)

Fig. 7.3.1 : IGBT Gate Pulse At Gate-Emitter, CELL-1 (R-Phase)

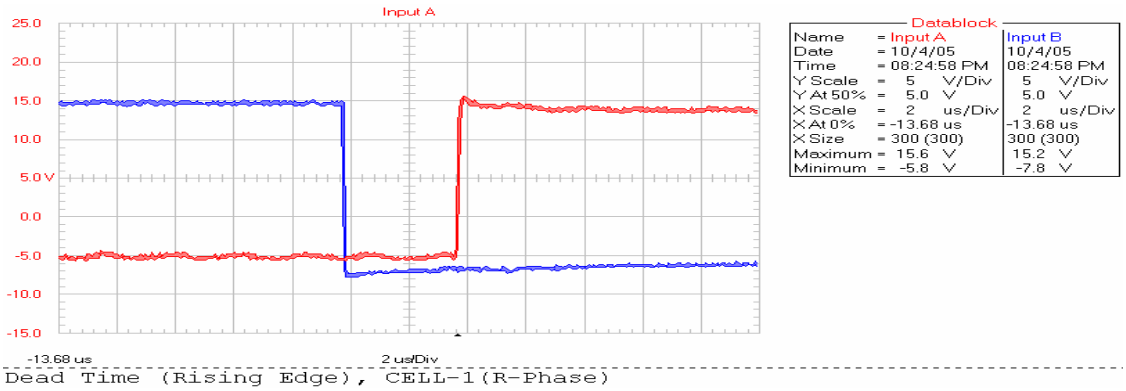


Fig. 7.3.2 : Dead-Time (Rising Edge), CELL-1 (R-Phase)

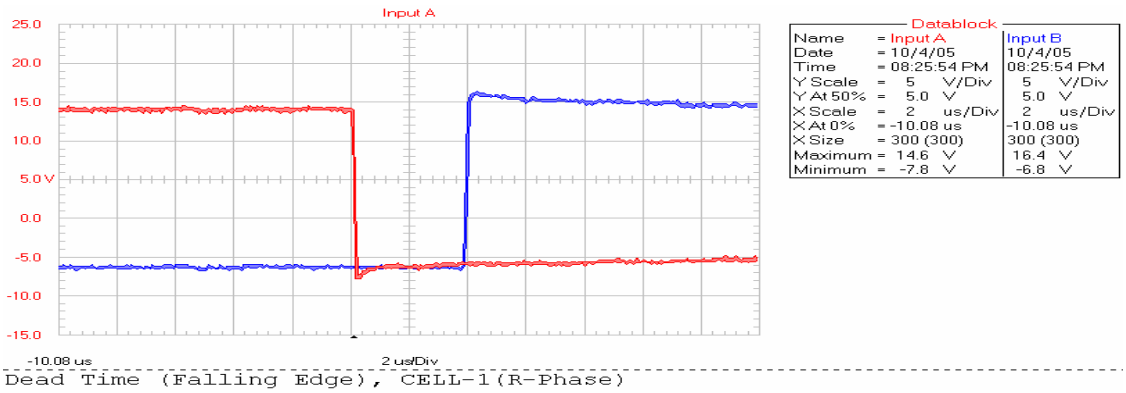


Fig. 7.3.3 : Dead-Time (Falling Edge), CELL-1 (R-Phase)

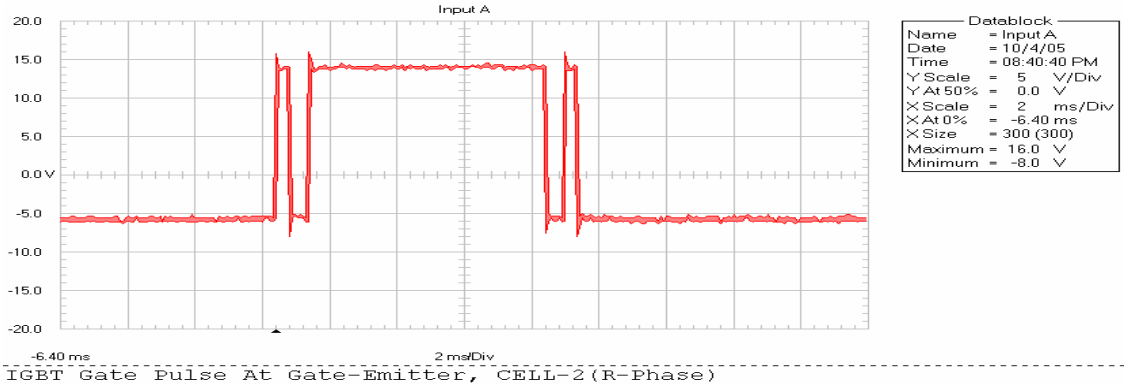


Fig. 7.3.4 : IGBT Gate Pulse At Gate-Emitter, CELL-2 (R-Phase)

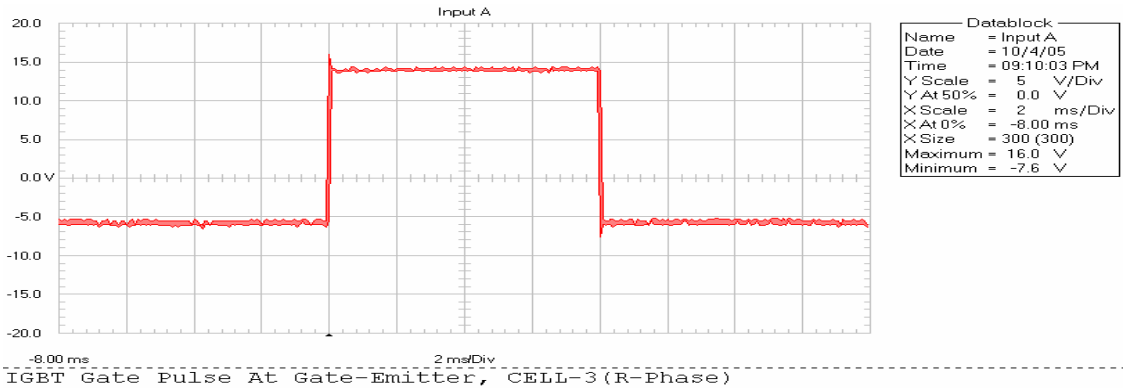


Fig. 7.3.5 : IGBT Gate Pulse At Gate-Emitter, CELL-3 (R-Phase)

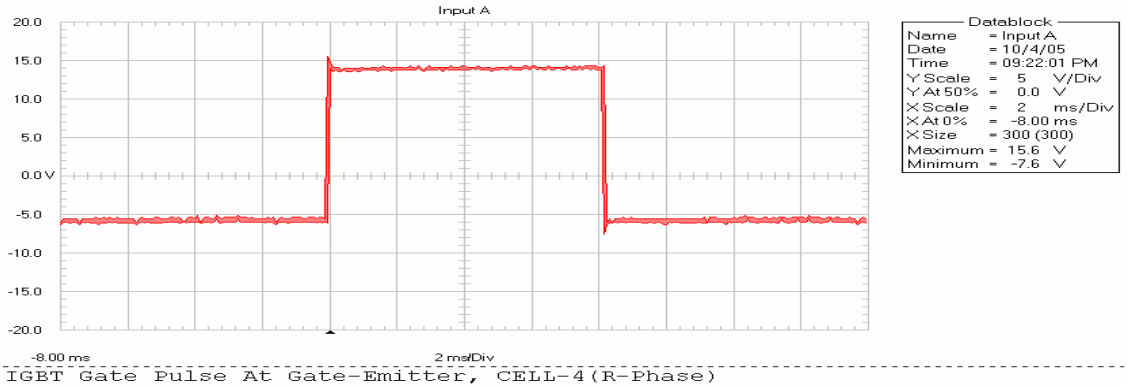


Fig. 7.3.6 : IGBT Gate Pulse At Gate-Emitter, CELL-4 (R-Phase)

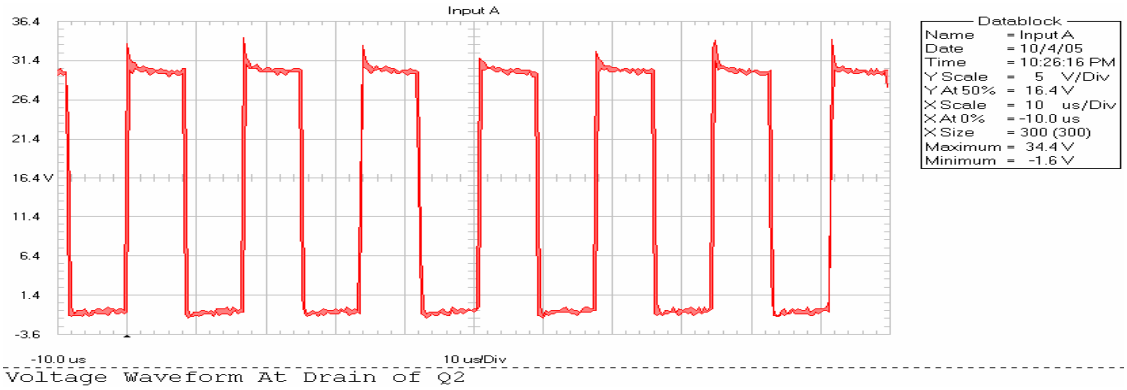


Fig. 7.3.7 : Voltage Waveform At Drain of Q2

7.4 Test Results of H-Bridge CELL

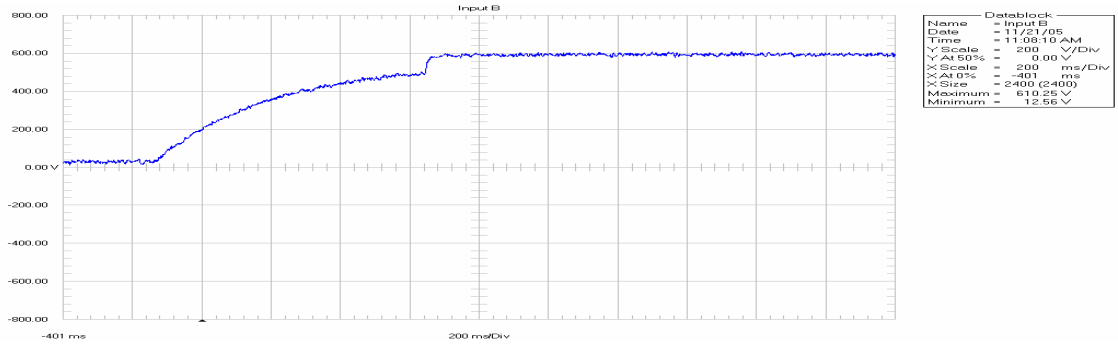


Fig. 7.4.1 : Soft-Charge Voltage Across Capacitor-Bank.

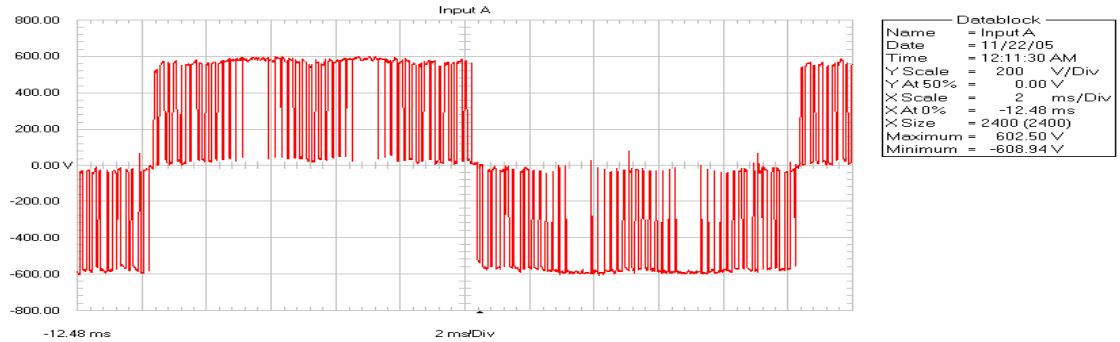


Fig. 7.4.2 : CELL-1 Output Voltage @ 50Hz.

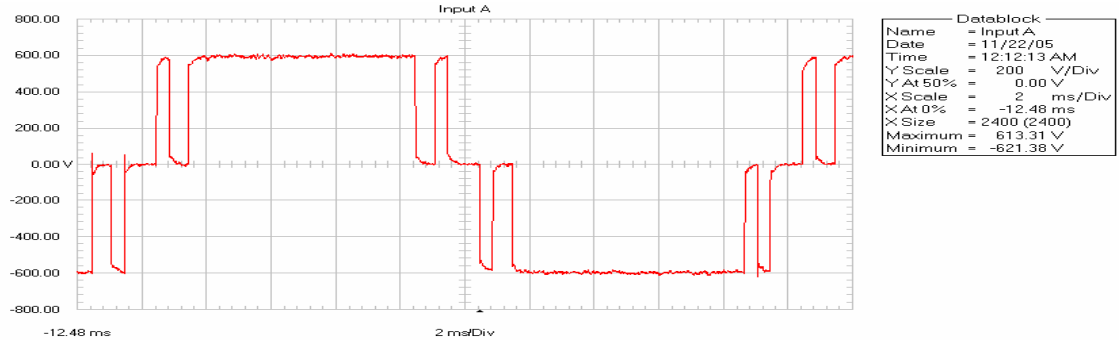


Fig. 7.4.3 : CELL-2 Output Voltage @ 50Hz.

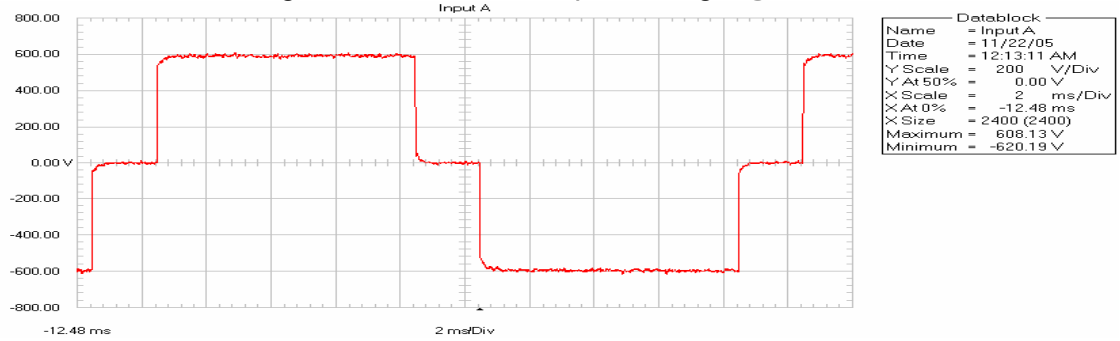


Fig. 7.4.4 : CELL-3 & 4 Output Voltage @ 50Hz.

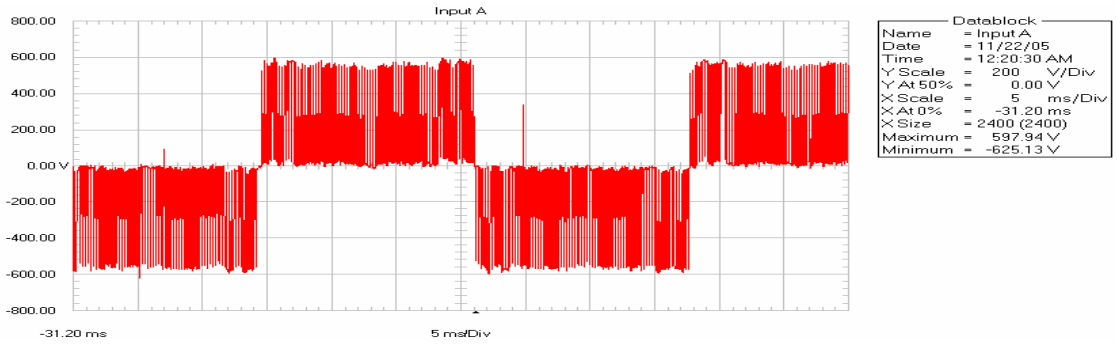


Fig. 7.4.5 : CELL-1 Output Voltage @ 35Hz.

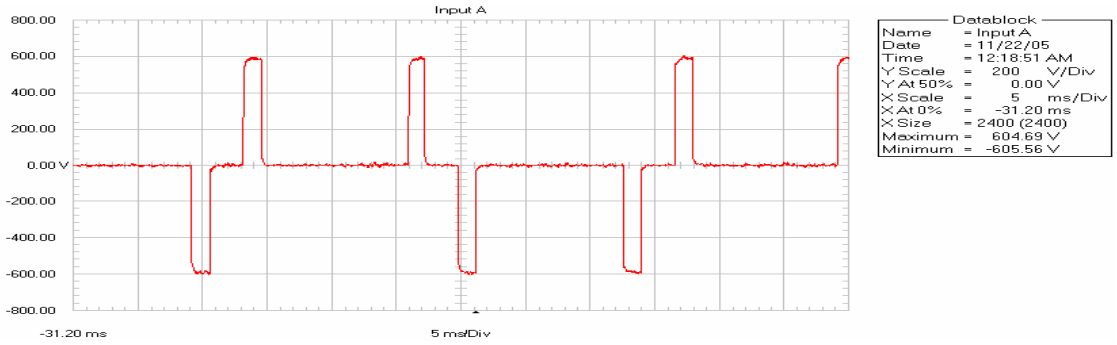


Fig. 7.4.6 : CELL-2 Output Voltage @ 35Hz.

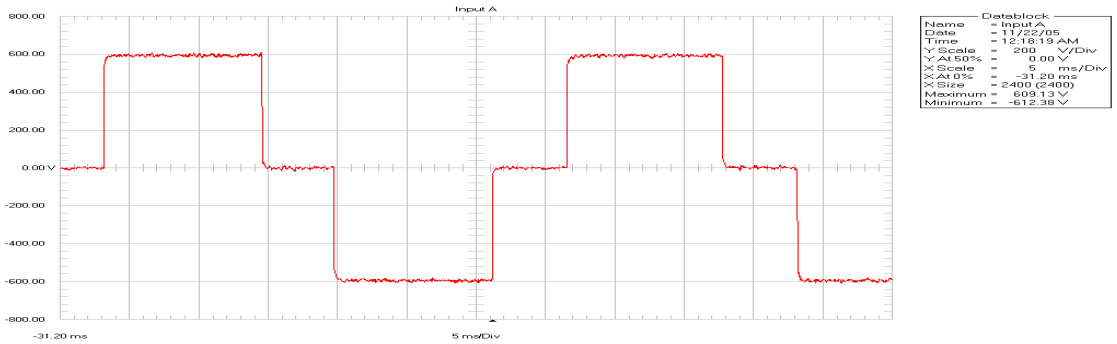


Fig. 7.4.7 : CELL-3 & 4 Output Voltage @ 35Hz.

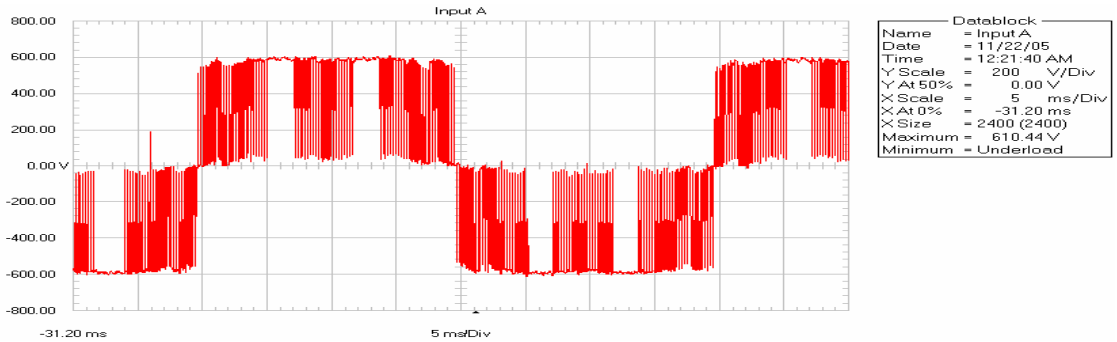


Fig. 7.4.8 : CELL-1 Output Voltage @ 25Hz.

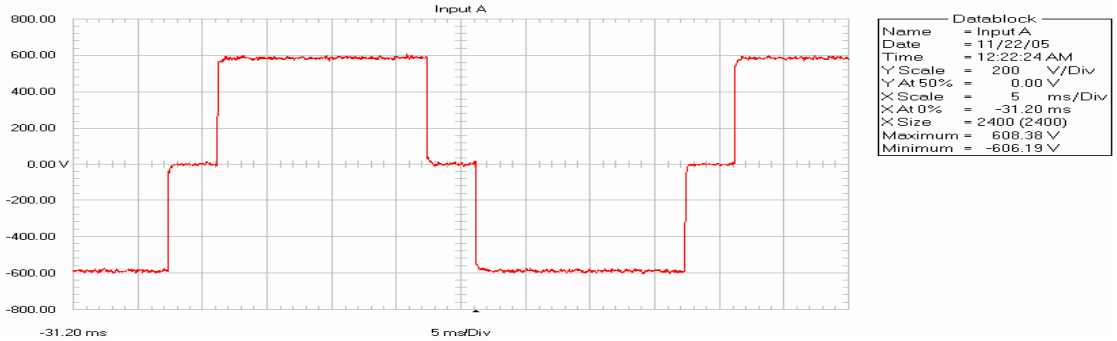


Fig. 7.4.9 : CELL-2 Output Voltage @ 25Hz.

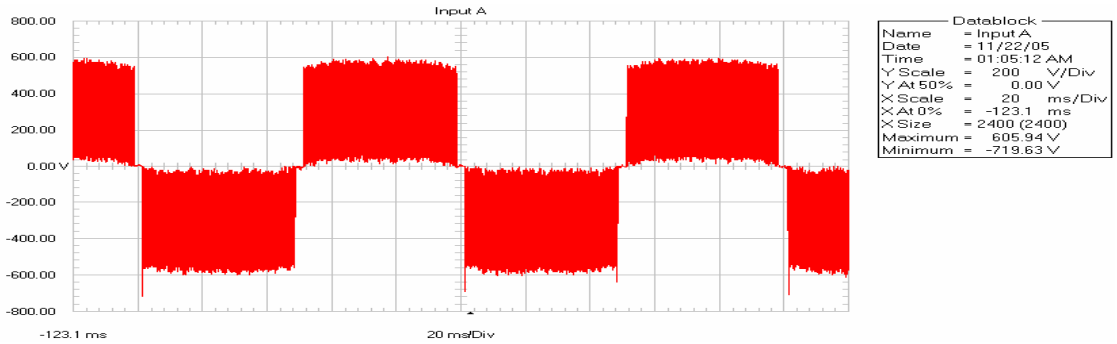


Fig. 7.4.10 : CELL-1 Output Voltage @ 10Hz.

8. CONCLUSION & FUTURE WORK

CONCLUSION:

The multi-level inverter provides a break through in the drive technology in medium voltage range with low THD, less dv/dt voltage stresses, good quality source currents, higher efficiency, good power factor, etc.

The simulation results show that by using novel space-vector algorithm, one can solve the problem of voltage unbalance in diode-clamped multi-level inverter. By comparing the PSIM simulation results of diode-clamped multi-level inverter and H-Bridge multi-level inverter, one can conclude that the later is more advantageous then the former in terms of simple switching algorithm, simple CELL structure, no dc-link voltage unbalance, less number of components requirement for same levels of output, easily extendable design, easy commercialization, etc.

The gate signals generated from the PCB's provide an proof for the authentication of the gate signals that are being generated by simulation.

The prototype model of single-phase one CELL provides us with an brief idea of the multi-level inverter.

FUTURE WORK:

- Testing of 3-Phase 9-Level inverter structure with 12-CELL modules.
- Selection of proper design of the isolation 24-pulse transformer.
- Modifying the PCB design of PCA-1019 with includes DSP.
- PCB designing and testing of the new firing topology in H-Bridge.
- Commercialization of MVD.

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APPENDIX - A

Specifications of motor model:

Name plate data :

Power rating : 2.2kw

Frequency : 50Hz

Rated voltage : 415V

Rated current : 5A

No.of.Poles : 4

Parameters :

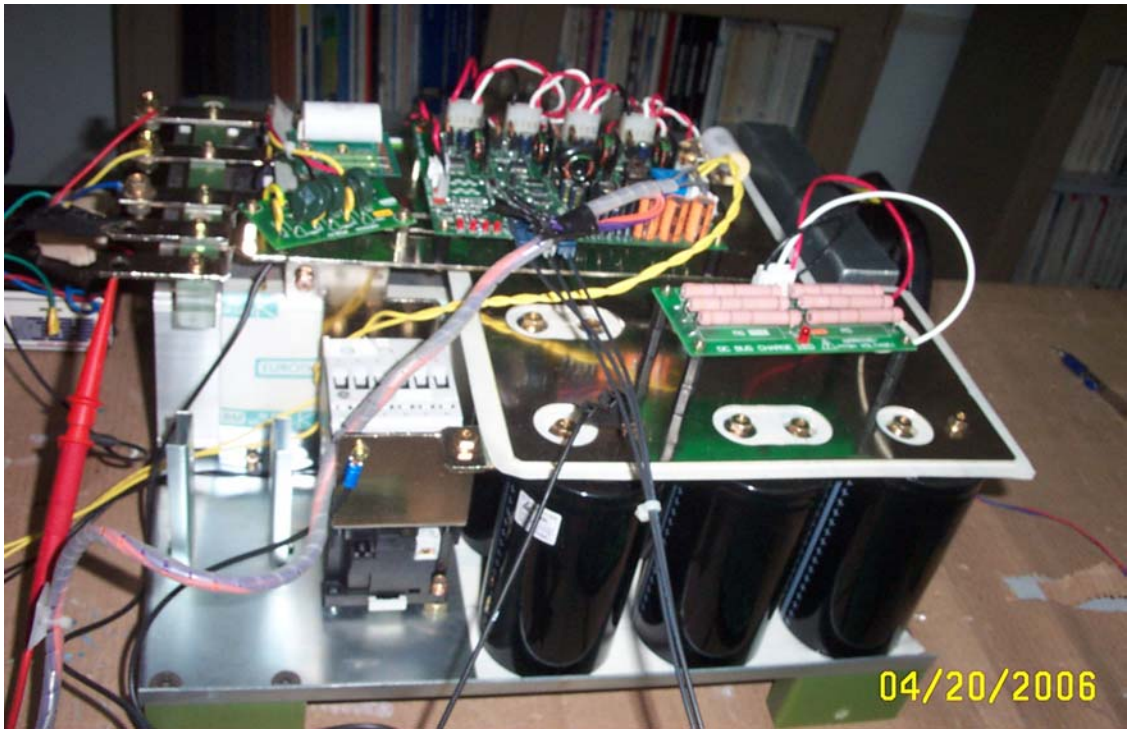
R1 = 2.3Ω ; R2 = 2.33 Ω ; X1 = X2 = 4.46 Ω ; Xm = 76.3 Ω ; J = 0.0089kg – m^2.

APPENDIX – B

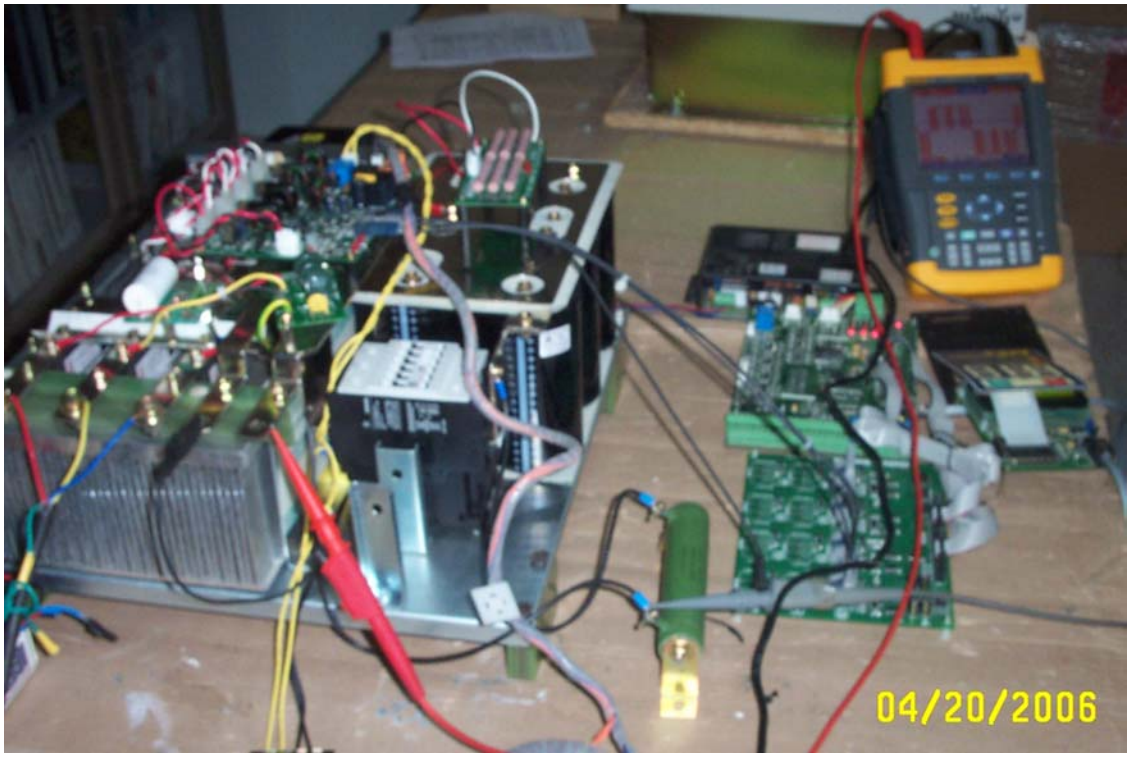
PCB-2004A

PCB-2007

PCB-1019



Single H-Bridge CELL



Experimental Setup