"DESIGN & DEVELOPMENT OF COST EFFECTIVE SMPS WORKING ON HIGH INPUT VOLTAGE"

A Major Project Report

Submitted in Partial Fulfillment of the Requirements

for Degree of

MASTER OF TECHNOLOGY

IN

ELECTRICAL ENGINEERING

(POWER APPARATUS & SYSTEMS)

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Certificate

This is to certify that the Major Project Report entitled "**Design & Development of cost effective SMPS working on High Input Voltage**" submitted by **Mr.Himanshu Dipakchandra Upadhyay (04MEE020)**, towards the partial fulfillment of the requirements of Master of Technology (Electrical Engineering) in the field of Power Apparatus & Systems of Nirma University of Science and Technology is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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HIMANSHU UPADHYAY

ABSTRACT

In this era due to Power electronics revolution, people have very efficient tools to solve problems of having DC voltage to power the Electronics Devices. Every new electronic product, except those that are battery powered, requires converting off–line 115 Vac or 230 Vac power to some dc voltage for powering the electronics.

Efficient conversion of electrical power is becoming a primary concern to companies and to society as a whole. Switching power supplies offer not only higher efficiencies but also offer greater flexibility to the designer. Recent advances in semiconductor, magnetic and passive technologies make the switching power supply an ever more popular choice in the power conversion arena today.

In the industries nowadays three phase supply is a prime need for their utility. Power controllers, AC Drives, DC Drives are the major devices used for different purposes.

As SMPS have very efficient performance, not to keep it –limited to lower voltage input range, but can be introduce it for the higher voltage inputs and enhance its versatility.

Now the aim is to fabricate the cost effective SMPS working on High input voltage. This is facilitates with following advantages.

- Most reliable
- Compact Design
- Low (audible) noise
- Very High Efficiency
- Cost effective solution

With this MATLAB simulations and fabricated SMPS Testing results are included.

NOMENCLATURE

✓ Abbreviations:-

B-B	Buck Boost
CM	Circular Miles
DEFC	Double Ended Forward Converter
EMF	Electro Motive Force
MOS	MOSFET
MFD	Micro Farad
PWM	Pulse Width Modulation
SMPS	Switched Mode Power Supply
TI	Texas Instruments

✓ Symbols:-

V_{in}	Input Voltage
V_{out}	Output Voltage
I_{out}	Output Current
I_{in}	Input Current
T_{on}	ON(Conduction) Time
T_{off}	OFF(Delay) Time
V_{drop}	Voltage Drop
I_{load}	Load Current
D	Duty Cycle
S_i	i^{th} Switch
V_{dc}	DC Voltage
V_{Master}	Output Voltage of Master Secondary.
V_{Slave}	output Voltage Slave Secondary
$V_{Dc,\min}$	Minimum DC Link Voltage

- $V_{Dc,\max}$ Maximum DC Link Voltage
- V_{ms} Max Voltage Stress Allowable
- E Emf
- N Number of Turns
- A_e Core Area
- $I_{av,\ primary}$ Average Primary Current
- δ Duty Cycle
- N_p Primary turns
- N_m Master Secondary turns
- N_s Slave Secondary turns
- V_{BE} Base- Emitter Voltage

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Chapter-1

INTRODUCTION

1.1 History

Historically, the linear regulator was the primary method of creating a regulated output voltage. It operates by reducing a higher input voltage down to the lower output voltage by linearly controlling the conductivity of a series pass power device in response to changes in its load. This results in a large voltage being placed across the pass unit with the load current flowing through it.

This headroom loss (V_{drop}* I_{load}) causes the linear regulator to only be 30 to 50 percent efficient. That means that for each watt delivered to the load, at least a watt has to be dissipated in heat. The cost of the heat sink actually makes the linear regulator uneconomical above 10 watts for small applications. Below that point, however, they are cost effective in step-down applications.

1.2 Overview of SMPS

The switching regulator operates the power devices in the full-on and cut-off states. This then results in either large currents being passed through the power devices with a low "on" voltage or no current flowing with high voltage across the device. This results in a much lower power being dissipated within the supply. The average switching power supply exhibits efficiencies of between 70 to 90 percent, regardless of the input voltage.

Higher levels of integration have driven the cost of switching power supplies downward which makes it an attractive choice for output powers greater than 10 watts or where multiple outputs are desired.

So Switched Mode Power Supply's popularity increased due to its tremendous advantages of high power conversion efficiency and increased design flexibilities.

1.3 Basics of SMPS

The Switched Mode Power Supply is essentially a dc to dc converter with control of the output voltage magnitude. Generally in the low and medium power application a Switched Mode Power Supply provides required DC power supply with negligible AC ripples.

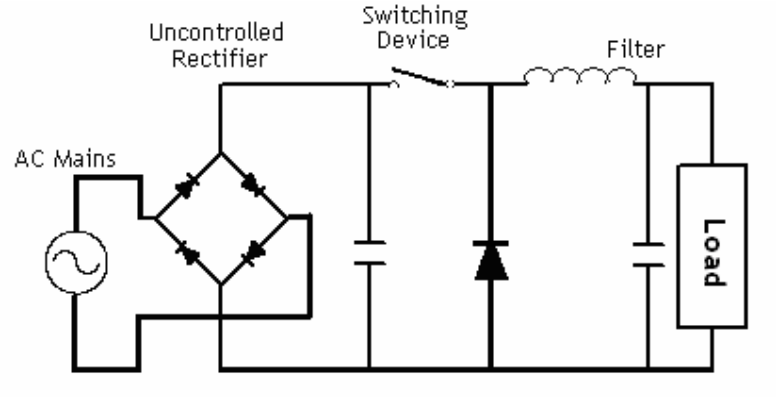


FIG: 1.1: Switched Mode Power Supply

1.4 Operation of SMPS

As we provide mains to the Switched Mode Power Supply – input it will be rectified by diode bridge rectifier followed by output capacitor that will provide constant DC voltage. The switch is turned on & off rapidly to give a voltage which is chopped between voltage level and zero. Chopped voltage is fed into *LC filter* network which than smoothes the chopped waveform to give a level voltage to the load. By switching the rectifier output very rapidly on & off control of output voltage is obtained. The magnitude is dependent on the duty cycle of the device.

Chapter-2

TOPOLOGIES OF SMPS

A topology is the arrangement of the power devices and their magnetic elements. Each topology has its own merits within certain applications. Some of the factors which determine the suitability of a particular topology to a certain application are:

1) Is the topology electrically isolated from the input to the output or not.
2) How much voltage appears across the power semiconductors?
3) Are multiple outputs required?
4) Buck or Boost application.

2.1 Buck Converter

The basic circuit configuration used in the buck converter is shown in the FIG 2.1. As you can see there are only four main components: Switching power MOSFET Q1, flywheel diode D1, inductor L and output filter capacitor C1. A control circuit (often a single IC) monitors the output voltage, and maintains it at the desired level by switching Q1 on and off at a fixed rate (the converters operating frequency), but with a varying duty cycle (the proportion of each switching period that Q1 is the input source through Q1 and L, and then into C1 and the load. The magnetic field in L therefore builds up, storing energy in the inductor - with the voltage drop across L opposing or bucking part of the input voltage.

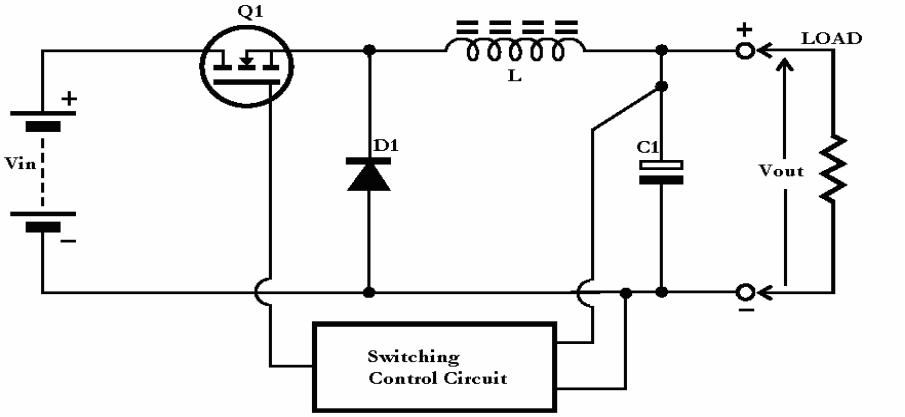


FIG: 2.1: Buck Converter

Then when Q1 is turned off, the inductor opposes any drop in current by suddenly reversing its EMF, and now supplies current to the load itself via D1. Without going too deeply into its operation, the DC output voltage which appears across the load is a fraction of the input voltage, and this fraction turns out to be equal to the duty cycle. So we can write:

$$\frac{V_{out}}{V_{in}} = D \tag{2.1}$$

Where D is the duty cycle, and equal to T_{on}/T, where T is the inverse of the operating frequency. So by varying the switching duty cycle, the buck converters output voltage can be varied as a fraction of the input voltage. A duty cycle of 50% gives a step-down ratio of 2:1, for example, as needed for a 24/12V step-down converter. And current ratio between output and input comes out to be the reciprocal of the voltage ratio - ignoring losses for a moment, and assuming our converter is perfectly efficient. So a quick rule of thumb is:

$$\frac{I_{out}}{I_{in}} = \frac{V_{in}}{V_{out}} \tag{2.2}$$

So when we are stepping down the voltage by 2:1, the input current is only half the value of the output current. Or it would be, if it were not for the converter's losses. Because real-world converters aren't perfect the input current is typically at least 10% higher than this.

2.2 Boost Converter

The basic boost Switched Mode Power Supply is no more complicated than the buck converter, but has the components arranged differently (shown in the FIG: 2.2) in order to step up the voltage. Again the operation consists of using Q1 as a high speed switch, with output voltage control by varying the switching duty cycle.

When Q1 is switched on, current flows from the input source through L and Q1, and energy is stored in the inductor's magnetic field. There is no current through D1, and the load current is supplied by the charge in C1. Then when Q1 is turned off, L opposes any drop in current by immediately reversing its EMF -so that the inductor voltage adds to (i.e., boosts) the source voltage, and source through L, D1 and the load, recharging C1 as well. The output voltage is therefore higher than the input voltage, and it turns out that the voltage step-up ratio is equal to:

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D)} \tag{2.3}$$

Where 1-D is actually the proportion of the switching cycle that Q1 is off, rather than on. So the step-up ratio is also equal to:

$$\frac{V_{out}}{V_{in}} = \frac{T}{T_{off}} \tag{2.4}$$

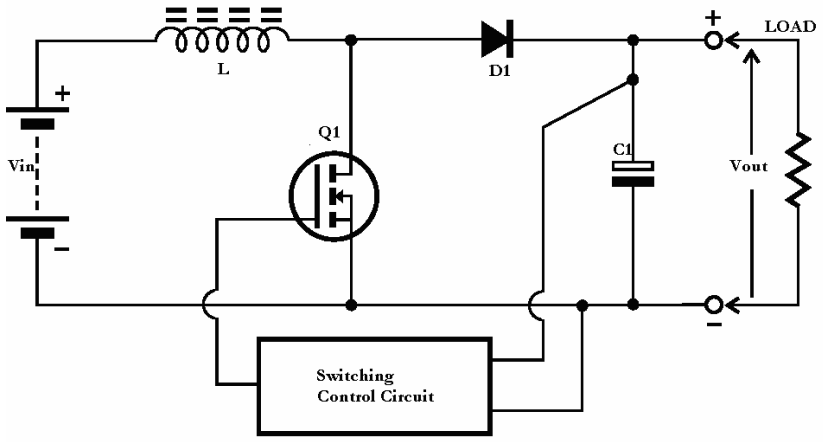


FIG: 2.2: Boost Converter

If you work it out, you find that a 2:1 step-up ratio is achieved with a duty cycle of 50% ($T_{on} = T_{off}$), while a 3:1 step-up needs a duty cycle of 66%. Again, if we assume that the converter is 100% efficient the ratio of output current to input current is just the reciprocal of the voltage ratio:

$$\frac{I_{in}}{I_{out}} = \frac{V_{out}}{V_{in}} \tag{2.5}$$

So if we step up the voltage by a factor of 2, the input current will be twice the output current. Of course in a real converter with losses, it will be higher again.

2.3 Buck-Boost Converter

The main components in a buck-boost converter are again much the same as in the buck and boost types, but they are configured in a different way again (shown in the FIG 2.3).

This allows the voltage to be stepped either up or down, depending on the duty cycle. Here when MOSFET Q1 is turned on, inductor L is again connected directly across the source voltage and current flows through it, storing energy in the magnetic field. No current can flow through D1 to the load, because this time the diode is connected so that it is reverse biased. Capacitor C1 must supply the load current in this T_{on} phase.

But when Q1 is turned off, L is disconnected from the source. Needless to say L again opposes any tendency for the current to drop, and instantly reverses its EMF. This generates a voltage which forward biases D1, and current flows into the load and to recharge C1. With this configuration the ratio between the output and input voltages turns out to be:

$$\frac{V_{out}}{V_{in}} = -\frac{D}{(1-D)} \tag{2.6}$$

This again equates to

$$\frac{V_{out}}{V_{in}} = -\frac{T_{on}}{T_{off}} \tag{2.7}$$

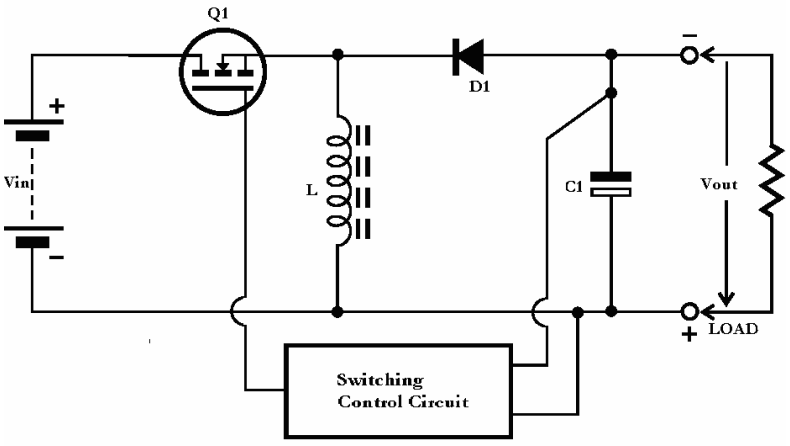


FIG: 2.3: Buck-Boost Converter

So the buck-boost converter steps the voltage down when the duty cycle is less than 50% (i.e., $T_{on} < T_{off}$), and steps it up when the duty cycle is greater than 50% ($T_{on} > T_{off}$). But note that the output voltage is always reversed in polarity with respect to the input - so the buck-boost converter is also a voltage inverter. When the duty cycle is exactly 50%, for example, V_{out} is essentially the same as V_{in} - except with the opposite polarity. So even when it is not being used to step the voltage up or down, the buck boost converter may be used to generate a negative voltage rail in equipment operating from a single battery.

As before, the ratio between output and input currents is simply the reciprocal of the voltage ratio, if we ignore losses.

2.4 Flyback Converter

All above converters looked at so far have virtually no electrical isolation between the input and output circuits; in fact they share a common connection. This is fine for many applications, but it can make these converters quite unsuitable for other applications where the output needs to be completely isolated from the input. Here is where a different type of topology tends to be used -the isolating type.

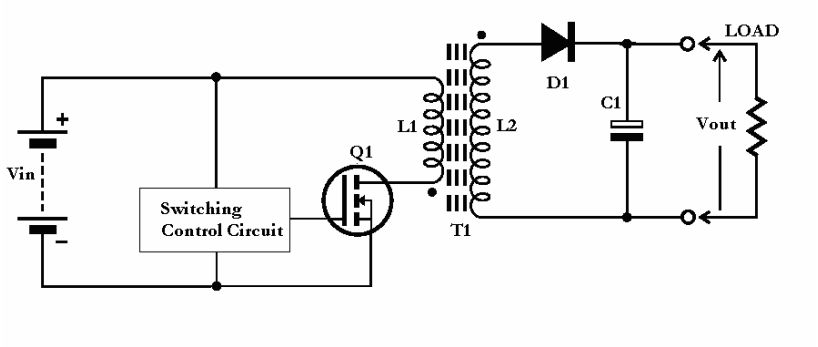


FIG: 2.4: Flyback Converter

The flyback converter can be developed as an extension of the Buck-Boost converter. Above Figure 2.4 shows the basic converter; in the B-B Fig replaces the inductor by a transformer. The buck-boost converter works by storing energy in the inductor during the ON phase and releasing it to the output during the OFF phase. With the transformer the energy storage is in the magnetisation of the transformer core. To increase the stored energy a gapped core is often used.

When MOSFET Q1 is switched on, current flows from the source through primary winding L1 and energy is stored in the transformer's magnetic field. Then when Q1 is turned off, the transformer tries to maintain the current flow through L1 by suddenly reversing the voltage across it-generating a Flyback pulse of back-EMF.

In the case of transformer design main attention is to be paid for flyback converter. The ratio between output and input voltage of a flyback converter is not simply a matter of the turn's ratio between L2 and L1, because the back-EMF voltage in both windings is determined by the amount of energy stored in the magnetic field, and hence depends on the winding inductance, the length of time that Q1 is turned on, etc. However the ratio between L2 and L1 certainly plays an important role, and most Flyback converters have a fairly high turn's ratio to allow a high voltage step-up ratio.

Because of the way the Flyback converter works, the magnetic flux in its transformer core never reverses in polarity. As a result the core needs to be fairly large for a given power level, to avoid magnetic saturation. Because of this Flyback converters tend to be used for relatively low power applications-like generating high voltages for insulation testers, Geiger counter tubes, cathode ray tubes and similar devices drawing relatively low current.

If third small winding is added in the transformer secondary, that can be allowed to sense Flyback pulse amplitude (should be reasonably close to output voltage V_{out}).This voltage can be allowed to fed to MOSFET switching control circuit to allow it to automatically adjust the switching and regulate the output voltage.

2.5 Forward Converter

The forward converter topology is shown in FIG 2.5. It is the most widely used topology in its range of 150-200W power output with maximum DC input voltage ranges 60-200V. The forward topology is the member of Push-pull family. In Push-pull there are two transistors, here it is having only one and hence the problem of flux imbalance is shorted out.

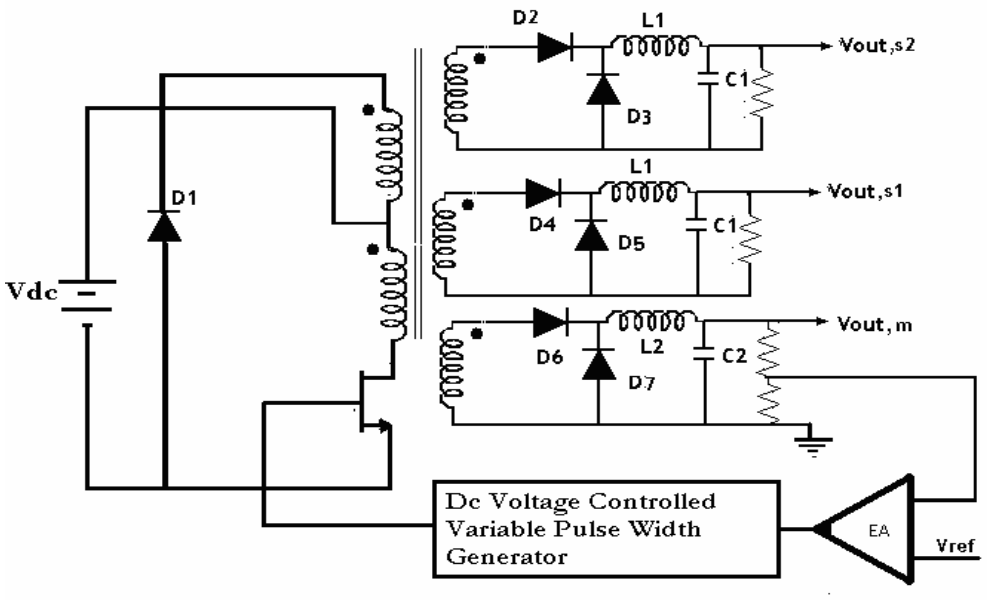


FIG: 2.5 Forward Converter.

Here with forward converter we can have multiple output-via transformers. One Master followed by two slaves. The output of master is fed back to switching control circuit in order to obtain constant regulated output at master and slave secondary. Master output is used to regulate the switching of Electronic-switching device and slave outputs are dependent upon the switching of the device.

The power flows to the loads when the power transistor Q is turned on. Thus converter is termed as Forward Converter.

For the purpose of High Voltage input, if we use this topology, magnetic point of view it has no problem. Here short coming of flux imbalance is no present. But the FIG 2.5.1 shows there will be more than 2 times DC voltage will come across the Power Transistor Q, when it would be OFF.

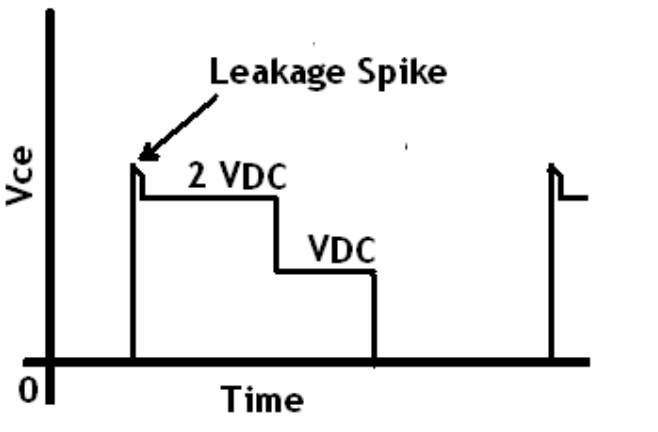


FIG: 2.5.1 Waveform across Transistor (Vce)

So for our purpose if we use this topology, we need High rating Device since, *off state* voltage stress appears across the Collector-Emitter terminal becomes more than double voltage of DC Link voltage. So use of this Topology can be no longer Economical.

2.6 Double Ended Forward Converter

The double ended forward converter topology is the member of Push Pull Class. The push pull converter provides isolated output feature, which was not there in Buck, Boost converters. Means its output returns are DC-isolated from input returns. But it has the leakage inductance effect in its transformer windings, so due to it the leakage inductance spike is present extra in the measure of break down voltage calculation. That is the criterion of selecting the switching Device. So the rating require be higher & higher and the same way the cost of the Switching device too. And that topology was using the transistor it had the problem of flux imbalance and due to which transistor was failing.

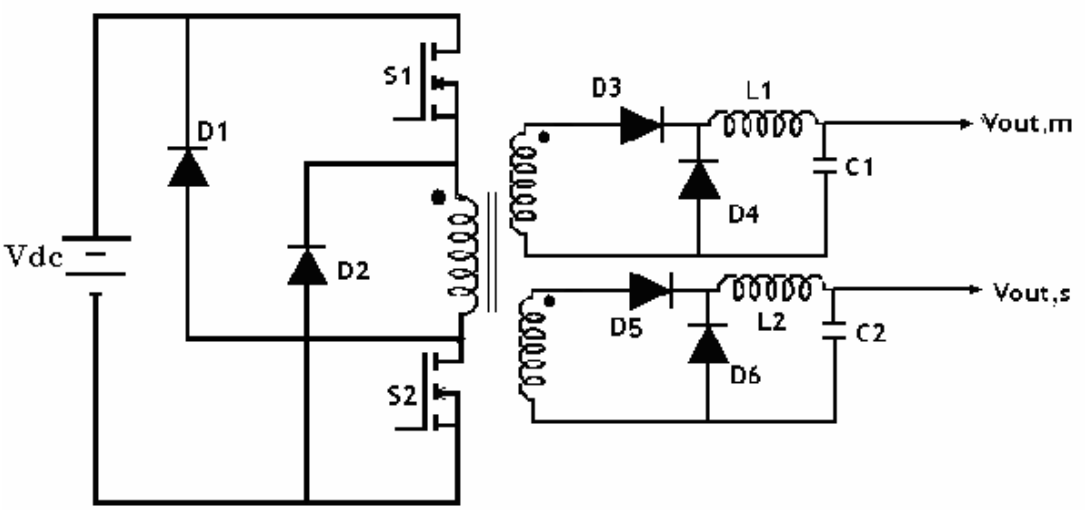


FIG: 2.6 Double Ended Forward Converter.

These two problems are overcome in new topology, Double Ended Forward Converter. The very basic diagram is as shown in Figure 2.6.

Although it has two switching devices rather than one compared with the forward converter, it has very significant advantage. In the off stage, both the switches are subjected to only DC input voltage rather than twice that as in the single ended forward converter. Further, at turnoff, there is *no leakage inductance spike.*

Although there are two switches with break down voltage rating 1000V which can take that stress, it is a far more reliable design to use the double ended forward

converter with half the off voltage stress. Reliability is of overriding importance in the power supply design.

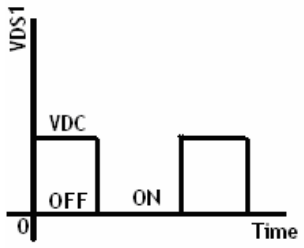


FIG :2.6.1

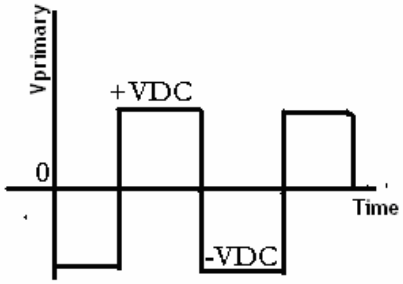


FIG :2.6.3

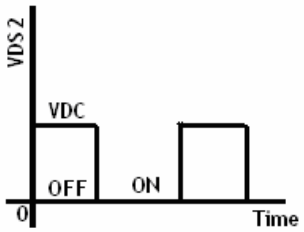


FIG :2.6.2

The FIG: 2.6.1 and 2.6.2 are the waveform across the Switch, and FIG: 2.6.3 shows the voltage waveform across the primary of transformer. From these waveforms it is very clear that with this topology OFF State voltage across the switch is just the same as the DC supply source voltage. So this can lead to the economic choice of the Switching Device. So for our purpose all requirements are met here. So Topology can be followed.

2.6.1 Operation

Double Ended Forward Converter works as follows. The Switches S_1 and S_2 are series with the top and bottom of the transformer primary. Both of these MOSFETs are turned on simultaneously and turned off simultaneously. When they are on, primary and secondary dots are positive and power is delivered to the loads. When they turn off, current stored in the magnetizing inductance reverses the polarity of all windings. The dot end of primary winding tries to go far negative but is caught at ground by the Diode D_2. The no dot end of primary tries to go far positive but caught at V_{dc} by Diode D_1. The drain of S_1 can never be more than V_{dc} below its source, and the source of the S_2 can never be more than V_{dc} above its drain. Leakage voltage spikes are clamped so that the maximum voltage stress on either Switch can never be more than the Maximum DC input voltage.

Chapter-3

PROPOSED SCHEMES

We have viewed some of the topologies of the Switched Mode Power Supply, conventionally used for our general domestic or industrial purpose. We need the Power Supply with perfect regulation and with a wide range of input. That should be cost effective to compete in the Market.

So presently available topologies are to be modified as per our needs in order to utilize them better way and execute our requirements of SMPS more effectively.

Our purpose of SMPS is to work on High input DC voltage and it should provide the control supply. Mainly this high DC voltage input will be the DC link voltage from the Drives, and output from the SMPS (Regulated Power Supply) will be the Control Supply for Drives. So these will eliminate bulky Transformers and drives would be compact, light and more efficient.

Closely suitable topologies among the previously discussed are: forward and Flyback. But the new topology Double ended forward converter is more efficient and economic. In the case of Flyback we can experiment with a huge device or two different special Switches (Discussed later).

3.1 DEFC Scheme

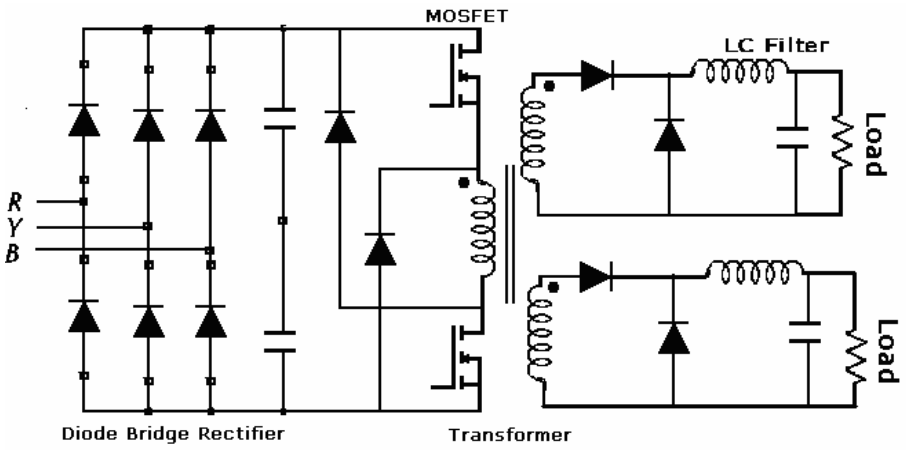


FIG: 3.1 Double Ended Forward Converter.

This scheme is proposed due to its special arrangement of switching devices Diodes and transformer. The main advantage of this scheme is that due to its

operation, device rating required are considerably reduces and the leakage spike is very low.

3.2 Flyback Scheme

With this configuration, for our High Voltage application we may have following two schemes:

- Conventional Switching Device
- TOPSwitch based Scheme

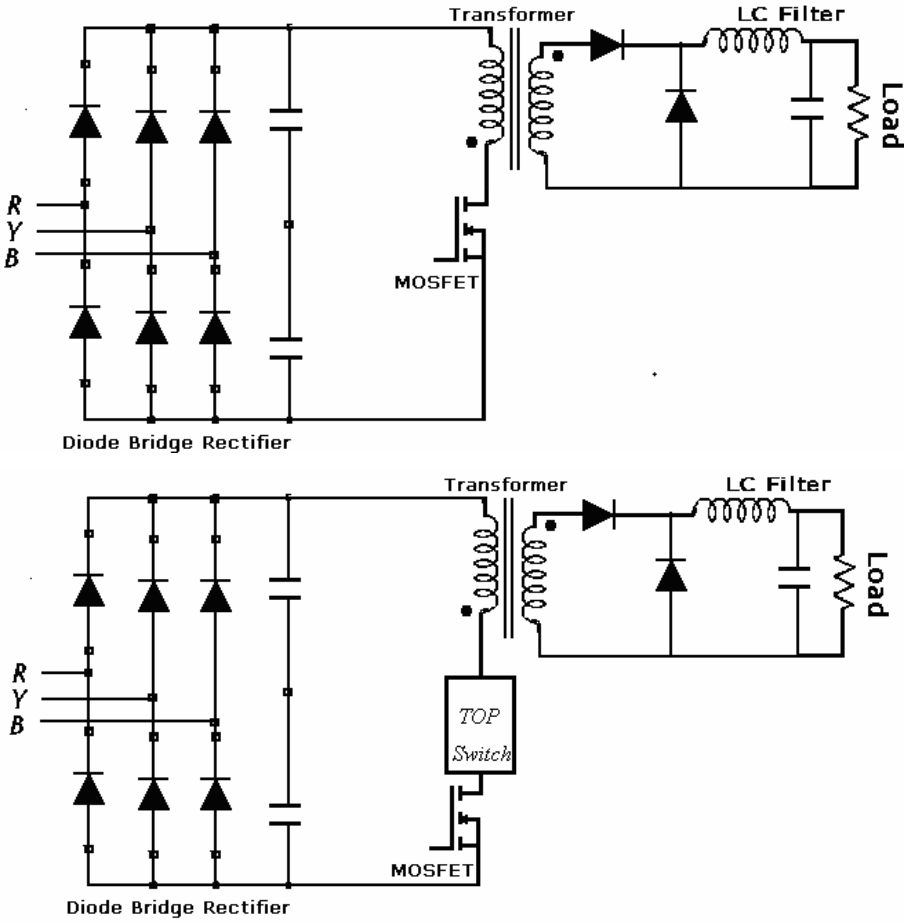


FIG: 3.2 Flyback Converter.

Precise Regulation with min. external components is achieved in the TOPSwitch based scheme. So such scheme can be supporting to economic & efficient design.

Chapter-4

SIMULATION

4.1 Introduction

We have taken the overview of Switched Mode Power Supply topologies. Now with Simulation software-MATLAB Simulink, we shall see the available topologies, how best we can fit in to our system to give optimum solution to our challenge.

As an alternative solutions available to develop cost effective SMPS working for High input can be suggested as follows;

- Double Ended Forward Converter
- Flyback Converter
- Flyback Integrated TOPSwitch Converter

In MATLAB, simulation is done in the mode of Simulink. Simulink Library is equipped with electrical and electronics block-sets, logical operators, mathematical tool boxes. With the use of these block sets we can simulate our electrical circuits.

Particularly our application deals with Power Electronics devices mostly. So for that MATLAB provides a block set named **SimPower.** In which all semiconductors, bridge configuration, firing scheme blocks are available. With this all the types of motors,
R- Load, RL Load or RLC loads are also available. Here we can define them and use for our purpose. For measurements MATLAB provides Voltmeter, Current meter, to view the waveforms different types of Scopes are available. User programmability in all block sets with desired features add feature to the simulation package. So one can simulate his project work on Simulink and view them for analyses.

4.2 Double Ended Forward Converter

In the forward Topologies, one of the most suitable TOPOLOGY for high input can be termed as **Double Ended Forward Converter** Topology. This topology avoids all the problems raised by the leakage inductance-SPIKE. Here we are going to use diodes in support to the MOSFETS in order to avoid higher rating of devices, so that we can use the lower range Devices easily available in the market and we can provide the economic solution. In the Schematic shown below is developed in MATALB Simulink and the results obtained are shown in the next section.

4.2.1 DEFC Schematic

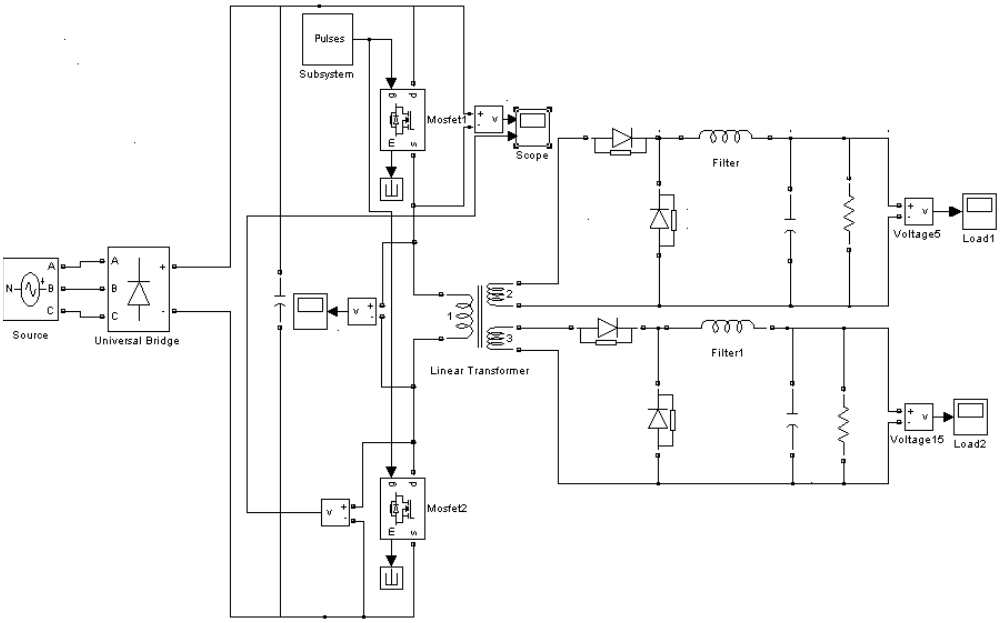


FIG: 4.2.1 DEFC Schematic from MATLAB Simulink

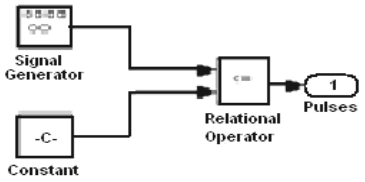


FIG: 4.2.2 Firing scheme as Subsystem of Main DEFC Schematic

FIG 4.2.1 shows the Schematic for Double Ended Forward Converter, developed from the SimPower Library available in the MATLAB. All Power devices

are dropped in from that library only. Control Scheme was generated separately and formed a subsystem to this block set for the firing purpose to the MOSFETs. Fast recovery diodes are to be used in the Rectifier Bridge. So from the MATLAB Library ideal diodes are used, finally output voltages are monitored at the load end. After rectification LC filter is provided to smoothen the wave shape and to get PURE DC output voltage. Measuring instruments are connected across loads, across Switching devices and transformer-in order to monitor the waveforms for analyses.

As shown in the FIG: 4.2.1 pulses are provided with the Subsystem-Pulses. The Schematic of Pulses is shown in the FIG: 4.2.2. This subsystem functions equivalent to our PWM IC. Basically we require pulses for driving the MOS. So that pulses are generated by comparing a constant voltage feedback available and the OSC waveform generated by R&C. As ramp is compared with a constant voltage it cuts at several points and at those points we get the pulses which are provided to MOS. So this Block is the complete control of our Double Ended Forward Converter. With which accurate and desired results are obtained.

4.2.2 DEFC Simulation Results

Waveforms are monitored across the load, switching device, and transformer. So after simulation we got following results.

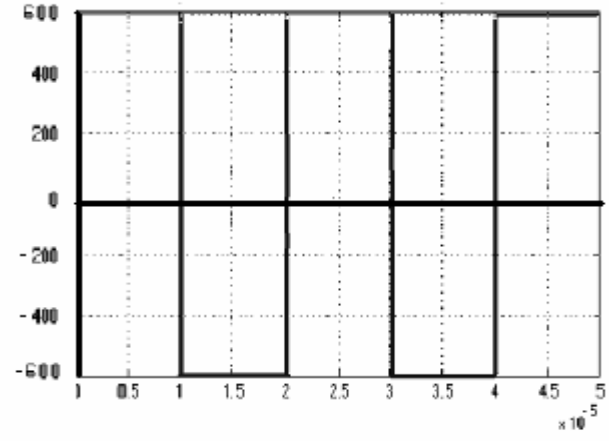


FIG: 4.2.2.1 Waveform across Transformer Primary

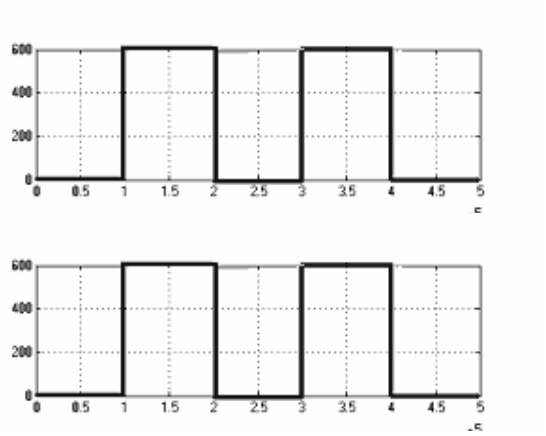


FIG: 4.2.2.2 Waveform across Switching Devices

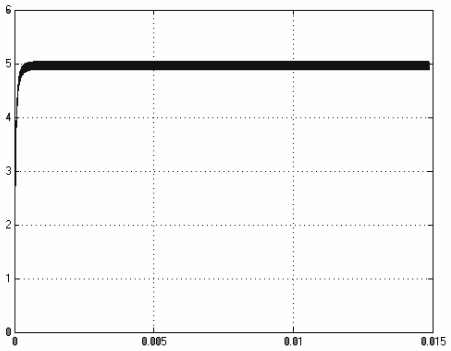


FIG: 4.2.2.3 Voltage output across Master Secondary

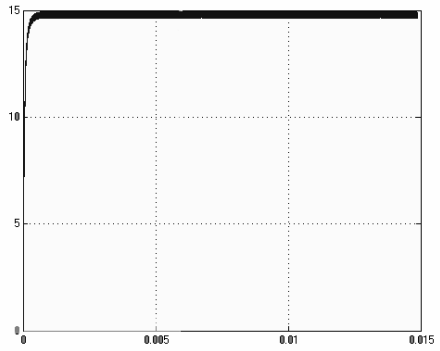


FIG: 4.2.2.4 Voltage output across Slave Secondary

Above figures are the simulation results of DEFC.Across the transformer we are getting the square wave with max DC voltage equals to the DC link voltage. This is clearly seen in the FIG: 4.2.2.1. Across the Switching device max stress will be only max input DC voltage, which achieved our target. So low rating device can be used for economic design.

Very important results are FIG: 4.2.2.3 & FIG: 4.2.2.4, which is the waveforms of outputs of DEFC.Waveforms, clearly signifies that voltage obtained at

load terminal is as per our calculation and requirements. So this simulation tells that the designed topology can be successfully implemented.

4.3 Flyback Converter

Flyback topology is one of the solutions for our purpose. The main advantage of this topology is the simplicity and min auxiliary components are required to design whole system. Simulation from MATLAB can be done with following Schematic.

4.3.1 Flyback Schematic

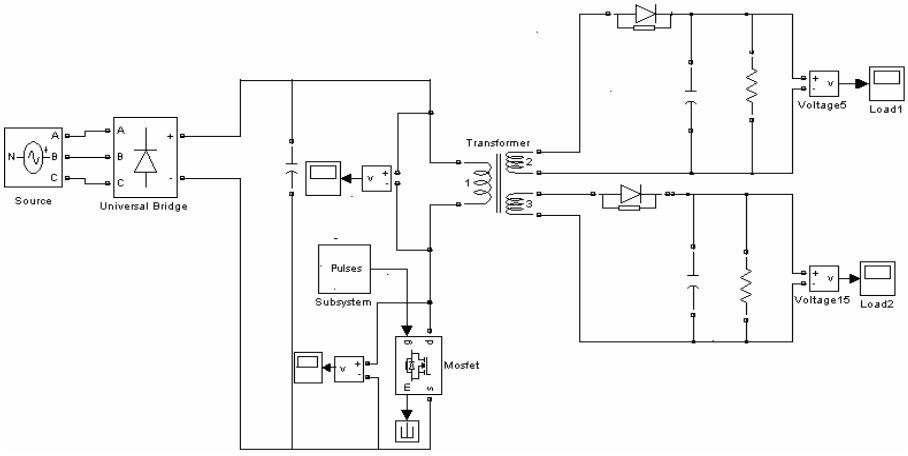


FIG: 4.3.1 Flyback Schematic from MATLAB Simulink

FIG 4.3.1 shows the Flyback topology implemented with the help of MATLAB Simulink. Simulink library has all the devices inbuilt which were simply dropped in the work space to develop the Schematic. Flyback topology was simulated and results were captured in the scopes.

The results of simulation are shown below, which signifies that the Switching device used in this topology should have higher rating than the previous topology. So this would be quite expensive device.

4.3.2 Flyback Simulation Results

Waveforms are monitored across the load, switching device, and transformer. So after simulation we got following results.

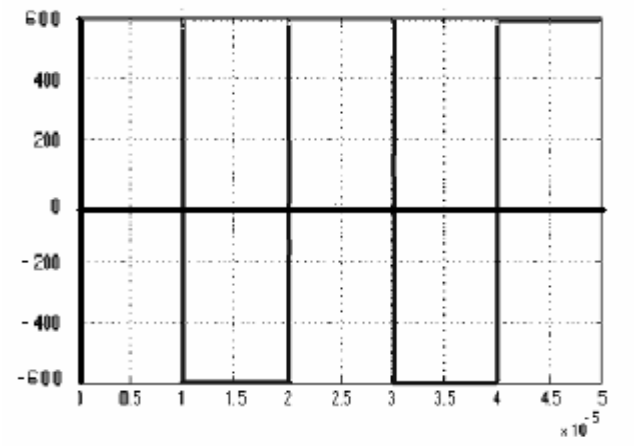


FIG: 4.3.2.1 Waveform across Transformer Primary

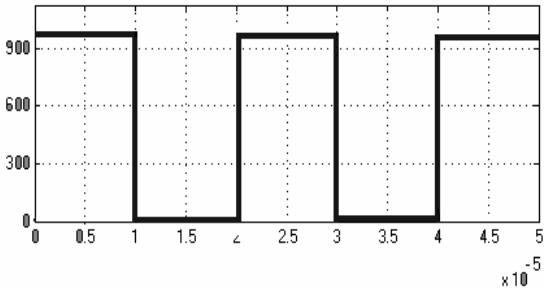


FIG: 4.3.2.2 Waveform across Switch

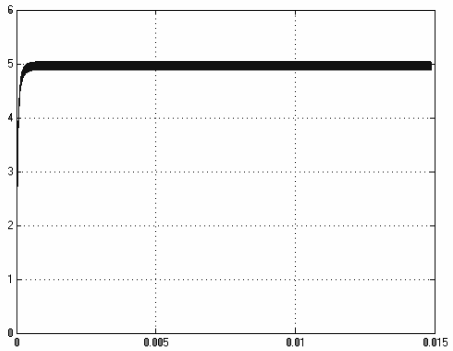


FIG: 4.2.2.3 Voltage output across Master Secondary

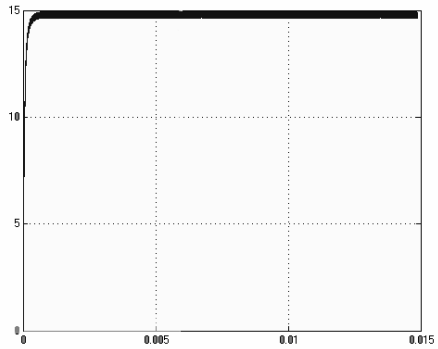


FIG: 4.2.2.4 Voltage output across Slave Secondary

Waveforms show the performance of the topology in the operating conditions. Mainly the primary voltage of the transformer signifies proper switching at proper time. The Voltage stress across the switching device is higher in this case due to air gap leakage inductance. So for this topology we need the switching device rated for higher voltage. FIG 4.2.2.3 & FIG 4.2.2.4 shows the output voltage at the load terminals. That is very clearly showing 5 V & 15 V for respective secondary.

4.4 Flyback Integrated TOPSwitch Converter

In normal Flyback topology we have seen that the switch stress is higher. So it should be avoided by any new modification in the present design. So we can think of splitting voltage during OFF state of the switch. By doing so per switch stress would be approx half. That can be convenient solution. If we incorporate TOPSwitch- with Flyback topology, than so many advantages are added to it. Design can be compact, precisely controlled, easily programmable and very important fact is- it is economic solution.

4.4.1 Introduction to TOPSwitch

A well known Company in the field of power electronics: POWER INTEGRATION has started new product known as TOPSwitch which can be introduced as follows:

It is basically a high frequency switching device with inbuilt PWM control at the gate terminal & which is governed by a control feedback.

Recently launched product TOPSwitch II,(GX) is the Device we are interested in. Which is having following features:

- Works with primary or OPTO feedback
- Cost competitive with linear regulators above 5W
- Built-in Auto-restart and current limiting
- Very low AC/DC losses – up to 90% efficiency
- Latching Thermal shutdown for system level protection
- Implements Flyback, Forward, Boost or Buck topology
- Stable in discontinuous or continuous conduction mode

- Circuit simplicity and Design Tools reduce time to market
- Lowest cost, lowest component count switcher solution

The second generation TOPSwitch-II family is more cost effective and provides several enhancements over the first generation TOPSwitch family. The TOPSwitch-II family extends the power range from 100W to 150W for 100/115/230 VAC input and from 50W to 90W for 85-265 VAC universal inputs.

This brings TOPSwitch technology advantages to many new applications, i.e. TV, Monitor, Audio amplifiers, etc. Many significant circuit enhancements that reduce the sensitivity to board layout and line transients now make the design even easier. The standard 8L PDIP package option reduces cost in lower power, high efficiency applications. The internal lead frame of this package uses six of its pins to transfer heat from the chip directly to the board, eliminating the cost of a heat sink. TOPSwitch incorporates all functions necessary for a switched mode control system into a three terminal monolithic IC: power MOSFET, PWM controller, and high voltage start up circuit, loop compensation and fault protection circuitry.

Basically our aim is to develop a Switched Mode Power Supply, working on high input Voltage and works as cost effective solution.

As Power Integration devices are available for operating at low voltage range, for our purpose, this may not hold good.

So it may require some modification, if we wish to use the same devices. The main problem becomes the voltage range. In order to utilize the main advantage of precise control, we have to provide some solution for voltage level.

So in the TOP243y package our requirement fits properly. That device is having voltage range half the requirement, for our application. So we can add one more Static device in order to share voltage during OFF state. Because during on time both will be ON in parallel and OFF in parallel. So operation will be perfect and unaffected and remain as normal operation.

4.4.2 Flyback Integrated TOPSwitch Schematic

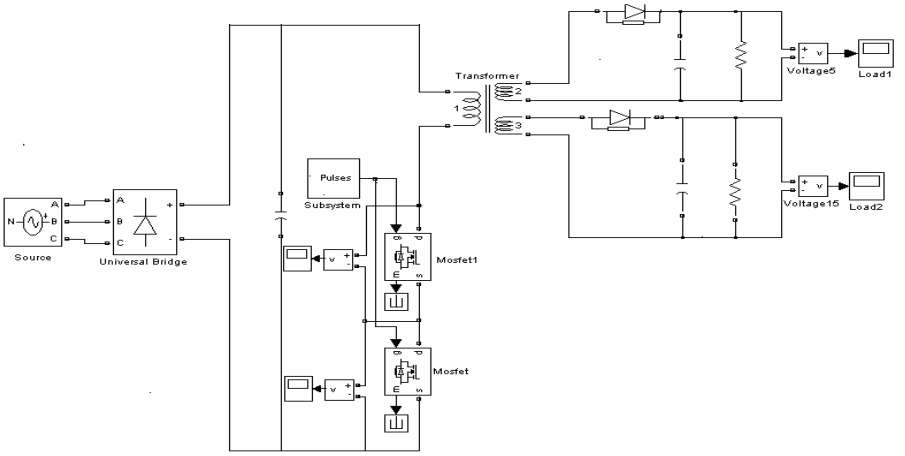


FIG: 4.4.2.1 Integrated TOPSwitch Schematic

The schematic is the same as Flyback topology with the modification that a single unit of High Voltage rated switching device is replaced by two cascaded devices: A TOPSwitch & a Lower Voltage rating MOSFET (Any Switching Device). For simulation purpose we have used two MOSFETs instead of TOP + MOS. Because TOPSwitch is having inbuilt MOSFET so we can replace it by MOSFET & its firing circuit.

The FIG: 4.4.2.1 shows the Schematic for the high voltage Switching Power Supply based on TOP Switch. As DC voltage will be available by providing 3-phase uncontrolled rectifier fed by conventional AC mains, followed by filtering DC Capacitor can be directly used as INPUT DC link voltage for SMPS. To withstand the High voltage during OFF time, we have used an Extra MOSFET cascaded to the TOPS *II (GX)*. So both will get turn on & off, simultaneously hence we can utilize the TOP Switch & its controls & regulation for HV purpose also.

Here transformer used is of special kind; switches are working on 132 KHz frequency, i.e. FERRITE CORE transformer. That can have multiple secondary in order to have isolated multiple outputs.

The above figure is the PSIM Schematic of the HVITS. (High Voltage Integrated TOP Switch). The TOP Switch is here represented as MOSFET. The results are shown in the following section.

4.4.3 Flyback Integrated TOPSwitch Simulation Results

Main waveform to be monitored is across the devices, rest of them will be same as the Flyback topology.

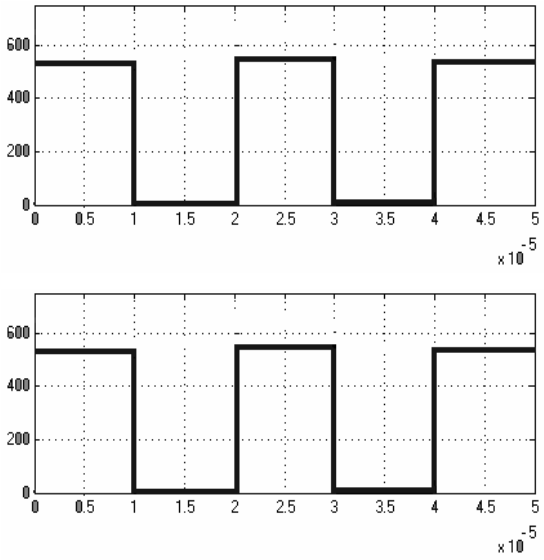


FIG: 4.4.3.1 TOPSwitch & MOSFET waveforms

Chapter-5

HARDWARE DESIGN

5.1 Double Ended Forward Converter

5.1.1 Power Device Specification

MOSFET:

Part No	Make	Breakdown Voltage	Gate-Source	ON State Resistant	Max Current
IRFPG50	International Rectifier	1000V	20V	2 Ohm	6.10 A

DIODE:

Part No	Make	Breakdown Voltage	Max Current
MUR8100E	Motorola	1000V	8.00A

5.1.2 Magnetic Design (Transformer)

The magnetic design of Double Ended Forward Converter consists of mainly the Transformer Design. The high frequency transformer is the heart of the SMPS. That basically has one primary and multiple secondary. Among them one is Master and rest are slave.

For The Double Ended Forward Converter the Voltage output Equation for Master Secondary can be written as:

$$V_{Master} = \left[\left(V_{DC,\min} - 2 \right) \left(\frac{N_m}{N_p} \right) - 1 \right] \left\{ \frac{2T_{on}}{T} \right\} \qquad (5.1)$$

Considering on state voltage drop 1V of each MOSFET the available DC min voltage at primary of the transformer will be ($V_{DC,\,min} - 2$).

Turn ratio of transformer is multiplied to the available rest voltages and from that 1V is deducted as considering the drop across the Rectifier DIODE as 1V.

This product is multiplied with the duty cycle. But here output pulses at the rectifier cathodes have a duty cycle of $2T_{on}/T$ as there s one such pulse duration T_{on} per half period. (T/2) .

Now the change in voltage of secondary per single turn change in the winding of secondary can be given by Farad's law:

$$E=N*A_e*(dB/dt)\times 10^{-8} \quad (5.2)$$

$$\therefore \quad \frac{E}{N}=A_e*(dB/dt)\times 10^{-8} \quad 5.3)$$

Here area is in square centimetre.

Change in the Core Flux is in Gauss.

Flux Change takes place during only ON time f the switching device.

So voltage per turn is directly proportional to the switching frequency.

And as the switching device is MOSFET so there is no risk of Flux imbalance in this topology. So with DEFC all the problems are solved.

Defining the Actual rating for this DEFC Topology of SMPS,

Output Power P_o=30W

$V_{Dc,\min}$ =Minimum DC Link Voltage = 450 V

$V_{Dc,\max}$ =Maximum DC Link Voltage = 750 V

V_{ms}= Max Voltage Stress Allowable=1200 V

Master Secondary output V_{Master}= 5V

Slave Secondary output V_{Slave}= 15V

Now,

Let's consider efficiency of the converter 80 Percentage;

$$\text{Input Power } P_{in} = 1.25 * P_o \qquad (5.4)$$

And we also know;

Input Power is

$$Pin = V_{Dc,\min} * 0.4 * I_{av,\ primary} \qquad (5.5)$$

Now comparing Equations 5.4 & 5.5;

$$I_{av,\ primary} = 3.13 * P_o / V_{Dc,\min} \qquad (5.6)$$

Where $I_{av,\ primary}$= Primary Average Current of Transformer.

= 0.20866 Amperes

$\approx$ 210 mA

And 80 Percent on time is sufficient for flux balancing point of view and hence max required duty cycle can be termed as Duty Cycle δ=0.4.

As per records the change in the flux is 1200G preferable when working with 100 KHz operating frequency.

$$\therefore \text{ Primary turns } N_p = (V_{DC} - 2) * T_{on} \times 10^{+8} * \frac{1}{A_e * dB} \qquad (5.7)$$

Where area A_e=0.395 cm^2; provided by the core manufacturer DATA sheet.

From Frequency – Power output Specification Core is: Philips Make (812E250)

From the Equations 5.7 & 5.1;

- ✓ Transformer Turns:
  - Primary=378
  - Mater=12
  - Slave= 36

- ✓ Size of the wire for winding of transformer:

The wire size measured in Circular mils. Where CM=10^6 * Square inch/ (π/4). As per the formula; the Circular mils required to wind the transformer-primary and secondary can be written as:

Circular mils needed= $500 * 1.97 * P_o / V_{Dc,\min}$

=66.

5.1.3 Control Scheme Design

In the power circuit there are two MOSFET used. The control circuit consists of mainly the Driver Circuit of these two MOSFET.

The main task of this driver circuit is to maintain the pulses at the gate terminal of both of the Switching Device such that the output @ secondary of the transformer is given to sensitive load maintained constant. It should be constant irrespective to the change in line or load conditions.

In terms of control saying we have to maintain the pulse width of the firing pulses such that it maintains the firing of MOSFET such that the change in load voltage is void and Sensitive load is fed continuously with constant voltage. For such control PWM control strategy is the perfect choice.

There are two type of control in PWM strategy are available for our requirement to be fulfilled.

- Voltage Mode Control
- Current Mode Control

Usually for the following purpose Voltage Mode PWM control method is used.

- There are wide input lines and/or output load variations possible.
- Particularly with low line - light load conditions where the current ramp slope is too shallow- for stable PWM operation.
- In the case of high power-noisy condition where noise on the current waveform would be difficult to control.
- Saturable reactor controllers are to be used as auxiliary secondary-side regulators.
- Applications where the complexities of dual feedback loops and/or slope compensation are to be avoided

But the limitations of this type of control Strategy is, any change in line or load must first be sensed as an output change and then corrected by the feedback loop.

- This usually means slow response.
- Complicated circuit design due to Poor cross regulation.

So on the other hand; The Current Mode PWM Control Strategy is advantageous by following means.

- Current-mode circuits include inherent pulse-by-pulse current limiting by merely clamping the command from the Error Amplifier, and the ease of providing load sharing when multiple power units are paralleled.
- Since inductor current rises with a slope determined by Vin-Vo, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage
- Since the Error Amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop (at least in the normal region of interest). This allows both simpler compensation and a higher gain bandwidth over a comparable voltage-mode circuit.

And usually used under the following requirements or one can say the selection criterion of The Current mode PWM control is:

- The application is for a DC/DC converter where the input voltage variation is relatively constrained.
- The fastest dynamic response is needed with a given switching frequency.
- A modular application where parallel ability with load sharing is required.
- In push-pull circuits where transformer's flux balancing is important.
- In low-cost applications requiring the absolute fewest components.

5.1.3.1 Introduction to PWM IC (UC3843)

So the above discussion suggests that we shall provide the control to our Power circuit scheme by current mode PWM control. Means we shall fix a current level for main power circuit, and during on load condition continuously we will monitor that current and according to the change in that we will provide control to the circuit.

Texas Instruments incorporated company UNITRODE Corporation has put PWM controller IC in the market which can be the Key component in Control Card Design.

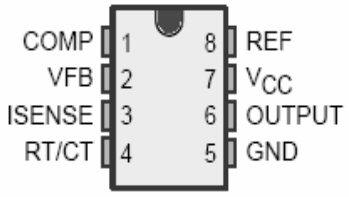


FIG: 5.1.3.1 PWM IC- UC3843

1. *COMP*: This is connected to the error amplifier internally, with the link of the output terminal of amplifier.

   This is provided to decide the Gain of Error amplifier set by the USER, by connecting the resistor across error amplifier as the feedback resistor.
2. $V_{F/B}$: This is the pin of voltage feedback input to the IC from the main output to be regulated. This output is compared at error amplifier and processed and regulated and tried to maintain it constant by varying the duty cycle of the switches.

3. $I_{SENSE:}$ Switch current is sensed and applied to the current sense, (CS), pin following some slight noise filtering. With this configuration, the error amplifier output is being compared to primary current. Most notably, it makes the converter's power stage resemble a voltage controlled current source. The voltage (error) amplifier defines the level of primary current to be allowed every switching cycle. As the load current changes, so to does the commanding error amplifier output voltage. Thus current sense pin also contributes in maintaining the output constant.
4. *OSC*: This is the oscillator pin, which will define the frequency of operation, by the proper design and RC calculation.
5. *GND*: This is common ground for the control circuit- we can call it the Ground PIN.
6. *OUT*: This is the output pin which will provide firing pulses for the switch.
7. *VCC*: Voltage source of the IC.
8. V_{REF}: This is the voltage reference pin. From here the reference voltage is taken for comparison to error amplifier as the main function.

For the purpose of using this IC in open frame is OK, but when we will plan to work in closer loop, we can not use this IC as it has max Duty cycle 100%.So till the feedback is not generated IC output will be DC, Which can not be given to pulse transformer, Because our both devices are getting fired through pulse transformer. So the alternate solution is to use other IC of same class with 50% duty cycle. All the feature remains same. Just the change will be, during no feedback it will provide 50% duty cycle pulses. Means when we will start the system, IC will provide max 50% duty cycle. So MOS will get firing pulses, output will be generated & than according to feedback in proportion, duty cycle will get change. And close loop operation will get synchronised.

5.1.4 DEFC PCB Design

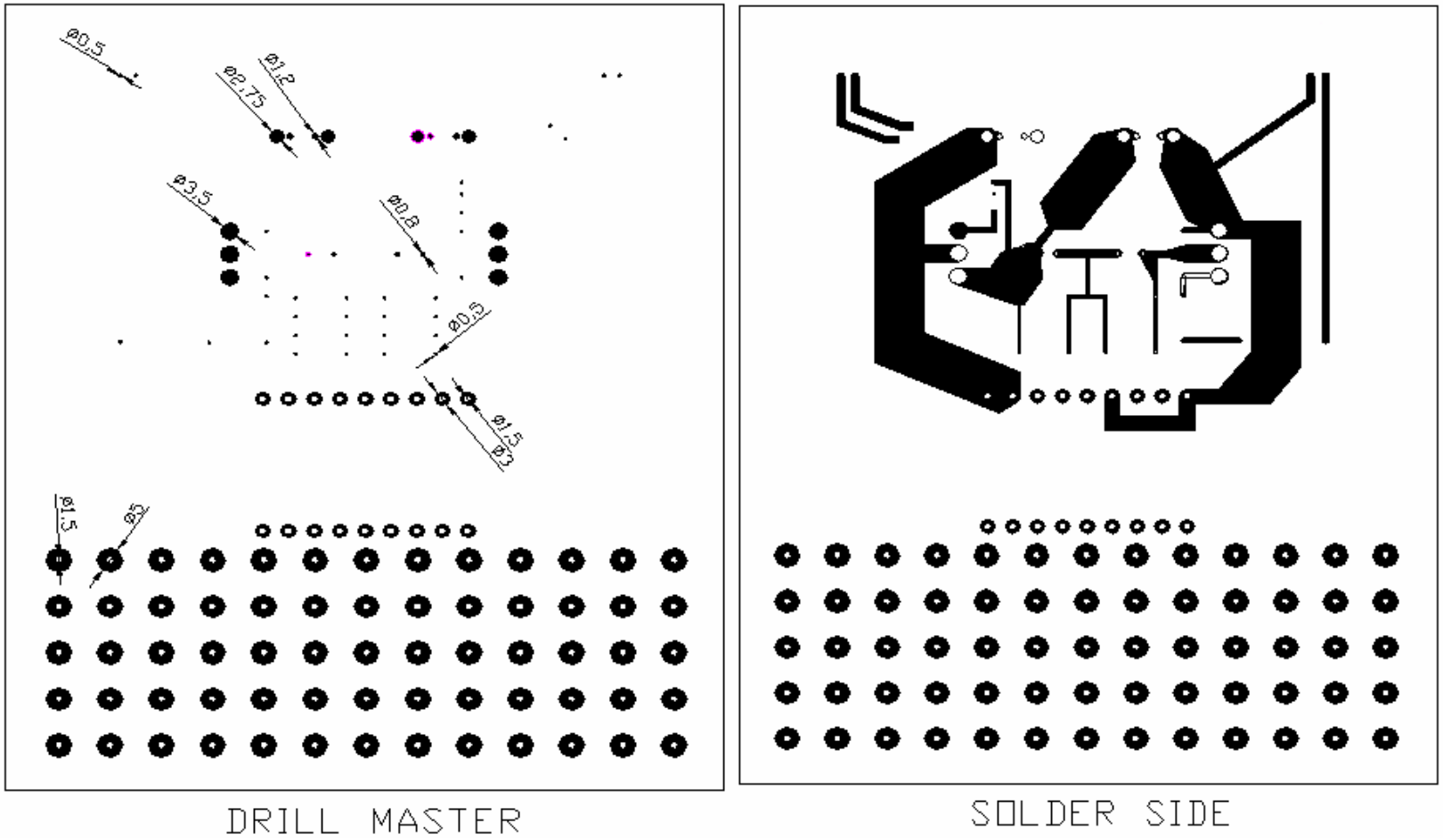


FIG: 5.1.4.1 PCB Layout, Drill master & Solder side

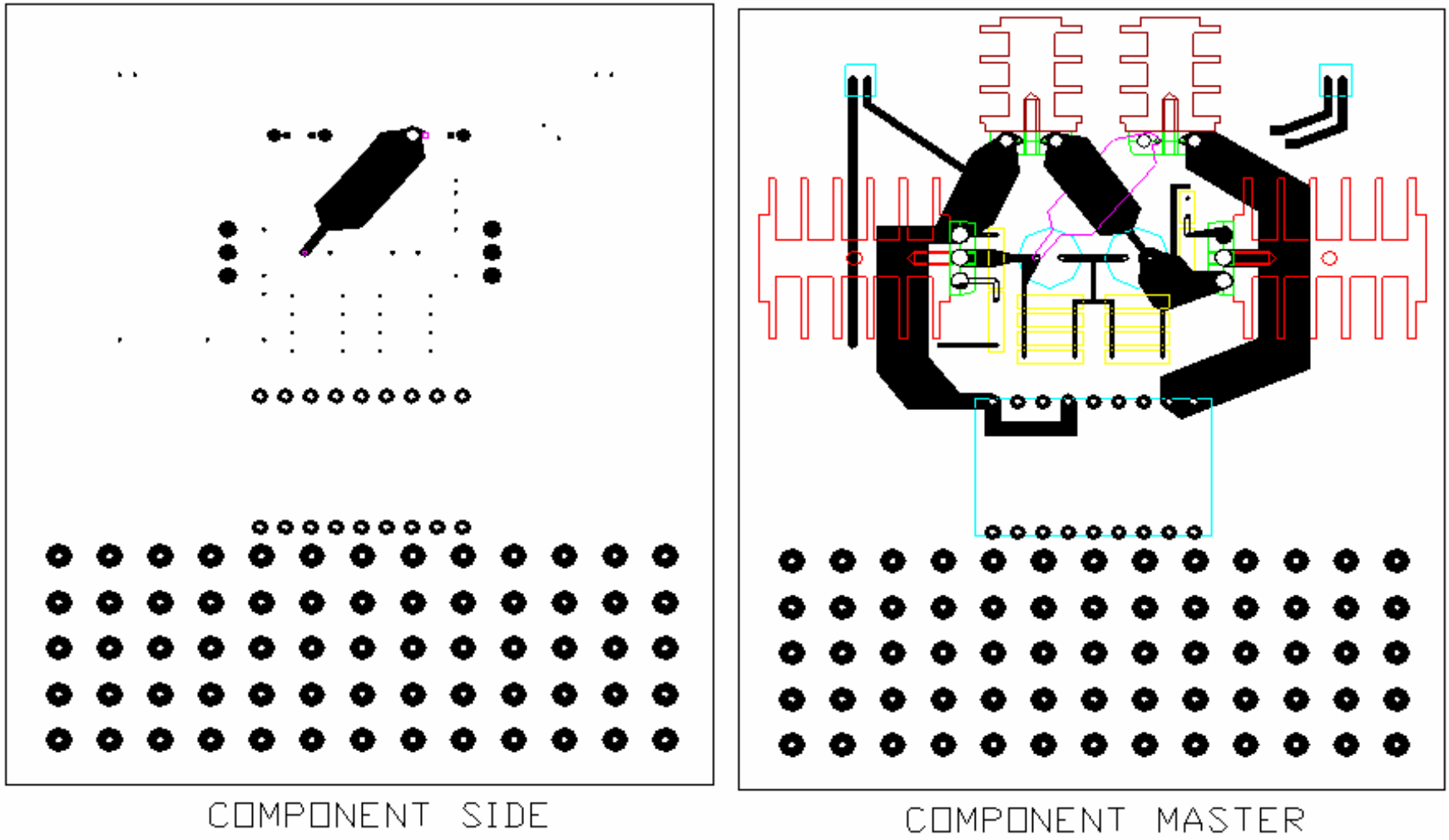


FIG: 5.1.4.2 PCB Layout, Component side & Component master

5.1.5 DEFC Schematic.

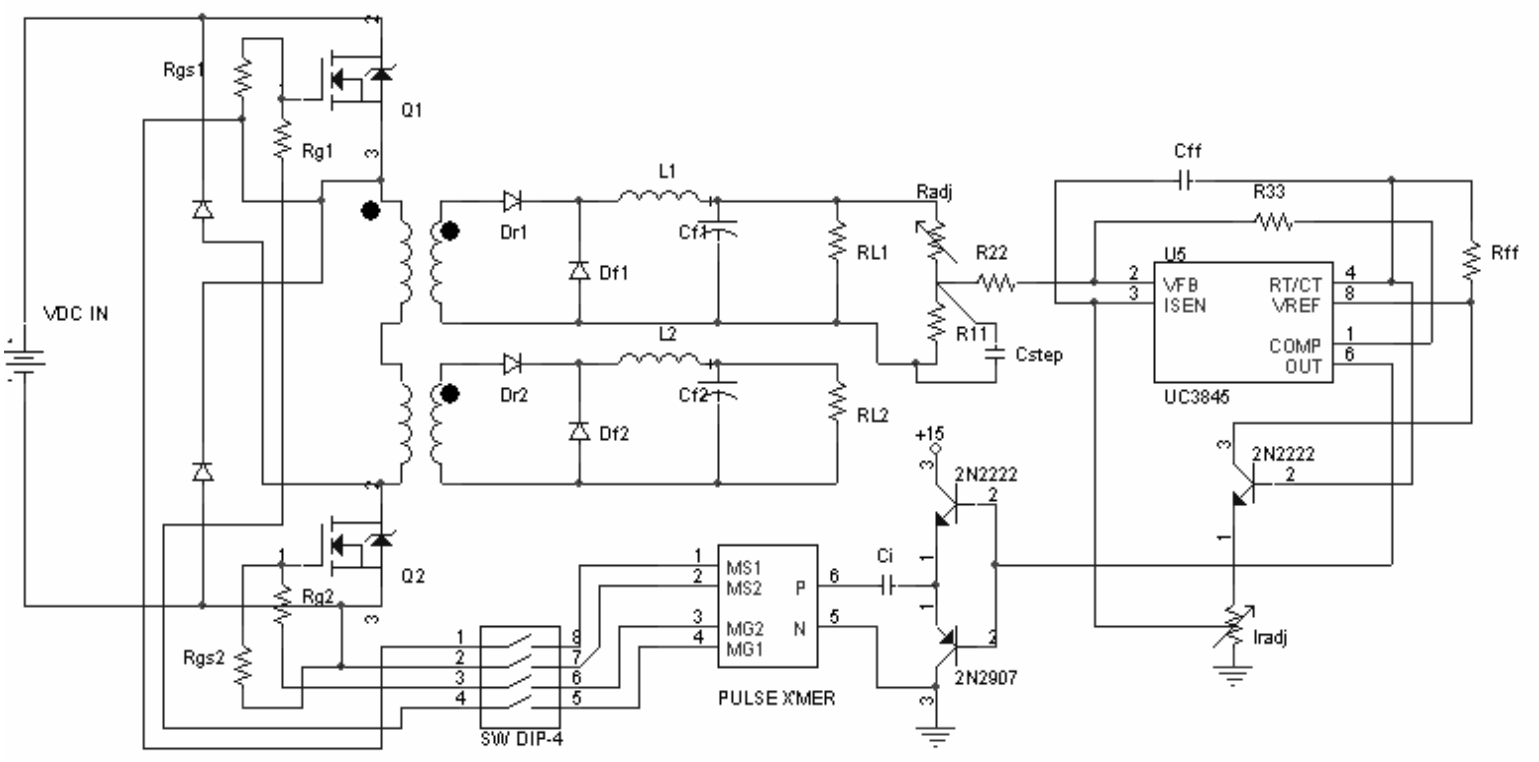


FIG: 5.1.5 Detail diagram of Double Ended Forward Converter

5.2 Flyback Converter

5.2.1 Power Component Specification

Part No	Make	Breakdown Voltage	Gate-Source	Max Current
IKW4T120	Infiniun	1200V	20V	40.00 A

5.2.2 Magnetic Design & Control Scheme

Today SMPS are mostly used to reduce size, and weight, and as a consequence the production costs of power supplies. Under these Conditions the most expensive component in modern power supplies is the transformer.

A choice of high operating frequency leads to a smaller volume-to-power ratio. On the other hand the core losses of magnetic components restrict the size reduction. The transformer power rating is mainly limited by prescribe temperature rise.

In this configuration the transformer act as an inductor in addition to its normal function of energy transfer. Here energy is transferred to load during the time when switch is OFF.

In a Flyback converter, the transformer is the main energy storage and processing element. Therefore, it has a large effect on the efficiency of the power supply as a whole. An efficient Flyback transformer will have low DC losses, low AC losses, low leakage inductance, and low winding capacitance.

The only significant DC losses in a power transformer will be due to the copper losses in the transformer windings. For a high efficiency design, the transformer wire gauge should be sufficiently large to reduce the copper losses to an acceptable level. A traditional design guideline is to size each winding for a current capacity of 200 to 500 circular mils per RMS ampere of current.

AC losses in the transformer arise from skin effect losses in the transformer windings, and AC core losses. High frequency currents tend to flow close to the surface of a conductor rather than its interior. This phenomenon is called the skin effect. The penetration of AC current into a conductor varies as the square root of the frequency, so for a higher frequency, currents will flow closer to the surface of the conductor and leave the interior underutilized. The result is a higher effective resistance for AC Current versus DC current. To minimize the AC copper losses in a transformer, no conductor should be used that has a thickness greater than 2 times the skin depth at the operating frequency of the supply.

A very important consideration in designing a low-loss transformer is minimizing the amount of leakage inductance. A transformer with high leakage inductance will dissipate large amounts of energy in the primary clamp components. The energy dissipated in the clamp is wasted and detracts from the Overall efficiency.

So calculation Starts from Parameters available are:

Output:

V10 = 18 V

V20 = 6 V and

Po = 30W

Input:

VDC_{max} = 750V

VDC_{min} = 450V

Frequency of operation = f = 132 KHz

Allowable Max Stress Vms

= VDCmax + (Np/Ns)(Vo+1) ;

Where N_p = Primary Turns

N_s = Secondary Turns

According to calculations;

$N_p = 150$

$N_{s1} = 8$

$N_{s2} = 22$

$L_p = 6.75mH$

$I_{avg} = 244mA$

$L_g = 1.97mm$

Control Scheme Remains same as DEFC, just the difference will be NO pulse Transformer is going to use, directly IC output is used to drive IGBT.

5.2.3 Flyback Schematic

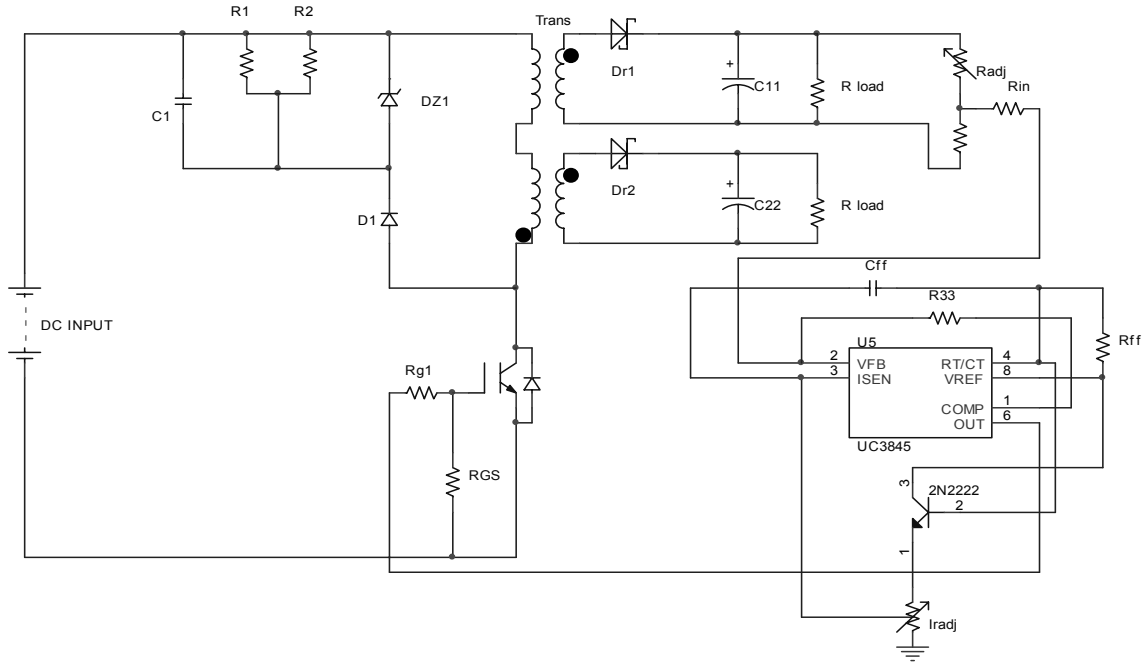


FIG: 5.1.6 Detail diagram of Flyback Converter

5.3 Flyback Integrated TOPSwitch Converter

5.3.1 Power Device Specification

MOSFET

Part No	Make	Breakdown Voltage	Gate-Source	ON State Resistant	Max Current
APT5020	APT	500V	20V	2 Ohm	6.10 A

TOPSwitch GX

Part No	Make	Breakdown Voltage	ON State Resistance	Max Current
TOP243Y	Power Integration	700V	7.8Ohm	3.6 A

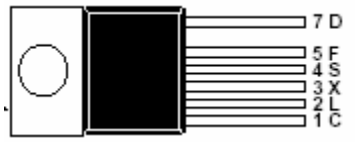
5.3.2 Introduction to TOPSwitch GX

Special Features:-

- Extended power range to 290 W
- Features eliminate or reduce cost of external components
- Fully integrated soft-start for minimum stress/overshoot
- Externally programmable accurate current limit
- Wider duty cycle for more power, smaller input capacitor
- Separate line sense and current limit pins on Y/R/F packages
- Line under-voltage (UV) detection: no turn off glitches
- Line over voltage (OV) shutdown extends line surge limit
- Frequency jittering reduces EMI and EMI filtering costs
- Regulates to zero load without dummy loading
- 132 kHz frequency reduces transformer/power supply size
- Half frequency option in Y/R/F packages for video applications
- Hysteretic thermal shutdown for automatic fault recovery
- Large thermal hysteresis prevents PC board overheating

TOPSwitch-GX uses the topology of cost effectively integrating the high voltage power MOSFET, PWM control, fault protection and other control circuitry onto a single CMOS chip. Many new functions are integrated to reduce system cost and improve design flexibility, performance and energy efficiency.

Depending on package type, the *TOPSwitch-GX* family has either 1 or 3 additional pins over the standard DRAIN, SOURCE and CONTROL terminals allowing the following functions: line sensing (OV/UV, line feed forward/DC max reduction), accurate externally set current limit, remote on/off, and synchronization to an external lower frequency and frequency selection (132 kHz/66 kHz). All package types provide the following transparent features: Soft-start, 132 kHz switching frequency (automatically reduced at light load), and frequency jittering for lower EMI, wider DCMAX, hysteretic thermal shutdown and larger creepage packages. In addition, all critical parameters (i.e. current limit, frequency, PWM gain) have tighter temperature and absolute tolerance, to simplify design and optimize system cost.



PIN Functional Description:

DRAIN (D) Pin:

High voltage power MOSFET drain output. The internal start-up bias current is drawn from this pin through a switched high-voltage current source. Internal current limit sense point for drain current connected to SOURCE pin and 66 kHz if connected to CONTROL pin. The switching frequency is internally set for fixed 132 kHz operation in P and G packages.

CONTROL (C) Pin:

Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also

used as the connection point for the supply bypass and auto-restart/ compensation capacitor.

LINE-SENSE (L) Pin:(Y PIN feature):-

Input pin for OV, UV, line feed forward with DCMAX reduction, remote ON/OFF and synchronization. A connection to SOURCE pin disables all functions on this pin.

According to our application Rl=3 M Ω

EXTERNAL CURRENT LIMIT (X) Pin:

Input pin for external current limit adjustment, remote ON/OFF, and synchronization. A connection to SOURCE pin disables all functions on this pin.

According to our application Rx=9.1K Ω

FREQUENCY (F) Pin:

Input pin for selecting switching frequency: 132 kHz if connected to SOURCE pin and 66 kHz if connected to CONTROL pin. The switching frequency is internally set for fixed 132 kHz operation in P and G packages.

SOURCE (S) Pin:

Output MOSFET source connection for high voltage power return. Primary side control circuit common and reference point.

The main Idea behind the HVITS converter is to utilize the Skills of regulation of the TOP Switch with inherent protection, Compact design soft start features for the purpose of providing regulated power supply to the load with a large input variation in the input side.

New idea is to use an auxiliary MOSFET in company with TOP to with stand very high voltage during off state in the case of SMPS working on High voltages.

The block diagram is given for such an arrangement, with feedback control Close Loop operation. Where feedback voltage and input current are responsible for next switching pattern of the Devices.

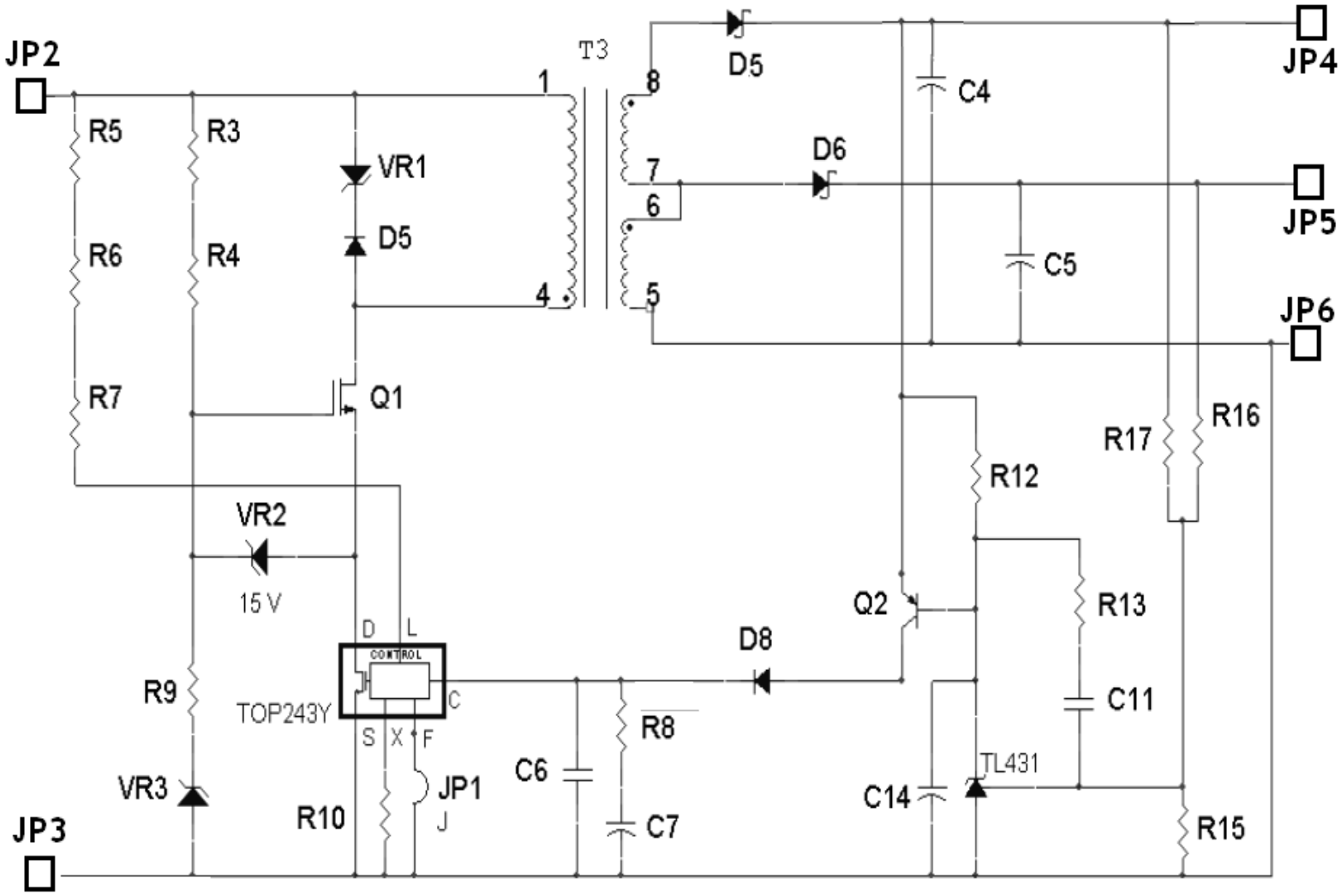


FIG: 5.3.2: Detail Diagram of Integrated TOPSwitch Design

Fig 5.3.2 shows the detail diagram of Integrated Flyback TOPSwitch Design. This is developed in the Power Integration Software which is provided with their catalogue. This software needs the user programmability in terms of their requirements. One can programme it for complete range of regulated power supply. Power Integration provides the Devices to be used for regulated power supply. Enough design tools are provided for particular design with their software in order to have comfortable Design.

They are manufacturing mainly TOPSwitches, Tiny Switches, Link Switch and so many ranges of Switches. These switches are mostly working on High Frequency, self regulated, with precise control. This switch is built such a way that for its control we need minimum components in the control scheme.

A high range of DC input is to be given to the SMPS. After that its transformer & clamping circuit is there. Main Device- TOPSwitch and Auxiliary MOSFET are connected in cascade form. The MOSFET needs its gate drive circuit synchronized with TOPSwitch. TOPSwitch has terminals like CONTROL, LINE SENSE, and Frequency PIN associate with Drain & Source.

Control Pin gets the Feedback from the output. Line sense Pin is the pin from where the line current is sensed in the TOPSwitch. PIN X is current control pin, from there a resistor will decide & control the max input current. Pin F will decide the operating frequency of the Device. For biasing, on the secondary side winding is provided.

Chapter-6

TESTING & RESULTS

After hardware design all the suggested topologies were tested under full load conditions. The results were recorded and the waveforms were stored. For all the topologies of SMPS under all the test conditions and experiments results are recorded as follows.

6.1 Prototype Testing Results

At the initial stage for the purpose of getting familiar with hardware work and for checking the topology developed is working properly or not, Prototype of Double ended Forward Converter was developed and tested.

That converter was rated for max 100V DC input and 15V DC output. The synchronous pulses were developed and the output voltage at 65V DC input was measured and recorded.

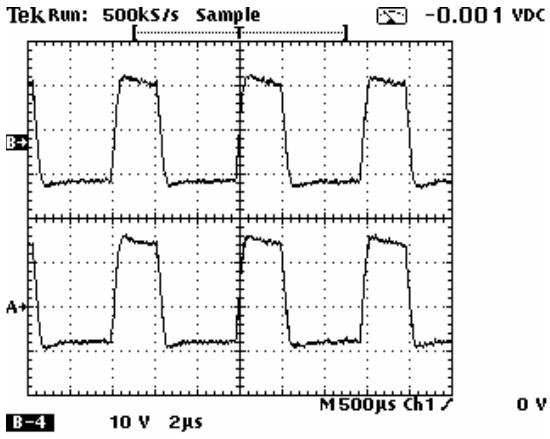


FIG: 6.1.1 Gate pulses at MOS1 & MOS2

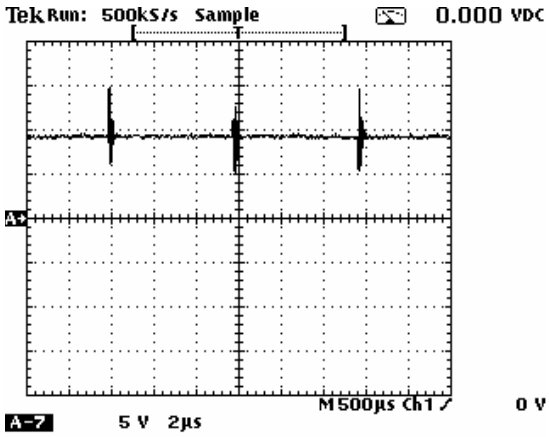


FIG: 6.1.2 Rectified & Filtered Output at load

The other topology that is Integrated TOPSwitch Flyback Converter- was also tested at lower voltages. The Prototype was developed for max 250V DC input. Experiment was carried out with TOP221 and tested till 200VDC. Output was designed to get 6V regulated output, with close loop implementation we have got regulation tuned at 6.27V DC as main output voltage. This was regulating for input 85V-200V DC.

Photographic waveforms for MAX and min voltage input, with TOPSwitch and transformers' primary voltages are shown simultaneously in FIG: 6.1.3 & FIG: 6.1.4.

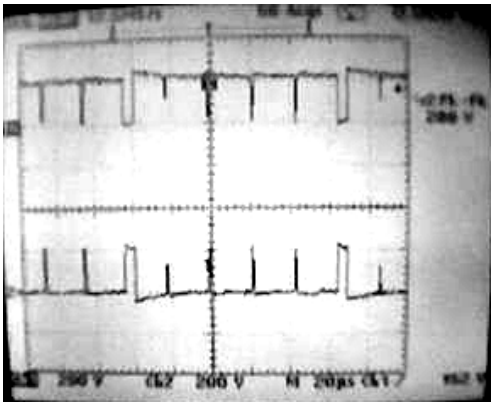


FIG: 6.1.3 Min Duty Cycle Operation

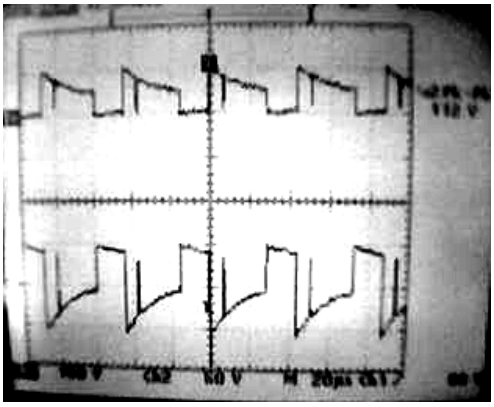


FIG: 6.1.4 Max Duty Cycle Operation

6.2 Double Ended Forward Converter Experimental results

After finishing prototype of DEFC, it was fabricated for full rated configuration and testing was started in steps and initially it was checked for *OPEN loop* configuration and after that it was tested for close loop operation. But in that layout problems were mainly causing high leakage inductance spike, which was creating problem. Then initial waveforms were trapped from GP Board work. Due to high frequency operation-long paths of current may create high leakage inductance problem. So on GP Board with closest possible arrangement of Power Devices was carried out and it was tested for max 300 V DC input. Those waveforms are shown in FIG: 6.2.1 to FIG: 6.2.7.

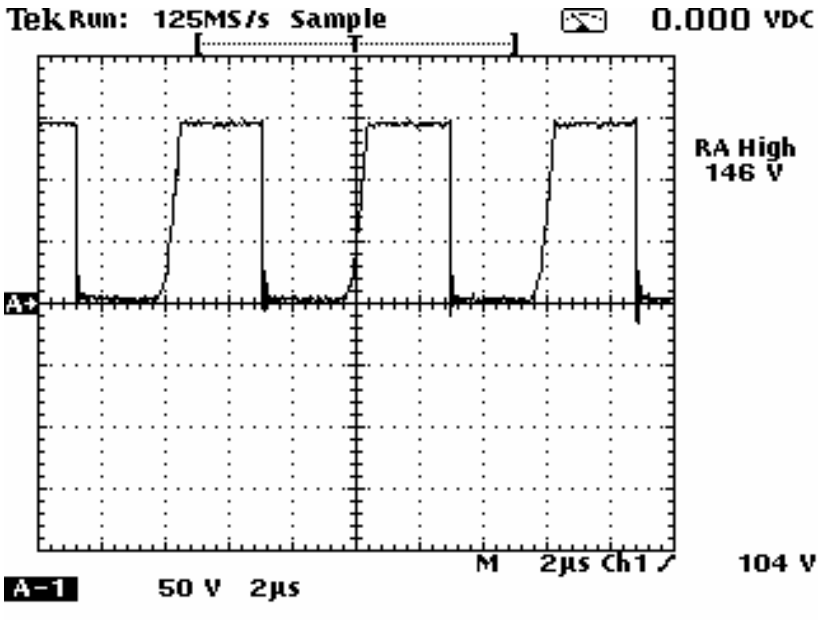


FIG: 6.2.1 Voltage across MOS with 150 VDC input

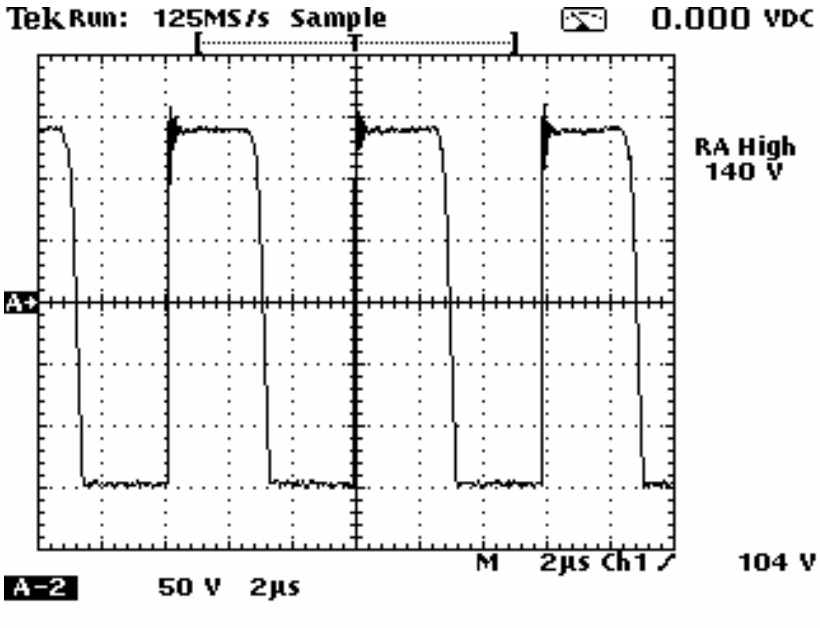


FIG: 6.2.2 Voltage across Primary of Transformer with 150 VDC input

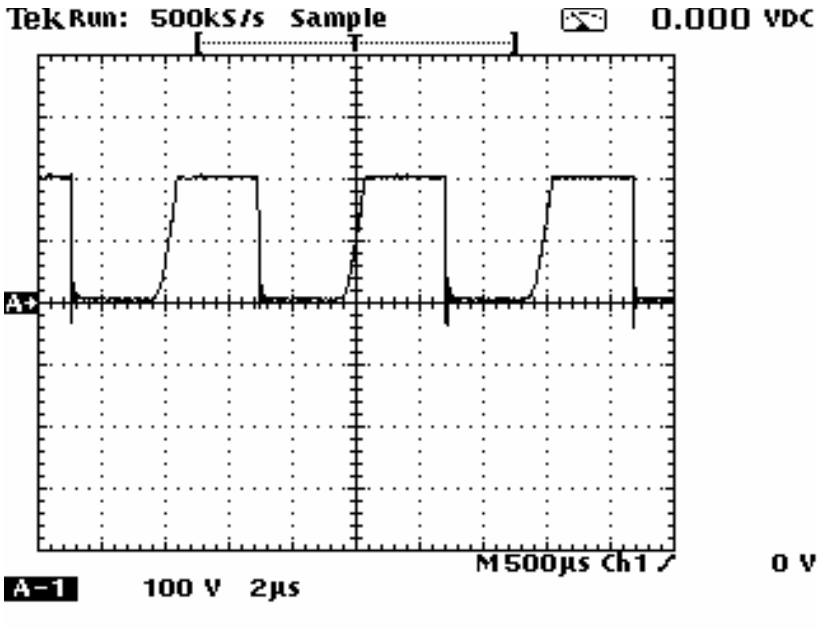


FIG: 6.2.3 Voltage across MOS with 200 VDC input

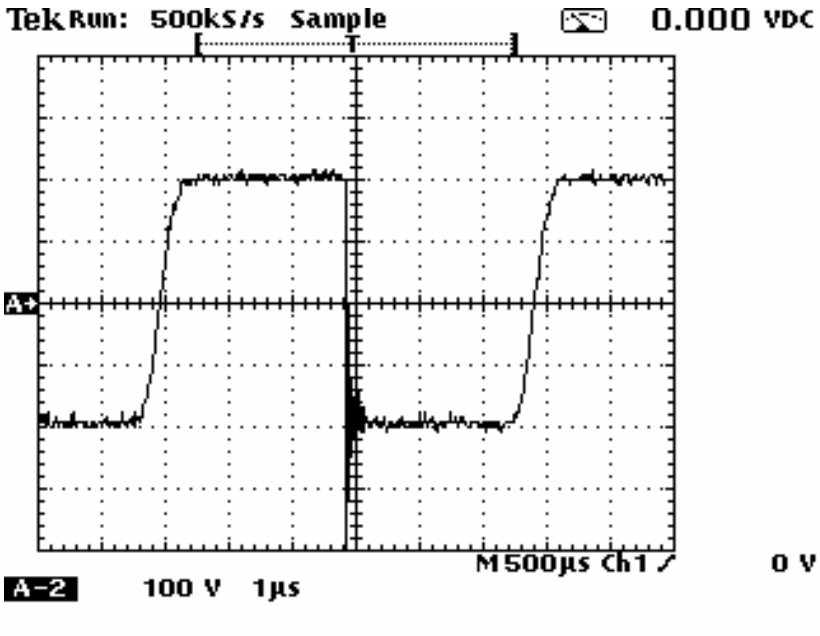


FIG: 6.2.4 Voltage across Transformer Primary with 200 VDC input

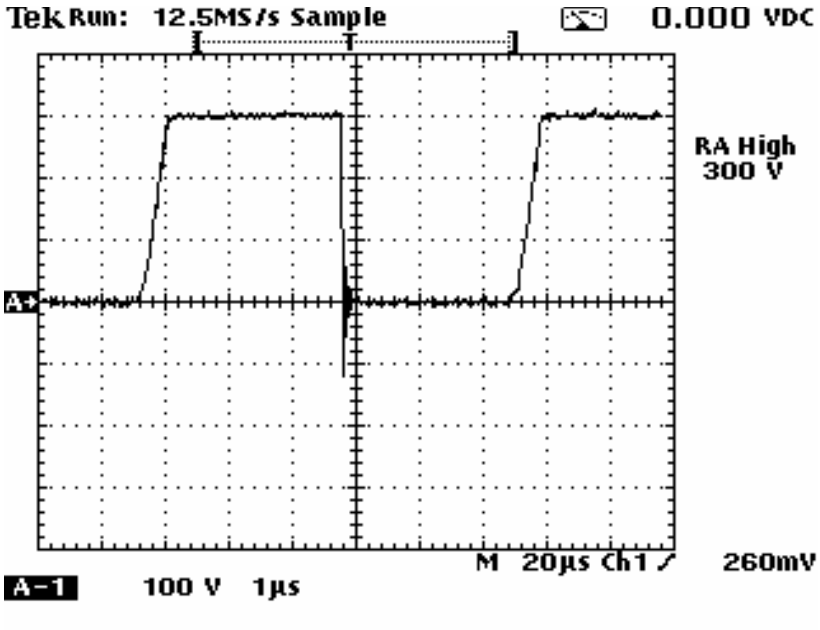


FIG: 6.2.5 Voltage across MOS with 300 VDC input

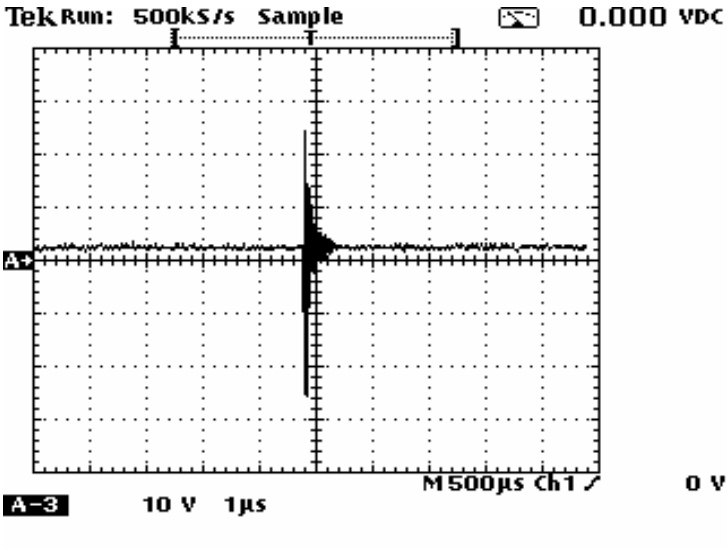


FIG: 6.2.6 Master Secondary Output

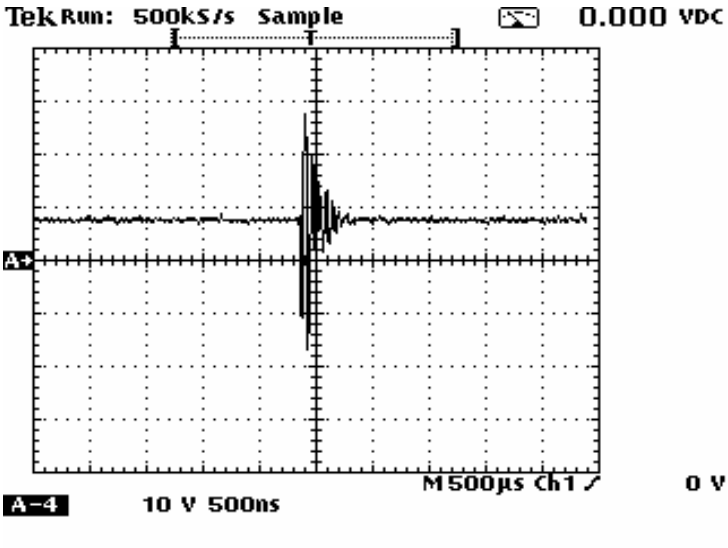


FIG: 6.2.7 Slave Secondary Output

Now due to layout problem PCB was developed in order to min Spike during switching of device. So after this all experiments were done with PCB layout.

So with that properly designed LAYOUT further testing was carried out. Next testing result is with 450V DC and more till its full capacity. With full load and full rated Voltage the SMPS was kept for heat RUN for more than an hour. During that it was showing proper results and the recorded waveforms are shown in FIG: 6.2.8 to 6.2.13

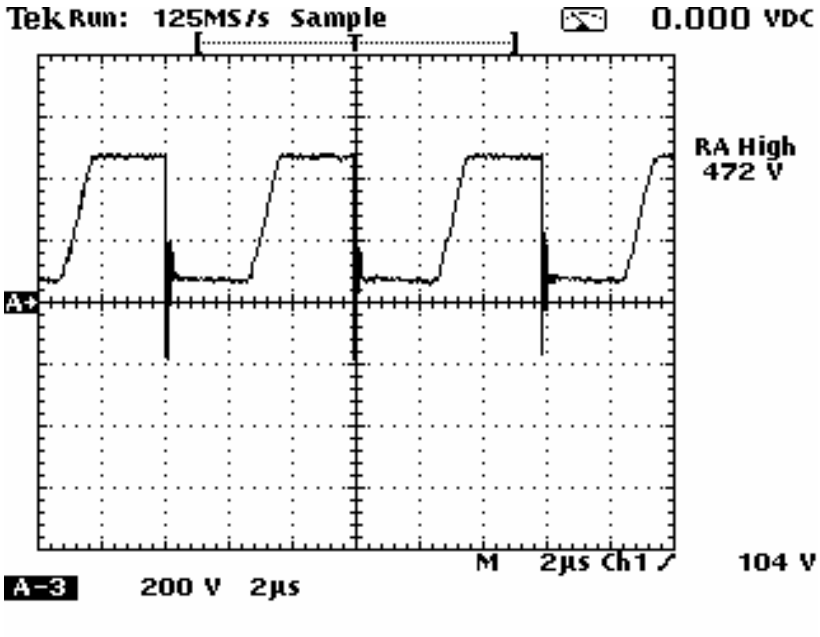


FIG: 6.2.8 Voltage across MOS with 450 VDC input

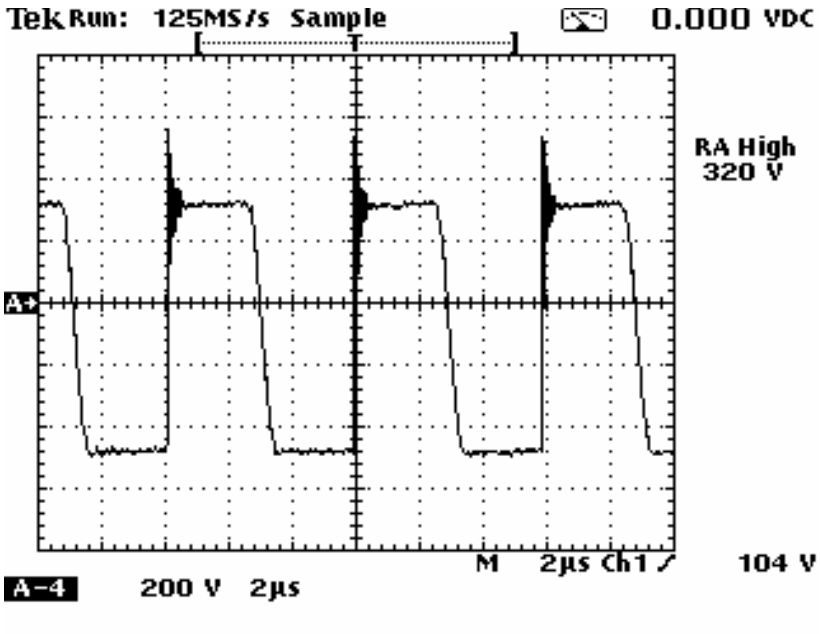


FIG: 6.2.9 Voltage across Transformer Primary with 450 VDC input

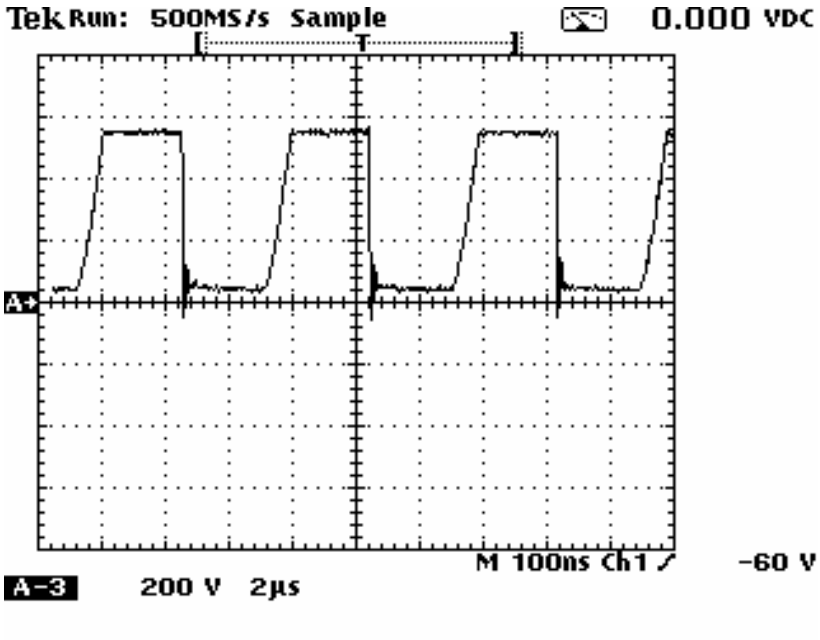


FIG: 6.2.10 Voltage across MOS with 585 VDC input

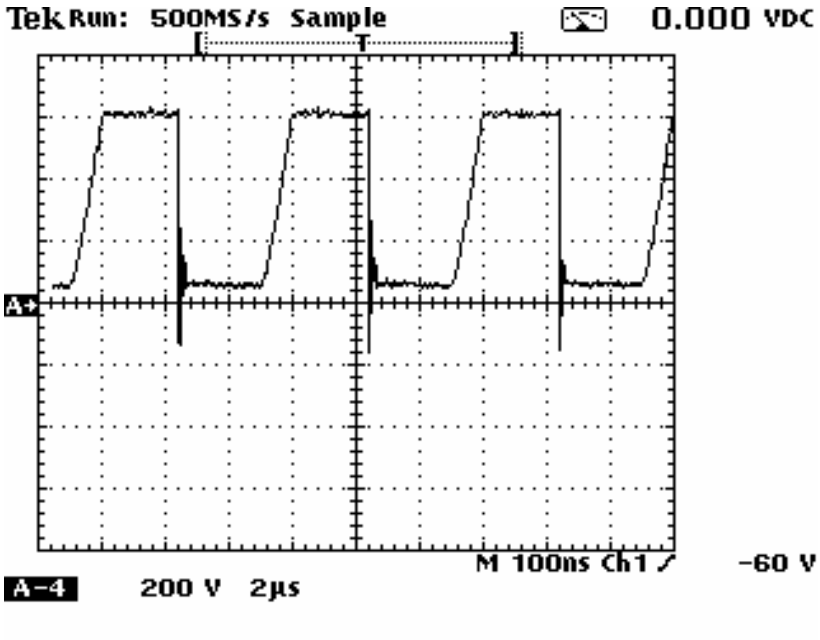


FIG: 6.2.11 Voltage across MOS with 600 VDC input

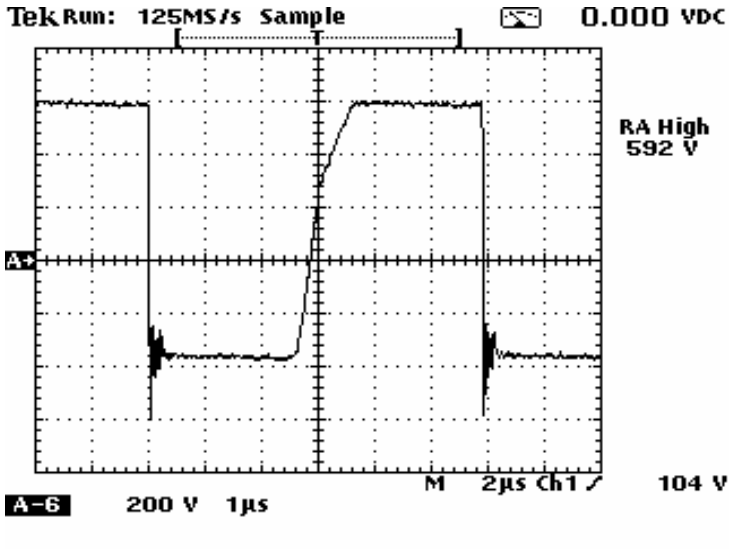


FIG: 6.2.12 Voltage across Transformer Primary with 600 VDC input

After getting successful results and waveform for open loop configuration in DEFC, it was experimented in close loop. Then we have started with 400VDC were regulation loop starts and it tries to regulate the output. From this voltage to full rating it is regulating output. Master output is regulated perfectly but cross regulation is quite poor. Slave secondary has output completely depending upon still transformer secondary turn ratio. In FIG: 6.2.13 to FIG: 6.2.18 it is shown for full rated voltage input.

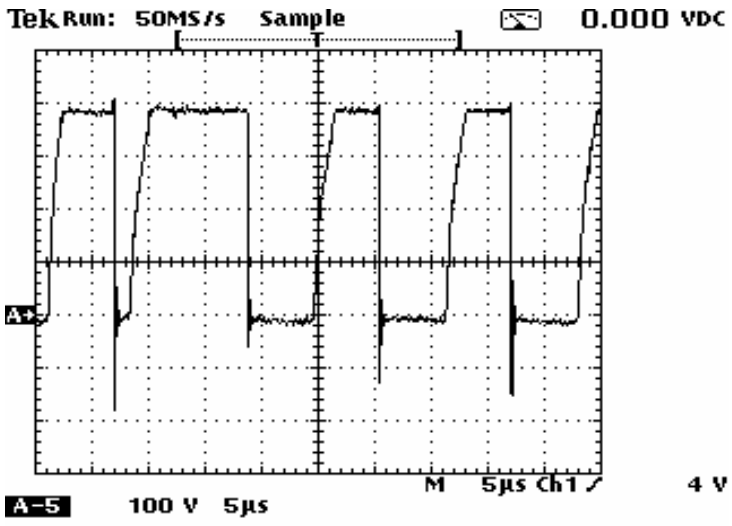


FIG: 6.2.13 Voltage across MOS with 400 VDC input (Close Loop)

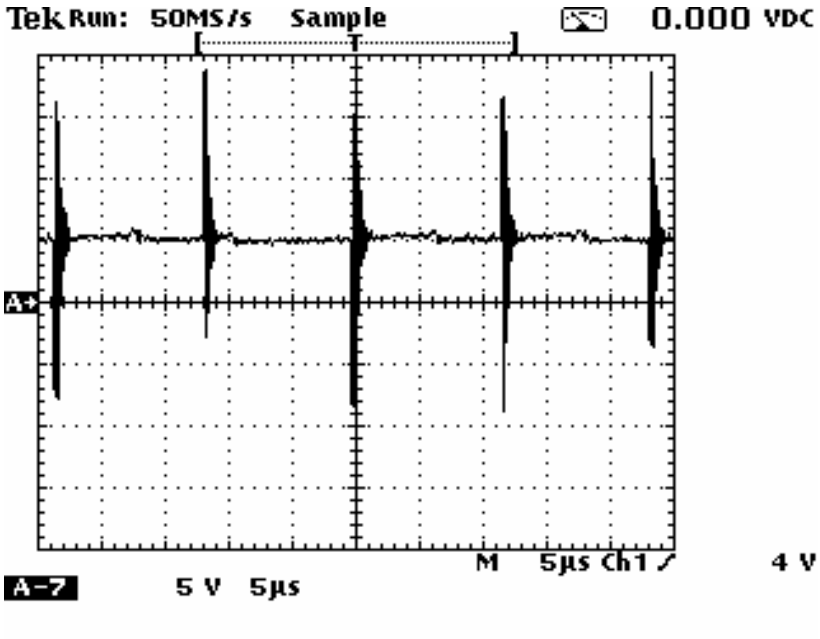


FIG: 6.2.14 Output of Master Secondary at 400VDC input

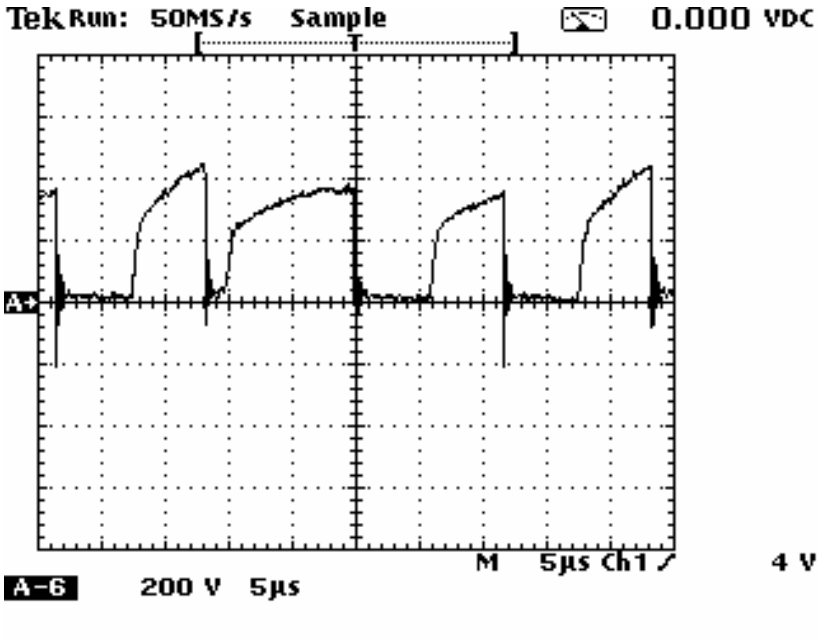


FIG: 6.2.15 Voltage across MOS with 500 VDC input (Close Loop)

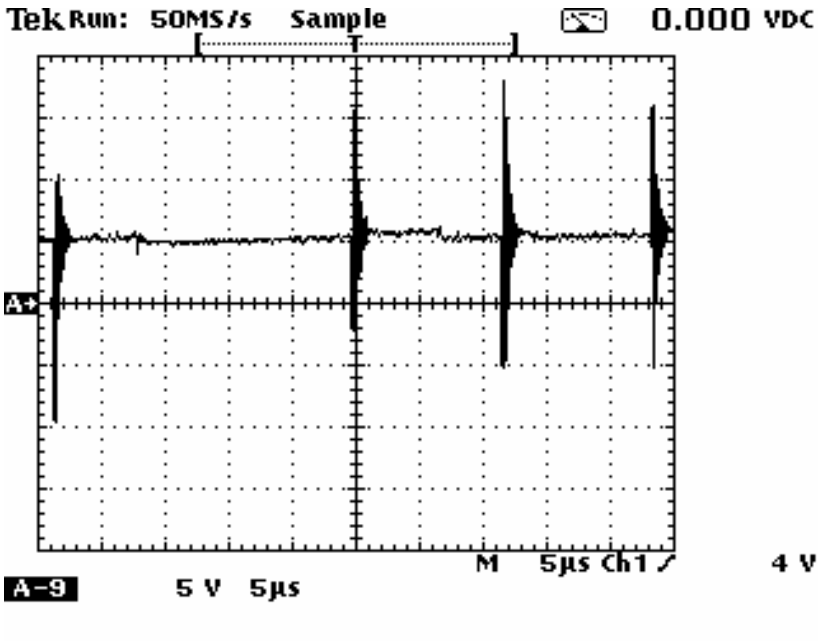


FIG: 6.2.16 *Output of Master Secondary at 500VDC input*

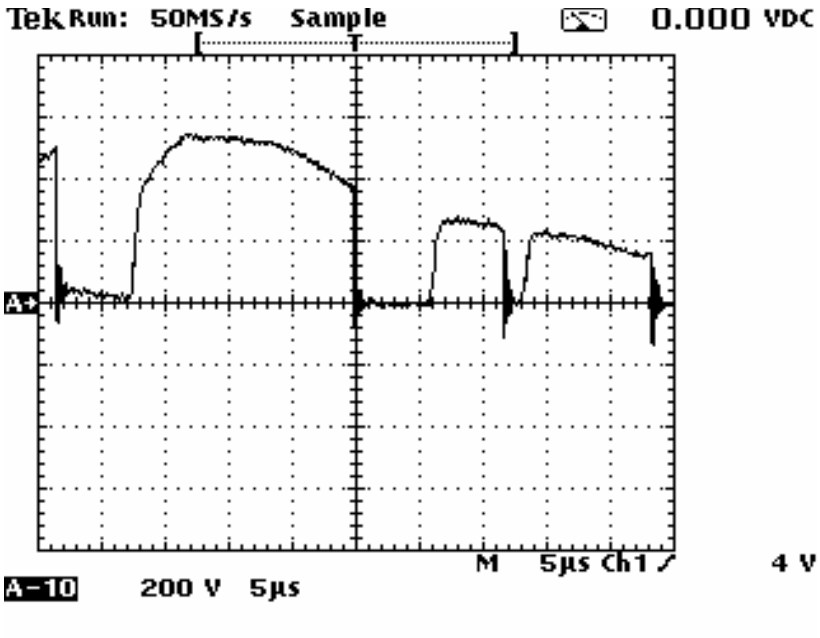


FIG: 6.2.17 Voltage across MOS with 585 VDC input (Close Loop)

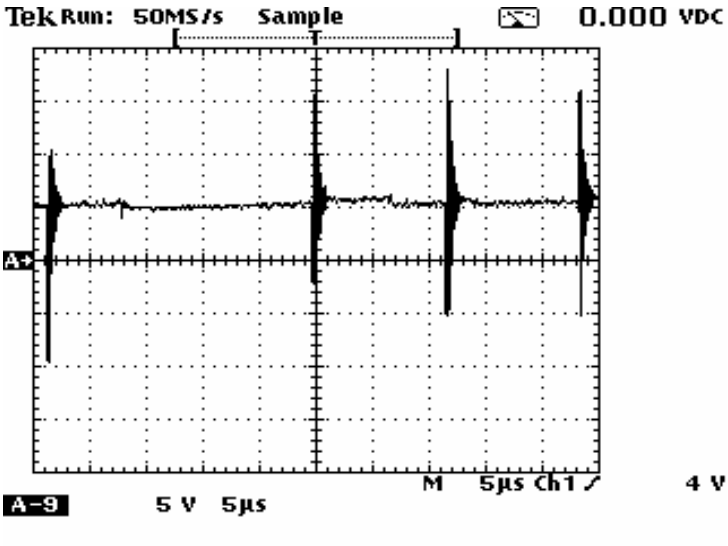


FIG: 6.2.18 *Output of Master Secondary at 585VDC input*

Till FIG 6.2.18 all waveforms across switch and regulated output are up to nominal voltage input to the Switched Mode Power Supply. As our converter is designed for 750V DC input, it should be tested for peak performance too. After finishing Nominal voltage test, peak performance test was also carried out. That is done in order to take care about the input power fluctuation and some spikes etc. So peak performance test was carried out at FULL LOAD and waveforms were recorded as mentioned in following fig 6.2.19.

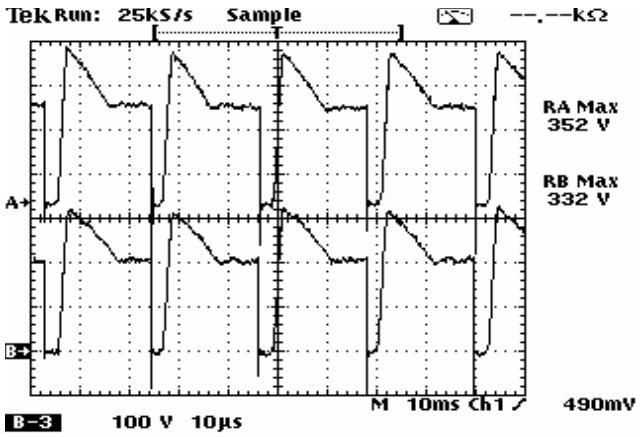


FIG: 6.2.19 Waveform across both MOSFETs Q1&Q2 with 650 VDC input

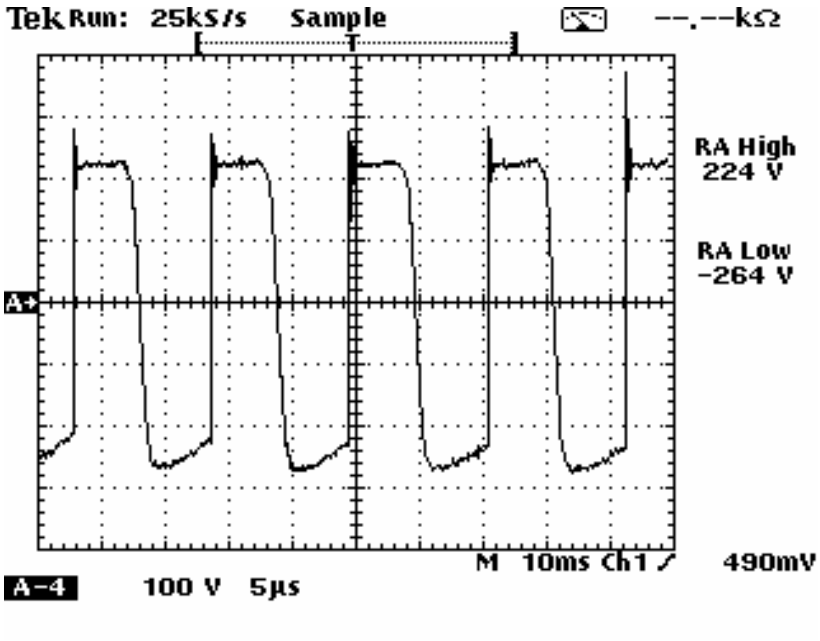


FIG: 6.2.20 Waveform across Transformer Primary with 650 VDC input

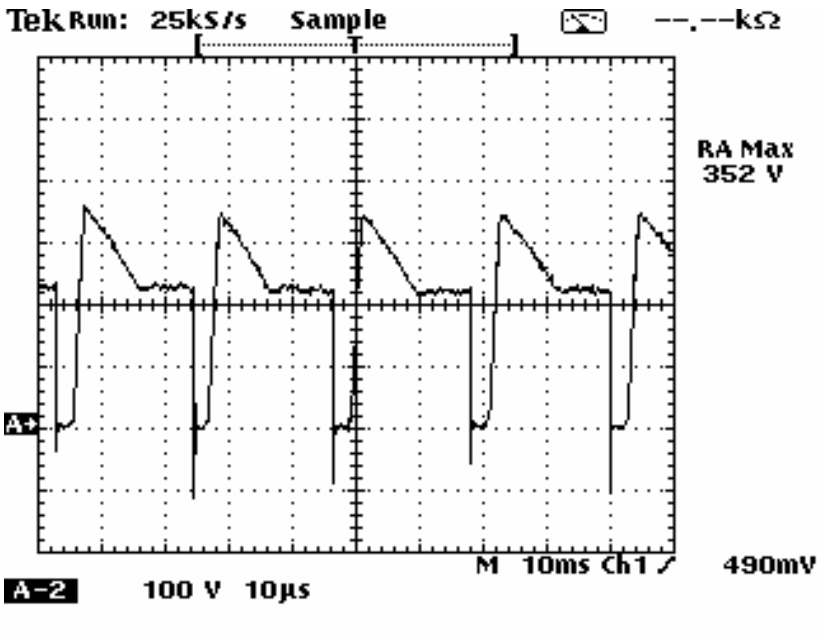


FIG: 6.2.21Waveform across MOSFET Q1 with 727 VDC input

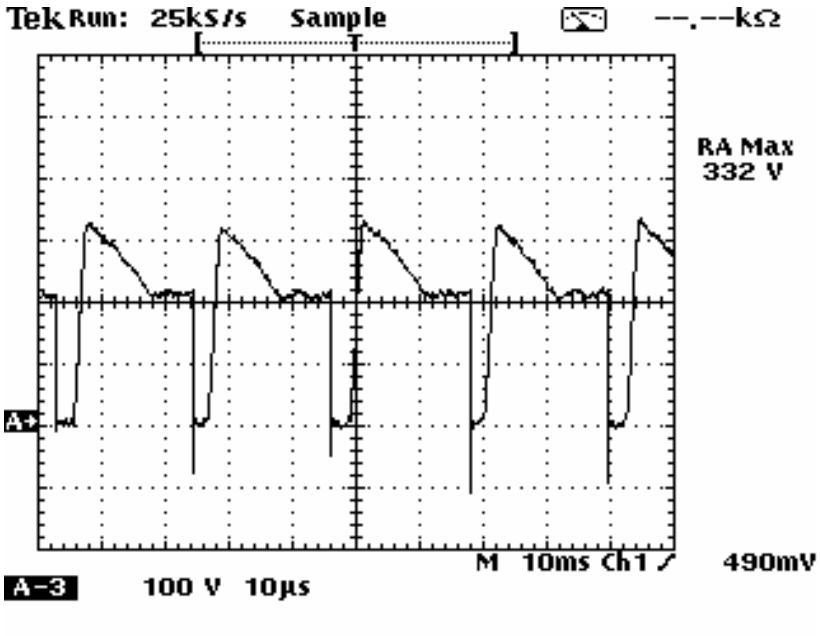


FIG: 6.2.22Waveform across MOSFET Q2 with 727 VDC input

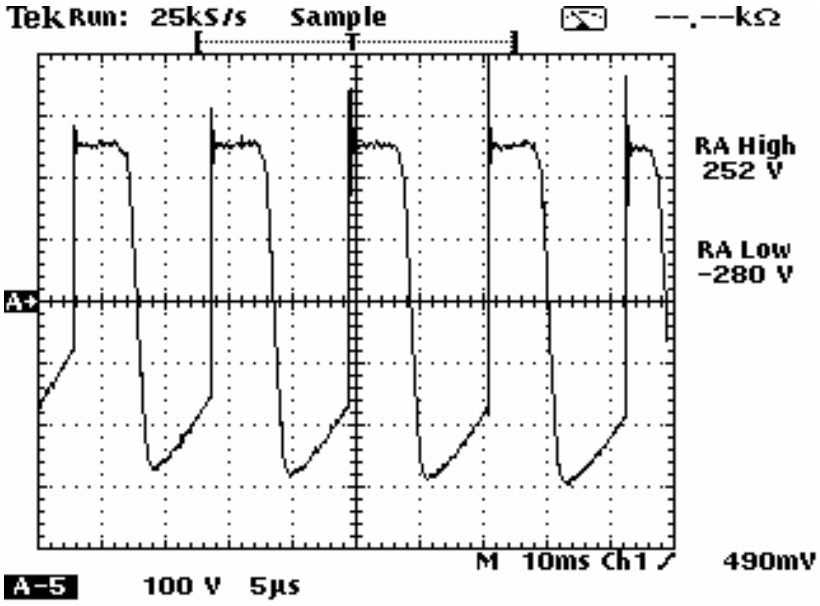


FIG: 6.2.23Waveform across Transformer Primary with 727 VDC input

Thus DEFC was successfully tested under all the load conditions and max input DC voltages. The afterwards this performance of DEFC was cross checked by other control scheme also & have got the same performance indexes.

6.3 Flyback Converter Experimental Results

After finishing DEFC topology of SMPS, the next topology was fabricated and tested for all loading and max & min regulating input voltages. Flyback topology was fabricated for full rated configuration and testing was started in steps and initially it was checked for *OPEN loop* configuration and after that it was tested for close loop operation. The waveforms stored are shown in figures shown below.

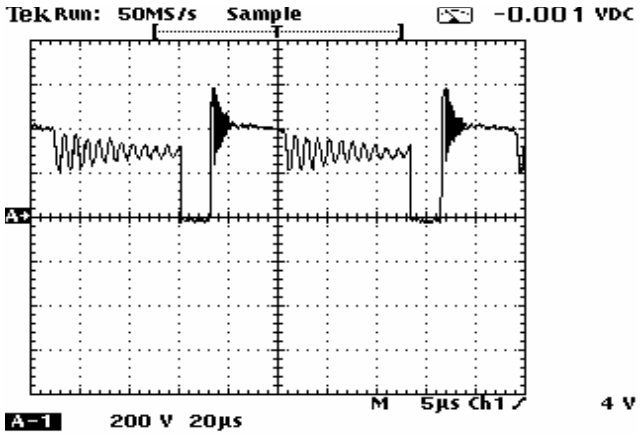


FIG: 6.3.1 Waveform across IGBT with 400 VDC input under regulation loop

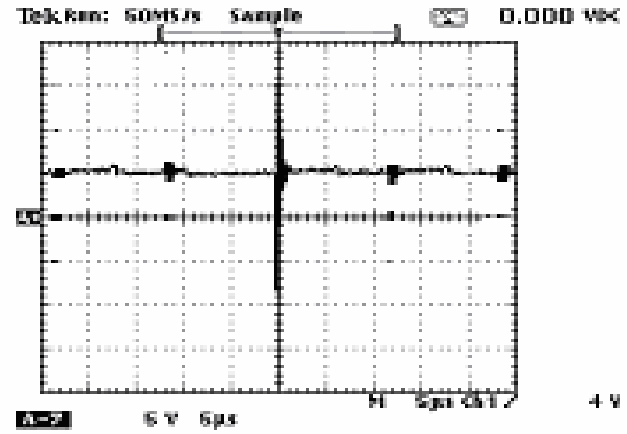


FIG 6.3.2 Master Secondary output at 400VDC input

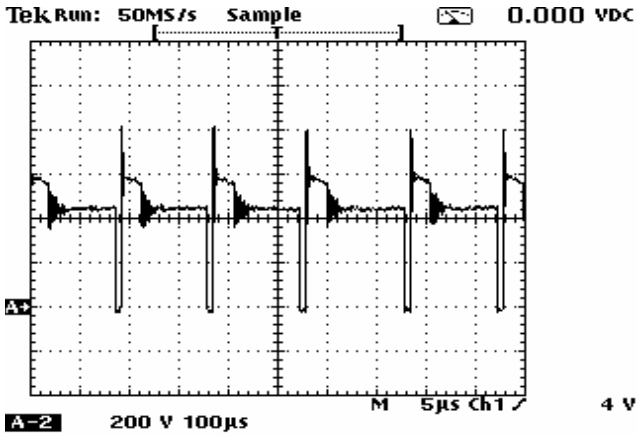


FIG: 6.3.3 Waveform across IGBT with 600 VDC input under regulation loop

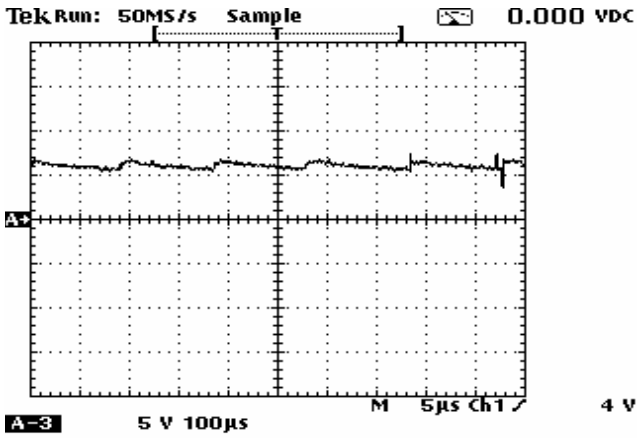


FIG 6.3.4 Master Secondary output at 600VDC input

Fig 6.3.4 clearly shows the effect of C-filter in the output waveform in the master secondary of the Flyback topology. As this is master secondary, feedback is taken from this side only so to avoid such problem Post filter was designed and that was provided to smoothen the master secondary output. That was achieved and regulated output tuned at 5V across master secondary was recorded shown in FIG: 6.3.5.

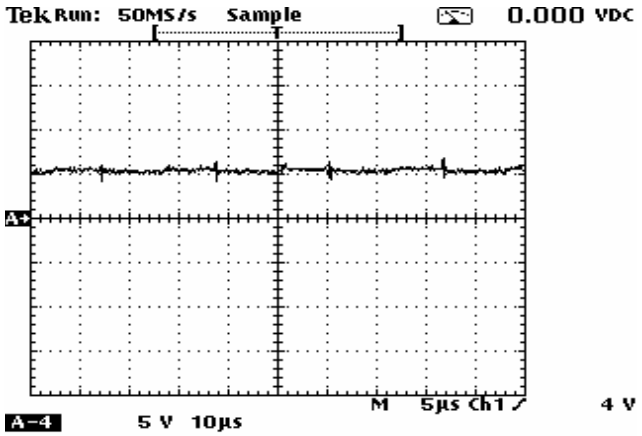


FIG: 6.3.5 *Master Secondary output at 600VDC input with post filter.*

Thus for Flyback topology also successful max voltage regulation testing was carried out. For min voltage and max voltage waveforms with regulation loop clearly indicates successful operation of Flyback Converter. After this last and innovative topology is to be seen is Flyback Integrated TOPSwitch Converter.

6.4 Flyback Integrated TOPSwitch Converter

This topology is the Hybrid topology of Flyback with TOPSwitch scheme. Here as mentioned earlier to reduce individual rating of device in Flyback topology TOPSwitch is introduced with conventional switch. That was commissioned and tested for all input & load range. Regulation was achieved after 350V DC; hence this converter's regulation range can be defined after 350VDC only. It is regulating output voltage for its span of DC input. Those waveforms are recorded and shown in following FIG: 6.4.1.

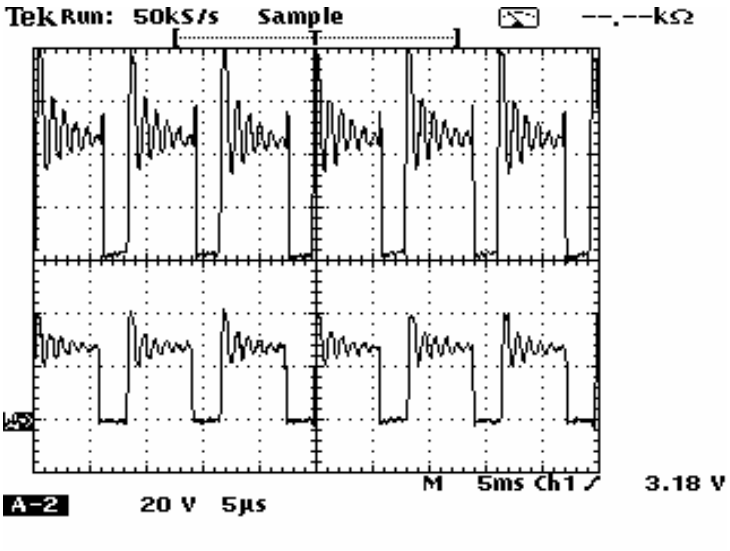


FIG: 6.4.1 Waveforms across TOPSwitch & Auxiliary Switch for 350V DC input

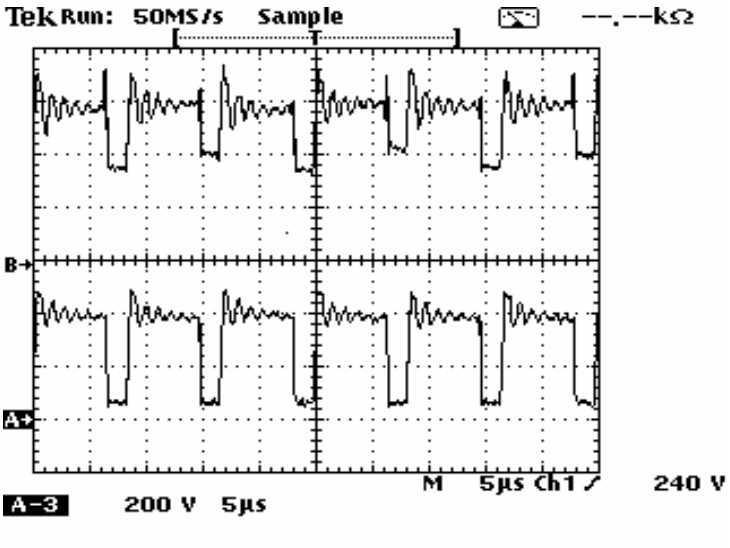


FIG: 6.4.2 Waveforms across TOPSwitch & Auxiliary Switch for 600V DC input

Thus integrated TOPSwitch Flyback Converter was also tested and commissioned after that for all converters LOAD Regulation test and Line regulation test was carried out. The results were recorded and presented in the next section.

6.5 Regulation Tests

DEFC Line Regulation at Fixed LOAD

Table A

Sr No	INPUT DC	Max Stress to Switch	Master Secondary O/P(Volt)	Slave Secondary O/P(Volt)
1	50	63	0.46	1.88
2	100	118	1.13	3.88
3	150	175	1.77	5.83
4	200	280	2.39	7.70
5	250	316	2.78	8.88
6	300	390	3.51	11.10
7	350	420	3.88	12.58
8	400	485	4.31	13.90
9	450	512	4.89	14.89
10	500	583	5.01	14.98
11	550	620	5.03	14.97
12	580	693	5.02	14.96
13	600	729	5.12	15.12
14	650	843	5.15	15.14

Flyback Line Regulation at Fixed LOAD

Table B

Sr No	INPUT DC	Max Stress to Switch	Master Secondary O/P(Volt)	Slave Secondary O/P(Volt)
1	50	110	2.06	7.19
2	100	219	4.91	16.44
3	150	330	5.01	16.70
4	200	432	4.98	16.37
5	250	512	5.02	16.50
6	300	610	5.02	16.45
7	350	720	5.30	18.10
8	400	800	5.30	18.20
9	450	820	5.31	18.22
10	500	899	5.32	18.29
11	550	1030	5.32	18.30
12	580	1135	5.33	18.40

For DEFC Load Regulation Test max 30Watt.

Line input 600DC

Sr No	Loading (%)	Master Output (V)	Slave Output (V)
1	25	5.17	14.98
2	50	5.15	14.93
3	75	5.15	14.90
4	100	5.11	14.86

For DEFC Load Regulation Test max 30Watt.
Line input 580DC

Sr No	Loading (%)	Master Output (V)	Slave Output (V)
1	25	5.13	15.05
2	50	5.13	15.00
3	75	5.05	14.93
4	100	5.00	14.88

For Fly back Load Regulation Test max 30Watt.
Line input 600DC

Sr No	Loading (%)	Master Output (V)	Slave Output (V)
1	25	5.45	18.90
2	50	5.31	18.41
3	75	5.30	18.17
4	100	5.30	17.59

For Fly back Load Regulation Test max 30Watt.
Line input 580DC

Sr No	Loading (%)	Master Output (V)	Slave Output (V)
1	25	5.40	18.49
2	50	5.33	18.30
3	75	5.31	18.04
4	100	5.30	17.60

Line regulation of Flyback Integrated TOPSwitch Converter at Fixed LOAD

Table C

Sr No	INPUT DC (V)	Master Secondary Output(V)	Slave Secondary Output(V)
1	50	0	0
2	100	0	0
3	150	4.2	11.35
4	300	4.9	19.85
5	400	5.01	19.95
6	450	5.00	20.00
7	500	5.02	20.01
8	550	5.02	20.02
9	585	5.01	20.01
10	600	5.00	20.00

LOAD Regulation Test at 30W and 620 V DC input for Int. TOPS

Table D

Sr No	Loading (%)	Master Output (V)	Slave Output (V)
1	25	5.14	21.05
2	50	5.05	20.40
3	75	5.02	20.05
4	100	5.01	20.03

6.6 Regulation Statistics

DEFC:

Line Regulation:

Master Regulation = 5.31%

Cross Regulation = 1.07%

Load Regulation:

Master Regulation: 1.16%

Cross Regulation: 0.80 %

Flyback:

Line Regulation:

Master Regulation = 6.00%

Cross Regulation = 10.17%

Load Regulation:

Master Regulation= 2.80%

Cross Regulation= 7.45 %

Integrated TOPSwitch:

Line Regulation:

Master Regulation = 2.00%

Cross Regulation = 0.75%

Load Regulation:

Master Regulation= 2.52%

Cross Regulation= 4.84%

Chapter-7

PHOTOGRAPHS OF HARDWARE

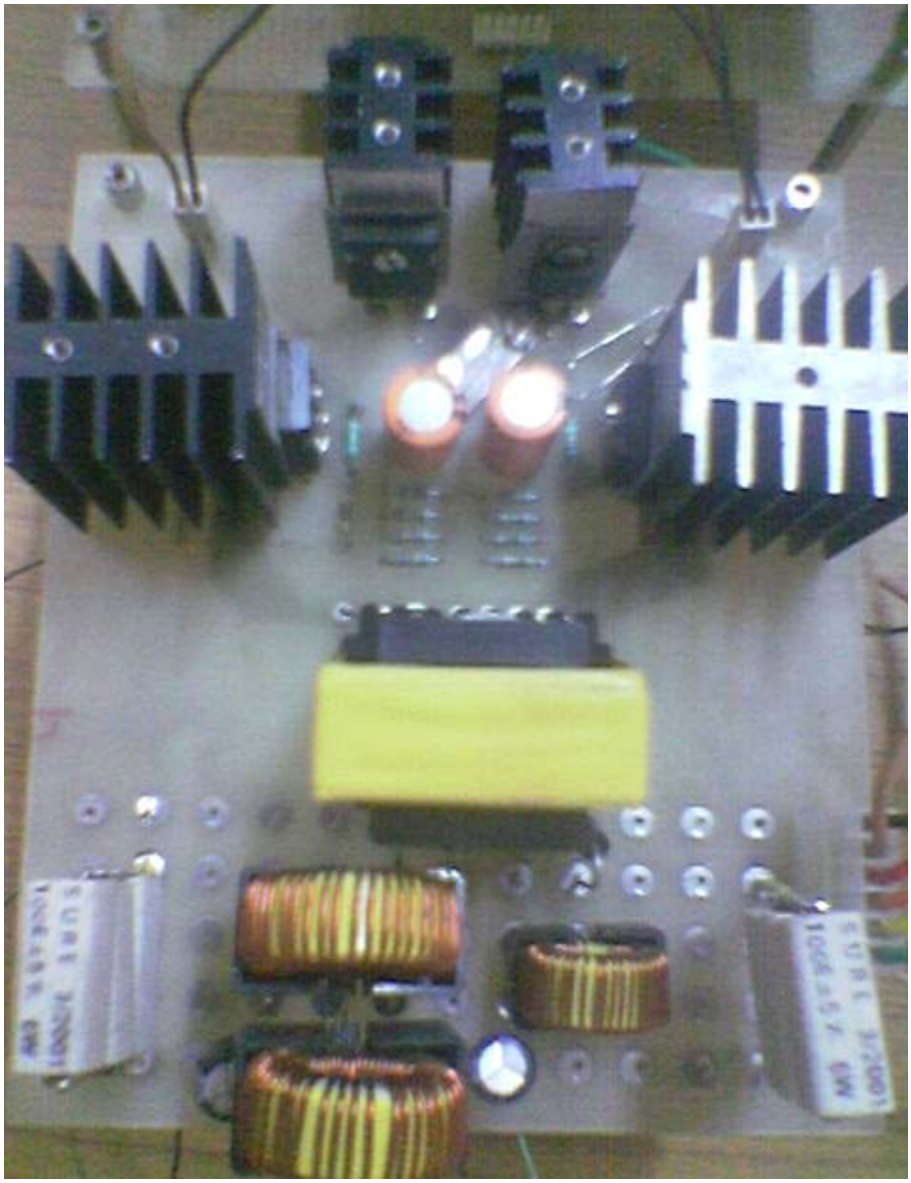


FIG: 7.1 DEFC Power Card

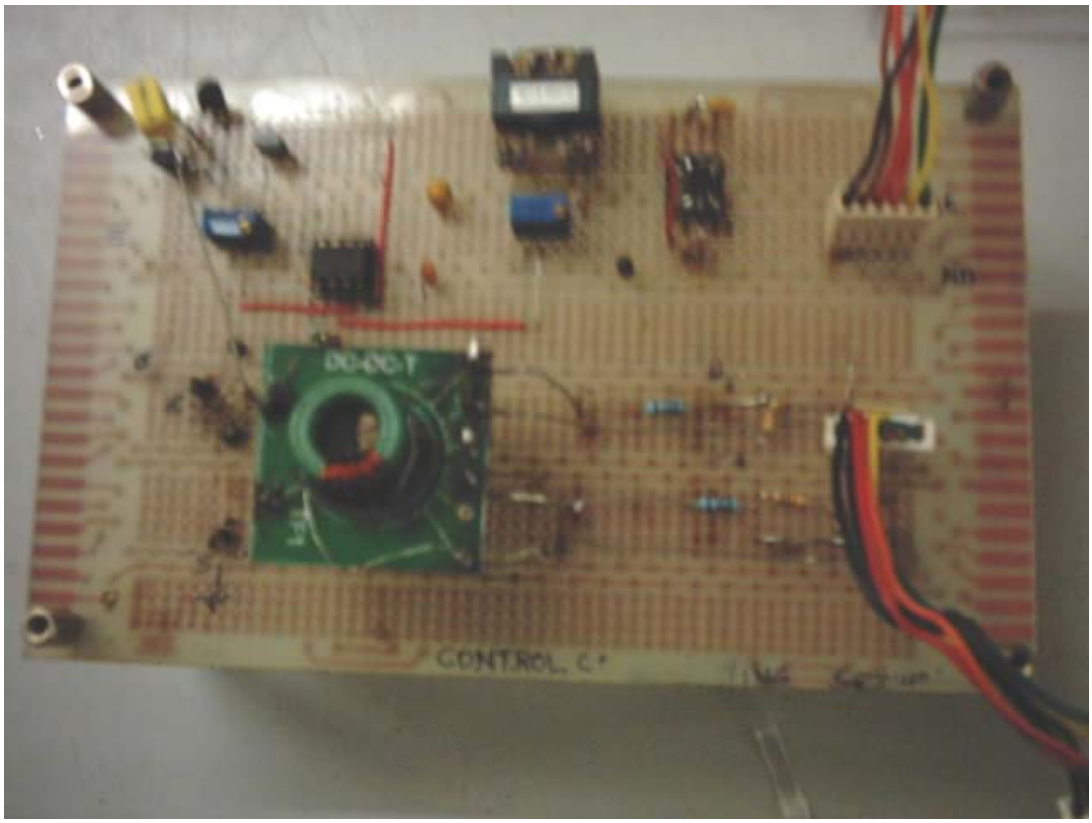


FIG: 7.2 DEFC Control Card

FIG: 7.3 DEFC Assembly

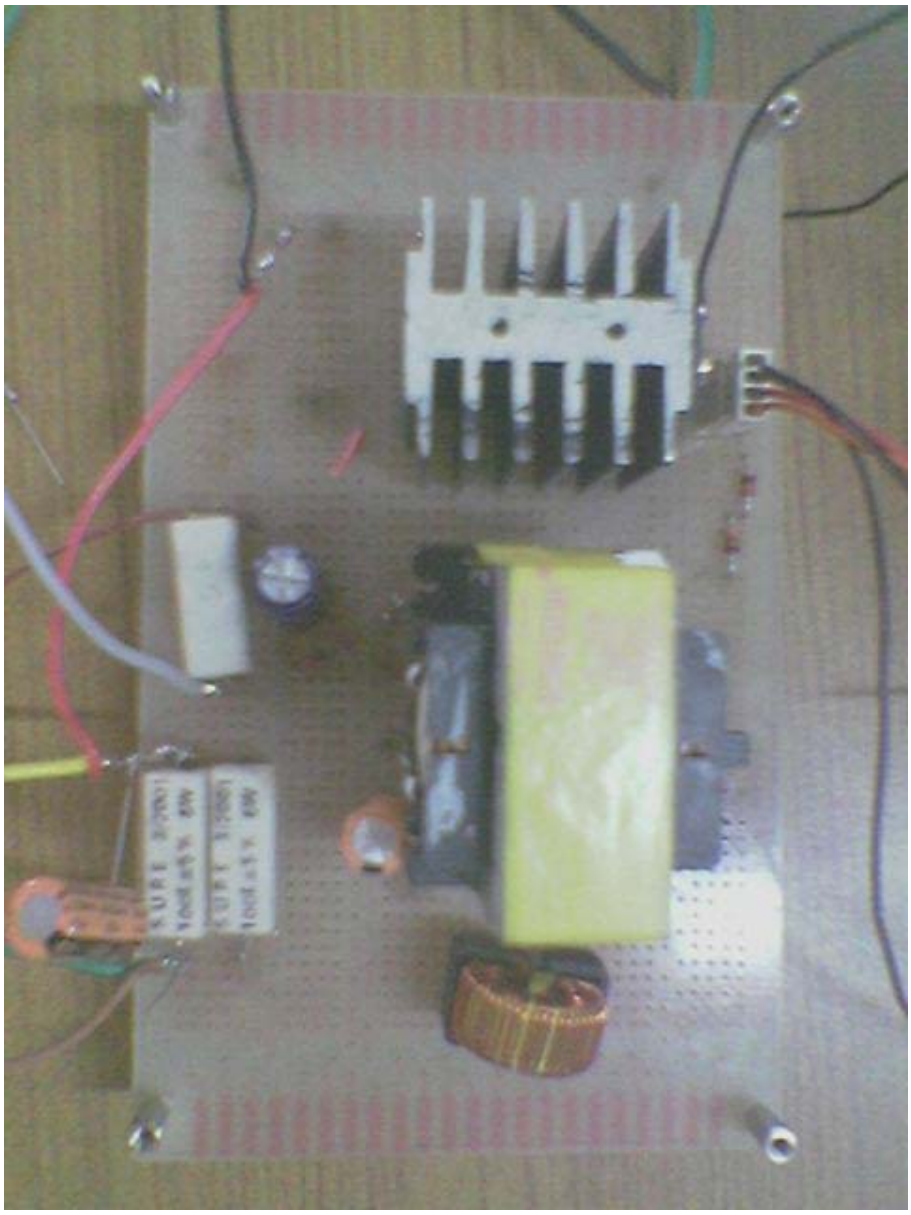


FIG: 7.4 Flyback Power Card

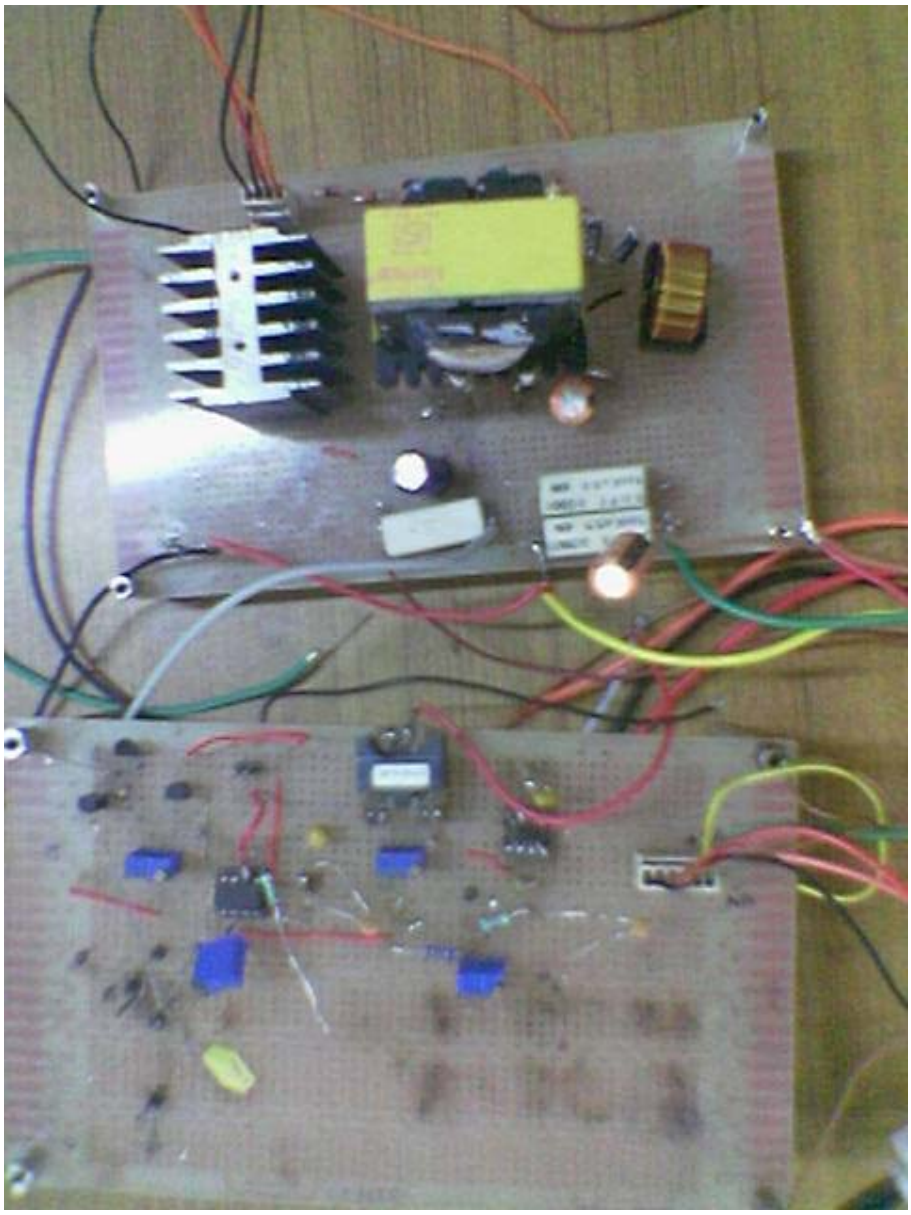


FIG: 7.5 Flyback Converter Assembly

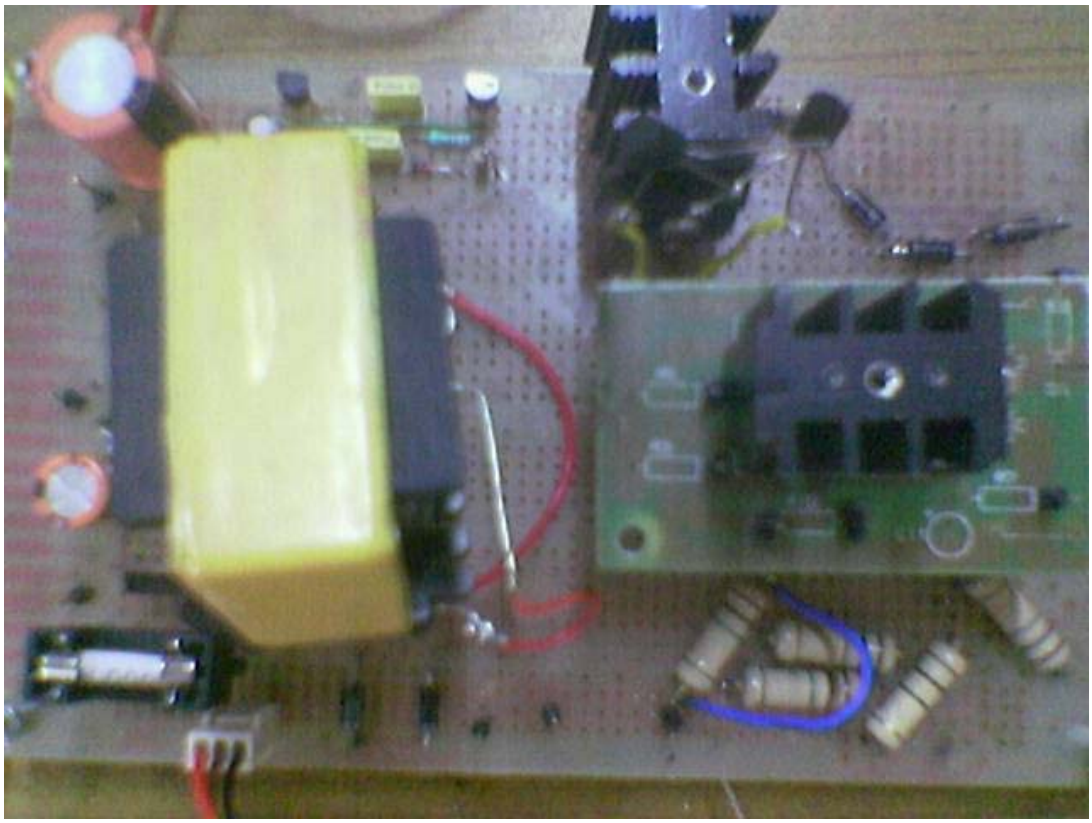


FIG: 7.6 Flyback integrated TOPSwitch Converter

Chapter-8

CONCLUSION & FUTURE SCOPE

Experimental results show very clearly that DEFC topology is the one of the economic solutions while implementing the Switch Mode Power Supply working on high input voltage. And performance achieved is also the accurate one. In control circuit, firing pulses generated are of voltage magnitude 15V which satisfies MOS driving requirements. And off State voltages across MOS are equal to V_{DC} applied.
So MOS choice becomes economic. And with this configuration developed DC voltage after filter stage is smooth with very low ripple content.

In the case of Flyback Topology good regulation is achieved and also fewer components are used. But the initial cost of high Voltage IGBT is quite high, which makes it costlier.

Integrated TOPSwitch seems to be the best solution. As TOP Switch is used no more External components are used, perfect regulation is achieved. It is light weight, compact and most economic solution.
A Performance Comparison Table of all the Topologies facilitates us to choose the proper solution for our particular need.

PERFORMANCE TABLE

	DEFC	Flyback	TOPSwitch
Performance	3	2	1
Cost	2	3	1
Weight	3	2	1
Size	3	2	1
Start-UP	2	2	1
Complexity	1	2	3

Table E

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- Application Notes of UNITRODE
- Application Notes of Texas Instruments
- Application Notes of Power Integration

APPENDIX

Line Regulation:

%Line Regulation in Voltage for SMPS = $\frac{Vonl - Vorated}{Vorated} \times 100$

Load Regulation:

%Load Regulation in Voltage for SMPS = $\frac{Vonl - Vorated}{Vonl} \times 100$