Computer Aided Optimized Design and Simulation of Synthetic Test Circuit for Testing 800kV Rating Circuit Breakers

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Abstract— **Development in electrical power transmission system requires the use of circuit breakers with increasing breaking capacity. At present circuit breakers are to be installed on 245 kV to 1100 kV power system with short circuit ratings up to 120kA. To test high voltage CBs, direct testing using the power system or short circuit alternators are not feasible. The testing of high voltage CBs of larger capacity requires very large capacity of testing station. To increase testing plant power is neither an economical nor a very practical solution. Synthetic testing is an alternative equivalent method for testing of high voltage circuit breakers and is accepted by the standards.**

This paper presents a TRV rating concepts , IEC standards TRV envelopes and types of synthetic test circuits and their comparison. Analysis and mathematical modeling of 4-parameters TRV synthetic test circuit is presented. In order to find the possible combinations of circuit components and to optimize the values of capacitance of capacitor banks for the desired frequencies of a particular rating of circuit-breaker, the program/software has been developed by using MATLAB and Visual Basic 6. Design and simulation of 4-parameters TRV synthetic testing circuit (Weil - Dobke type) is done by using PSIM simulator as per new TRV requirements given in IEC 62271-100 (2008). The circuit is designed and simulated for both terminal faults as well as short line faults test duty for 800kV rating circuit-breakers.

Keywords- A.C. high voltage circuit breakers, direct testing, synthetic tests, TRV circuits, Terminal and Short-line faults.

I. INTRODUCTION

In synthetic testing, there are two sources of power supply for the testing.

(i) Current source (ii) Voltage source

The current source is a high current, low voltage source. It supplies short circuit current during the test. The voltage source is a high voltage low current source. It provides restriking and recovery voltage.

The synthetic testing circuit is shown in Fig.1, where inductance L1 is to control the short circuit current. The master CB is used as backup circuit breaker. If the CB under test (TB) fails to operate, the master CB opens. Make switch is used to apply short circuit current at the desired moment during the test. For the operation of the circuit, First of all the MB and TB are closed. Then the short circuit current is passed by closing Make switch (MS). The short circuit current is interrupted by opening the circuit breaker under test at desired moment. The closing and opening of the circuit breakers at the desired moment is done by the Automatic controller.

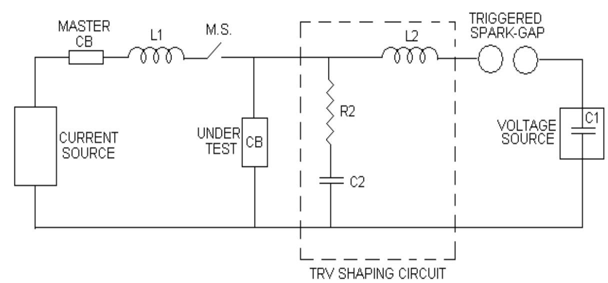

Fig.1. Synthetic testing circuit

The capacitor C1 is a high voltage source. L2, R2 and C2 are to control transient recovery voltage and RRRV. The triggered spark gap is fired slightly before the short circuit current reaches its natural zero. There is a control circuit to fire the triggered spark gap at the desired moment. The advantages of synthetic testing are as follows:

- The breaker can be tested for desired TRV and R.R.R.V.
- The short-circuit generator has to supply current at a relatively less voltage (as compared to direct testing).
- Both test current and test voltage can be independently varied. This gives flexibility to test. The method is simple.

II. TYPES OF SYNTHETIC TEST CIRCUIT AND COMPARISON

Several synthetic testing methods have been developed and their performances have been studied in the past forty years[4],[8-13]. If the source of energy during the interaction interval is used to classify the methods adopted, they can be distinguished by two basic methods:

(i) Current injection and
(ii) Voltage injection method.

Depending on whether voltage circuit or source is switched on before or after current zero, the type of synthetic testing is known as current injection or voltage injection respectively.

Further the current injection method can be classified as parallel current injection and series current injection method.

In parallel current injection method, the voltage circuit is inserted in parallel with the test breaker, while in series current injection method, it is inserted in series. The parallel current injection type synthetic testing is popular in Germany and is known as Weil - Dobke circuit. The series current injection type synthetic test circuit was suggested by Kaplan Bashatyr (U.S.S.R) and is known as Russian circuit. In voltage injection method, the voltage source is switched on after the current zero. This method was suggested by Siemens, Germany.

More than forty years of synthetic testing experience shows that the current injection method has better equivalence than the voltage injection method. To produce four-parameter TRV, several TRV circuits have been developed but parallel current injection method with a Weil-Dobke TRV control circuit is the most popular used synthetic testing circuit in the high power laboratories as it is capable of providing RRRV and recovery voltage as required by various standards. Weil-Dobke circuit has a low capacity requirement on the main capacitor bank as compared to other TRV control circuits and is easy to design the various components. However, special attention should be paid on the insulation coordination of TRV branches.

III. TRV Rating Concepts and IEC Standards TRV Envelopes

As per IEC 62271-100, the rated characteristics of a circuit breaker include rated transient recovery voltage for terminal faults as well as short line fault condition.

A. Interruption of terminal faults:

The terminal fault is defined as a fault occurring very near to the terminal of the circuit breaker and that the reactance between the fault point and breaker is negligible.

Under this condition, the fault or short circuit current depends upon the source voltage and source impedance, as the impedance between the breaker and the fault is negligible. After the arc extinguishes at natural zero, the circuit recovers and TRV appears across the breaker pole.

B. Interruption of short line faults:

The faults occurring between a distance of a few km to a few tens km from the circuit breaker are called the short line or kilometric faults. Such faults are characterized by high frequency of restriking voltage of the order of 10 to 100kHz depending upon the line length and fault location. The resulting TRV for short line fault appearing across CB pole is the vector sum of the voltage from the source and the line side.

Short circuit tests on High voltage circuit-breakers require circuit with response specified by IEC standards[3] represented by either Fig. 2 or Fig. 3.

IEC standards define two TRV envelopes [3],[7].

A. Case of two parameters

For circuit breakers rated less than 100 kV, the envelope is defined by the two parameter method.

u_c = reference voltage (TRV peak value) in kV;

t_3 = time to reach u_c in microseconds.

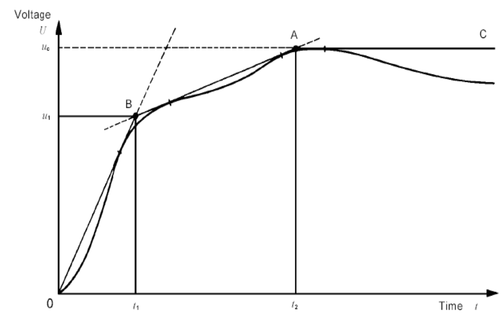

Fig.2. Representation by four parameters (u_1 and t_1, u_c and t_2) of a prospective transient recovery voltage of a circuit , **case-1**

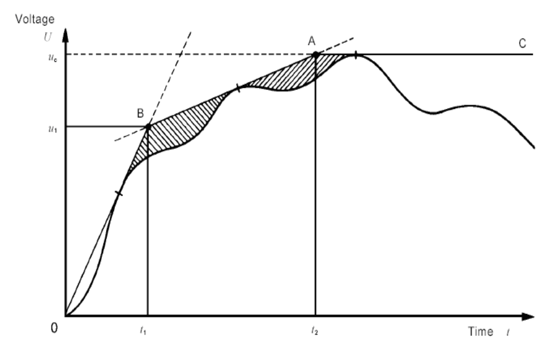

Fig.3. Representation by four parameters (u_1 and t_1, u_c and t_2) of a prospective transient recovery voltage of a circuit **case-2**

B. Case of four parameters

For circuit breakers rated 100kV and above, the TRV envelope is defined by the four-parameter method represented by either Fig.2 or Fig.3.

u_1 = first reference voltage, in kV,

t_1 = time to reach u_1, in microseconds

u_c =second reference voltage(TRV peak value), in kV

t_2 = time to reach u_c in microseconds.

TRV parameters are defined as a function of the rated voltage(U_r), the first-pole-to-clear factor (k_{pp}) and the amplitude factor(k_{af}) as follows:

$$u_1 = 0.75x\ (k_{pp})\ x\ U_r \sqrt{\frac{2}{3}}$$

t_1 is derived from u_1 and the specified value of the rate of rise u_1/t_1=RRRV.

$t_2 = 4t_1$ for terminal fault and short line fault;

For rated voltages equal or higher than 100kV, the time delay $t_d = 2$ μs for terminal fault and short line fault;

$$u_c = k_{af} \times k_{pp} \times U_r \sqrt{\frac{2}{3}},$$

Where $k_{af} = 1.4$ for terminal and short line fault;

$k_{pp} = 1.3$ for terminal fault

$= 1.0$ for short line fault

IV. Analysis and Mathematical Modeling of 4 -Parameters TRV Synthetic Test Circuit

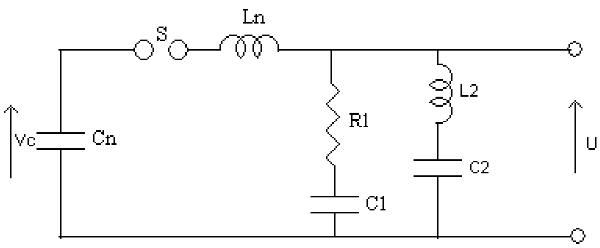

Fig.4. Multi frequency circuit

The circuit shown in Fig.4 permits to produce 4– parameters transient recovery voltages (TRV) according to IEC standards. Vc is the charging voltage. Cn, C1, C2, Ln, L2 and R1 are the circuit components. The magnitude and the frequency of the transient recovery voltage depend on the voltage to which the capacitor Cn is charged and the values of circuit components. u is the transient recovery voltage. C1, C2, Ln, L2 and R1 are to control TRV and RRRV.

The expression for the transient recovery voltage is as follows:

$$u(s) = -\frac{CnVc}{s}\cdot\frac{(1+sR1C1)(1+s^2L2C2)}{s^4 LnCnL2C2C1 + s^3 R1CnC1C2(Ln+L2) + s^2\left[LnCn(C1+C2)+L2C2(Cn+C1)\right] + sR1C1(Cn+C2)+Cn+C1+C2}$$

The time expression of the recovery voltage is complex, but by making some hypotheses, it is possible to obtain some fundamental information concerning the TRV generated by this configuration[11]. Indeed, a simple analysis of the position of the poles of the above mentioned expression reveals the existence of 2 frequencies:

A. Low Frequency Circuit

The low frequency voltage wave corresponds to the natural oscillation of the circuit represented by Fig.5. This low frequency circuit consists of circuit components Cn, C2, Ln and L2.

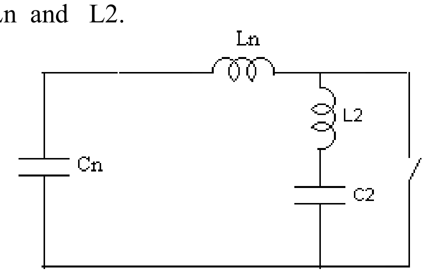

Fig.5. Low frequency circuit

$$fn_2 = \frac{1}{2\pi\sqrt{(Ln + L2).\dfrac{Cn \times C2}{Cn + C2}}}$$

$$\therefore t_{m2} = \frac{10^3}{2 \times fn_2} \qquad (1)$$

Where

fn_2 = low frequency oscillation of the voltage wave, kHz

t_{m2} = Time to reach peak of low frequency voltage wave, μs

B. High Frequency Circuit

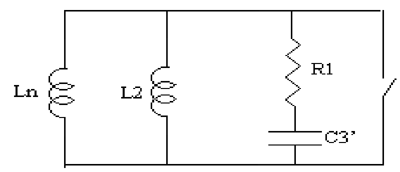

Fig.6. High frequency circuit

The high frequency voltage wave arises from the free oscillation of the circuit shown in Fig.6. The value of high frequency depends upon the circuit components $C3'$, Ln and L2.

$$C3' = C1 \times \frac{Cn + C2}{Cn + C1 + C2}$$

$$Leq = Ln \parallel L2 = \frac{Ln \times L2}{Ln + L2}$$

$$fn_1 = \frac{1}{2\pi\sqrt{Leq \times C3'}}$$

$$\therefore t_{m1} = \frac{10^3}{2 \times fn_1} \qquad (2)$$

Where

fn_1 = high frequency oscillation of the voltage wave, kHz

t_{m1} = time to reach peak of high frequency voltage wave, μs.

The TRV can then be considered as a result of the oscillations of both low frequency and high frequency circuits.

V. Design and Simulation of 4-Parameters TRV Synthetic Test Circuit

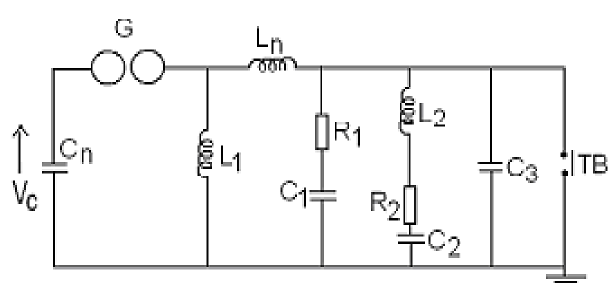

Fig.7. 4 parameters TRV synthetic testing control circuit

To produce four-parameter TRV, several TRV circuits have been developed but parallel current injection method with a Weil-Dobke TRV control circuit shown in Fig.7 is the most popular used synthetic testing circuit in the high power laboratories as it is capable of providing RRRV and recovery voltage as required by various standards. Weil-Dobke circuit has a low capacity requirement on the main capacitor bank as compared to other TRV control circuits and is easy to design the various components. This circuit permits to produce 4 – parameters transient recovery voltages (TRV) according to IEC standards.

Program/Software development for finding circuit components:

For the design optimization of 4-parameters TRV control circuits, the independent variables x_1, x_2, x_3, x_4 and x_5 may be chosen as follows:
x_1 = Capacitance of the main capacitor bank , Cn in µF
x_2 = Capacitance of TRV capacitor bank-I, C1 in µF
x_3 = Capacitance of TRV capacitor bank-II, C2 in µF
x_4 = Inductance of reactor Ln in mH
x_5 = Inductance of reactor L2 in mH.

The objective function chosen:
Minimize the value of capacitance (hence energy required or size of the capacitor banks) of capacitor Banks for the same test conditions (same TRV parameters for a particular rating of circuit-breakers).
The constraints function gi (x_1, x_2, x_3, x_4, x_5) consists of the following:
g_1 = tm_1 = time to reach peak of high frequency voltage wave, in µs.
g_2 = tm_2 = time to reach peak of low frequency voltage wave, in µs.

In order to find the possible combinations of circuit components and to optimize the values of capacitance of capacitor banks for the desired frequencies tm_1 and tm_2 of a particular rating of circuit-breaker, program has been developed by using MATLAB M-file. Design optimization is done to reduce the values of capacitance of capacitor banks and hence reduce the energy required, size and cost of the capacitor banks.

Program/software is also developed with the help of VISUAL BASIC 6 software to find all possible combinations of the circuit components and also to optimize the circuit components for the desired frequencies tm_1 and tm_2 for a particular rating of circuit-breaker. This software is user friendly and speed is very fast, just by one click it will show all the possible combinations of circuit components for the desired frequencies. The flow chart or the algorithm to find optimized circuit components is shown in Fig.8.

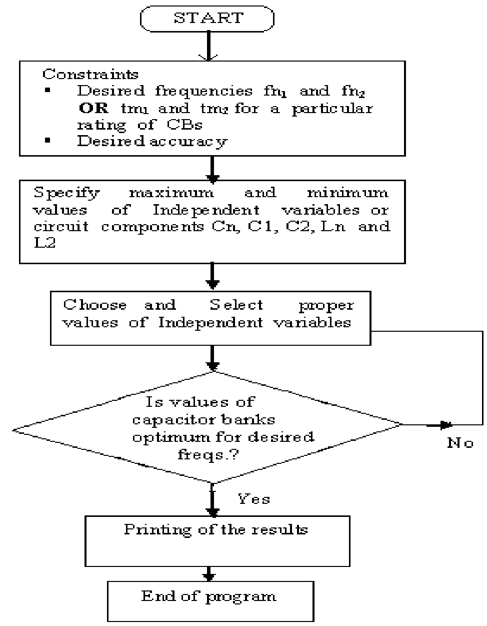

Fig.8. Flowchart for finding optimized circuit components

Example of finding optimized circuit components for a given position of poles or frequencies fn_1 and fn_2 (tm_1 and tm_2) of a terminal fault test duty TRV for a 800kV rating circuit-breakers:
Input data:
Minimum value of Cn: 36e-6
Maximum value of Cn: 40e-6
Step of Cn: 2e-6

Minimum value of C1: 0.6e-6
Maximum value of C1: 1e-6
Step of C1: 0.1e-6

Minimum value of C2: 1e-6
Maximum value of C2: 3e-6
Step of C2: 0.2e-6

Minimum value of Ln: 45e-3
Maximum value of Ln: 50e-3
Step of Ln: 1e-3

Minimum value of L2: 38e-3
Maximum value of L2: 44e-3
Step of L2: 1e-3

Tm1: 430e-6
Tm2: 1300e-6

Final output:
OPTIMIZATION ###
Optimized C1
Cn = 3.600000e-005 **Ln = 4.700000e-002**
L2 = 4.400000e-002 **C2 = 1.985457e-006**
C1 = 8.426692e-007 **Tm1 = 4.300000e-004**
Tm2 = 1.300000e-003 |

Optimized C2

Cn = 3.600000e-005 Ln = 4.700000e-002
L2 = 4.400000e-002 C2 = 1.985457e-006
C1 = 8.426692e-007 Tm1 = 4.300000e-004
Tm2 = 1.300000e-003 |

After finding the optimized circuit components for the desired frequencies of fn_1 and fn_2 for 800kV, the circuit is designed and simulated by using PSIM simulator as per new TRV requirements given in IEC 62271-100. The circuit is designed and simulated for terminal fault as well as short-line fault test duty condition. The algorithm for the design and simulation of synthetic testing circuit for High Voltage circuit Breakers is shown in Fig.9. The TRV curves obtained are shown in Fig.10 to 12.

TRV parameters from these waveforms are given in Table-II. The expected TRV parameters for testing 800 kV rating circuit breakers for both terminal and short line fault test duty are given in Table-I. Design optimization is also done to reduce the energy required by the capacitor banks and hence reduce the size and cost of capacitor banks also to save the space required. Table III shows the energy required by each capacitor bank and the total energy required for terminal fault test duty condition. Table IV shows the optimal circuit components of TRV control circuit for testing 800kV rating CBs.

TABLE I
EXPECTED TRV PARAMETERS ACCORDING OF IEC FOR 800 KV RATING CIRCUIT-BREAKERS

TRV Parameters	Test duty: Terminal fault	Test duty: Short line fault
First reference voltage u_1, kV	637	490
Time to reach u_1, t_1 µs	318	245
TRV peak value , u_c kV	1189	914
Time to reach u_c, t_2 µs	1272	980
Rate of rise, u_1/t_1, kV/µs	2	2

TABLE II
TRV PARAMETERS OBTAINED FOR 800 KV RATING CIRCUIT-BREAKERS

TRV Parameters	Test duty: Terminal fault	Test duty: Short line fault
First reference voltage u_1, kV	640	486
Time to reach u_1, t_1 µs	318	244
TRV peak value , u_c kV	1189	913
Time to reach u_c, t_2 µs	1270	980
Rate of rise, u_1/t_1, kV/µs	2.01	1. 99

TABLE III
MAXIMUM VOLTAGE ACROSS EACH CAPACITOR BANK AND ENERGY REQUIREMENT FOR EACH CAPACITOR BANK FOR TESTING 800KV CBS.

Capacitor Banks	Value	Max. Voltage across capacitor Bank, kV	Energy required kJ	Total Energy reqd. MJ
Main Capacitor Bank: C_n	36 µF	807	11722.4	
TRV Capacitor Bank: C_1	0.85 µF	1185	596.80	14.60
C_2	2. 2 µF	1435	2265.14	
Stray capacitor Bank: C_3	21 nF	1189	14.85	

TABLE IV
OPTIMAL CIRCUIT COMPONENTS OF TRV CONTROL CIRCUIT FOR TESTING 800KV RATING CIRCUIT-BREAKERS

Circuit components	Terminal Fault	Short line fault
Capacitor Banks		
Main Capacitor Bank: C_n	36 µF	36 µF
TRV Capacitor Bank: C_1	0.85 µF	0.6 µF
C_2	2.2 µF	2.2 µF
Stray capacitor Bank: C_3	21 nF	21 nF
Reactors : L_n	48 mH	40 mH
L_1	200 mH	200 mH
L_2	44 mH	33 mH
Resistors : R_1	34 Ω	24 Ω
R_2	10 Ω	10 Ω

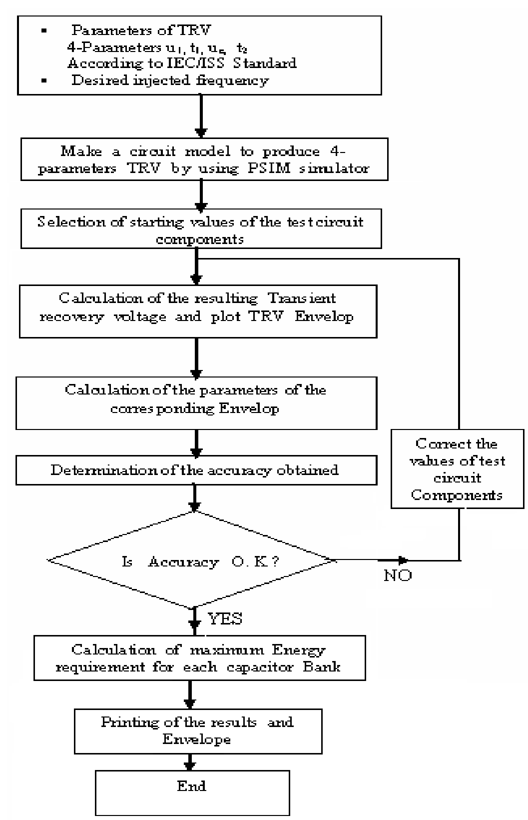

Fig.9. Algorithm for the design and simulation of synthetic testing circuits for High Voltage circuit Breakers using PSIM Simulator

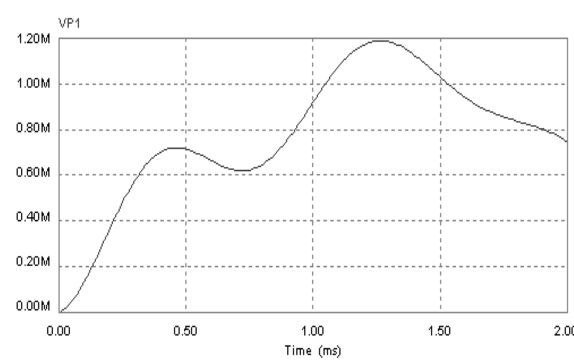

Fig.10. Terminal fault TRV for 800 kV circuit breaker as per case-I (TRV curve represented in Fig.2.)

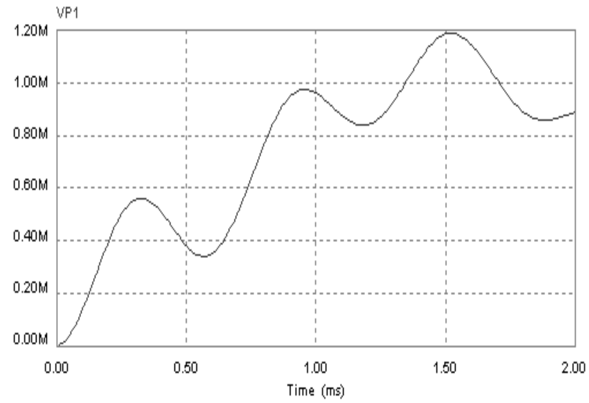

Fig. 11. Terminal fault TRV for 800 kV circuit breaker as per case-II (TRV curve represented in Fig.3.)

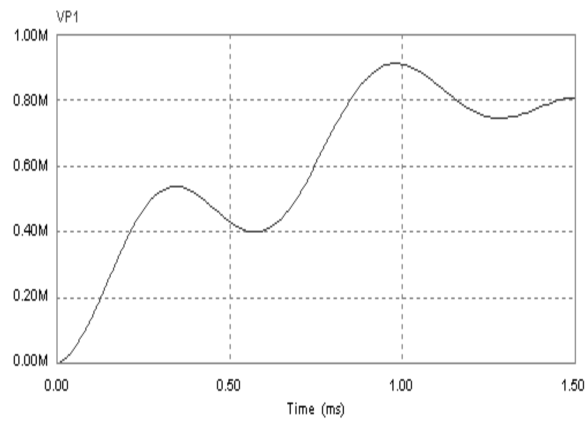

Fig.12. Short-line fault TRV for 800 kV circuit breaker as per case-I (TRV curve represented in Fig. 2)

VI. Results and Conclusion

IEC standards define the parameters of TRV, it is quite impossible to analytically link these parameters with the values of the components of the test circuit. So computer aided design and simulation of synthetic testing circuits is first necessary in order to determine the parameters of the TRV corresponding to a given test circuit.

The objective was to design and simulate 4-Parameters TRV synthetic testing circuit used for testing high voltage and Extra high voltage circuit breakers according to new TRV requirements given in IEC 62271-100 (2008). The circuit is designed and simulated for both Terminal as well as Short line faults test duty for 800kV rating circuit-breakers. Design optimization is also done to reduce the energy required by the capacitor banks and hence reduce the size and cost of capacitor banks also to save the space required.

The results obtained by using synthetic test circuit has been discussed and compared with the required results according to IEC standards. The results shown are almost the same according to IEC standards.

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