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A time efficient method for determination of static non-linearities of high-speed high-resolution ADCs

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Abstract

Static non-linearity tests on ADCs take many hours to complete, especially when they are of high-resolution, say, 10-bits or more. Efforts to reduce this test time have been attempted, but suggested methods are either not suitable for high-speed high-resolution ADCs or deviate from procedures given in relevant standards, viz. IEC 61083-1, IEEE 1057 or IEEE 1241. In this paper, a novel method is proposed to test such ADCs. It is simple, easy to implement, requires less time and does not impose any change to relevant standards. Instead of the conventional method of applying one DC waveform at a time to the ADC, the proposed method involves application of several DC waveforms (say, 32 or 64) at once, configured as a staircase waveform. Many staircases are used to cover the input voltage range. Thus, in a single acquisition, information corresponding to several DC waveform applications is generated. Hence, a reduction in test time is achieved. Generation of these staircases is straightforward using an arbitrary waveform generator. The timesavings achieved from this method depend on available memory and waveform uploading speed of the arbitrary waveform generator.
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Keywords: High-speed high-resolution ADC; Testing; Static-integral and differential non-linearity; Staircase; AWG

1. Introduction

Recent advances in very large-scale integrated chip technology has led to design and manufacture of superior, high-resolution and high-speed analog-to-digital converters (ADCs). Such ADCs are used in a wide variety of applications e.g. imaging, video, communication, instrumentation, etc. One specific application concerns measurement of high voltage impulse waveforms while testing power apparatus, during calibration of impulse voltage measuring systems and in intercomparison of impulse reference measuring systems. Signals to be

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acquired in all these activities are non-repetitive events and contain higher frequencies. Additionally, presence of noise, interference and low signal-to-noise ratio makes accurate and sensitive measurements all the more difficult [1,2]. In such scenarios, where accuracies to be achieved are very high (and have to progressively be improved), it is imperative that only the highest calibre ADCs become the natural choice for use in impulse measurements [2].

As per modern metrology practice, it is mandatory that each component in a measuring system be periodically subjected to a functional check and also be calibrated, so that, traceability of measured quantities and contributions to uncertainty from individual components, can be well established. In an impulse measuring system, apart from other components, the digitizer (i.e. in other words ADC) forms the most crucial part. In spite of great advances in technology employed during its manufacture, actual ADC characteristics are far from ideal. There exist several types of deviations from ideal characteristics e.g. static and dynamic non-linearities, offset and gain errors, aperture uncertainty, and so on [3,4]. Procedures to determine ADC characteristics exist, and depending on the application, some or all of these could acquire greater significance. In wide-band measurements (as in impulse tests) dynamic and static characteristics of an ADC are crucial benchmarks to assess its quality and suitability [5].

Apart from gain and offset errors, static test allows estimation of integral (INL) and differential (DNL) non-linearities. Both these are regarded very significant, as they indicate presence of bit-level anomalies and code transition levels, which in-turn, dictates accuracy of the measured impulses, viz. peak voltages, impulse scale factors, time parameters etc. [2,4,5]. Static non-linearity test performed as per the conventional method (outlined in [6] and [7]), takes a long time to complete, especially, for higher resolution ADCs. Even under complete computer control, literature reveals that, this test procedure takes anywhere between 6 and 9 h for a 12-bit ADC. Therefore, it is certainly worthwhile to explore and develop methods to reduce this test time.

2. Literature review

Efforts to reduce static test time have been attempted. Effectively, they attempt to reduce either the number of transition levels or applied voltage changes. Proposals like the feedback loop technique [8,9] and the more recent ones [10–14] have yielded varying degrees of success. Feedback loop method [8,9] is reported to be suitable for only high resolution and low sampling rate ADCs and also requires a dedicated hardware for this purpose.

The method of variable step-size estimated with extrapolated convergence factor algorithm [10,11] focuses on reducing the number of voltage levels to be applied. It is an iterative method (based on the idea of calculating the increment to apply in the next iteration, using the previous two data records) and yields reduction in test time by a factor of 2–4, depending on resolution of ADC, required confidence level and noise in experimental set up. This method is suitable for high resolution ADCs, in which, standard deviation of noise is at least some LSB. Performance of the method (i.e. algorithm) is reported to deteriorate drastically in the absence of noise [11].

A very efficient method, namely, a histogram-based approach employing small-amplitude triangular waves superimposed on gradually increasing DC has been proposed by Alegria et al. [12,13]. The method uniformly stimulates several ADC codes per step over the entire range, and requires less number of sample acquisitions, consequently offering a great reduction in test time. Requirements concerning distortion, slope and frequency of triangular waveform were overcome by use of a DC calibrator and a function generator. It is reported that, very significant reduction in test time can be achieved, viz. it takes only 5 min for a 12-bit ADC. This is indeed remarkable. However, this procedure would impose a need for a change in the existing standards [6,7], as it is quasi-static and histogram-based. This aspect is, perhaps, its only limitation.

In [14], a model-based technique was reported, to extract both static and dynamic non-linearities from a single data record of a sampled high frequency sine wave. This technique derives from the dynamic INL measurement, an approximation

of the static INL, at all codes. The method does not require overdriving of the signal. It is shown to be suitable for production line testing of a particular type of ADC. However, savings in static test time achievable are not mentioned.

Therefore, it emerges that the methods discussed so far, suffer from some of the following issues:

1. Proposed alternatives [10,11] are not strictly as per procedure and method described in IEC standard [6].
2. Not applicable for high-speed, high-resolution ADCs [8,9].
3. Involve implementation of iterative algorithms and convergence may not be guaranteed always and under all conditions [10,11].
4. Additional equipment or dedicated hardware required [11].

Hence, it is desirable to develop fast, time efficient, simple-to-implement procedures that are as per existing standards, for estimating static characteristics of high-speed, high-resolution ADCs.

3. Conventional static test

The test procedure for determining static nonlinearity as per [6], will be referred to as the conventional method. The method stipulates application of at least five levels of DC voltage corresponding to each discrete level of vertical resolution. An n-bit ADC has 2^n discrete levels. So, a DC voltage of $(1/5) * N * 2^{-n} *$ FSV is applied to the waveform recorder low voltage input, where, N is varied from 1 to $5 * 2^n$, and FSV is full-scale voltage. Each applied DC waveform has to be acquired and mean of at least 100 samples calculated and the quantization (or transfer) characteristic is obtained. Static non-linearities are determined from this characteristic. For a 10-bit ADC, this test amounts to sequentially generating 5120 DC levels, followed by data acquisition. This signal generation-acquisition cycle is the time consuming part, even in spite of its complete automation. The test procedure as per [7] is slightly different, and more or less takes same time.

4. Principle of proposed method

The proposed method is similar to the conventional method in all respects, except that, instead of sequentially applying a single DC waveform, several DC waveforms configured as a staircase is applied to the ADC, at once. Thus, it enables generation of data corresponding to these multiple DC waveforms, in a single operation. A required number of staircases (each with an appropriate offset voltage) are generated to span the entire vertical range (for a selected input voltage). Fig. 1 illustrates the underlying principle. For e.g. if the number of steps per staircase is 64, then the number of staircases required for a 10-bit ADC is equal to 80 (i.e. *5120/64*). Compared to the several individual DC waveform generation-acquisition cycles, the time required for generation of a staircase and its subsequent acquisition is far less. This is the main difference between the two methods and is solely responsible for the timesaving that accrues. With little modifications, the proposed method can be harmonized with requirements in [7] as well.

Staircase waveforms with desired specifications (viz. step length, step height, number of steps, offset voltage, etc.) are easily generated using programmable function generators in the 'arbitrary waveform generation' mode. For this, initially, the numerical values corresponding to the waveform to be generated (in this case, a staircase) are computed, and then uploaded into the memory buffer of the function generator, using pertinent

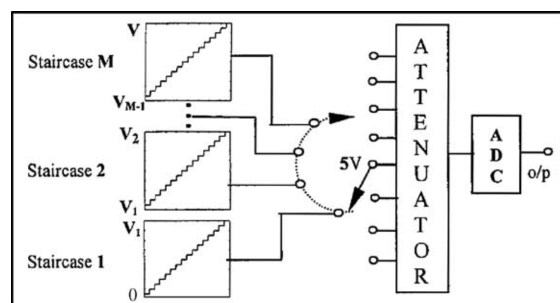

Fig. 1. Principle of proposed method. A single AWG generates many staircases with required offset to span the entire vertical resolution for a selected input voltage.

commands. Time for uploading is the least, when 'binary' option is employed, e.g. it takes a few tens of seconds (quoted value is equipment specific) using 'binary-block' format. Subsequently, the analog waveform is outputted. Care is exercised to ensure that, during each upload operation, the maximum resolution of function generator (DAC) is being used. As is evident from Fig. 1, the starting of the next staircase should exactly match with the last step of the previous staircase, so that each step of the staircase exactly corresponds to the individual DC waveforms applied in the conventional method. This requirement is easy to achieve.

One important matter that needs to be clarified at this juncture is, whether the proposed test could qualify, as a static test, since the applied stimulus, strictly speaking, is not a true DC excitation. The answer to this is, fortunately, yes. As the staircase waveform consists of steps, and each of these steps is chosen to exist for a sufficiently long interval of time (1–2 ms), the characteristics of the applied stimulus can certainly be considered to excite the 'static' features. Also, since periodicity of the staircase is chosen to be very low (of the order of a few Hertz) the test conditions closely conform to that existing under a DC excitation in the conventional method. Also, acquisition of this staircase data by the ADC under test is done at a relatively slow speed (sampling time = 1–2 μs or more). So, influences, if any, related to settling of ADC response due to step change in input would not be imposed on the acquired data. Normally, such step response settling times would be of the order of a few tens of nanoseconds, and so is not expected to interfere. Hence, test conditions being impressed in proposed method can be considered to be 'static' in character.

A sample staircase generated using a function generator Agilent 33250A (recorded using an 8-bit DSO) and consisting of 64 steps is shown in Fig. 2. Another example is included (Fig. 3), in which a 10 steps-per-staircase is generated. The first two consecutive staircases are shown together, using 'snapshot' feature of the DSO. This is done to explicitly depict the DC offset of the second staircase with respect to the first one. The staircase shown in Fig. 2 is required to test a 10-bit ADC

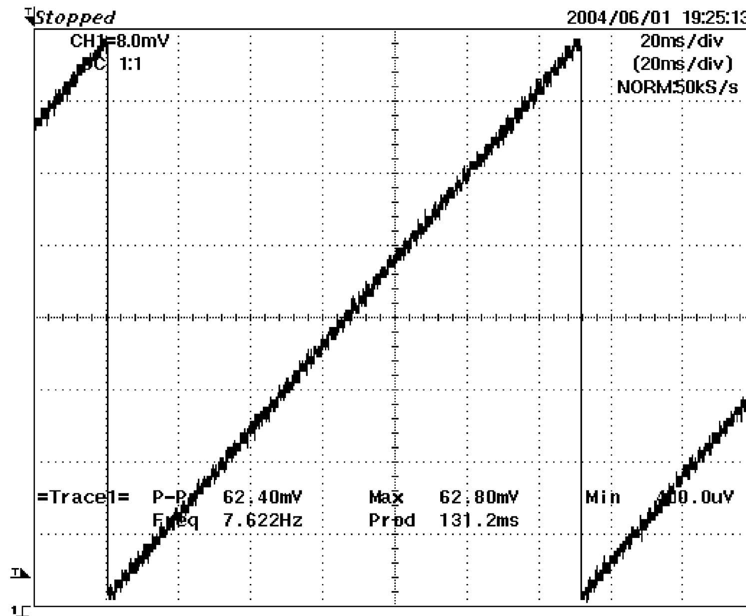

Fig. 2. Output of function generator (Agilent 33250A) showing one cycle of a 64 steps staircase (vertically zoomed), step-width = 1024 points, step-height = 0.97 mV, sampling time = 2 μs, frequency = 7.629394 Hz.

Fig. 3. Output of function generator (Agilent 33250A) showing one cycle each of two successive staircases (vertically zoomed) with 10 steps per staircase. Step-width = 1000 points, step-height = 3.906 mV, sampling time = 10 μs, frequency = 10 Hz. (*Note*: noise level in each step is ±1 mVpp).

(256 K memory), while the other in Fig. 3 is customized to test an 8-bit ADC (with 10032 points memory). In both cases, the 5 V input range is considered.

5. Choice of parameters and related issues

Selection of the staircase parameters are closely related to the specifications of DUT and function generator viz. its memory, noise level, resolution etc. While making this choice, certain issues arise and are discussed below:

- Choice of number of steps and its width directly depends on size of memory available in function generator and digitizer, whichever, is lesser. Initially, the width of each step must be chosen to be sufficiently large so that it produces the effect of a DC excitation. Considering each step to consist of 1 K sample points and a sampling time of 1–2 μs (or more) makes the step 1–2 ms wide. Next, the number of steps per staircase can be determined, for a given memory length. Lastly, the frequency of the staircase is determined as the reciprocal of the product of number of steps per staircase and duration of each step. With the staircase parameters chosen as explained, it emerges that, even with a reasonably small memory of 64 K (in function generator), the frequency of staircase would be of the order of a few tens of Hertz, and thus 'staticness' criterion is closely satisfied.
- Issues concerning noise-level or accuracy of function generator, required voltage resolution for selected range and the number of steps per staircase to be chosen, could become critical in certain situations. For example, if noise level in signal source is comparable to the minimum voltage resolution required for a selected voltage range, then there is a likelihood of overlap of data in neighbouring steps. Or, in other words, data from two neighbouring steps will become indistinguishable. An example of this situation is illustrated in Fig. 4. Here, a 64 steps staircase (with 1 K points per step, step

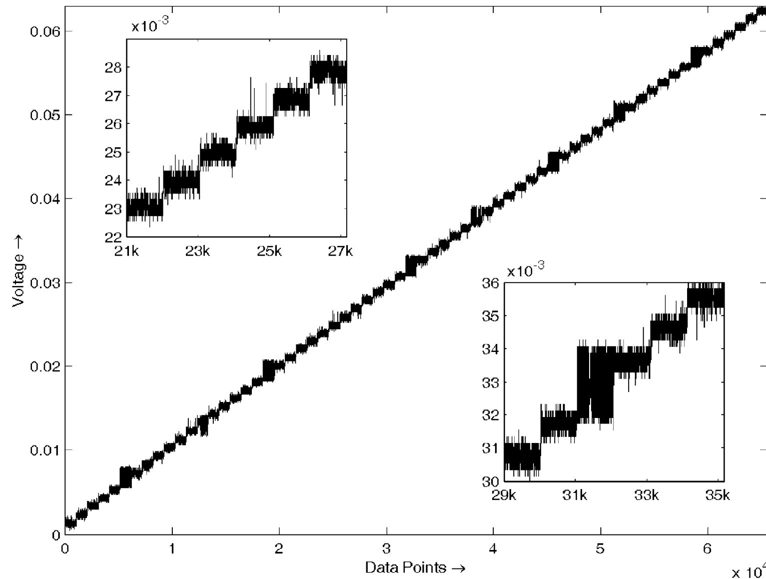

Fig. 4. A 10-bit ADC (RTD 710A) output showing problems associated due to the required voltage resolution being equal to noise level of function generator.

height = 5 V/5120 i.e. = 0.97 mV) was applied to a 10-bit ADC (RTD 710A). Data was acquired using a 100 mV input range and the ADC output is shown in Fig. 4. The average step-height and the noise level are seen to be equal. Fig. 4 clearly illustrates that, data from neighbouring steps are overlapping at many places; the upper subplot shows regions of an acceptable situation, while the bottom subplot shows an overlap. Had the noise level been lower, then, all the 64 steps would have been well resolved. One means of avoiding this situation is to replace the source with a low noise source. Alternatively, selecting the immediate next higher voltage range on the digitizer, so that, required voltage resolution becomes higher (and more or less noise level is same) is another practical and simpler solution. Of course, this is subject to availability of required voltage rating in the function generator.

- The average value corresponding to each step is computed as the mean of 400 data samples drawn from the centre of the step. Drawing samples belonging to the centre of the step is done to disregard any settling effects the ADC response might have, due to a step change in input. As a further verification, the ADC step response was measured using a 3 ns rise-time step generator and the ADC output was acquired with its highest sampling interval (10 ns). The step response was found to settle well within 60–70 ns. So, measurements as per proposed method are not influenced from this artefact.
- Existence of a small difference between the nominal voltage range of a channel and the actually available voltage range is inherent in digitizers and digital oscilloscopes. So, during static test experiments, it becomes necessary to compensate for this small difference by increasing the input to that extent, so as to actually span the selected voltage range. This was done in all the measurements reported.
- Lastly, it is well accepted that, the function generator i.e. signal source selected should have a resolution of, at least, four times the ADC (device) under test. Also, it must have a very low noise level, low drift, high thermal stability etc.

Details of test set up and results are presented in next sections.

6. Test set up

The proposed technique was implemented on two ADC systems, whose details are given below:

- A 10-bit, 200 MSa/s, 256 K memory, 2 channels, digitizer (RTD 710A, Sony Tektronix Inc.).
- An 8-bit, 200 MSa/s, 10032 points memory, 4 channels, digital oscilloscope (DL 1540, Yokogawa).

A function generator, Agilent 33250A, having a resolution of 12-bit, and maximum memory of 64 K (selectable in fixed steps) was used as signal source. All programs were coded using VEE Pro 6.01, a graphical programming language specially suited for use in computer control of instruments, automated testing and data acquisition, etc.

Table 1 lists the measured times required to upload data (in binary format) into function generator memory (via GPIB) and subsequently output the analog waveform, for different lengths of waveform data. These times are very close to that given in specifications.

As can be seen, time required for transferring larger data lengths is lower. This aspect can be exploited to have as many steps per staircase as practical (subject to other constraints), so as to achieve overall reduction in test time.

A few other matters encountered during experiments must be mentioned, and they are as follows:

- Usually, the static characteristic test is done for only one voltage setting (range) and it is considered as representative of the input channel. However, as already mentioned, the voltage range chosen must preferably be the highest voltage range that can be generated by the available programmable voltage source. This choice provides a larger separation among consecutive steps.
- Internal triggering can be difficult when input signal amplitude is very low (e.g. first few DC waveform applications in conventional method). So, external trigger with sync-pulse option of function generator can used to synchronize the operation.
- In the previously proposed methods, problems like linearity requirements, frequency stability, spectral purity etc. of triangular and sinusoidal waveforms existed. In the proposed method, these matters translate into requirements like low noise, low drift, good thermal stability etc. for the source.
- Care was taken to allow the function generator (DAC) output to 'settle down'. This is done by introducing an intentional delay of 100 ms, between the instant of outputting the analog waveform and acquiring the same with the ADC under test. As per Agilent 33250A manual, the output settling time is less than 50 ns.
- Warm up time of the equipment used has also a bearing on the final results. Therefore, identical warm up times (of 10 min) were employed for both methods.

Table 1
Uploading time measured for different steps per staircase

Function generator	Steps per staircase	Samples per step (K)	Memory (K)	Upload time (binary format) (s)
Agilent	16	1	16	8
33250A	64	1	64	26

(Accuracy: ± 1% of setting ± 1 mVpp see Fig. 3).

7. Experimental results

The static (transfer) characteristics of both the ADC systems (described in previous section) were determined following the conventional and proposed method, for a 5 V input range. Average of 1000 data points (out of a 4 K record) were considered in the conventional method. All other aspects were maintained identical during the experiments. Figs. 5 and 6 show the transfer characteristics for RTD 710A and DL1540 respectively, employing either of the methods. In both these figures, it is clearly seen that, the transfer characteristics estimated by the conventional and proposed method are almost indistinguishable. The zoomed subplots

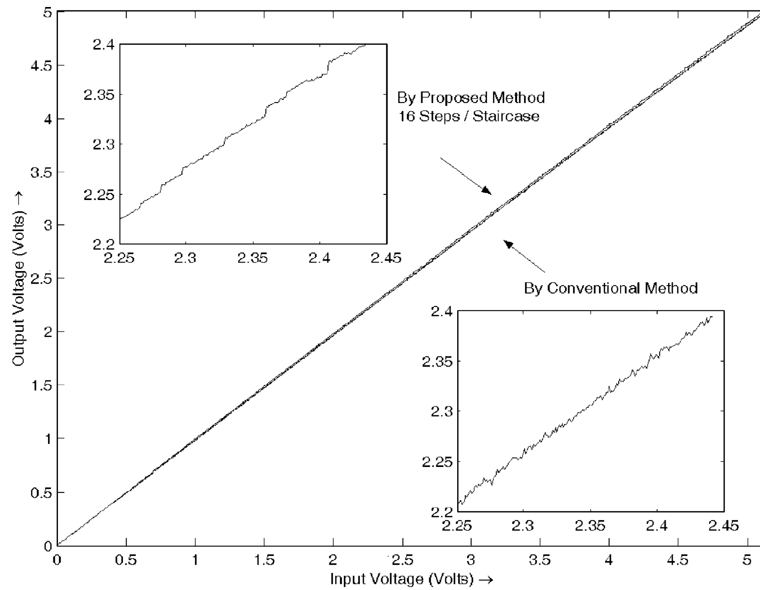

Fig. 5. Comparison of static transfer characteristic of RTD 710A by conventional and proposed method (for 5 V input range).

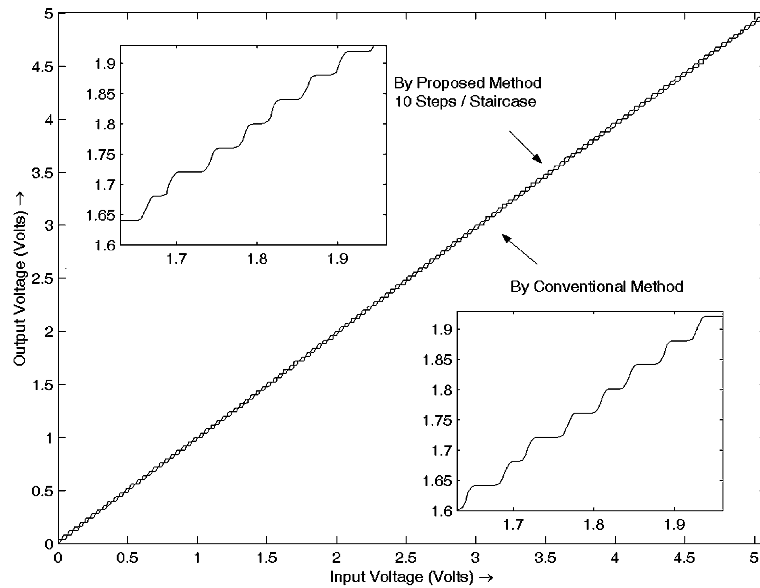

Fig. 6. Comparison of static transfer characteristic of DL 1540 by conventional and proposed method (for 5 V input range).

provide finer details of the transfer characteristics. A close match between these two subplots is observed, while the minor differences can, perhaps, be attributed to the noise characteristics of the function generator. Further, the extent of match between subplots is excellent in Fig. 6 for DL 1540, than it is for RTD 710A, in Fig. 5. This is because, resolution of the function generator (12-

bits) is sixteen times better than DL 1540 (8-bits), while it only four times better than RTD 710A (10-bits). In both these figures, a small amount of over-drive given to the input is clearly seen. Lastly, these experiments were repeated several times following the proposed method, and repeatable results were obtained.

Next, the static INL and DNL for RTD 710A, estimated by the conventional and proposed methods are shown in Fig. 7. The agreement of the INL and DNL as obtained from the two methods is clear. Additionally, the shape of INL and DNL reported in [15] for RTD 710 is in close agreement with the results presented here. The INL and DNL results for DL 1540 are presented in Fig. 8. Finally, one more example is included in Fig. 9 depicting INL and DNL for RTD 710A, determined by the proposed method, using 16 and 64 steps per staircase respectively.

The time reduction achieved by the proposed method compared to the conventional method is quite substantial. For the 10-bit RTD 710A, the conventional method required about 181 min while the proposed method employing 64 steps per staircase needed only 40 min, a timesaving of as much as 77%. In case of DL 1540, only 10 steps per staircase could be applied, as its memory was only 10032 points. The corresponding static test times clocked by the conventional and proposed method were 39.5 min and 19 min respectively, resulting in a overall time reduction of about 50%. However, increasing the number of steps per staircase to 64 (by overruling the minimum step width requirement) resulted in a time reduction of close to 77%. Thus, demonstrating that the availability of a larger memory can be exploited by the proposed method to reduce test time. Table 2 summarises the time reductions achieved.

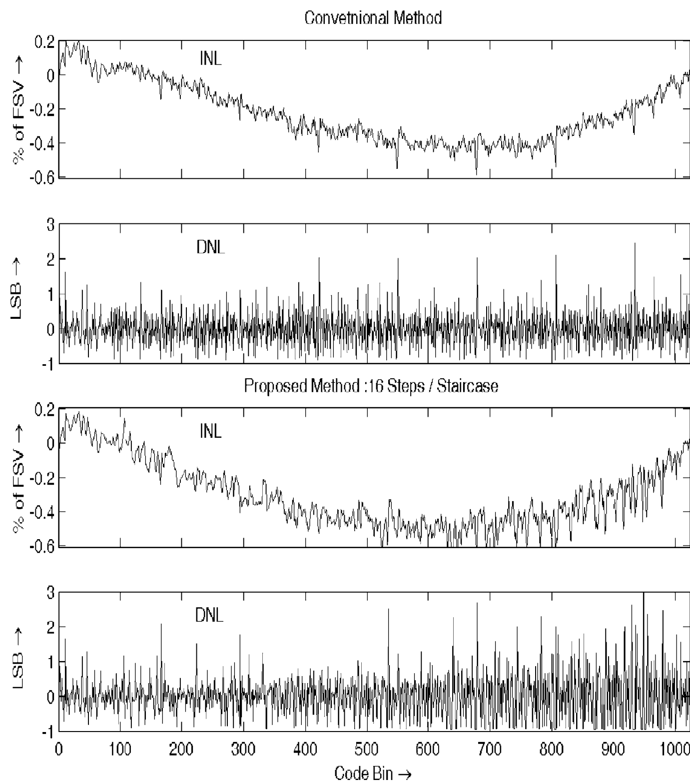

Fig. 7. Static non-linearity by conventional and proposed method (RTD 710A).

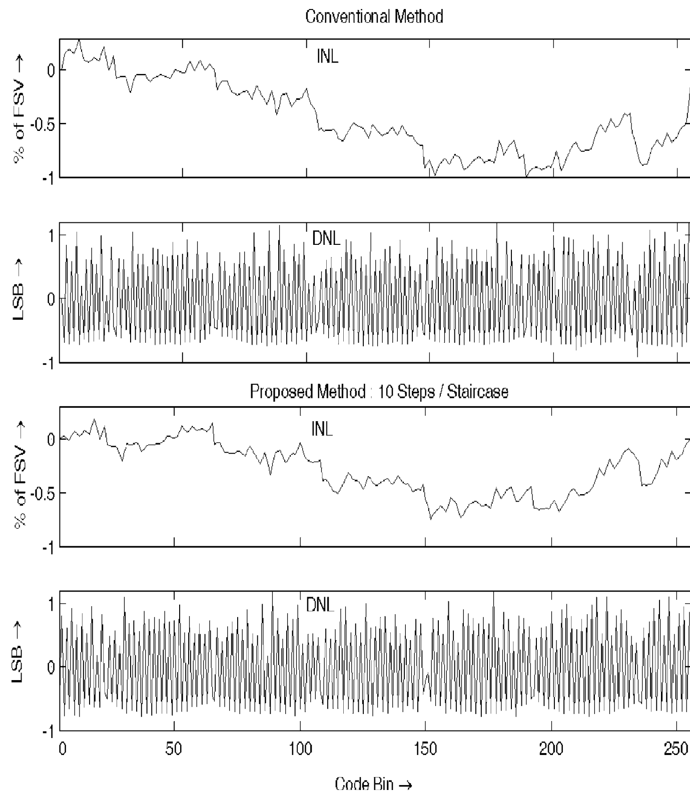

Fig. 8. Static non-linearity by conventional and proposed method (DL 1540).

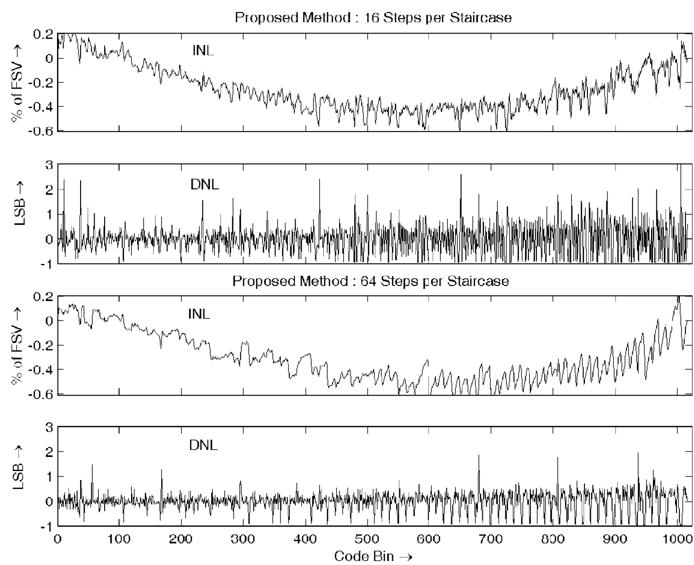

Fig. 9. Static non-linearity by proposed method with 16 and 64 steps per staircase (RTD 710A).

Table 2
Results for static-nonlinearity test (5 V input range)

Device under test	RTD 710A		DL1540
Voltage resolution	0.97 mV		3.906 mV
Steps per staircase	64	16	10
Data samples per step	1024	1024	1000
Record length (memory)	64 K	16 K	10,000
No. of staircases required[a]	81	324	131
Sampling interval, μs	2	2	10
Frequency of staircase, Hz	7.6294	30.5176	10
Time, proposed method	40 min	50 min	19 min
Time, conventional method	181 min		39.5 min

[a] Extra number of staircases to account for overdrive included.

8. Discussion

- The very close match of static non-linearity results obtained from the two methods goes to prove that, the test conditions impressed by the staircase on ADC in proposed approach, is similar to that, which exists in the conventional method. Thus, a validation of the proposed method is indirectly achieved.
- Recently, another function generator, Wavetek 301 (universal waveform generator) became available to the authors. It has a memory of 4 M and resolution of 12-bits. Implementation of the proposed method using this source is currently under progress. The equipment specification (strangely!) does not mention time required for the uploading operation. However, preliminary investigations reveal that, the time for uploading a 16 K data record (in binary format) is just 2.5 s, which is significantly less compared to the speed afforded by Agilent 33250A. This improved capability (viz. the upload time and memory length) being afforded by the newer function generator implies that, by using them, additional time reductions could be achieved following the proposed method. This is certainly an encouraging feature.
- Another possibility of reducing test time may be achieved by the use of two identical function generators. Here, while one AWG is uploading the staircase, the other is outputting the staircase. This way, further reduction in test time can be achieved. However, the limitation is that both AWG must possess exactly identical noise characteristics, offset and gain errors. Else, subsequent staircases will not match properly (due to different offsets).
- The department has procured a state-of-the-art High-resolution Impulse Analysis System HiAS 743 (with 2 standard channels, 2 reference channels, a resolution of 12-bits with a sampling of 120 MSa/s). For this system, the time required as per conventional method will be ~ 12 h (extrapolating as per times reported in Table 2). In fact, this huge test time requirement was the prime motivation for the proposed method. It will be implemented on HiAS 743 as and when function generators suitable for testing such reference-class, 12-bit system become available.
- Another interesting point is that, calibration-grade, extremely low noise, programmable DC sources are now commercially available and these also have a built-in staircase generation possibility. So, implementing the proposed method would be much easier.
- There are some requirements specific to only IEEE 1057 [7], like length of data record required for achieving '*Precision of Estimates*' (Clause 4.1.2.1.1). With little effort, the proposed method can suitably be modified to comply with them as well.
- Lastly, the proposed method, as envisaged, does not impose any change to the existing standards, viz. IEC 61083-1 or IEEE 1057, as far as static test is concerned. The method is equally applicable to ADCs of all resolutions and speeds. On these counts, the proposed method is considered to be a novel, efficient and original contribution.

9. Conclusions

A novel, easy to implement and time-efficient method (using staircase waveforms instead of DC) for determining the static characteristics of high-speed, high-resolution ADC has been successfully demonstrated. Implementation of

proposed method was done on a 10-bit and 8-bit ADC system, and a test time saving of almost 77% was achieved. Unlike earlier methods, this method is suitable for all types of ADCs, does not introduce a need to change standards, and the test times required are still manageable. With availability of function generators with larger memory, better noise characteristics and less uploading time, further time reductions can certainly be anticipated.

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