Impact of Scaling on Power Analysis in ASIC Design

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Abstract— **Power is considered to be the major limiter to the faster and more complex Application Specific Integrated Circuits (ASIC). Designing an ASIC in today's deep submicron geometries is harder than ever, and the problems continue to worsen with shrinking geometries. In order to address this challenge, a combination of process, circuit design and micro-architecture changes are required. Consequently, to focus the optimization efforts in the right direction, authors have analyzed the effectiveness of an energy reduction mechanism that employs voltage scaling. Effect of technology variation on power dissipation is also highlighted. Mentor Graphics tools are used for this analysis. Among the various abstraction levels, analysis is carried out at the transistor level which leads to reasonable accuracy.**

Keywords— **ASIC design, Design flow, LFSR, Power dissipation, Scaling**

I. INTRODUCTION

Power dissipation has become an important design consideration, which can be attributed to the fast growing battery-driven devices such as mobile, laptops, palmtops etc. and concerns about circuit reliability and packaging costs. Power is widely considered to be the major impediment for more powerful high performance ASIC.

For CMOS circuits, the major sources of power consumption are dynamic and leakage power, with the latter becoming more significant as threshold voltage scales with technology [1]. In order to devising new solutions to address the increasingly important power problem, it is essential for circuit designers and architects to have a mechanism to analyse future trends accurately and understand the relative importance of these components. Here we evaluate the anticipated effectiveness of supply voltage scaling and technology those are widely used for power minimization.

ASIC design teams face a growing problem. ASIC power consumption estimates that take place before the design phase lack both scope and credibility. These shortcomings affect process, design and Intellectual property (IP) selection. Alternatively, supply voltage can be scaled to achieve tolerable power dissipation. For that characterisation of power based on supply voltage variation should be available.

The modern ASIC design flow has evolved and increased in complexity just as the devices that are being designed have dramatically increased in complexity. This design flow is now heavily dependent on EDA tools and many of the tasks that were once carried out manually are now automated by EDA tools with little or no manual intervention.
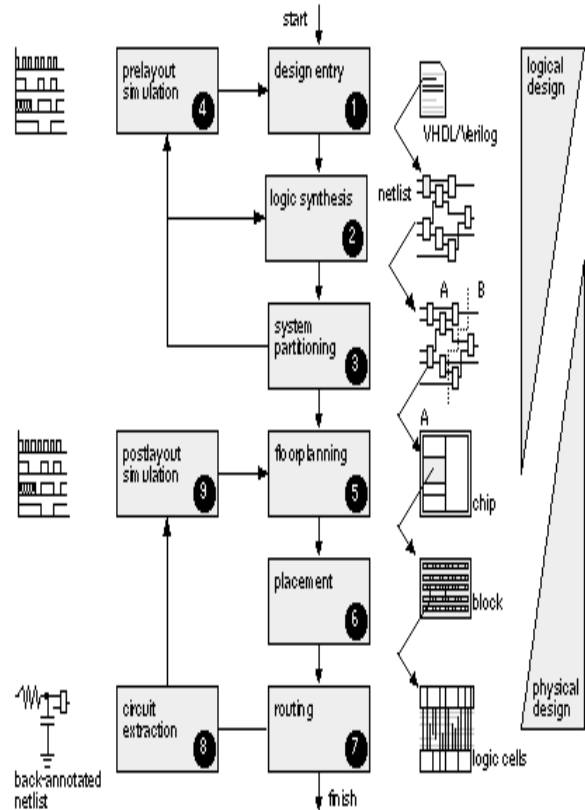

Fig. 1 ASIC design flow

1. Design entry: Enter the design into an ASIC design system, either using a hardware description language (HDL) or schematic entry.
2. Logic synthesis: Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a netlist —a description of the logic cells and their connections.
3. System partitioning: Divide a large system into ASIC-sized pieces.
4. Pre-layout simulation: Check to see if the design functions correctly.
5. Floor-planning: Arrange the blocks of the netlist on the chip.
6. Placement: Decide the locations of cells in a block.
7. Routing. Make the connections between cells and blocks.
8. Extraction: Determine the resistance and capacitance of interconnect.

II. DESIGN FLOW FOR POWER ANALYSIS

For power analysis, complete ASIC design flow is followed upto transistor level netlist as shown in Fig. 2 [6]. Necessary tools are used from Mentor Graphics. VHDL code is written in HDL Designer editor. It is synthesised with Leonardo Spectrum. After synthesis, gate level netlist file with the extension .v is generated. For the next step, Design Architect tool is used, where the gate level netlist file is imported and schematic can be captured. From this schematic, spice file – a transistor level netlist can be generated with .spi extension. Then necessary modifications are made in this file so that using this file, layout can be prepared in IC Station tool.
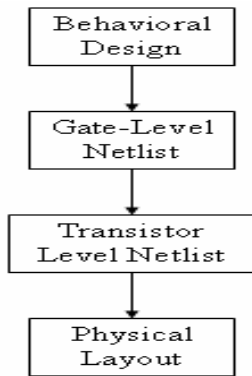

Fig.2 ASIC design flow for power analysis

III. POWER ANALYSIS FOR LFSR

A simple Linear Feedback Shift Register (LFSR) is selected to observe the impact of supply voltage variation on estimated power. The reason for LFSR is that it consists of combinational as well as sequential components.

A. Design description

The LFSR is a shift register which using, feedback, modifies itself on each rising edge of the clock. The feedback causes the value in the shift register to cycle through set unique values. The choice of length, gate type, LFSR type, and maximum length logic depends on application. Here for power analysis, simple 3-bit LFSR based on ex-or gate is designed.

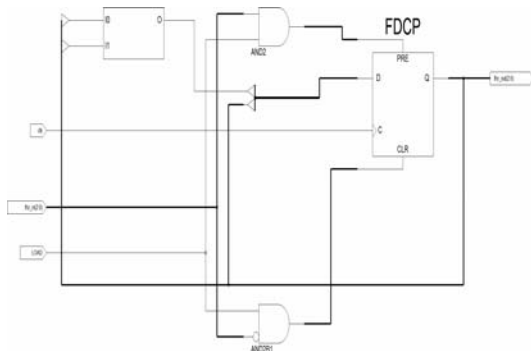VHDL code is written for simple LFSR. After the synthesis, generated RTL is shown in Fig. 3.

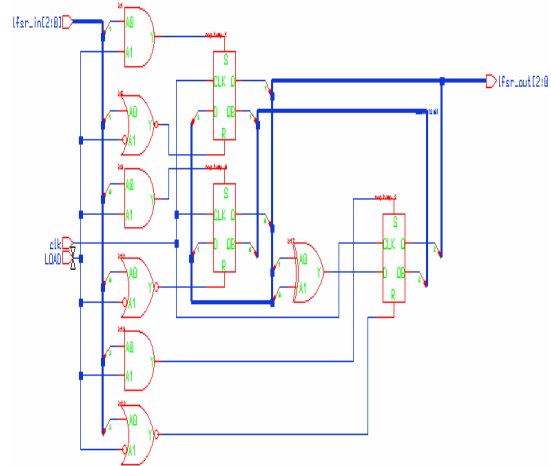Fig. 3 RTL of LFSR after synthesis

Fig.4 Schematic captured in Design Architect tool

B. Power analysis for different supply voltage

Reduction of the nominal supply voltage gives a significant reduction on power consumption at the expense of performance. As the drive current capability reduces, the operating frequency must be reduced. But this voltage scaling can be applied whenever the system requirements allow it.

Here generated gate level netlist or spice file is used to estimate the power. Supply voltage is varied from 1.5 V to 2.5 V in step of 0.2 V. Power dissipation for these supply voltages is shown in Fig. 5. It shows that the power reduction is almost linear with the change on supply voltage. The negative effect on performance dominates when the decrease in supply voltage is larger than about 20 % [1]. This observation shows that supply voltage reduction can help for power reduction up to certain limit.

There are some problems associated with supply voltage scaling. In memory structures, as cell capacitances decrease, the amount of charge they can store reduces and makes them more susceptible to soft errors.
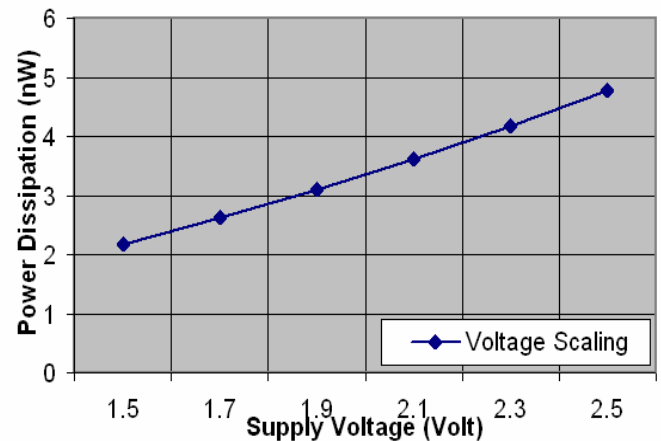

Fig. 5 Power dissipation supply voltage scaling

C. Power analysis for different technology

Similarly following same procedure, power is estimated for 0.35 μm and 0.18 μm technology. The variation in estimated power is shown in Fig. 6
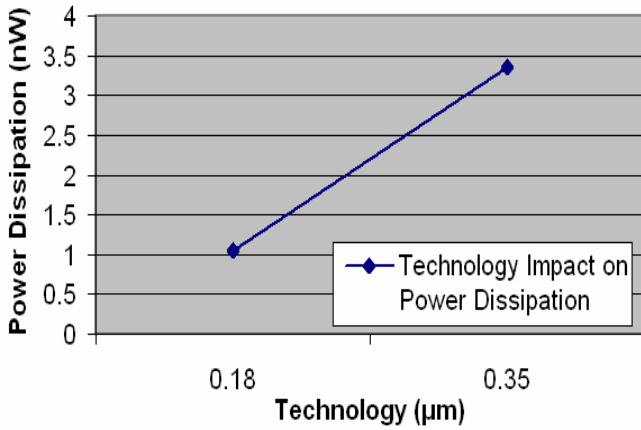
Fig. 6 Technology impact on power dissipation

IV. SIMULATION RESULTS

In this analysis flow, logical simulation is carried out after synthesis of VHDL code. The simulation result is shown in Fig 7. Another simulation is carried out after transistor level netlist i.e spice file using Eldo spice simulator. Again the simulation is for power dissipation based on the variations in supply voltage as well as for different technologies. After these simulation numerical values for power dissipation is obtained. These values are summarised in graphs as shown in Fig. 5 and Fig. 6.

V. CONCLUSION

In this paper LFSR is implemented, viewing it as a complete ASIC design. It is implemented in 0.35μm technology and variation in supply voltage shows the almost linear relation with power dissipation. Reduction in power dissipation can be obtained up to certain extent by decreasing the supply voltage within limit. Again same design flow is repeated for 0.35 μm and 0.18 μm technology, which the impact of scaling on power dissipation.

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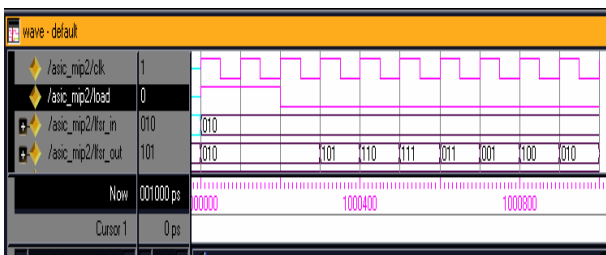
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Fig. 7 Logical simulation result of LFSR