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INVESTIGATIONS ON SPACE PHASOR BASED HYSTERESIS CURRENT CONTROLLERS AND COMMON-MODE VOLTAGE ELIMINATION SCHEME WITH DC-LINK CAPACITOR VOLTAGE BALANCING FOR MULTI-LEVEL INVERTER FED INDUCTION MOTOR DRIVES

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Abstract: This paper focuses on the various control schemes for multi-level voltage source inverter (VSI) fed induction motor (IM) drive systems. The hysteresis current controller presented for three-level inverter is aimed to achieve a current-control strategy with optimum switching for the multi-level inverter. Whereas, the hysteresis current controller proposed for a two-level inverter, focuses on the control of switching frequency variation. A five-level inverter topology offering simple power-bus structure and reduced diode count is also proposed in this paper. This paper also presents a common-mode voltage (CMV) elimination scheme for a dual five-level inverter fed open-end winding IM drive. This paper presents the studies on the capacitor voltage balancing for multi-level inverter fed IM drives, and reports the practical limitations to achieve the same. Open-loop and close-loop control schemes for the simultaneous achievement of capacitor voltage balancing and CMV elimination in a dual five-level inverter fed open-end winding IM drive are also proposed. All the proposed schemes are first simulated and then experimentally verified using digital signal processor controlled IM drives.

Keywords: Common-mode voltage elimination, Current error space phasor based hysteresis controller, dc-link capacitor voltage balancing, induction motor drive, multi-level inverter.

1 Introduction

Demand for control of electric power for electric motor drives is increasing day-by-day with the industrial growth around the globe. Inverter fed ac motor drive systems form an important class of power electronic circuits, popularly known as *adjustable speed drives* (ASD). *Induction motor* (IM) is the workhorse of the industry because of the simplicity of construction and ruggedness offered by it. The block schematic of a conventional *two-level voltage source inverter* (VSI) fed IM drive is shown in Fig. 1. The *pulse width modulation* (PWM) inverter reduces the amplitudes of lower order harmonics in the motor terminal voltage by shifting the dominating harmonics towards higher frequencies. Power schematic of a conventional two-level inverter is shown in Fig. 2, where A, B and C are the inverter poles. Each leg of Fig. 2 has two switches (such as S_1 and S_4 for pole-A), which are switched in a complementary fashion. Hence, with respect to point O (lower or negative dc-bus, Fig. 2), each of these inverter poles can attain any of the two distinct voltage levels ($+V_{dc}$ or 0), and therefore the inverter is called *two-level inverter* [1]-[7].

Switching PWM-VSI fed ASD at higher frequencies also causes significant amount of losses and generates conducted as well as radiated *electromagnetic interference* (EMI). The *dv/dt* effect caused by inverter can result in additional EMI and increased stress on the insulation of machine windings. This large *dv/dt* also appears in the alternating CMV generated by the inverters and can cause the motor shaft voltages, flow of motor bearing currents and consequently increased ground leakage currents. Hence, for high-voltage high-power industrial drives, conventional PWM-VSIs operating at high switching frequencies are seldom preferred.

Reduction in harmonic contents of the output voltage of PWM-VSI fed IM drives, especially for high-voltage high-power applications, is made possible by the use of m*ulti-level inverters*. Multi-level inverters are realized from a number of smaller discrete voltage sources, and they generate output voltage waveforms with more steps of smaller magnitudes.

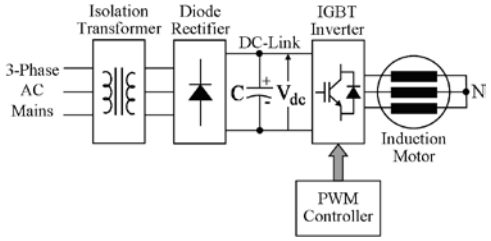

Fig. 1: Block schematic of a VSI fed conventional IM drive

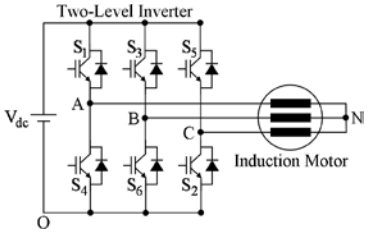

Fig. 2: Power schematic of a two-level VSI

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Significant advantages offered by the multi-level inverters compared to their two-level counterparts are [1]-[7]:

- Use of lower voltage ratings of power devices;
- Reduced *total harmonic distortion* (THD) in voltage;
- Reduced torque pulsations in the drive system;
- Reduced EMI problems by reducing switching *dv/dt*;
- Lower CMV and hence lower bearing currents;
- Less stress on insulation of machine phase windings;
- Lower switching frequency resulting reduced losses.

Thus, although designed initially to reduce the harmonic contents in the output voltage waveforms, the multi-level inverters have very quickly established themselves as a preferred and extensively used option for realizing high-voltage high-power drives for laminators, mills, conveyors, pumps, fans, blowers, compressors, etc. in industrial, marine, utility and traction applications.

2 Current error space phasor based self-adaptive hysteresis controller for three-level inverter

Current-controlled PWM (CC-PWM) inverters offer considerable advantages as compared to conventional voltage-controlled PWM (VC-PWM) VSIs and hence, are extensively employed in high performance drive (HPD) systems. Some of the drawbacks of conventional hysteresis controller, e.g., limit cycle oscillations, overshoot in current error, generation of sub harmonic components in the current and random (non-optimum) switching [1]-[2] are very well known. In the field of space phasor based hysteresis controllers, most of the research is concentrated on getting the optimum switching and fast dynamic response in association with inherent advantages of hysteresis current controller for two-level VSIs. Extension of these strategies to multi-level VSIs is not straight forward.

This paper presents a current error space phasor based hysteresis controller for any three-level VSI fed IM drives. In the present work, the proposed scheme is implemented on a three-level inverter formed using a dual two-level VSI fed open-end winding induction motor structure [1] as shown in Fig. 3. It does not need computation of machine back emf space phasor for sector identification and information on the same is indirectly derived from the directions and amplitude of current error space phasor. The direction of current error can be found from (1) where, $\mathbf{\Delta i}$ current error space phasor, $\mathbf{V_k}$ is the inverter voltage vector ($\mathbf{k}$ can be any number from **0** to **18**, Fig. 4), $\mathbf{V_m}$ is the machine voltage vector, and L_σ is the leakage inductance of motor. The controller always selects the adjacent inverter voltage vector (among the three vectors forming a triangular sector of Fig. 4, in which, tip of $\mathbf{V_m}$ lies), to keep $\mathbf{\Delta i}$ within the proposed hexagonal boundary. This ensures the optimum PWM vector selection with fast dynamic response of the controller. The scheme is self-adaptive for any possible amplitude and position of $\mathbf{V_m}$. The controller is capable of operating the inverter in two-level, three-level (Fig. 5(a)) and in over-modulation range leading to twelve-step mode of operation, with smooth transitions (Fig. 5(b)). Sector change detection and vector selection is done using simple look-up tables based on the output of hysteresis comparators [1]. The proposed controller can be extended for higher levels of multi-level inverter fed high performance drives by simply constructing suitable look-up tables.

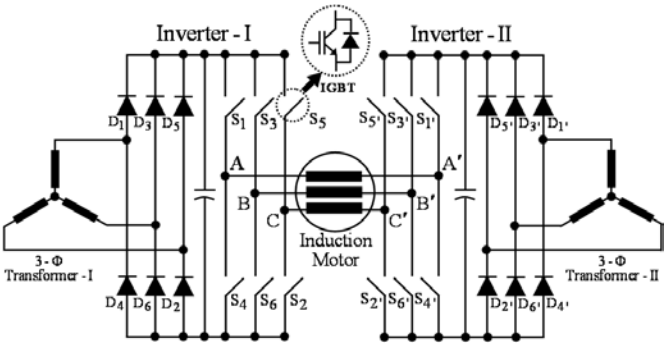


Fig. 3: Power schematic of dual two-level inverter fed three-phase open-end windings IM drive (three-level inverter)

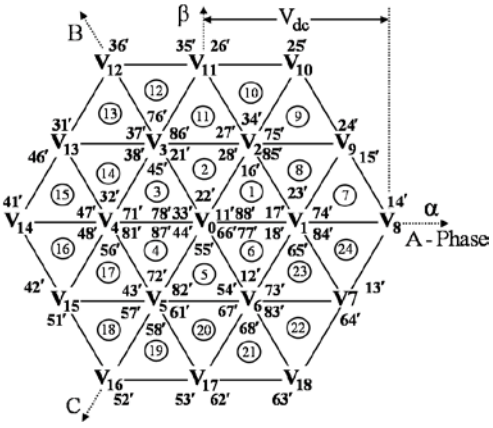
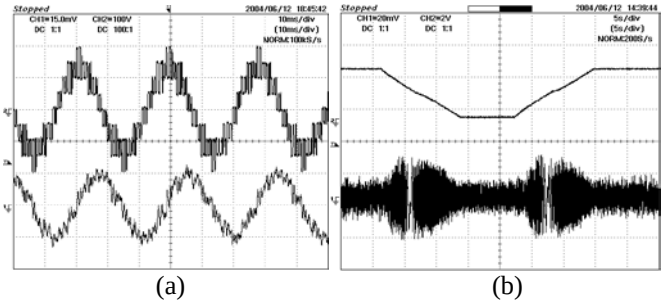


Fig. 4: Combined voltage space phasor structure generated by dual two-level inverter fed open-end winding IM drive

$$\frac{d\mathbf{\Delta i}}{dt} = \frac{\mathbf{V_k} - \mathbf{V_m}}{L_\sigma} \tag{1}$$



(a) (b)

Fig. 5: (a) Three-level operation: machine phase voltage ($v_{AA'}$) and phase current (i_A) [Y-axis; upper trace: 1 div. = 100 V, lower trace: 1 div. = 1.5 A, X-axis: 1 div. = 10 ms], and (b) Speed reversal transients: machine speed and phase current (i_A) [Y-axis; upper trace: 1div. = 1760 rpm, lower trace: 1div. = 2 A, X-axis: 1 div. = 5 s]

3 Control of switching frequency variation in current error space phasor based hysteresis controller

The common problems associated with the conventional, as well as current error space phasor based hysteresis controllers with fixed bands (boundaries), are the wide variation of switching frequency in a fundamental output cycle and variation of switching frequency with the variation in the speed of the load motor [1]-[2]. These problems cause increased switching losses in the inverter, non-optimum current ripple, and excess harmonics in the load current, which leads to additional heating in the motor. Different techniques are presented in literature to control the switching frequency in hysteresis current controller based inverter fed IM drives by employing various band control strategies. These techniques are either complex to implement, requires extensive knowledge of the system parameters, suffer from the stability problems, or have limitations in transient performance.

This paper describes current error space phasor based simple hysteresis controller for controlling the switching frequency variation in the two-level PWM inverter fed IM drives. A novel concept of on-line variation of parabolic boundary for the current error space phasor, depending on operating speed (as shown in Fig. 6), is suggested for the first time in this chapter for getting the switching frequency spectrum of the output voltage of hysteresis controller similar to that of the constant switching frequency VC-SVPWM based VSI fed IM drive. Based on (2) where Δt is the time in which the current error space phasor will increase by $\Delta(\mathbf{\Delta i})$, requirements of appropriate parabolic bands for current error space phasor for different speeds of the motor are mathematically analyzed, to maintain the desired inverter switching frequency range throughout the linear operating range of the drive. A generalized technique is also developed to determine the set of parabolic boundaries, as shown in Fig. 7, for controlling the switching frequency variation in the two-level inverter, for any given induction motor. This makes the proposed controller capable of providing desired switching frequency variation control independent of load machine parameters. The steady state (Fig. 8) and transient performance of proposed controller is experimentally verified in entire operating range up to the six-step mode of operation [2].

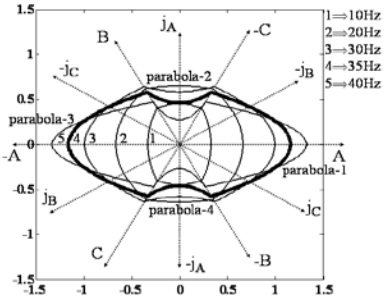


Fig. 6: Shape and size of the parabolic boundary of current error space phasor in Sector-2 for different operating frequencies [conventional Y-axis and X-axis: 1div.=0.5 A]

$$\Delta t = \left(\frac{L_\sigma \Delta(\mathbf{\Delta i})}{\mathbf{V_k} - \mathbf{V_m}} \right) \tag{2}$$

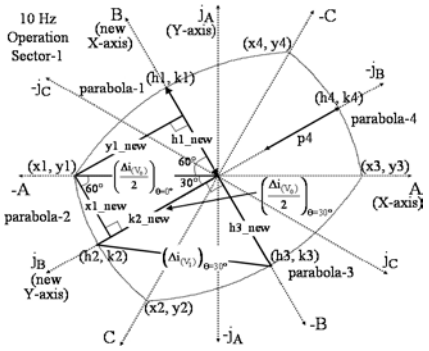


Fig. 7: Finding the parameters of boundary defining parabolas with respect to new reference axis (B and j_B) for Sector-1 (generalizes algorithm for this is developed)

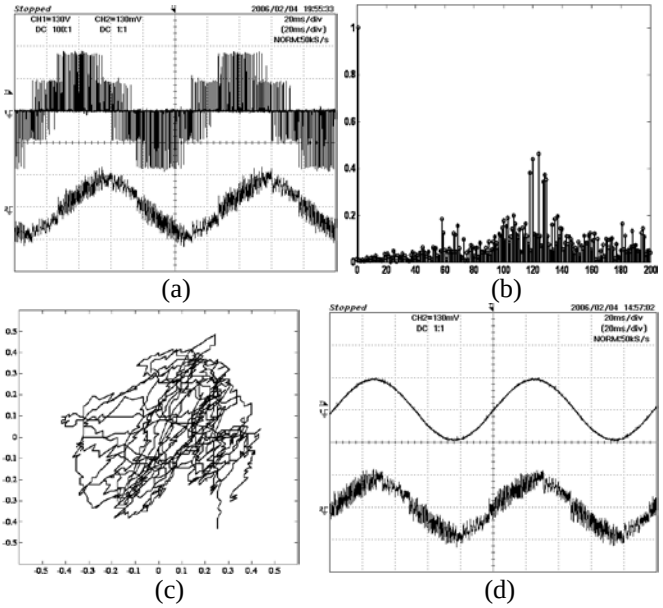


Fig. 8: 10 Hz operation: (a) machine phase voltage (v_{AN}), and current (i_A) [Y-axis; upper trace: 1div.=130V, lower trace: 1div.=1.3A, X-axis: 1div.=20 ms], (b) normalized harmonic spectrum (FFT) of v_{AN} [Y-axis: amplitude 1div.=0.2, X-axis: order of harmonic 1div.=20], (c) $\mathbf{\Delta i}$ in Sector-1 [Y-axis and X-axis: 1div.=0.1 A], and (d) upper trace: reference machine phase current (i_A^*), and lower trace: i_A [Y-axis; upper and lower traces: 1div.=1.3A, X-axis: 1div.=20 ms]

4 Simultaneous elimination of common-mode voltage and dc-link capacitor voltage imbalance in five-level inverter

4.1 Generation of alternating CMV in PWM IM Drives

PWM inverters generate alternating CMV in the IM drive system (at the inverter poles) [3]-[7]. These alternating CMV with high *dv/dt*, appear across the motor shaft to ground and

induce bearing currents, which lead to erosion of the bearing material and early mechanical failure (by pitting and fluting) of the bearings because of electric discharge machining (EDM) effect. Due to the parasitic capacitance between the motor windings and the frame, the inverter generated CMV also adds to the total leakage current through the ground conductor, which acts as a source of conducted EMI in the drive system causing malfunctioning of electronic equipment and false tripping of relays.

4.2 Proposed five-level inverter

A five-level inverter topology (as shown in Fig. 9) is proposed with switching state combination selection strategy for PWM control for an IM drive for complete elimination of CMV in the entire operating range of the drive, including over-modulation. Individual five-level inverter (Table 1) of the proposed scheme offers simple and modular power-bus structure with reduced power diode count as compared to that of a conventional five-level NPC inverter [3]. Proposed open-end winding IM drive needs nearly half the dc-link voltage and offers more number of redundant switching state combinations as compared to a single five-level inverter fed conventional IM drive. The multiplicity of inverter switching state combinations, with which the space vector combinations are generated in the proposed open-end winding IM drive, is exploited in an effective manner to eliminate the CMV. In the proposed scheme the switching state selection is done in such a way that there is no CMV at the inverter poles, (3) and (4), as well as in the phase windings of the machine, (5). With the absence of CMV in the drive, possibilities of all the associated problems such as, shaft voltages, possibility of electrostatic coupling, bearing currents, conducted EMI due to leakage currents etc., are also eliminated.

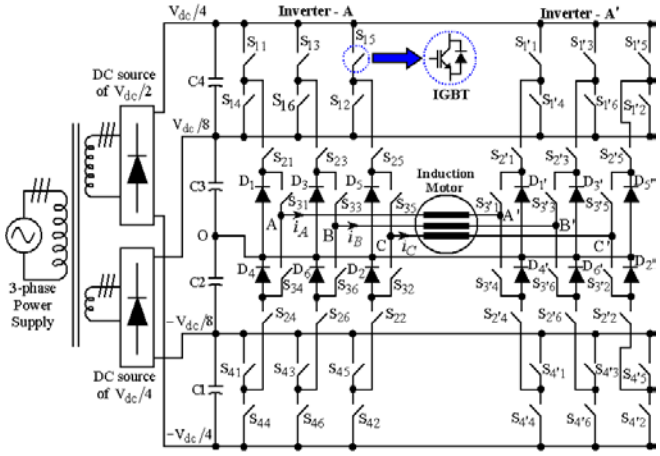


Fig. 9: Power schematic of proposed five-level inverter fed IM drive with CMV elimination and voltage balancing

$$v_{CMA} = \left(v_{AO} + v_{BO} + v_{CO}\right)/3 \quad (3)$$

$$v_{CMA'} = \left(v_{A'O'} + v_{B'O'} + v_{C'O'}\right)/3 \quad (4)$$

$$v_{CM} = v_{CMA} - v_{CMA'} \quad (5)$$

Table 1: Generation of five different voltage levels based on state of the switches for pole-A of Inverter-A (Fig. 9)*

Pole voltage v_{AO}	Voltage Level	State of the switch**			
		S_{11}	S_{21}	S_{24}	S_{41}
$V_{dc}/4$	2	1	1	0	1
$V_{dc}/8$	1	0	1	0	1
0	0	0	0	0	1
$-V_{dc}/8$	-1	0	0	1	1
$-V_{dc}/4$	-2	0	0	1	0

*[S_{11} and S_{14}, S_{21} and S_{34}, S_{24} and S_{31}, and $S_{41}$and S_{44} are four different complementary pairs of switches]

** ["1" indicates ON state and "0" indicates OFF state of the switch]

4.3 Imbalance in dc-link capacitor voltages

Because of the charging or discharging of dc-link capacitors when load current is drawn from the different nodes of the dc-link [4]-[7], the potential across the dc-capacitors varies from their balanced state. The dc-link capacitors will be charged to excessive high voltage and this high voltage may appear across the power switching devices of the multi-level inverter. This imbalance also causes the lower order harmonics appearing at the inverter output voltage which adversely affect the operation of induction motor by torque pulsation and excessive heating. Presence of larger number of dc-link capacitors and dc neutral points (dc-link nodes) makes the task of capacitor voltage balancing more complicated with increasing levels of multi-level NPC inverter. In most of the literature, the problems of CMV elimination and dc-link capacitor voltage balancing in multi-level inverters are dealt with as separate entities.

4.3.1 Open-loop scheme

Dependency of divergence of capacitor voltages on dc-link neutral currents (on the motor current and inverter switching states) is mathematically analyzed, as shown in (6), and conditions to keep the balance in all the capacitor voltages are established [4]. It is investigated that in five-level drive with a single dc power supply, even though the CMV elimination can be achieved throughout the operating range, including over modulation, it is not simultaneously possible to achieve the dc-link capacitor voltage balancing for higher speed range of operation, without any additional hardware [4]-[7]. The proposed open-loop scheme is inherently able to maintain the balancing in the dc-link capacitors in the entire modulation range in motoring as well as regenerating modes of operation.

$$\begin{aligned} \Delta v_{43} &= v_{C4} - v_{C3} = \frac{1}{C}\int i_3 dt \\ \Delta v_{32} &= v_{C3} - v_{C2} = \frac{1}{C}\int i_2 dt \\ \Delta v_{21} &= v_{C2} - v_{C1} = \frac{1}{C}\int i_1 dt \end{aligned} \quad (6)$$

4.3.2 Closed-loop scheme

A closed-loop control action is needed that stops not only the further unbalancing of capacitor voltages but also takes the corrective actions to bring back the capacitor voltages in the balanced state [5]-[7]. A simple closed-loop control scheme, based only on the switching state redundancy, as shown in Fig. 10, is also proposed. Effective utilization of redundant switching state combinations eliminates the need for extra hardware for achieving the capacitor voltage balancing, and at the same time the output fundamental voltage of the inverter is not affected. The proposed closed-loop control scheme simultaneously achieves the CMV elimination and the dc-link capacitor voltage balancing in the linear (Fig. 11) as well as in the over-modulation range (up to 24-step mode).

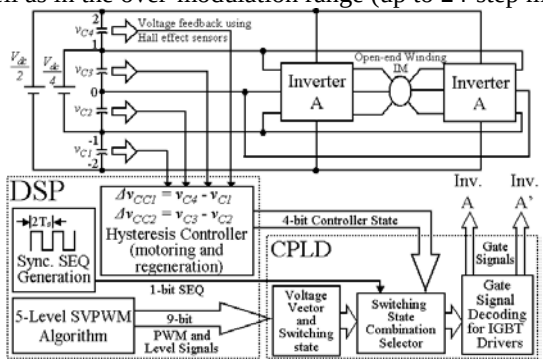


Fig. 10: Block schematic of hysteresis comparator based closed-loop control scheme for the proposed drive

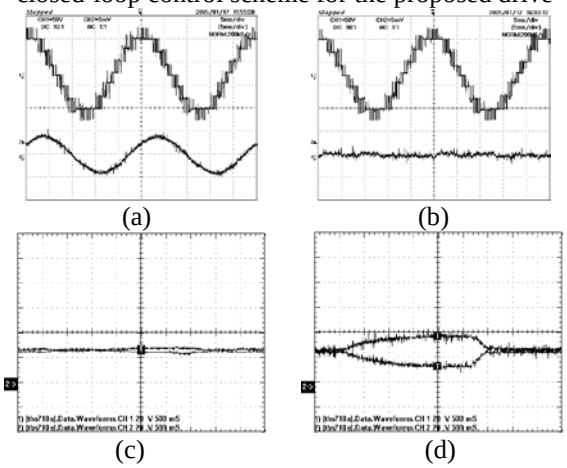


Fig. 11: Closed-loop control disabled and enabled again during five-level operation; (a) $v_{AA'}$ and i_A during balanced condition [Y-axis; upper trace: 1div. = 50 V, lower trace: 1div. = 2 A, X-axis: 1div. = 5 ms], (b) $v_{AA'}$ and common-mode current ($i_A+i_B+i_C$) during balanced condition [Y-axis; upper trace: 1div. = 50 V, lower trace: 1div. = 2 A, X-axis: 1div. = 5 ms], (c) capacitor voltages v_{C2}, and v_{C3}, and (d) v_{C1}, and v_{C4} [Y-axis: 1div. = 20 V, X-axis: 1div. = 500 ms],

5 Conclusion

The hysteresis current controllers, which need fast ADC's, have been implemented on the TMS320F2407A processor using vector control. The multi-level inverter modulation schemes for CMV elimination and dc-link capacitor voltage balancing have been implemented on the TMS320F240 processor using V/f control. Gate signals of the switches are decoded from a digital logic, which is implemented using flash-erasable reprogrammable CMOS logic device PALCE22V10 or programmable CPLD XC95108-20PC84C. Experimental results are presented, which show close agreement with simulation results. All the proposed schemes successfully eliminate the addressed problems. Though the proposed topologies and control schemes are for high-voltage and high-power industrial IM drives, due to laboratory constraints the experimental results are taken on the 1.5 kW/3.7 kW prototypes. But all the proposed schemes are general in nature and can be easily implemented for high-voltage high-power drives with appropriate device ratings.

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