DESIGN OF PLL AND CLOCK FREQUENCY GENERATION

Major Project Report

Submitted in partial fulfillment of the requirements

For the Degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Thakore Kruti Pranavkumar

(09MEC012)

Department of Electronics & Communication Engineering

Institute of Technology

Nirma University

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Under the Guidance of

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Declaration

This is to certify that

i) The thesis comprises my original work towards the Degree of Master of Technology in Electronics & Communication Engineering (VLSI Design) at Nirma University, Ahmedabad and has not been submitted elsewhere for a degree.

ii) Due acknowledgement has been made in the text to all other material used.

Thakore Kruti Pranavkumar

Certificate

This is to certify that the Major Project Report entitled "**Design of PLL and Clock Frequency Generation**" submitted by **Thakore Kruti Pranavkumar (09MEC012)**, towards the partial fulfillment of the requirements for the Degree of Master of Technology in Electronics & Communication Engineering (VLSI Design) of Nirma University, Ahmedabad is the record of work carried out by her under our supervision and guidance. In our opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree.

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Acknowledgement

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My affectionate thanks are due to my family who made me able to do such work.

<div align="right">

- Thakore Kruti Pranavkumar

09MEC012

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Abstract

In recent years, the increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs and routers, etc., is pushing the off-chip data rate into the gigabit-per-second range. In the past, high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for the IC package. For this reason, the off-chip data rate should move to the range of Gb/s-per-pin. The processors of today work with the operating frequency of GHz. The Phase Lock Loop acts as a clock generator which multiplies the lower frequency reference clock to match up to the operating frequency of the processor.

The objective of this project is to design phase lock loop for clock generation. A Phase Lock Loop designed for the application of clock generation has been realized using 0.35 μm CMOS technology. The application targets clock generation at speed of 1GHz with input frequency 250MHz. Total power dissipation of the PLL is 94.1mWatt at 3.3V power supply. The jitter is reduced to 5ps using high speed phase frequency detector design with dead zone compensation and charge pump with minimum mismatch in the up and down currents. The design simulation results agree fairly well with the expected results.

The pre layout simulation results are evaluated using Eldo Spice Tool and Layout is made using Mentor Graphics Back End Design Tools like IC Station and DA-IC (Design Architect).

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Nomenclature

A	Area, μm^2
A_V	Voltage Gain
β	Beta
μ	Micro
G	Giga
Hz	Hertz
W/L	Width to Length Ratio
p	pico
m	Mili
M	Mega
t_p	Propagation Delay
V	Volt
W	Watt

Acronyms

PLL	Phase Lock Loop
PFD	Phase Frequency Detector
CMOS	Complementary Semiconductor Metal Oxide
IC	Integrated Circuit
LP	Low Power
LV	Low Voltage
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Filed Effect Transistor
nMOS	n-Channel Metal Oxide Semiconductor
PD	Power Dissipation
pMOS	p-Channel Metal Oxide Semiconductor
SPICE	Simulation Program for Integrated Circuit Emphasis
TSMC	Taiwan Semiconductor Manufacturing Company
VLSI	Very Large Scale Integration

Chapter 1

Introduction

Phase-lock loops (PLL) have been one of the basic building blocks in modern Electronic systems. They have been widely used in communications, multimedia and many other applications. They are utilized as on-chip clock frequency generators to synthesize a low skewed and higher internal frequency clock from an external lower frequency signal.

This chapter provides a brief introduction to the concept of clock generation using Phase- Lock Loops (PLL). The initial sections provide an overview of the concept of phase locking. The various application of PLL like clock generation, clock recovery, and clock distribution has been discussed in subsequent section. The chapter in the later part provides an insight of the basic principle of clock generation and its requirement in communication system.

Common applications of PLL are listed as below:

1.1 Concept of clock generation using PLL

Many electronic systems include processors that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock up to the operating frequency of the processor.

1.2 Clock recovery

Some data streams, especially high-speed serial data streams are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery.
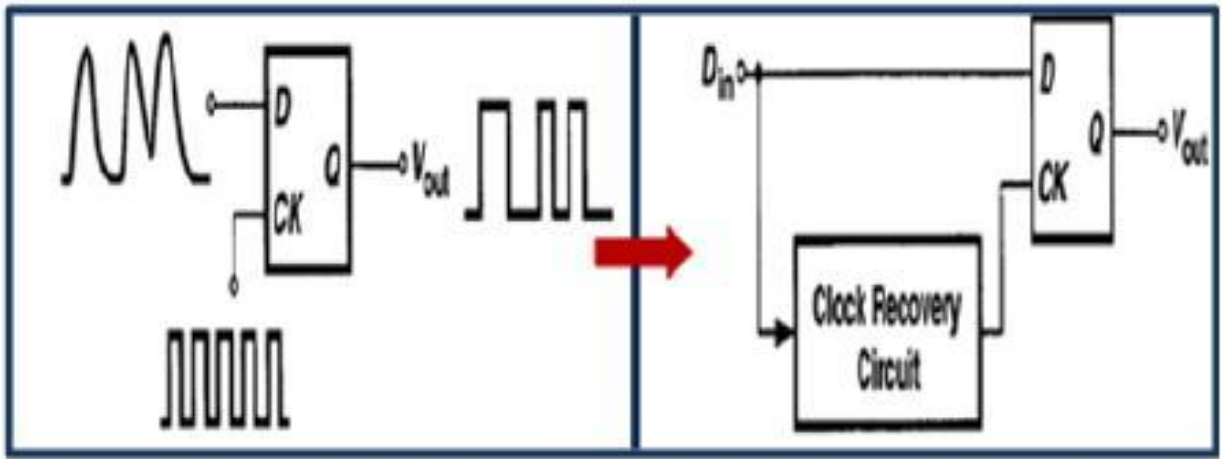
Figure 1.1: Basic clock recovery circuit

1.3 Clock distribution

The reference clock enters the chip and drives a phase locked loop (PLL), which then drives the system's clock distribution. The clock distribution is usually balanced so that the clock arrives at every endpoint simultaneously. One of those endpoints is the PLL's feedback input. The function of the PLL is to compare the distributed clock to the incoming reference clock, and vary the phase and frequency of its output until the reference and feedback clocks are phase and frequency matched. The clock distribution arrangement is as shown in figure 1.2.
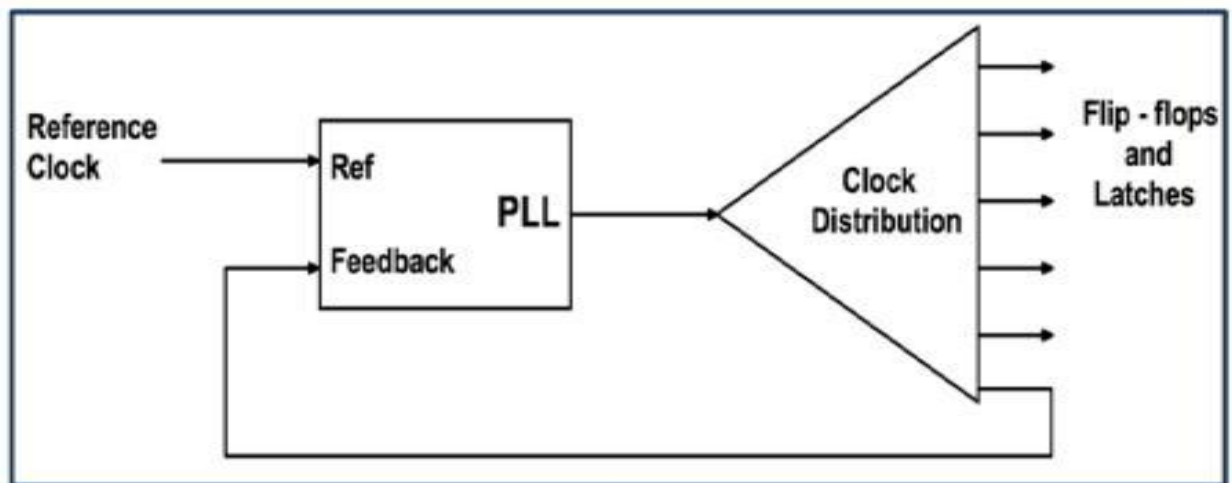
Figure 1.2: Clock distribution arrangement

1.4 Jitter reduction

Jitter, which is the variation of the clock period from one cycle to another cycle compared to the average clock period. The clock jitter directly affects the maximum running frequency of the circuit because it reduces the usable cycle time. When the clock period is small, the digital circuits in the critical path may not have enough usable time to process the data in one period, resulting in the failure of the circuit.

Figure 1.3: An example of Jitter

A PLL can be used to reduce jitter. The deviation of the signal from its ideal zero crossing position is called as jitter. with the use of high speed PFD the reduction in jitter can be achieved. That PFD followed by charge pump and loop filter will further reduce the jitter.

1.5 Motivation for The Project
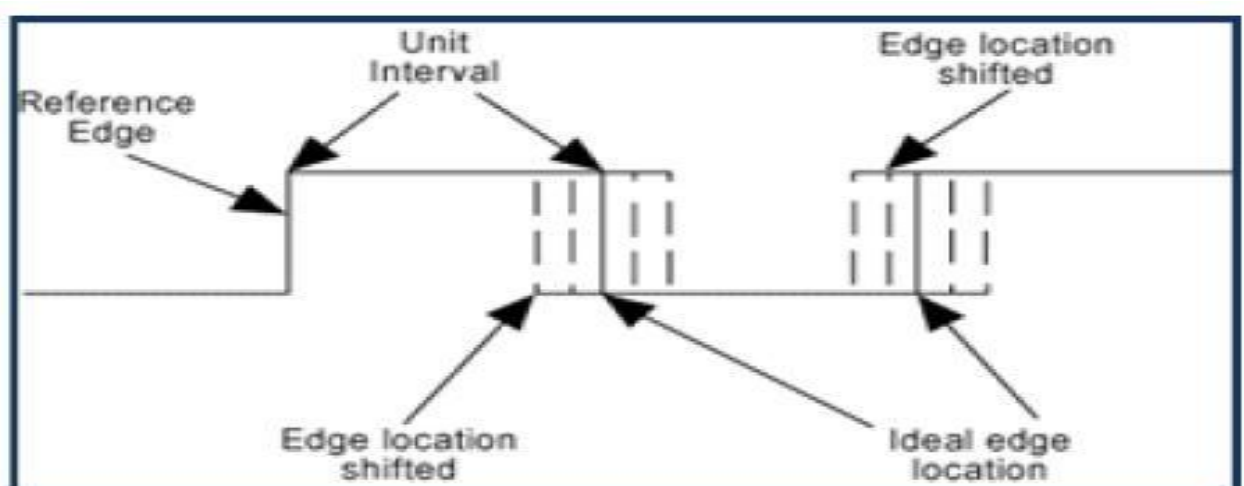
We are witnessing the dominance of microelectronics (VLSI) in every spectrum of "Electronics and Communication" forming the backbone of modern electronics industry in Mobile Communications, Computers, State-of-Art Processors etc. Designing high performance analog circuit is becoming increasingly challenging with the persistent trend towards low power consumption and supply voltages.[14],[3],[9] In today's world, where demand for portable battery operated devices is increasing [6], a major thrust is given towards low power methodologies for high speed applications.[7] This reduction in power can be achieved by moving towards smaller feature size processes [4]. However, as we move towards smaller feature size processes, the process variations and other non-ideality will greatly affect the overall performance of the device[5]. One such application where low voltage,low jitter,low power dissipation, low noise ,high speed are required is phase lock loop for one particular application - clock generation for microprocessors and portable devices.[11],[10].In the design of PLL the considerable parameters are low jitter , low power consumption,high speed,higher frequency range with lower noise.All these parameters can be achieved with some small modifications in the different blocks of the PLL. In the literature,[12],[8],[2],[1] a few design of PLL can be found for the clock generation application.Since the jitter is proven to be inversely proportional to the power consumption [13],a trade-off between these two parameters must be found.The proposed implementation features simultaneous low jitter and low power consumption is achived.However, very little emphasis is placed on actual details of operation of these structures along with experimental results to

compare jitter, power consumption, and supply voltage of the PLL structure.A new phase lock loop for the clock generation design which achieves low jitter, low power consumption, high speed at low voltage supply has been presented.

1.6   Desertation Report Organization

The rest of the content of the thesis is organized as follows.

Chapter 1 introduction: This chapter mainly deals with a brief introduction to phase locked looping and the clock generation circuit.

Chapter 2 PLL : This chapter describes the design of PLL and the locking of PLL used for the clock generation.

Chapter 3 simulation results and analysis: This chapter depicts the pre-simulation results observed for various PLL building blocks. The post simulation results with lay out is discussed. The analysis done form the results are also discussed in this chapter.

Chapter 4 references: In this chapter all the references are covered from where the related material is found.

Chapter 5 Conclusion and Future work: In this chapter the design of PLL for clock generation is concluded and the future work is discussed.

Chapter 2

PHASE LOCK LOOP

This chapter deals with the design of phase lock loop with the detailed block diagram of each block. Working of each block with reduced jitter is explained in this chapter.The phase lock loop particularly used for the purpose of clock generation in this thesis. In the later chapter the particular work of clock generation is explained.

2.1   General considerations

As illustrated in the following figure, the phase lock loop with the following features work for the clock generation. The design of the PLL will start with the very basic block diagram of the phase lock loop. Figure 2.1 shows the typical block diagram of phase lock loop.
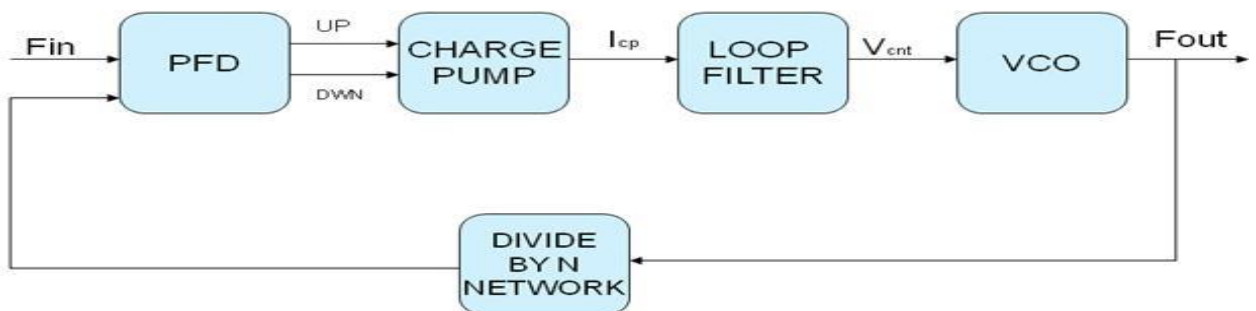

Figure 2.1: Basic block diagram of phase lock loop

From the basic block diagram, PLL system can be easily recognized as a feedback control system. As it was mentioned, the clock generation is achieved using PLL.PLL is the circuit that synchronizes the output signal with the reference signal and hence the name Phase Lock Loop. This system consists of following main components:

a. Phase Frequency Detector

b. Charge pump

c. Loop filter

d. VCO

e. Divide by N Network

If the frequency and phase of the input signal and output are the same, the output of phase and frequency detector must be zero. Therefore, the output signal of loop filter will be a constant value. This constant voltage is to be used as the input to the voltage controlled oscillator. Constant input voltage to the VCO will result in constant frequency of the output signal of that VCO. Thus, the output frequency is locked at the value N*Vref. If the phase/frequency difference between reference and output signal of PLL, PFD would develop a nonzero output signal either at Up or Dn terminal, which represents phase difference between the input signal and output signal of VCO in the form of voltage. The output of the loop filter will change accordingly. Because input voltage of VCO changes, output frequency of VCO will also changes. After sometime, PLL output frequency the same as the input frequency i.e. PLL will be in locked condition. Specifications of the intended PLL are shown in the table 2.1:

2.2   Phase Detector

The main function of Phase detector is to sense the phase difference between input clock and the output clock of the VCO. The PFD generates the phase difference in

Table 2.1: Design Specification

Input frequency range	250 MHz
Vdd	$3.3V$
Vss	$0V$
Maximum voltage of input signal to PFD	$3.3V$
System frequency	$1GHz$
Technology	$.35\mu$m

terms of voltage which is further applied to the VCO in the form of control voltage (Vcntl) through charge pump and low pass filter. As we know there are two types of digital phase detectors.

a. XOR Phase detector

b. Phase Frequency Detector

2.2.1   Phase frequency detector (PFD):

Phase frequency detector is one of the important part in PLL circuits. PFD (Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal. PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals. Fig. 2.2 shows a block diagram of PFD with its inputs and outputs.CLKREF and CLKVCO are the two inputs of PFD and UP and DWN are two outputs of PFD block. If both the input signals are in synchronization with each other than output signals are at ground condition. If CLKREF is leading than that error reflects at output in the pulse width of DWN signal and UP signal is ground. If CLKVCo is leading than UP signal has pulse train with the pulse width of that error between two input signals.
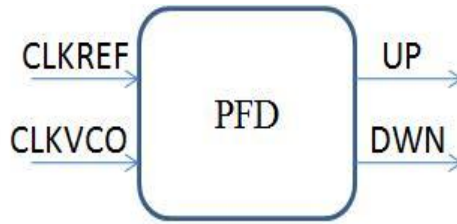
Figure 2.2: Phase Frequency Detector

The main problem of the lock acquisition is that the acquisition range relies upon WLPF .That is, it is required that the (w2 -w1) should be lesser than WLPF .this introduces a trade-off given as follows.

If WLPF of the LPF is reduced in an attempt to minimize the ripples on VCNT, the acquisition range of the LPF would decrease. But increasing the acquisition range would increase the ripples on VCNT. Thus to keep a track on the frequency difference in addition to the phase difference, a FD is also added. This kind of acquisition is called as "aided acquisition". Hence it is required to have a PFD instead of simply a PD. It merges the operation of PD and PFD for proper data acquisition.
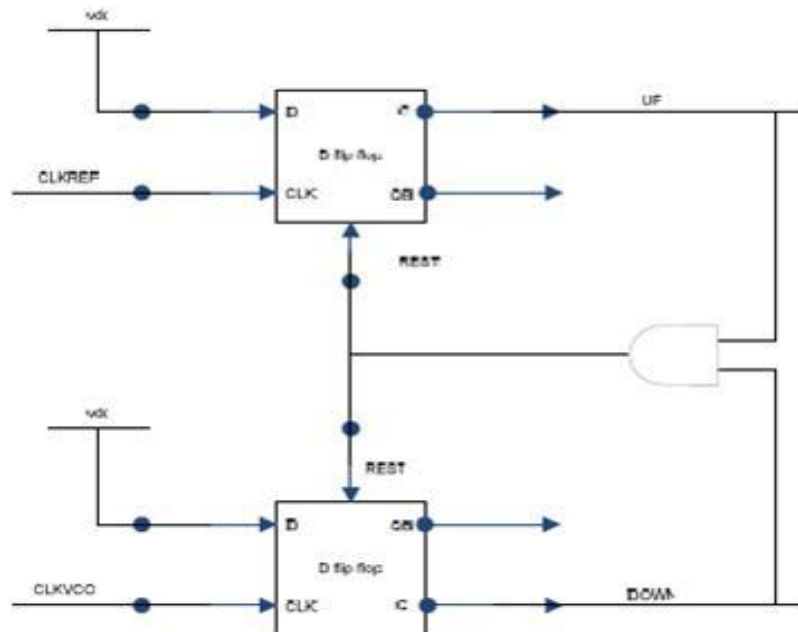

Figure 2.3: Traditional PFD

Figure 2.3, shows a detailed design for PFD. A simple design of PFD say TYPE I PFD consists of two D flip flops and AND gate. As the figure shows the D input of the flip-flops is connected to VDD and the input signals (CLKREF, CLKVCO) are applied to the clock input. When one of the clocks change to high, this flip-flop will charged and change its output to high. The AND gate is for preventing both flip-flop to be high at the same time. As we can see the inputs of the AND gate are the both Up and DOWN signal from both flip-flops, and the output of the AND gate is connected to the reset input of the flip-flops. As soon as both outputs (UP, DOWN) are high the AND gate will generate a high signal that will reset both flip-flops avoiding the situation of both high at the same time.
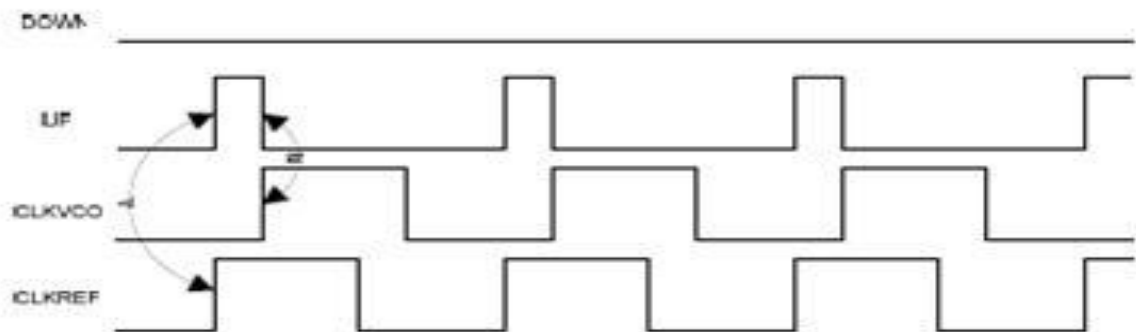

Figure 2.4: Signals Transaction

Figure 2.4 shows the signal transaction of the Type I PFD, when both the signals are not equal. When both the frequencies are equal then UP (QA) and DN (QB) signals are pulses for very small duration. This is because both flip-flops will get reset as they will get logic 1 level at their output.

2.2.2 Dead Zone:

As we mentioned before, dead-zone is due to small phase error. When the phase difference between PFD's input signals, the output signals of the PFD will not be proportional to this error. The reason of this problem is the delay time of the internal components of the flip-flop and the reset time that need s the AND gate to reset both flip-flops.
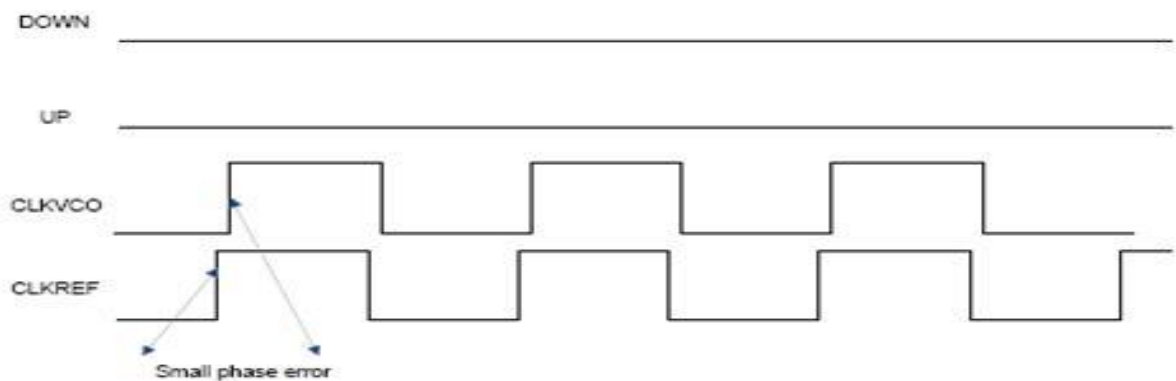

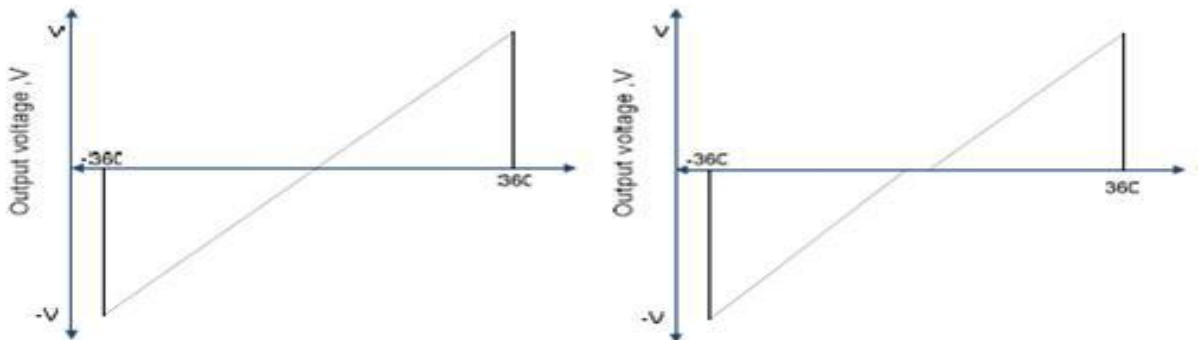Figure 2.5: Signals Transaction with dead zone

Figure 2.6: Phase error with and without dead zone

This is due to inability to detect the phase error in this region. As shown in the figure 2.5 and 2.6. Plenty of solution has been done for this problem some of them reduce the delay time in the internal components of the PFDs, other solution eliminate the reset path by implementing new reset techniques that will not create a delay and

produce a high speed PFDs.

2.2.3 Type I PFD (Traditional PFD architecture):

The design consists of two flip-flops and a NOR gate. The design is implemented using .35 μm CMOS Technology.As the design is simulated using CMOS technology in place of AND gate ,as shown in the tradition block diagram ,here NOR gate is used.Bubbled AND gate is equal to NOR gate.Due to the reset path this design suffers from large dead zone.In the reset path the delay of reset path and the delay of NOR gate is added. The schematic design of traditional PFD with two D flip-flop and one NAND gate is shown in figure 2.7.
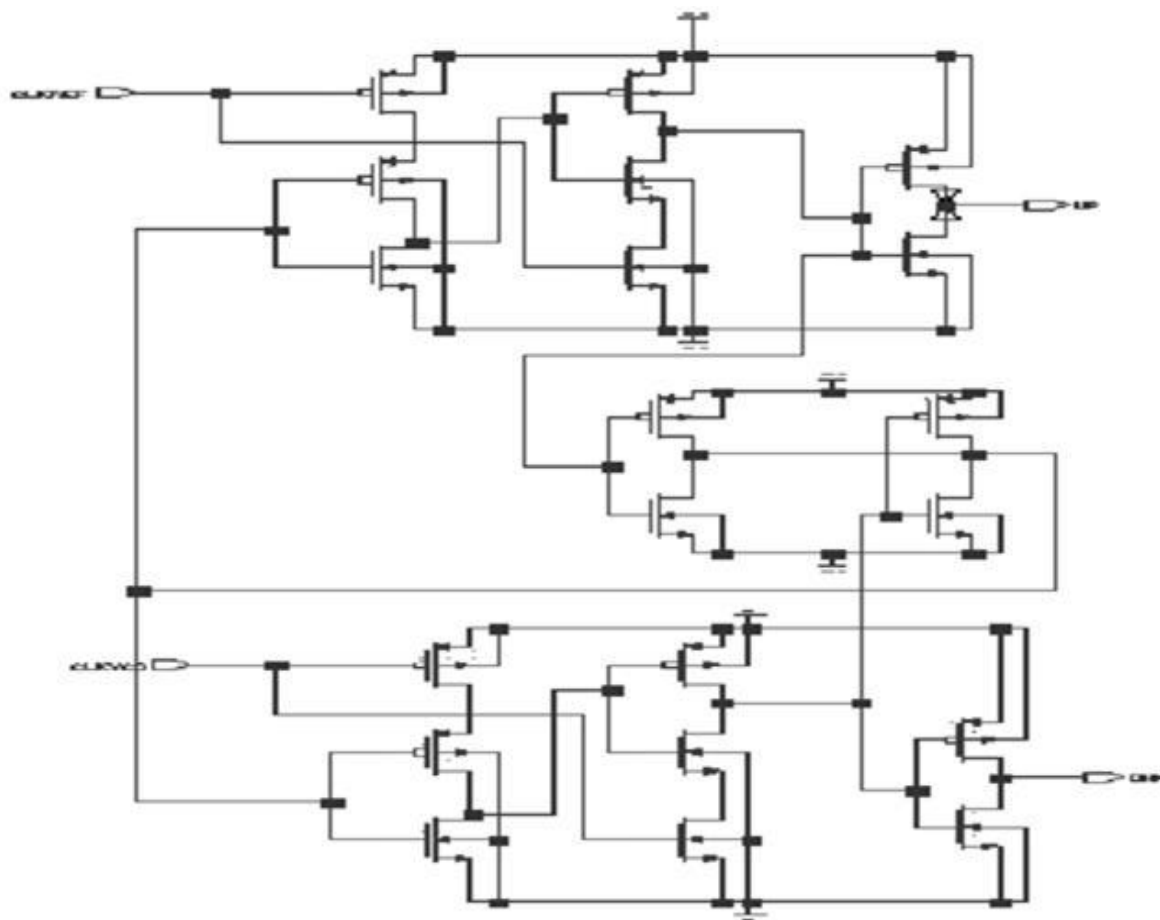

Figure 2.7: Implementation of Traditional PFD

Because of the high power consumption and the large dead zone of type I, some modifications have been done with this design. The modification on type I PFD has enabled us to remove the reset path gate and reduce the delay time of the digital gate that causing the dead zone problem.
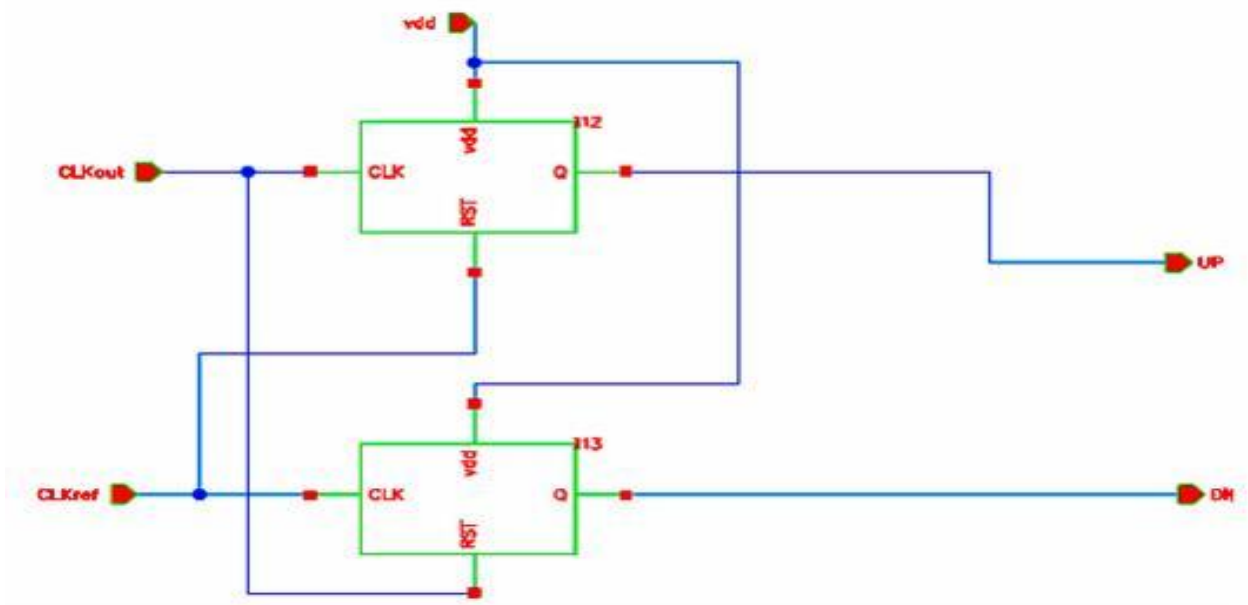
2.2.4 Type II PFD :

Figure 2.8: Block Diagram of Type II PFD

In order to reduce the dead zone some modifications are done with the type I PFD . So new Type II PFD block diagram with connection and the actual implementation is shown below in figure 2.8 and 2.9. As shown in the figure 2.8 - the block diagram of type II PFD ,in the reset path in place of digital gate connection direct connection from reset of D-flip flop signal to respective clkref and clkout. Which reduces the delay and the dead zone.

In type II PFD the D flip-flop schematic design has few changes from the original type I PFD as shown in the implementation of type II PFD. With this arrangement fifty percentage of jitter is reduced and the power consumption is also redused.But still there is smaller dead zone that can be improved with high speed PFD. In this type III PFD the feedback path is totally removed so automatically the delay time is reduced and so the dead zone.
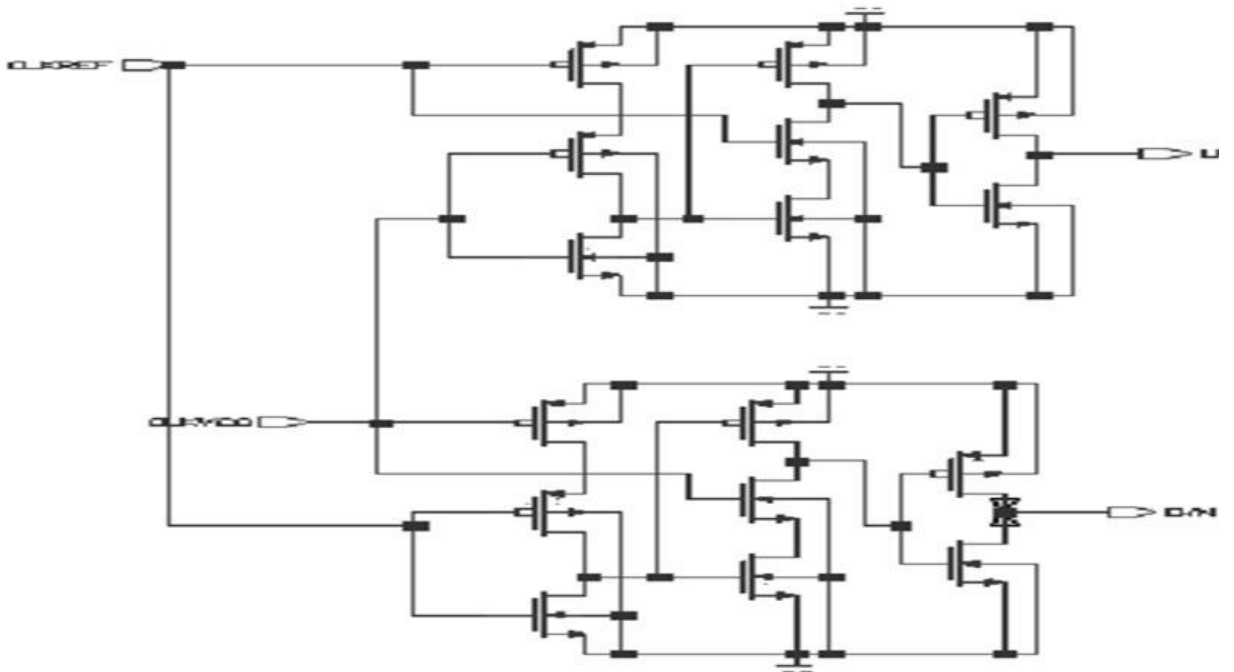

Figure 2.9: Implementation of Type II PFD

2.2.5 Type III PFD(High Speed PFD):

To be able to achieve a higher speed than the type II PFD as discussed, another design is being proposed in this section. This design eliminates the reset path, which will lead to a smaller time delay. To be able to detect the phase error and has a fast reset, this design depends on detecting the raising and falling edge of two input signals to do the job. From the implementation of the type III PFD , has six transistors with

the pair of NAND gate and inverter.Instead of having feedback reset path, both CLK signals will reset both outputs as soon as they are high at the same time.
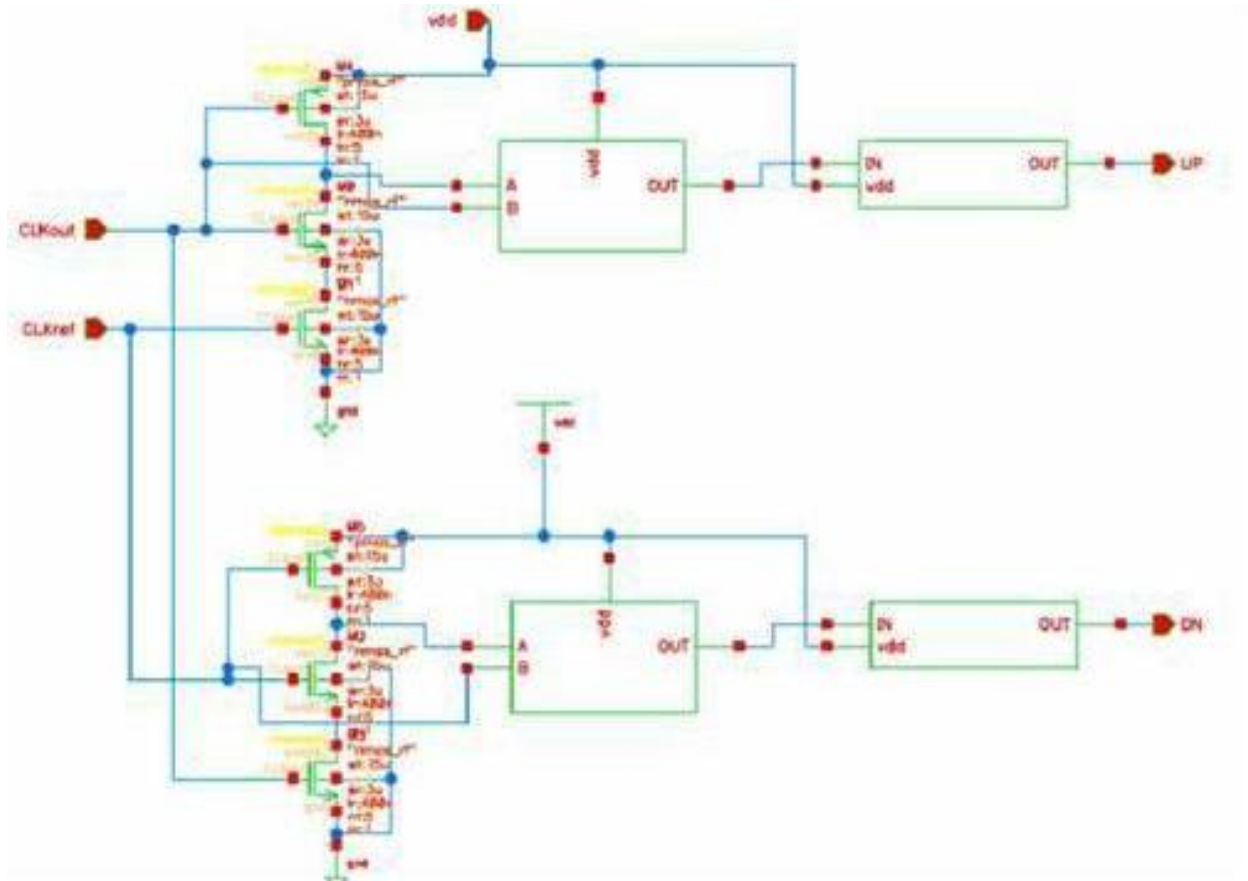

Figure 2.10: Schematic design of Type III PDF

With these results, Type III PFD is the best candidate for our PLL design since it has low power consumption and almost zero dead zone. With this high speed PFD the simulation is done with 50 MHz, 250 MHz and at 1 GHz. For this project input frequency is 250MHZ and system frequency is 1 GHZ - CLKREF to the high speed PFD is 250 MHz frequency.
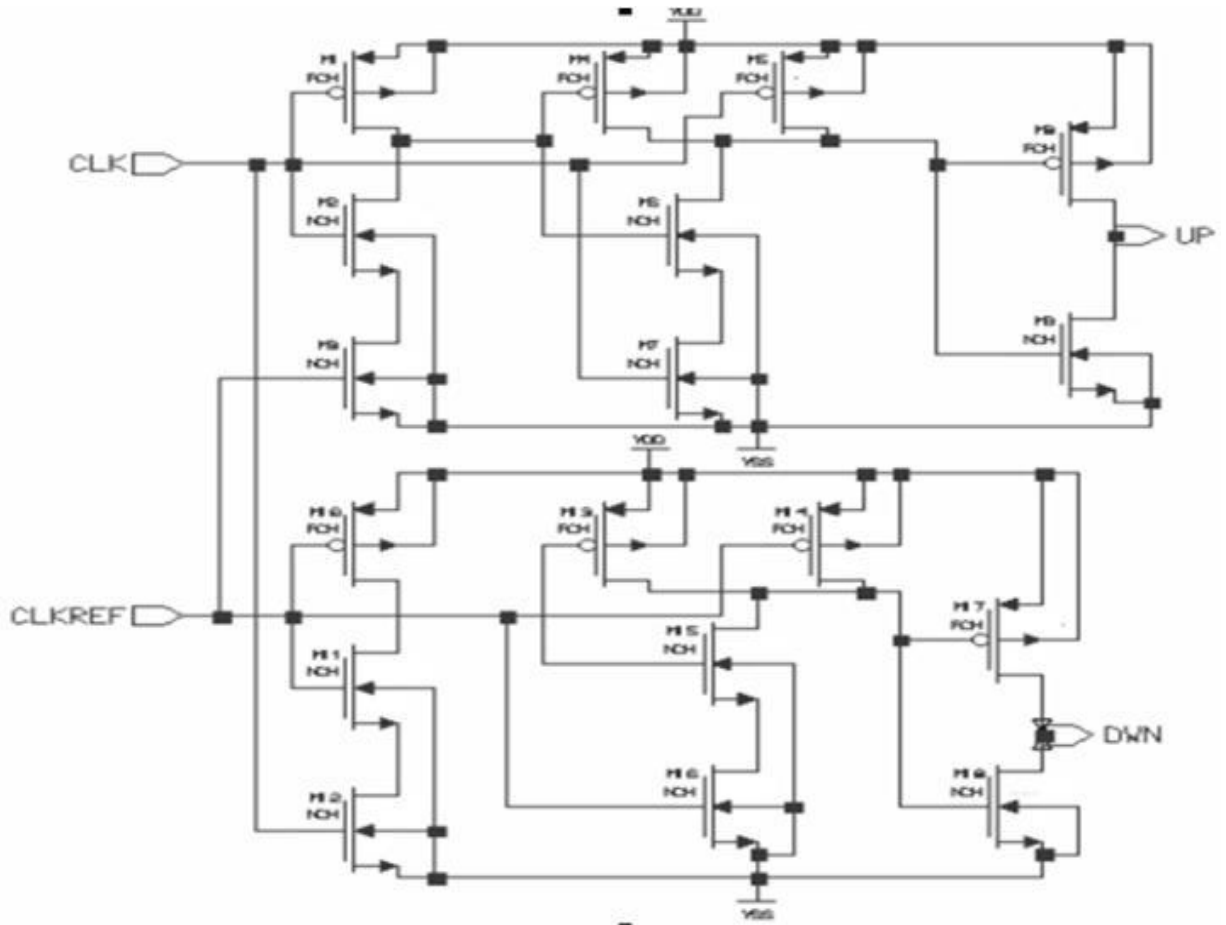
Figure 2.11: Implementation of Type III PDF

2.3 Charge Pump:

Charge pump is the circuit that translates the UP and DOWN signals from the PFD to control voltage that will control the VCO. The main purpose of a charge pump is to convert the logic states of the phase frequency detector into analog signals suitable to control the voltage-controlled oscillator (VCO).[9] Basically, the charge pump consists of current sources and switches. The output of the charge pump is connected to a low pass filter that integrates the charge pump output current to an equivalent VCO control voltage (Vcntl). Figure below shows a typical charge pump cascaded with a loop filter.

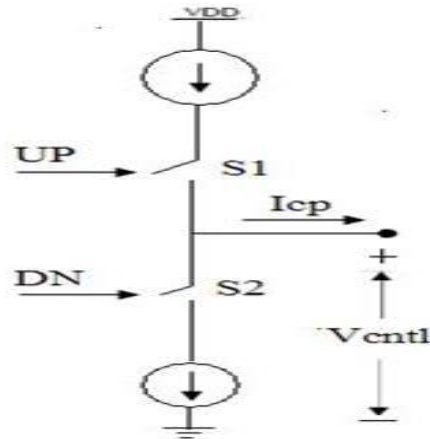When UP signal is high, the switch S1 will be closed and there will be current Icp

Figure 2.12: Generalized Charge pump

charging the loop filter. When DN signal is high, the switch S2 will be closed and there will be current Icp discharging the loop filter. The charge pump can be treated as three-state device that gives an output current of +Icp, -Icp, or zero (in ideal case), depending on the combination of UP and DN signals.

Table 2.2: Working conditions of charge pump

UP signal	DN signal	Condition	Note
1	0	Charging	I_{cp} flows into filter
0	1	Discharging	I_{cp} flows out from filter
0	0	V_{cnt} Constant	$I_{cp} = 0$
1	1	V_{cnt} Constant	I_{cp} Constant

When the VCO output frequency is leading the reference frequency, the PFD will activate the DOWN signal and deactivate the UP signal. Hence, switch S1 will be opened and switch S2 will be closed. This time, current ICP will flow out from the filter and reduce the Vcnt. Consequently, the VCO output frequency is decreases. The lock condition of the PLL is established when the VCO output frequency is the same as the reference frequency. During this period, the PFD will deactivate both up and down signals. Hence switches S1 and S2 will be opened until the VCO output frequency changes. Since switches are open, there is no current path formation, hence
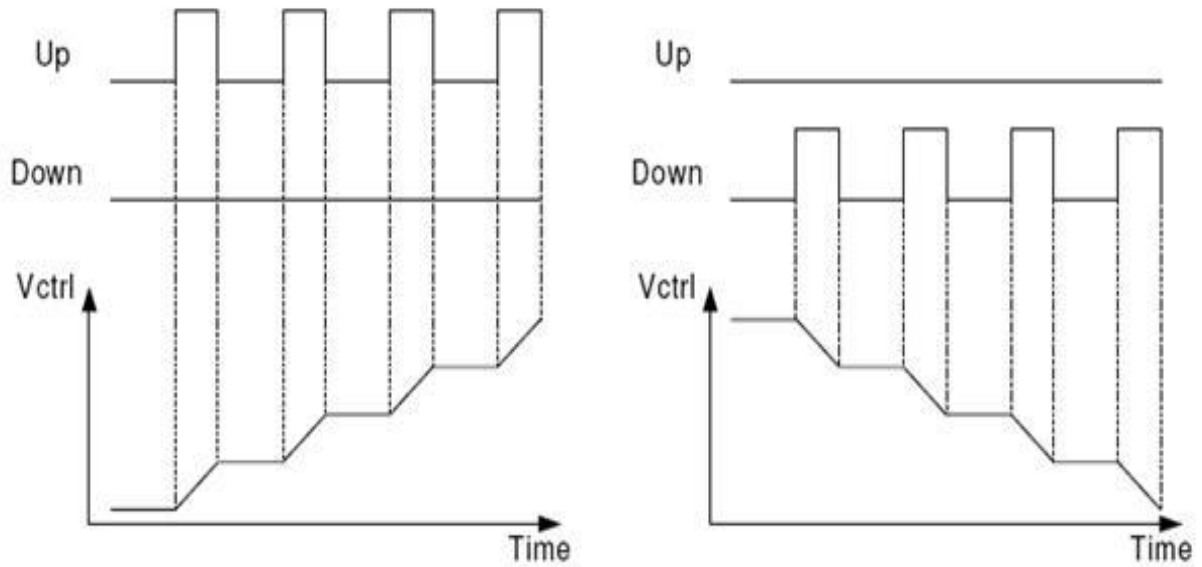
Figure 2.13: Ideal Behavior of Charge Pump

no current will flow into or out from the filter. Ideal behavior can be given by the figure.

2.3.1 Non-idealities in the Charge Pump and the Effect

The charge pump that is supposed to be ideal, in practice, has some nonidealities. When the UP =DN=1, the charge pump is not supposed to produce any current to the loop filter. In reality, it still delivers current which will change the control voltage of the VCO since both current sink and source cannot be exactly same.[**?**]

2.3.2 Sources of these non-idealities

1. The mismatch in charging and discharging current. This is due to the effect of the channel length modulation of the MOS while PMOS and NMOS are typically used as the output transistors. Different levels of control voltage of the loop filter will yield in different levels of voltage between drain and source of the PMOS and NMOS. So even though the current sources for charging and discharging have equal magnitude,

match will only occur at one particular control voltage.

2. Mismatch in the turn on time (delay and rise time) of the charging and discharging current.

3. Mismatch due to the leakage current in the charge pump.

4. Among these non-idealities, the significant effect to the reference spur comes from the mismatch in amplitude and leakage current.
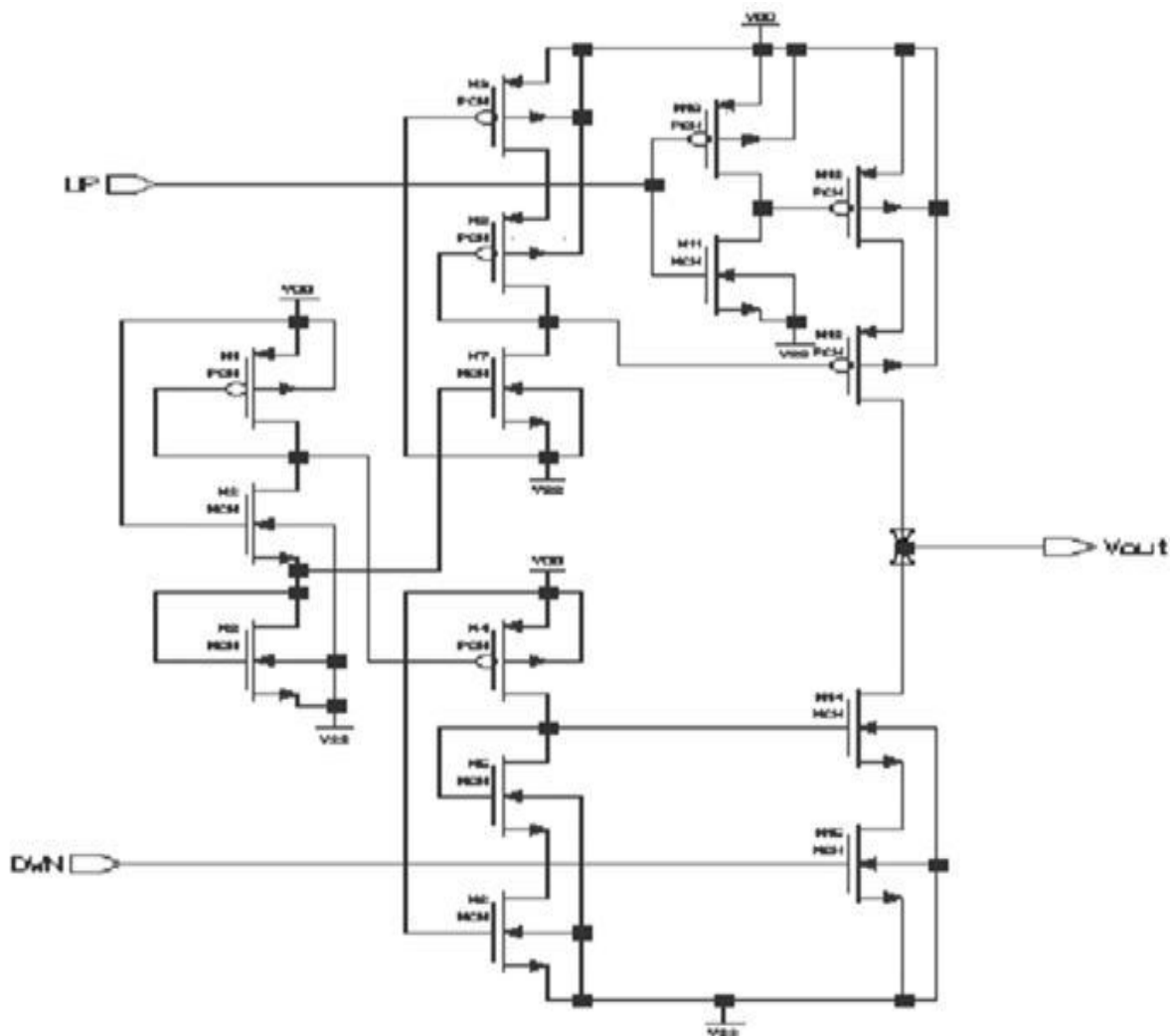
2.3.3   Implementation of charge pump

Figure 2.14: Implementation of charge pump

2.4   Loop Filter:

The inclusion of a loop filter at the output of the Charge Pump serves two functions. First, the loop filter integrates the pulses to produce a time-average, or continuous value. Second, it defines the loop bandwidth, which in turn affects the capture range, jitter and bandwidth. The dynamic characteristics of the phase-locked loop are therefore governed principally by the loop filter. Therefore, choosing the best loop filter is a critical step in a PLL design. Selection on the most suitable filter for the PLL circuit based on specifications required provides a superior performance both in time and frequency domain. Furthermore, the loop filter values should be chosen to optimize the overall loop performance instead of a particular characteristic. For example, the output jitter is reduced to some extent by decreasing the loop bandwidth. This, however, reduces speed of the response. There are two types of loop filters, passive and active filters. Passive filters consist of only resistors and capacitors while active filters have active elements in addition to the passive elements. Very often, a low pass filter is used as the loop filter. This low pass filter serves as a device to filter out any high frequency harmonics from the phase detector and to provide a time average DC signal output, which becomes the input voltage for the VCO.

2.4.1   Analysis of Loop Filter Designs

There are three commonly used loop filter designs. They are the first-order design, the second-order design and third-order design.For this project second order low pass filter is used as loop filter to serve the purpose.This loop filter converts the Icp current from the charge pump to control voltage Vcnt, which is the input to the VCO for generation of new frequency range.
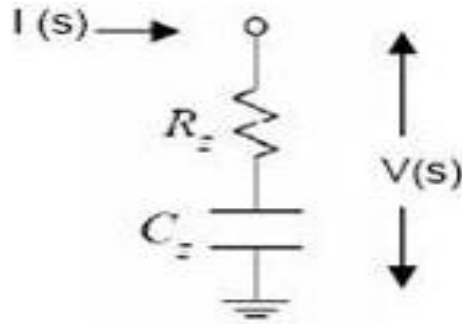
2.4.2 First-Order Loop Filter Design

Figure 2.15: first order Loop filter

The first-order loop filter design consists of a single resistor and capacitor. This filter can also be constructed by only a capacitor which will add only a pole in the transfer function. Adding a resistor in series with the capacitor will add a zero in transfer function. This will enhance the stability of the system. Simply stating the function of the capacitor is to suppress high frequency variations form the charge pump output and the function of the loop filter is to convert the current from the charge pump to a voltage, the transfer function is V(s)/ I(s) .

$$V(s) = I(s)Z(s)$$

$$V(s) = I(s)\left(R_z + \frac{1}{sC_z}\right)$$

$$\frac{V(s)}{I(s)} = \left(\frac{R_zC_zs + 1}{C_zs}\right)$$

The first-order loop filter does not have a second capacitor to smooth out current spikes. Since the charge pump drives the series combination of resistor and capacitor, each time a current is injected into the loop filter; control voltage experiences a large jump. Even in locked condition the mismatch between +ICP and -ICP, charge injection and clock feed through of switch S1 and S2 introduce large voltage jumps in

Vcntl. The resulting ripple severely disturbs the VCO corrupting the output phase. The ability to slow down spontaneous transitions is a very important feature and thus, a major disadvantage in this type of loop filter.

2.4.3   Second-Order Loop Filter Design

The second-order loop filter has the second capacitor to smooth out current spikes.The circuit connection and the transfer function are as following:
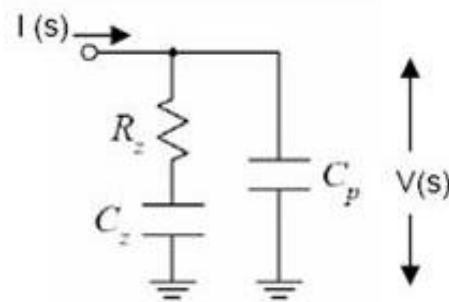

Figure 2.16: Second-Order Loop Filter

$$\frac{V(s)}{I(s)} = \frac{sR_zC_z + 1}{sC_p\left(1 + \frac{sR_zC_zC_p}{C_z+C_p}\right)}$$

This type of filter has two poles one at low frequency and one have high frequency and a zero which will add the stability of the system. So finally with the use of one resister and two capacitor the loop filter will work as low pass filter and full fill the requirement. Here the second order low pass filter generates the range of control voltage from 0v to 1.89v.

2.5 Voltage Control Oscillator:

Oscillators are used to create a periodic logic or analog signal with a stable and predictable frequency.VCO is an electronic oscillator specifically designed to be controlled in oscillation frequency by a voltage input -Vcnt form the loop filter.General requirements for a high-quality VCO include high spectral purity, linear voltage-to-frequency transfer characteristic, and good frequency stability to power supply and temperature variation.VCO must also have very low power consumption and low fabrication cost as well.

List of types of VCO:

a. LC VCO

b. Current starved VCO

c. Source coupled VCO

d. Differential VCO

Placing the highest priority on speed implies that the CMOS oscillator must be constructed using the simplest structures, such as an odd-number inverter ring oscillator. To obtain high speed performance and low power the VCO design methodology follows the guidelines as below.

1. Minimize all parasitics by using the circuits with minimum complexity.

2. Choose those architectures which enable circuits to operate at maximum speed.

3. Utilize unavoidable parasitics. No external reactive elements.

To fulfill all the requirements Current Starved VCO is used in this project as VCO block. Which comprises of Odd numbered chain of inverters and two input stage transistors, which limits current flow to the inverter.The output of VCO is buffed with the use of two inverters at the end of the VCO output.
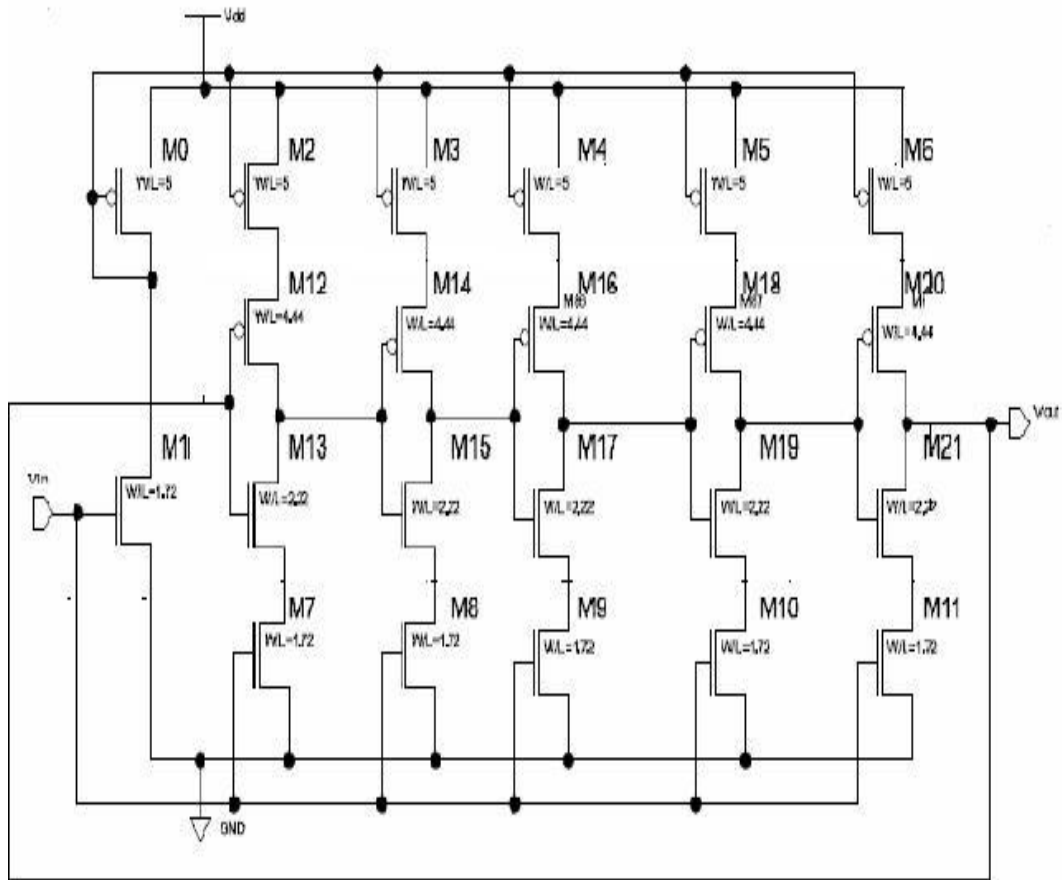
Figure 2.17: Implementation of VCO

The current-starved VCO is shown. The operation of the current-starved VCO is similar to that of a ring oscillator. Ideally, in the VCO configuration, the ring of inverters consists of an odd number of inverting stages to ensure that the oscillator will self-start. In the case of this design, five number of inverting stages are constructed. MOSFETs M12 and M13 operate as an inverter, while MOSFETs M2 and M7 operate as current source/sink which limit the current available to the inverter, M12 and M13; in other words, the inverter is starved for current. The MOSFETs M0 and M1 drain currents are the same and are set by the input control voltage. The currents in M0 and M1 are mirrored in each inverter/current source stage. At the out put of VCO two buffer invertors are connected. Voltage Control Oscillator generate system frequency - 1Ghz with the use of input control voltage generated by the loop filter.

To match the VCO frequency with the input reference frequency divide by N network is required. For this case input frequency is 250 MHz and the system frequency is 1 GHz - divide by 4 network is required.

2.6 Divide By N Network:

Divide By N Network for the phase lock loop is constructed with digital flip flop. The most commonly implementation is based on flip-flops such as the D, T, and JK. All these types provide similar performance capabilities and are suitable for this application. The JK flip flop configuration was selected for this project.
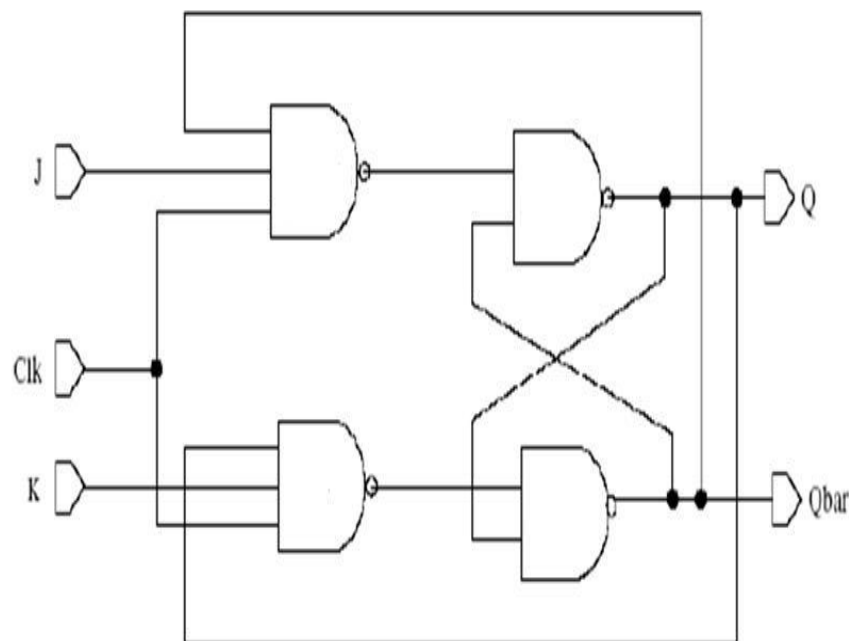

Figure 2.18: Block Diagram Of Divide By N Network

JK-Flip Flop can be configured to divide by four, the flip flop needs to first divide by two. A JK-Flip Flop has two inputs (J and K) with CLK input as tird input and two

outputs (Q and Q not). To convert the JK-FF into a frequency divider, the J and K inputs are first tied to VDD. The output signal of VCO is inputted into the CLK and the output is taken at Q. For every two periods of the input signal, the flip-flop will output a signal twice the original period. This effectively divides the signals frequency by a fact of two (f = 1/T). To divide by a factor of four, another JK-FF is implemented in the same configuration. The Q of the first flip flop is connected to the CLK of the second JK-FF and the output will have a period of 4 times larger than the original input.
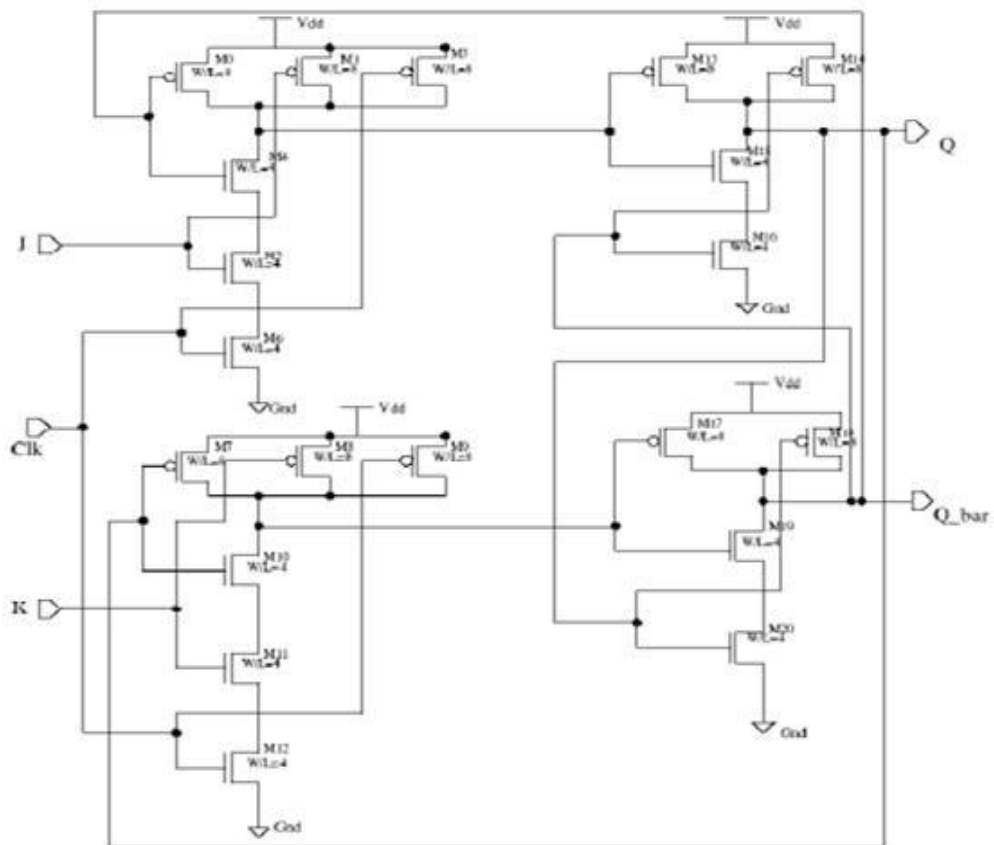
Figure 2.19: Implementation Of Divide By N Network

With the use of this divide by N network the system frequency matches with the input frequency. This frequency id the input to the PFD as second input signal - CLKVCO. With this signal the feedback path of PLL is completed and the synchronization function of the PLL is start with these two input frequencies.

Chapter 3

Simulation Results

3.1 Pre-Simulation Results

Pre-Simulation results are carried out using Eldo Spice in TSMC $0.35\mu m$ Technology and results are depicted in following Figures.Simulated wave forms are carried out at 50 MHz frequency for type I, II and III PFD with their dead zone.
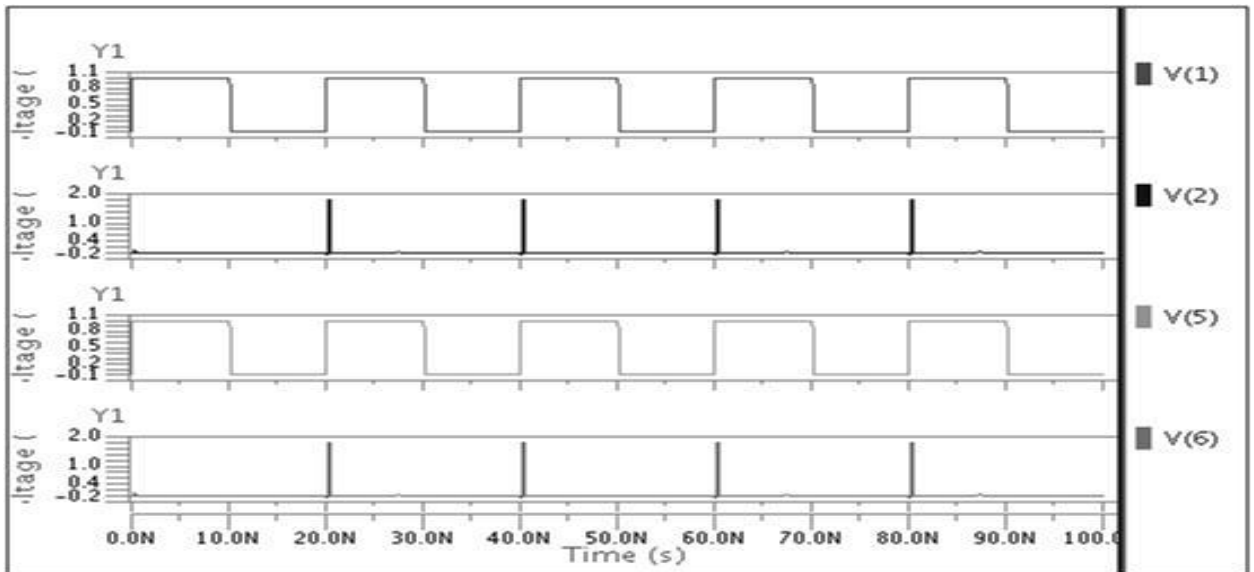
* **Type I PFD simulation waveforms:**

Figure 3.1: Type I PFD simulation
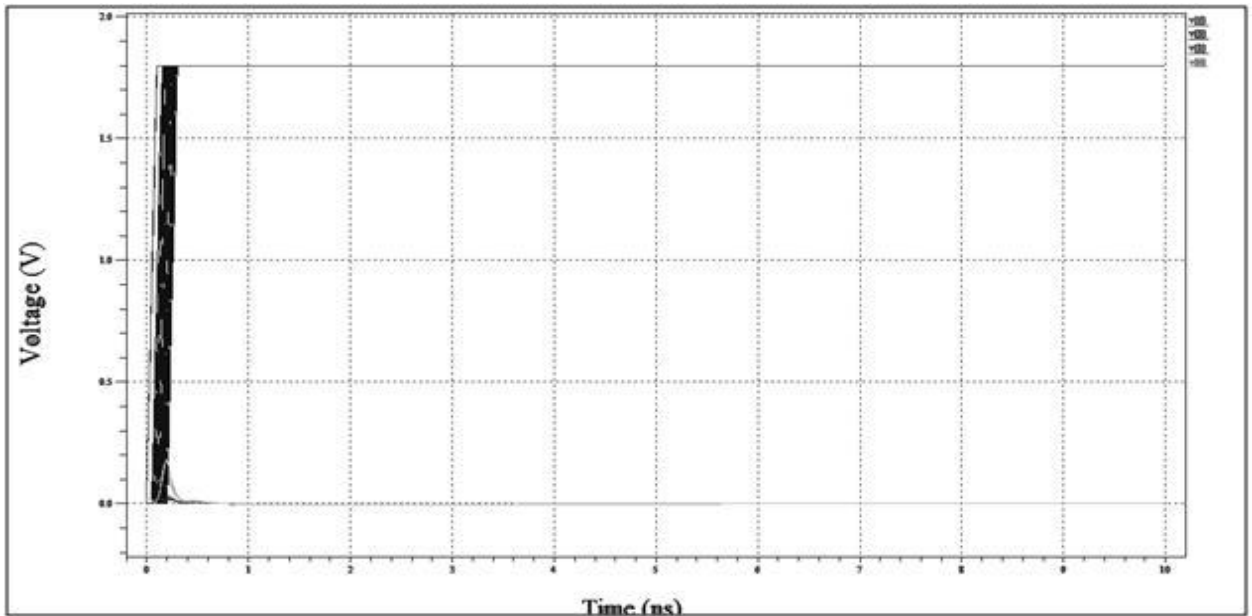
* Dead Zone simulation waveform Of Type I

Figure 3.2: Dead Zone in TYPE I PFD

Table 3.1: Experimental results of type I PFD

Input frequency range	50 MHz
Vdd	$3.3V$
Vss	$0V$
Power dissipation	$45.5watt$
Jitter	$< 70ps$
Technology	$0.35\ \mu$m

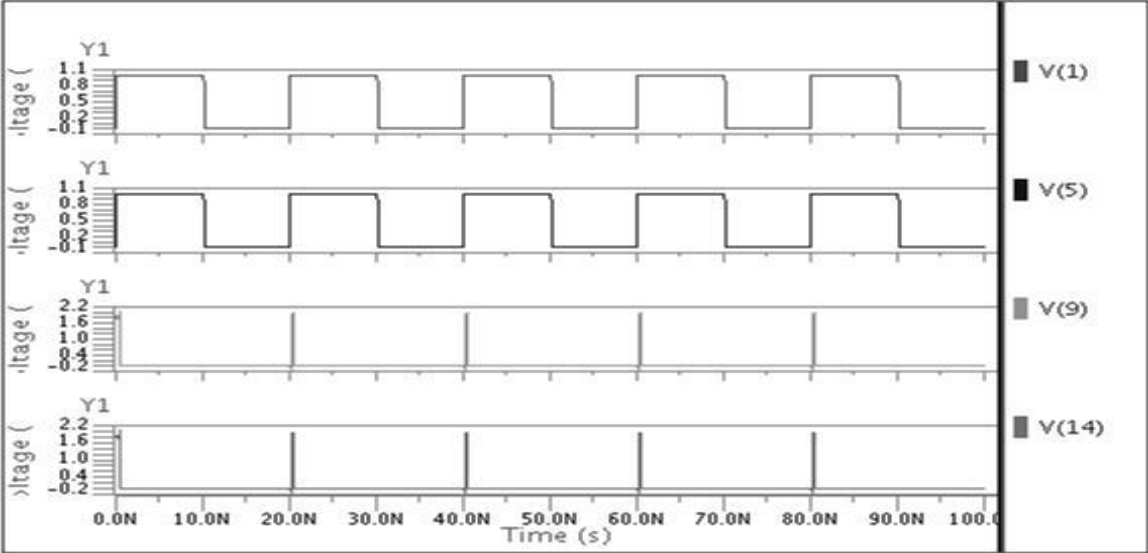*** Simulation waveform Of Type II PFD**

Figure 3.3: Type II PFD simulation

* Dead Zone simulation waveform Of Type II
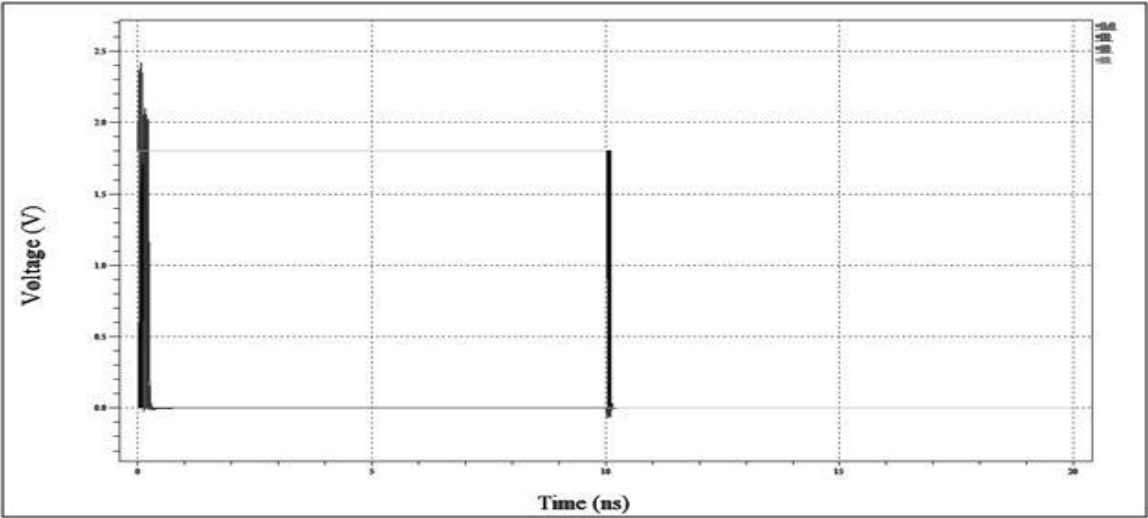
Figure 3.4: Dead Zone in Type II PFD

Table 3.2: Experimental results of type II PFD

Input frequency range	50 MHz
Vdd	$3.3V$
Vss	$0V$
Power dissipation	$2.06nwatt$
Jitter	$< 35ps$
Technology	$.35\mu$

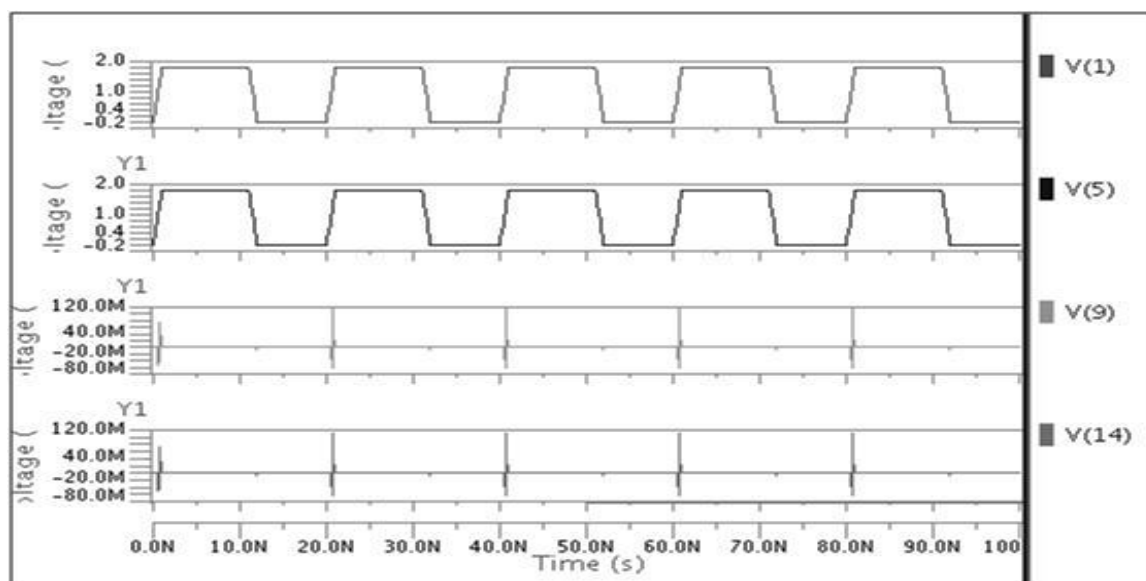*** Simulation waveform Of Type III PFD (LOCK CONDITION)**

Figure 3.5: Type III PFD simulation (LOCK CONDITION)

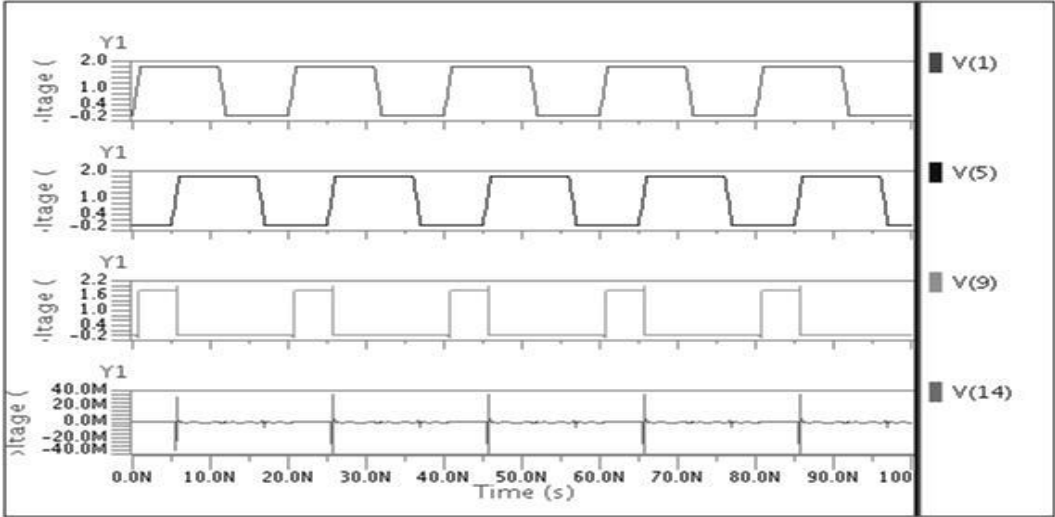*** Simulation waveform Of Type III PFD (CLKREF LEADING)**

Figure 3.6: Type III PFD simulation (CLKREF LEADING)

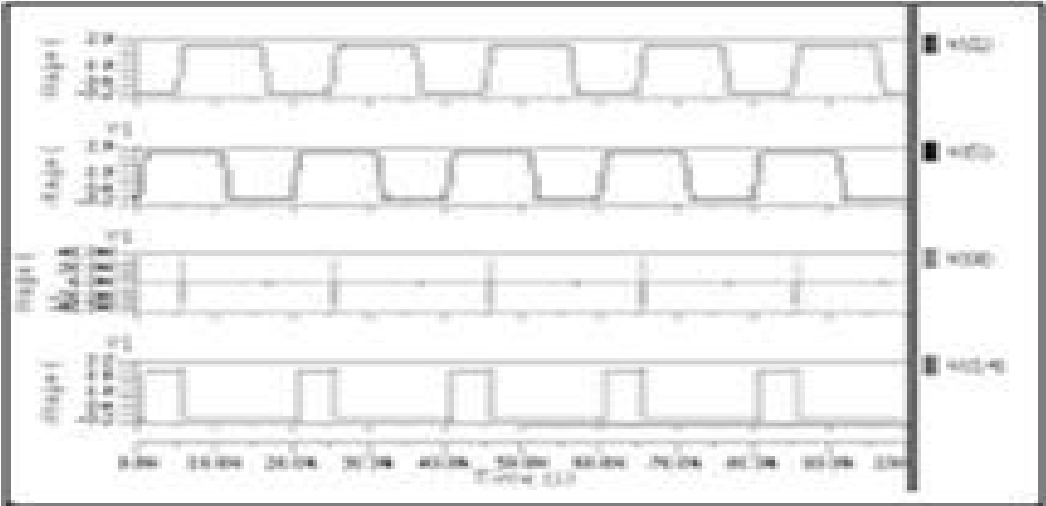*** Simulation waveform Of Type III PFD (CLKOUT LEADING)**

Figure 3.7: Type III PFD simulation (CLKOUT LEADING)

* Simulation waveform Of Dead Zone in Type III PFD

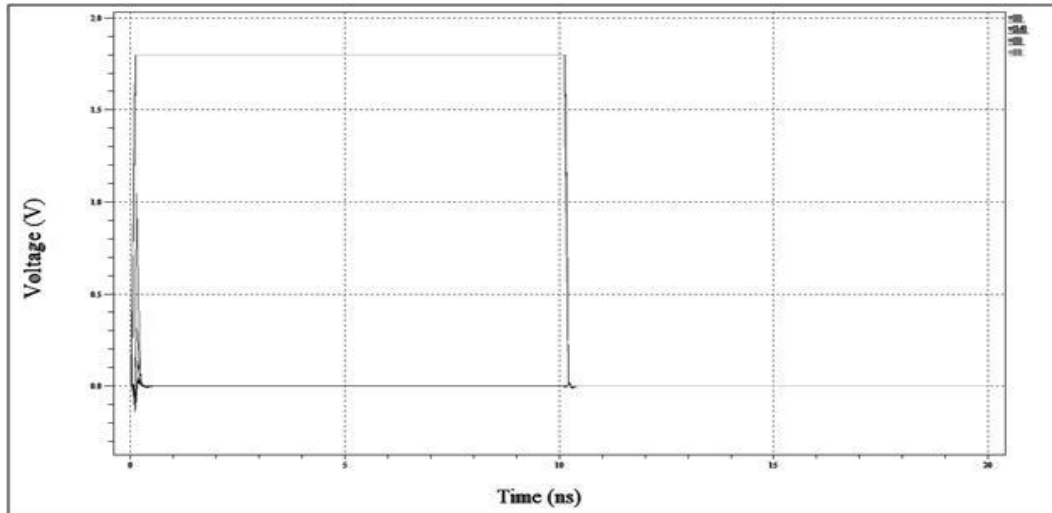Figure 3.8: Dead Zone in Type III PFD

Table 3.3: Experimental results of type III PFD

Input frequency range	50 MHz
Vdd	$3.3V$
Vss	$0V$
Power dissipation	$0.87 nwatt$
Jitter	$< 14 ps$
Technology	$.35\mu$

Table 3.4: Comparison of Jitter and Power for High Speed PFD With Different Frequency

Input frequency range	Power Dissipation	Jitter
50 MHz	$0.87nwatt$	$14ps$
250 MHz	$0.48nwatt$	$5ps$
1 GHz	$0.39nwatt$	$2ps$

With the high speed Phase Frequency Detector Jitter and power dissipation both are achieved low compare to Type I and Type II Phase Frequency Detector. The High Speed Phase Frequency Detector is the best candidate for the PFD block in Phase Lock Loop. With this PFD at 250 MHz and 1 GHz frequency the jitter and power results are good. As for this project 250 MHz frequency is selected for input frequency the jitter and power are under tolerable limits.

* Results generated by charge pump Icp = 18.6amp

* Gain of Charge Pump - Kcp = Icp/2 pi A/rad = 18.6amp / 2 pi = 2.96 A/rad

Loop filter is the second order low pass filter. The values selected for the R = 100k , C1 = 0.36pf and C2 = 15pf.

* Simulation waveform of charge pump with loop filter
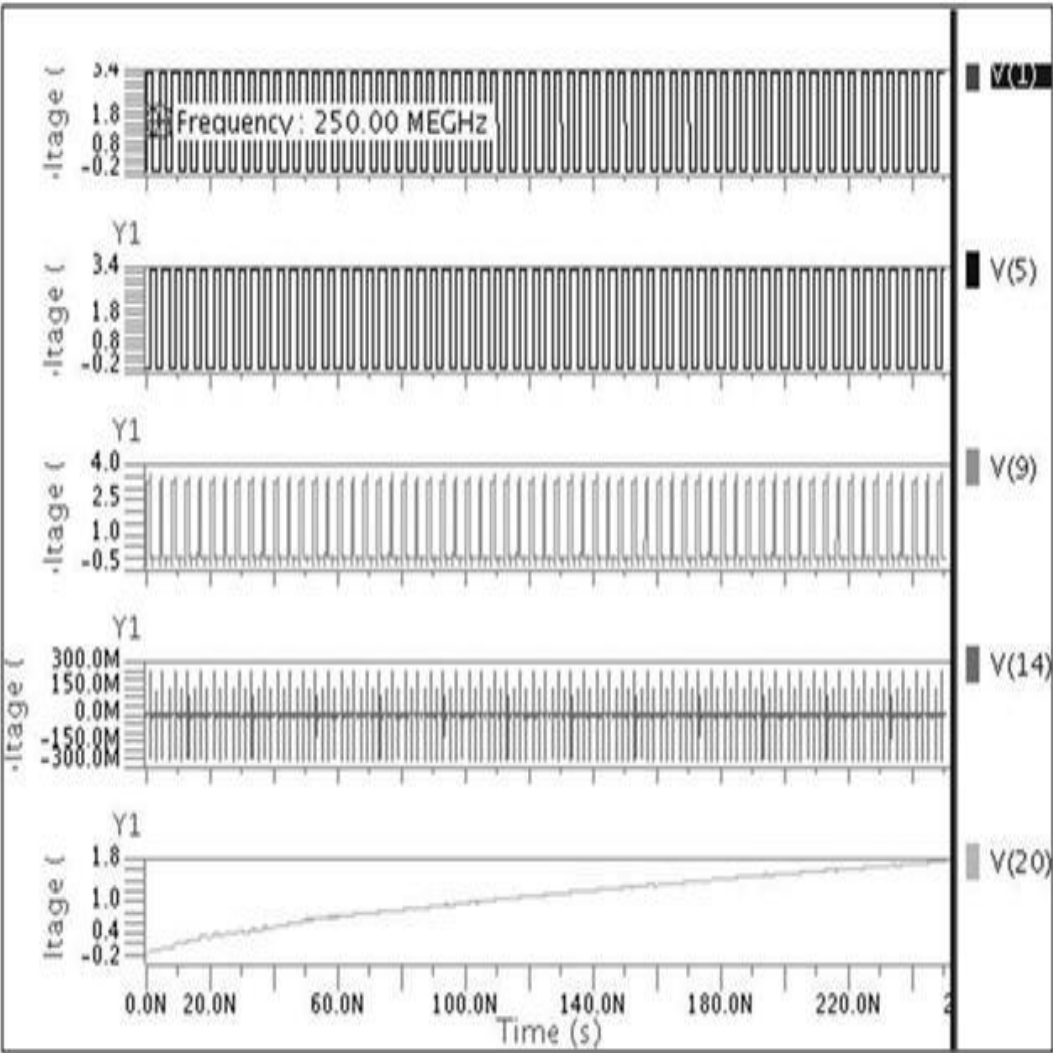
Figure 3.9: Simulation of charge pump with loop filter

Vcnt (volts)	Frequency (MHz)
0.2	100
0.3	203
0.4	315.5
0.5	402.38
0.6	530.45
0.75	620.39
0.99	731.43
1.02	803.58
1.35	890.29
1.68	910.76
1.8	996.96
1.89	1000

* Plot of VCO Characteristic

Figure 3.10: Vcnt vs. VCO Frequency

* Simulation waveform of VCO

Figure 3.11: Simulation of VCO

* Simulation waveform of Divide By 2 Network
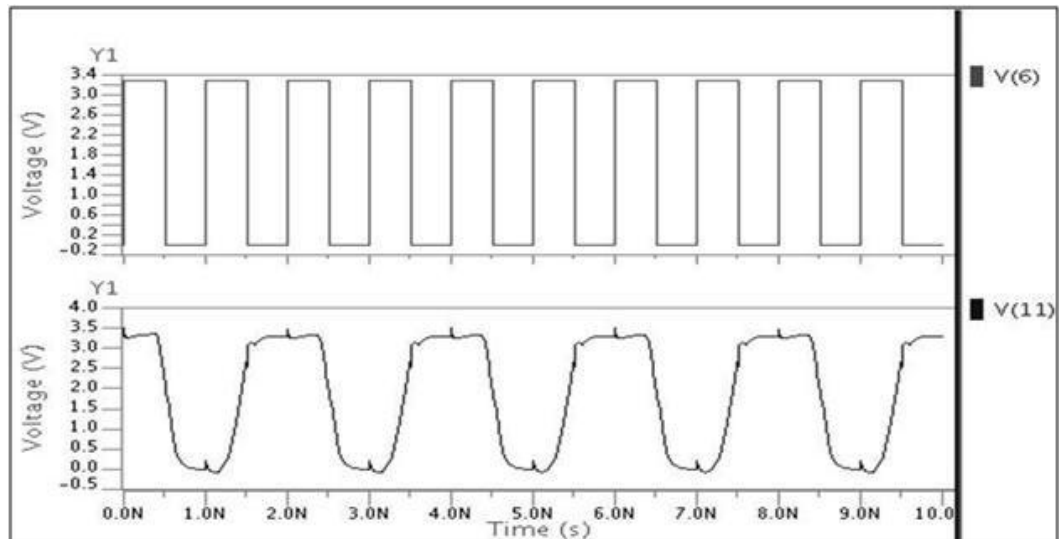
Figure 3.12: Simulation waveform of Divide By 2 Network

* Simulation waveform of Divide By 4 Network
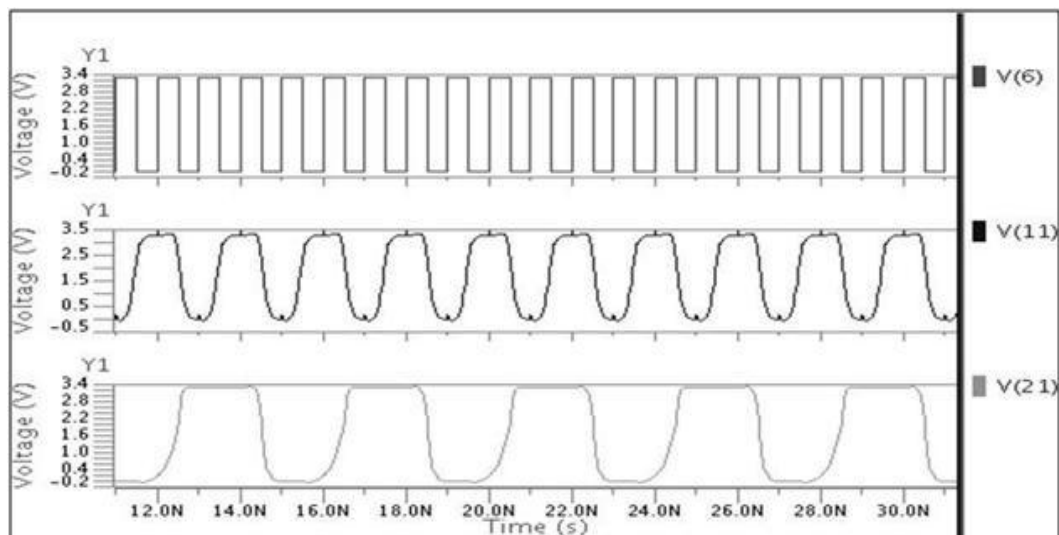
Figure 3.13: Simulation waveform of Divide By 4 Network
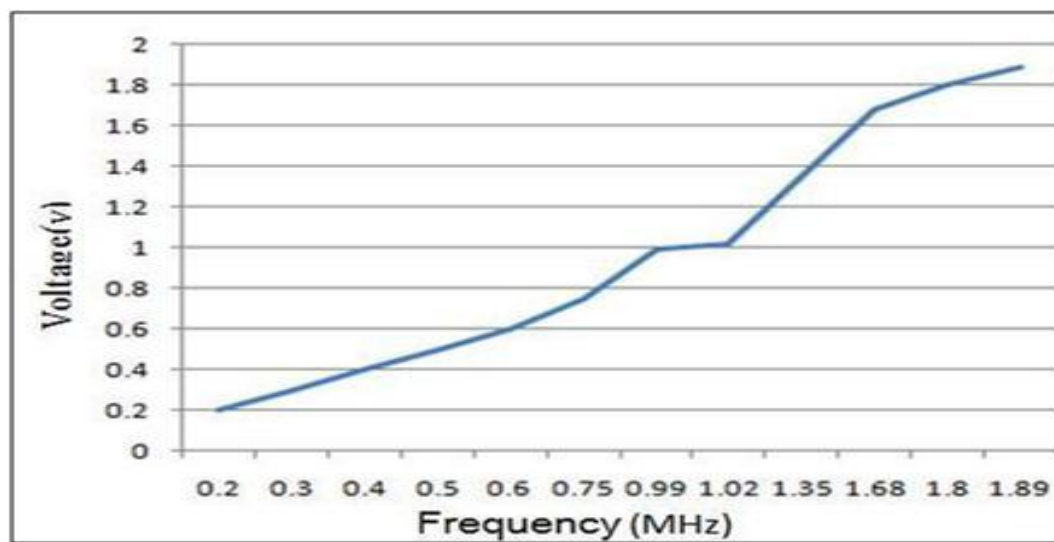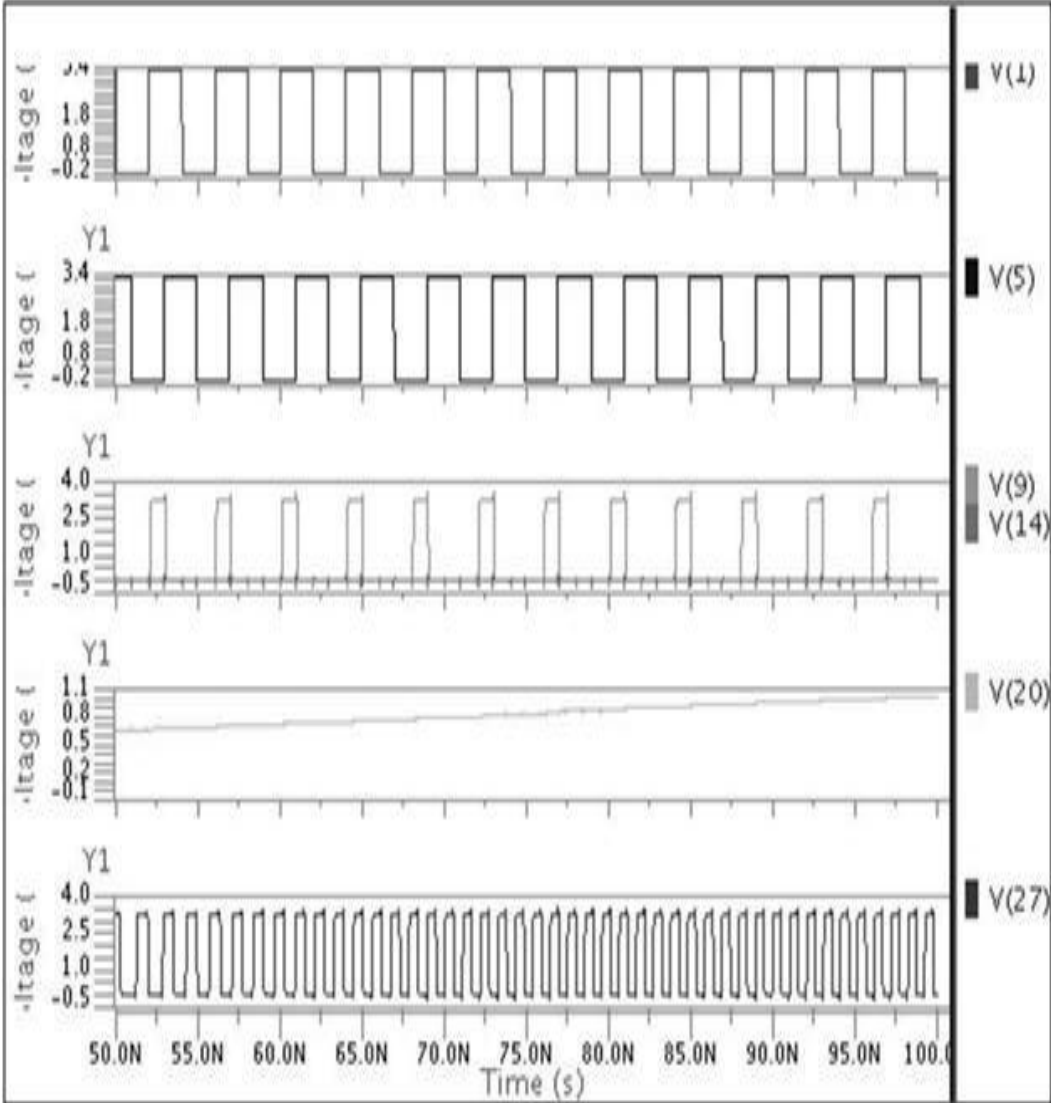
* PLL output
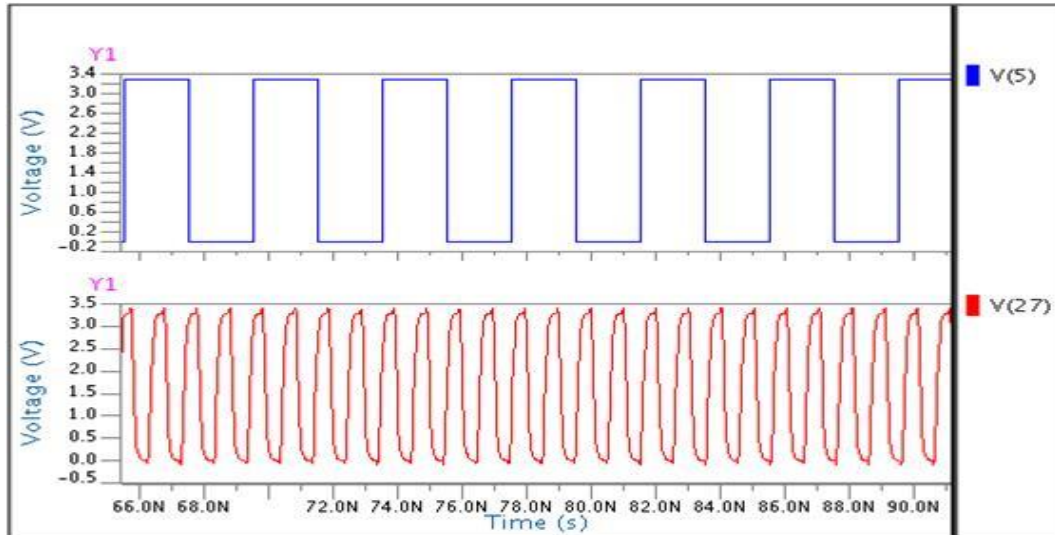
Figure 3.14: PLL output

Phase lock loop with input frequency 250 MHz and the system frequency 1GHz. Input frequency is the input to the Phase frequency detector which is the crystal frequency in the case of microprocessor and the system frequency is the output of Voltage control oscillator , which is the input frequency for the overall system. With the use of this PLL both the purposes are solved - system can work on higher frequency compare to the crystal frequency and in synchronization with input frequency.

Table 3.5: Experimental results of System's operating range

Input Frequency	System Frequency	Lock Time
500MHz	$994.95MHz$	$75ns$
250MHz	$998.57MHz$	$55ns$

* Pre simulation waveform of each block of PLL
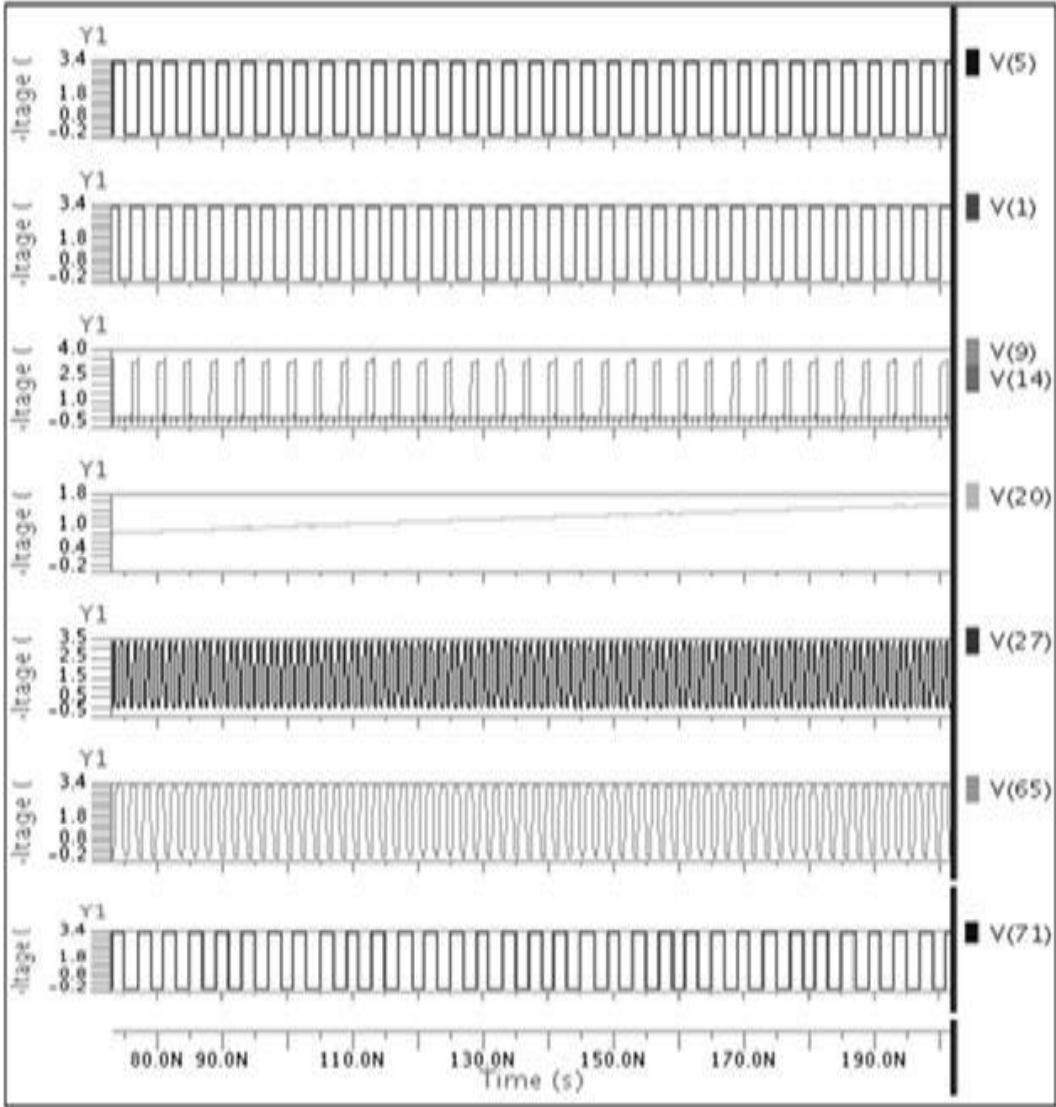
Figure 3.15: PLL output

3.2 Post-Simulation Results with Layout

Pre-layout Simulation is carried out using ELDO Spice in TSMC 0.35 μ m standard digital CMOS process Technology.The LAY-OUT is prepared with the use of IC STATION using MENTOR GRAPHICS and results are depicted in following Figures. Lay - out of Phase Lock Loop is prepared with Phase Frequency Detector , Charge Pump , Loop Filter , Voltage Control Oscillator and divide by N Network.With input frequency 250 MHz and System Frequency 1 GHz.Total number of MOSFET transistors are used in this Phase Lock Loop is 115 MOSFET transistors.

Figure 3.16: LAY-OUT OF PLL WITH 115 MOS-TRANSISTERS having gate length .35um

Chapter 4

Conclusion and Future Scope

4.1 Conclusion

In this project, phase lock loop has been characterized and simulated for the particular application of clock generation. The phase lock loop is designed in TSMC 0.18 μ m standard digital CMOS process.The post simulation (layout)of the same work is done in TSMC 0.35 μ m standard digital CMOS process.

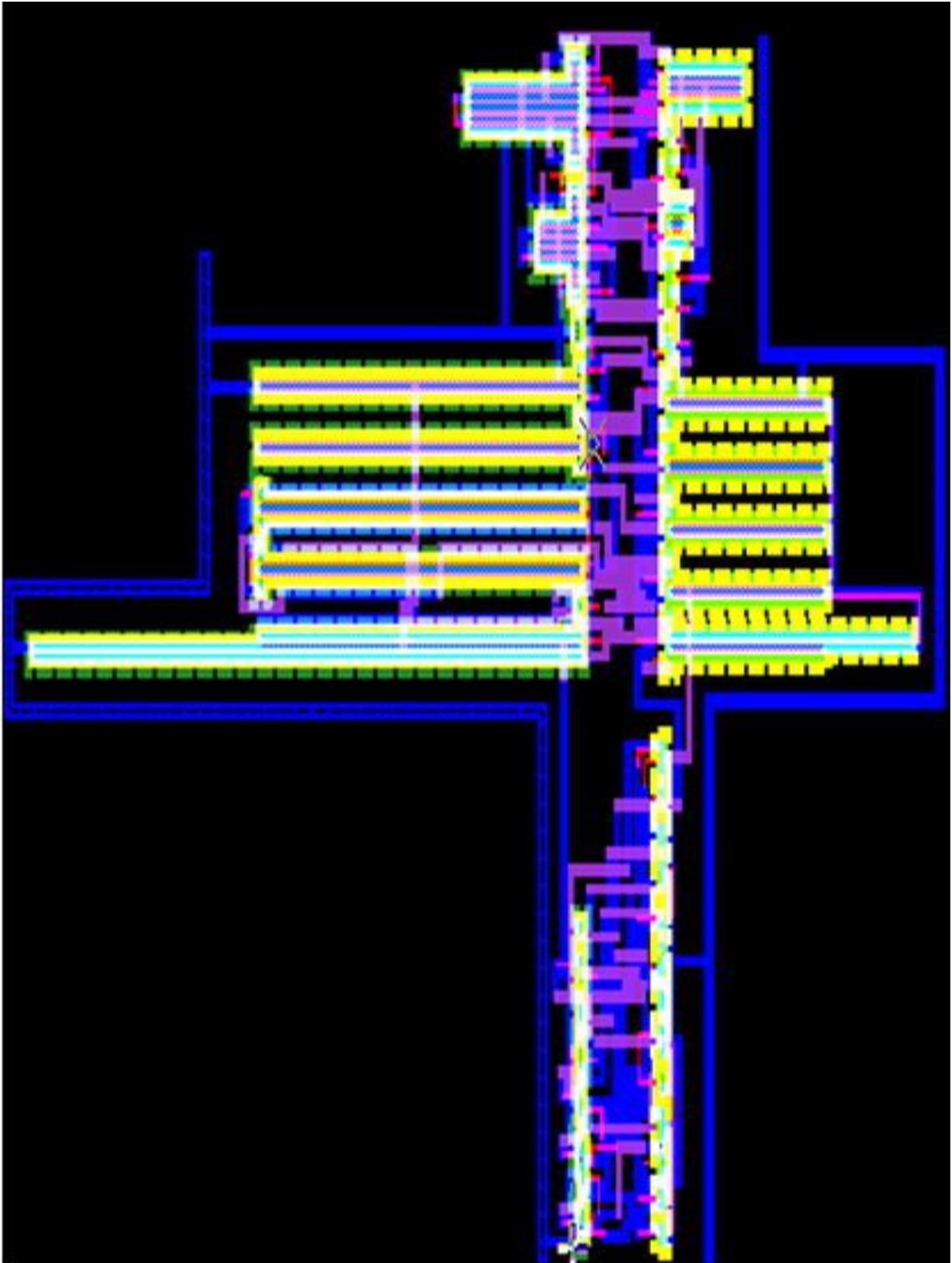The phase lock loop is characterized in terms of the jitter, supply voltage, frequency range, power dissipation and area. The simulation results allow the circuit designer to fully explore the tradeoffs in PLL design,such as frequency range of the LPF and minimum ripple on VCNT .The jitter is proven to be inversely proportional to the power consumption.

The main objective of this project,to design a PLL with low jitter and low power consumption for clock generation is full filled with the current methodologies like modified circuits of PFD, charge pump, loop filter, VCO. With the use of high speed PFD , charge pump , second order loop filter , current starved VCO and divide by 4 network with JK Flip Flop minimums of jitter and very low power dissipation is achieved at low voltage supply.

From simulation results , this new design for clock generation exhibits low jitter and

43

low power dissipation compared to conventional phase lock loop.

4.2 Future Scope

All the analog circuits can be replaced with digital circuits in Traditional Phase Lock Loop. In this project the design is proposed only for clock generation application , but can be extend for clock recovery ,clock multiplication and many more applications. This project has prepared a platform for researchers in the area of low power and low jitter PLL for clock generator. The research can start with any of the frequency and further explore the possibilities of reduction in power and reduction in jitter also. With consideration of other parameters like area, leakage current, phase noise.

Appendix A

TSMC 0.35 μm Model File

Temperature parameters=Default

    temp mod .LIB NOM

    .MODEL NOTCHEDROW C

    .MODEL HR R

    .MODEL N NMOS (LEVEL = 53

    +VERSION = 3.1 TNOM = 27 TOX = 7.8E-9

    +XJ = 1E-7 NCH = 2.2E17 VTH0 = 0.5490813

    +K1 = 0.5749179 K2 = 0.0163016 K3 = 86.4438467

    +K3B = -2.4838433 W0 = 2.749916E-5 NLX = 1.416066E-7

    +DVT0W = 0 DVT1W = 0 DVT2W = 0

    +DVT0 = 6.0353135 DVT1 = 1 DVT2 = -0.1328729

    +U0 = 421.3862314 UA = -1.41643E-10 UB = 1.752303E-18

    +UC = 3.989584E-11 VSAT = 1.583891E5 A0 = 1.2236736

    +AGS = 0.1918056 B0 = 1.038291E-6 B1 = 5E-6

    +KETA = 5.546028E-3 A1 = 0 A2 = 0.4476846

    +RDSW = 764.4088626 PRWG = 0.0377705 PRWB = -0.1206337

    +WR = 1 WINT = 1.518873E-7 LINT = 2.97436E-9

    +XL = -5E-8 XW = 1.5E-7 DWG = -4.754209E-9

    +DWB = 7.013949E-9 VOFF = -0.0888645 NFACTOR = 1.2729614

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.6947057 ETAB = -6.98415E-3

+DSUB = 0.8431979 PCLM = 1.3930628 PDIBLC1 = 1.950934E-3

+PDIBLC2 = 4.57703E-3 PDIBLCB = -1E-3 DROUT = 0.0991119

+PSCBE1 = 6.908691E8 PSCBE2 = 4.912459E-4 PVAG = 0

+DELTA = 0.01 RSH = 3.2 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 2.91E-10 CGSO = 2.91E-10 CGBO = 1E-12

+CJ = 1.003925E-3 PB = 0.8 MJ = 0.3422887

+CJSW = 3.505428E-10 PBSW = 0.8 MJSW = 0.1352212

+CJSWG = 1.82E-10 PBSWG = 0.8 MJSWG = 0.1352212

+CF = 0 PVTH0 = -0.0153579 PRDSW = -73.1424529

+PK2 = 1.780077E-3 WKETA = -5.618765E-3 LKETA = -2.160521E-3)

.MODEL P PMOS (LEVEL = 53

+VERSION = 3.1 TNOM = 27 TOX = 7.8E-9

+XJ = 1E-7 NCH = 8.52E16 VTH0 = -0.6807607

+K1 = 0.4403339 K2 = -0.0138626 K3 = 54.9133679

+K3B = -5 W0 = 5.301139E-6 NLX = 2.393615E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 1.3829615 DVT1 = 0.5424266 DVT2 = -0.0265749

+U0 = 155.5194682 UA = 1E-10 UB = 1.979139E-18

+UC = -1.38347E-11 VSAT = 1.789066E5 A0 = 1.103255

+AGS = 0.3728533 B0 = 2.551996E-6 B1 = 5E-6

+KETA = -7.333027E-3 A1 = 5.697551E-4 A2 = 0.3

+RDSW = 3.951913E3 PRWG = -0.1527603 PRWB = 0.0444598

+WR = 1 WINT = 1.542662E-7 LINT = 0

+XL = -5E-8 XW = 1.5E-7 DWG = -1.456452E-8

+DWB = 1.043713E-8 VOFF = -0.1265542 NFACTOR = 2

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 1.751433E-3 ETAB = 1.401174E-4

+DSUB = 0.0102926 PCLM = 3.4183459 PDIBLC1 = 0.0568076

+PDIBLC2 = 2.128314E-3 PDIBLCB = -1E-3 DROUT = 0.3276874

+PSCBE1 = 8E10 PSCBE2 = 5.14442E-10 PVAG = 1.3183679

+DELTA = 0.01 RSH = 2.6 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 2.49E-10 CGSO = 2.49E-10 CGBO = 1E-12

+CJ = 1.433541E-3 PB = 0.99 MJ = 0.5527511

+CJSW = 4.291576E-10 PBSW = 0.99 MJSW = 0.3523334

+CJSWG = 4.42E-11 PBSWG = 0.99 MJSWG = 0.3523334

+CF = 0 PVTH0 = 8.946877E-3 PRDSW = -35.1190446

+PK2 = 1.580013E-3 WKETA = 3.20553E-3 LKETA = -1.413928E-4)

temp mod

.ENDL

.END

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[1] Kruti P. Thakore and N. M. Devashrayee. High speed phase frequency detector with charge pump and loop filter for low jitter and loe power pll. International Journal of Electronics and Communication Technology (IJECT), vol 2 , ISSUE II, April, 2011.

[2] Kruti P. Thakore and N. M. Devashrayee. Low power and low jitter pll for clock generator. International Conferance on Current Trends in Technology, NUiCONE 2010, December, 2010.

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[4] Kruti P. Thakore and N. M. Devashrayee. Low power low jitter phase frequency detector for phase lock loop. International Journal of Engineering Science and Technology (IJEST) ISSN : 0975-5462 , VOL 3 ISSUE III, June, 2011.