DESIGN AND DEVELOPMENT OF SMPS WITH SYNCHRONOUS RECTIFICATION TECHNIQUE

Major Project Report

Submitted in Partial Fulfillment of the Requirements for the Degree of

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Electrical Engineering

(Power Electronics, Machines & Drives)

By

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CERTIFICATE

This is to certify that the Major Project Report entitled **"Design and Development of SMPS with Synchronous Rectification technique"** submitted by **Mr.Krunalsinh H. Dattesh (09MEE018)**, towards the partial fulfillment of the requirements for the award of degree in **Master of Technology (Electrical Engineering)** in the field of **Power Electronics, Machines & Drives** of Nirma University is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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Abstract

In SMPS there are different topologies like buck converter boost converter, flyback converter, push pull converter, half bridge converter, full bridge converter commonly used. SMPS works on high operating frequency which gives efficient output. The main reason which makes the SMPS most reliable power supply is that it is a compact size device. Using ferrite core for transformer we can reduce the size further making it useful for robotics and highly sophisticated applications. The drawback is production of electromagnetic interference and poor regulation. Also for simple circuit the power losses are more. In rectification side schottky diodes are used. The major factor, limiting the efficiency is the power loss in the schottky diode rectification. In most of topologies the synchronous rectification should never be allowed to turn on simultaneously, so short circuit condition can be created. These entire problems overcome by synchronous rectifier using MOSFETs. MOSFET is used for switching purpose which replace the schottky diode because of the better control can be achieved and so conduction losses can be reduced. In this project the technique called Synchronous rectification is used having the advantages of high performance, high power converters including better efficiency, low power dissipation, better thermal performance, good quality, improved manufacturing yields through automated assembly processes (higher reliability). This is achieved by two different control methods i.e. Voltage mode control and Current mode control.Topology is selected depending on the ratings of proposed load. In this project Half- bridge topology is best suited for the 25 V dc, 250 Watt.

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Nomenclature

A_c ..... Core cross section area
A_p ..... Area Product
A_w ..... Window are
B_m ..... Flux density
D_{max} ..... duty cycle
f_s ..... Switching frequency
I_1 ..... Primary side current (Amperes)
I_2 ..... Secondary side current (Amperes)
I_L ..... Inductor current
I_m ..... Magnetizing current
I_{load} ..... Load current
j ..... current density
K_w ..... Window utilization factor
l_e ..... Mean length per turns
L_m ..... Magnetizing inductance
l_m ..... Mean magnetic length
$N_(P)$ ..... Primary winding
$N_(S)$ ..... Secondary winding
P_o ..... Output Power
Q ..... Efficiency of the transformer
SR ..... Synchronous Rectifier
T_S ..... Switching Time Period (seconds)
T_{ON} ..... on time
$T_(OFF)$ ..... off time
V_1 ..... Primary side voltage (Volt)
V_2 ..... Secondary side voltage (Volt)
V_{IN} ..... Input voltage
V_{OUT} ..... Output voltage
V_C ..... Transformer reset voltage
V_{BD} ..... Forward-voltage drops of the body diodes
V_{ref} ..... Reference voltage
V_{rl} ..... Voltage drop due to the winding resistance of the inductor and transformer
V_d ..... Voltage drop in diodes
V_{pp} ..... Peak ripple voltage

Abbreviations

CMC ..... Current mode control
EMI ..... Electro-magnetic interference
PSU ..... Power supply unit
SMPS ..... Switched mode power supply
VMC ..... Voltage mode control
ZVS ..... Zero-Voltage switching
ZCS ..... Zero-current switching

Contents

Chapter 1

INTRODUCTION

A switched-mode power supply is a power supply unit (PSU) that converts the voltage and current characteristics from one form to another incorporating a switching regulator in order to be highly efficient. SMPS transfers power from a source like a battery or the electrical power grid to the load (e.g., a personal computer). The function of the converter is usually to provide a regulated output voltage usually at a different level from the input voltage.

In linear power supply we can not get close loop control that is the major drawback and power loss is high because of the transistor. In order to obtain almost negligible ripple voltage in the dc output, physical size of filter circuits required is quite large. This makes the dc power supply inefficient, bulky and weighty. All these problems are overcome by the SMPS.

The switching mode power supply (SMPS) operates at a high frequency and is of small size and weight, as the filtering inductor and capacitor are reduced and power density is increased. There are several types of isolated dc-dc converter; the commonly used converters are buck converter, boost converter, flyback converter, push-pull converter, half-bridge converter and full bridge converter. There are two feedback control methods that are widely used in SMPS; one is the voltage mode control (VMC) that senses only the output voltage, V_{out} and another is current mode control (CMC) that senses both the V_{out} and the filter inductor current as the feedback signals.

1.1 Application of SMPS

- Power supply cum Battery charger for communications.
- Power adapter.
- Computer power supplies.
- Medical Instruments
- Robotics applications.
- Military applications.
- Satellites and Space Craft applications.
- Home appliances

1.2 Comparison of SMPS and Linear power supply

Advantages of SMPS

- SMPS is of smaller size , lighter in weight and possesses higher efficiency because of its high-frequency operation.
- SMPS is less sensitive to input voltage variations.
- Feedback control is possible in SMPS.
- Power loss is reduced.

Disadvantages of SMPS

- SMPS has higher output ripple and its regulation is worse.
- SMPS is a source of both electromagnetic and radio interference due to high frequency switching.
- Control of radio frequency noise requires the use of filters on both input and output of SMPS.

Advantages of linear power supply

- Easy to design and fairly inexpensive to manufacture.
- Noise free operation.
- Control circuit is much easier than SMPS.
- Since there is no high frequency switching so electro-magnetic interference (EMI) is practically absent in linear power supply.

Disadvantages of linear power supply

- Power loss is high.
- Linear power supply is heavy and bulky because of the low frequency transformer and output voltage filter circuit.
- Feedback control is not possible.

1.3 Objectiv of Project

In this project synchronous Rectifier is used as a technique to reduce the conduction losses of switches. This is achieve by replacing schottky diodes by MOSFETs which are controlled and synchronized with the inverter side MOSFETs. The synchronization of Rectifier and inverter side MOSFETs is done using - PWM controller with Integrated Half-bridge and SyncFET driver.

1.4 Basic block diagram

- Rectifier and filter This block contains diode rectifier and DC filters to get almost a constant DC.
- High frequency switch This is an inverter section in which the switched operate at high frequency.

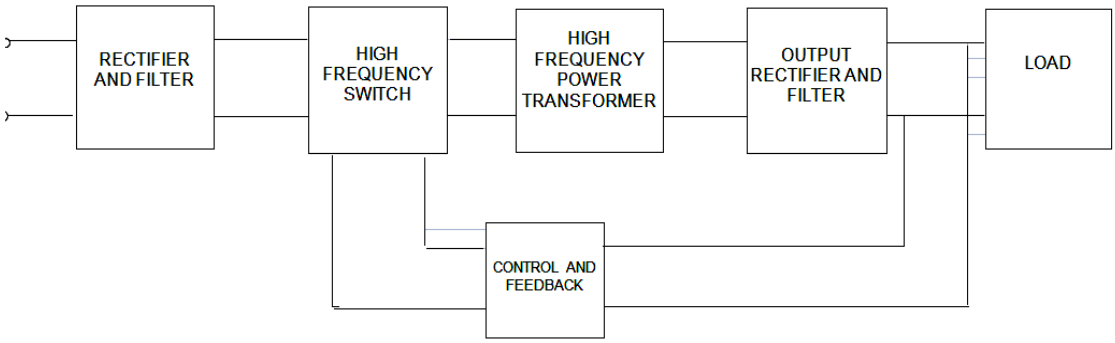

Figure 1.1: Block Diagram of SMPS

- High frequency power transformer The high frequency ac is stepped up or stepped down depending on the ratings. Ferrite core transformer is generally used to reduce the iron losses.
- Output rectifier and filter The AC is then again rectified and filtered to get the required output DC voltage.
- Load The load connected may be any circuit which is supplied by the SMPS.
- Control and feedback The feedback from the load is taken to make the output controllable and constant.

1.5 Thesis Organization

Chapter1 is the introduction to the basic of the SMPS, advantages and disadvantages of the SMPS with linear power supply, main objectives of the project and basic block diagram of the SMPS.

Chapter2 shows various paper referred to understand the basics of the topic and further development in this area.

Chapter3 shows the topology selection and introduction to the selected topology Half-Bridge.

Chapter4 gives the introduction to the synchronous rectification,benefits, different technique i)self-driven of SR and ii) Control-driven and basic controlling methods of SMPS.

Chapter5 shows the hardware design of the power circuit which includes the design of power transformer, design of input side capacitor, design of control circuit. **Chapter6** shows the simulation of the control circuit, power circuit and, its hardware implementation and testing at the different voltages. Fabrication of half-bridge inverter and synchronous rectifier and various results at different voltages.

Chapter 2

LITERATURE SURVEY

[1] Jaroslave Dudrik, Juraj Oetter, "High Frequency Soft Switching DC-DC Converter for Voltage and Current DC Power Sources", Acta Polytechnic Hungering, Vol.4, No.2, pp. 29-46, 2007.

Summary: This paper presets soft switching PWM DC-DC converters using power MOSFETs and IGBTs. This paper totally focused on the full-bridge converters suitable for high power applications. There are three types of soft switching techniques (1) ZVS PWM converters (2)ZCS PWM converters (3) ZVS ZCS PWM converters. The ZVS converter exhibits low primary-side switching loss and generated EMI. By using snubber capacitors in parallel to transistors, the turn-off losses are remarkably decreased. In all three techniques use phase-shift control at constant switching frequency. The switches must have reverse-voltage blocking capacity. An important advantage of the circuit is that the rectifier diodes do not suffer from reverse recovery problem since they commutate with zero-voltage switching. Zero-voltage Zero-current switching PWM converters is very attractive for high voltage, high power applications where IGBTs are predominantly used as a power switches.Because of phase-shifted PWM control the circulating current flows through a transformer and switching devices during freewheeling intervals ,due to this RMS current stresses of the transformer and switching devices are still high compared with that of the conventional hard-switching. To decrease the circulating current to zero and to achieve zero-current switching various snubber connected mostly at secondary side of trans-

former are applied.

[2] Marcelo Bruno and Jose Luiz f. Vieira, "A High-Performance ZVS Full-Bridge DC-DC 0-50-V/0-10-A Power Supply with Phase-Shift Control", IEEE Transactions on Power Electronics,Vol.14,No.3,pp. 495-505,1999.

Summary: This paper present the modified version of the zero-voltage switching full-bridge phase-shift dc-dc converter, which incorporates commutation auxiliary inductors to provide ZVS for the entire load range. By using a commutation aid circuit, the ringing and the overshoot across the output rectifier diodes are reduced. In control stage two control loops operating in cascade mode, inner loop regulates the output current at a reference value and the external voltage loop keeps a constant output voltage at a specified value, independently of load and input-voltage changes.

[3] Babak Abdi, Jafar Milimonfared, Ahmad Mahin Fallah, "A High-performance 1.3 Kw SMPS with Single Switch Forward Topology".

Summary: This paper present the losses due to the transformer leakage inductance and the winding resistance on smps. Because of the leakage inductance it increase the power loss across switch ,noise level, Electro magnetic interference and cost. It decrease the efficiency of the smps. The modified sandwich winding or inter laminate windings reduces this problem.

[4] Jegandren.J, Gobbi.R, Hussain s.Athab "An Investigation on control Strategies for Fast Transient Response of SMPS", Proceeding of the 2008 IEEE Conference on Innovative Technologies in Intelligent Systems and Industrial Applications Multimedia University, Cyberjays, Malaysia, 12-13 July 2008, pp.110-115

Summary: This paper present the voltage control method and peak current control method of the SMPS. The main purpose of control methods is to adjust the duty cycle of the PWM to regulate the output voltage. Peak current mode control helps the SMPS faster transient response compare to the voltage mode control. Voltage mode control is also called as a single loop control method because only the output voltage, Vout is sensed and used in the feedback control circuit. Current mode control method uses two feedback signals the are the output voltage and the filter inductor current. The voltage injection switching inducter method is investigated and it provides better

transient response to peak current mode control method.

[5] Wojciech A. Tabisz, Fred C. Lee and Dan Y. Chen "A mosfet resonant synchronous rectifier for high-frequency dc to dc converters", IEE.

Summary: In this paper a resonant synchronous rectifier which combines the fast switching of Schottky diodes with the low conduction drop of MOSFET devices is presented. In the resonant synchronous rectifier the MOSFETs are driven in a resonant fashion by the power circuit. As a result, the gate drivers are eliminated, thus reducing the circuit complexity. In addition, the energy stored in the parasitic capacitances is partially recovered and switching losses are reduced. The MOSFETs are on during most of the switching period thus reducing the conduction losses. However, the instantaneous switching of the load current is performed by the Schottky diodes with the MOSFET devices off. In this manner, the low conduction loss of MOSFET synchronous rectifiers is combined with the fast switching of Schottky diodes. If parasitic gate resistance is reduced in MOSFET designs, the resonant synchronous rectifier technique could be applied at 10 MHz with significant improvement of efficiency over PWM synchronous rectifier or Schottky diode rectifiers.

[6] XIE Xuefei, Joe C. P. LIU, Franki N. K. POON, Bryan M. H. PONG, "Two Methods to Drive Synchronous Rectifiers During Dead Time in Forward Topologies", pp. 993 - 999.

Summary: Two SR driven methods, gate charge retention driven and energy recovery current driven are proposed in this paper both of them effectively solve the drive problem of SR during dead time in forward topology. The first method is a simple and low-cost voltage driven SR. Only a few small signal power components are added to perform gate charge retention function. The second method is a current driven SR with energy recovery. It recovers the current sensing energy so that it can be applied in high frequency power conversion. Furthermore, drive voltage of SR is constant and programmable during line fluctuation. This eases the optimization of SR design.

[7] Ehsan Adib, "Zero-Voltage-Transition PWM Converters With Synchronous Rectifier", IEEE TRANSACTIONS ON POWER ELECTRONICS, Vol. 25, NO. 1, 2010

Summary: This paper present zero-voltage-transition (ZVT) pulse width-modulated buck converter with synchronous rectifier (SR). The SR decreases the conduction losses but main problem is the reverse recovery time of SR body diode which increases the switching losses and electromagnetic interferences (EMIs). In ZVT technique a capacitor is placed in parallel with the main switch to provide soft switching condition for switch turn off. Soft switching condition for switch turn on is achieved by an auxiliary switch, which discharge the snubber capacitor across the main switch. Therefore, when the auxiliary switch is turned on in ZVT converters, it first provides the converter inductor current and the converter main diode turns off. Then, the snubber capacitor of main switch is discharged in a resonance fashion. Thus, ZVT techniques create a time gap between the conduction time of the main switch and diode. Therefore, ZVT technique is a proper solution for reverse recovery problem of converter main diode. Consequently, by applying ZVT techniques to regular converters with SR, the losses related to the reverse recovery time of SR body diode can be reduced significantly. Applying SR to ZVT converter reduces the conduction losses and also results in wide soft switching rang and improve efficiency.

[8] Hong Mao, Osama Abdel Rahman, "Zero-Voltage-Switching DC-DC Converters With Synchronous Rectifiers", IEEE TRANSACTIONS ON POWER ELECTRONICS, Vol. 23, NO. 1,pp. 369-378, 2008.

Summary: In this paper present Active resonant tank (ART) cells to achieve zero-voltage-switching (ZVS) and eliminate body diode conduction in dc-dc converters with synchronous rectifiers (SRs). In low-output-voltage dc-dc converters, SRs are widely utilized to reduce rectifier conduction loss and improve converter efficiency. However, during switches' transition, SRs' parasitic body diodes unavoidably carry load current, which decreases conversion efficiency because voltage drop across body diodes is much higher than that across SRs. Moreover, body diodes' reverse recovery leads to increased switching losses and electromagnetic interference. With the proposed cells of an ART, the body diode conduction of the SR is eliminated during the switching transition from a SR to an active switch, and thus body diode reverse-recovery- related switching and ringing losses are saved. An ART cell consists of a

resonant tank and an auxiliary switch. A resonant tank cell is charged in a resonant manner and energy is stored in the capacitor of the tank. Prior to a switching transition from a SR to an active switch, the energy stored in the tank capacitor is released and converted to inductor current, which forces the SR current changes direction to avoid conduction of the body diode and related reverse recovery when the SR turns off. Moreover, at the help of energy released from the ART, the active switch's junction capacitance is discharged, which allows the active switch turns on at ZVS. Since energy commutation occurs only during switching transition, conduction loss in the ART cell is limited. Moreover, the auxiliary switch turns off at ZVS and the SR operates at ZVS. The concept of ART cells is generally introduced and detailed analysis is presented based on a synchronous buck converter. High efficiency at high switching frequency is achieved due to the reduced switching loss and reverse-recovery loss compared to conventional hard-switching buck converter.

[9] Daocheng Huang, Dianbo Fu, Fred. C. Lee, "High Switching Frequency, High Efficiency CLL Resonant Converter with Synchronous Rectifier", IEEE, pp. 804-809, 2009.

Summary: This paper present a CLL resonant tank (CLL) as an attractive option in the front-end application as DC/DC converter. This topology can achieve zero-voltage switching (ZVS) from zero load to full load, low turn off loss, ZCS for output rectifier, and easy to realize secondary rectification. There are two resonant frequency ,One is series resonant frequency, and other one parallel resonant frequency. The parallel resonant frequency is introduced by L1 and C1. and the series resonant one by C1,L1 and L2. If the switching frequency is lower than the parallel resonant frequency, ZCS is achieved. If the switching frequency is higher than the parallel resonant frequency, ZVS is reached. A novel design methodology of CLL resonant converter is proposed based on the trade-off among efficiency, hold up time and ZVS requirement. A transformer structure for better performance in high frequency application is proposed. And current type synchronous rectifier (SR) drive scheme is used in this topology.

[10] Mingci Geng, Quanyuan Feng, "Design of A Synchronous Rectifier Controller

for Limiting Reverse Current", IEEE, 2009.

Summary: This paper present a novel current limiting circuit and the relative mechanism are both designed for the controlling loops of a peak-current-mode synchronous buck converter. Since MOSFETs are bidirectional switches, when MOSFETs are used to replace conventional diodes in SR, the reverse current flow will occur under specific conditions, such as start-up, light load and no load. To improve that, the converters have to limit the reverse currents to reduce its conduction loss. In this paper, a simple circuit, which utilizes the CB amplifier to detect the reverse current, is designed. Simulation results verify that this approach is able to improve SR buck converter light load and middle-load efficiency. And transient response also has a better result.

[11] N.Z. Yahaya, K.M. Begam and M. Awan, "Investigation of High Frequency Effects on Soft-Switched Synchronous Rectifier Buck Converter", Symposium on industrial Electronics and Application, kuala Lumpur, Malaysia, pp. 525-529, 2009.

Summary: This paper presents the effects of switching frequency where reduction in losses is significant to the converter's performance. In this paper the proposed zero-voltage-switching synchronous buck converter circuit is compared with the conventional synchronous buck converter by applying different frequency. It can be observed that in conventional synchronous buck converter that there are several non-zero voltage switching points occurred during turn-on and off transitions of the MOSFETs and also exists a floating drain voltage of high side switch, indicating of high switching loss. In proposed new synchronous buck converter circuit, there are additional LC components added in parallel with both high side and low side switch. The other component, capacitor, Cx connected in series with low side switch is used to reduce the floating drain voltage of high side switch. The body diode conduction loss has also been reduced significantly with shorter reverse voltage time. The additional LC components may introduce drawbacks to the system which yield a more costly and bulky converter. By using an accurate controller and third generation predictive gate driver scheme, the losses can be further reduced.

[12] Kohji Kuwabara, Hirofumi Matsuo, Kazuo Kobayash, and Katsuhiko Nishimura, "A Novel Synchronous Rectification Circuit Using a Saturable Current Transformer"

IEE, pp. 143-148, 2002.

Summary: This paper presents a novel synchronous rectification circuit using a saturable current transformer and as design oriented analysis is introduced. The proposed synchronous rectification circuit is applied to the forward DC-DC converter with the low output voltage there often exists a deteriorative problem caused by an insufficient driving voltage for the MOS-FET. Also, an inverse current through the MOS-FET and extraordinary phenomena occur when the multiple converters with synchronous rectifier are connected in parallel to increase the output power and system reliability. To solve the above problems, a synchronous rectification circuit with a current transformer CT is proposed.

In this circuit, a current through the primary winding of CT induces a current through the secondary winding and this current drives the FET. Therefore, the Circuit can operate without a requirement for the extra driving current. When a reverse current is applied to the Circuit, the gate to source is reverse biased and the FET is turned off. Thus, the circuit can operate as if it were a two-terminal rectification device. This circuit may be suitable for a synchronous rectification circuit, but there are following two problems. One problem is increase on-time duration of a body diode in MOS-FET and another is that a voltage across the primary Winding of CT is made high. Firstly the current flows through the body diode in MOS-FET when the circuit is turned on. The current which flows through the body diode, is fed to the secondary winding of CT and the gate current flows to turn on the FET. The on-time &on of the body diode must be decreased because a voltage across a body diode whose resistance is much larger that of an on-resistance of FET. If a secondary to primary turn ratio of CT is small, a gate current is increased, and FET turn on quickly Moreover, when FET continues to on, there appears a voltage across the primary winding of CT, which is proportional to the gate voltage. To reduce this voltage, the secondary to primary turn ratio must be large, but this method does not make short appropriately the on-time duration of the body diode. To improve the above contrary problems, the novel technique using a third winding is introduced, but the circuit configuration is complicated. The turn on time of MOS-FET is proportional to the output current

as FET is driven by the feedback current in the current transformer. Therefore, the turn on is faster when the output current is larger. As this synchronous rectification circuit operates as a rectifier of two-terminal device, it is also possible to apply to any rectification circuits in the buck-boost converter, half-bridge converter and so forth.

Chapter 3

SMPS TOPOLOGY SELECTION

3.1 Introduction to SMPS topologies

- Buck converter
- Boost converter
- Forward converter
- Fly-back converter
- Push-pull converter
- Half bridge converter
- Full bridge converter

INPUT VOLTAGE	OUTPUT POWER	PREFERRED TOPOLOGY
Universal(90-264) V_{AC}	P_O < 150 W, Load current < 10 A	Fly-back, Forward
Universal(90-264) V_{AC}	P_O < 150 W, Load current > 10 A	Forward
Universal(90-264) V_{AC}	150W < P_O < 350W	Two-switch Forward, Half bridge, Push-pull
Universal(90-264) V_{AC}	P_O < 500 W	Half bridge, Push-pull
V_{in} > 350 V_{DC}	P_O < 750 W	Half bridge
V_{in} < 200 V_{DC}	P_O < 500 W	Push-pull
V_{in} > 350 V_{DC}	500 W <P_O <1000W	Full bridge
V_{in} > 350 V_{DC}	1000W < P_O <2000W	ZVT Full bridge
V_{in} > 350 V_{DC}	P_O > 2000W	More than one ZVT Full bridge in parallel, interleaved with more than one ZVT Full bridge

Figure 3.1: SMPS topology selection

3.2 Flow chart for SMPS topology selection

Assumptions:

- Input voltage: 120 to 400 V_{DC} (which is typical for rectified AC line voltage or the output of PFC boost)
- Output voltages <60 V

Note:

- This is just a basic guidance in selecting proper SMPS topology, which is based on the author's personal view. The right topology will be selected depending on specific requirements for the power supply (including cost and time factors) and personal experience of the designer.
- P_o- Overall output power,
- I_o- maximum output current

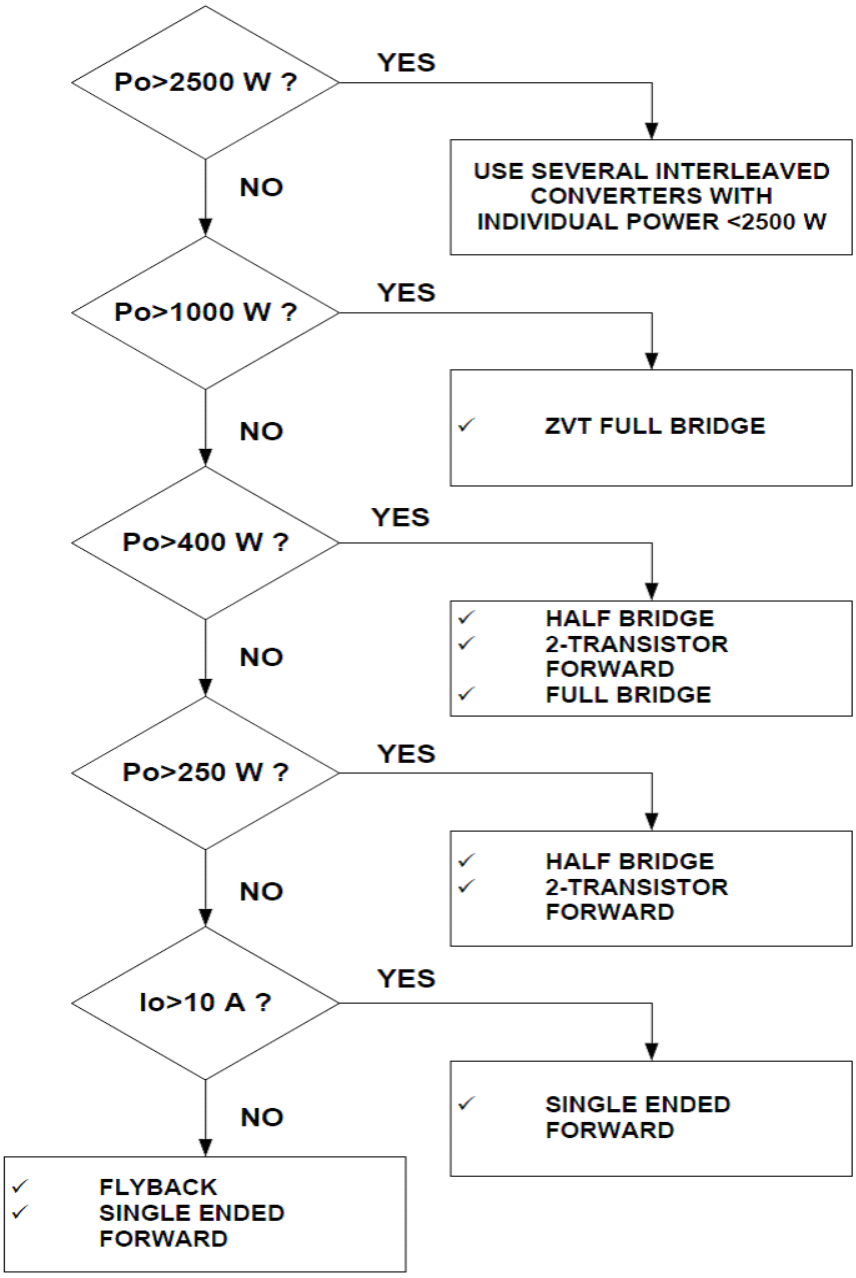

Figure 3.2: Flow chart of SMPS topology selection

3.3 HALF-BRIDGE CONVERTER

The switches Q_1 and Q_2 form one leg of the bridge, with the remaining half being formed by the capacitors $C_3$and C_4. Therefore, it is called a half-bridge converter. The switches Q_1 and Q_2 create pulsating AC voltage at the transformer primary. The transformer is used to step down the pulsating primary voltage, and to provide isolation between the input voltage source V_{IN} and the output voltage. In the steady state of operation, capacitors C_3 and C_4 are charged to equal voltage, which results in the junction of C_3 and C_4 being charged to half the potential of the input voltage. When the switch Q_1 is ON for the period of T_{ON}, the dot end of the primary connects to positive V_{IN}, and the voltage across the capacitor C_4 (V_{C4}) is applied to the transformer primary. This condition results in half of the input voltage being V_{IN}, which is applied to the primary when the switch Q_1 is ON. The diode D_4 becomes reverse-biased, and the diodeD_3 becomes forward-biased, which carry the full inductor current through the secondary winding NS_1.The difference of the primary voltage reflected on the secondary N_{S1} and output voltage V_{OUT} is applied to the output inductor L in the forward direction. Therefore, the inductor current I_L rises linearly from its present value of I_{L1} to I_{L2}. During this T_{ON} period, the reflected secondary current, plus the primary magnetizing current flows through the switch Q_1. As the voltage is applied to the primary in the forward direction during this T_{ON} period, and when the switch Q_1 is ON, the flux density in the core changes from its initial value of B_1 to B_2. At the end of the T_{ON} period, the switch Q_1 turns OFF, and remains off for the rest of the switching period T_S. The switch Q_2 will be turned ON after half of the switching period $T_S/2$ during the TOFF period, both switches are off. When switch Q_1 is turned off, the body diode of the switch Q_2 provides the path for the leakage energy stored in the transformer primary, and the output rectifier diode D_4 becomes forward-biased. As the diode D_4 become forward-biased, it carries half of the inductor current through the transformer secondary N_{S2} and half of the inductor current is carried by the diode D_3 through the transformer secondary N_{S1}. Therefore, the equal and opposite voltage is applied at the transformer secondary,

assuming both secondary windings $N_{S1}$and N_{S2} have an equal number of turns. As a result, the net voltage applied across the secondary during the T_{OFF} period is zero, which keeps the flux density in the transformer core constant to its value of B_2.The output voltage V_{OUT} is applied to the inductor L in the reverse direction when both switches are OFF. Therefore, the inductor current I_L decreases linearly from its initial value of I_{L2} to I_{L1}. The body diodes of switches Q_1 and Q_2 provide the path for the transformer leakage energy. After the time period $T_S/2$ when the switch Q_2 turns ON, the dot end of the primary connects to the negative of V_{IN}, and the voltage across the capacitor C_3 (V_{C3}) is applied to the transformer primary. Therefore, half of the input voltage V_{IN} is applied to the primary when the switch Q_2 is ON in the reverse direction, as shown in Figure 3.3. The value of the magnetic flux density in the core is changed from its initial value of B_2 to B_1. Assuming the number of secondary winding turns of N_{S1} is equal to N_{S2}, and to avoid magnetic saturation in the transformer core, the T_{ON} period of both switches should be the same. After the T_{ON} period, Q_2 turns OFF and remains off for the rest of the period T_S.

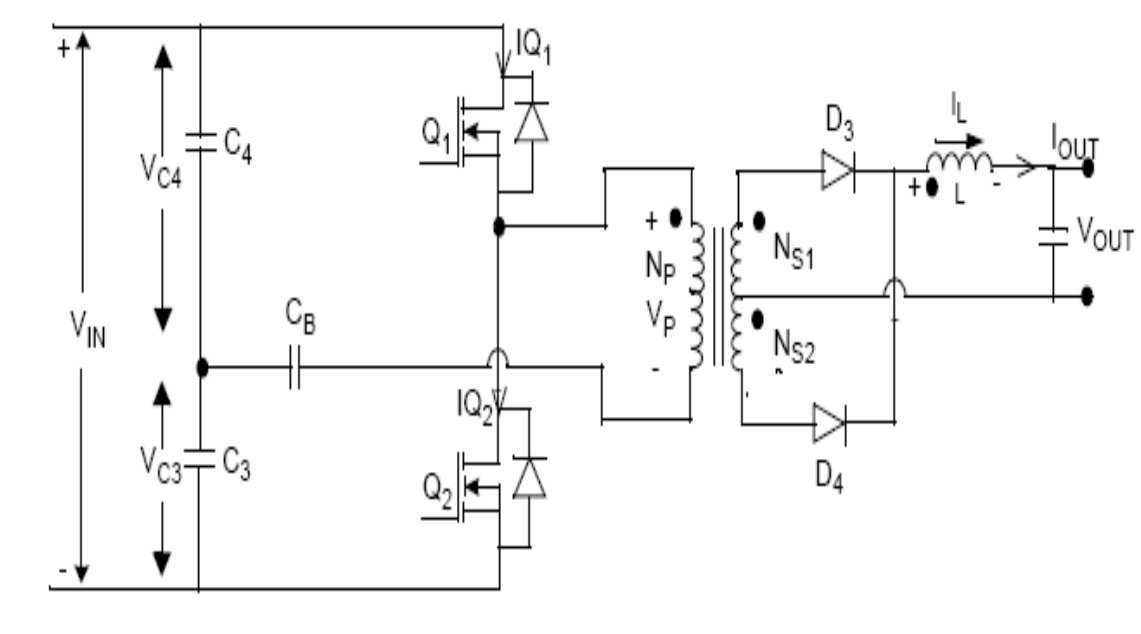

Figure 3.3: Half Bridge converter circuit

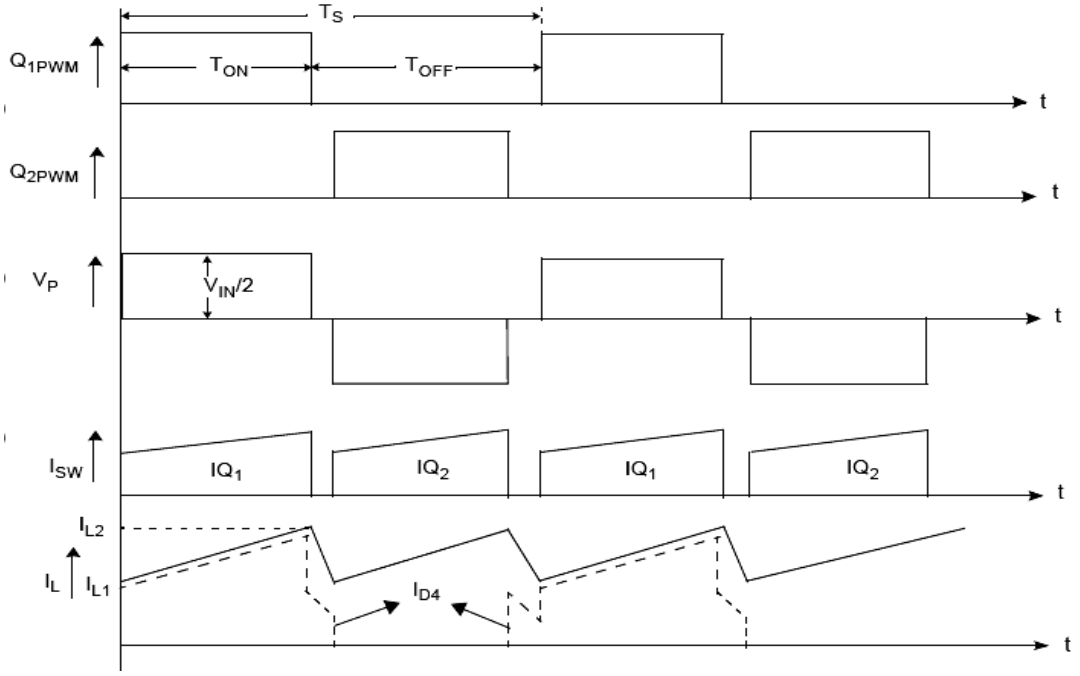

Figure 3.4: Half bridge converter waveforms

Chapter 4

INTRODUCTION TO SYNCHRONOUS RECTIFICATION

The conduction loss of diode rectifier contributes significantly to the overall power loss in a power supply, especially in low output-voltage applications. The rectifier conduction loss is proportional to the product of its forward-voltage drop, V_F, and the forward conduction current, I_F. In Synchronous Rectification the Schottky rectifier diodes are replace by the MOSFETs and the Rectification done between inverter side MOSFETs and rectifier side MOSFETs. The Schottky diode is selected by its forward voltage drop and reverse leakage current characteristics. But as output voltages drop, the diode's forward voltage is more significant which reduces the converter's efficiency. Physical limitations prevent the forward voltage drop of diodes from being reduced below approximately 0.3 V. In contrast, the on resistance, R_{DSON}, of MOSFETs can be lowered, either by increasing the size of the die or by paralleling discrete devices. Consequently, a MOSFET used in place of a diode can have a significantly smaller voltage drop at a given current than the diode. This makes SR attractive, especially in applications sensitive to efficiency, converter size, and thermal performance, such as portable or handheld devices. A synchronous rectifier presents a resistive i-v characteristics, as shown in Fig.4.1 Under certain current level, the forward-voltage drop

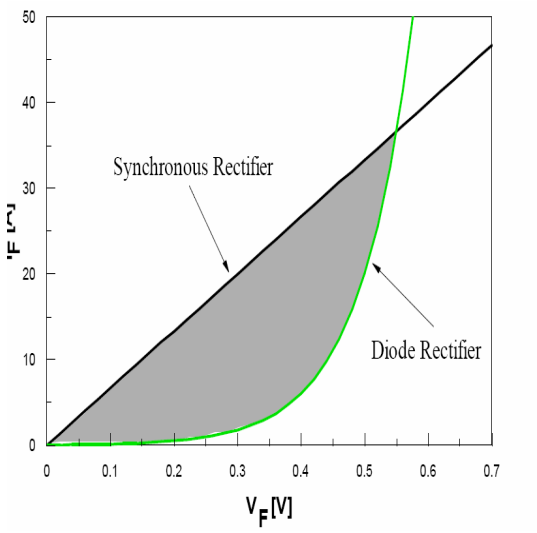

Figure 4.1: I-V characteristics of Synchronous rectifier

of a synchronous rectifier can be lower than that of a diode rectifier, and consequently reduces the rectifier conduction loss.

4.0.1 Benefits of Synchronous Rectification

The advantages of using SR in high-performance, high-power converters include better efficiency, lower power dissipation, better thermal performance, lower profile, increased quality, improved manufacturing yields though automated assembly processes (higher reliability), and inherently optimal current sharing when synchronous FETs are paralleled. A number of MOSFETs can be paralleled to handle higher output currents. Because the effective R_{DSON} in this case is inversely proportional to the number of paralleled devices, conduction losses are reduced.

4.0.2 Synchronous Rectifier Implementations

Based on the method employed in driving SRs, It can be classified into two groups: (1) control-driven and (2) self-driven. In a control-driven SR implementation, the SRs are driven by gate-drive signals derived from the gate-drive of the main switch. In a self-driven SR implementation, the SRs are driven directly with the secondary voltage of the transformer. As a result, the self-driven SR approach is very attractive since it is simple and requires a minimum number of components. However, the performance of self driven SRs depends on the resetting method of the power transformer since the freewheeling synchronous rectifier is driven by the reset voltage. Ideally, it would be desirable that the resetting time be equal to the off-time of the primary switch. Then the output current would freewheel through the SR for the entire off (freewheeling) time.

A. Forward Converter with RCD Clamp and Self-Driven SRs

In this circuit, synchronous rectifiers SR_2 (Q_2 and D_2) and SR_3 (Q_3 and D_3) are cross coupled to these secondary winding of the transformer and are directly driven by the secondary voltage. Since no driver or control circuit is used to provide the gate-drive signals, this implementation of synchronous rectification is the simplest possible. However, its performance is strongly dependent on the method of the transformer core resetting, because the gate-drive signal for synchronous rectifier SR_3 is derived from the reset voltage. As can be seen from the waveform in Fig.4.3(e), once the

transformer reset is completed, the magnetizing current of the transformer, I_{m-}, starts flowing through the body diode of SR_2. The magnitude of this current is given by:

where N is the turns ratio of the transformer, V_C is the transformer reset voltage, L_m is magnetizing inductance of the transformer, and Cs is the total capacitance seen at the drain of the primary switch. This capacitance is the sum of the output capacitance of the primary switch (C_{oss}), winding capacitance of the transformer (C_{tr}), the clamp-diode junction capacitance(C_D), reflected input capacitance of SR_3 (C_{iss} N_{Q3} / 2), and reflected output capacitance of SR2(C_{oss} N_{Q2} / 2).

Also, as can be seen from the waveforms in Fig.4.3(f), after the transformer reset is completed, the difference between load current I_o and magnetizing current I_m -is diverted from transistor Q_3 to the body diode, D_3, of SR_3. Due to relatively high forward-voltage drops of the body diodes of SR_2 and SR_3, the efficiency of synchronous rectification is reduced. The efficiency loss due to the body-diode conduction depends on the duration of the dead time (T_{dead}) and the forward-voltage drops of the body diodes (V_{BD}). This loss can be minimized by connecting Schottky diodes in parallel with SR_2 and/or SR_3 or by minimizing the conduction times of D_2 andD_3. While the conduction time of D_3 can be minimized either by driving Q_3 by an external gate drive signal or by minimizing the dead time by employing a different reset scheme , the conduction time of D_2 can be shortened only by employing a transformer reset scheme that minimizes the dead time, as will be discussed in more detail in the following subsections. However, it should be noted that for load currents much greater than magnetizing current I_{m-}, the efficiency loss occurring during the dead time due to the conduction of D_3 is much greater than that of D_2. Since for properly designed converter $I_{m-}$is usually less than 2 A, the effect of D_2 conduction loss due to I_{m-} on the efficiency is relatively small at output currents exceeding 15 to20 A. The conduction losses of the body diodes of SR_2 and SR_3 are also dependent on the commutation time T_{com} on and T_{com} off shown in Figs.4.3(e) and 4.3(f). In fact, the body diode of SR_2, D_2, conducts only during a brief period immediately after the primary switch is turned off and during the dead time. While the dead time

is solely determined by the transformer reset voltage, the commutation time of D_2 after the turn-off of the primary switch depends on the fall time of the secondary voltage (see Fig.4.3(d)) and the commutation time (T_{com} off) of the output current from diode D_2 to transistor Q_3. Commutation time T_{com} off is dependent on the secondary-side inductance that consists of the leakage inductance of the transformer, the packaging inductance of the SRs, and the secondary-side interconnect inductance. The secondary-side inductance also determines the commutation time(T_{com} on) which is required to commutate current from diode D_3 to transistor Q_2 after the primary switch is turned on. Since for output current $I_o >> I_{m-}$, the conduction loss of body diode D_3 during the dead time is much higher than the correspondingconduction loss of D_2. As a result, the conduction loss of D_2 during commutation time T_{com} off has a much stronger effect on the total conduction loss of SR_2 compared to the effect that the conduction loss of D_3 during commutation time T_{com} on has on the total loss of SR_3. To minimize the commutation times, the total inductance of the secondary side should be minimized. Finally, it should be noted that the conduction of the body diodes of SRs not only increases the conduction loss, but also introduces the power loss due to their reverse recovery. This loss, which appears on the body diode and the transistor of the opposite SR during the diode turn-off, is proportional to the recovered charge Q_{rr} indicated in Figs.4.3(e) and 4.3(f), frequency, and secondary voltage [A20]. Therefore, it is relatively significant at full load and high line. The only method of eliminating this loss is to parallel the Schottky diodes to SR_2 and SR_3.

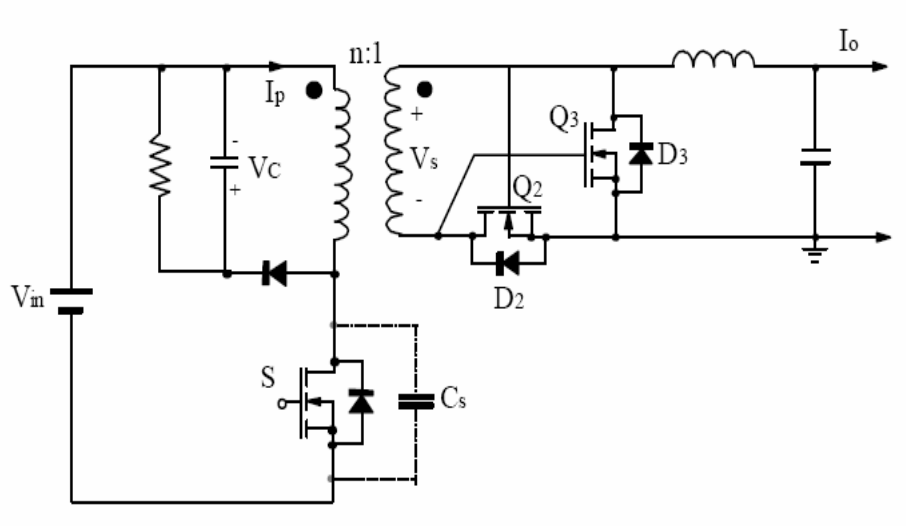

Figure 4.2: Forward converter with self driven SRs

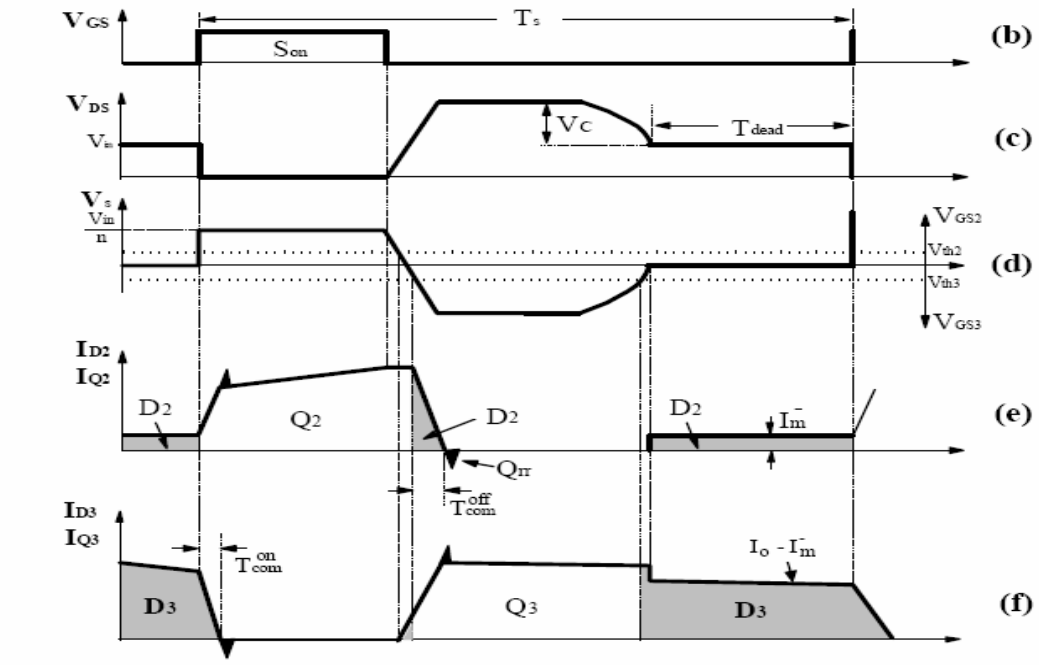

Figure 4.3: Waveforms of forward converter with self driven SRs

B. Forward Converter with Control-Driven SRs

The forward converter with control-driven SRs and its key waveforms are shown in Fig.4.5. In this circuit, transistors Q_2 and Q_3 are driven by gate-drive signals derived from the primary-switch gate drive. As a result, the conduction times of the synchronous rectifiers are independent of the transformer-resetting method, but solely depend on the timing of the gate drive signals. However, as can be seen from Figs.4.5(e) and (f), while driving the SRs from the control circuit results in the maximum conduction time of Q_3, it has no effect on the conduction time of the magnetizing current though diode D_2 during the dead time. Namely, since during the dead time transistor Q_2 is off (gate-drive to Q_2 is low), the conduction of diode D_2 during the dead time with control-driven SRs (see Fig.4.5) is exactly the same as for the self-driven SRs (see Fig.4.3). Ideally, the gate-drive timing of SRs should allow no conduction of the body diodes of the SRs except for the unavoidable conduction of D_2 during the dead time. This is only possible with a very precise gate drive timing where the gate-drive of one SR is applied or terminated at the same instant the gate-drive of the other SR is terminated or applied. In practical applications, this ideally complementary drive is not possible. Accidental, brief overlapping of the gate-drive signals that turn on both SRs simultaneously would short the secondary, causing an increased secondary current, and thus would lower efficiency or, in severe cases, would cause converter failure. To avoid simultaneous conduction of SRs in practical applications, a delay between the gate-drive signals must be introduced. Since during the delay period no gate-drive signal is applied to the SRs, the body diodes of the SRs are conducting. This not only increase conduction loss but also introduces reverse-recovery loss. Therefore, the performance of control-driven SRs is strongly dependent on the timing of the gate drive.

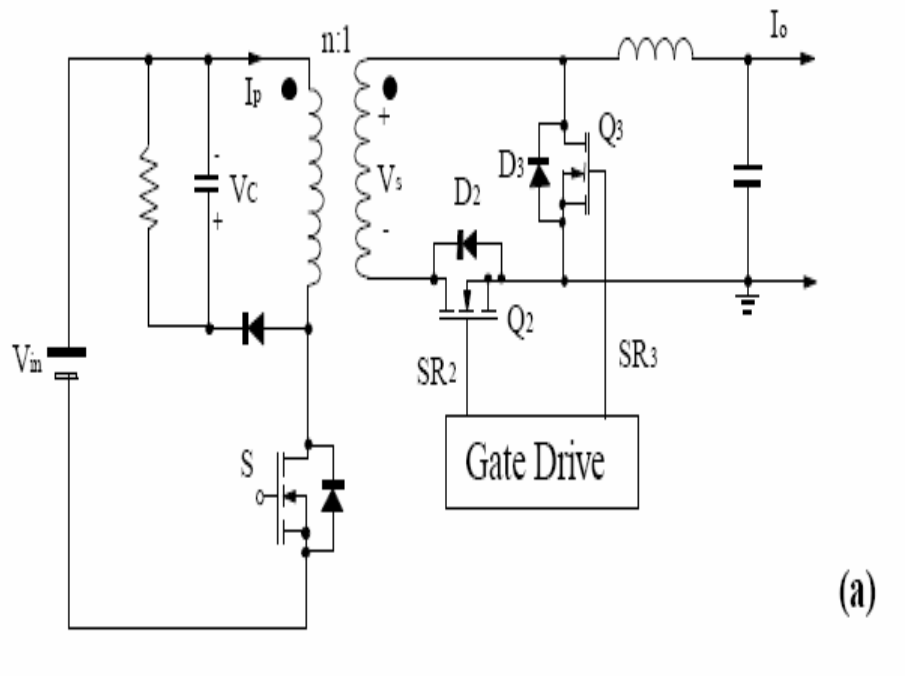

Figure 4.4: Forward converters with control driven SRs

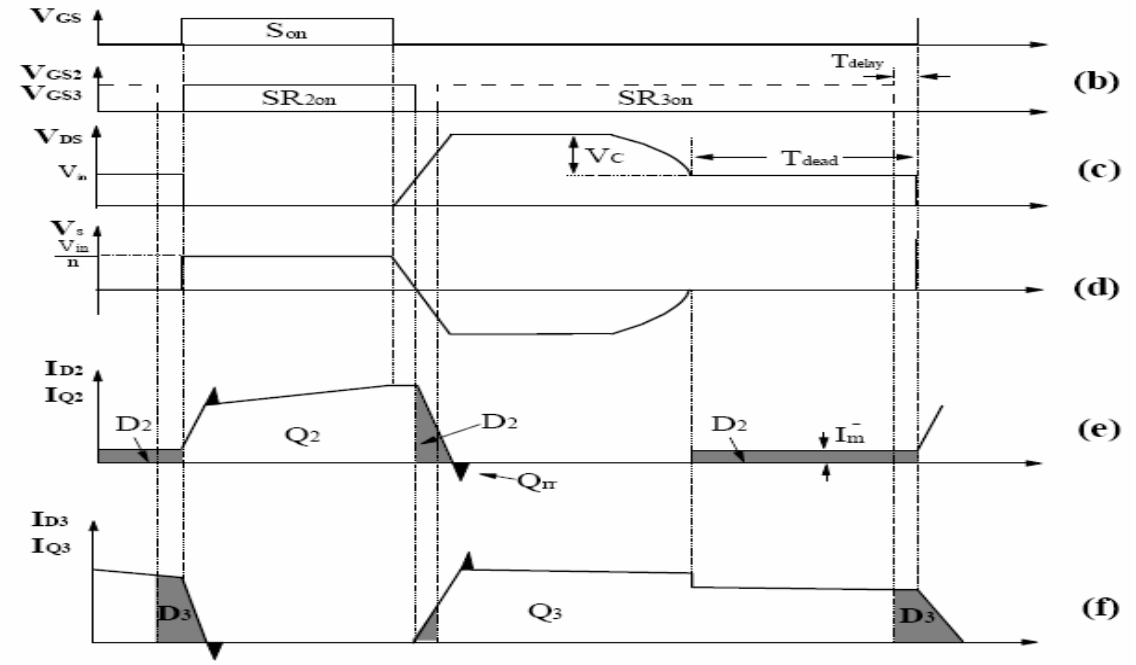

Figure 4.5: Waveforms or forward converter with control driven SRs

4.1 Basic Controlling Methods

There are two feedback control methods; one is the voltage mode control and another current mode control. The main purpose of these control methods is to adjust the duty cycle of the PWM to regulate the output voltage. Voltage mode control method is also called as a single loop control method because only the output voltage, V_{out} is sensed and used in the feedback control circuit. Current mode control method uses two feedback signals that are the output voltage and the filter inductor current.

4.1.1 Voltage Mode Control

The most extended dc-dc converter uses voltage mode control ,where there is a single feedback loop with the output voltage used as the feedback signal. The output voltage V_{out} from the dc-dc converter is sensed and compared to a reference voltage V_{ref}. The difference between the V_{ref} and V_{out} is known as V_{error}. V_{error} is then compared with a fixed frequency triangular waveform, and output is a pulse-width modulated signal that is used to control the switch. When V error is positive, the PWM duty ratio is decreased so that so that the ON time of the switch is for a longer period. Where when the V error is negative, the PWM duty ratio is increased and the switch is ON for a shorter period. When V error is zero, the previous PWM duty ratio is maintained.

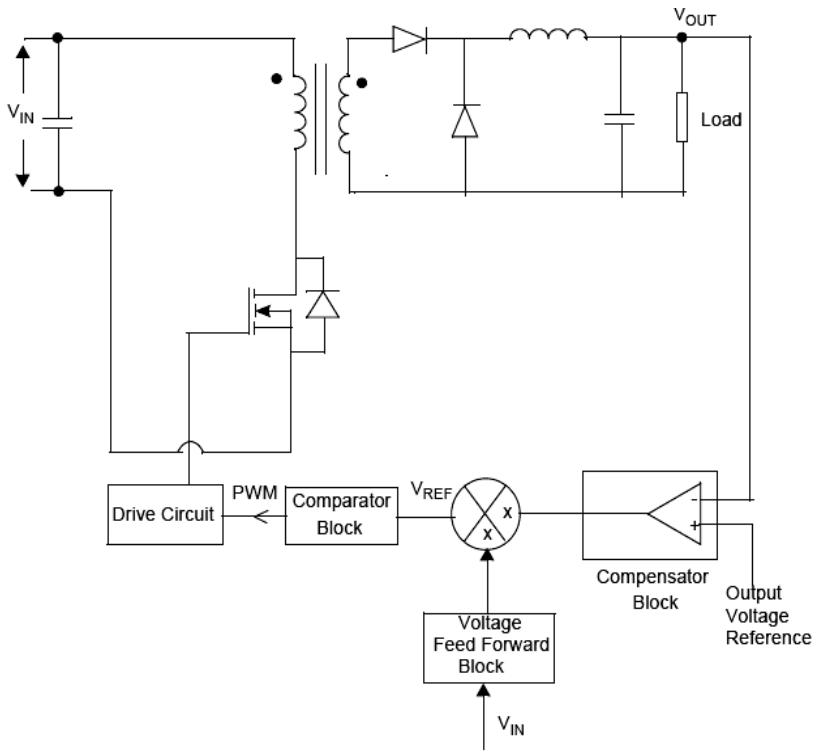

Figure 4.6: Voltage control method

4.1.2 Current Control Method

The current mode control technique requires two feedback loops, In this mode, two parameters are measured for control purposes. The output voltage is measured at the output capacitor or at the load end (known as remote sensing). The output inductor/primary switch current is also measured. In current mode control, the output voltage is first compared with the reference voltage (desired output voltage). This error is then processed by the compensation block to generate the reference signal for the current loop. This current reference is compared to the measured current. Any error generated by the comparison of the reference generated by the voltage compensation block and the actual current drawn from the input is processed by the current compensation block. This generates the required duty cycle to maintain the output voltage within the specified limit. As current mode control senses the circuit current, any change in output load current or the input voltage can be corrected before it affects the output voltage. Sensing the input current, which depends on input voltage, provides the inherent feed-forward feature. Current mode control provides

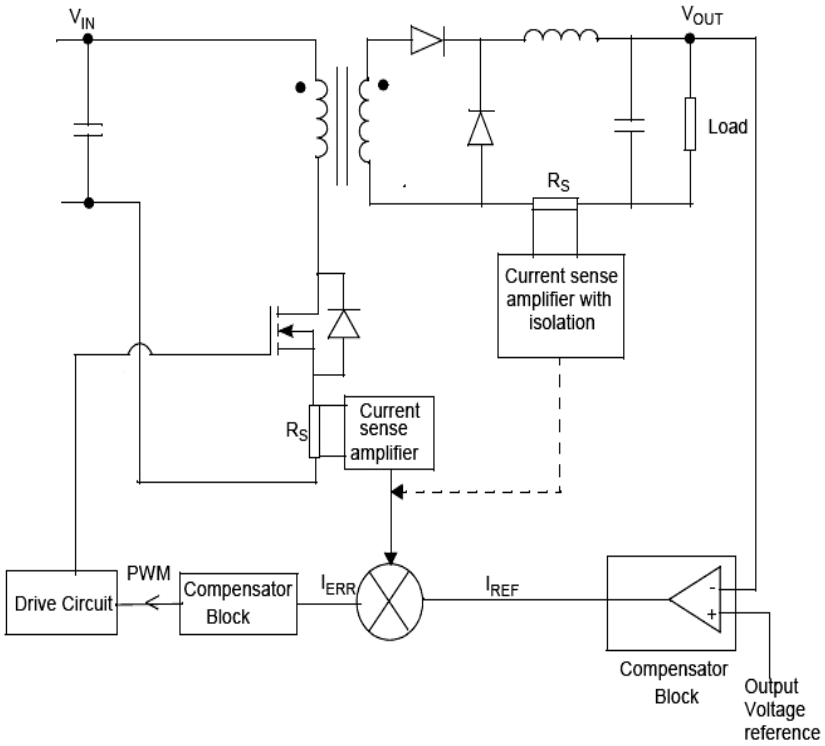

Figure 4.7: Current control method

inherent input current symmetry for the push-pull and bridge converters, inherent current limiting features and load sharing features for multiple converters connected in parallel. It also improves step load response and transient response because of the inner current loop.

Chapter 5

DESIGN OF POWER CIRCUIT

5.1 Design of Power stage of Half-Bridge converter

5.1.1 Design of Main Transformer

Ferrites are the best core material choice for frequency from 10 kHz to 50 mHz because of several advantages over other types of magnetic material as high electrical resistivity, low eddy current losses, low cost, high stability and lowest volume. The half bridge converter allows flux excursion in the first and third quadrants of the B-H curve. This has the effect of making core loss consideration the limiting factor in B_{max} choice instead of the possibility of saturation. A good material for low core loss at 100 kHz and saturation is VITROPERM 500 F. In this design 25 kHz switching frequency, limiting the core losses to an acceptable level allows the flux to operate at a maximum flux level (B_{max}) of 0.15 T (3000 G).

Specifications of SMPS

Output voltage: 25 V DC

Load Current: 10 A

Input voltage: 160-280 V AC

Step-1: Secondary Output Power Calculation

$$Po = Vo' \times Io$$

$=(Vo + Vrl + Vd) \times Io$

$=(25 + 2.5 + 1.5) \times 14$

=406 Watts

Where, Vo = Output voltage,

Vrl = Voltage drop due to the winding resistance of the inductor and transformer 10percentage of Vo,

Vd = Voltage drop in rectifier diodes

Io is taken as 1.33 times the continuous load current

Step-2: Calculation of Area Product

$$Ap = \frac{Po \times (\sqrt{2} + \frac{1}{\eta})}{4 \times Kw \times J \times Bm \times fs}$$

Where,

Po = 406Watt

Q= Efficiency of the transformer = 0.8,

Kw = Window utilization factor = 0.45,

J = Current density = 3A/mm2

Bm = Maximum flux density = 0.2wb/m2 = 0.2 T

fs = Switching frequency = 25 kHz

$Ap = \frac{406\times(\sqrt{2}+\frac{1}{0.8})}{4\times0.45\times3A/mm^2\times0.2Wb/mm^2\times25\times10^3}$
$=4.006 \times 10^4 mm^4$

Chosen a suitable core (from data sheet) with value of area product greater than the calculated value, so, ferrite core type E 42/21/15 is selected, with following specifications:

Ap= Area product = $4.659\times10^4 mm^4$,
Ac= Core cross section area = 182 mm^2,
Aw= Window area = 256 mm^2,
le= Mean length per turn = 93 mm
lm= Mean magnetic length = 97.2 mm
AL= (nH/turn2) 25% = 4778

Step-3: Calculation of Primary Turns

$N1 = \frac{V_{dcmax}}{4\times2\times Ac\times Bm\times fs}$
$N1 = \frac{\sqrt{2}\times280\times0.7}{4\times2\times182*10^-6\times0.2\times25000}$
=39

Step-4: Calculation of Turns ratio

n=N2/N1
$=\frac{Vo'}{2\times Dmax\times(Vdcmin-voltagedropacrossfluxwalkingcapacitor)}$
Considering Dmax = maximum duty cycle = 0.45, and voltage drop across flux walking capacitor = 10 % of Vdcmax
$n = \frac{29}{2\times0.45\times(160\times\sqrt{2}-0.1\times277.18)}$
=0.162

Step-5: Calculation of Secondary Turns

N2 = $n \times N1$

= 0.162×39

= 6.318

= 7 turns

Note:Here two secondary windings so total secondary turns are 14.

Step-6: The wire gauge selection

I2 = $Io \times \sqrt{D}max$

= $14 \times \sqrt{0}.45$

= 9.39 A

I1 = $n \times Io$

= 0.162×14

= 2.268 A

Cross sectional area of the primary wire

a1 = I1/J

= 2.268/3

= 0.756 mm^4

Cross sectional area of the secondary wire

a2 = I2/J

= 9.39/3

= 3.13 mm^4

SUMMARY:

Sr. No.	Parameter	Value
1	Ferrite Core Type	EE 42/21/15
2	Primary Turns	39
3	Secondary Turns	14
4	Primary Wire Gauge	19 SWG
5	Secondary Wire Gauge	14 SWG

CROSS CHECK

Using the actual conductor area, it was check back to see if the turns fit into the window area Aw of the core by checking for the inequality

$AwKw \geq a1N1 + a2N2$

$(256 \times 0.4) \geq (0.756 \times 38) + 2(3.13 \times 7)$

$102.4 \geq 72.54$

So, the inequality is satisfied, which means that the windings will fit in the available window area

5.1.2 Design of input side Capacitors

Assuming peak to peak ripple voltage at output be 3V. Therefore Vpp=3V

Now $Vpp = \frac{I}{2 \times f \times C}$

Therefore, $C = \frac{I_{load}}{2 \times Vpp \times f}$

From the theory of turn ratio of transformer, we have

$\frac{V_2}{V_1} = \frac{I_2}{I_1}$

$\frac{50}{163} = \frac{10}{I_1}$

The primary current $I_1 = 3.06\text{A} = I_{load}$

so, C = $\frac{3.06}{2 \times 3 \times 50}$

=15300 μ F

This value is near to the simulation value used in the simulation of SMPS.

5.2 Design of control circuit of Half-Bridge converter and Synchronous Rectifier

LM5035-PWM CONTROLLER WITH INTEGRATED HALF-BRIDGE AND SYNCH FET DRIVER:

The LM5035 PWM Controller contains all of the features necessary to implement half-bridge voltage-mode controlled power converters. The LM5035 provides two gate driver outputs to directly drive the primary side power MOSFETs and two signal level output to control secondary synchronous rectifier through an isolation interface. Secondary side driver, such as the LM5110,are typically used to provide the necessary gate drive current to control the sync MOSFETs.

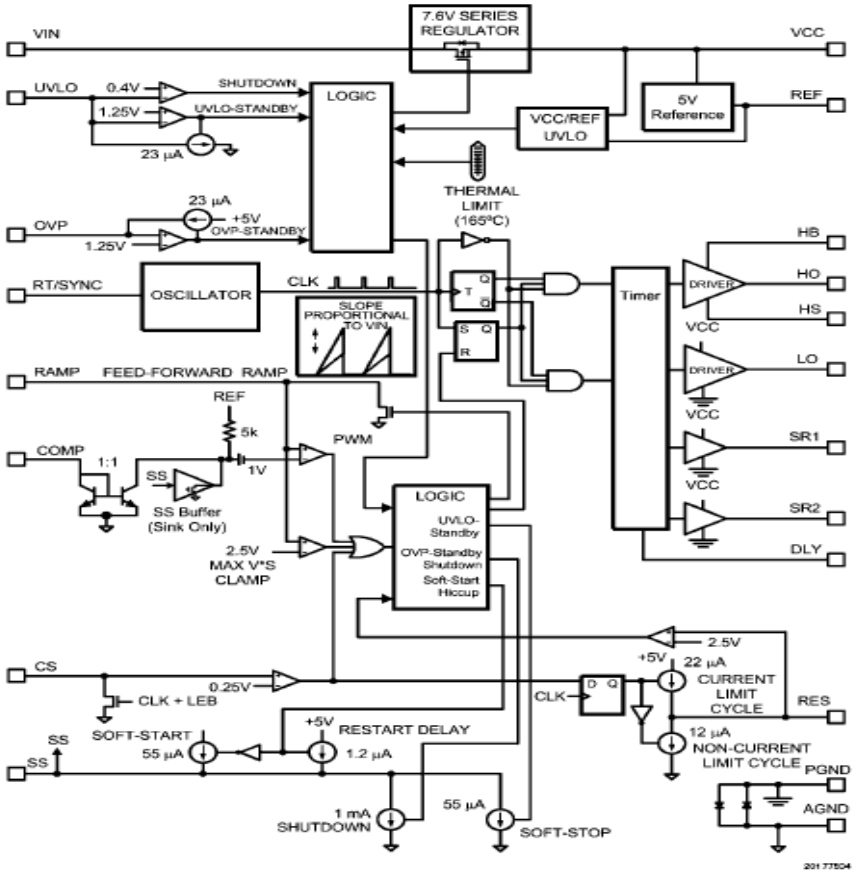

Figure 5.1: Block diagram of LM5035

5.2.1 Test Circuit

- RT pin gives the Oscillator Frequency . We can set the desire frequency by connecting the variable resistor port. Selected frequency is 50 kHz
- V_{IN} 15 V DC supply voltage select.
- External V_{CC} voltage can be applicable from 8 V to 15 V DC.

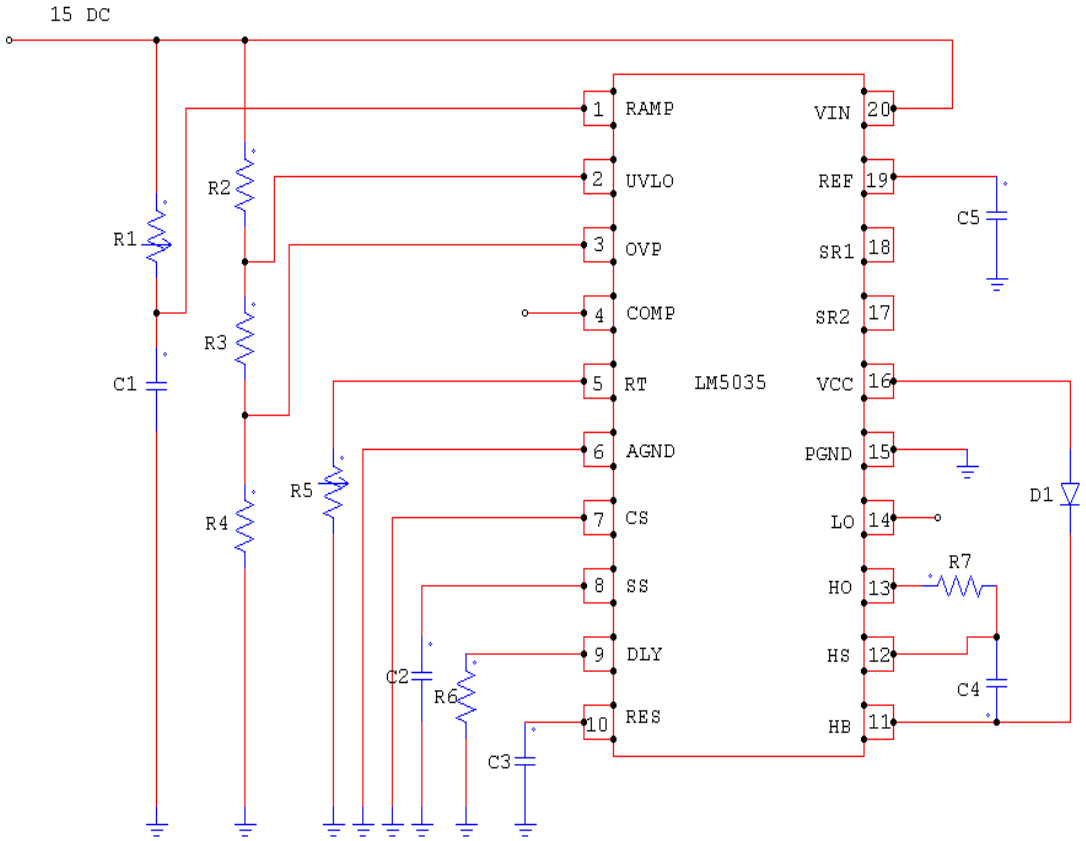

Figure 5.2: Test circuit of LM5035

Table I: List of components of test circuit:

serial No	component	Description	value
1	R_1	Metal film oxide	$220K\Omega$
2	R_2	Mental film oxide	$86.95K\Omega,\frac{1}{4}$
3	R_3	Mental film oxide	$3.23K\Omega,\frac{1}{4}$
4	R_4	Mental film oxide	$6.012K\Omega,\frac{1}{4}$
5	R_5	Mental film oxide	$125K\Omega,\frac{1}{4}$
6	R_6	Mental film oxide	$20K\Omega,\frac{1}{4}$
7	R_7	Mental film oxide	$1K\Omega,\frac{1}{4}$
8	C_1	Ceramic	470pf
9	C_2	Ceramic	$0.01\mu F$
10	C_3	ceramic	$0.2\mu F$
11	C_4,C_5	ceramic	$0.1\mu F$
12	D_1	Diode	1N4007,1000V

5.2.2 Design of Voltage divider circuit

$$R_1 = \frac{UVLO_{on} - UVLOoff}{23\mu A} \tag{5.1}$$

$$R_{COMBINED} = \frac{1.25V \times R_1}{UVLO_{off}1.25V} \tag{5.2}$$

$$R_3 = \frac{1.25V \times (R_1 + R_{COMBINED})}{OVP_{off}} \tag{5.3}$$

$$R_2 = R_{COMBINED} - R_3 \tag{5.4}$$

Taking $UVLO_{on}$=15V, $UVLO_{on}$=13V, OVP_{off}=20V

by this calculation, $R_1 = 86.956k\Omega$

$R_2 = 3.238k\Omega$

$R_3 = 6.012k\Omega$

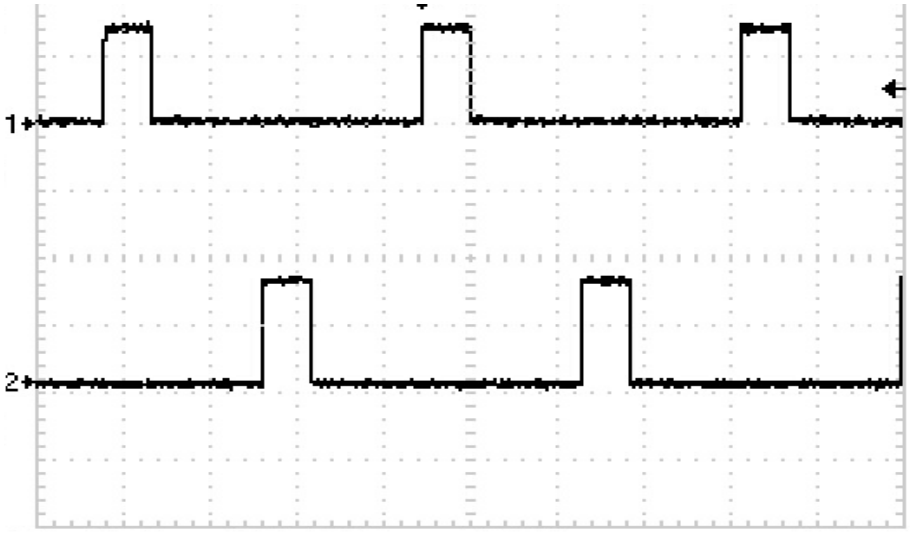

Figure 5.3: Gate pulses of inverter Upper trace HO: Lower trace Lo
X-axis 10 μs/div, Y-axis: 5 V/div

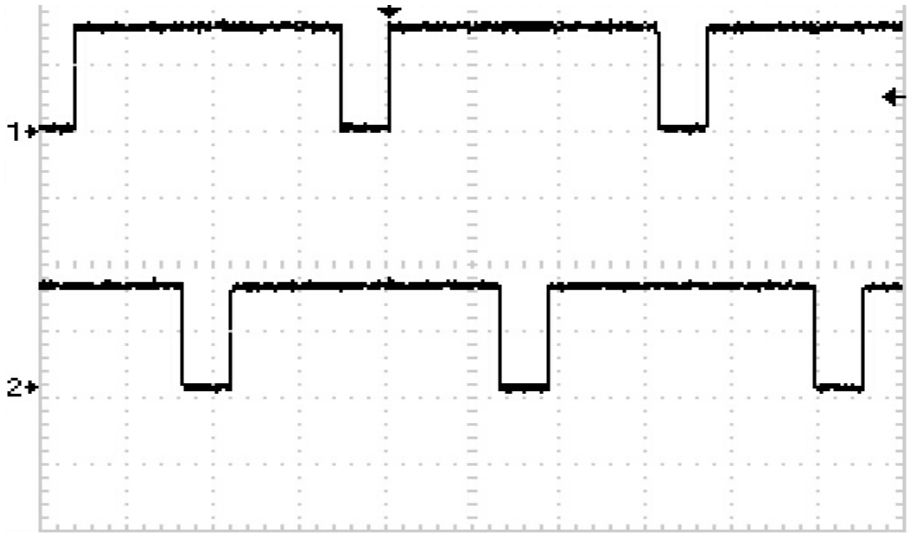

Figure 5.4: Gate pulses of Synchronous rectifier Upper trace SR1: Lower trave SR2
X-axis 10 μs/div, Y-axis: 5V/div

fig. 5.3, fig. 5.4 respectively shows the gate pulses of the inverter and Synchronous rectifier MOSFETS from the controller IC LM5035 with the 25 kHz frequency. Here the Synchronous rectifier pulses SR_1 and SR_2 have the large duty cycle than the inverter pulses because of the large reset time of the transformer secondary windings.

5.3 Synchronous rectifier driver circuit and output results

In this report two gate driver circuits are given to drive the Synchronous rectifier MOSFETs . In this circuit two optocoupler (6N137) and totempole arrangement are used which gives the isolation between control IC and power circuit and increase the current capacity of driver.

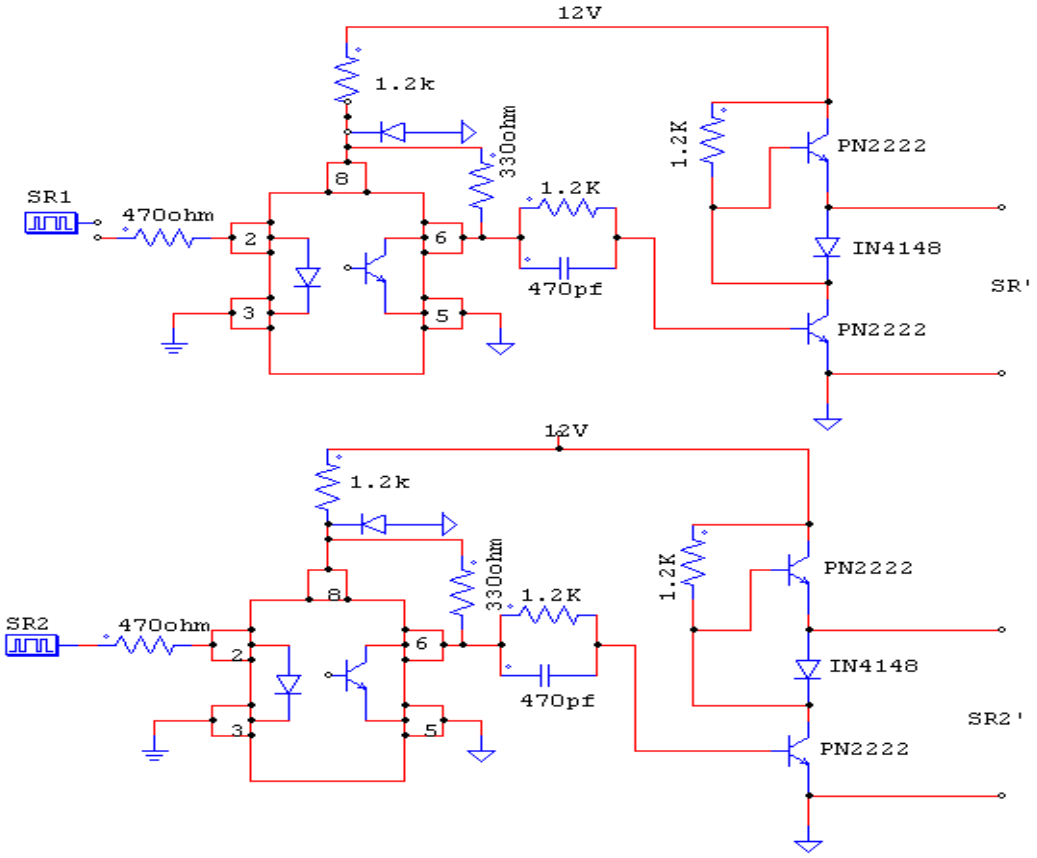

Figure 5.5: Gate driver circuit for SR

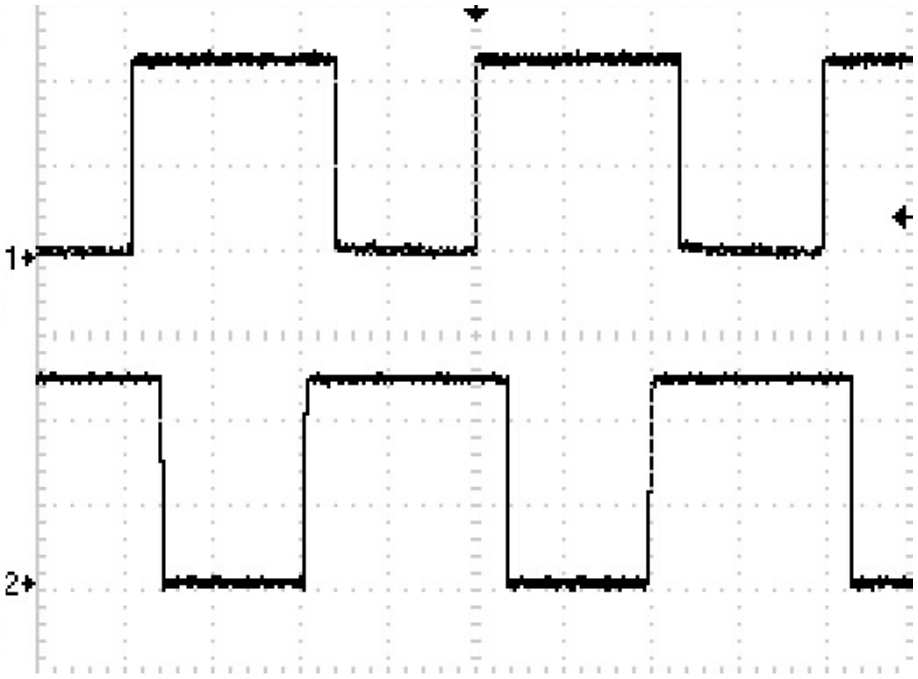

Figure 5.6: Gate driver pulses Upper trace SR1'pulse: Lower trave SR2'pulse
X axis:10 μ s/div, Y axis:5 V/div

The waveforms of Totem pole driver shows that the driver is very fast. The advantage of the Totem pole arrangement is, it increases the current and voltage capacity of the driver. Also Ouptocoupler provides the proper isolation between the input and output pulses. Hence this driver gives the proper and efficient operation at high switching frequency.

Chapter 6

SIMULATION RESULTS:

6.1 Simulation of SMPS

This is the simulation of SMPS . This simulation is divided in five parts ,

1 Input supply voltage 230 V

2 Input side Rectifier

3 In put side Inverter using half-bride converter

4 Transformer with the rating of 160-280 V , 10 Amp, switching frequency 25 kHz.

5 Out put side rectifier.

Here rectifier gives DC link voltage to the Inverter. Here C1 ,C2 capacitors are connected across the dc link which gives the half of the supply voltage to the each inverter MOSFETs. Inverter convert the dc voltage in to the ac voltage and supply to the transformer. Now transformer step down the ac voltage and further this ac voltage is convert in to the dc voltage by the out put rectifier using and supply to the load. By this simulation we got out put 50 V across the load and the 10 Amp out put current which are the desirable values.

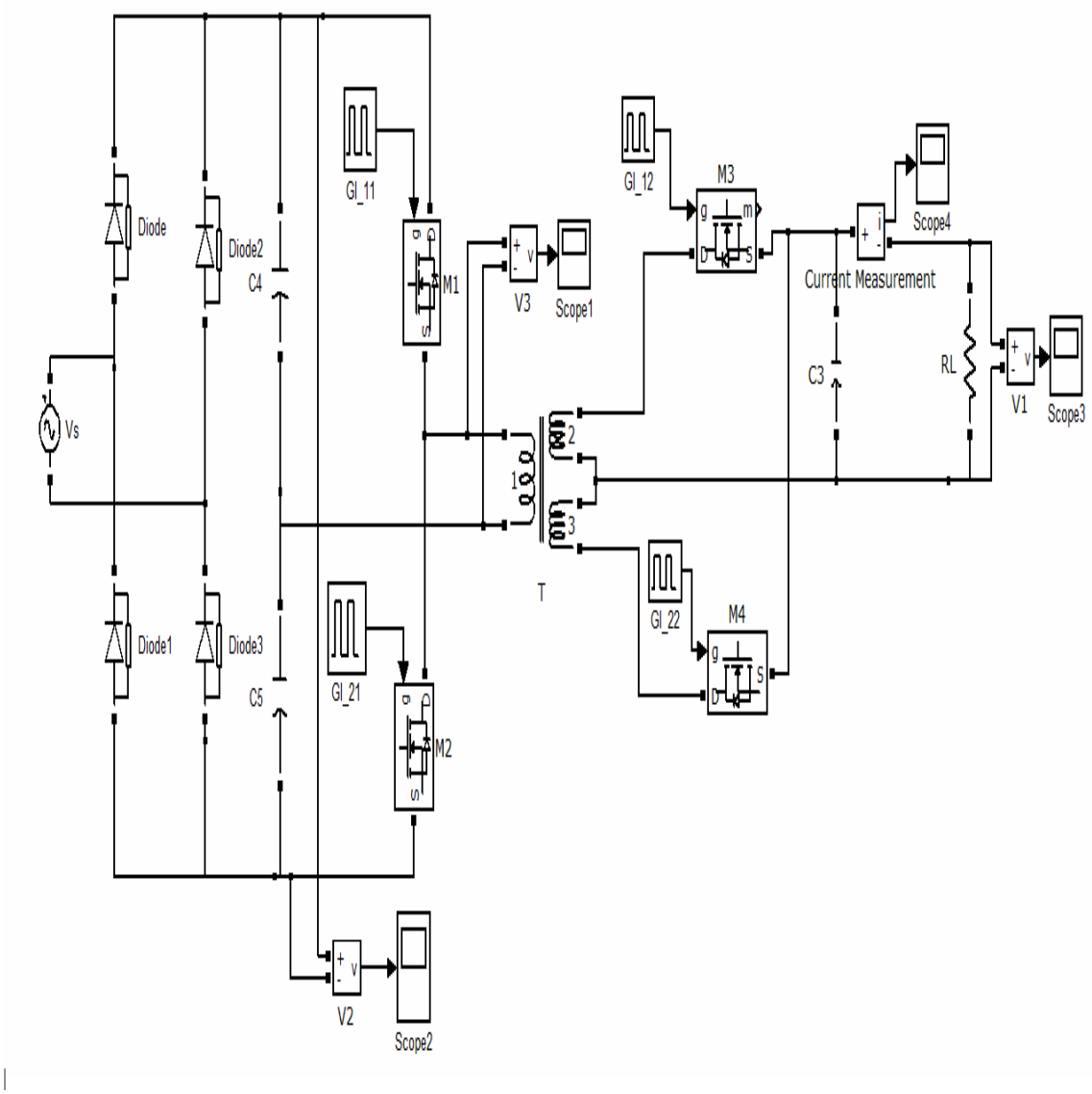

Figure 6.1: Simulation circuit

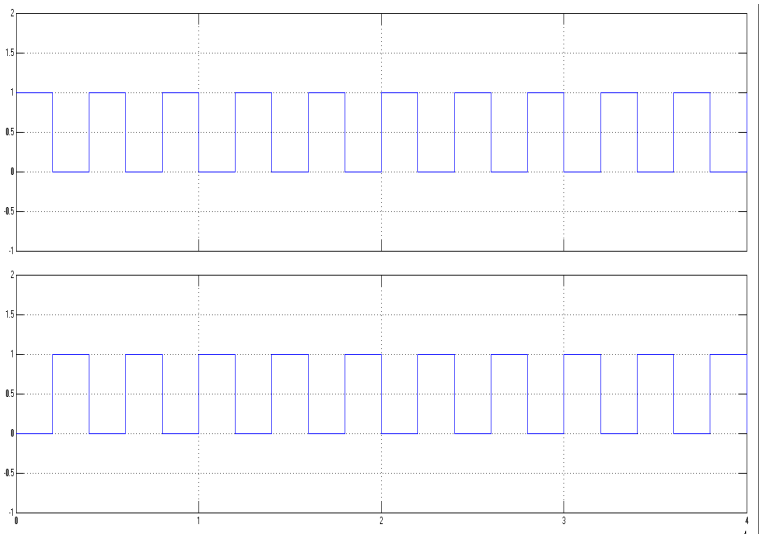

Figure 6.2: Gate pulse Upper trace HO pulse:Lower trace LO pulse for inverter MOSFETS

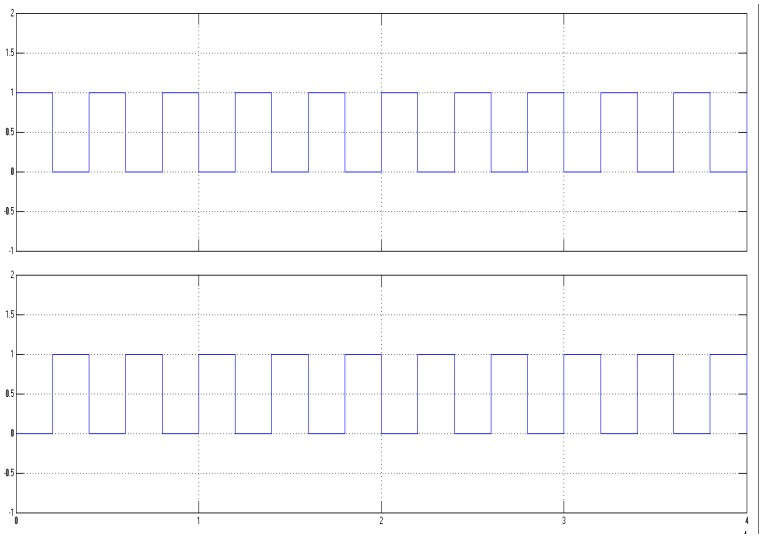

Figure 6.3: Gate pulse Upper trace SR1 pulse:Lower trace SR2 pulse for inverter MOSFETS

6.1.1 Simulation Results:

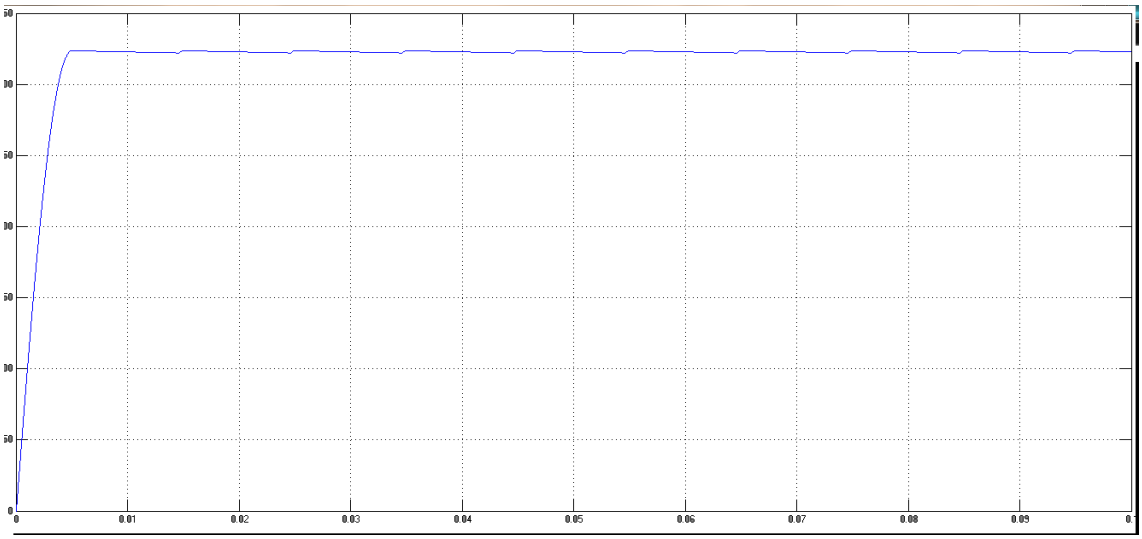

Figure 6.4: DC-Link Voltage

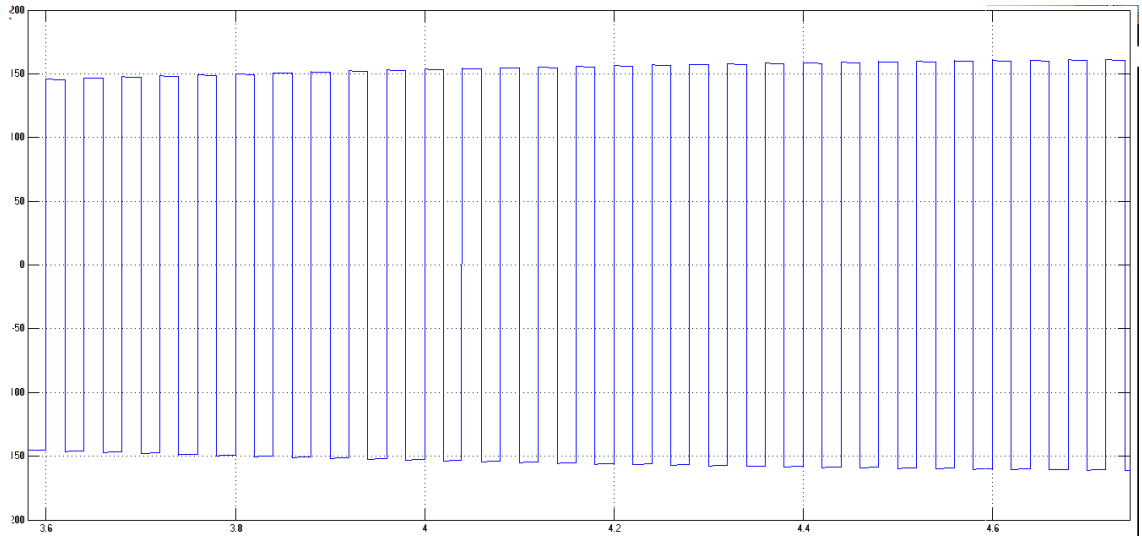

Figure 6.5: Transformer primary voltage

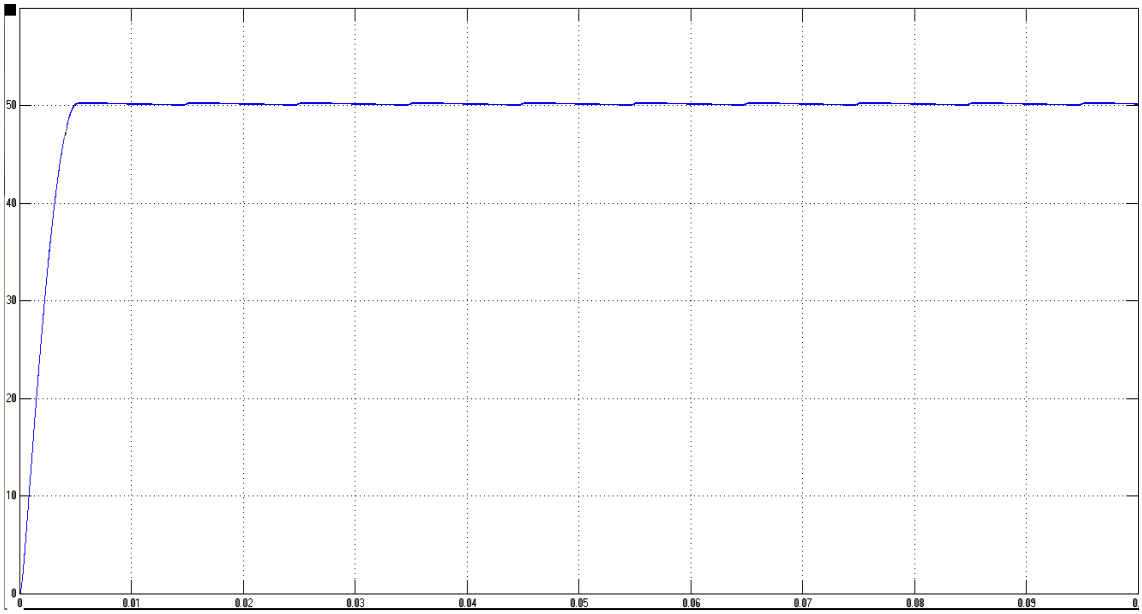

Figure 6.6: Output voltage

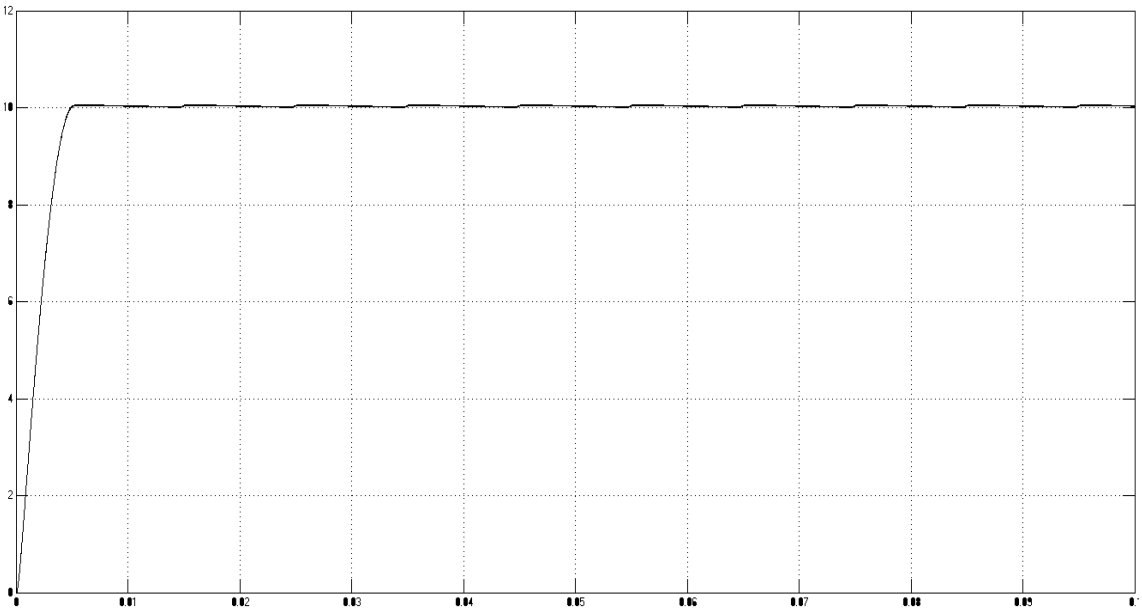

Figure 6.7: Output current

Chapter 7

HARDWARE IMPLEMENTATION AND RESULTS:

7.1 Schematic of SMPS using Half-bridge topology:

fig.7.1 is the Schematic diagram of the SMPS using Half-bridge topology. In this Schematic diagram LM5035 is used for the controller ic. This controller gives the two driver output pulses HO and LO which are directly given to the inverter MOSFETs and two signal level output pulses for the Synchronous Rectifier MOSFETs. Here two Totem pole driver is used to increase the capacity to drive Synchronous Rectifier MOSFETs. Isolation is provide by using optocoupler (6N137).

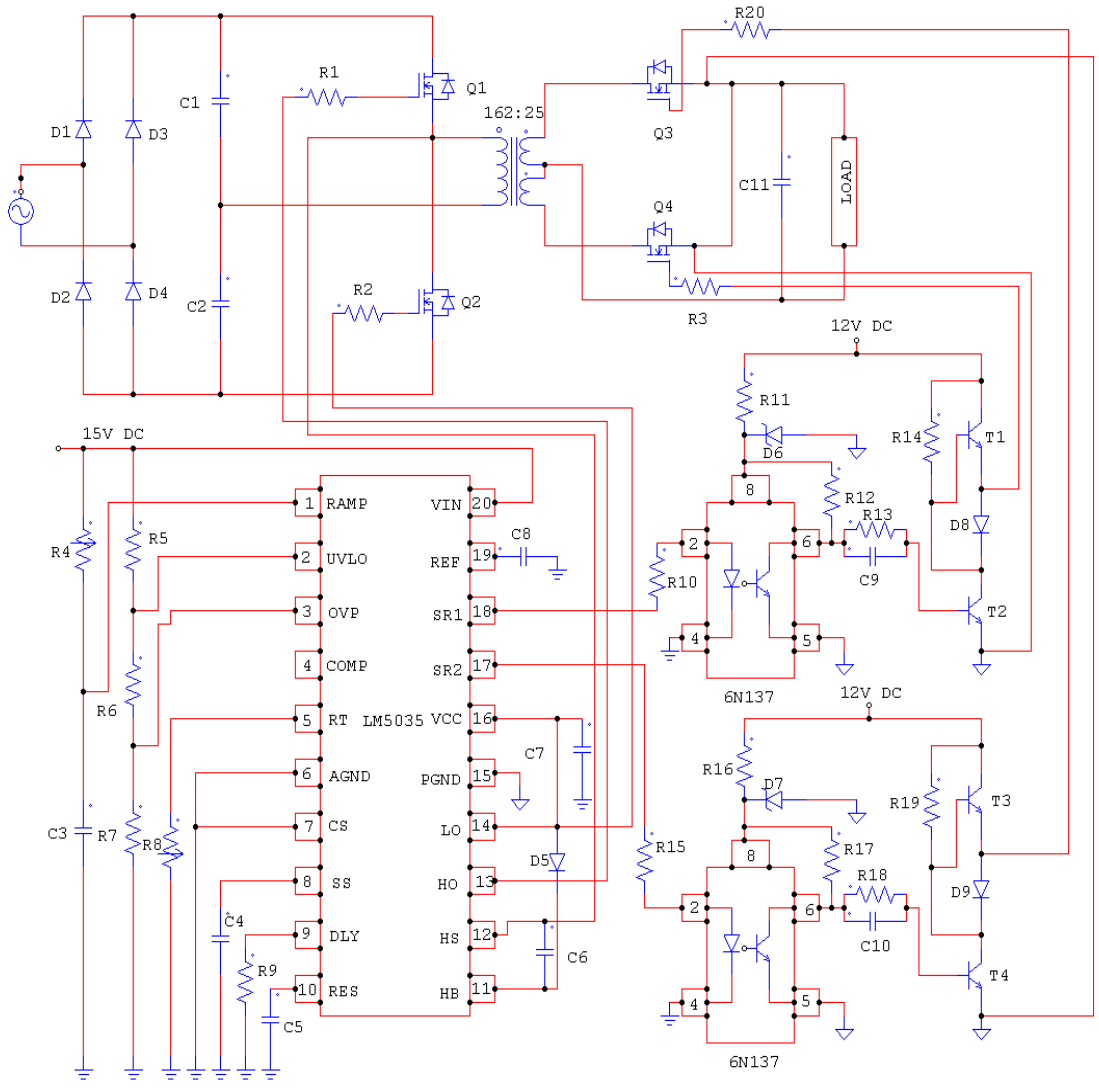

Figure 7.1: Schematic of SMPS

Table I: List of components of SMPS Schematic

Serial no	**Components**	**Description**	Value
1	R_1,R_2,R_3,R_{11},R_{16},R_{20}	Metal film oxide	$1K\Omega$
2	R_4,R_8	Metal film oxide	$220K\Omega$
3	R_5	Metal film oxide	$86.95K\Omega$
4	R_6	Metal film oxide	$3.23K\Omega$
5	R_7	Metal film oxide	$6.012K\Omega$
6	R_9	Metal film oxide	$22K\Omega$
7	R_{10}, R_{15}	Metal film oxide	470Ω
8	R_{12}, R_{17}	Metal film oxide	330Ω
9	R_{13}, R_{14}, R_{18}, R_{19}	Metal film oxide	$1.2K\Omega$
10	C_1,C_2	Electrolite	$5000\mu F$,200V
11	C_3,C_9,C_{10}	Ceramic	470pf
12	C_4	Ceramic	$0.01\mu F$
13	C_5	Ceramic	$0.2\mu F$
14	C_6,C_8	Ceramic	$0.1\mu F$
15	C_7	Electrolite	$1\mu F$
16	C_{11}	Electrolite	$1000\mu F$,63V
17	T_1,T_2,T_3,T_4	Transistor(PN2222)	40V
18	D_6,D_7	Zener	5.1V
19	D_8,D_9	Switching Diode(IN4148)	100V
20	Q_1,Q_2,Q_3,Q_4	MOSFET(IRFP350)	400V,15A

7.2 Hardware Results:

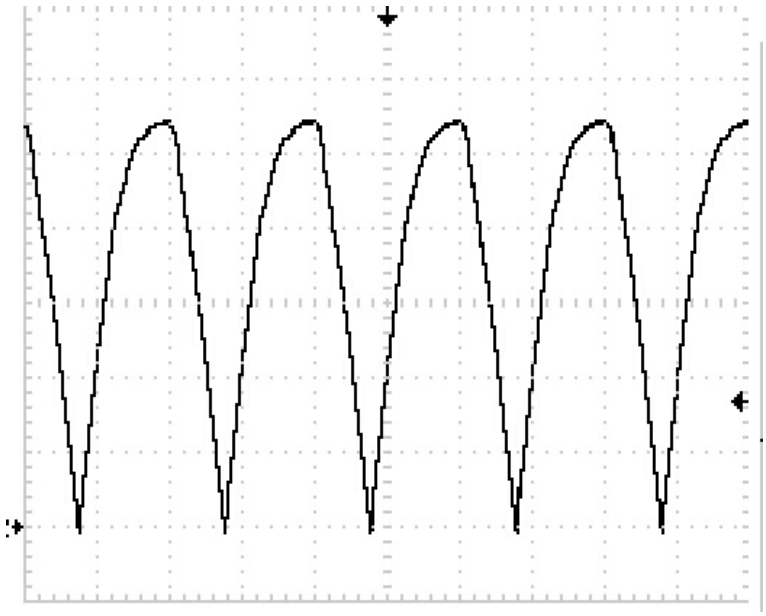

Figure 7.2: Input side rectifier output X-axis:50 ms/div, Y axis:50 V/div

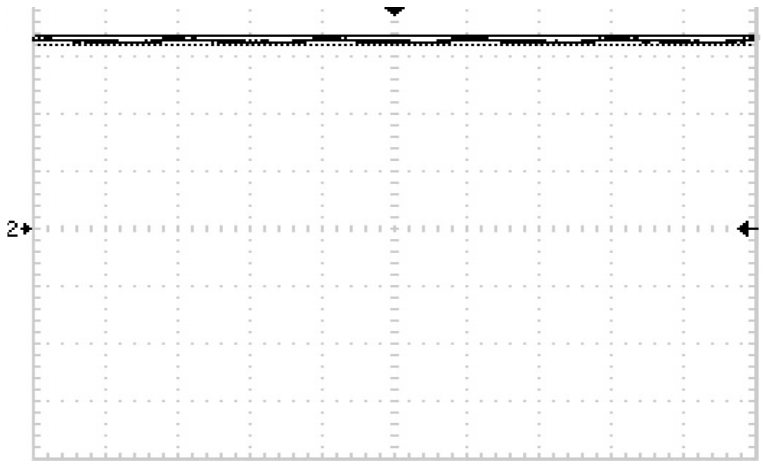

Figure 7.3: Input side DC link voltage X-axis:5 ms/div, Y-axis:20 V/div
Δ V 3.20 V ripple

fig. 7.2 shows the input side rectifier output with out using filter capacitor. fig. 7.3 shows the input side dc link voltage with filter capacitor. This rectifier is tested at the 60 V ac and gives the 60 V dc output with 3.20 V ripple voltage.

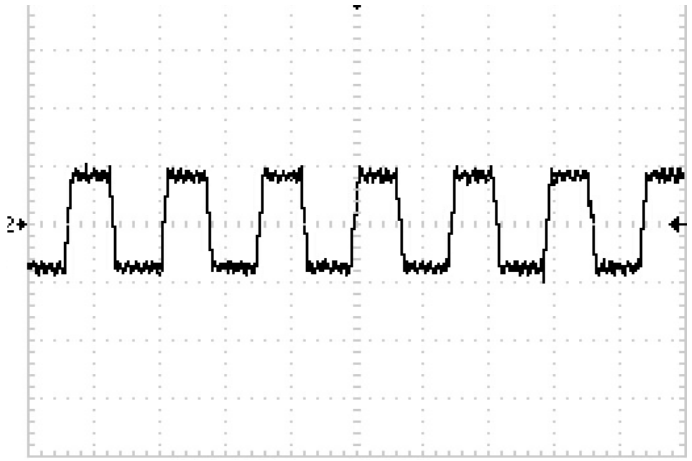

Figure 7.4: Inverter output voltage with high frequency transformer at 30 V DC
X axis:25 μs/div, Y axis:5 V/div

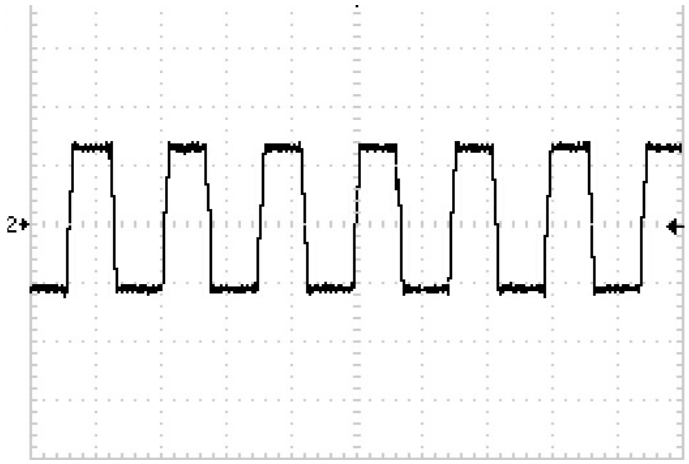

Figure 7.5: Inverter output voltage with high frequency transformer at 40 V DC
X axis:25 μs/div, Y axis:5 V/div

Half-Bridge inverter is tested at different dc link voltages 30 V dc, 40 V dc respectively. Various output voltage waveforms are shown in fig. 7.4 and fig. 7.5.

Half-Bridge inverter is tested at different dc link voltages 30 V dc, 40 V dc respectively with high frequency transformer. Various output voltage waveforms with 25 kHz frequency are shown in fig. 7.4 and fig. 7.5 respectively.

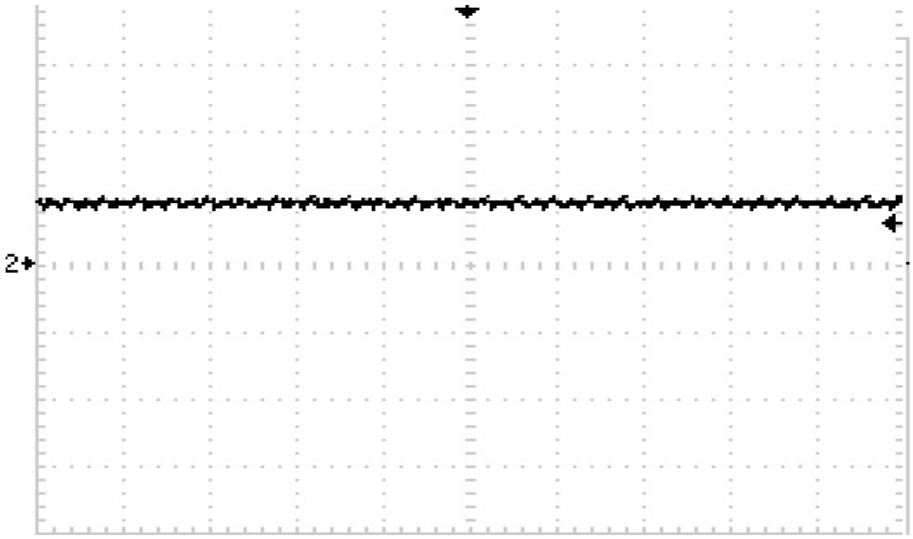

Figure 7.6: Synchronous Rectifier output voltage at 30 V pk-pk input
X axis:100 μs/div, Y axis:2 V/div

fig. 7.6 shows the load output voltage of the Synchronous Rectifier. Synchronous Rectifier gives the 2 V dc output voltage at the 30 V ac inverter input voltage with 0.1 mv ripple voltage.

7.3 Hardware Setup:

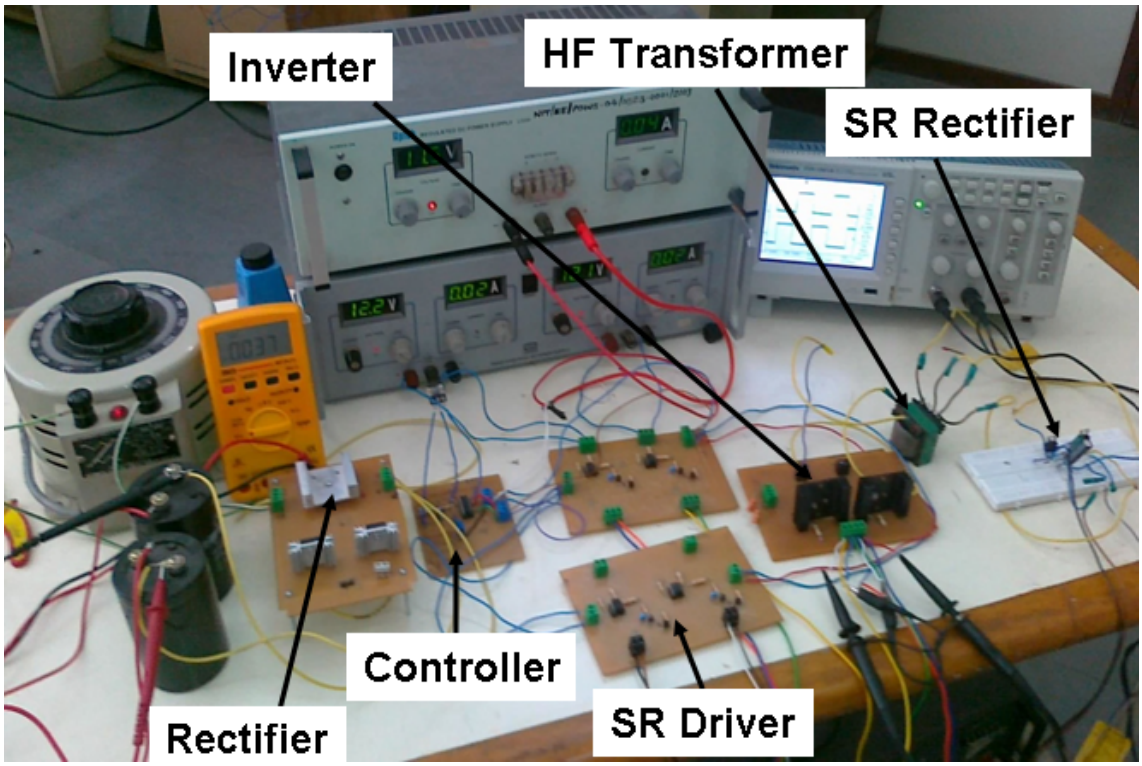

Figure 7.7: Complete Hardware Setup

Chapter 8

CONCLUSION AND FUTURE SCOPE

8.1 Conclusion

It is concluded that half-bridge topology with Synchronous Rectification Technique for proposed project is the best suited technique with reduced losses and better control over the voltage. There are also different SR techniques like self driven and control driven, but in this project control driven SR is designed and developed. The basic simulation gives very good results for the output voltage of 25V and 10A load current. The device selection is done on the basis of theoretical calculations and the simulation models developed in MATLAB. Half bridge topology is selected based on the selection charge depending on various selection parameters. A half-bridge inverter circuit is prepared and tested at 30 V and 40 V dc supply by applying obtain gate pulses and satisfactory results are achieved. In this report gate driver for Synchronous Rectifier are developed and got satisfactory gate pulse are obtain. Synchronous Rectifier circuit is tested at 30 V dc supply at primary side of the transformer and it gives the 2 V dc with 100 mv ripple.

8.2 Future Scope

This project can be extended by using close loop control at the output rectifier side. It can be extend for the higher voltage testing by changing the topology of the inverter.

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Appendix A

Ic used:

- Datasheet of LM5035
- Datasheet of IRFP460
- Datasheet of 6N137
- Datasheet of 1N4007
- Datasheet of IN4148
- Datasheet of PN2222