Design and Development of Three Phase Diode Point Clamped Active Front End Converter

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***Abstract*—The paper presents the design, development and implementation of a Three Phase diode clamped active front-end converter in rectification mode for the power factor control and power quality improvement. Specifically this paper concentrates on the dc link capacitor balancing and maintenance of near to unity power factor of the supply. The paper also proposes an existing and popular mathematical modeling for the converter. The modulation technique used ensures minimum switching losses. Proposed scheme also has wide input range and good input side power factor.**

Keywords-Active Front End Converters, Unity Power factor Controlling, Power quality improvement.

I. INTRODUCTION

RECTIFIERS or DC Converters are extensively used in various applications like power supplies, dc motor drives, front-end converters in variable speed drives, SMPS, HVDC transmission lines etc. Traditionally the converters have been dominated by the use of Diode Bridges or phase controlled rectifiers. These converters act as non-linear loads on the power system and draw input currents which are rich in harmonics and have poor supply power factor. Thus creating power quality problem for the power distribution networks and for the other important electrical systems in the vicinity of it. So as to get rid of these problems several regulatory norms have been instituted such as IEEE-519. IEC555 etc. and these standards or norms have been strictly enforced on the consumers and manufacturers. To meet these standards and achieve power quality improvement there has been extensive use of passive filters, active filters and Hybrid Filters, along with the conventional rectifiers in high power and already installed applications. In this respect new advancements have been initiated in the field of power quality improvement and they have become integral and inherent part of the electrical systems.

Various topologies of three-phase power factor improvement have been developed like the buck, boost, and buck-boost converters. The use of Active Front-End Converter (AFC) topologies have also become extensive in the power quality improvement techniques because of their excellent performance like sinusoidal input currents with negligible THD, high supply power factor, regulated and near to ripple free dc output voltage, reduced voltage stresses, reduced dv/dt stresses and hence low EMI emissions [1] [3] [5] [6]. The sinusoidal supply currents at unity power factor are produced in the AFCs. With higher number of levels, high voltage, high power applications are possible.

In this paper a three-phase diode clamped converter is proposed to reduce the line-current harmonics, give nearly unity power factor, produce well- regulated dc output voltage with negligible ripples and provide dc bus capacitor voltage balance. The converter strategy helps in maintaining the regulatory norms such as IEEE-219 and IEC555 [2] [7]. The proposed topology also nullifies the use of bulky passive and hybrid filters which were previously very much popular [4]. A PI controller is realized on TMS320F240 DSP to achieve the dc link voltage control, the dc link capacitor voltage balance and the input line side power factor control. To verify the validity of the proposed scheme the hardware implementation has been included in this paper. A mathematical model of the converter has also been suggested in this paper [8].

II. SYSTEM DESCRIPTION

The adopted three-phase power factor correction converter using the neutral point topology is shown in the Figure 1 below. The input of the topology is the three-phase 50 Hz ac supply and each line contains boosting inductors at the input side. Each power switch which is IGBT in this case blocks a voltage of half the dc link across them. The switches are commutated with a high switching frequency to generate the PWM signals for the gate pulse of the IGBT.

The main requirement of the boosting inductor is to boost the dc link voltage from the rectified value of 584V to around 800V. Here the converter also works as a boost converter. The switching sequence of the devices is controlled by the PI controller. Here the switches Ta1, Ta2, Tb1, Tb2, Tc1, Tc2 make up the positive pairs of IGBTs, whereas the switches Ta3, Ta4, Tb3, Tb4, Tc3, Tc4 are the negative IGBT pairs.

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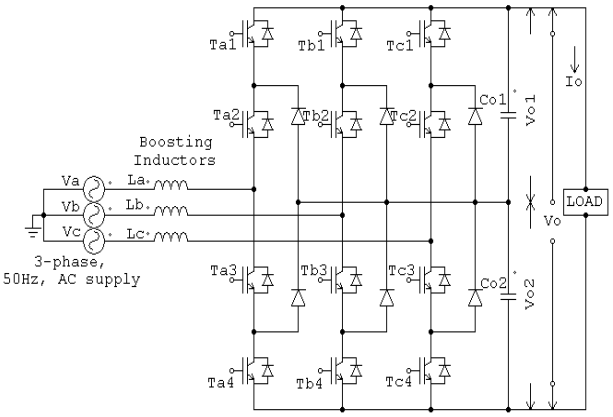

Figure 1 Proposed Three-Phase Neutral Point Clamped Converter

III. Block Diagram And Control Strategy

The main aspects for the control strategy for the proposed converter topology were as under.

1. Minimization of input current harmonics.
2. Maintaining near to unity power factor.
3. Regulating and controlling of the DC load voltage.
4. Maintaining DC link capacitor voltage balancing.

The proposed block diagram and control strategy of the converter topology is shown in the Figure 2 below.

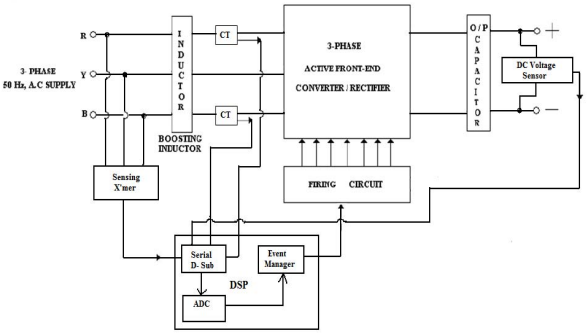

Figure 2 Block Diagram and Control Strategy of proposed Three-Phase Neutral Point Clamped Converter

In the proposed control strategy PI controllers which are implemented on DSP are used for the controlling of the firing pulses of the two groups of IGBTs in the same leg of the converter. The reference signal is set at the required value and the feedback of the output voltage is taken out and compared and corrected using the PI then this is compared with the input side line voltages and a carrier signal which in all decides the switching frequency of the power switches. The output of the PI controller and the voltage and current sensors at the line side when multiplied produces a DC quantity which when compared with the triangular waveform decides the on time and off time of the IGBT.

As can be seen from the Figure 2 the output voltage and the input line side voltages are sensed using the voltage sensors. The compared output of the voltages and the PI controller output serve as the firing sequence of the converter switches to make it to work as a rectifier and in turn also control the power factor of the line side by optimizing the switching sequence. The firing is in the form of PWMs obtained from the controller.

IV. Mathematical Model Of Converter

The converter mathematical model is derived from the gating signals generator system (switching functions), and relates the rectifier input currents with the dc bus voltage. The derived model allows the design of the control that keeps the dc voltage constant and balanced.

The positive and negative current that flows through the rectifier dc bus is defined by the following equations:

$$i_p = S_{ap} \cdot i_a + S_{bp} \cdot i_b + S_{cp} \cdot i_c \quad (1)$$

$$i_n = S_{an} \cdot i_a + S_{bn} \cdot i_b + S_{cn} \cdot i_c \quad (2)$$

Where S_{ap}, S_{bp}, S_{cp}, S_{an}, S_{bn}, and S_{cn} are the rectifier switching functions for the positive (e.g. T_{a1}, T_{a2}) and negative (e.g. T_{a3}, T_{a4}) switches. The relation between the rectifier input line voltages and the voltages across each electrolytic capacitor are defined by:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} S_{abp} & S_{abn} \\ S_{bcp} & S_{bcn} \\ S_{cap} & S_{can} \end{bmatrix} \cdot \begin{pmatrix} V_p \\ V_n \end{pmatrix} \quad (3)$$

Assume Vo1 and Vo2 as Vpn and Vcn respectively, assume Co1, Ro1, Co2 & Ro2 as Cp, Rp, Cn & Rn respectively and Io has two components i_n and i_p negative and positive load currents respectively. Also assume the pole voltages Vao, Vbo and Vco, the neutral point current i_o is also assumed. So the following relations can be derived,

$$V_p - V_n = V_{dc} \quad (4)$$

$$V_p + V_n = 2 \cdot \Delta V_{dc} \quad (5)$$

Replacing (4), (5) in (3) we get,

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} S_{abp} - S_{abn} \\ S_{bcp} - S_{bcn} \\ S_{cap} - S_{can} \end{bmatrix} \cdot \frac{V_{dc}}{2} + \begin{bmatrix} S_{abp} + S_{abn} \\ S_{bcp} + S_{bcn} \\ S_{cap} + S_{can} \end{bmatrix} \cdot \Delta V_{dc} \quad (6)$$

Also we can get the total negative and positive dc bus currents as summation of the capacitor current and the current flowing through the load,

$$i_n = C_n \frac{dV_n}{dt} + \frac{V_n}{R_n} \quad (7)$$

$$i_p = C_p \frac{dV_p}{dt} + \frac{V_p}{R_n} \quad (8)$$

But Cn = Cp = C and the neutral current, i_o, is equal to in+ip. The equations that relate the system line voltages with the converter input currents and dc voltages are:

$$\begin{bmatrix} V_{abs} \\ V_{bcs} \\ V_{cas} \end{bmatrix} = L \cdot \begin{bmatrix} \frac{d(i_a - i_b)}{dt} \\ \frac{d(i_b - i_c)}{dt} \\ \frac{d(i_c - i_a)}{dt} \end{bmatrix} + \begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} \quad (9)$$

By replacing (9) in (6) the final sets of equations that represent the mathematical model of the front-end rectifier in *abc* reference frame are obtained.

$$\frac{d(i_m)}{dt} = \frac{1}{3L} \cdot V_s - \frac{1}{3L} S \frac{V_{dc}}{2} - \frac{1}{3L} S_{cp} \Delta V_{dc} \quad (10)$$

$$\frac{d(V_{dc})}{dt} = \frac{1}{C} S^T \cdot i_{sn} - \frac{V_{dc}}{2C}\left(\frac{1}{R_p} + \frac{1}{R_c}\right) - \Delta V_{dc} \quad (11)$$

$$\frac{d(\Delta V_{dc})}{dt} = \frac{1}{2C} S_{cp}^T \cdot i_{sc} + \frac{V_{dc}}{4C}\left(\frac{1}{R_n} - \frac{1}{R_p}\right) - \frac{\Delta V_{dc}}{2C}\left(\frac{1}{R_p} + \frac{1}{R_n}\right) \quad (12)$$

The switching function matrices *S* and *Snp* are derived from the gating signals generator block that contains the sinusoidal reference signal and the two triangular carrier waveforms, as shown in Figure 3. The derivation of the two switching functions is obtained from the intersection of the two signals.

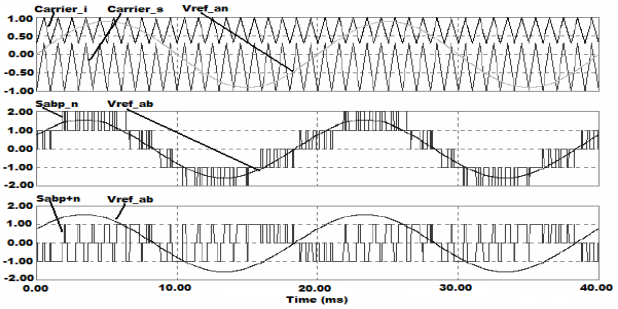

Figure 3 Line to line switching functions for the three-level active front-end rectifier, Sab and Snp. (a) Sinusoidal reference waveform, Vref_an, and triangular carrier waveforms, Carrier_s and Carrier_i. (b) Rectifier line to line switching function S. (c) Rectifier line to neutral switching function Snp.

The active front-end rectifier operates with two switching functions: *S* which defines the rectifier input voltage waveform, and *Snp* which is the one that has the information regarding the voltage unbalanced across the electrolytic capacitors. The mathematical functions that represent *Sap* and *San* have the following expression:

$$S_{ap}(t) = m \cdot \sin(\omega t) - d \quad (13)$$

$$S_{an}(t) = d - m \cdot \sin(\omega t) \quad (14)$$

Where *m* is the rectifier modulation index and *d* the unbalanced factor across the two electrolytic capacitors

(Figure.4). by using Fourier series, the expressions that define the rectifier switching functions *Sap*, *Sbp* and *Scp* are the following:

$$S_{ap} = \left\{\frac{1}{1-d}\left[\frac{m}{2} - \frac{m}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{d}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\right]\right\}\sin(\omega t)$$

$$S_{ap} = \left\{\frac{1}{1-d}\left[\frac{m}{2} - \frac{m}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{d}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\right]\right\}\sin\left(\omega t - \frac{2\Pi}{3}\right)$$

$$S_{ap} = \left\{\frac{1}{1-d}\left[\frac{m}{2} - \frac{m}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{d}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\right]\right\}\sin\left(\omega t + \frac{2\Pi}{3}\right) \quad (15)$$

Following the same procedure to obtain S_{an}, S_{bn}, and S_{cn}:

$$S_{ap} = \left\{\frac{1}{1+d}\left[\frac{m}{2} - \frac{m}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{d}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\right]\right\}\sin(\omega t)$$

$$S_{ap} = \left\{\frac{1}{1+d}\left[\frac{m}{2} - \frac{m}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{d}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\right]\right\}\sin\left(\omega t - \frac{2\Pi}{3}\right)$$

$$S_{ap} = \left\{\frac{1}{1+d}\left[\frac{m}{2} - \frac{m}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{d}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\right]\right\}\sin\left(\omega t + \frac{2\Pi}{3}\right) \quad (16)$$

Since,

$$S = \begin{bmatrix} S_{abp} - s_{abn} \\ S_{bcp} - s_{bcn} \\ S_{cap} - s_{can} \end{bmatrix} and \begin{bmatrix} S_{abp,n} = S_{ap,n} - s_{bp,n} \\ S_{bcp,n} = S_{bp,n} - s_{cp,n} \\ S_{cap,n} = S_{cp,n} - s_{ap,n} \end{bmatrix} \quad (17)$$

Finally,

$$S = \frac{\sqrt{3}}{1-d^2}\begin{bmatrix} \left[m - \frac{2dm}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{2d^2}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\sin\left(\omega t + \frac{\Pi}{6}\right)\right] \\ \left[m - \frac{2dm}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{2d^2}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\sin\left(\omega t - \frac{\Pi}{2}\right)\right] \\ \left[m - \frac{2dm}{\Pi}\sin^{-1}\left(\frac{d}{m}\right) - \frac{2d^2}{\Pi}\cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right)\sin\left(\omega t + \frac{5\Pi}{6}\right)\right] \end{bmatrix} \quad (18)$$

The transfer switching matrix *Snp* is defined by:

$$S_{np} = \begin{bmatrix} S_{abp} + S_{abn} \\ S_{bcp} + S_{bcn} \\ S_{cap} + S_{can} \end{bmatrix}$$

$$S_{np} = \frac{\sqrt{3}}{1-d^2} \begin{bmatrix} \left[dm - \frac{2m}{\Pi} \sin^{-1}\left(\frac{d}{m}\right) - \frac{2d}{\Pi} \cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right) \sin\left(\omega t + \frac{\Pi}{6}\right) \right] \\ \left[dm - \frac{2m}{\Pi} \sin^{-1}\left(\frac{d}{m}\right) - \frac{2d}{\Pi} \cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right) \sin\left(\omega t - \frac{\Pi}{2}\right) \right] \\ \left[dm - \frac{2m}{\Pi} \sin^{-1}\left(\frac{d}{m}\right) - \frac{2d}{\Pi} \cos\left(\sin^{-1}\left(\frac{d}{m}\right)\right) \sin\left(\omega t + \frac{5\Pi}{6}\right) \right] \end{bmatrix} \quad (19)$$

The set of equations (10), (11) and (12) can be simplified by using the Park's Transformation [8]. In the *dq* reference frame the converter equations are the following:

$$\frac{d[i_m]_{dq}}{dt} + W[i_m]_{dq} = \frac{1}{3L}[V_s]_{dq} - \frac{1}{6L}[S]_{dq} V_{dc} - \frac{1}{3L}[S_{np}]_{dq} \Delta V_{dc}$$

$$\frac{d}{dt}(V_{dc}) = \frac{1}{C} S_{dq}^T [i_{sn}]_{dq} - \frac{V_{dc}}{2C}\left(\frac{R_p + R_n}{R_p \cdot R_n}\right) - \frac{\Delta V_{dc}}{C}\left(\frac{R_p - R_n}{R_p \cdot R_n}\right)$$

$$\frac{d(\Delta V_{dc})}{dt} = \frac{1}{2C}[S]_{dq}^T [i_{sc}]_{dq} + \frac{V_{dc}}{4C}\left(\frac{R_p - R_n}{R_p \cdot R_n}\right) - \frac{\Delta V_{dc}}{2C}\left(\frac{R_p + R_n}{R_p \cdot R_n}\right) \quad (20)$$

Here,

$$W = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}$$

And ω = 2πf.

V. Hardware Implementation And Results

The performance of the proposed control strategy and the three-phase diode clamped active front-end converter topology has been verified by the hardware results. The mains line-line voltages are taken at 415V rms with a supply frequency of 50Hz. After following the design steps the capacitance of the two DC link capacitors was taken as 4700μF each and the boost inductance for each line was taken as 5.3 mH. A switching frequency was 5 kHz. The proposed converter was designed for a load of 10 kW power rating. The total desired DC link was set at 800 V. The waveforms for the phase voltages and the line currents of the converter in the rectification mode are shown in Figure 4. The % THD of the line current is very much within the admissible limits. This is a highly desirable feature of a high power factor converter. Figure 5 depicts the waveforms of the DC link voltage and ripple in DC link voltage for the upper capacitor bank Co1 in the rectification mode. Figure 6 depicts the waveforms of the DC link voltage and ripple in DC link voltage for the lower capacitor bank Co2 in the rectification mode. Figure 7 shows the complete DC link output at no load and figure 8 shows the complete DC link output at 10 kW load. The DC output ripple in any case of loading remains within the maximum allowable limit of ± 20V. The input power factor during both the cases remains close to unity. During both the cases the DC link across the both capacitors remains balanced. Thus the proposed control strategy of the converter balances the DC bus capacitor voltages under all the conditions of load and also improves the power quality.

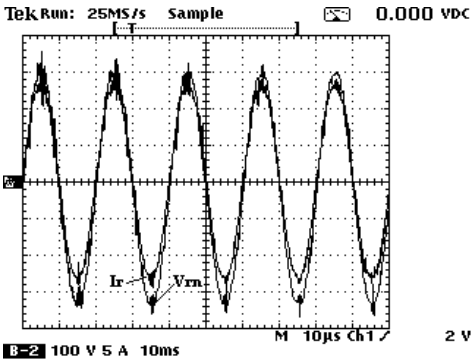

Figure 4 Phase voltage and Line current in rectification mode

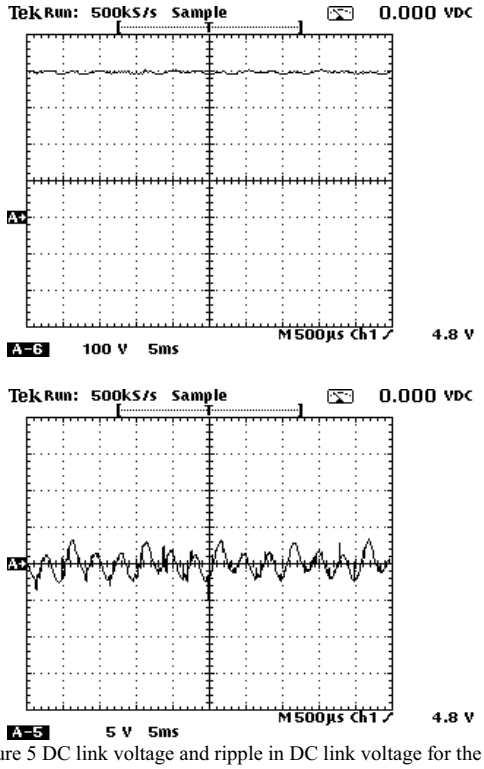

Figure 5 DC link voltage and ripple in DC link voltage for the upper capacitor bank Co1

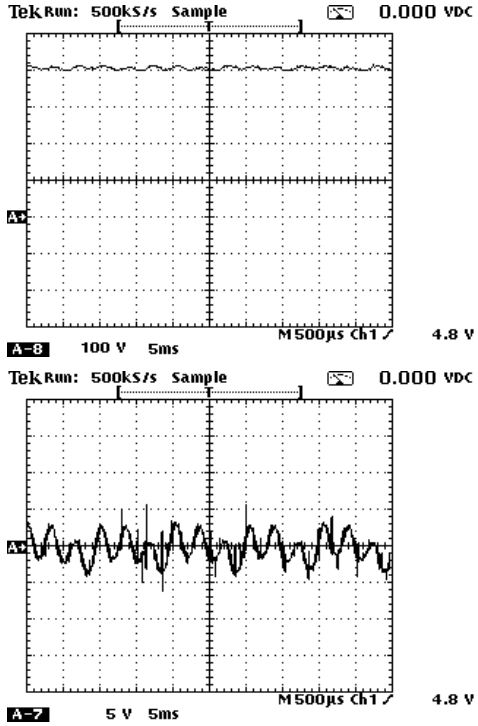

Figure 6 DC link voltage and ripple in DC link voltage for the lower capacitor bank Co2

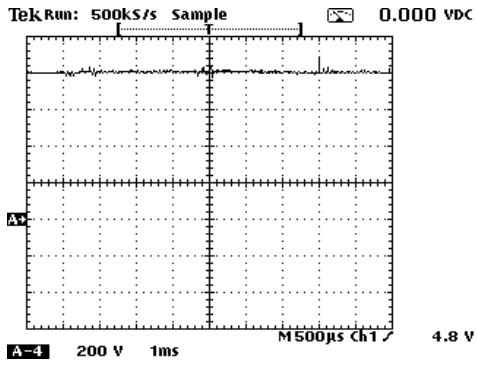

Figure 7 Complete DC link voltage with no load

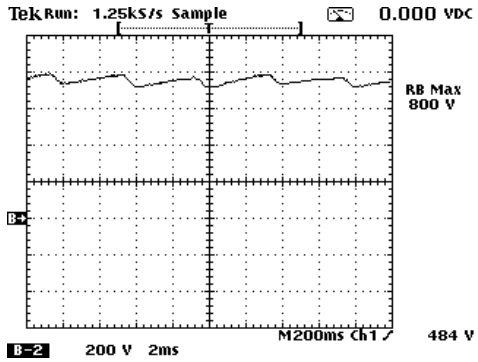

Figure 8 Complete DC link with 10 kW load

VI. CONCLUSION

A three-phase neutral point clamped active front-end converter is proposed to achieve sinusoidal supply currents with nearly unity input line power factor, well regulated and balanced dc link voltage at the output with capacitor voltage balancing. the proposed control strategy was based on the capacitor balancing technique and in turn also maintaining near to unity power factor. The main objective fulfilled from the results is that by achieving near to unity power factor the switching losses reduces and the conversion efficiency of the converter increases. The converter is highly suitable for medium voltage and medium power industrial applications. the converter does not allow the harmonics and reactive power to flow in the system. This converter does not pose any problem for the critical instruments and apparatus used in critical applications like the ones used in medical field (i.e. in hospitals) and connected to the system. Thus the proposed converter is a useful power quality improvement converter suitable for various types of applications including domestic, commercial and industrial applications. The control topology of the converter is implemented on the DSP (Digital Signal Processor) TMS320F240 which shows the reliablity and flexibility in the system. The converter has been operated for a 10 kW load and the DC link has been set at 800 V with a ripple of $\pm$ 20 V which is $\pm$ 5 % of the DC link which is well under admissible limits.

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