# Design and Fabrication of High Efficiency ZVT Boost Converter for Power Amplifiers

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Abstract— This paper describes the detailed design of High Efficiency DC-DC ZVT Boost converter with 115 W output power. This can be used as a preregulator to any half bridge or full bridge SMPS designed for power amplifiers. The converter consists of current mode control. The operation of this converter is carried out at high switching frequency. This high switching frequency is necessary to reduce size and weight of DC-DC converter. However this yields high switching losses consequently low efficiency in hard switching. ZVS quasiresonant converters which are designed to reduce switching losses, but the reduction of switching losses in these converters results in conduction losses by increase in voltage and current stress of switches. So zero voltage transition technique in boost converter is opted here, which gives minimum semiconductor stress and low losses. In order to increase the efficiency of the power supply and reduce un-acceptable switching losses in the power devices, this zero voltage transition boost converter can be used as a preregulator to any SMPS. This paper briefly touches upon the design steps, detailed derivations of design equations, observed waveforms and efficiency results for ZVT boost converter. This High efficiency Converter can also be used for firing Gallium Arsenide FETs of Solid state power amplifiers used in space applications.

*Index terms*— DC to DC Converters, Zero Voltage Transition (ZVT), Boost converter, Current Control mode.

#### I. INTRODUCTION

LECTRONIC CIRCUITS utilize dc power for its operation. **L**Requirements of DC voltages depend upon type of active devices, family of Integrated Circuits and the other components used in the equipments. All electronic equipments, whether designed for satellite, home appliances or industrial applications, invariably require DC supply with more than one voltage level and in both positive and negative polarity. Latest digital devices like microprocessors, FPGA, ASICs Digital signal processing ICs typically need +1.8, +2.5, +3.3 or +5.0 volts. TTL, CMOS and many Analog ICs are frequently operated with +5.0 Volts, while the ECL devices are operated at -5 volts. Gallium Arsenide FETs used in the microwave Amplifiers are biased by using either +8.0, -5.0 volts, or +3.5 and -3.5 volts. +12, -12, +15, -15 and +24 volts supply are also often used in the electronic circuits with MOSFETs, relay in industrial control etc. Thus, power supply with vast variety of DC voltage levels and with current requirement commensurate with the complexity of the functions to be performed is required.

# II. BLOCK DIAGRAM AND CONTROL STRATEGY

The proposed block diagram and control strategy of the converter topology is shown in the Figure 1 below.

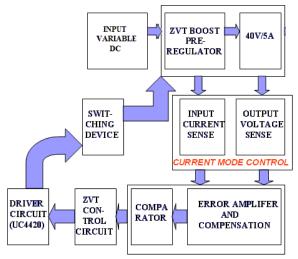


Figure. 1 Block Diagram and Control strategy of Proposed Converter

In order to improve efficiency of the power converter it is required to reduce switching losses. The dynamic losses of the switching semi-conductors at higher operating frequencies and elevated input voltages are excessive. The switching losses can be reduced by using snubbers, quasi or fully resonant techniques or soft – switching (Zero Voltage Transitions) circuits. As shown in figure.1 ZVT technique is used adopted here in conventional boost converter to enhance its efficiency.

### III. INTRODUCTION TO ZVT BOOST CONVERTER

Zero Voltage Transition technique is introduced in conventional boost converter by connecting a resonant inductor, Lr, auxiliary switch,  $M_2$  and a capacitor, C in parallel of main switch  $M_1$ .Other ZVT circuit includes  $D_r$ ,  $D_a$ ,  $D_c$ ,  $C_b$ ,  $D_{rr}$  and  $C_{rr}$  as shown in Figure.2. Unlike simple boost converter, the performance of ZVT Boost Converter is divided into six stages shown in Figure.3.

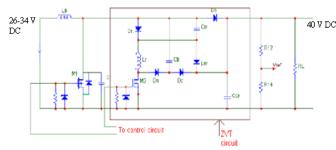
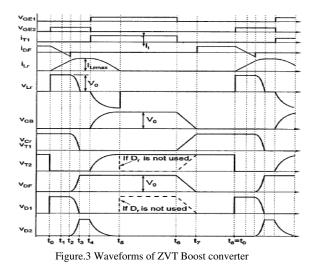


Figure. 2. Zero Voltage Transition Boost Converter Power Schematic



#### Stage 1

This stage begins with MOSFET  $M_1$  (main) and  $M_2$  (auxiliary) turned off.  $D_b$  is on and is conducting current  $I_{IN}$  of the main inductor  $L_b$ . The turn on signal is sent to MOSFET  $M_2$  from the control logic circuit at which time  $D_r$  and  $M_2$  are turned on at near ZCS. The ZVT inductor  $L_r$  limits the rate of rise of the current through  $D_r$  and  $M_2$ . As the current in  $M_2$  reaches  $I_{IN}$ ,  $D_b$  current falls to zero, and thus  $D_b$  turns off under ZVS.

## Stage 2

Diode  $D_b$  and MOSFET  $M_1$  are now both in the off state.At this stage,  $V_{Cr} = V_{out}$ . A parallel resonance between  $L_r$ and  $C_r$  begins to resonate through the path  $C_r-D_r-L_r-M_2$ under the input current  $I_{in}$  and with the initial current of  $I_{Lr}$  of the inductor  $L_r$ . When the transfer of energy stored in capacitor  $C_r$  to the inductor  $L_r$  is completed, and the current and energy values of the inductor  $L_r$  reach their maximum level at the same time. Now only MOSFET  $M_2$  is on and is conducting the maximum current of the inductor  $L_r$ . Also, the  $V_{Cr} = 0$ .

# Stage 3

MOSFET  $M_1$  receives a turn on signal and at the same time the turn on signal is removed from MOSFET  $M_2$ . So,  $M_1$  turns on under ZVS and conducts current  $I_{in}$  and  $M_2$ turns off under near ZVS through  $C_b$ . Serial resonance between  $L_r$  and  $C_b$  starts to resonate through  $L_r$ - $D_a$ - $C_b$ - $D_r$ under the maximum inductor current. Thus, throughout this stage the energy stored in the inductor  $L_r$  is transferred to capacitor  $C_b$ . As soon as the inductor current drops to zero, auxiliary diodes  $D_r$  and  $D_a$  are turned off under ZCS through  $L_r\!,$  and  $C_b$  is charged to  $V_o\!.$ 

#### Stage 4

MOSFET  $M_1$  continues to conduct input current  $I_{in}$ , and ZVT circuit is not active. The duration of this stage is the 'on' time of the MOSFET  $M_1$  as a traditional normally operating boost converter and is determined by PWM control. **Stage 5** 

The gate signal of the main MOSFET  $M_1$  is removed and  $M_1$  turns off under ZVS. Auxiliary diode  $D_c$  turns on with ZVS because of capacitor  $C_b$  being charged to  $V_o$ . During this stage  $C_r$  is charged and  $C_b$  is discharged. When  $C_r$  voltage reaches  $V_o$  and  $C_b$  goes to zero simultaneously, diode  $D_b$  is turned on with ZVS and the auxiliary diode  $D_c$  is turned off with ZVS. Thus,  $C_b$  restricts the rise rate of MOSFET  $M_1$  voltage and  $M_1$  is turned off under near ZVS. **Stage 6** 

Main diode  $D_b$  continues conducting the input current  $I_{in}$  and the snubber circuit is not active. This stages duration is the 'off' time of the MOSFET  $M_1$  as in a conventional PWM boost converter. At the end of stage 6, stage 1 would again begin starting another switching cycle.

# IV. DESIGN OF POWER STAGE OF ZVT BOOST CONVERTER

Selection of ZVT circuit components:-

The value of  $L_r$  can be calculated using the following equation:

$$\frac{V_0}{L_r} 3t_{rr} \le I_{in,\max}$$

(where  $t_{rr}$  represents the reverse recovery time of the main diode  $D_b$ .  $D_b$  is a Schottky diode 45CKQ100 with a very fast recovery time.)

$$\frac{V_0}{L_r} 3t_{rr} \le \frac{P}{V_{IN MIN}}$$
$$L_r \ge 416 nH$$

The value of  $C_b$  can be calculated using the following equation:

$$\frac{\pi}{2}\sqrt{L_r C_b} \ge t_{f2}$$

where  $t_{f2}$  represents the fall time of the auxiliary MOSFET M<sub>2</sub>.

$$\frac{\pi}{2}\sqrt{150nH} \times C_b \ge 10ns$$

$$C_b \ge 0.27 nF$$

Selected value for  $C_b$  is 1 nF in this circuit.

The value of  $C_r$  can be calculated using the following equation:

$$\frac{C_r + C_b}{I_{in,\max}} \times V_0 \ge t_{f1}$$

Where  $t_{f1}$  represents the fall time of the main MOSFET M<sub>1</sub>.

$$\frac{C_r + 1nF}{17A} \times 50 \ge 10ns$$

$$C_r \geq 2.4nF$$

These values of  $C_r$ ,  $C_b$ , and  $L_r$  also satisfy the following equation:

$$\frac{1}{2}L_r \left(I_{in,\max} + I_{rr,\max}\right)^2 + \frac{1}{2}C_r V_0^2 \cong \frac{1}{2}C_b V_0^2$$

#### V. CONTROL STAGE OF ZVT BOOST CONVERTER

The control logic is designed to get desired waveforms as shown in figure.2. Following circuit has been added to the control circuit designed for boost converter using PWM IC 1846.

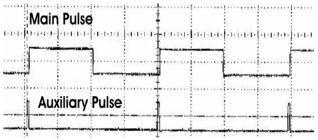


Figure.4 Waveforms of Control Logic for ZVT circuit

As shown in Figure.3, the output waveforms of control IC 1846 is given to monostable multivibrator IC CD4098 and NAND gate IC 4093. Then output of monostable multivibrator is given to NAND gate and to the gate drive of auxiliary MOSFET. Thus NAND IC 4093 performs the NAND logic with its two inputs and its output is given to the main MOSFET M1. The on time of the auxiliary MOSFET is set at 200 ns to ensure the MOSFET was conducting for a long enough period of time. The on time of main MOSFET was calculated using operation switching frequency, 100 KHz and a 50% duty cycle.

Gate waveforms obtained by this logic are shown in Figure.4 where main pulse is given to gate of main MOSFET and Auxiliary Pulse to gate of the Auxiliary MOSFET.

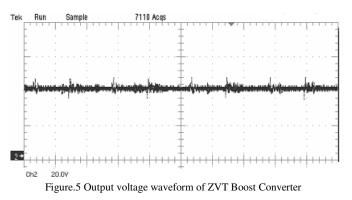
$$T_{OFF} = 0.5 \times T = 5 \,\mu s$$
  
 $T_{ON} = T_{MAIN} + T_{AUX} = 4.8 \,\mu s + 200 \,ns = 5 \,\mu s$ 

#### VI. CONCLUSION

The results of the ZVT Boost Converter operated with a resistive load is shown is tabulated in Table.1.

Vin	lin	Vo	Io	Efficiency(%)
26.3	4.49	40.217	2.87	97
28.1	4.19	40.231	2.873	98
30	3.91	40.261	2.875	98.6
32	3.66	40.277	2.876	98.9
34	3.44	40.297	2.878	98.9





The developed converter has 97% efficiency at 115 W output power. The ZVT circuit implementation in conventional Boost Converter reduces switching and conduction losses and this approach is a promising technology for designing high efficiency power converters with higher power output. Also the spikes and the noise associated with switching environment of power converter are mitigated.

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#### Note:

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