"DEVELOPMENT OF A POWER MODULE FOR SPACE QUALIFIED KLYSTRON TRANSMITTER"

A Major Project Report

Submitted in Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY

IN

ELECTRICAL ENGINEERING

(POWER APPARATUS & SYSTEMS)

By
ATUL GUPTA
(04MEE003)

Department of Electrical Engineering
INSTITUTE OF TECHNOLOGY
NIRMA UNIVERSITY OF SCIENCE & TECHNOLOGY,
AHMEDABAD 382 481

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CERTIFICATE

This is to certify that the Major Project Report entitled "**Development of A Power Module for Space Qualified Klystron Transmitter**," submitted by **Mr. Atul Gupta (04MEE003)**, towards the partial fulfillment of the requirements for **Master of Technology** (Electrical Engineering) in the field of **Power Apparatus & Systems** of **Nirma University of Science and Technology** is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

Date:

Project Guide:

Mr. C.R.Patel
Lecturer,
Department of
Institute of Technology,
Nirma University, Ahmedabad

HOD
Department of Electrical Engineering
Institute of Technology
Nirma University, Ahmedabad

Director
Institute of Technology
Nirma University, Ahmedabad

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Atul Gupta

ABSTRACT

This project aims for the design, simulation, fabrication & testing of a compact DC-DC converter. This DC-DC converter may be a resonant converter or it can be a simple full bridge type. This high voltage DC-DC converter is used for Missile application so weight and the area of this converter should be optimum. High voltage DC-DC converter is usually used in different types of electronic equipments. Typical examples are telecommunication equipments with vacuum tubes (TWT), industrial application and space applications.

The heart of this converter is a high frequency transformer, which plays a vital role for designing of DC-DC converter. The design of high-voltage DC-DC converters is challenging because the large turn ratio of the transformer exacerbates the transformer non-idealities. In particular the leakage inductance and the winding capacitance can significantly change converter behavior. So, all the parasitic components are taken into account while selecting the converter topology.

To fulfill the requirement of the project specification there are many converter topologies. But the prime importance is to select the best topology in the sense of robustness and optimum size.

In the given time period of 10 months, simulation, fabrication and testing of DC-DC full bridge converter for space qualified Klystron Tube is done.

Transformer is designed for the given specifications. Transformer on 'C' core is fabricated. Results with 'C' core transformer matched with the required specifications. Primary and secondary waveforms for this transformer are analyzed with full bridge type DC-DC converter.

Open loop and close loop operation of full bridge converter are tested successfully. Over all system stability is analyzed for the required limits.

LIST OF FIGURES

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NOMENCLATURE

SYMBOL

E_{AV}	=	Average voltage across transformer
V_o	=	Voltage across the filter capacitor
V_{om}	=	Voltage across the transformer secondary developed
N_p	=	Number of turns in transformer primary winding
N_s	=	Number of turns in transformer secondary winding
P_o	=	Peak Power Output
I_p	=	Transformer primary current
I_s	=	Transformer Secondary current
l	=	Magnetic path length in cm.
μ_e	=	Permeability
A	=	Area of cores in
L_p	=	Primary inductance
L_s	=	Secondary inductance
ΔV	=	Voltage Ripple
Q	=	Total charge stored by capacitor
P_c	=	Conduction losses in IGBT
P_b	=	Blocking losses in IGBT
P_s	=	Switching losses in IGBT
t_r	=	Rise time during switch on
t_{off}	=	Total off time during switch off
t_f	=	Fall time during off condition

ABBREVIATONS

AC – Alternating current

DC – Direct current

EMI – Electromagnetic interference

TWT- Traveling Wave Tube

CCM - Continuous conduction mode

ZVS – Zero voltage switching

ZCS – Zero current switching

HV - High voltage

BJT – Bipolar junction transistor

IGBT – Insulated gate bipolar transistor

PWM – Pulse width modulation

RFI – Radio frequency interference

SCR – Silicon controlled rectifier

SMPS - Switch Mode Power Supplies

UPS – Uninterruptible power supply

CONTENTS

CHAPTER 1 INTRODUCTION

1.1 OVERVIEW OF PROJECT

The project "**Development of a Power Module for Space Qualified Klystron Transmitter**" is a project considering the design, simulation, and fabrication & testing of the compact DC-DC converter for space application. In this project a 48 V DC is to be converted into a 6 kV DC. The specifications of this converter are:

- Input Voltage : 48 ± 4 V DC
- Output Voltage : 6 KV DC
- Peak Output Power : 1600 W
- Average Output Power : 550 W
- Efficiency : >90%
- Switching Frequency : 60-500 KHz

A converter is a basic module (building block) in power electronic systems. It utilizes power semiconductor devices controlled by signal electronics (integrated circuits) and possibly energy storage elements such as inductors and capacitors.

Converter as a generic term refers to a single power conversion stage that can perform any of the functions listed above. Basic DC-DC converter takes unregulated dc input as an input and gives regulated dc voltage as an output. Output voltage is fed back to the control circuit that adjusts gate pulses or width of gate pulses to get regulated output. Generally converter consists of power electronic switches, which turned ON and turned OFF by gate drive pulses. MOSFETS, power BJTs and IGBTS are widely used as power electronic switches as they are self-commutating devices and do not require auxiliary commutating circuits. Output voltage is regulated by adjusting turn ON and turns OFF time given to these switches. Selection of proper switch is done by their characteristics and requirements.

High voltage dc-dc converters are usually used in very different types of electronic equipments. Typical examples are telecommunication equipments with vacuum tubes (TWT), industrial application and space applications.

There are number of topologies available for dc-dc converters. The prime emphasis is to select the suitable topology in the sense of robustness, high efficiency and optimum weight.

Topology comprises either of a single stage or a double stage power conversion. The compact design considers all the aspects like cost, weight, and easy operation. The heart of this converter is a high frequency transformer, which plays a vital roll for designing of DC-DC converter.

This specific task as a one year M.Tech thesis has been done in "central Electronics Engineering Research Institute", Pilani (Rajasthan).as per the topology concern a full bridge converter topology is selected for this task. Besides this topology a number of schemes are reviewed and literature was surveyed. All the facilities regarding converter simulation, fabrication, & testing are provided by CEERI, Pilani. The bloke diagram of full bridge converter is shown in Figure 1.1

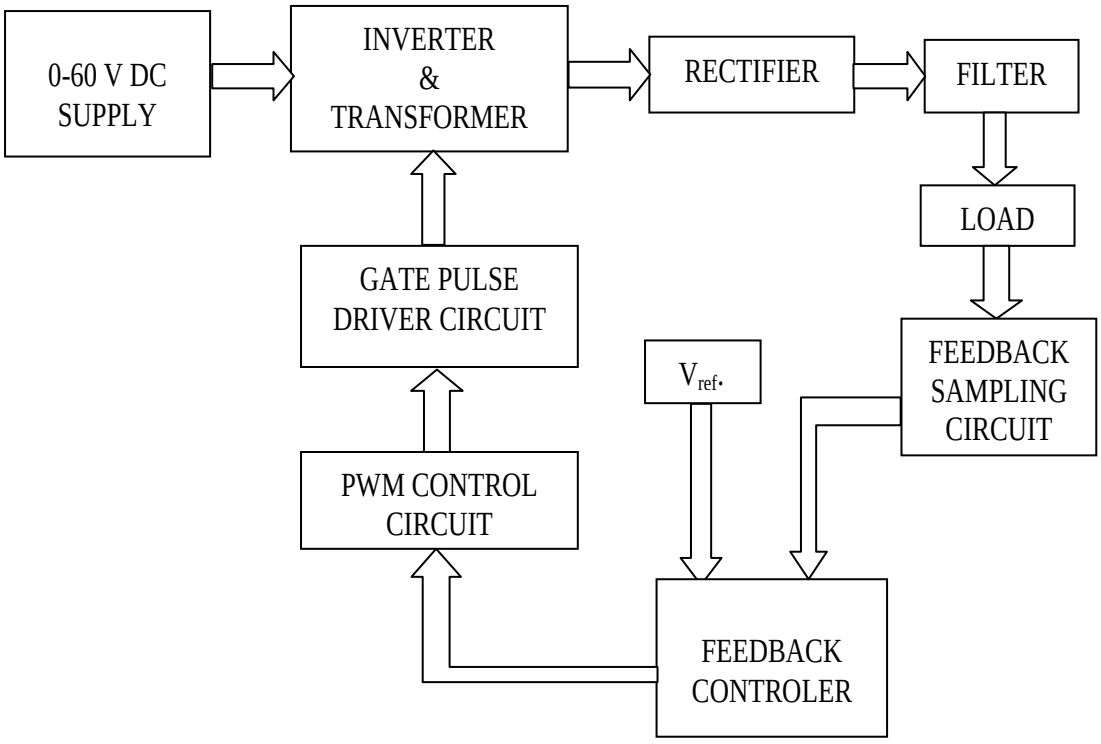

Figure 1.1: Block Diagram of DC-DC Converter

1.2 INTRODUCTION TO CEERI

Central Electronics Engineering Research Institute (CEERI), Pilani, is a pioneer Research Institute in the Country and a laboratory of Council of Scientific and Industrial Research (CSIR), New Delhi, established in 1953, for advanced Research and Development (R&D) in the field of Electronics. Since its inception it has been working for the growth of electronics in the country and has established the required infrastructure and well experienced manpower for undertaking R&D in the following areas:

- MEMS & Micro sensors
- Electron Tubes
- Photonic Components & Subsystems
- Electronics for Society, Environment & Industry

1.2.1 Major R&D Programs

The major R&D programs of CEERI can be categorized into three major areas; microwave tubes, semiconductor devices and electronics systems. In the area of microwave tubes the major focus is on communication tubes and industrial tubes. In the area of semiconductor devices, projects are being actively pursued on IC design, power devices, device processing, microwave devices, hybrid microchips, opto-electronic devices and semi-conductor materials. R&D work in the area of electronics systems is focused on digital systems, agro-electronics, speech technology, industrial electronics, instrumentation systems and communication engineering. Some of the current projects related to:

- Development of PC-based monitoring system for withering process in tea industry
- Development of InGaAs / InP PIN detectors
- Development of hybrid PIN/FET receivers for 140 M bit/s data rates
- Development of some sub-assemblies of G&P matched mini TWT
- ASIC design of advanced architecture microprocessor chip

1.2.2 Significant Achievements

- Design of space qualified hybrid microcircuits for use by ISRO.
- Design of serial data controller chip.
- Design of high voltage deflection transistor for TV applications.
- Development of hybrid PIN / FET for long haul optical communication system.
- Development of 30 W (CW) TWT, 2MW S-band magnetron, high current density cathodes.
- EPLD / FPGA-based design of decoder for digital TV.
- Development of laboratory model of 2 x 35 kVA DC drive for mining loco.
- Development of laboratory prototype of 'Electric Vehicle".

1.2.3 Major Technologies Transferred to Industry

- S-band, 30W TWT (BEL, Bangalore)
- 500 VA UPS (Shakti Electronics, Jaipur)
- 75 KW energy efficient DC drive for mining locomotives
- 50 KVA unity power factor converter
- Zirconia oxygen analyzer (EMP Controls Pvt. Ltd, Bombay)

1.2.4 Specialization of Industrial Electronics Group

- 150 KVA single phase to three phase converter for electric locomotive.
- 40 KVA AC motor drive for mining locomotive.
- 7.5 KVA power supply for 5 mw klystron tube.
- 75 KW dc motor drive for mining locomotive.
- Integrated position control system using brushless dc motor.
- Excitation control system for diesel electric locomotive.
- Technology for energy efficient electric vehicle.
- Development of PWM amplifier and electronics for electromechanical actuator.
- Speed indicating and recording instruments for locomotives.
- Unity power factor converter.
- Low power uninterruptible power supplies.

1.3 LITERATURE SURVEY

In the literature survey several topologies are included and described their suitability regarding the converter specifications. The topology may be a single stage or a double stage power conversion. In each topology the most important part is a high frequency transformer, which plays a vital role for designing of DC-DC converter. The nature of this transformer depends upon the application. Since the output voltage is high, so, a step-up transformer is used in topology. The compact design of a converter considers all the aspects like cost, weight, and easy operation.

1.3.1 Double Stage Power Conversion

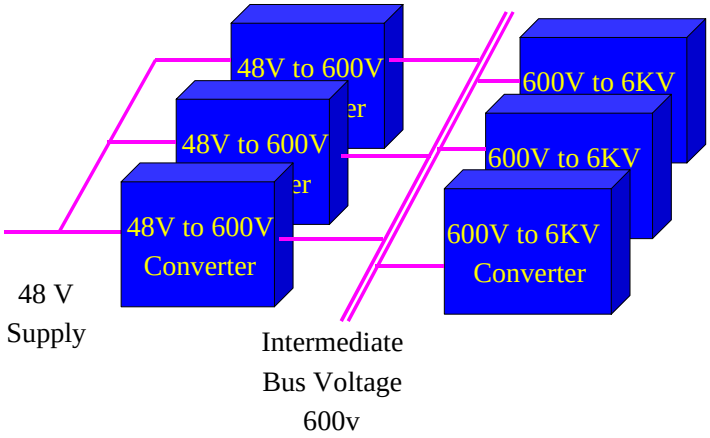

Figure 1.2: A Double-Stage High Voltage DC-DC Converter

A battery supplies 48 V to the input of front-end converter. In addition, the front-end converter regulates the intermediate bus voltage to 600 V whereas the load converter changes this 600 V to about 6 KV.

The system specifications do not require the isolation between the input side and the output side of the front-end converter, so, use of the transformer based converter would not be a good solution unless effect of the isolated converter to the power density is studied. Several non-isolated and isolated topologies are there. In order to select suitable topology, advantages and the limitations of each converter topology is carefully taken into account.

1.3.2 Non-Isolated Topologies

The single boost converter has been reported to be applicable in this application. According to system specifications, the converter has to step-up 48 V of the input voltage to 600 V of the regulated intermediate bus voltage where the DC voltage gain becomes 12 to 15. In order to provide such a large DC gain, the conventional boost converter has to operate under quite large duty cycle over 0.95. Also, considering the large input current the boost converter needs to work in the continuous conduction mode (CCM) to reduce the current stress of the main switch and the output rectifier.

Drawbacks

- The boost converter experiences severe reverse recovery problem at the output rectifier.
- The main switch causes less efficiency due to increased switching loss.
- The conduction loss of the main switch is very large because the high voltage-rating device has large on-resistance.
- The output rectifier would not function properly due to the very short turn-on period. If no soft switching technique is applied to the conventional boost converter, the switching frequency is limited to several kHz to reduce the switching loss. Accordingly, the size of the passive components such as input inductor and output capacitor would be bulky, causing power density to be reduced.

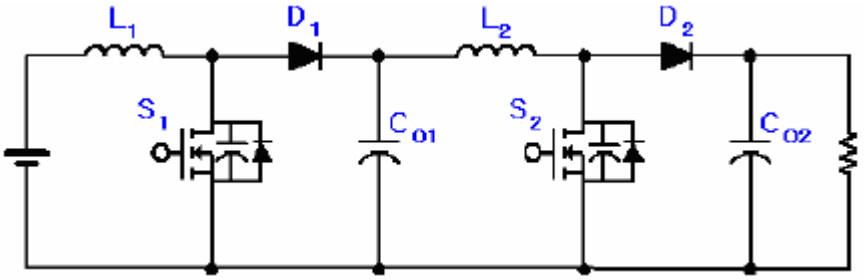

Figure 1.3: Cascaded Boost Converters

In order to avoid some aforementioned problems, a cascaded boost converter is presented as shown in Figure 1.3. Here the intermediate bus voltage is established between two stages and two series connected converters share the large voltage ratio. As shown in Figure 1.3. This structure can solve the large duty cycle problem. Also, the lower voltage rating MOSFET and diode can be placed in the first stage converter resulting in the reduced conduction loss and reverse recovery related loss.

However, the reverse recovery problem still exists in the secondary stage converter, which prevents the switching frequency from being increased. As a result, the passive component volume will be increased. In addition, the total efficiency would be lower because the power processing occurs two times in the cascaded converters. The control scheme also would be complex. A non-isolated boost converter would be another option for the front-end converter. The three-level boost converter shown in Figure 1.4 has been successfully employed.

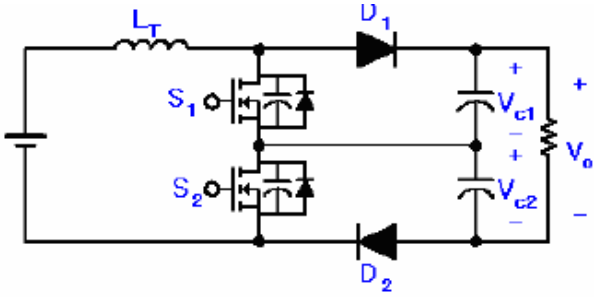

Figure 1.4: 3-Level Boost Converter

By using a three-level structure, the converter can obtain some advantages over the conventional boost converter. Firstly, the voltage stress of the switches and the rectifiers become half of the output voltage. Hence, the low voltage rating MOSFET and diode can be utilized to reduce the conduction loss.

At the same time, the reverse recovery related loss could be reduced when the low voltage rating diode is applied for the rectifier. Furthermore, the current ripple frequency through the input inductor becomes two times higher than the switching frequency, which enables the size of the input inductor to be shrunk.

1.3.3 Isolated Topologies

This subsection covers the isolated converters for the front-end converter. The isolated converter is basically derived from the boost converter although there are converters, which cannot be classified into the boost converter.

Figure 1.5 shows the basic isolated bridge-type boost converter. In the conventional boost converter, a transformer is introduced between the main switch and the output rectifier. Then, the single switch is replaced with the full-bridge configuration. Also, the secondary side of the transformer has the full-wave rectifier configuration in place of the single output rectifier.

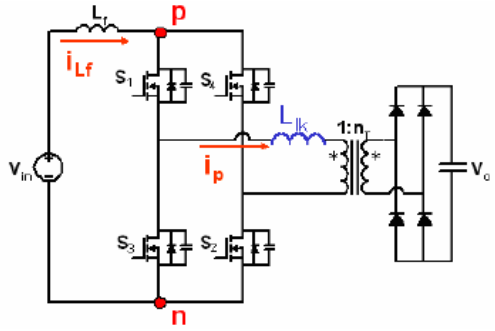

Figure 1.5: Full Bridge-Type Boost Converter

In the dc-dc converter, it is desirable to minimize the leakage inductances of primary and secondary by providing a tight magnetic coupling between the two windings. The energy associated with the leakage inductances has to be absorbed by the switching elements and their snubber circuits, thus clearly indicating a need to minimize the leakage inductances. Similarly, in a switch mode dc-dc converter, it is desirable to make the magnetizing inductance L_m as high as possible to minimize the magnetizing current i_m that flows through the switches and thus increases their current ratings.

1.3.4 Single Stage Power Conversion

The design of high-voltage dc-to-dc converters is challenging because the large turn ratio of the transformer exacerbates the transformer non-idealities. In particular the leakage inductance and the winding capacitance can significantly change converter behavior. In switched-mode converters the leakage inductance causes undesirable voltage spikes, which can damage circuit components, and the winding capacitance results in current spikes and slow rise times. Both non-idealities can lead to greatly increased switching and snubber losses and reduced converter efficiency and reliability. Because of their tolerance of transformer non-idealities, resonant converters appear well suited to high-voltage applications.

A resonant converter is defined as a power conditioning system that utilizes a resonant LC circuit as a part of the power conversion process. All resonant converters operate in essentially the same way as a square pulse of voltage or current is generated by the power switches and this is applied to a resonant circuit. Energy circulates in the resonant circuit and some or all of it is then tapped off to supply the output.

1.3.5 Resonant Converter

With the earliest switched-mode power converters, higher frequencies allowed smaller L's and C's and these resulted to smaller, lighter, and less costly systems. Moving to higher frequencies results in greater susceptibility to parasitic capacitance, leakage inductance, greater stress in the switching devices and increased EMI and RFI.

A resonant mode system offers the potential of achieving the benefits while sidestepping many of the disadvantages of higher frequencies. With a resonant circuit in the power path, the switches can be configured to operate at either zero current or voltage points in the waveform, greatly reducing their stress levels; the resonant sine wave minimizes higher frequency harmonics reducing noise levels; and since the circuit now requires inductance and capacitance, parasitic elements may enhance rather than detract from circuit performance. With these benefits, power systems operating in the range of 500 KHz to 2.0 MHz are now practical.

A full bridge isolated version of the parallel resonant converter is given in Figure 1.6. For this discussion, a 1:1 turn's ratio is assumed. The converter differs from the series resonant converter because it is the tank capacitor voltage, rather than the tank inductor current, which is rectified and filtered to produce the dc load voltage. A two-pole L-C low pass filter (LF and CF) performs this filter function.

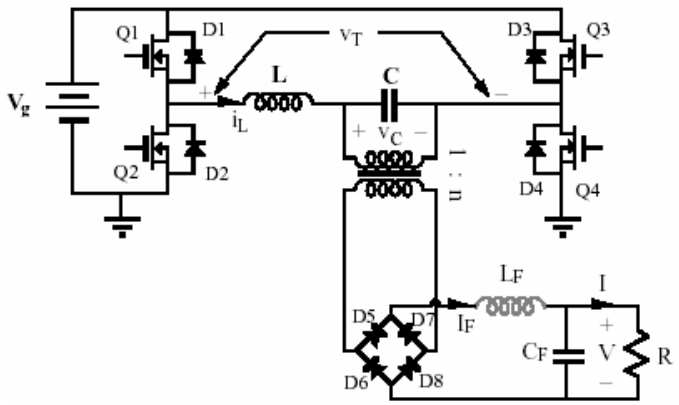

Figure 1.6: Full Bridge Realization of Parallel Resonant Converter

An attractive alternative for high-voltage dc-to-dc applications is the use of a resonant converter in which the transformer non-idealities are incorporated into the basic operation of the circuit. One can use the leakage inductance and winding capacitance partially or wholly as resonant tank elements, and thereby turn these non-idealities into useful articles. Such a converter should function efficiently and reliably.

1.3.6 Different Topologies

Different topologies are considered here from the IEEE journals and thesis reports:

1. High Efficiency High Step-Up DC-DC Converter. [1]

Features

- It uses diodes and coupled windings instead of active switches.
- It uses a low voltage rated single switch, so no isolation is required.
- High efficiency is achieved because the leakage energy is recycled and the output rectifier reverse-recovery problem is alleviated.
- The leakage inductor can be used to control the current decrease rate di /dt of the output rectifier.

2. 1 KW, 9KV DC-DC Converter Module With Time Sharing Control Of O/P Voltage And I/P Current. [2]

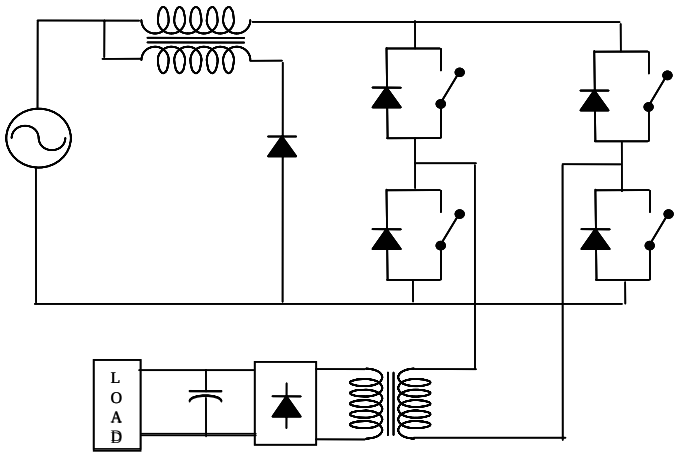

Figure 1.7: Basic Converter Scheme

Features

- A current source converter can perform both buck mode and boost mode allowing regulation of output voltage below and above the supply voltage.
- It is a current source converter using fly back diode.
- O/P voltage regulation is achieved by duty cycle control in powering phase.
- I/P current is controlled by proper selection of duration of fly back interval (in which inductor energy drops) and restore interval (where inductor energy rises).

Drawbacks

- Transformer parasitic can cause considerable problem.
- Leakage inductance can interfere with winding capacitance during restore operation, and they results in high freq oscillations, which may cause power consumption.

3. Auxiliary Series Resonant Converter: A New Converter for High-Voltage, High-Power Applications [4]

Features

- Converter is based on the series resonant converter using auxiliary switches.
- It maintains ZVS for both main and auxiliary circuit.
- Low EMI generated under all conditions.
- Fast and robust transient response with no output voltage overshoot or oscillations.

Drawbacks

- Transformer parasitic inductance and capacitance are very high.
- Overall cost of the converter increases due to increased number of switches.

4. A ZCS PWM Converter for High Voltage and High Power Application [3]

Features

- This converter makes use of parasitic components of HV transformer and rectifier diodes to implement ZCS operation.
- Rectifier diode at high voltage side operates with ZVS.
- The constant frequency phase shift control, make the converter attractive for high voltage and high power application.
- An output filtering inductor is not used on the HV side due to high voltage drop so the converter is current fed.

1.4 Klystron Operation

- Klystrons are microwave amplifiers based on vacuum electronic technology.
- The amplifying medium is a beam of electrons, which is constrained by a magnetic field.
- As the beam passes through the first (input) cavity, it experiences the input signal as an RF-frequency-varying electric field, which either accelerates or retards the electrons in the gap. The effect is velocity modulation.
- After passing through some intermediate cavities, the beam is demodulated and the amplified signal is output.
- The residual energy in the beam is dissipated in the collector.

1.4.1 Klystron Layout

Klystron word is derived from the Greek, meaning to wash or break over, such as waves breaking on a beach. As it is well known, waves break on a beach because they first lose their velocity and then give up their energy to the surroundings. The name contrasts favorably with the sister tube to the klystron which is Traveling Wave Tube (TWT).

In the klystron tube the main part is cathode which emits electrons which are focused through a hole in electrode to form a beam.

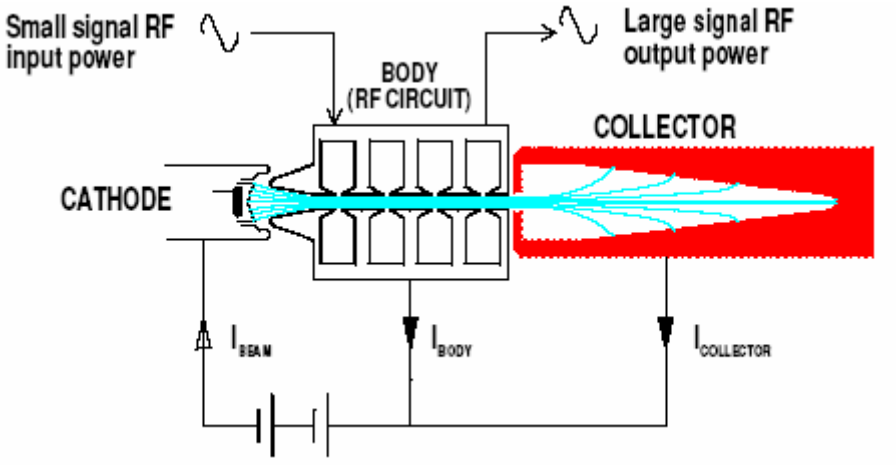

Figure 1.8: Basic Circuit of Klystron Tube

CHAPTER 2 SIMULATION RESULTS

To check the feasibility of the transformer, using the parameters Np, Ns, Ip, Is, simulation is done on SABER. These simulations are done in the ideal condition because, physical parameters of transformer like leakage inductances, winding capacitances; primary and secondary inductances, can not be defined until transformer is fabricated. Results of simulations for open loop configuration are shown in figure 2.2 to figure 2.5.

2.1 OPEN LOOP SIMULATION

A transformer as per specifications is simulated on the ***SABER*** software with full bridge converter. IGBTs are used as switching elements. The waveforms across primary and secondary coil of transformer are analyzed with resistive load. Transformer secondary voltage is rectified with full bridge rectifier and capacitive filter to get DC voltage at output. Load resistance is taken to be 100 kΩ. There is no arrangement for controlling the output voltage in this simulation. Switching frequency is selected 60 KHz. Pulse width is adjusted at maximum 45% of switching time.

2.1.1 Schematic Diagram of Full Bridge Converter

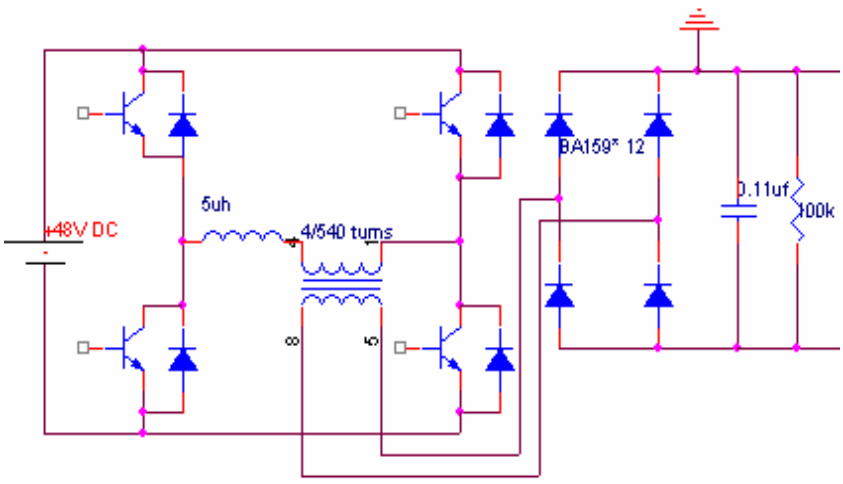

Figure 2.1: Realization of Open Loop Full Bridge Converter in SABER

2.1.2 Simulation Results

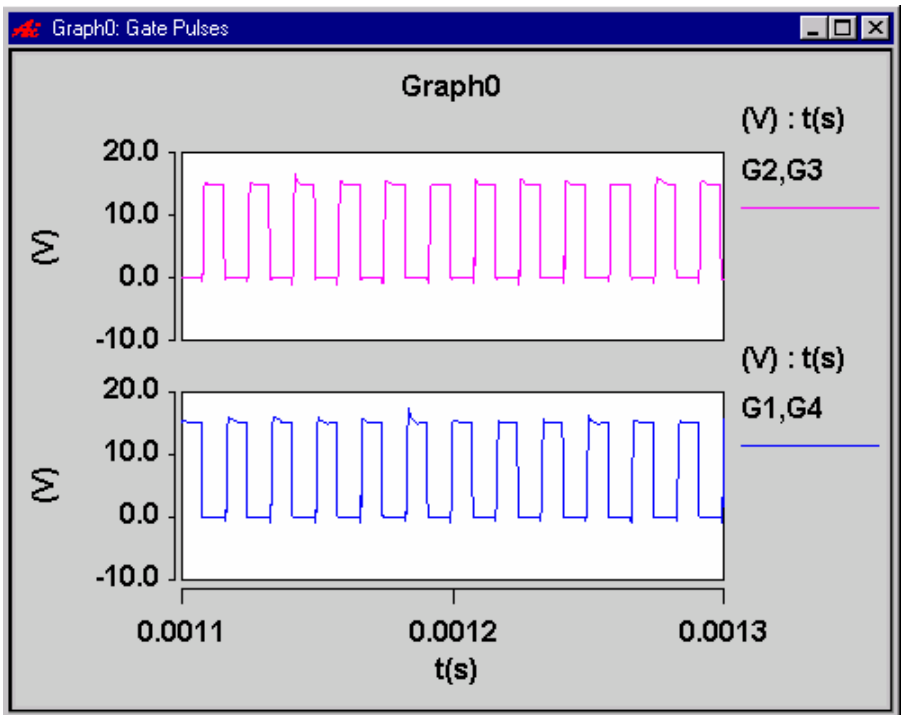

Figure 2.2: Gate Pulses of IGBTs for Open Loop DC-DC Converter

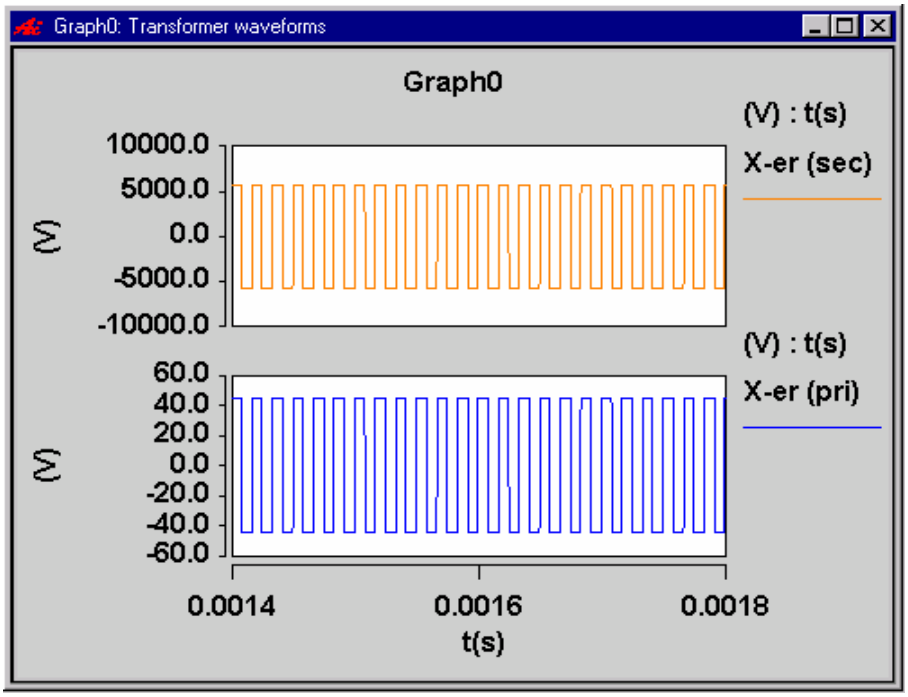

Figure 2.3: Output Waveform of Transformer for Open Loop Realization

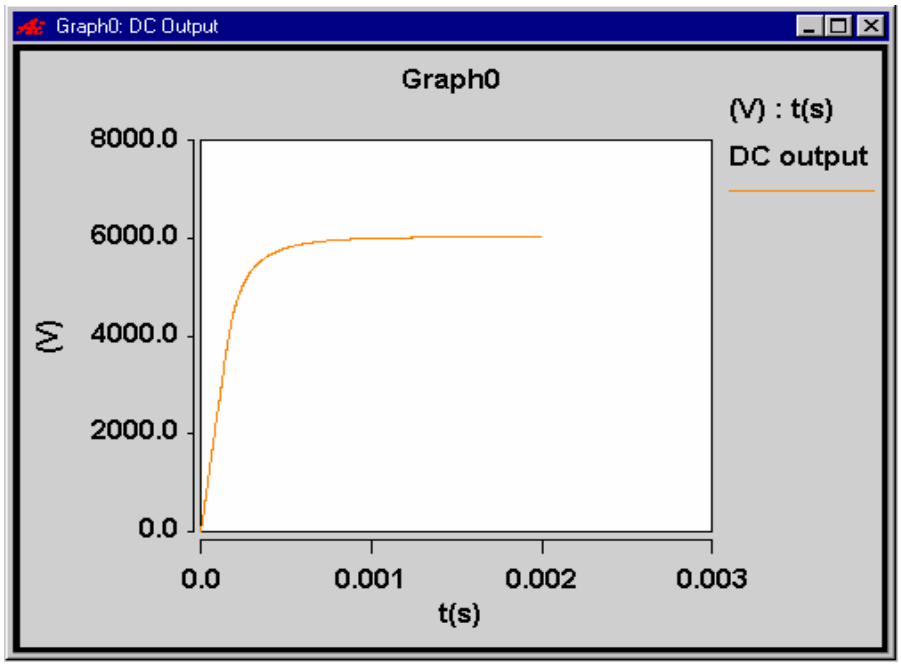

Figure 2.4: Open Loop Simulation Result with V_{out} = 6000 V

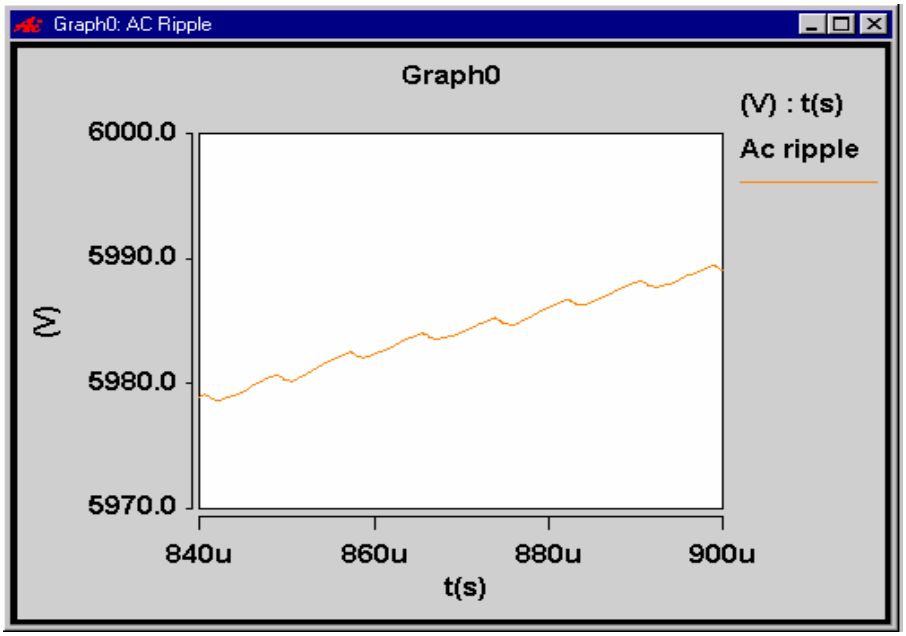

Figure 2.5: Ripple in Output DC

2.2 CLOSED LOOP STABILITY

A close loop system is designed and the system stability is checked. A sample from the output voltage is taken and this is given to the external Error amplifier where it is compared with the reference voltage. Block diagram of close loop system is shown in figure (2.6)

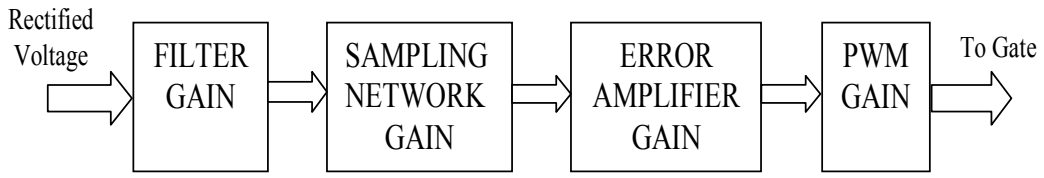

Figure 2.6: Block Diagram of Close Loop Circuit

2.2.1 Conditions for the Stable System

For any stable circuit, following conditions should be fulfilled:

1. Phase margin should be at least 45°.
2. To prevent rapid changes of phase shift with frequency characteristic of a circuit, with a –2 gain slope, the slope of the open loop gain-frequency curve crossover frequency should be –1.
3. Overall close loop system is stable only if the total system gain is stable.

2.2.2 Gain Characteristic of Output LC Filter

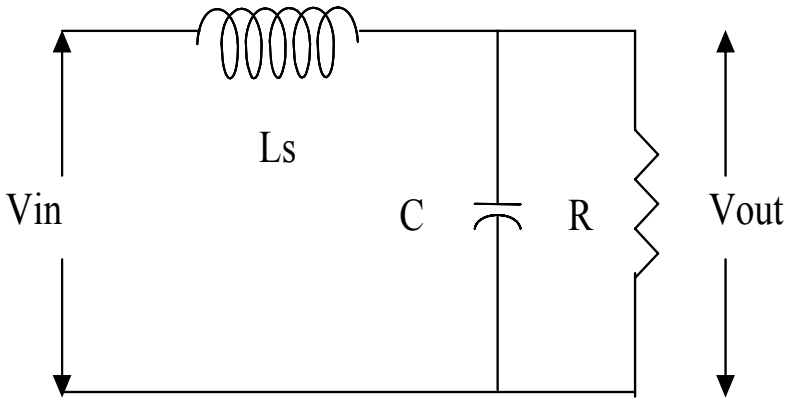

Figure 2.7: Output Filter

Transfer function of the given filter is given by equation (2.2),

$Z = (R/Cs)/(R+1/Cs)$…….. (2.1)

$$G_{LC} = \frac{V_O}{V_i} = \frac{Z}{Z + L\,s} \quad \text{……..……..... (2.2)}$$

Where, Z = Parallel combination of the load resistance and capacitance

Ls = Total filter inductance referred to secondary side of transformer

= Secondary leakage + Series inductor referred to secondary side

$= 8.45 * 10^{-3} + (5 * 10^{-6}) * (540/4)^2$ H = 99.575 mH

C = Total filter capacitance = 0.11 µF

R = Load Resistance = 70 kΩ

$G_{LC} = 1 / (LCs^2 + L*s/R + 1)$……..……..……..…..(2.3)

2.2.2.1 Bode Plot of Filter Transfer Function

The gain characteristic of an output LC filter with various output load resistances is shown in figure (2.8) & (2.9). Bode plot is plotted for the critical load which is defined as $R_0 = \sqrt{L/C}$. If the circuit is stable for the gain curve corresponding to critical load, it will be stable at other loads.

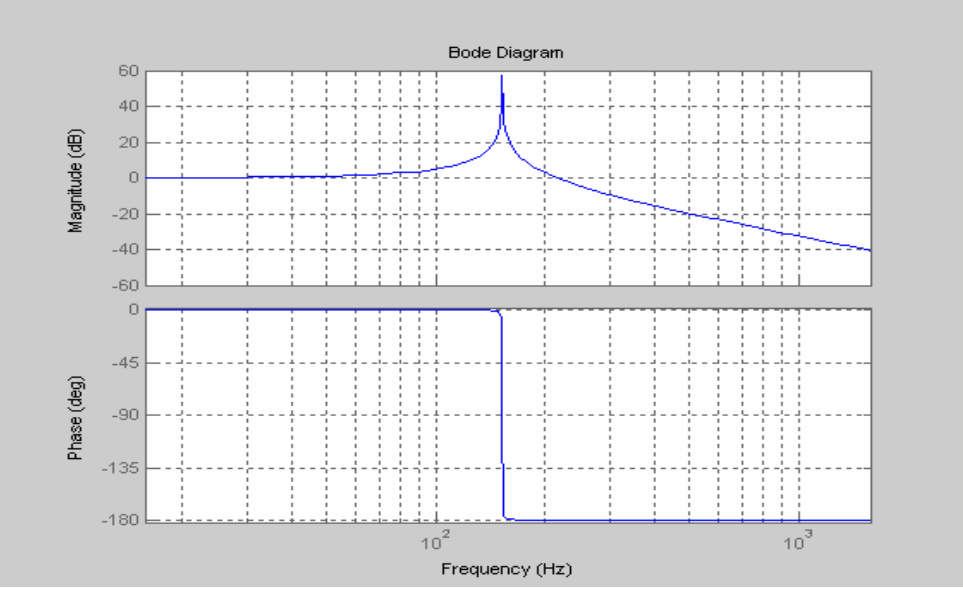

Figure 2.8: Bode Plot of Filter with 70K Load

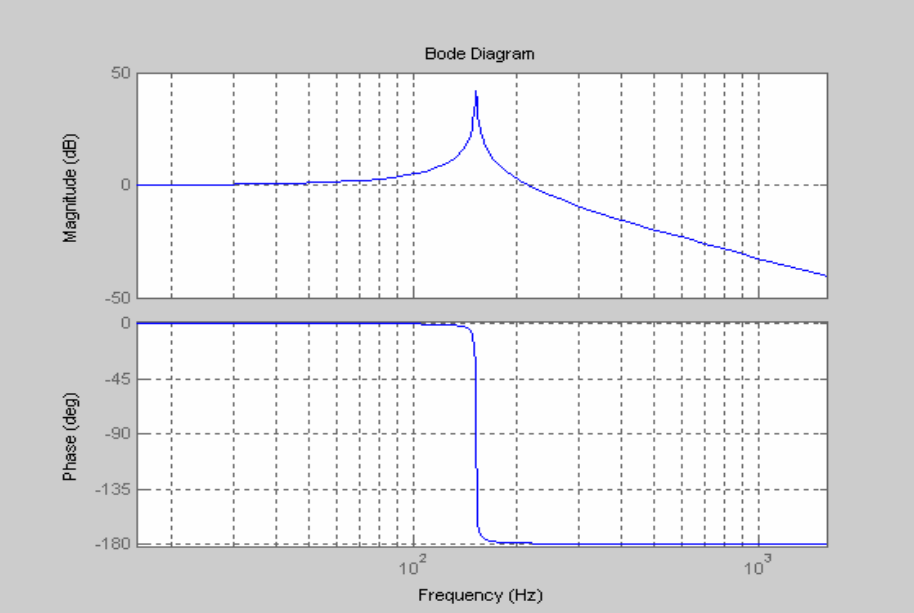

Figure 2.9: Bode Plot of Output Filter for Critical Load R_0

It is seen from the bode plots, that the value of the gain is 0 dB (numerical gain of 1) at DC and low frequencies up to the corner frequency $F_0 = 1/2\pi\sqrt{LC}$. At DC and frequencies less than F_0, the impedance of capacitance is much greater than that of inductance and the output-input gain is unity.

Beyond F_0, the impedance of capacitance decreases and that of inductance increases at the rate of 20 dB/ decade, making the gain slope fall at a rate of –40 dB per decade or at a –2 slope. The transition to a –2 slope at F_0 is not abrupt. The gain curve leaves 0 dB smoothly just before F_0 and asymptotically approaches the –2 slope shortly after F_0.

2.2.3 Sampling Network Gain

For feedback control the sample of output voltage is taken through sampling network. Consider the condition of maximum output voltage i.e. 6000 V. The sample is 3.0 volt is taken from the R2. Sampling network is shown in figure (2.10).

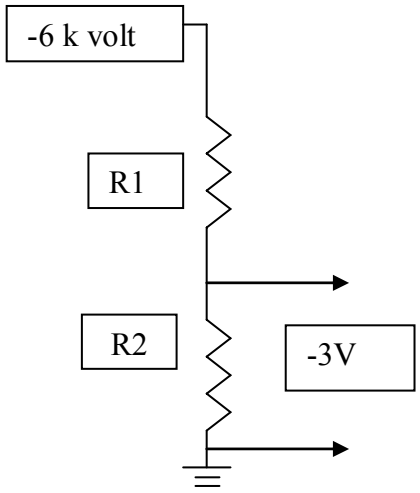

Figure 2.10: Sampling Network

Let, R_1 = 19.8 MΩ, & $R_2 * 6 * 10^3 / (R_1+R_2) = 3$ Volt

Minimum gain $(G_S) = \dfrac{R2-5\%}{(R1+R2)+5\%} = 4.795*10^{-4}$……..…….(2.4)

2.2.4 Error Amplifier Transfer Function

A closed loop system should have gain of 0 dB at crossover frequency for stability. Hence the gain of the error amplifier at F_{co} is equal and opposite of the gain G_t.

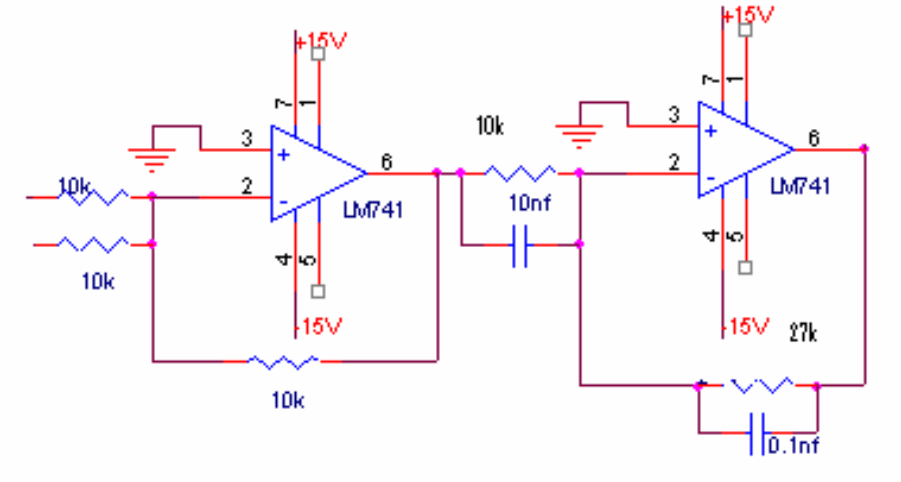

Figure 2.11: External Error Amplifier

Transfer function of external amplifier is given by T1:

$T_1 = (R_2/R_1)*(1+R_1*C_1*s)/ (1+R_2*C_2*s)$…..…….... (2.5)

Adopting Venable's scheme, the ratio of $F_{co} / F_z = K$ will be chosen equal to $= F_p / F_{co} = K$, now a zero causes a phase lead and a pole causes a phase lag. The phase lead at frequency F due to a zero at frequency F_z is

$$\theta_{ld} = \tan -1 \frac{F}{F_z} \text{ ……..…… (2.6)}$$

Similarly phase lead at F_{co} due to a zero is given by:

$\theta_{ld}(\text{at } F_{co}) = \tan -1K$ ……..(2.7)

Similarly phase lag at F_{co} due to a pole is given by:

$$\theta_{lag}(\text{at } F_{co}) = \tan -1\frac{1}{K} \text{ …….. (2.8)}$$

These shifts are in addition to inherent low 90° phase shift of the error amplifier with its pole at origin. The error amplifier is an inverter and at low frequency causes a 180° phase shift. Total phase lag is then;

$$\theta_{(EA)} = 180° + 90° - \tan -1K + \tan -1\frac{1}{K} \text{ ……..…… (2.9)}$$

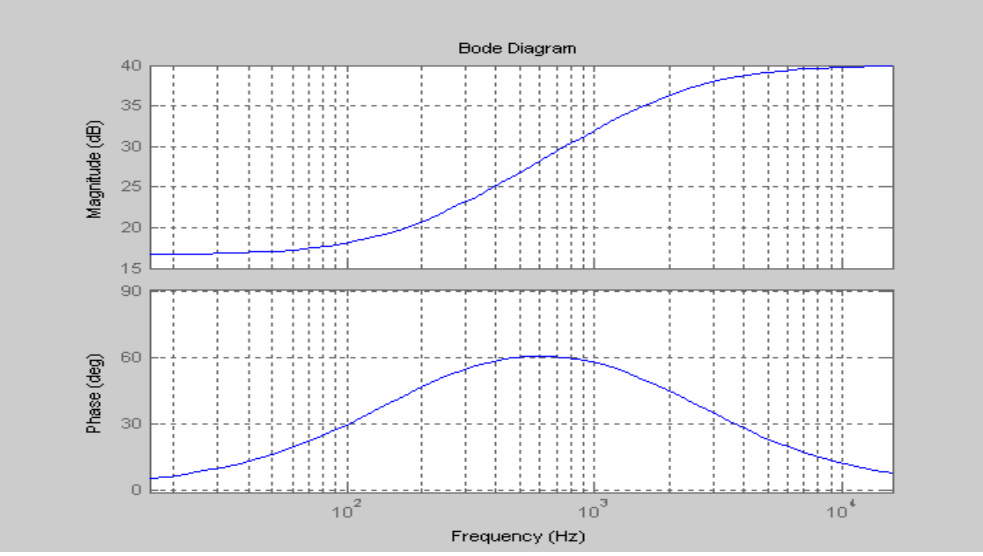

Figure 2.12: Bode Plot for Error Amplifier

2.2.5 Pulse Width Modulator Gain

The gain from the error amplifier output to the average voltage at V_{sr} (input end of the output inductor) is the PWM gain and is designated as G_{pwm}. The PWM compares the DC voltage level from V_{ea} to a 3-volt triangle at V_t. When V_{ea} is at the bottom of the saw-tooth wave, ON time or pulse width at V_{sr} is zero.

$$V_{av} = \frac{(Vs - 1)t_{on}}{T} \quad \text{..... (2.10)}$$

Where, V_S = DC supply voltage.

When V_{ea} has moved up to the top of the 3V triangle, then the voltage at the output should be maximum i.e. 6000V. So,

$G_{pwm} = 6000/3 = 2000$..... (2.11)

2.2.6 Total System Gain

Total phase lag provide by overall system is given by; phase lag provide by error amplifier + phase shift provide by output filter + pulse width modulator + sampling network. Total gain $G_t = G_{LC} + G_{pwm} + G_S$ (in dB)

$G_t = G_{LC} * G_{pwm} * G_S$ (in decimal)..... (2.12)

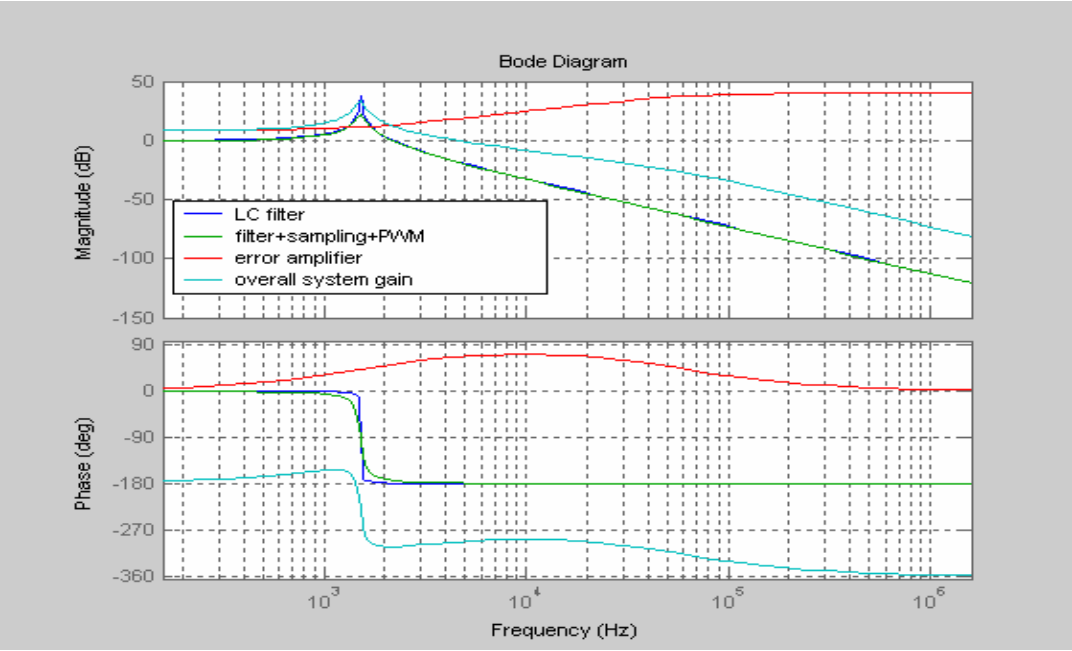

Figure 2.13: Total Gain Characteristics

CHAPTER 3 HARDWARE DESIGN

3.1 TRANSFORMER DESIGN

The design of high-voltage DC-DC converter is challenging because the large turn ratio of the transformer exacerbate the transformer non-idealities. In particular, the leakage inductance and the winding capacitance significantly change behavior of converter. In switched-mode converters the leakage inductance causes undesirable voltage spikes that can damage circuit components and the winding capacitance results in current spikes and slow rise times. Both non-idealities can lead to greatly increased switching and snubber losses and reduced converter efficiency and reliability.

3.1.1 Functions of Transformer

The purpose of a power transformer is to transfer power efficiently and instantaneously from an external electrical source to an external load. In doing so, the transformer also provides important additional capabilities:

- The primary to secondary turn's ratio can be established to efficiently accommodate widely different input/output voltage levels.
- Multiple secondary wires with different numbers of turns can be used to achieve multiple outputs at different voltage levels.
- Separate primary and secondary windings facilitate high voltage input/output isolation, especially important for safety in off-line applications.

3.1.2 Transformer with 'E' Type Ferrite Core

3.1.2.1 Core Selection

(i) Material

Select a core material appropriate for the desired transformer frequency. With power ferrites, higher frequency materials have higher resistivity, hence lower eddy current losses. However, the permeability is generally lower, resulting in greater magnetizing current, which must be dealt with in snubber and clamps. With metal alloy cores, the higher frequency materials have higher resistivity and require very thin

laminations. Although saturation flux density is very much greater than with ferrite materials, this is irrelevant because flux swing is severely limited by eddy current losses. Ferrite is the best choice in transformer applications except for mechanical ruggedness. In our design we used ***"E-65*32*13" ferrite core***.

In most ferrite materials, hysteresis losses dominate up to 200-300 KHz. At higher frequencies, eddy current losses take over, because they tend to vary with frequency squared (for the same flux swing and wave shape).

(ii) Shape

The window configuration is extremely important. The window should be as wide as possible to maximize winding breadth and minimize the number of layers. This results in minimized R_{ac} and leakage inductance. Also, with a wide window, the fixed creep age allowance dimension has less impact. With a wider window, less winding height is required, and the window area can be better utilized. In our design we used two *E –shaped* core.

(iii) Frequency

There are several meanings to the term "frequency" in switching power supply applications. In this design, "switching frequency", f_S, is defined as the frequency at which, switch drive pulses are generated. It is the frequency seen by the output filter, the frequency of the output ripple and input ripple current. It is an important concept in control loop design. In a single-ended power circuit such as the forward converter, the power switch, the transformer, and the output rectifier all operate at the switching frequency. The transformer frequency and the switching frequency are the same.

3.1.2.2 Primary Winding

To utilize the full efficiency of transformer, core losses should be low. So, transformer is tested for different conditions to reduce the heat loss in primary winding. Two arrangements made to reduce heat losses are:

- Copper strips in primary instead of wire.
- Multi-stranded wire.

3.1.2.3 Number of Turns

The main specifications and detailed calculation of primary and secondary parameters are given here. To find out the turn ratio; transformer EMF equation is used:

$E_{av} = 4*B*A*N*f*10^{-8}$ volts…….. (For low frequency)……..... (3.1)

$E_{av} = 2.86*B*A*N*f*10^{-4}$ volts…… (For high frequency)……..….... (3.2)

$E_{av} = A*N*dB/dt *10^{-8}$ volts……. (For full bridge)……..... (3.3)

Here, dB = Field excursion (3200 gauss at 50 Hz and excursion will decrease at high frequencies)

So we take dB = 2500 gauss at 100 KHz

dt = ON time (duty period)

A = Area of two 'E' cores in cm^2 ($532*10^{-2}$)

Using (3.3), we get the turn ratio of primary winding having E_{Min}= 48-4 = 44V

N_p =1.323 ….so we can choose N_p = 2 Turns...…….……...(3.4)

Now using formula $V_o = V_{om} * 2* t_{on} / T$…….……...…...…… (3.5)

Here, V_o= voltage across the filter capacitor after rectification of voltage of secondary

V_{om} = voltage across the transformer secondary developed

By using (3.5) Putting V_o= 6000V, $t_{on} / T = 0.4$

We get V_{om}= 7500V

Since $V_{om}= (((V_{dc}-2)* N_s/N_p)-0.5)*2* t_{on} / T$…….……... (3.6)

By using (3.6) we get the value of Ns.

N_s = 390 turns…….……..…….…….…..... (3.7)

3.1.2.4 Currents

P = V*I…….…….. ...(3.8)

Here: P_o = Peak Power Output (1600w) & V = Output voltage (6000v)

So secondary current

I_s = 0.266 Amps….……....….. (3.9)

And primary current $I_p = V_o*I_s / V_{dc}$……... (3.10)

Using (3.10) we get the value of peak primary current.

I_p = 33.33 A……...…… (3.11)

3.1.2.5 Inductances

To calculate the primary inductance we used the formula given below:

$$Lp = \frac{4\pi N_p{}^2 A \mu_e}{10^9 l} \quad \text{……..……... (3.12)}$$

where,

l = magnetic path length in cm. (14.7)

μ_e = permeability for 'E' core (800)

A = Area of two 'E' cores in cm^2 ($532*10^{-2}$)

N_p = 2 turns

By putting values of l, A, N_p & μ_e in equation (3.12) we get the primary inductance as

L_p = 14.55 μH…… (3.13)

Similarly, by replacing N_p with N_s in equation (3.12) we get the value of secondary inductance as

$$Ls = \frac{4\pi N_s{}^2 A \mu_e}{10^9 l} \quad \text{……..……. (3.14)}$$

At N_s = 390 turns,

L_s = 553 mH…….….. (3.15)

3.1.2.6 Measured Values of Transformer Specifications on 'E' Core

The transformer specifications measured on LCR Bridge are given below:

- Primary Inductance: 17.4 μH
- Primary Leakage Inductance: 1.6 μH
- Secondary Inductance: 612 mH
- Secondary Leakage Inductance: 12.51 mH

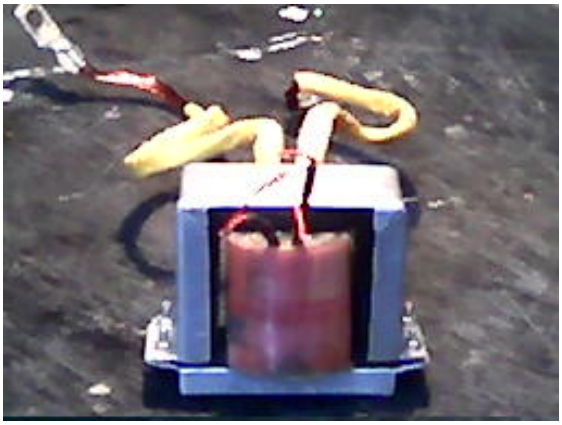

Figure 3.1: View of 'E' Core Transformer with Multi-Stranded Wire

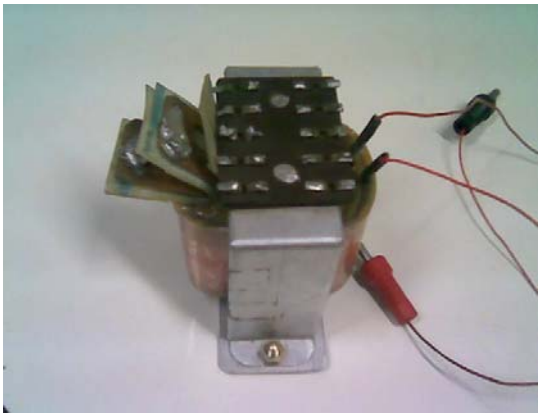

Figure 3.2: View of 'E' Core Transformer with Copper Strips

3.1.2.7 Limitations of 'E' Core

- Area offered by core is less.
- Due to less area, more turns are wound in a layer. Thus, high voltage surge may result in transformer failure.
- Since number of turns in secondary is more, number of layers is increased in the secondary winding. Thus, there is a possibility of insulation failure.

3.1.3 Transformer with 'C' Type μ-Metal Core

All the limitations of 'E' core can be removed successfully by using 'C' cores. 'C' cores are strip wound, impregnate and cut into two halves. Since these cores are assembled around the bobbins in a very short time it takes less time to manufacture the transformer. Cores are produced from silicon steel, Ni Fe materials and amorphous metals. The front and side view of the 'C' core used is shown in figure 3.8.

3.1.3.1 Calculations of Number of Turns

To calculate the number of turns for 'C' cores, the major factor is the area of core. The steps involved in designing of core are more or less similar to 'E' core. To calculate the number of primary turns, equation (3.3) is used.

$A = 5.91\ cm^2$

On calculating the value of primary turns from equation (3.3) we get

$N_p = 1.19 \approx 2$ turns……..(3.16)

Similarly, by using equation (3.5) & (3.6) we get the number of secondary turns as

$N_s = 270$ turns…….…….…..….. (3.17)

Now,

$N_s / N_p = 135$

Keeping the ratio of transformation same, we get

$N_p = 4$ turns……...…....(3.18)

$N_s = 540$ turns……...… (3.19)

3.1.3.2 Measured Values of Transformer Specifications on 'C' Core

The transformer specifications measured on LCR Bridge are given below:

- Primary Inductance: 88 μH
- Primary Leakage Inductance: 1.8 μH
- Secondary Inductance: 1474 mH
- Secondary Leakage Inductance: 8.45 mH

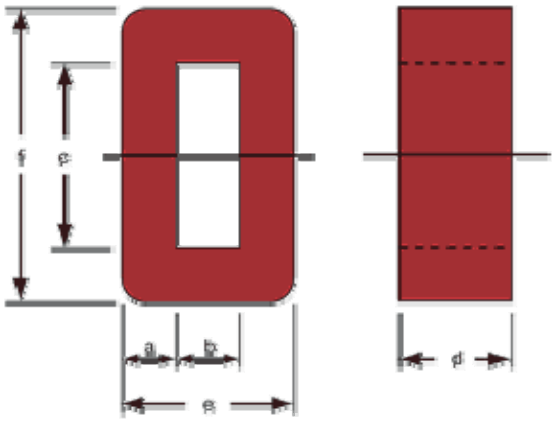

Figure 3.3: Transformer with 'C' Core

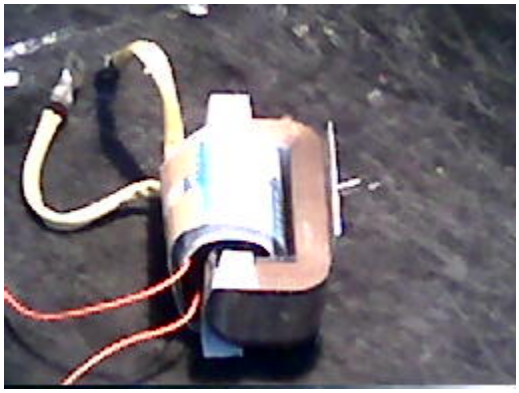

Figure 3.4: View of Transformer with 'C' Core

Table 1: Dimensions of 'C' Core

CORE No.	a (mm)	b (mm)	c (mm)	d (mm)	e (mm)	f (mm)	lm (cm)	Ac (cm2)	MASS (g)	VOL (cm3)	Wa (cm2)
AMCC-100	16 ± 1	20	70	45 ±1	52 ±1	102 ±3	25	5.91	1060	148	14

3.2 AUXILIARY VARIABLE DC SUPPLY FOR INVERTER

According to the converter specifications, a DC supply is required at the input. A 48 ± 4 V DC input is required. So, first of all, a DC power supply is designed for this purpose, which gives the variable DC voltage in input with the help of an auto-transformer.

3.2.1 Block Diagram of Variable DC Supply

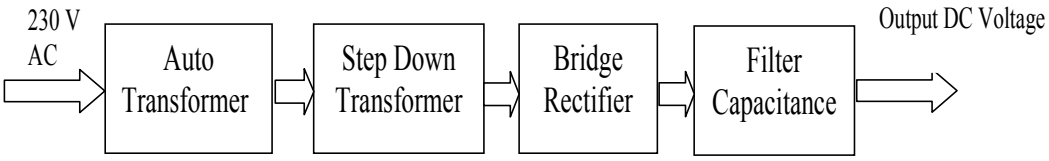

Figure3.5: Block Diagram of Variable DC Supply

3.2.2 Circuit Diagram of the Supply

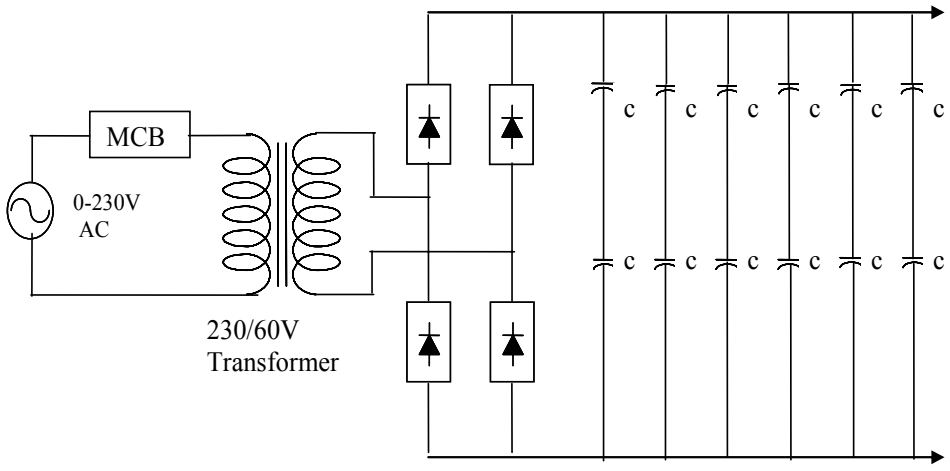

Figure 3.6: Circuit Diagram of 60V Variable DC Supply

Specifications of each module in supply are given below:

(i) Step-down Transformer

The specifications of the transformer are given as:

Input Voltage: 220 volt (AC)

Output Voltage: 60 volt (AC)

Input Current: 5 Amps.

Output Current: 18 Amps.

Frequency: 50Hz

(ii) Bridge Rectifier

In our transformer secondary the current is 18 Amps. So we used higher current rating diodes for the rectification of the AC to DC. Rating of the diode is given below:

- Diode Name: GE9640 1N3768
- Voltage Rating: 1000 Volts
- Current Rating: 35 Amps.

(iii) Calculation for the Filter Capacitance

Total charge stored by capacitor is given by the equation

$Q = C \Delta V$…… (3.20)

Where: Q = Total charge stored by capacitor,

C = Total Capacitance

ΔV = Voltage Ripple (generally we take ΔV as 2 -8% of output voltage)

So ΔV = 5 volt

Vout = 60 volt

Also $Q = I\,dt$…….…….…….. (3.21)

Where: dt is the discharge time of capacitor (Let dt = 8 mSec)

I = Output Current

From equations (3.20) & (3.21), we get the value of capacitance,

C = 30,000 μF/40 V

In figure (3.11), value of C = 10,000 μF/40 V

3.2.3 LAB Prototype of Supply

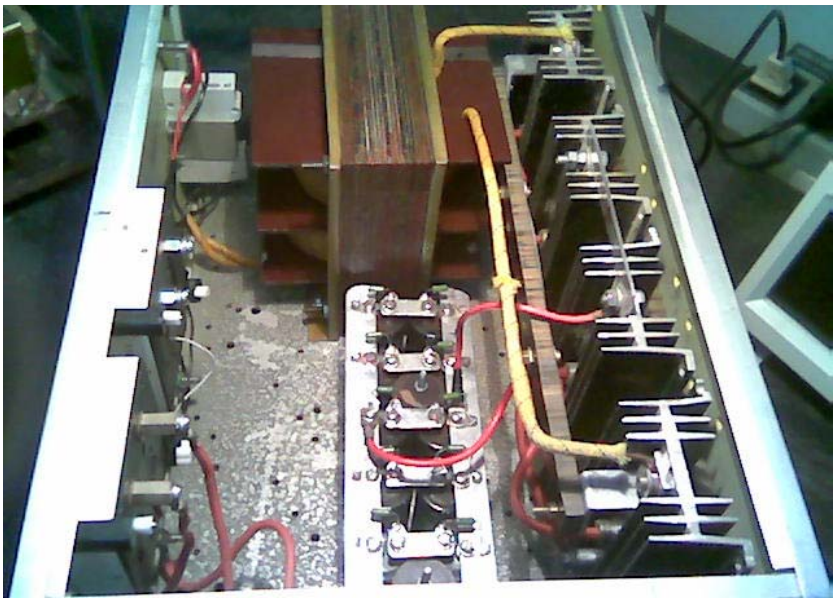

Figure 3.7: Internal Structure of 60 Volt Variable DC Supply

Figure 3.8: Complete View of 60 Volt Variable DC Supply

3.3 DEVICE SELECTION

Power loss calculation for the IGBT's:

1. Conduction Losses

The conduction losses are caused by forward voltage drop.

$$P_c = V_{sat} * I_c * \text{Duty Cycle} \quad \text{(3.22)}$$

Here, $V_{fwd} = V_{sat.}$

I_c = Transformer primary current rating

2. Blocking Losses

These losses are caused by a low leakage current while blocking a high voltage.

So, $P_b = V_{blk} * I$ watt (3.23)

Here, I = Leakage current,

V_{blk} = Blocking voltage applied

3. Switching Losses

This is the amount of energy required for a certain switching operation. These losses can be calculated from the data sheet.

So, $P_{on} = V * I * t_r / t$ watts (3.24)

& $P_{off} = V * I * t_{off} / t$ watts (3.25)

Where,

t_r = Rise time during switch on

t_{off} = Total off time during switch off ($t_{off} = t_{d\ (off)} + t_f$)

t_f = Fall time during off condition

t = Total switching time

By using equations (3.22) to (3.25), the power loss per IGBT for different devices was calculated. We are using device BSM 35 GB120 DN2 for IGBT and found that the power loss is almost double of the loss of proposed device IXYS VII 130-06P1.

3.3.1 Features of Selected Devices

Power losses are given for three different devices in (Table-2)

Table 2: Loss Comparison of Different Devices

S.No.	Device Specifications	IXYS VII 130-06P1	BSM 35 GB 120 DN2	SEMICRON SKM756B063D
1.	**Rating of Device**	Ic=121A,Vc=600v 2-IGBT pack	Ic=50A,Vc=1200v 2-IGBT pack	Ic=100A,Vc=600v 2-IGBT pack
2.	**Size**	L=5.1cm,W=3.43cm Wt=24gm	L=94mm,W=34mm Wt=180gm	L=9.4cm,W=3.4cm Wt=160gm
3.	**Power Loss Per IGBT**	60watt @ 200khz 35.17watt @ 60kHz	115watt @ 200kHz 60watt @ 60kHz	90watt @ 200kHz 42watt @ 60kHz
4.	**Special Features**	NTC-arrangement for controlling the temperature		
5.	**Rise Time**	Tr =11n sec(fastest)	Tr = 60 n sec	Tr =50n sec
6.	**Energy Loss**	Eon=.8mJ Eoff=2.3mJ		Eon=3mJ Eoff=2.5mJ
7.	**Junction Temperature**	Rth(j-c) =0.33k/watt	Rth(j-c)=0.44k/watt	Rth(j-c)=0.35k/watt

3.4 GATE DRIVER CIRCUIT

3.4.1 Requirement of Gate Driver

For the operation of any converter circuit, power switches are needed. These switches may be IGBT or MOSFET's. In a half bridge circuit, two switches operate in each half cycle. To drive these switches, suitable gate pulses are fed. These gate pulses should match with the device specifications. To perform the above task, we used a hybrid integrated circuit IC-M57962L.

At the rectifier input, 24 V AC is supplied. Since, there are two gate drivers for two switches, we need two 24 V AC supplies. Also a logic circuit is needed, which ensures that the proper switching of the two IGBT switches.

3.4.2 Description of IC- M57962L

M57962L is a hybrid integrated circuit designed for driving n-channel IGBT modules in any gate amplifier application. This device operates as an isolation amplifier for these modules and provides the required electrical isolation between the input and output with an opto-coupler.

Short circuit protection is provided by a built in de-saturation detector. A fault signal is provided if the short circuit protection is activated.

Features

- Built in high CMRR opto-coupler (VCMR: Typical 30kV/s, Min. 15kV/s)
- Electrical Isolation between input and output with opto-couplers
- TTL compatible input interface
- Two supply drive topology
- Built in short circuit protection circuit with a pin for fault output

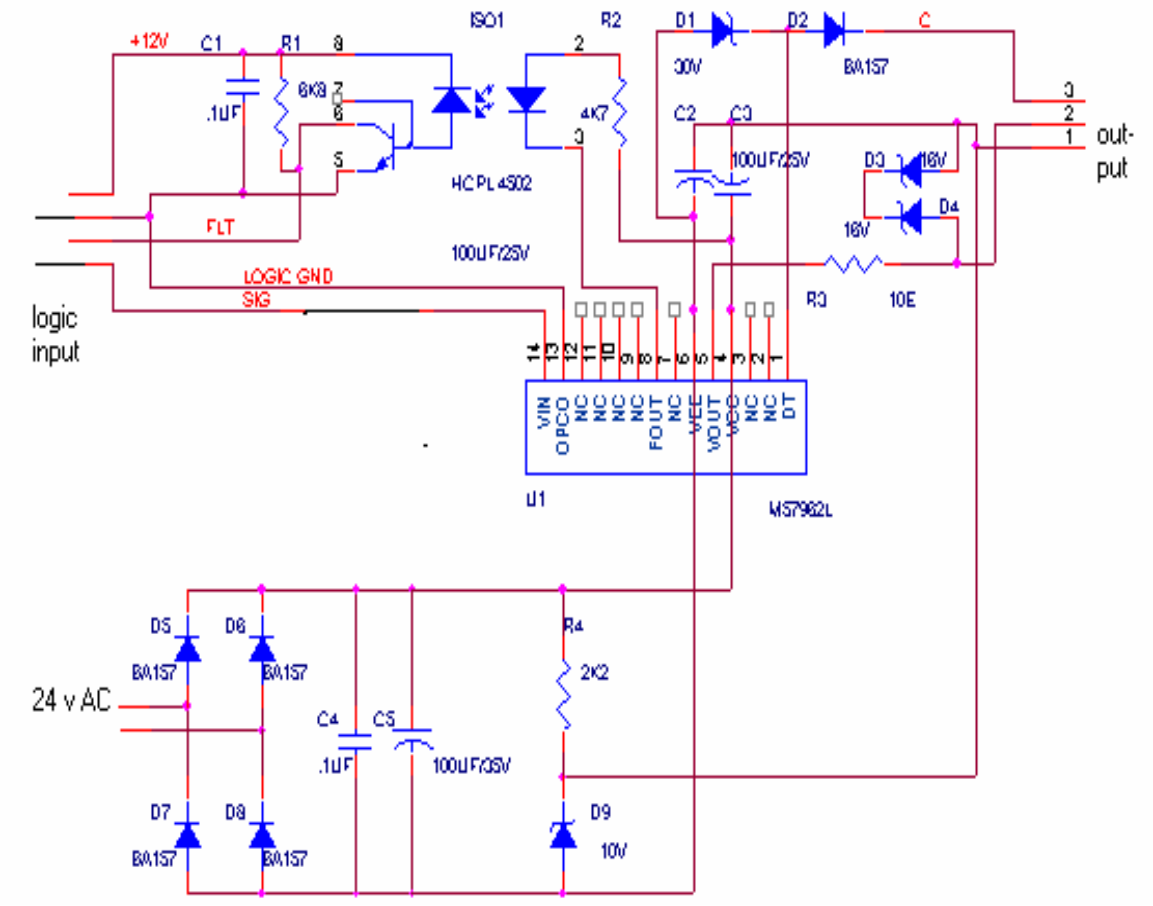

Figure 3.9: Gate Driver Circuit

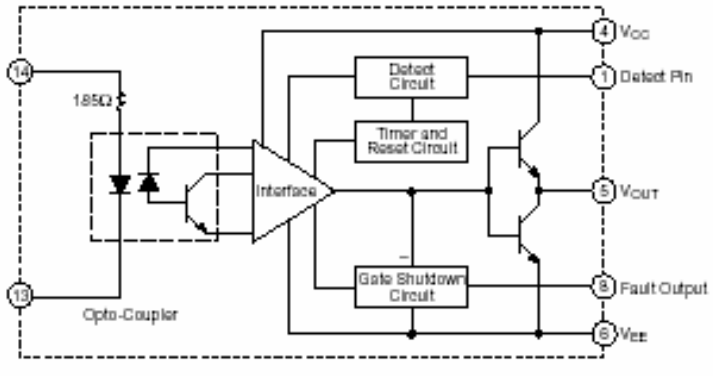

Figure 3.10: Block Diagram of IC-M57962L

3.4.3 Description of IC-HCPL4 502

The HCPL-4502 opto-couplers consist of an AlGaAs LED optically coupled to a high-speed photo-detector transistor. A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor opto-couplers by reducing the base-collector capacitance of the input transistor. An internal noise shield provides superior common mode rejection of 10 KV/µs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard of 220 V.

Features

- High speed-1 M Bit/s
- Superior CMR-10 kV/µs
- Dual-Channel
- Double working voltage-480V RMS
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)

Applications

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

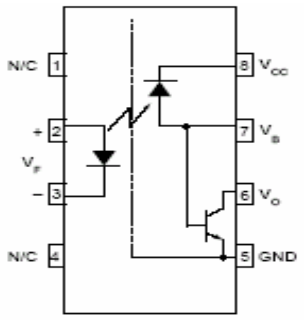

Figure 3.11: Block Diagram of IC-HCPL4502

3.5 LOGIC CIRCUIT

3.5.1 Requirement of Logic Circuit

For each switching device, an individual gate driver is required. In each half cycle two switches are in conduction. So, to ensure the proper operation of switching devices, a logic circuit is designed. This circuit provides two pulses, one is in out of phase with another. This circuit provides the two logic outputs **Q & Q'** at pin no. 11 and 14.the input of this IC is 15 volt DC and in output it will provide two pulses of 15 volt.

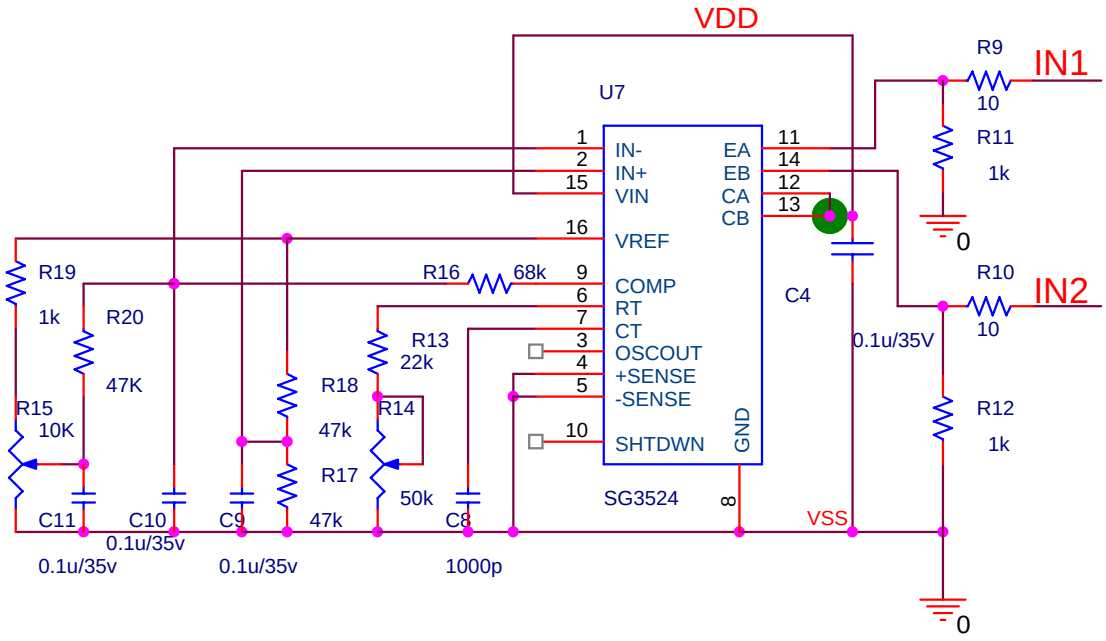

Figure 3.12: Logic Circuit for Gate Driver in Open Loop

3.5.2 Description of IC-SG3524

The SG3524 incorporates on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. The SG3524 family is designed for switching regulators of polarity, transformer-coupled dc-to-dc converters, transformer less voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-ship reference, error amplifier, programmable oscillator, pulse steering flip flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shutdown circuitry.

Features

- Complete PWM power control circuitry
- Uncommitted outputs for single ended
- Or push pull applications
- Low standby current 8ma typical
- Operation up to 300khz
- 1% maximum temperature variation
- Off reference voltage

3.5.3 Principle of Operation of IC-3524

The SG3524 is a fixed frequency pulse-width modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (RT) and one timing capacitor (CT). RT establishes a constant charging current for CT. This results in a linear voltage ramp at CT, which is fed to the comparator providing linear control of the output pulse width by the error amplifier.

The SG3524 contains an on-board 5V regulator that serves as a reference and as power supply for the SG3524's internal control circuitry. It is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common mode range of error amplifier or an external reference may be used.

A second resistor divider network to generate a feedback signal to error amplifier senses the power supply output. The amplifier output voltage is then compared to the linear voltage ramp at CT. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (QA or QB) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both output are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of CT. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or in parallel for single-ended applications in which the frequency is equal to that of the oscillator.

The output of the error amplifier shares a common input to the comparator with the current limiting at shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator

3.6 SUPPLY FOR GATE DRIVER

3.6.1 Requirement of Supply Circuit

For gate driver, an input supply of 24 V DC is needed. This supply gives 24 V AC to both gate drivers. There is a provision in gate driver circuit for conversion of this 24 V AC to 24 V DC. Supply circuit has a regulated power supply IC-1525 which provides two logic pulses for two switches of a half bridge inverter circuit. This will ensure the proper operation of two switches in both the half cycles. Transformer of this inverter consists of two secondary wires. This will provide the necessary 24 V AC output.

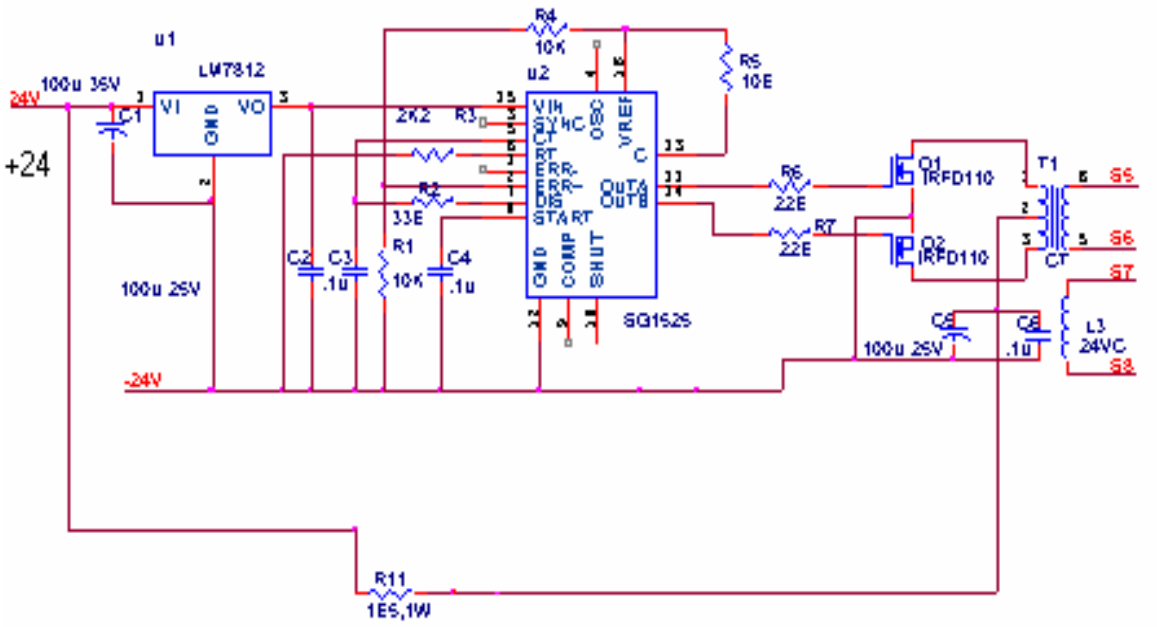

Figure 3.13: Supply Circuit for Gate Driver

3.7 LAB PROTOTYPE OF CONVERTER

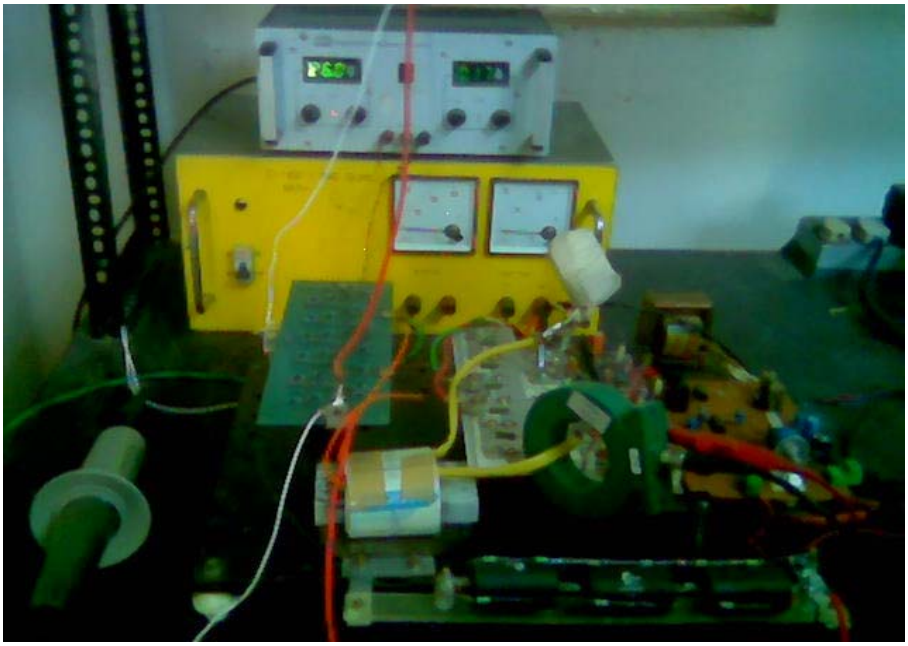

Figure 3.14: Complete Lab prototype of Full Bridge DC-DC Converter

Figure 3.15: Lab prototype of Logic Circuit

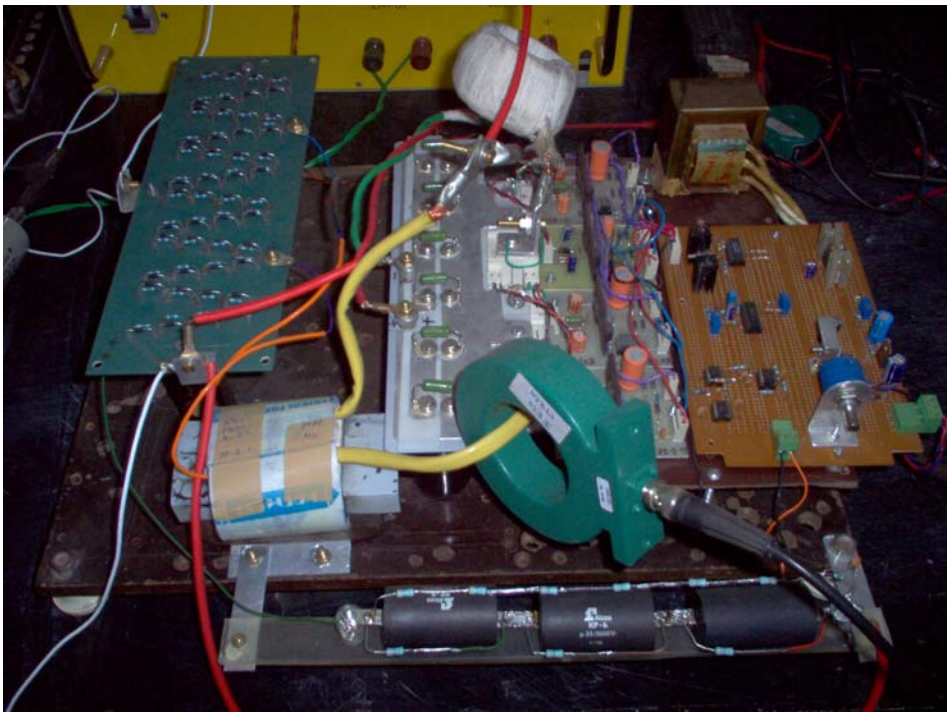

Figure 3.16: Lab prototype of Full Bridge DC-DC Converter with Close Loop

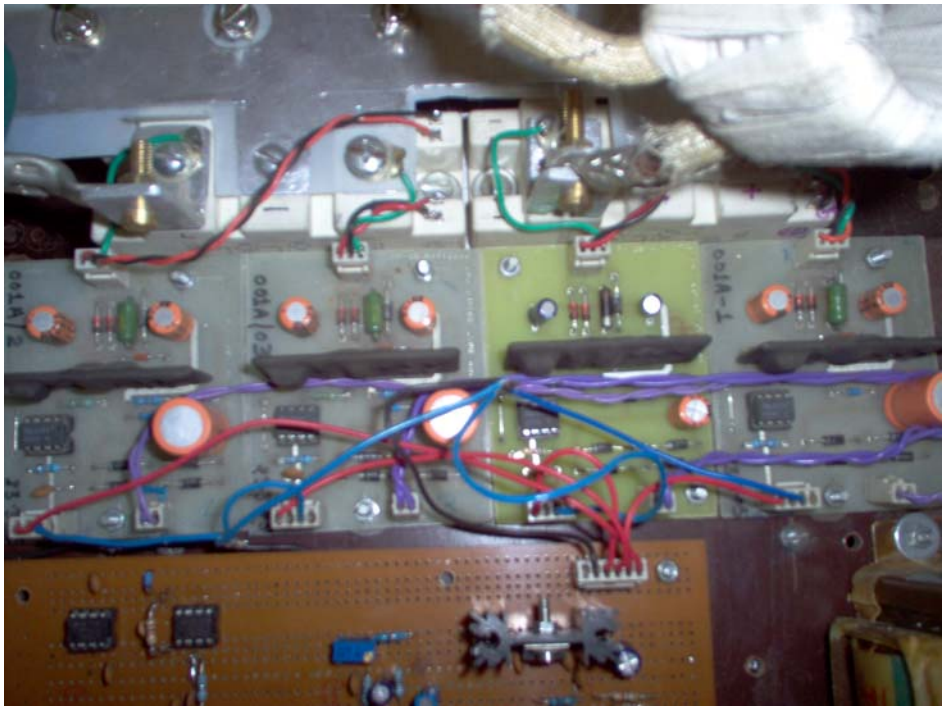

Figure 3.17: Lab prototype of Driver Circuit

CHAPTER 4 HARDWARE RESULTS

A full bridge DC-DC converter is simulated and fabricated in the laboratory. In the testing of the lab prototype, it is found that the calculated values of transformer specifications matches with the system specifications. All the results are taken on the resistive load. Line regulation is calculated for different conditions. Schematic diagram of the DC-DC converter with close loop is shown in figure 4.1

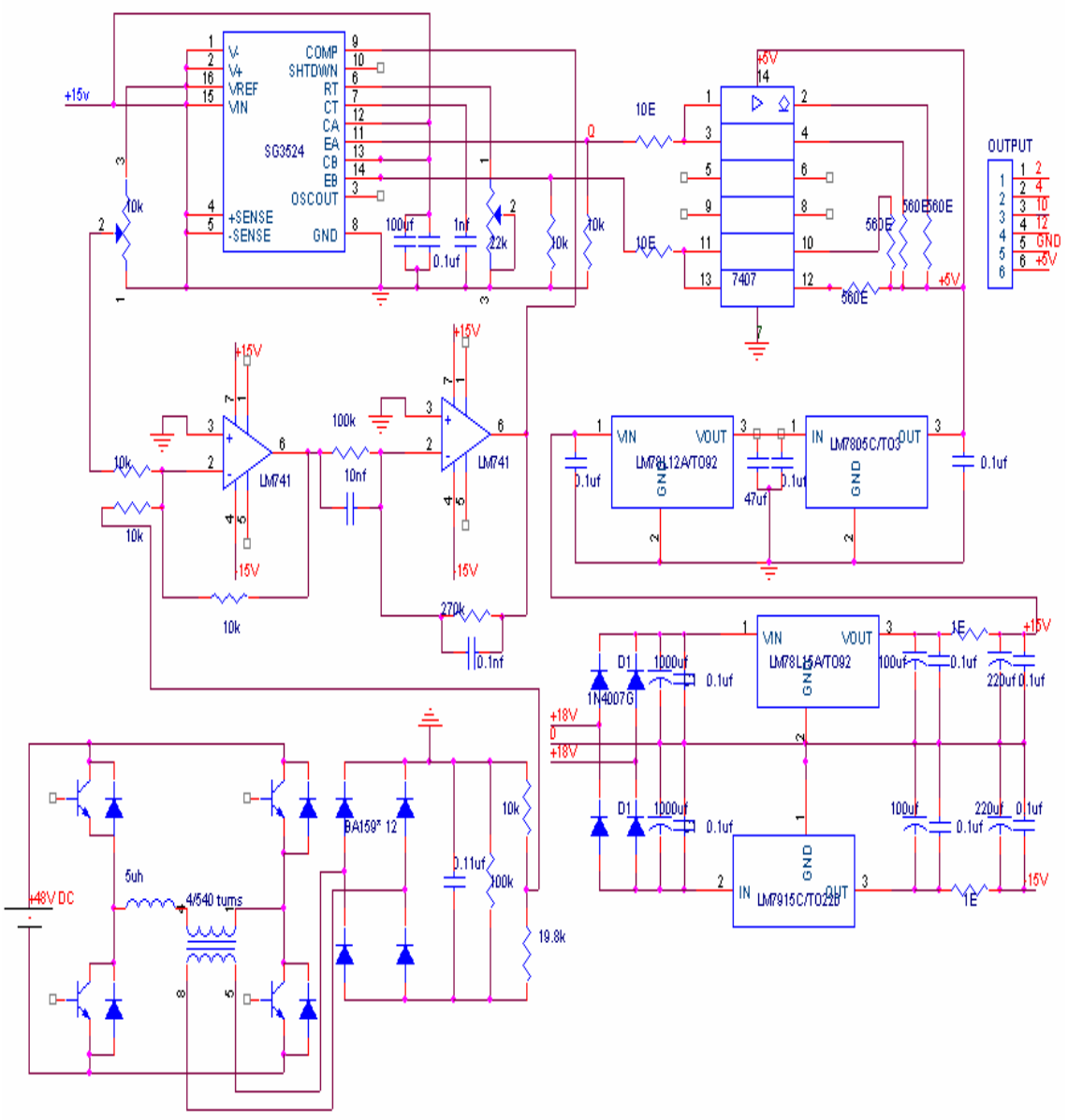

Figure 4.1: Schematic Diagram of Close Loop DC-DC Converter

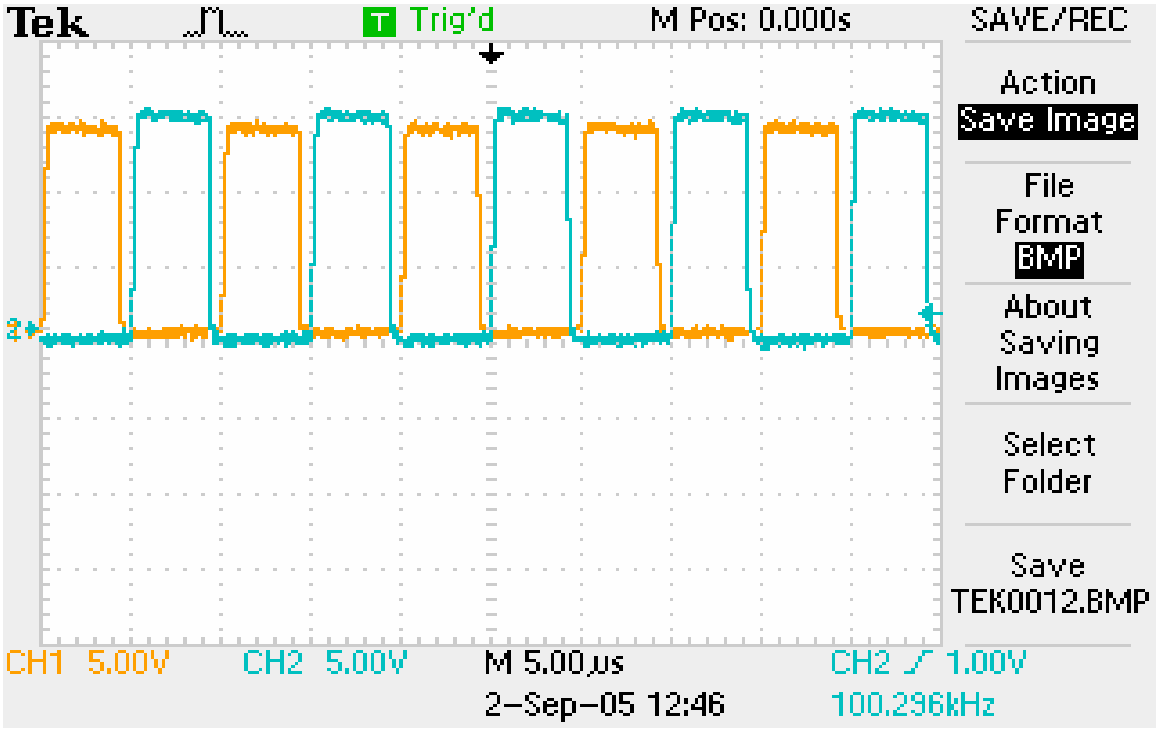

Figure 4.2: Output Waveform of Logic Circuit

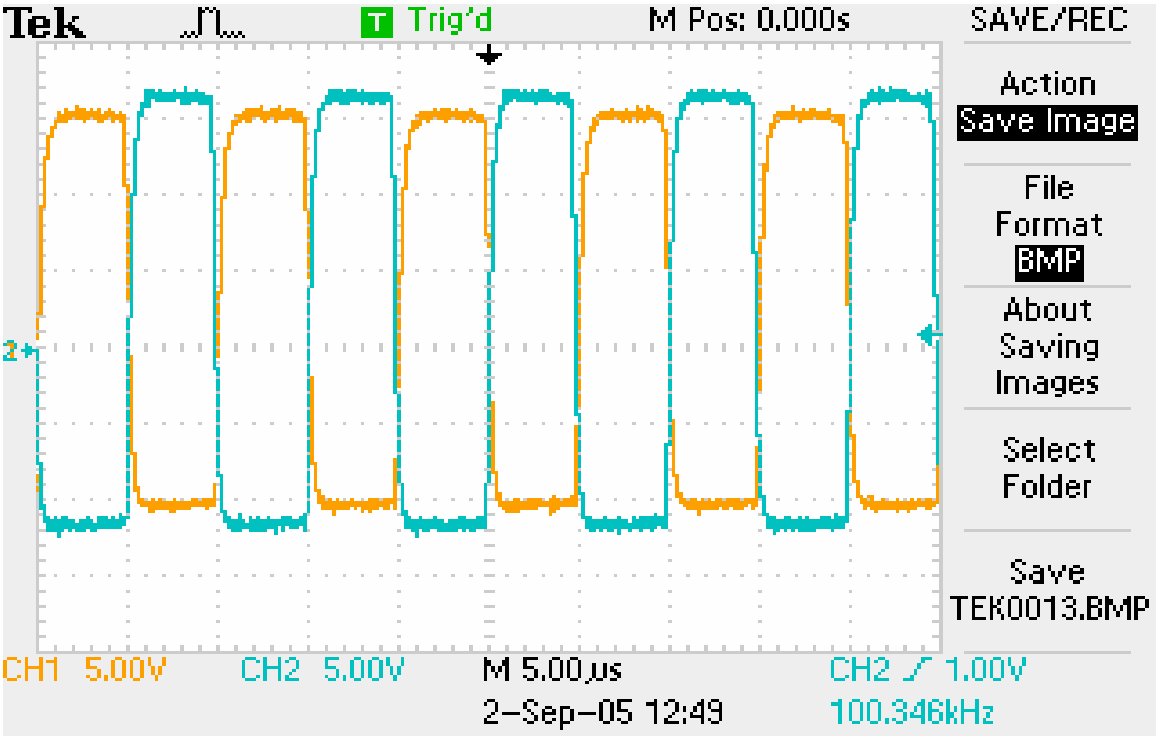

Figure 4.3: Gate Pulses for IGBTs

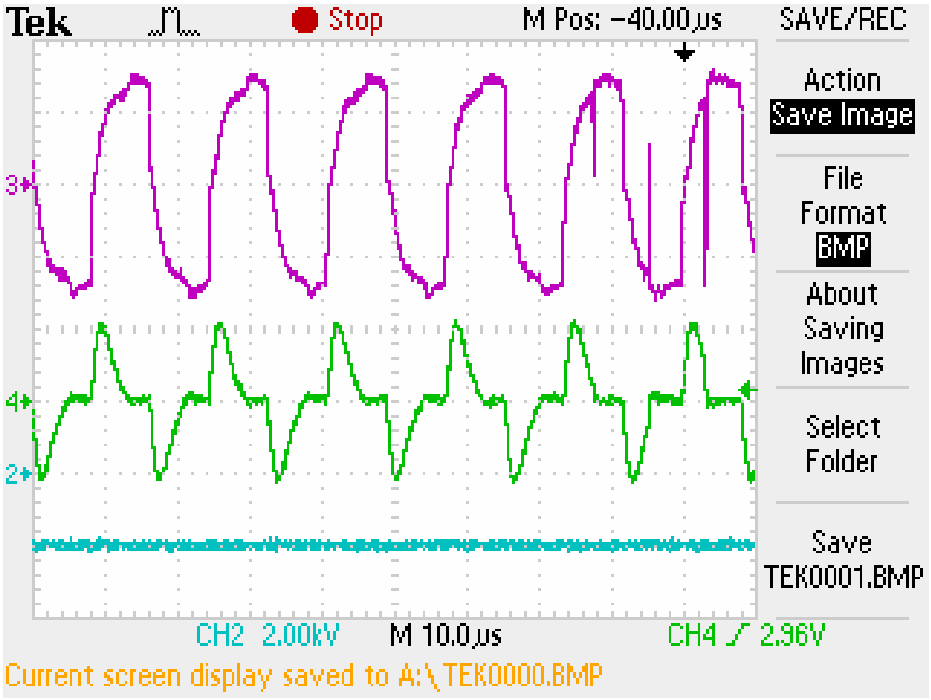

Figure 4.4: Transformer and Output Waveforms without Choke Coil in Primary (Channel -2: DC Output, Channel -3: Primary Voltage, Channel -4: Primary current) (Vs = 15 V, Is = 7 Amps, f = 60 KHz, Pulse width = 7 µsec.)

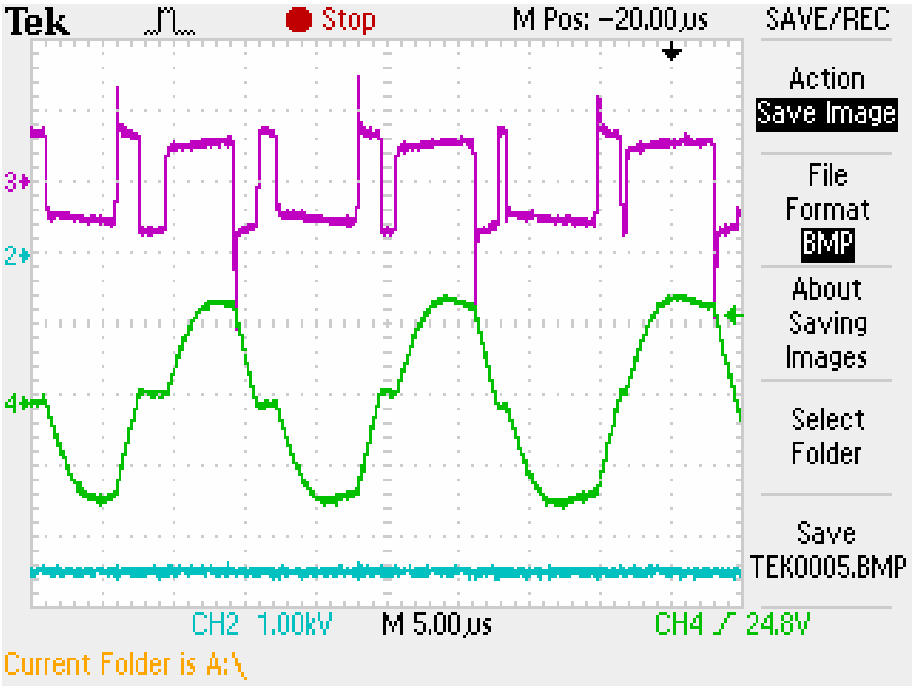

Figure 4.5: Transformer and Output Waveforms with Choke Coil in Primary (Channel -2: DC Output, Channel -3: Primary Voltage, Channel -4: Primary current) (Vs = 35 V, Is = 11 Amps, f = 60 KHz, Pulse width = 7 µsec.)

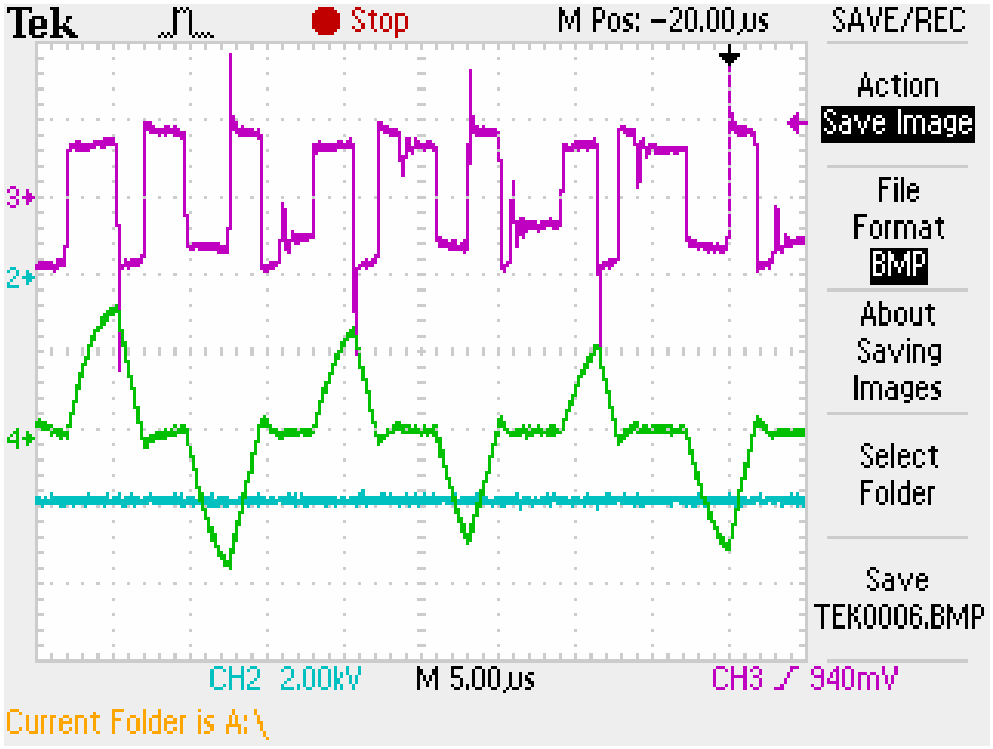

Figure 4.6: Transformer and Output Waveforms with Choke Coil in Primary (Channel -2: DC Output, Channel -3: Primary Voltage, Channel -4: Primary current) (Vs = 44 V, Is = 14 Amps, f = 60 KHz, Pulse width = 7 µsec.)

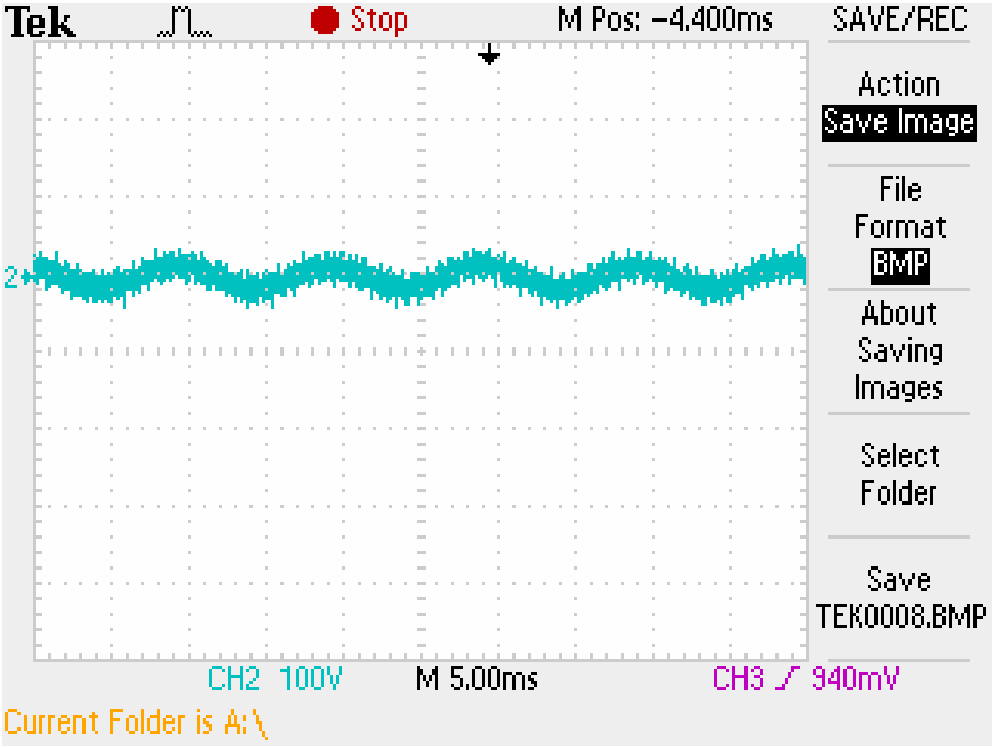

Figure 4.7: AC Ripple in Output DC (V_{out} = 6 KV)

4.1 MEASUREMENTS

With the designed transformer, voltages at primary and secondary windings are measured on CRO. Also line voltage regulation is calculated at different load resistances. Line regulation is defined as percentage change in output voltage on certain change in input voltage. Calculated line regulation is shown in tables 3-5.

Table 3: Line Voltage Regulations at 60 KΩ (10 KΩ / 100W each) Resistive Loads

Set Output Voltage	**Input Voltage (change in input voltage 48 ± 8.33 %)**			**Output Voltage Regulation**
	44V	**48V**	**52V**	
4 KV	3.89 KV	4 KV	4.07 KV	+ 1.75 % - 2.75 %
3 KV	2.91 KV	3 KV	3.07 KV	+ 2.33 % - 3.00 %
2 KV	1.93 KV	2 KV	2.04 KV	+ 2.00 % -3.50 %
1 KV	965 V	1 KV	1.03 KV	+ 3.00 % - 3.00 %

Table 4: Line Voltage Regulations at 80 KΩ (10 KΩ / 100W each) Resistive Loads

Set Output Voltage	**Input Voltage (change in input voltage 48 ± 8.33 %)**			**Output Voltage Regulation**
	44V	**48V**	**52V**	
4 KV	3.90 KV	4 KV	4.07 KV	+ 1.75 % - 2.50 %
2 KV	1.96 KV	2 KV	2.04 KV	+ 2.00 % - 2.00 %
1 KV	960 V	1 KV	1.01 KV	+ 1.00 % - 4.00 %

Table 5: Line Voltage Regulations at 50 KΩ (10 KΩ / 100W each) Resistive Loads

Set Output Voltage	**Input Voltage (change in input voltage 48 ± 8.33 %)**			**Output Voltage Regulation**
	44V	**48V**	**52V**	
3.5 KV	3.40 KV	3.5 KV	3.62 KV	+ 3.42 % - 2.85 %
2 KV	1.95 KV	2 KV	2.07 KV	+ 3.50 % - 2.50 %

CHAPTER 5 CONCLUSIONS & FUTURE SCOPE

5.1 CONCLUSION

In the given time, simulation, fabrication and testing of a full bridge DC-DC converter has been completed successfully for specific high voltage of 6 kV.

Transformer is designed for Vp = 48 V & Vs = 6 kV. Transformer on 'C' core is fabricated. Results with 'C' core transformer matched with the required specifications. Primary and secondary waveforms for this transformer are analyzed with full bridge type DC-DC converter.

Open loop and close loop operation of full bridge converter are tested successfully. Over all system stability is analyzed for the required limits.

The voltage regulation at 4 kV output in close loop is found +1.75%,so the output voltage can be controlled by using PWM technique. And the 80 V peak-peak ripple is found in 6 kV DC output.

5.2 FUTURE SCOPE

- Over all system efficiency can be increased by replacing IGBTs to IXYS VII 130.06P1.
- The system can be optimized in size and weight by using designed PCB.
- For the given specifications, the system can be analyzed for other topologies.

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[7] Abraham I. Pressman, "Switching power supply design," *McGraw Hill international editions*, New York, 1992.

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APPENDIX A

MATLAB CODE
FOR
CLOSE LOOP STABILITY

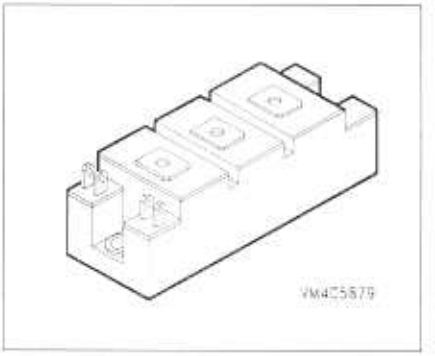
MATLAB Program for Close Loop Stability of the System

```
Clear all
Close all
Clc
s = tf ('s')
%filter transfer function
h1=1/(1+(99.575e-3/70e3)*s+99.575e-3*.11e-6*s^2)                % Load = 70k
% Overall transfer function of filter + Samping Network + PWM
h2=2000*5.04e-4/(1+(99.575e-3/70e3)*s+99.575e-3*.11e-6*s^2)     % Load = 70k
% 5.046e-4(sampling network), 2000(PWM)
% Overall transfer function of filter + sampling Network + PWM; FOR critical load
h3=2000*5.04e-4/(1+(99.575e-3/12e3)*s+99.575e-3*.11e-6*s^2)
% Critical load sqrt (L/C)=12k,5.046e-4(sampling network),2000(PWM)
bode(h1,h2,h3)
% ERROR AMPLIFIER: system (H1) should be stable for critical load
R1=10e3;
R2=27e3;
C1=10e-9;
C2=.1e-9;
h4=2000*1*5.04e-4/(1+(99.575e-3/12e3)*s+99.575e-3*.11e-6*s^2)
%critical load sqrt (L/C)=12k,5.046e-4(sampling network),2000(error amp)
T1=(R2/R1)*(1+R1*C1*s)/(1+R2*C2*s)    %  Error Amplifier Gain
H1=-T1*h4
zpk(h4)
bode(h1)
bode(h1,h4,T1,H1)
rlocus(H1)
```

APPENDIX B

DATA SHEET
OF
IGBT-BSM 35 GB 120 DN2

IGBT Power Module



- Half-bridge
- Including fast free-wheeling diodes
- Doubled diode area
- Package with insulated metal base plate

Type	V_{CE}	I_C	Package	Ordering Code
BSM 35 GB 120 DN2	1200V	50A	HALF-BRIDGE 1	C67070-A2111-A70

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CE}	1200	V
Collector-gate voltage R_{GE} = 20 kΩ	V_{CGR}	1200	
Gate-emitter voltage	V_{GE}	± 20	
DC collector current T_C = 25 °C T_C = 80 °C	I_C	 50 35	A
Pulsed collector current, t_p = 1 ms T_C = 25 °C T_C = 80 °C	I_{Cpuls}	 100 70	
Power dissipation per IGBT T_C = 25 °C	P_{tot}	 280	W
Chip temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	-40 ... + 125	
Thermal resistance, chip case	R_{thJC}	≤ 0.44	K/W
Diode thermal resistance, chip case	R_{thJCD}	≤ 0.8	
Insulation test voltage, t = 1min.	V_{is}	2500	Vac
Creepage distance	-	20	mm
Clearance	-	11	
DIN humidity category, DIN 40 040	-	F	sec
IEC climatic category, DIN IEC 68-1	-	40 / 125 / 56	

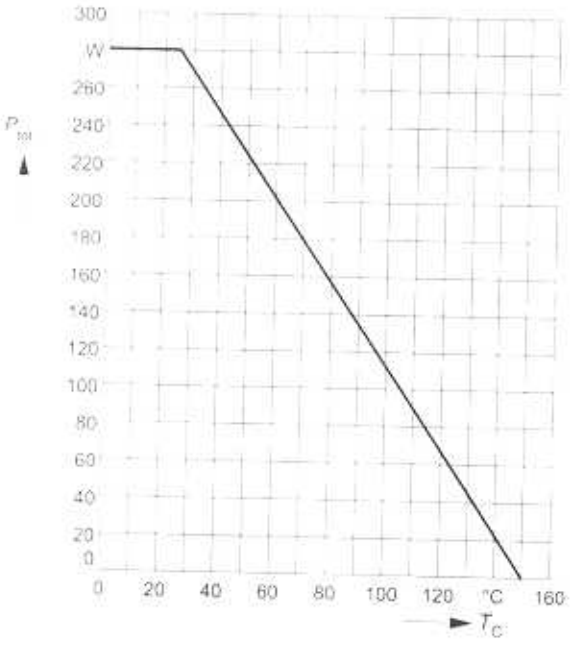
Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Gate threshold voltage $V_{GE} = V_{CE}$, I_C = 1.2 mA	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 35 A, T_j = 25 °C V_{GE} = 15 V, I_C = 35 A, T_j = 125 °C	$V_{CE(sat)}$	- -	2.7 3.3	3.2 3.9	
Zero gate voltage collector current V_{CE} = 1200 V, V_{GE} = 0 V, T_j = 25 °C V_{CE} = 1200 V, V_{GE} = 0 V, T_j = 125 °C	I_{CES}	- -	0.6 2.4	1 -	mA
Gate-emitter leakage current V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	-	-	150	nA
AC Characteristics					
Transconductance V_{CE} = 20 V, I_C = 35 A	g_{fs}	11	-	-	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	-	2	-	nF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	-	0.3	-	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	-	0.14	-	

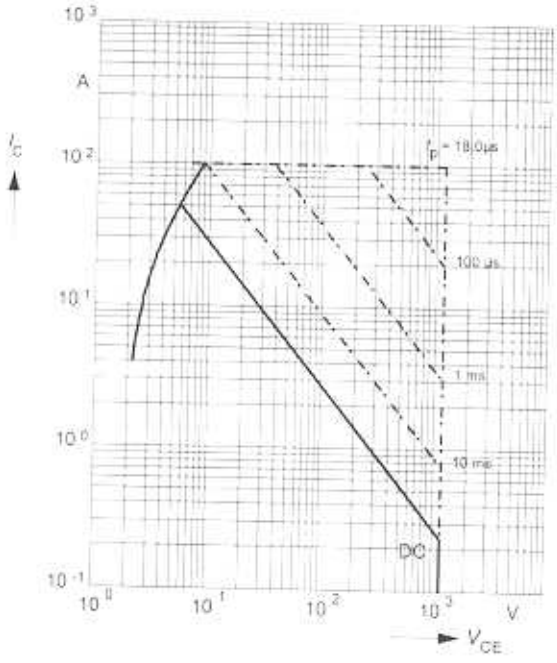
Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Switching Characteristics, Inductive Load at T_j = 125 °C					
Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 35 A R_{Gon} = 39 Ω	$t_{d(on)}$	-	60	120	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 35 A R_{Gon} = 39 Ω	t_r	-	60	120	
Turn-off delay time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 35 A R_{Goff} = 39 Ω	$t_{d(off)}$	-	400	600	
Fall time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 35 A R_{Goff} = 39 Ω	t_f	-	50	75	
Free-Wheel Diode					
Diode forward voltage I_F = 35 A, V_{GE} = 0 V, T_j = 25 °C I_F = 35 A, V_{GE} = 0 V, T_j = 125 °C	V_F	- -	2.3 1.9	2.8 -	V
Reverse recovery time I_F = 35 A, V_R = -600 V, V_{GE} = 0 V di_F/dt = -800 A/µs, T_j = 125 °C	t_{rr}	-	0.25	-	µs
Reverse recovery charge I_F = 35 A, V_R = -600 V, V_{GE} = 0 V di_F/dt = -800 A/µs T_j = 25 °C T_j = 125 °C	Q_{rr}	- -	2 5	- -	µC

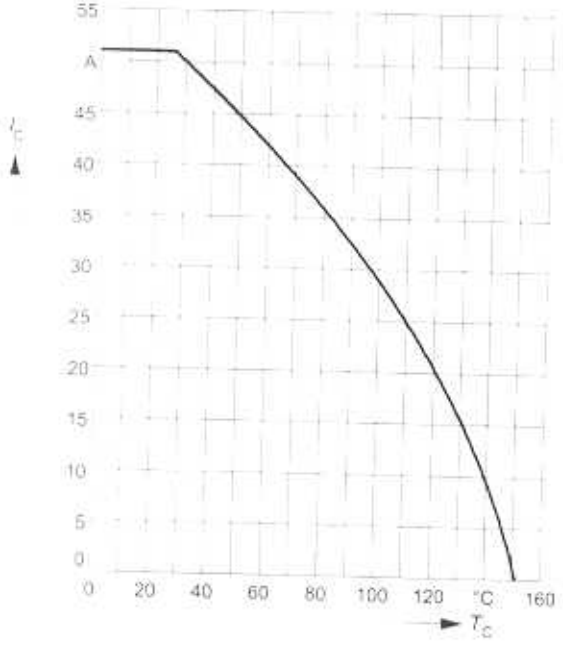
Power dissipation
$P_{tot} = f(T_C)$
parameter: $T_j \leq 150$ °C



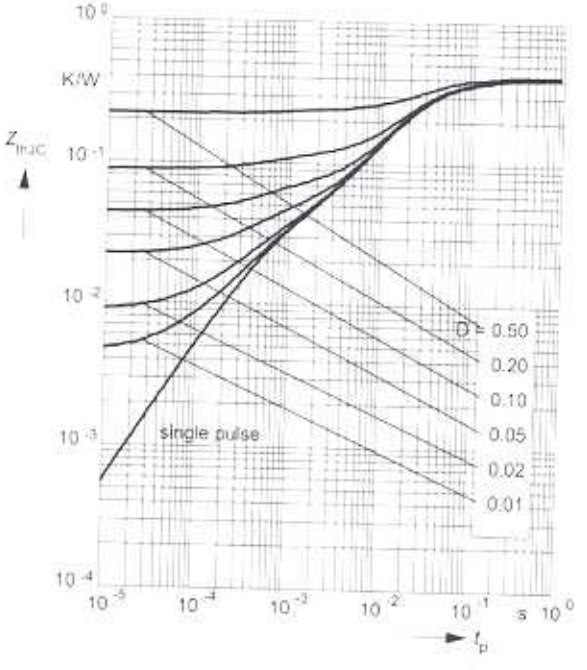
Safe operating area
$I_C = f(V_{CE})$
parameter: $D = 0$, $T_C = 25$°C , $T_j \leq 150$ °C



Collector current
$I_C = f(T_C)$
parameter: $V_{GE} \geq 15$ V , $T_j \leq 150$ °C



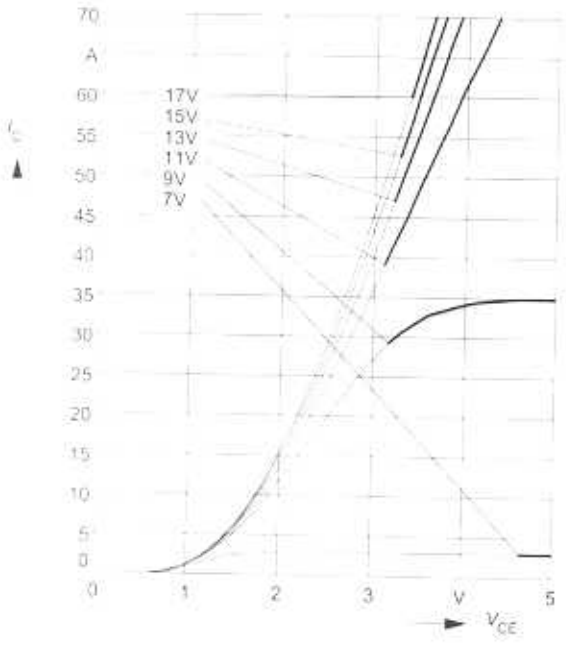
Transient thermal impedance IGBT
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



Typ. output characteristics

$I_C = f(V_{CE})$

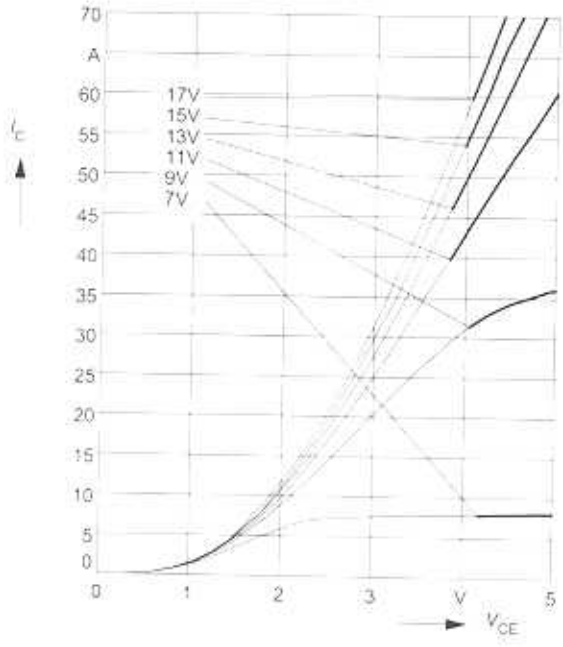
parameter: t_p = 80 µs, T_j = 25 °C



Typ. output characteristics

$I_C = f(V_{CE})$

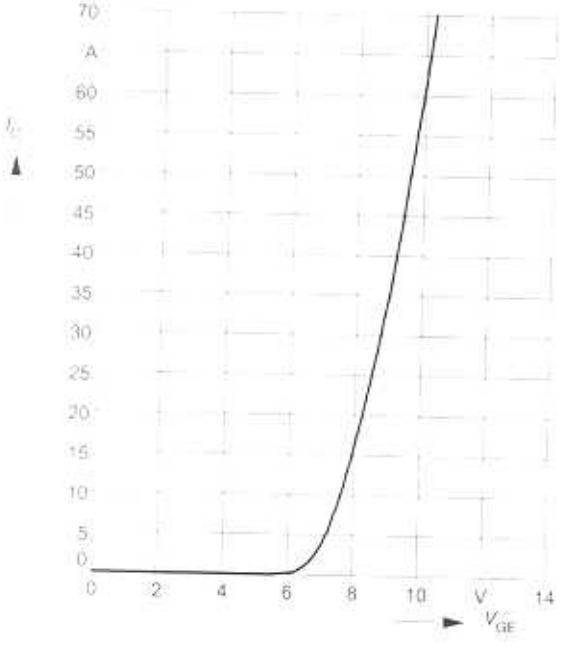
parameter: t_p = 80 µs, T_j = 125 °C



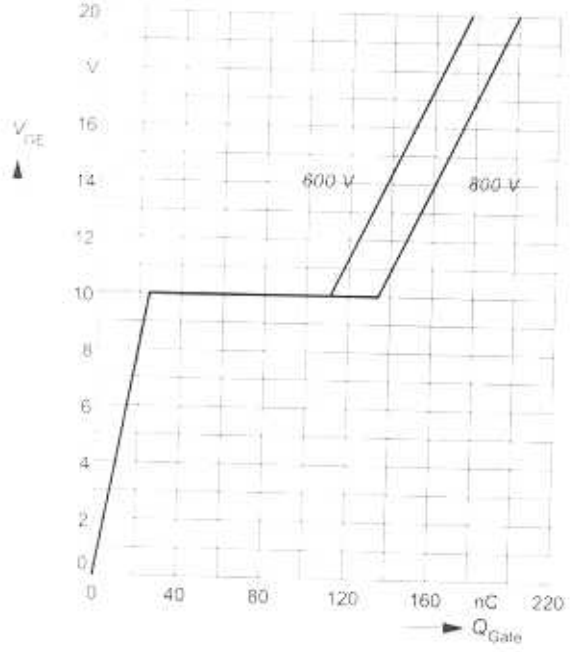
Typ. transfer characteristics

$I_C = f(V_{GE})$

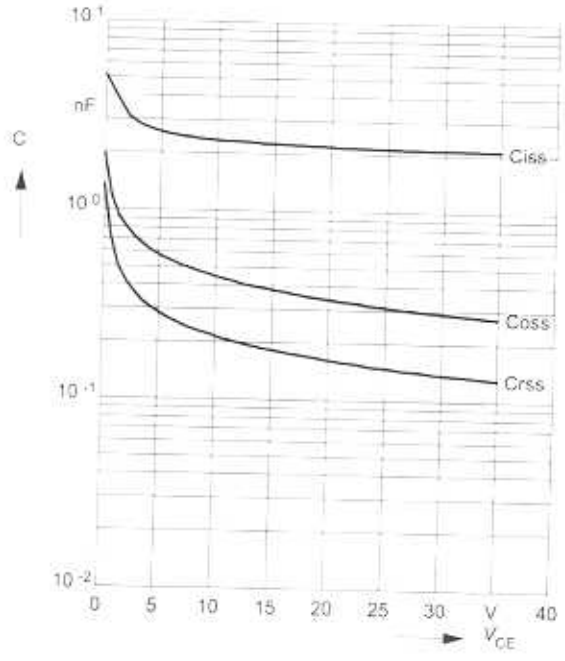
parameter: t_p = 80 µs, V_{CE} = 20 V



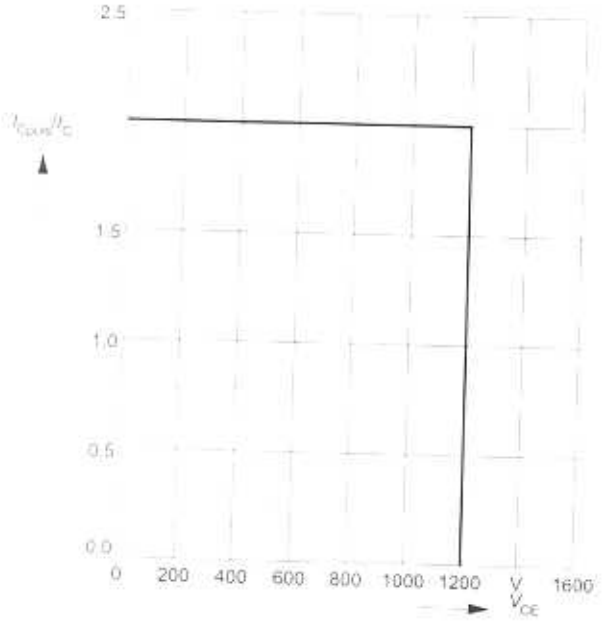
Typ. gate charge
$V_{GE} = f(Q_{Gate})$
parameter: $I_{C\ puls} = 35$ A



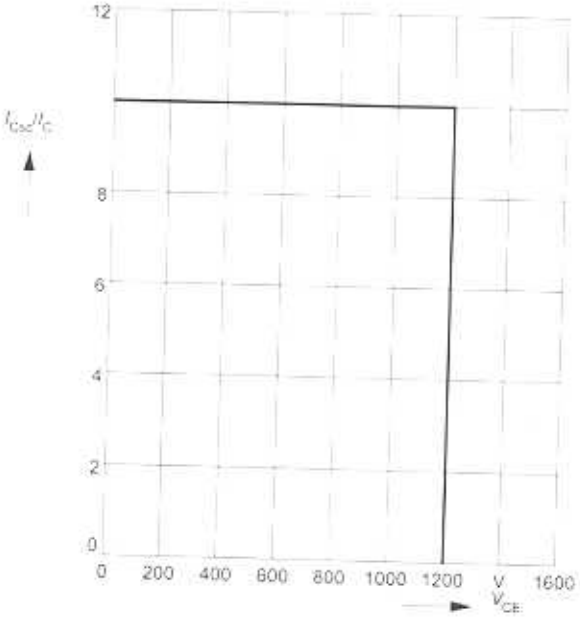
Typ. capacitances
$C = f(V_{CE})$
parameter: $V_{GE} = 0$ V, f = 1 MHz



Reverse biased safe operating area
$I_{Cpuls} = f(V_{CE})$, $T_j = 150°C$
parameter: $V_{GE} = 15$ V



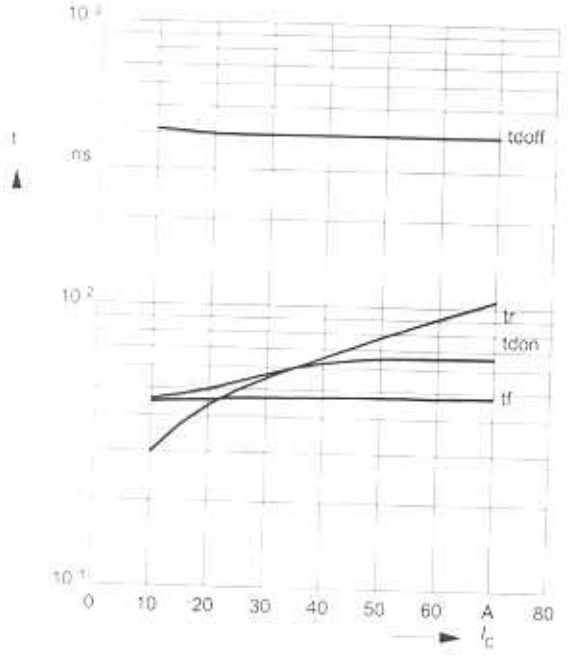
Short circuit safe operating area
$I_{Csc} = f(V_{CE})$, $T_j = 150°C$
parameter: $V_{GE} = \pm 15$ V, $t_{SC} \leq 10$ µs, L < 50 nH



Typ. switching time

$t = f(I_C)$, inductive load , T_j = 125°C

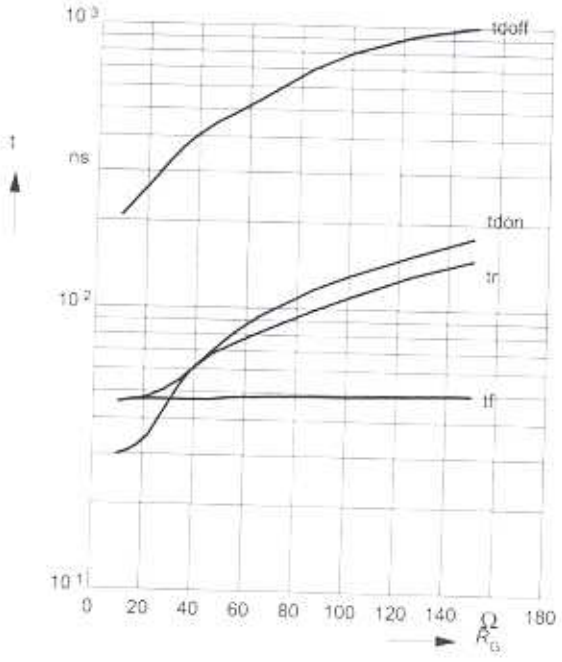
par.: V_{CE} = 600 V, V_{GE} = ± 15 V, R_G = 39 Ω



Typ. switching time

$t = f(R_G)$, inductive load , T_j = 125°C

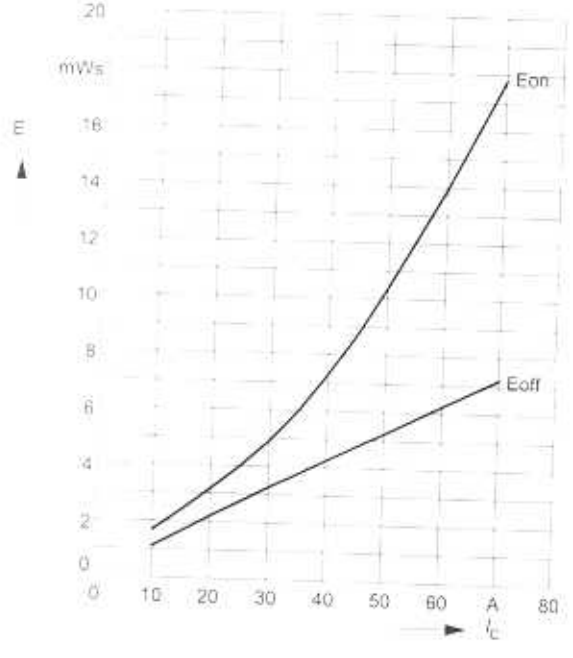
par.: V_{CE} = 600 V, V_{GE} = ± 15 V, I_C = 35 A



Typ. switching losses

$E = f(I_C)$, inductive load , T_j = 125°C

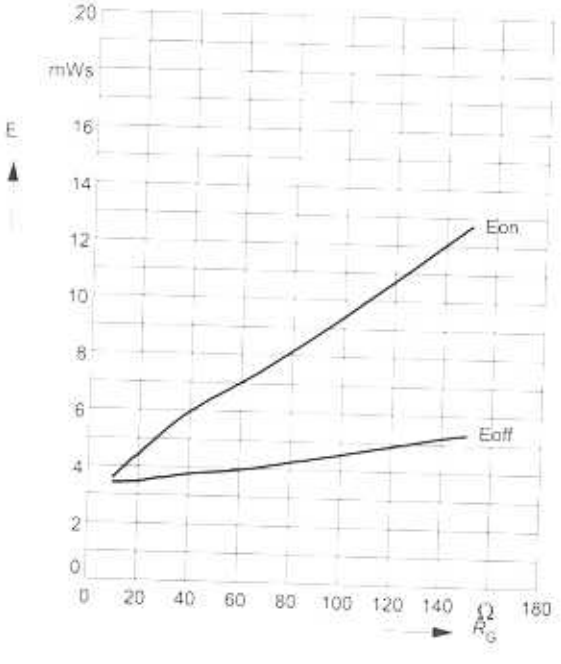
par.: V_{CE} = 600 V, V_{GE} = ± 15 V, R_G = 39 Ω



Typ. switching losses

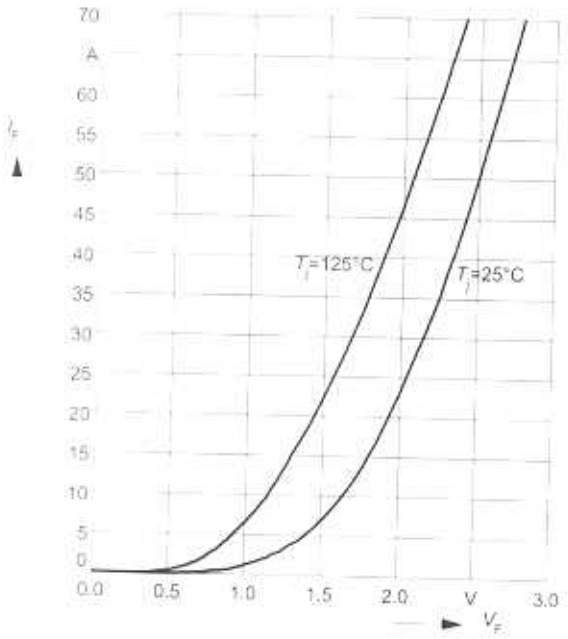
$E = f(R_G)$, inductive load , T_j = 125°C

par.: V_{CE} = 600V, V_{GE} = ± 15 V, I_C = 35 A



Forward characteristics of fast recovery reverse diode $I_F = f(V_F)$

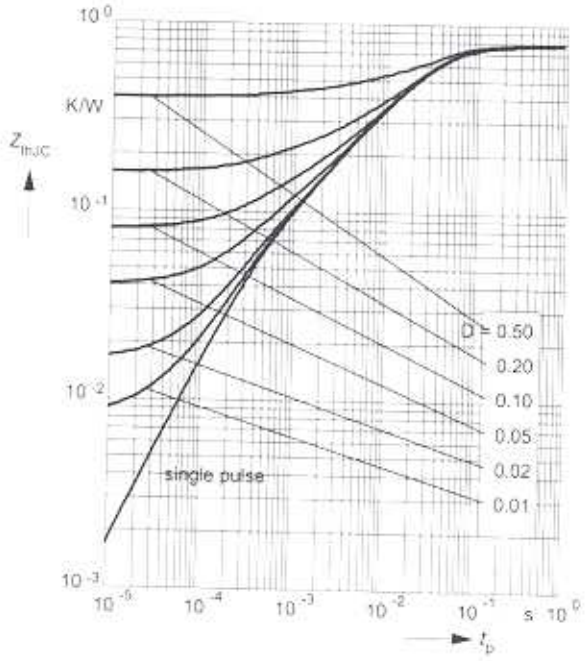
parameter: T_j



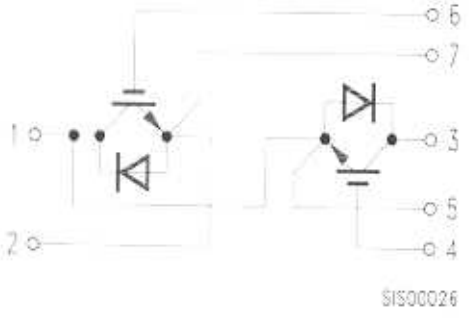
Transient thermal impedance Diode

$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$



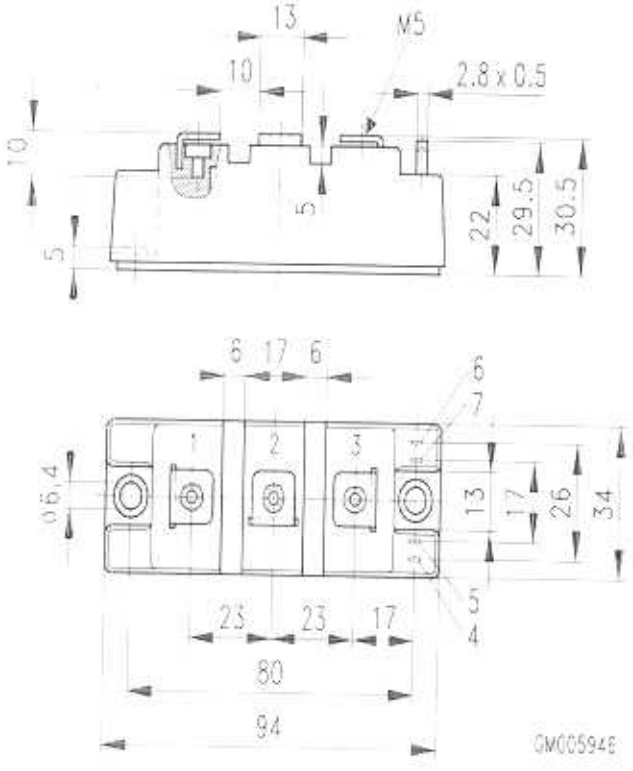
Circuit Diagram



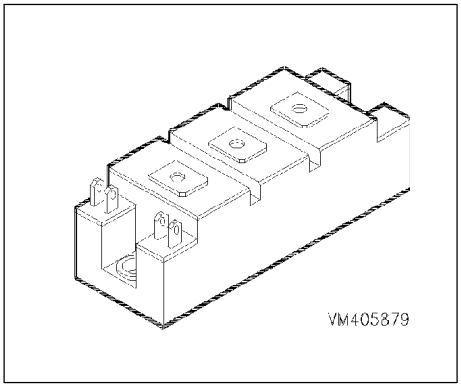
Package Outlines

Dimensions in mm

Weight: 180 g



IGBT Power Module



- Half-bridge
- Including fast free-wheeling diodes
- Doubled diode area
- Package with insulated metal base plate

Type	V_{CE}	I_C	Package	Ordering Code
BSM 35 GB 120 DN2	1200V	50A	HALF-BRIDGE 1	C67070-A2111-A70

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CE}	1200	V
Collector-gate voltage	V_{CGR}		
R_{GE} = 20 kΩ		1200	
Gate-emitter voltage	V_{GE}	± 20	
DC collector current	I_C		A
T_C = 25 °C		50	
T_C = 80 °C		35	
Pulsed collector current, t_p = 1 ms	I_{Cpuls}		
T_C = 25 °C		100	
T_C = 80 °C		70	
Power dissipation per IGBT	P_{tot}		W
T_C = 25 °C		280	
Chip temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	-40 ... + 125	

Thermal resistance, chip case	R_{thJC}	≤ 0.44	K/W
Diode thermal resistance, chip case	R_{thJCD}	≤ 0.8	
Insulation test voltage, t = 1min.	V_{is}	2500	Vac
Creepage distance	-	20	mm
Clearance	-	11	
DIN humidity category, DIN 40 040	-	F	sec
IEC climatic category, DIN IEC 68-1	-	40 / 125 / 56	

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Gate threshold voltage $V_{GE} = V_{CE}$, I_C = 1.2 mA	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 35 A, T_j = 25 °C V_{GE} = 15 V, I_C = 35 A, T_j = 125 °C	$V_{CE(sat)}$	- -	2.7 3.3	3.2 3.9	
Zero gate voltage collector current V_{CE} = 1200 V, V_{GE} = 0 V, T_j = 25 °C V_{CE} = 1200 V, V_{GE} = 0 V, T_j = 125 °C	I_{CES}	- -	0.6 2.4	1 -	mA
Gate-emitter leakage current V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	-	-	150	nA
AC Characteristics					
Transconductance V_{CE} = 20 V, I_C = 35 A	g_{fs}	11	-	-	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	-	2	-	nF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	-	0.3	-	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	-	0.14	-	

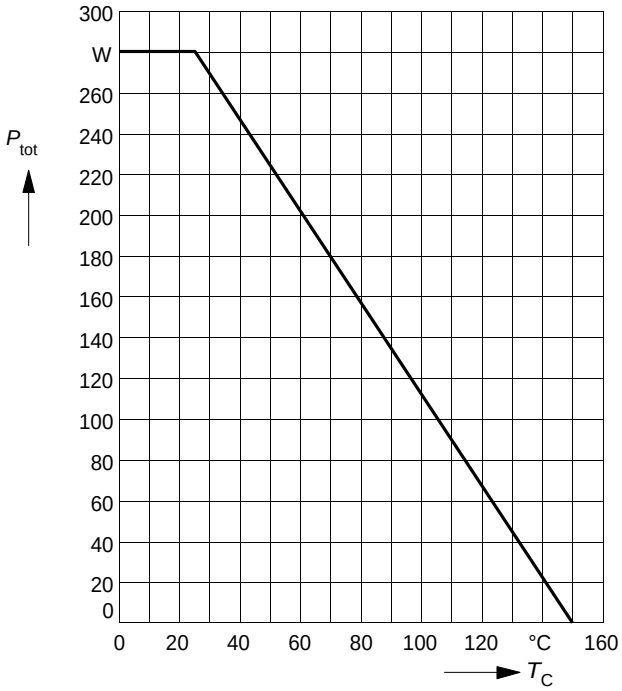
Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Switching Characteristics, Inductive Load at T_j = 125 °C					
Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 35 A R_{Gon} = 39 Ω	$t_{d(on)}$	- -	60 -	120 -	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 35 A R_{Gon} = 39 Ω	t_r	- -	60 -	120 -	
Turn-off delay time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 35 A R_{Goff} = 39 Ω	$t_{d(off)}$	- -	400 -	600 -	
Fall time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 35 A R_{Goff} = 39 Ω	t_f	- -	50 -	75 -	
Free-Wheel Diode					
Diode forward voltage I_F = 35 A, V_{GE} = 0 V, T_j = 25 °C I_F = 35 A, V_{GE} = 0 V, T_j = 125 °C	V_F	- -	2.3 1.9	2.8 -	V
Reverse recovery time I_F = 35 A, V_R = -600 V, V_{GE} = 0 V di_F/dt = -800 A/µs, T_j = 125 °C	t_{rr}	-	0.25	-	µs
Reverse recovery charge I_F = 35 A, V_R = -600 V, V_{GE} = 0 V di_F/dt = -800 A/µs T_j = 25 °C T_j = 125 °C	Q_{rr}	- -	2 5	- -	µC

Power dissipation

$P_{tot} = f(T_C)$

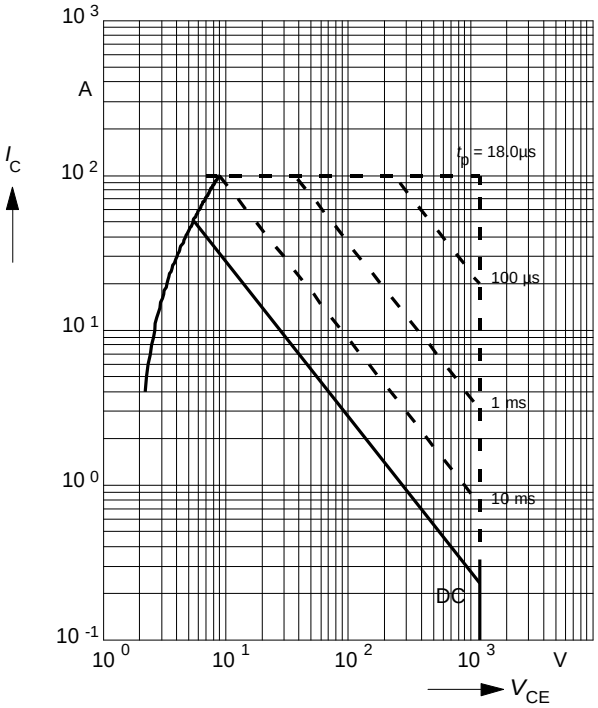
parameter: $T_j \leq 150$ °C



Safe operating area

$I_C = f(V_{CE})$

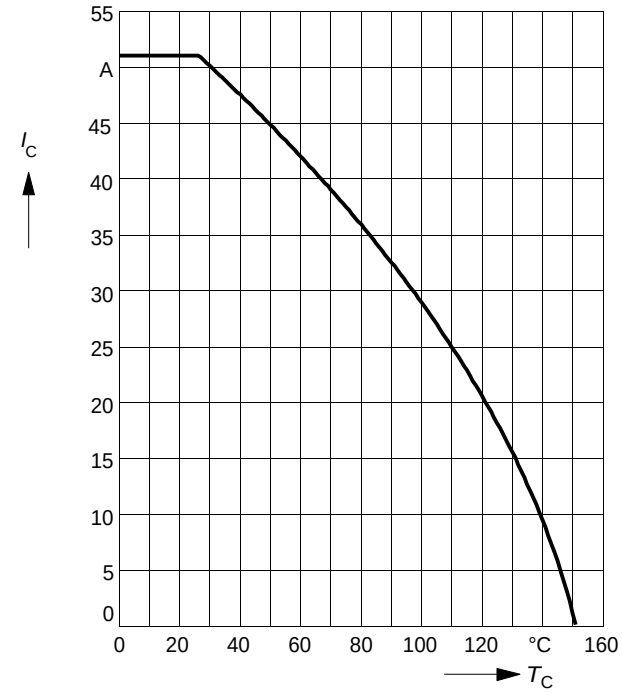
parameter: $D = 0$, $T_C = 25$°C , $T_j \leq 150$ °C



Collector current

$I_C = f(T_C)$

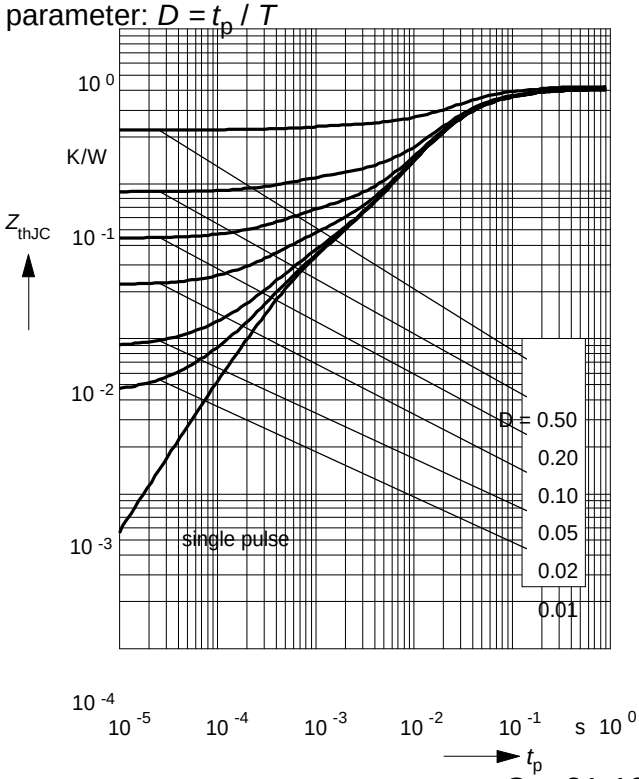
parameter: $V_{GE} \geq 15$ V , $T_j \leq 150$ °C



Transient thermal impedance IGBT

$Z_{th\,JC} = f(t_p)$

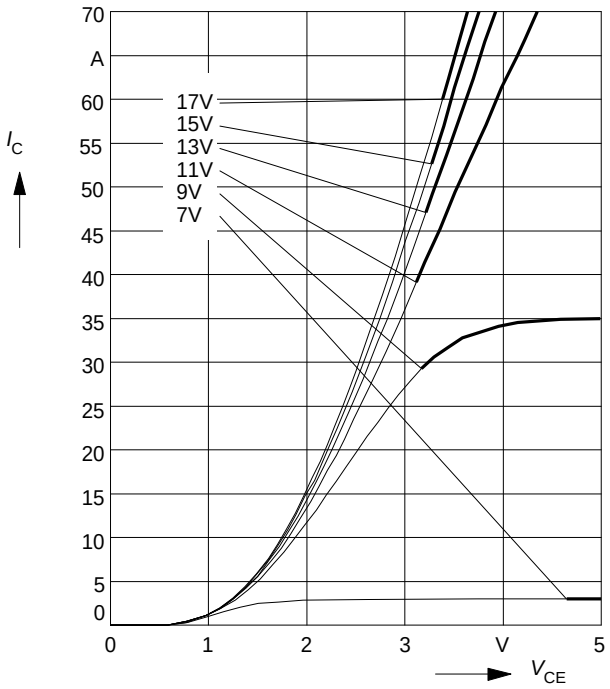
parameter: $D = t_p / T$



Typ. output characteristics

$I_C = f(V_{CE})$

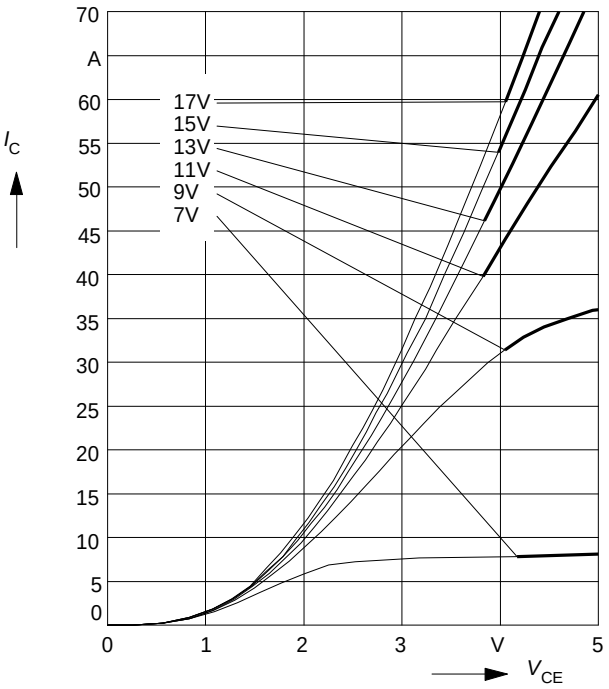
parameter: t_p = 80 µs, T_j = 25 °C



Typ. output characteristics

$I_C = f(V_{CE})$

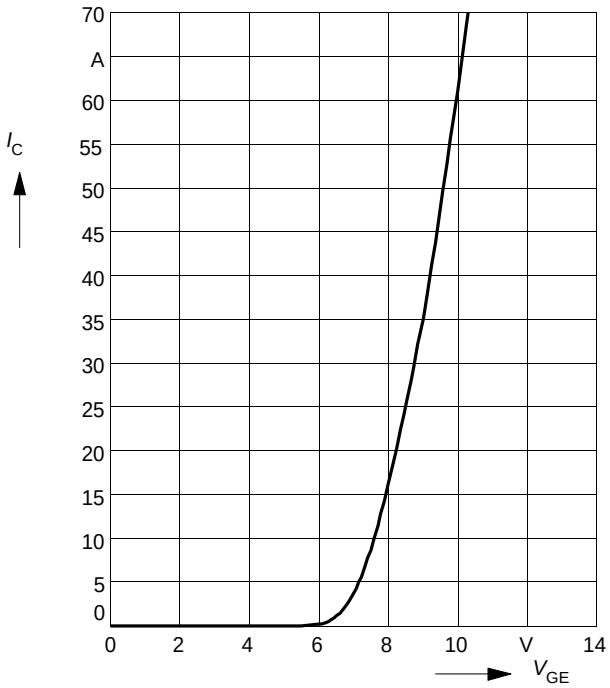
parameter: t_p = 80 µs, T_j = 125 °C



Typ. transfer characteristics

$I_C = f(V_{GE})$

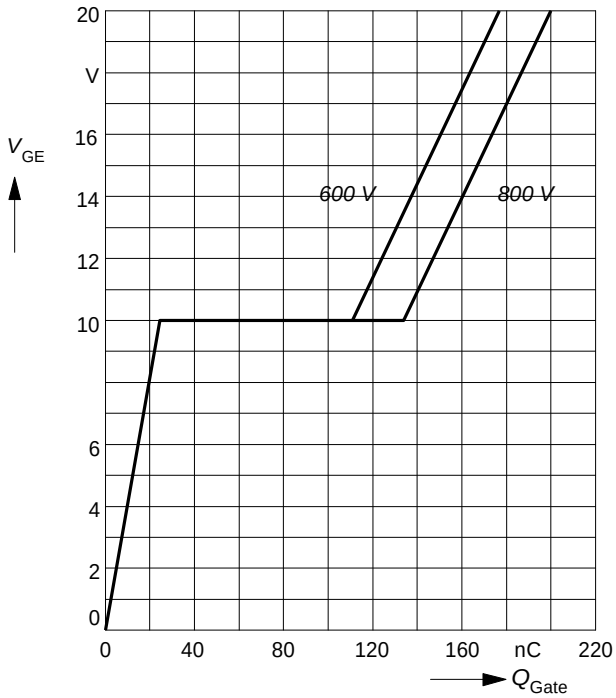
parameter: t_p = 80 µs, V_{CE} = 20 V



Typ. gate charge

$V_{GE} = f(Q_{Gate})$

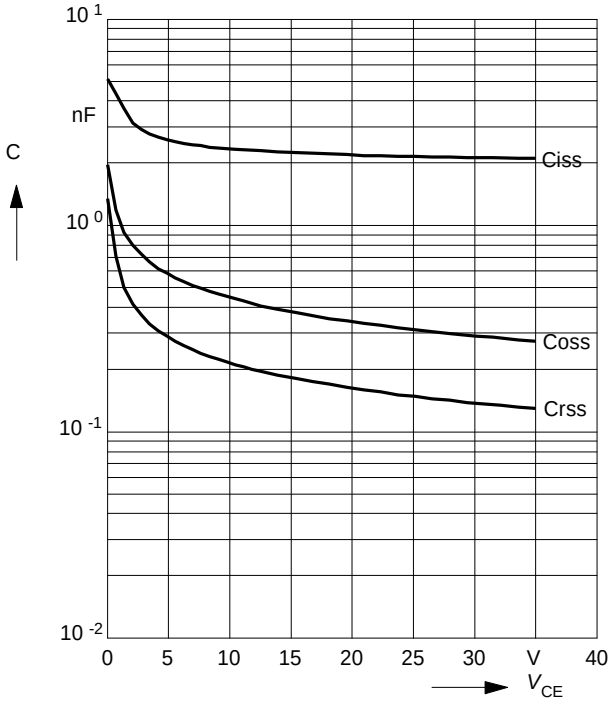
parameter: $I_{C\ puls}$ = 35 A



Typ. capacitances

$C = f\ (V_{CE})$

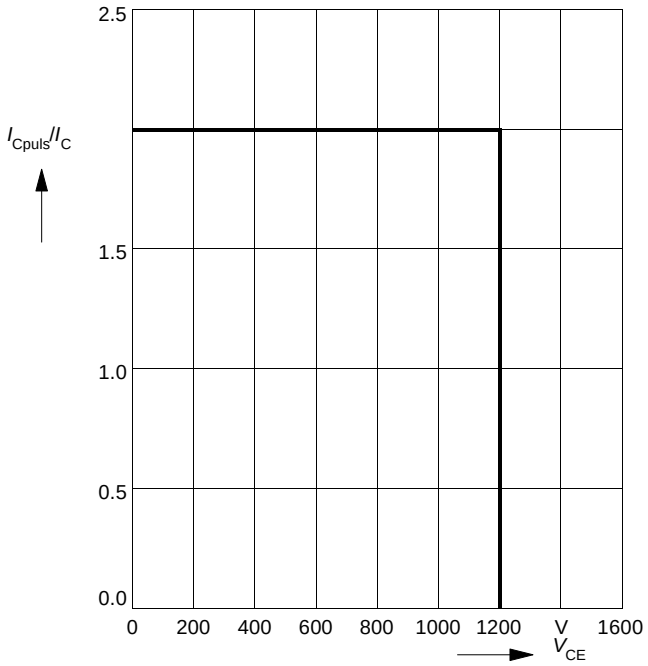
parameter: V_{GE} = 0 V, f = 1 MHz



Reverse biased safe operating area

$I_{Cpuls} = f(V_{CE})$, T_j = 150°C

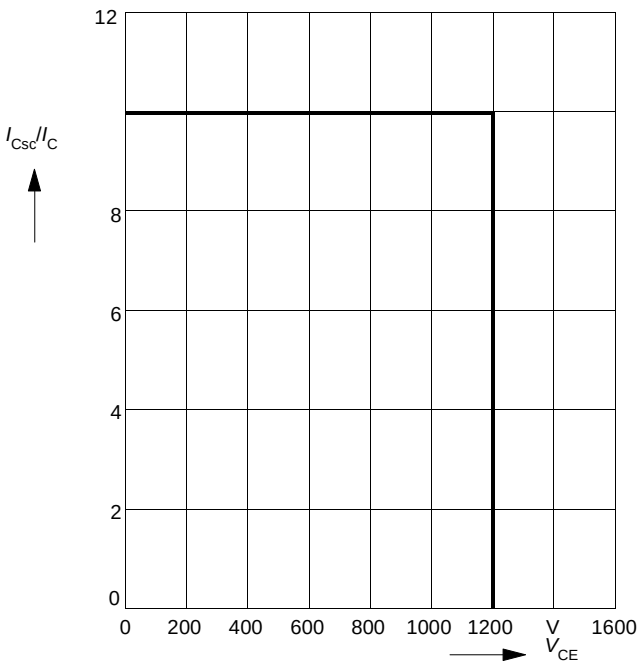
parameter: V_{GE} = 15 V



Short circuit safe operating area

$I_{Csc} = f(V_{CE})$, T_j = 150°C

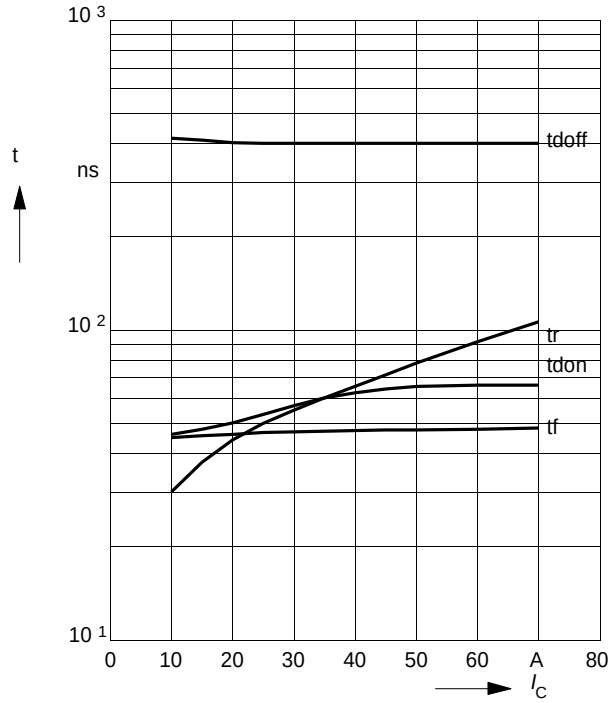
parameter: V_{GE} = ± 15 V, $t_{SC} \leq$ 10 µs, L < 50 nH



Typ. switching time

$I = f(I_C)$, inductive load , T_j = 125°C

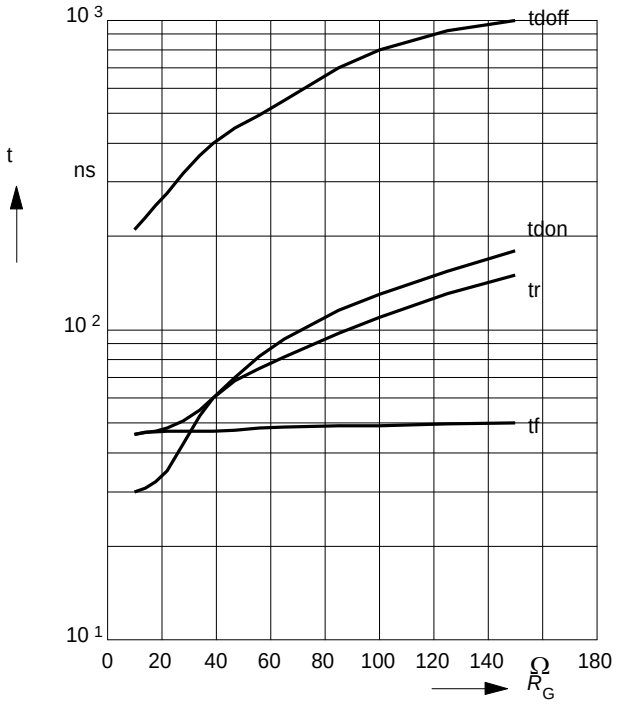
par.: V_{CE} = 600 V, V_{GE} = ± 15 V, R_G = 39 Ω



Typ. switching time

$t = f(R_G)$, inductive load , T_j = 125°C

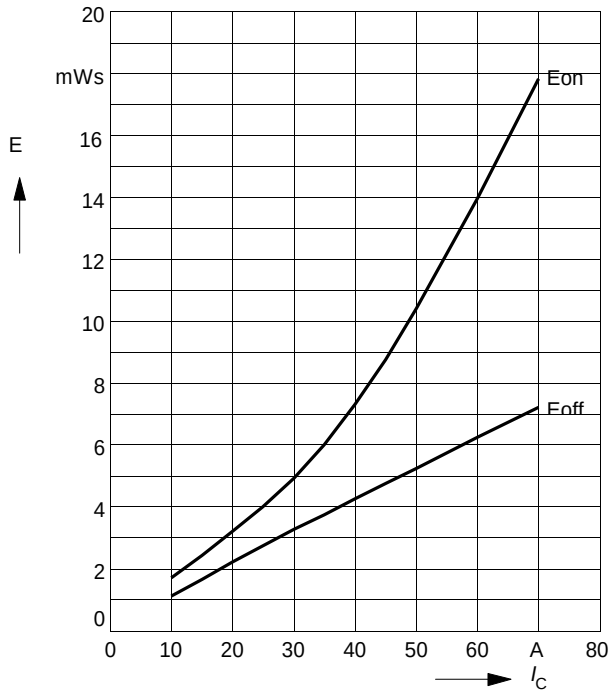
par.: V_{CE} = 600 V, V_{GE} = ± 15 V, I_C = 35 A



Typ. switching losses

$E = f(I_C)$, inductive load , T_j = 125°C

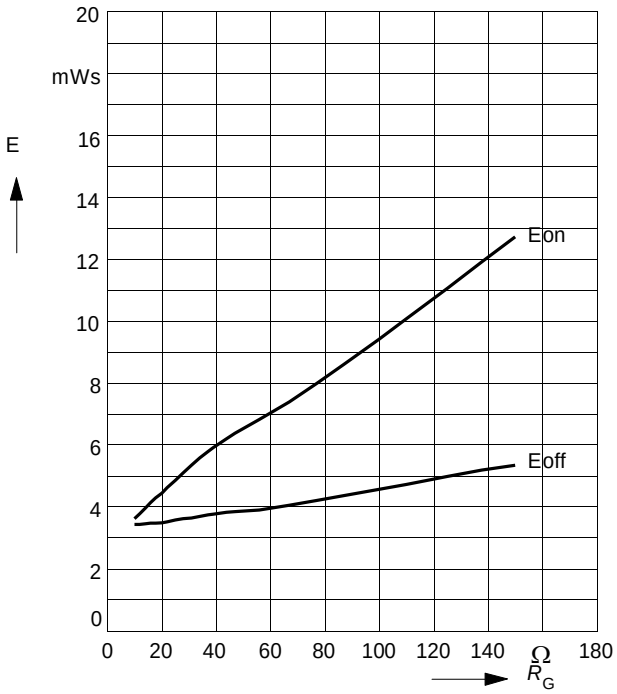
par.: V_{CE} = 600 V, V_{GE} = ± 15 V, R_G = 39 Ω



Typ. switching losses

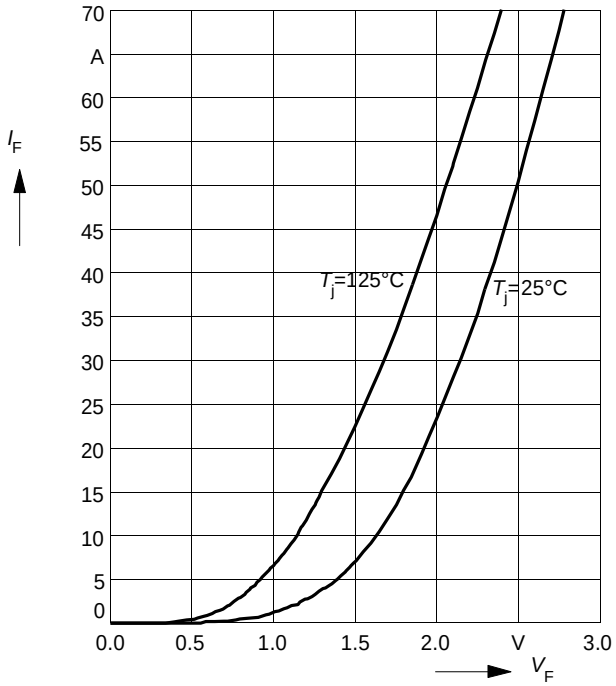
$E = f(R_G)$, inductive load , T_j = 125°C

par.: V_{CE} = 600V, V_{GE} = ± 15 V, I_C = 35 A



Forward characteristics of fast recovery reverse diode $I_F = f(V_F)$

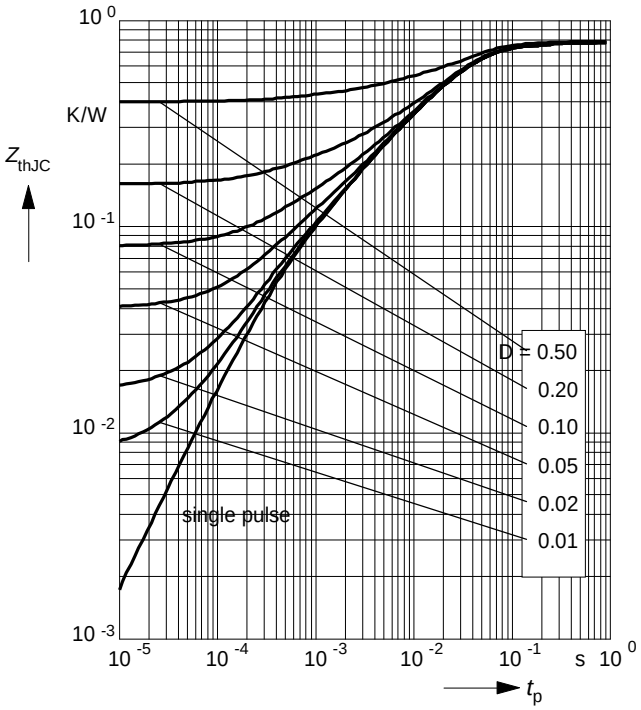
parameter: T_j



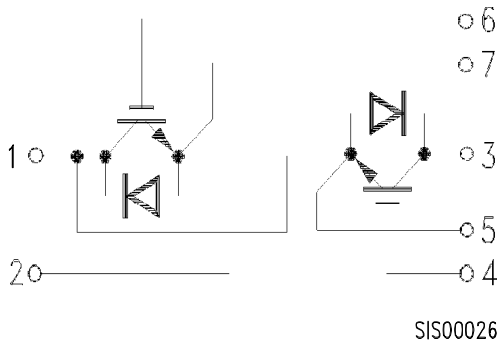
Transient thermal impedance Diode

$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$



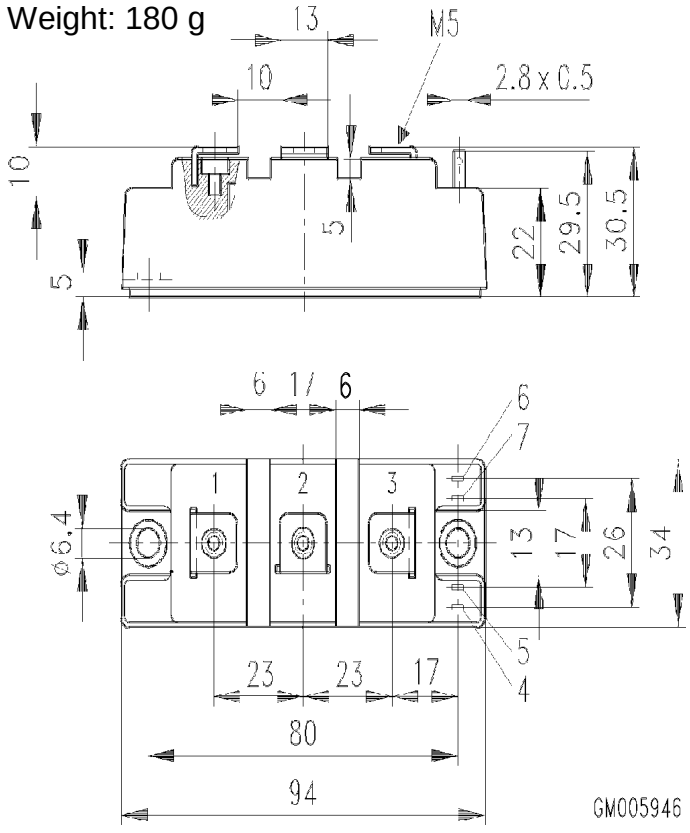
Circuit Diagram



Package Outlines

Dimensions in mm

Weight: 180 g



APPENDIX C

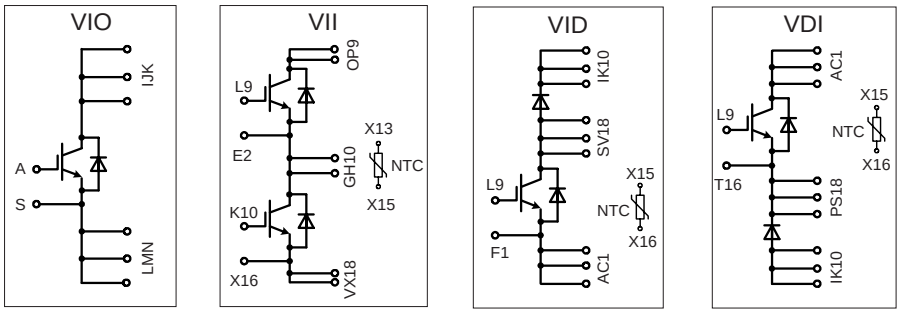
DATA SHEET
OF
IGBT- VII 130-06P1

IGBT Modules in ECO-PAC 2

Short Circuit SOA Capability
Square RBSOA

Preliminary data sheet

I_{C25} = 121 A
V_{CES} = 600 V
$V_{CE(sat)\ typ.}$ = 2.3 V



Pin arangement see outlines

IGBTs

Symbol	Conditions	Maximum Ratings	
V_{CES}	T_{VJ} = 25°C to 150°C	600	V
V_{GES}		± 20	V
I_{C25}	T_C = 25°C	121	A
I_{C80}	T_C = 80°C	83	A
I_{CM}	V_{GE} = ±15 V; R_G = 2.2 Ω; T_{VJ} = 125°C	200	A
V_{CEK}	RBSOA, Clamped inductive load; L = 100 µH	360	V
t_{SC} (SCSOA)	V_{CE} = V_{CES}; V_{GE} = ±15 V; R_G = 2.2 Ω; T_{VJ} = 125°C non-repetitive	10	µs
P_{tot}	T_C = 25°C	379	W

Symbol	Conditions	Characteristic Values (T_{VJ} = 25°C, unless otherwise specified) min.	typ.	max.	
$V_{CE(sat)}$	I_C = 130 A; V_{GE} = 15 V; T_{VJ} = 25°C		2.3	2.9	V
	T_{VJ} = 125°C		2.6		V
$V_{GE(th)}$	I_C = 1.5 mA; V_{GE} = V_{CE}	4.5		6.5	V
I_{CES}	V_{CE} = V_{CES}; V_{GE} = 0 V; T_{VJ} = 25°C			1.2	mA
	T_{VJ} = 125°C			7.5	mA
I_{GES}	V_{CE} = 0 V; V_{GE} = ± 20 V			400	nA
$t_{d(on)}$	Inductive load, T_{VJ} = 125°C		25		ns
t_r	V_{CE} = 300 V; I_C = 80 A		11		ns
$t_{d(off)}$	V_{GE} = 15/0 V; R_G = 2.2 Ω		150		ns
t_f			30		ns
E_{on}			0.8		mJ
E_{off}			2.3		mJ
C_{ies}	V_{CE} = 25 V; V_{GE} = 0 V; f = 1 MHz		4.2		nF
R_{thJC}	(per IGBT)			0.33	K/W
R_{thJH}	with heatsink compound (0.42 K/m.K; 50 µm)		0.66		K/W

Features

- NPT IGBT's
  - positive temperature coefficient of saturation voltage
  - fast switching
- FRED diodes
  - fast reverse recovery
  - low forward voltage
- Industry Standard Package
  - solderable pins for PCB mounting
  - isolated DCB ceramic base plate

Advantages

- space and weight savings
- reduced protection circuits
- leads with expansion bend for stress relief

Typical Applications

- AC and DC motor control
- AC servo and robot drives
- power supplies
- welding inverters

IXYS reserves the right to change limits, test conditions and dimensions.

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Reverse diodes (FRED)

Symbol	Conditions	Maximum Ratings	
I_{F25}	T_C = 25°C	134.0	A
I_{F80}	T_C = 80°C	82.3	A

Symbol	Conditions	Characteristic Values min.	typ.	max.	
V_F	I_F = 80 A; T_{VJ} = 25°C		1.85	2.06	V
	T_{VJ} = 125°C		1.40		V
I_{RM}	I_F = 60 A; di_F/dt = 500 A/µs; T_{VJ} = 125°C		28		A
t_{rr}	V_R = 300 V; V_{GE} = 0 V		100		ns
R_{thJC}				0.66	K/W
R_{thJH}	with heatsink compound (0.42 K/m.K; 50 µm)		1.32		K/W

Temperature Sensor NTC

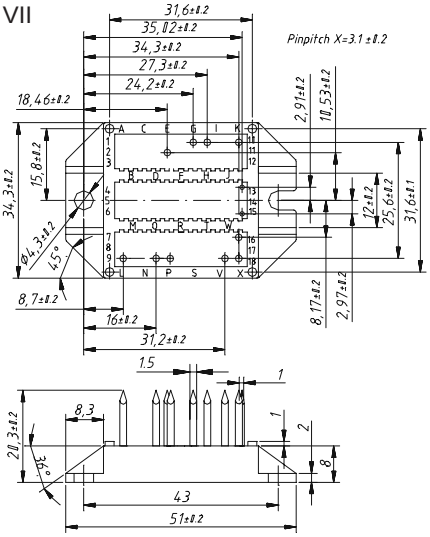
Symbol	Conditions	Characteristic Values min.	typ.	max.	
R_{25}	T = 25°C	4.75	5.0	5.25	kΩ
$B_{25/50}$			3375		K

Module

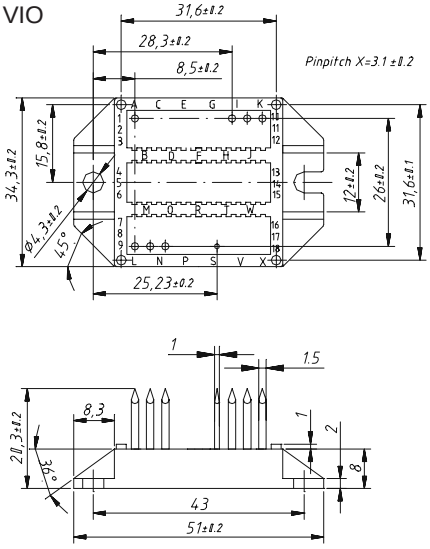
Symbol	Conditions	Maximum Ratings	
T_{VJ}		-40...+150	°C
T_{stg}		-40...+150	°C
V_{ISOL}	$I_{ISOL} \leq$ 1 mA; 50/60 Hz	3000	V~
M_d	mounting torque (M4)	1.5 - 2.0	Nm
		14 - 18	lb.in.
a	Max. allowable acceleration	50	m/s^2

Symbol	Conditions	Characteristic Values min.	typ.	max.	
d_S	Creepage distance on surface (Pin to heatsink)	11.2			mm
d_A	Strike distance in air (Pin to heatsink)	11.2			mm
Weight			24		g

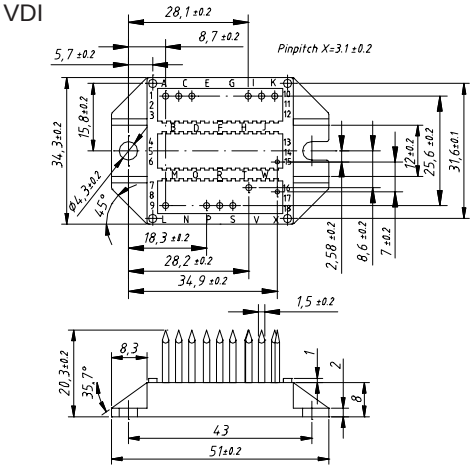
VII



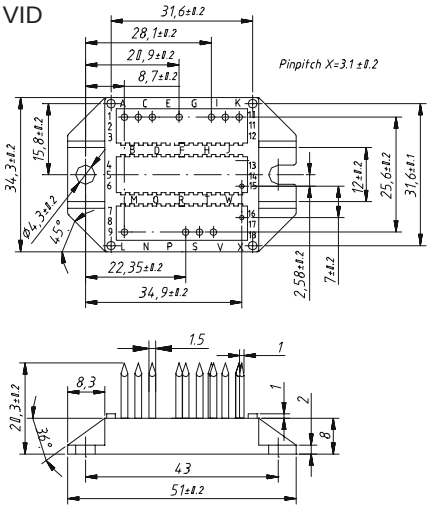
VIO



VDI



VID



Data according to IEC 60747 and refer to a single transistor or diode unless otherwise stated.
IXYS reserves the right to change limits, test conditions and dimensions.

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APPENDIX D

DATA SHEET
OF
IGBT- SKM 75GB063D

SKM 75GB063D ...

SEMITRANS™ 2

Superfast NPT-IGBT Modules

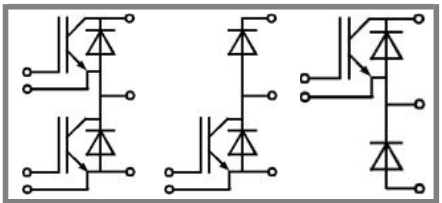
SKM 75GB063D
SKM 75GAR063D
SKM 75GAL063D

Features

- N channel, homogeneous Si-structure (NPT-Non punch-through IGBT)
- Low tail current with low temperature dependence
- High short circuit capability, self limiting if term. G is clamped to E
- Pos. temp.-coeff. of V_{CEsat}
- Very low C_{ies}, C_{oes}, C_{res}
- Latch-up free
- Fast & soft inverse CAL diodes
- Isolated copper baseplate using DBC Direct Copper Bonding Technology without hard mould
- Large clearance (10 mm) and creepage distances (20 mm)

Typical Applications

- Switching (not for linear use)
- Switched mode power supplies
- UPS
- Three phase inverters for servo / AC motor speed control
- Pulse fre4uencies also 5 106H7



GB GAL GAR

Absolute Maximum Ratings	T_c 8 25 °C, unless otherwise specified		
Symbol	**Conditions**	**Values**	**Units**
IGBT			
V_{CES}		600	V
I_C	T_c 8 25 (75) °C	100 (75)	A
I_{CRM}	t_p 8 1 ms	150	A
V_{GES}		@ 20	V
T_{vj}, (T_{stg})	$T_{OPERATION}$ C T_{stg}	- 40 ... + (125) 150	°C
V_{isol}	AC, 1 min.	2500	V
Inverse diode			
I_F	T_c 8 25 (80) °C	75 (50)	A
I_{FRM}	t_p 8 1 ms	150	A
I_{FSM}	t_p 8 10 ms; sin.; T_j 8 150 °C	440	A
Freewheeling diode			
I_F	T_c 8 25 (80) °C	100 (75)	A
I_{FRM}	t_p 8 1 ms	200	A
I_{FSM}	t_p 8 10 ms; sin; T_j 8 150 °C	720	A

Characteristics	T_c 8 25 °C, unless otherwise specified				
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Units**
IGBT					
$V_{GE(th)}$	V_{GE} 8 V_{CE}, I_C 8 1 mA	4,5	5,5	6,5	V
I_{CES}	V_{GE} 8 0, V_{CE} 8 V_{CES}, T_j 8 25 (125) °C		0,1	0,3	mA
$V_{CE(TO)}$	T_j 8 25 (125) °C		1,05 (1)		V
r_{CE}	V_{GE} 8 15 V, T_j 8 25 (125) °C		14 (18,7)		mO
$V_{CE(sat)}$	I_{Cnom} 8 75 A, V_{GE} 8 15 V, chip level		2,1 (2,4)	2,5 (2,8)	V
C_{ies}	under following conditions		4,2		nF
C_{oes}	V_{GE} 8 0, V_{CE} 8 25 V, f 8 1 MH7		0,5		nF
C_{res}			0,3		nF
L_{CE}				30	nH
$R_{CC'+EE'}$	res., terminal-chip T_c8 25 (125) °C		0,75 (1)		mO
$t_{d(on)}$	V_{CC} 8 300 V, I_{Cnom} 8 75 A		60		ns
t_r	R_{Gon} 8 R_{Goff} 8 15 O, T_j 8 125 °C		50		ns
$t_{d(off)}$	V_{GE} 8 @ 15 V		350		ns
t_f			35		ns
E_{on} (E_{off})			3 (2,5)		mJ
Inverse diode					
V_F 8 V_{EC}	I_{Fnom} 8 75 A; V_{GE} 8 0 V; T_j 8 25 (125) °C		1,55 (1,55)	1,9	V
$V_{(TO)}$	T_j 8 125 () °C			0,9	V
r_T	T_j 8 125 () °C		10	13,3	mO
I_{RRM}	I_{Fnom} 8 75 A; T_j 8 125 () °C		30		A
Q_{rr}	di/dt 8 800 A/ps		3,7		pC
E_{rr}	V_{GE} 8 0 V				mJ
FWD					
V_F 8 V_{EC}	I_F 8 100 A; V_{GE} 8 0 V, T_j 8 25 (125) °C		1,55 (1,55)	1,9	V
$V_{(TO)}$	T_j 8 125 () °C			0,9	V
r_T	T_j 8 125 () °C		8	10	mO
I_{RRM}	I_F 8 100 A; T_j 8 125 () °C		44		A
Q_{rr}	di/dt 8 0 A/ps		6		pC
E_{rr}	V_{GE} 8 V				mJ
Thermal characteristics					
$R_{th(j-c)}$	per IGBT			0,35	K/W
$R_{th(j-c)D}$	per Inverse Diode			1	K/W
$R_{th(j-c)FD}$	per FWD			0,6	K/W
$R_{th(c-s)}$	per module			0,05	K/W
Mechanical data					
M_s	to heatsin6 M6	3		5	Nm
M_t	to terminals M5	2,5		5	Nm
w				160	g

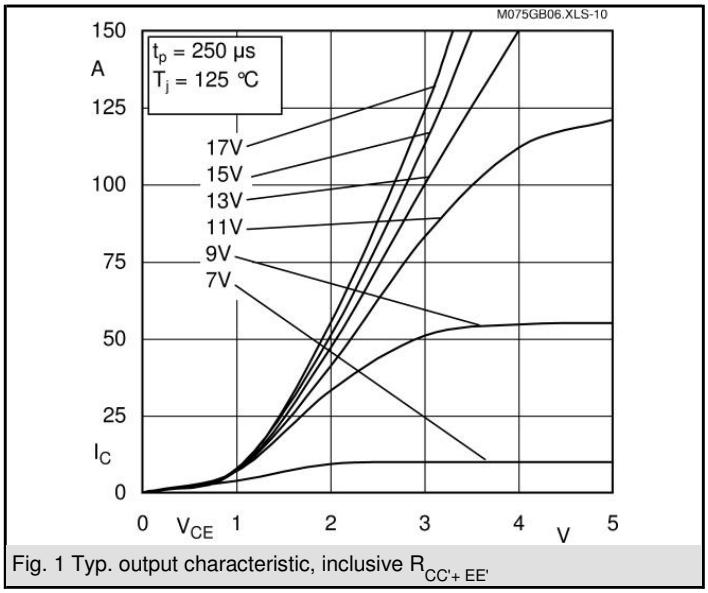


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

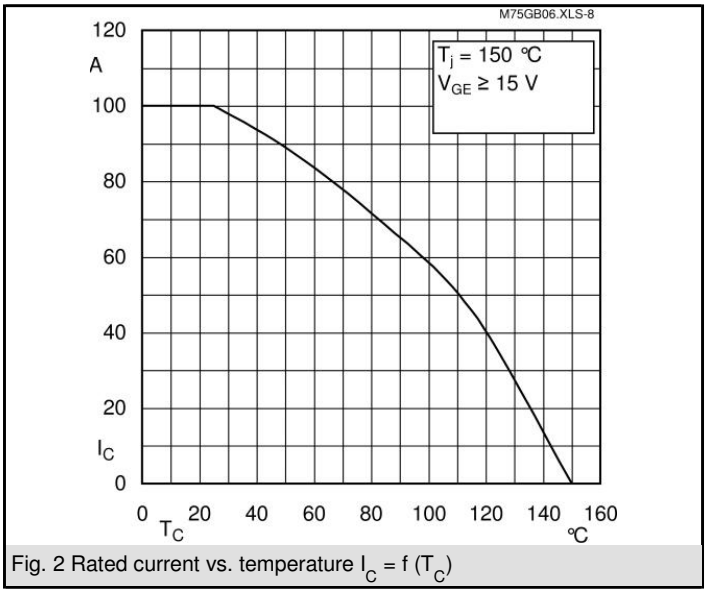


Fig. 2 Rated current vs. temperature $I_C = f(T_C)$

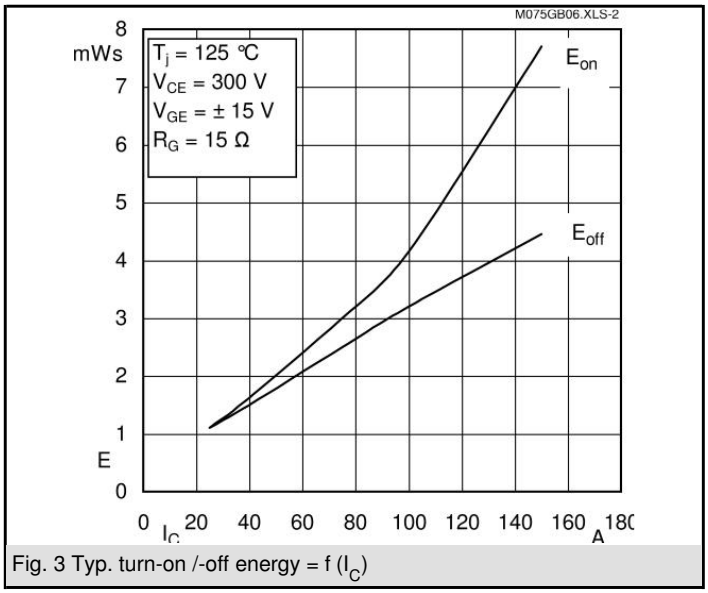


Fig. 3 Typ. turn-on /-off energy = f (I_C)

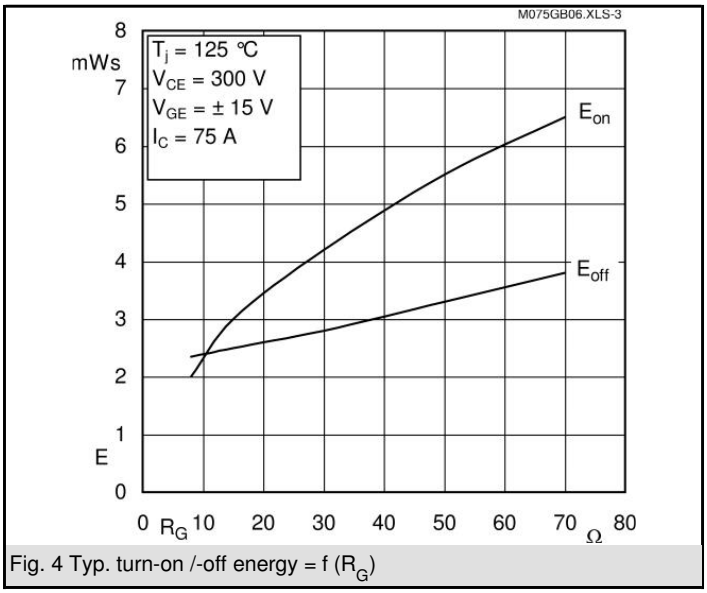


Fig. 4 Typ. turn-on /-off energy = f (R_G)

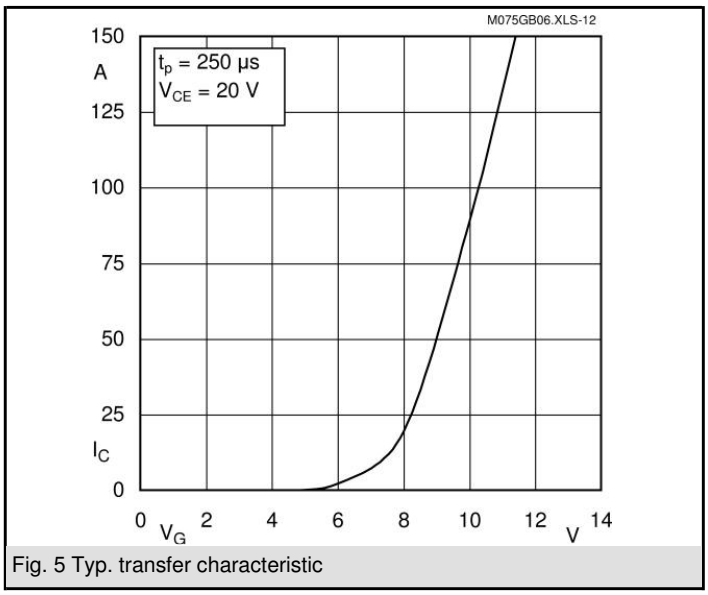


Fig. 5 Typ. transfer characteristic

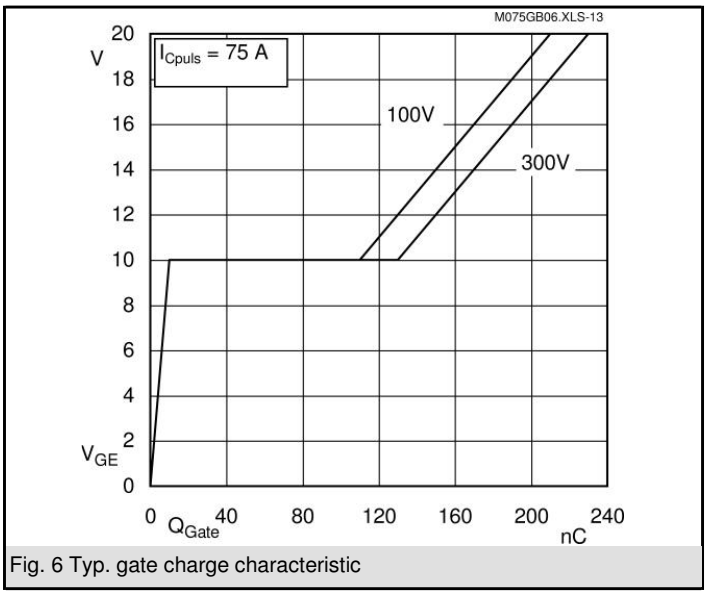


Fig. 6 Typ. gate charge characteristic

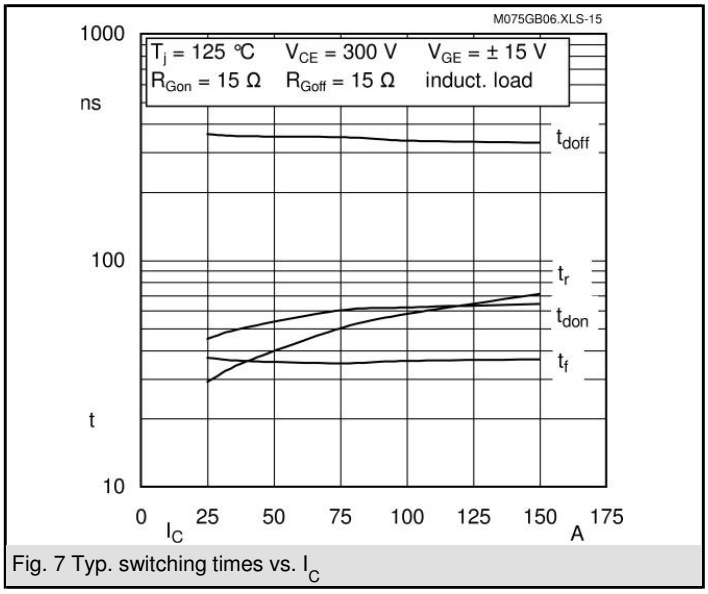


Fig. 7 Typ. switching times vs. I_C

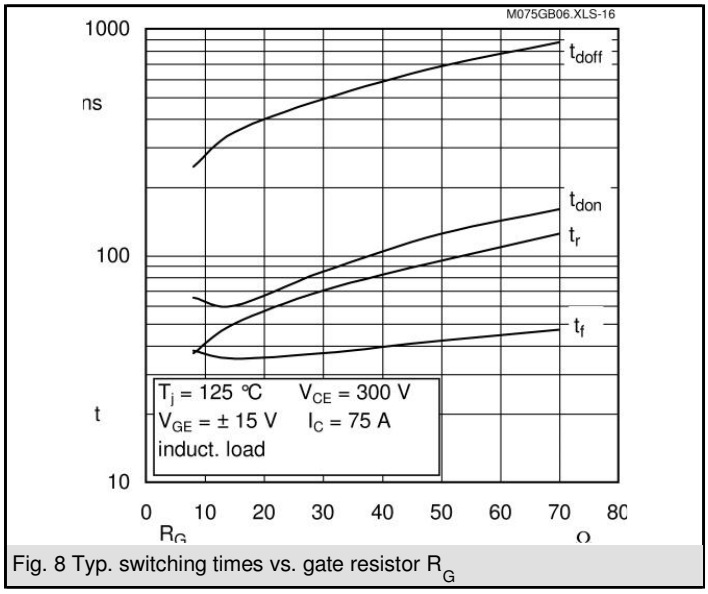


Fig. 8 Typ. switching times vs. gate resistor R_G

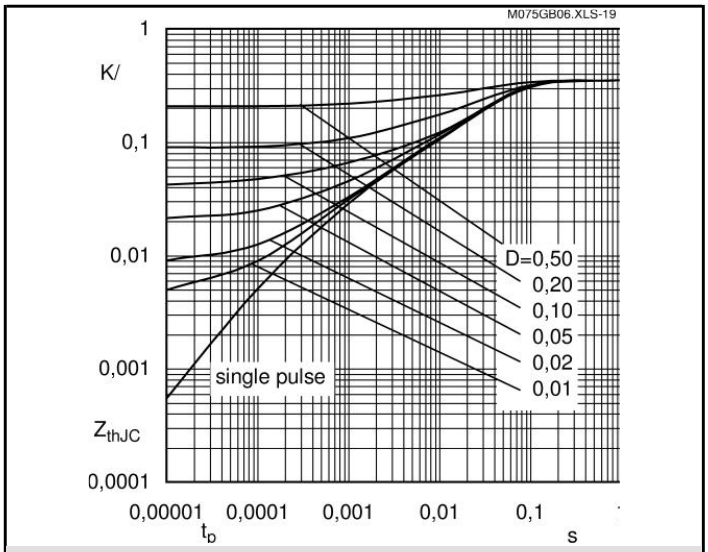


Fig. 9 Transient thermal impedance of IGBT

$Z_{thp(j-c)} = f(t_p)$; $D = t_p/t_c = t_p * f$

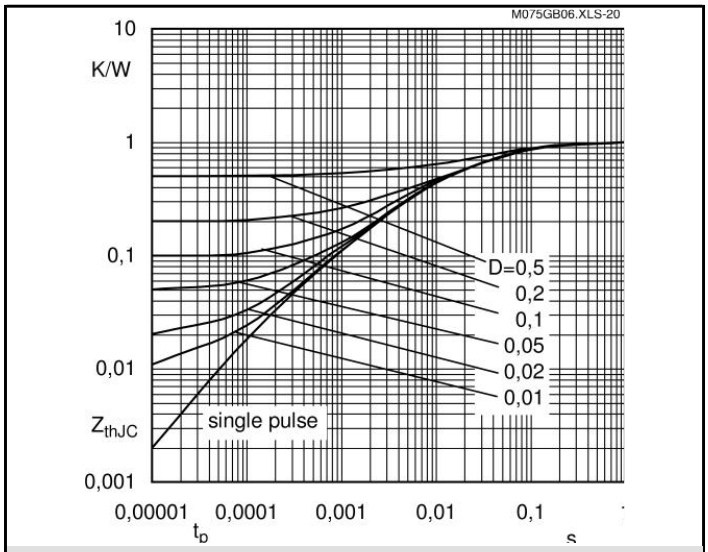


Fig. 10 Transient thermal impedance of FWD

$Z_{thp(j-c)} = f(t_p)$; $D = t_p/t_c = t_p * f$

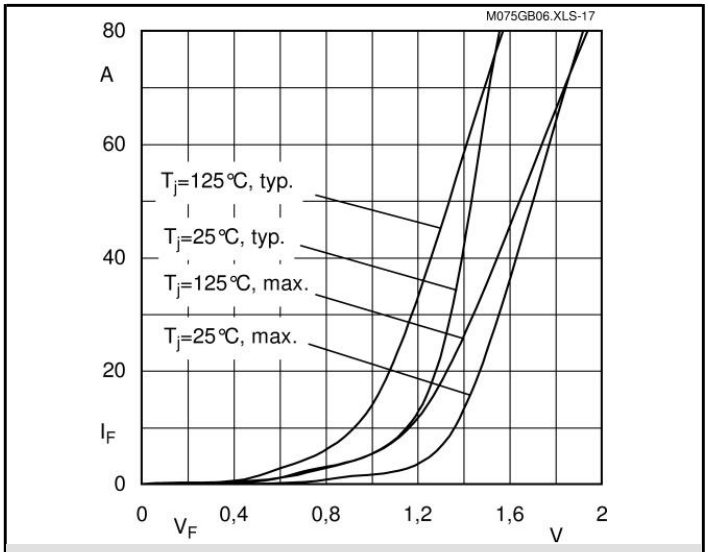


Fig. 11 CAL diode forward characteristic

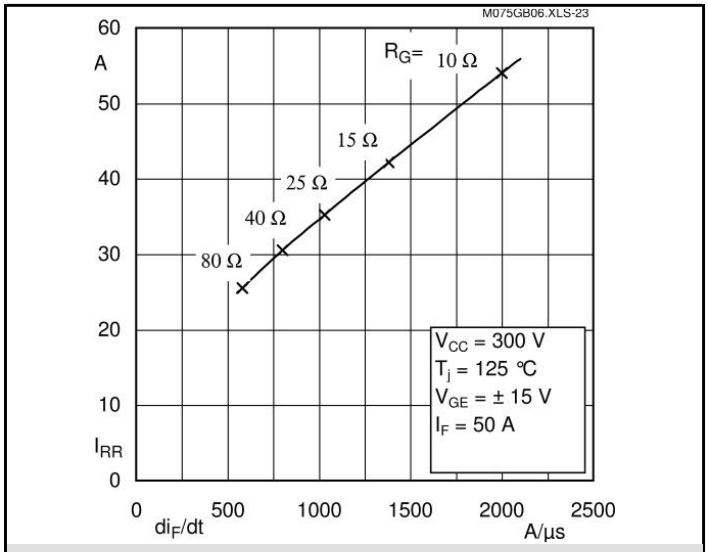


Fig. 12 Typ. CAL diode peak reverse recovery current

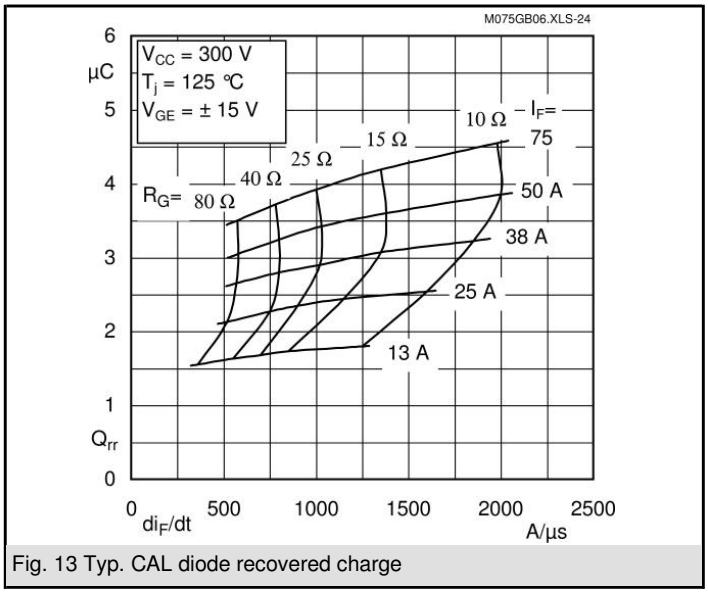
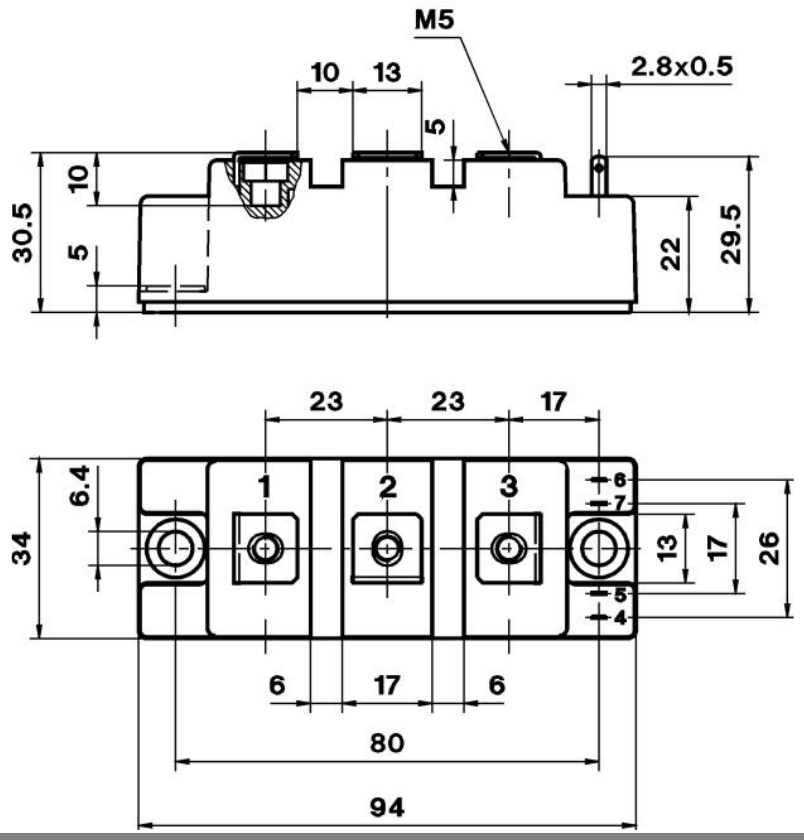


Fig. 13 Typ. CAL diode recovered charge

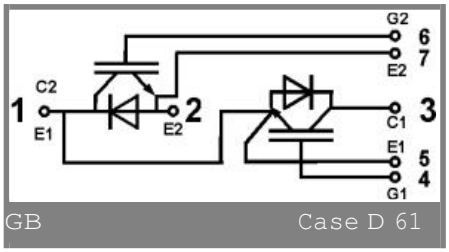
UL Recognized
File no. E 63 532

Dimensions in mm

CASED61



Case D 61



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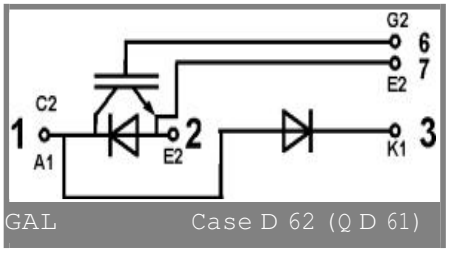
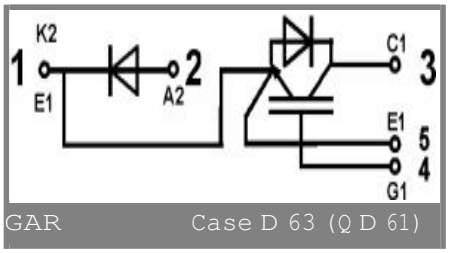


GAL Case D 62 (Q D 61)



GAR Case D 63 (Q D 61)

This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

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