

# A 10kv, 100mA DC Power Supply using Zero Voltage Switching with Full Bridge AC-DC Converter

<sup>1</sup>Jignesh Pandya, <sup>2</sup>J.G.Jamnani

<sup>1</sup>Department of Electrical Engineering, C.U.Shah Polytechnic, Surendranagar, India

<sup>2</sup>Department of Electrical Engineering, Nirma University, Ahmedabad, India

**Abstract** - Nowadays a compact high voltage dc power supply is more in demand so high switching frequency is require for reduce the size of power supply. High switching frequency increase the switching loss which is minimize with the zero voltage switching. The conventional phase-shifted zero voltage switching (ZVS) DC-DC converter is applied to the many power supplies in order to reduce the voltage and current stresses of the main switching devices. The ZVS method needs fairly large leakage inductance in the primary side of the high frequency transformer to get good ZVS characteristics. During the small dead time between conductions of the two bridge legs, the increased magnetizing current resonates with MOSFET output capacitance, resulting in ZVS operation. Switching losses are quite reducing with the ZVS operation in full bridge converter so efficiency of converter is increased. A crockroft-Walton voltage multiplier circuit is connected in secondary side of high frequency transformer which increases the output voltage level and rectified it. This study describes the details of high voltage DC power supply whose output voltage is 10kV, 100mA. Simulation is done by using PSIM 6.0 software. Design equations and Simulation results are presented and discussed. Hardware results very close to the simulation results.

**Index Terms** - DC-DC Converter, DC Power Supply, Voltage Doubler circuit, Zero Voltage Switching.

## I INTRODUCTION

The continuing success of square-wave PWM topology in switching converters can be attributed to its ease of operation. But with the demands for higher power densities, the switching frequencies are approaching 1MHz range. At these frequencies, square-wave converters switching losses become very high leading to excessive heat dissipation. Due to smaller size of the power components, managing the excessive heat becomes a difficult problem and wipes out whatever advantages higher frequency operation provides [1].

Various topologies have been proposed to reduce the switching losses and allow high frequency operation. All these topologies shape the switching waveforms so that at the point of switching, either the current (at turn off) or the voltage (at turn-on) is zero. Various studies have concluded that at high frequencies, zero-voltage turn-on is the most desirable feature for low switching losses. ZVS is preferred over ZCS at high frequency, the reason has with internal capacitance of switch. When the switched is turned-on at zero current but at finite voltage, the charge on the internal capacitance is dissipated in the switch. This loss does not occur if the switch turn- on at zero voltage

The full-bridge phase-shifted converter topology [2-4] provides a much easier solution to the wave shaping problem. Its control features are similar to regular PWM converters and it uses parasitic elements to control the switching transition for zero voltage switching. Also, the absence of resonant peaks limits the stresses on switching components.

In this paper, the main emphasis has been given up on the simulation and design of the high voltage DC power supply with 100 kHz frequency. At first stage, to study the zero voltage switching in full bridge converter and voltage multiplier circuits. Finally Design and simulation is done on High Voltage DC power supply of 10kV, 100mA with 100 kHz frequency. Hardware results are also shown here which is very close to simulation results.

The benefits of lossless Zero Voltage Transition (ZVT) switching techniques are well known throughout the power supply industry. The parasitic circuit elements are used advantageously to facilitate resonant transitions rather than snubbing dissipatively. The resonant tank functions to put zero voltage across the switching devices prior to turn-on, eliminating power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources gain significant improvements in efficiency with this technique [5].

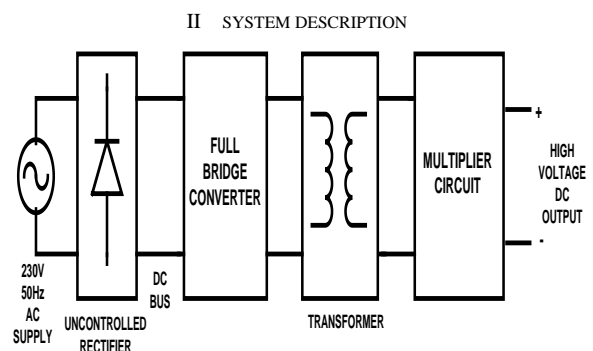


Fig.1 Basic Block diagram of High Voltage DC Power Supply

To achieve zero voltage switching in full bridge converter the leakage inductance of transformer is used and magnetizing current produce the sufficient energy to make the zero voltage switching with the parasitic capacitor of

MOSFET and if the leakage inductance of transformer is less than the required inductance than external inductor is connected in series with the primary winding of the High frequency transformer to achieve the ZVS in full bridge converter. ZVS is achieved so switching loss is reduced and so increases the efficiency of full bridge converter. In above fig.1 the output of full bridge converter is given to high frequency step-up transformer and so increase the secondary voltage of the transformer and this voltage is given to Crockroft-Walton multiplier circuit which increase the output voltage and rectified it so high voltage dc output is available.

So, to reduce the switching losses in high frequency converter, zero voltage switching or zero current switching (ZCS) methods are used. ZVS is more commonly used as compared to ZCS because it has following advantages.

#### Advantages of ZVS over ZCS :

- No power loss due to discharging  $C_{oss}$  in ZVS.
- No higher peak currents in zero voltage switching.
- High efficiency with high voltage input at high frequency.
- Can incorporate parasitic circuit component L and C.
- Reduce gate drive requirements (no miller effect)
- Short circuit tolerant
- ZVS is preferred over ZCS at high frequency, the reason has to do with internal capacitance of switch. When the switched is turned-on a zero current but at finite voltage, the charge on the internal capacitance is dissipated in the switch. This loss does not occur if the switch turn- on at zero voltage.

### III RESONANT CIRCUIT DESIGN

#### Compute $L_R$ and $C_R$ :

There are several ways to calculate the value of the resonant inductor ( $L_R$ =External series inductance + Leakage inductance) and minimum primary current required for any application. Each of these is based upon the following fundamental relationships. The resonant tank period must be at least four times higher than the transition time to fully resonate within the maximum transition time  $t_{MAX}$  at light load.

$$T_{RES} = 4t_{MAX}$$

$$f_{RES} = 1/(4t_{MAX})$$

$$\omega r = 2\pi f_{RES} = 2\pi/4t_{MAX} = \pi/2t_{MAX}$$

The resonant radian frequency  $\omega r$  is related to the resonant components by the equation  $\omega r = 1 / (L_R C_R)^{1/2}$

So,

Resonant Inductor value  $L_R = 1/(\omega r^2 C_R)$

The specified MOSFET switch output capacitance  $C_{oss}$  will be multiplied by a 4/3 factor per the MOSFET manufactures Application Notes to approximate the correct average capacitance value with a varying drain voltage. During each transition, two switch capacitances are driven

in parallel, doubling the total capacitance to  $(8/3)*C_{oss}$ . Transformer capacitance  $C_{XFMR}$  must also be added as it is not negligible in many high frequency applications, especially at lower power levels where smaller switches are incorporated.

Resonant capacitance  $C_R = (8/3)*C_{oss} + C_{XFMR}$

So, resonant inductor is given by

$$L_R = 1 / [(\pi/2t_{MAX})^2 * ((8/3)*C_{oss} + C_{XFMR})]$$

#### Stored Energy Requirements :

The energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. So,

$$\frac{1}{2} * L_R I_{PRI(MIN)}^2 > \frac{1}{2} * C_R * V_{IN(MAX)}^2$$

Since  $C_R$  and  $V_{IN}$  are known, so  $L_R$  can be calculated

#### Minimum (critical) Primary Current :

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation. Operating below this critical current level will result in lossy transitions.

$$I_{PRI(MIN)} = [(C_R * V_{IN}^2) / L_R]^{1/2}$$

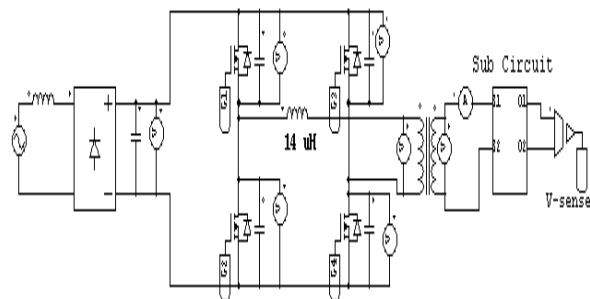
This value can be supported by calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower than  $I_{P(MIN)}$ , it can be used to confirm the calculations.

$$I_{R(AVG)} = C_R V_{IN} / T_{MAX}$$

### IV SIMULATION OF THE SYSTEM

Simulation is carried out by Using PSIM 6.0 Software

Fig.2 shows the Close loop simulation diagram of High Voltage DC Power Supply in which an inductor is connected in series with the primary winding of high frequency transformer to achieve the zero voltage switching and Fig.3 shows sub circuit which is Eight Stage of Crockroft Walton Voltage Multiplier Circuit is connected in the secondary side of the transformer which gives 10 kV output voltage.



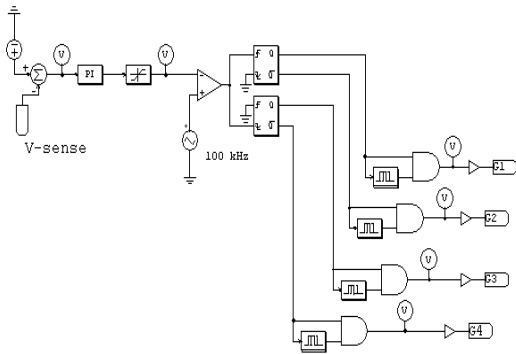


Fig.2 Close loop simulation diagram of High Voltage DC Power Supply

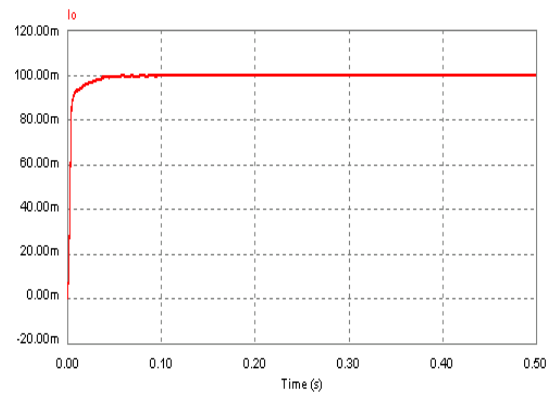


Fig.6 Output Current of proposed High Voltage DC Power Supply

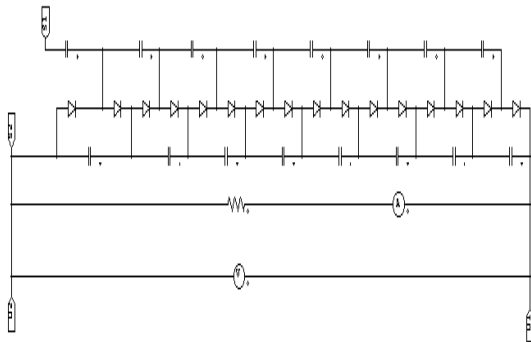


Fig.3 Eight Stage Crookft - Walton Voltage Multiplier Circuit

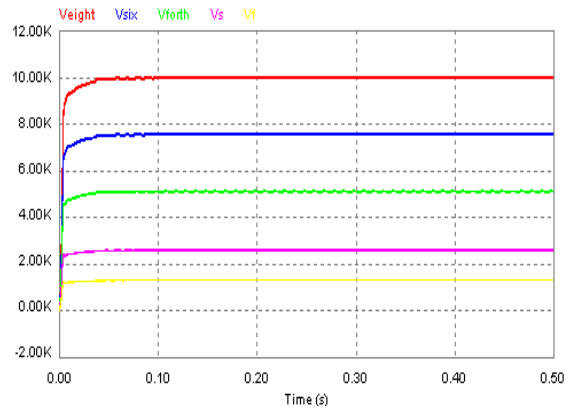


Fig.7 Each stage Output Voltage of Crookft Walton multiplier stage.

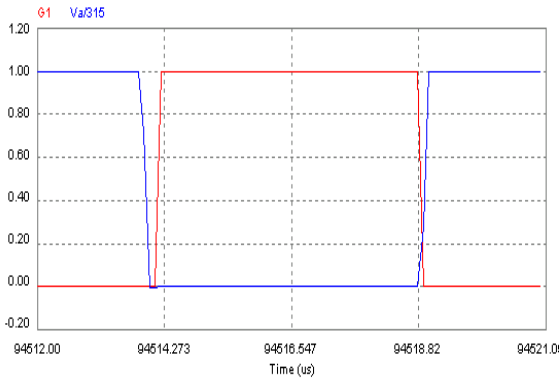


Fig.4 Zero Voltage across the switch before the gate pulse is ON

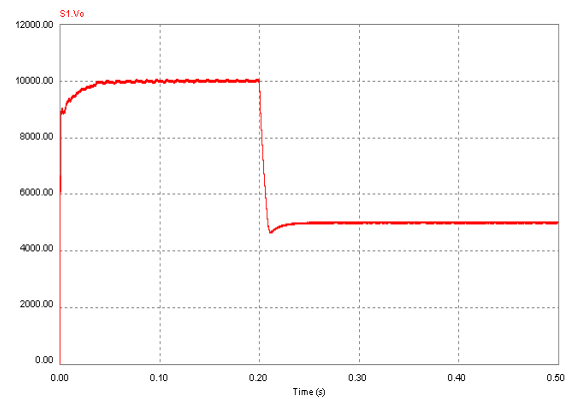


Fig.8 Output Voltage according to set reference Voltage

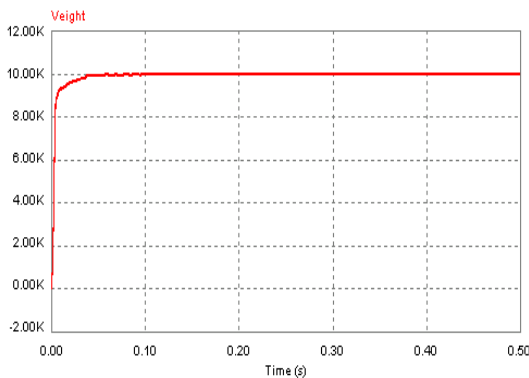


Fig.5 Output Voltage of proposed High Voltage DC Power Supply

Fig.4 shows the zero voltage switching is achieved before the gate pulse is ON. Here gate pulse is ON when voltage across the switch is zero so switching loss is reduced and so efficiency of the power supply is increase. Fig.5 shows the output voltage of power supply 10kV achieved and Fig.6 shows the output current 100mA is achieved of high voltage dc power supply with close loop operation. Fig.7 shows the each stage Output Voltage of Crookft Walton multiplier circuit which is 1.25kV for first stage, 2.5kV for second stage, 5kV for fourth stage, 7.5kV for sixth stage, 10kV for eighth stage. Fig.8 shows output voltage according to set reference voltage when reference voltage is equal to 1 output voltage is 10kV and reference voltage is 0.5 output voltage is 5 kV.

V HARDWARE RESULT

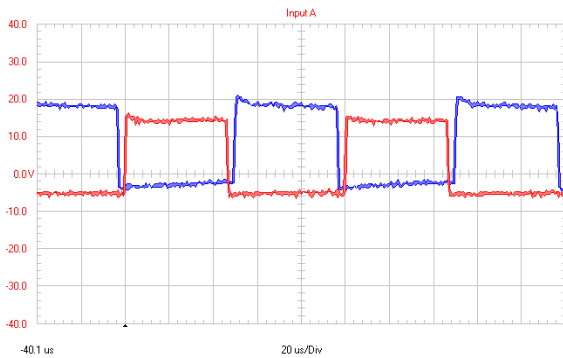


Fig.9 Gate Pulse for Switch-1 & Switch-2

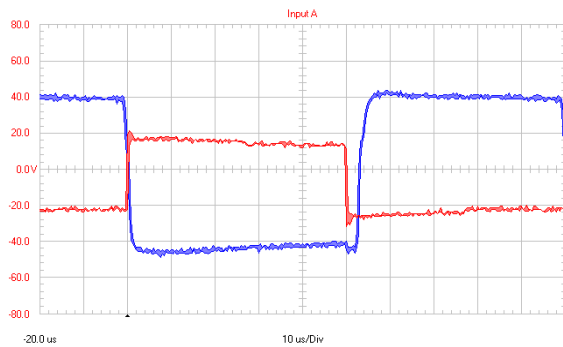


Fig.10 Zero Voltage across the switch before the gate pulse is ON

Fig.9 shows the gate pulse of switch 1 and switch 2 of same leg of full bridge converter and Fig.10 shows zero voltage switching is achieved across the switch before the gate pulse is ON.

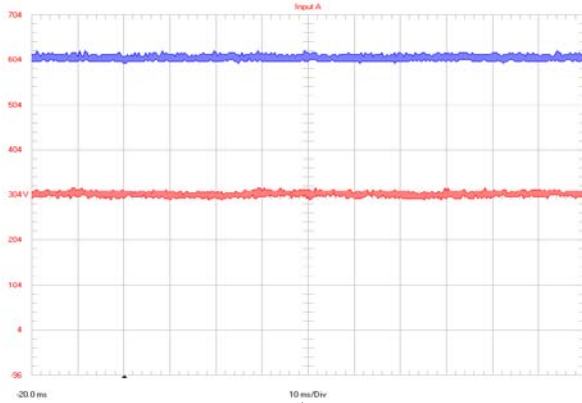


Fig.11 Output Voltage of 1<sup>st</sup> Stage 300 V & Second stage 600 V of C-W multiplier

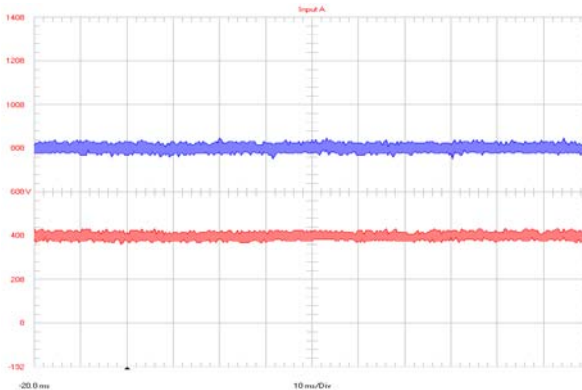


Fig.12 Output Voltage of 1<sup>st</sup> Stage 400 V & Second Stage 800V of C-W multiplier

Fig.11 shows output voltage of first stage which is 300V across first stage of multiplier and total eight stages so 2.4kV generate voltage across the C-W Multiplier.

Same way Fig.12 shows output voltage of first stage which is 400V across first stage of multiplier and total eight stages so 3.2kV generate voltage across the C-W Multiplier.

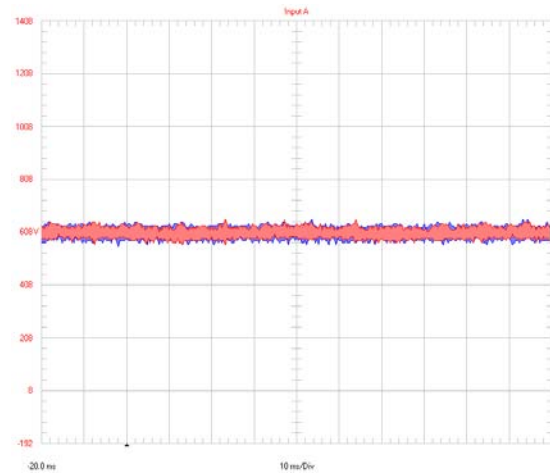


Fig.13 Output Voltage of 1<sup>st</sup> Stage 600 V & Second Stage 600V of C-W multiplier

Fig.13 shows output voltage of first stage which is 613V across first stage of multiplier same way across the second stage of multiplier 613V as shown in figure and total eight stage so 5kV generate voltage across the C-W Multiplier and same two secondary of the crockroft Walton multiplier stage so both are connected in series so total 10kV voltage generated.

The following parameters are taken for the Design and Simulation as shown in Table I:

Table I  
Design Parameter taken for Simulation

Supply Voltage	230 AC
MOSFET	IRFPE50 N
MOSFET output Capacitance	800 pF
External Series Inductor	14 uH
Resonant Inductor	18 uH
Resonant Capacance	2800 pF
Capacitor of Multiplier circuit	500 nF
Crookroft Walton Multiplier Circuit	8 Stage
Transformer ratio	1: 2
Switching Frequency	100 kHz
Output Resistance	100 kΩ
Delay in Gate pulse Generating Circuit	0.3 sec

VI CONCLUSION

The proposed topology shows that the size of high

voltage dc power supply can be reduced by increasing the switching frequency. However the switching losses will be more. But using resonant technique, switching losses are reduced and therefore the efficiency is increased.

To achieve Zero Voltage Switching with phase shifted PWM, the leakage inductance of transformer should be taken high and give a sufficient dead band between the two lag switches but at the same time duty cycle is decrease which is the demerit of ZVS with phase shifted PWM full bridge converter.

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