DESIGN AND FABRICATION OF ELECTRONIC POWER CONDITIONER FOR POWER AMPLIFIER

Major Project Report

Submitted in Partial Fulfillment of the Requirements for the degree of

MASTER OF TECHNOLOGY

IN

ELECTRICAL ENGINEERING

(Power Apparatus & Systems)

By

Monika R Sharma
(05MEE016)

Department of Electrical Engineering
INSTITUTE OF TECHNOLOGY
NIRMA UNIVERSITY OF SCIENCE AND TECHNOLOGY,
AHMEDABAD 382 481
MAY 2007

CERTIFICATE

This is to certify that the Major Project Report entitled **"Design and Fabrication of Electronic Power Conditioner for Power Amplifier"** submitted by **Ms. Monika R Sharma (05MEE016)** towards the partial fulfillment of the requirements for the award of degree in Master of Technology (Electrical Engineering) in the field of Power Apparatus & Systems of Nirma University of Science and Technology is the record of work carried out by him/her under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

Date:

Industry – Guide

Mr. N.J. Shelat
Head, ETAD
SAC (ISRO), Ahmedabad

Institute – Guide

Mr. Amit N.Patel
Lecturer, (Electrical Dept),
Institute of Technology, Nirma University

Head of Department

Department of Electrical Engineering
Institute of Technology
Nirma University
Ahmedabad

Director

Institute of Technology
Nirma University
Ahmedabad

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MONIKA R SHARMA

ABSTRACT

This report describes the detailed design of High Efficiency DC-DC converter with 75W output power required for Power Amplifier. The converter consists current mode control boost preregulator, half bridge converter and control circuit design of this converter is carried out at high switching frequency. This high switching frequency is necessary to reduce size and weight of DC-DC converter. However this yields high switching losses consequently low efficiency in hard switching. ZVS quasi-resonant converters which are designed to reduce switching losses, but the reduction of switching losses in these converters results in conduction losses by increase in voltage and current stress of switches. So Zero voltage transition technique in Boost preregulator is opted here, which gives minimum semiconductor stress and low losses. Zero voltage transition boost preregulator is connected at the previous stage in order to increase the efficiency of the power supply and reduce un-acceptable switching losses in the power devices. Output of this preregulator is given to the Half Bridge converter that follows diode rectification and filtering. This report describes all design steps, detailed derivations of design equations, observed waveforms and efficiency results for both Boost preregulator and Half Bridge Converter. This High efficiency Converter can be used for firing Gallium Arsenide FETs of Solid state power amplifier used in space applications.

LIST OF FIGURES AND TABLES

NOMENCLATURE

f_S	- Switching frequency
D	- Duty cycle
V_{IN}	- Input DC voltage
V_O	- Output DC voltage
T_{ON}	- On time
T_{OFF}	- Off time
T_S	- Switching period
ΔV_O	- Output Ripple voltage
ΔI_L	- Inductor Ripple current
V_{GS}	- MOSFET gate to source voltage
R_{DS}	- MOSFET on state drain to source resistance
Ts	- Switching time
D’	- 1-D
I_L	- Boost Inductor current
V_L	- Boost Inductor voltage
V_D	- forward diode voltage
ESR	- Effective series resistance of capacitor
t_r	- Rising time of MOSFET
t_f	- Fall time of MOSFET
V_{DSS}	- Maximum drain to source voltage
I_D	- Drain current
T_A	- Ambient temperature
Tj	- junction temperature
$R\theta J_A$	- Thermal Resistance
P_D	- power dissipated in MOSFET
A_L	- mH@1000turns
OD	- Output Diameter
ID	- Inner Diameter
L_m	- Magnetic path length
Ct	- Oscillator Capacitor

Rt	- Oscillator Resistance
μ	- Permeability
J	- Current Density
Awg	- Wire Gauge
Zp	- Primary Impedance of current transformer
Zs	- Secondary Impedance of current transformer
Np	- Primary turns
Ns	- Secondary turns
Wa(s)	- Secondary winding area
Wa(p)	- Primary winding area
Is	- Secondary current
Ip	- Primary current
K	- Space factor
f_C	- Crossover frequency

CONTENTS

1.1 Electronic Power Conditioner:

All electronic circuits utilize the DC power for its operation. Requirements of DC voltages depend upon type of active devices, family of Integrated Circuits and the other components used in the equipments. All electronic equipments, whether designed for satellite, home appliance or industrial applications, invariably require DC supply with more than one voltage level and in both positive and negative polarity. Latest digital devices like microprocessors, FPGA, ASICs Digital signal processing ICs typically need +1.8, +2.5, +3.3 or +5.0 volts. TTL, CMOS and many Analog ICs are frequently operated with +5.0 Volts, while the ECL devices are operated at -5 volts. Gallium Arsenide FETs used in the microwave Amplifiers are biased by using either +8.0, -5.0 volts, or +3.5 and –3.5 volts. +12, -12, +15, -15 and +24 volts supply are also often used in the electronic circuits with transistors, relay in industrial control etc. Thus, power supply with vast variety of DC voltage levels and with current requirement commensurate with the complexity of the functions to be performed is required.

The electrical energy or the basic source of supply is available in the form of sinusoidal AC supply for household and industrial applications. An array of the solar cell with battery backup is used to generate and support the power requirements of all equipments in satellites

Input energy for all ground equipments is not in the form of DC voltage. The input power in the satellite is available with typical nominal voltage of 43, 28, 70 or 100 volts and this voltage decreases considerably, during the eclipse. As a result the all the equipments on satellite platform also receives the power with variable DC voltages over operating life periods.

The electronic circuit that performs the function of converting the DC voltage available from the battery or the solar array system into the other DC voltages and also conditions the input power to the exact need of load is known as “ELECTRONICS POWER CONDITIONER”, (EPC). The EPC takes care of any change in input power, environment and also some special requirements for the safety and protection of the electronic systems. EPC is an interface between the equipment and the external source of

energy, which is designed to absorb and mitigate all the perturbation in power source, environment and even in the equipment. All our household electronic appliances and industrial electronic equipments have either a DC power supply interfacing with the utility, or a power converter between the battery and the electronics. Customarily the same is known as SMPS (Switch mode power supply), DC-DC Converter or simply DC power supply. The word EPC is more conventionally used for DC power supply designed for high power amplifier either in the earth station or in the satellite. But as far as functionalities are concerned all DC power supplies are required to cater for the similar need, "power/voltage conversion and conditioning as per the requirements of the electronics for unperturbed operation". Satellite payload makes use of large quantity of power amplifiers, either as 'Solid State Power Amplifier' (SSPA) or 'Traveling Wave Tube Amplifier' (TWTA). Power amplifiers utilize majority of the DC power and the platform area allocated to the payload. Therefore the design and performance of the EPC associated with either SSPA or TWTA is most important from the viewpoint of power consumption, mass and size.

Fundamentally EPC is an interface between source and load.

1.2 Design Objective:

The aim of this project is to Design, Develop and Realize High efficiency DC/DC converter that includes Zero Voltage Transition Boost preregulator and Half Bridge Converter for power amplifier operated at 26-44V. Various soft switching techniques and control techniques have been studied and relative merits and demerits of each have been analyzed. Here Zero voltage transition along with current mode control is used in the Boost preregulator followed by Half Bridge Converter.

1.3 Design Specifications and Block Diagram:

1.3.1 Design Specifications:

(i) Input Voltage Range: 26 to 44 V

(ii) Topology: Boost preregulator + Half bridge converter

(iii) Switching Frequency: 100 KHz

(iv) Outputs: Boost preregulator: 40V/5A DC
Half Bridge converter: 28V/3A DC

(v) Line + Load + Temperature regulation: 1%

(vi) PARD (Periodic and Random deviation): 500 mV

(vii) Efficiency: 86%

(viii) Output Power: 84W

(ix) Onboard, tentative for power amplifier

1.3.2 Block Diagram:

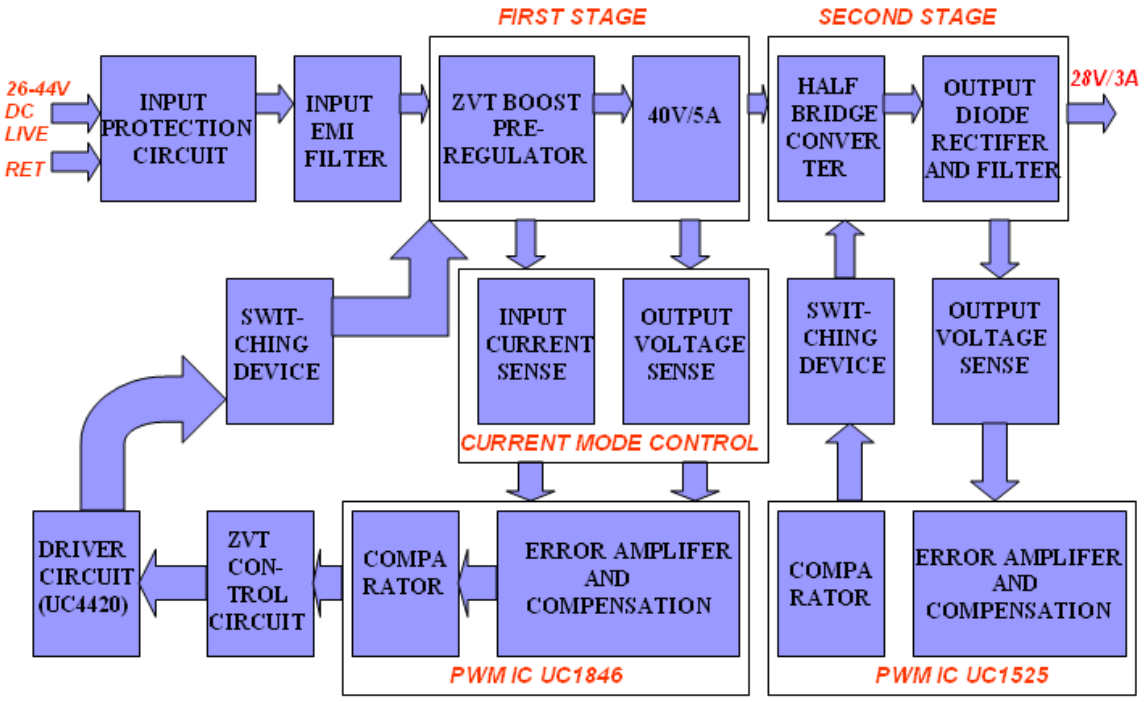


Figure 1.3.2 Block Diagram of project

1.4 Zero voltage Switching fundamentals:

1.4.1 Power Supply losses:

The typical losses in switching power supplies can be divided in two classes: conduction losses and switching losses. The most common switching element used in modern switching power supplies is the power MOSFET. The device when enhanced for conduction has a finite channel resistance named $R_{DS\ (ON).}$ When current passes through this device conduction losses results that are proportional to:

$$P_c = I^2_{DS(RMS)} \times R_{DS(ON)}$$

In addition to the conduction losses, due to the switching action of the device in the presence of high currents and high voltages, there are also switching losses. These losses can be subdivided in turn-on, turn-off and capacitive discharge losses.

The energy in turn-off instance can be found by integrating the product of the voltage and current waveforms over the complete switching interval i.e.

$$W_{tOFF} = \int_{0}^{ts} V_t \times i_t dt$$

Where t_s is the transition period.

Assuming linear waveforms and symmetry, the above integral can be simplified to the following

$$W_{tOFF} = \frac{I_{PEAK} \times V_{PEAK} \times t_s}{2}$$

The total power lost therefore can be found by multiplying the above with the repetition rate, which is switching frequency hence

$$P_{OFF} = \frac{I_{PEAK} \times V_{PEAK} \times t_s \times f}{2}$$

The turn-on switching losses can be similarly found by integrating the current and voltage waveforms over the switching interval:

$$P_{ON} = \frac{I_{PEAK} \times V_{PEAK} \times t_s \times f}{2}$$

To reduce the switching losses several methods are used.

1.4.2 Switching losses control methods:

In order to improve efficiency of the power converter it is required reducing switching losses. The dynamic losses of the switching semi-conductors at higher operating frequencies and elevated input voltages are excessive. The switching losses can be reduced by using Snubbers, quasi or fully resonant techniques or soft – switching (Zero Voltage Transitions) circuits.

The sinusoidal wave shape of resonant – mode topologies could alleviate the issue of undesirable power losses at the switching transitions by allowing switching to take place while either the voltage or current was zero and hence it becomes possible to develop successful power systems with switching frequencies into the mega-hertz range. While these frequencies did allow gains to be made in the power density, new problems arose in maintaining efficient operation as:

(a) Since a sinusoidal wave shape cannot contain the same energy as a square wave of the same amplitude, peak currents were higher than equivalent PWM designs. In converting from square – wave to resonant designs, the savings in reduced switching losses was offset by the I^2R losses caused by the higher peak currents of the sinusoidal wave shape.
(b) An additional troublesome characteristic is the fact that control is accomplished by varying the switching frequency, a situation that complicates the design of the input and output filters and causes the system designer concern over noise immunity.

1.4.3 Soft-switching (ZVT) circuits:

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on time with resonant switching transitions. The parasitic circuit elements are used advantageously to facilitate resonant transitions rather than snubbing dissipatively. The resonant tank functions to put zero voltage across the switching devices prior to turn – on, eliminating power loss due to the simultaneous overlap of the switch current and voltage at each transition.

1.5 Boost preregulator:

Boost converter with zero voltage transition has been chosen for regulating the variable raw input bus with efficiency in excess of 96 % as the first stage of the project. The purpose behind connecting this converter is to increase overall efficiency of the converter and also the Half Bridge Converter that is followed by this Boost preregulator can be designed at higher output power in future if desired.

The Boost topology has been preferred over the Buck converter due to the following advantages:
(a) Due to non pulsating input current, smaller size of input filter is sufficient for achieving the desired attenuation of input current ripple and hence the EMI Compliance.
(b) It is required to operate the boost pre regulator with at least 40 volts output (higher than maximum bus input) where as output of the buck regulator needs to be 20 volts (less than minimum bus input). Since the output of the pre regulator is applied as an input to the high voltage converter, current flowing in to the high voltage transformer primary is smaller by a factor of 2.5 times for boost pre regulator. This results in to considerable reduction of conduction losses in the switching MOSFETs of high voltage transformer.

(c) The use of comparatively thinner wire gauge helps in achieving better precision, consistency and over coming practical winding problems associated with high voltage transformer winding.

(d) The gate drive signal for the buck power switch requires floating connection. While the MOSFET in the Boost the PWM pulses can directly drive topology available from the MOSFET Driver ICs.

(e) Implementation of the soft switching for mitigating the switching losses is comparatively less complicated for Boost topology.

Considering all above factors, boost topology with 40 volts regulated output has been designed as pre regulator.

1.6 Half Bridge Converter:

The half bridge topology is more frequently used in power converter circuits for ground application. For the operation of this topology, it required to split the input DC source in to two equal half. Detail of this converter is explained in CHAPTER 3.

1.7 Control Techniques:

1.7.1 Voltage mode control:

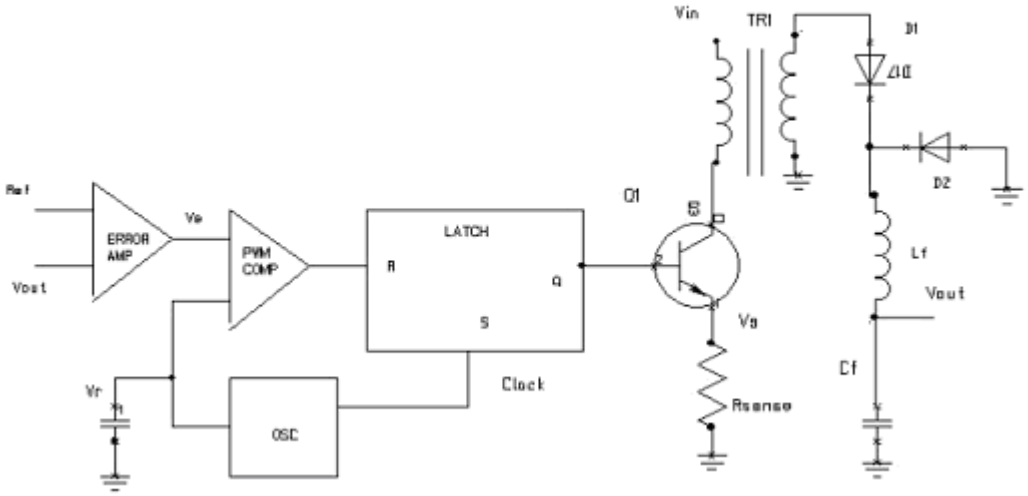


Figure 1.7.1 Voltage mode control

In power supply varying the duty cycle of power switches controls the output voltage. Traditionally duty cycle control was done by comparing the amplified difference of the output voltage feedback signal and a fixed stable reference to a saw tooth

waveform derived from an oscillator. This constitutes the basic voltage mode control and current mode control scheme. The voltage mode control has the following disadvantages:

(a) Any change in line and load must first be sensed as its impact on output change and then corrected by the feedback loop. This usually means slow response.

(b) The output filter adds two poles to the control loop requiring either a dominant pole low frequency roll-off at the error amplifier or complex two pole two zero network in the compensation.

Both these demerits pose significant problem in designing the control loop. Current mode control overcomes both the above limitations.

1.7.2 Current mode control:

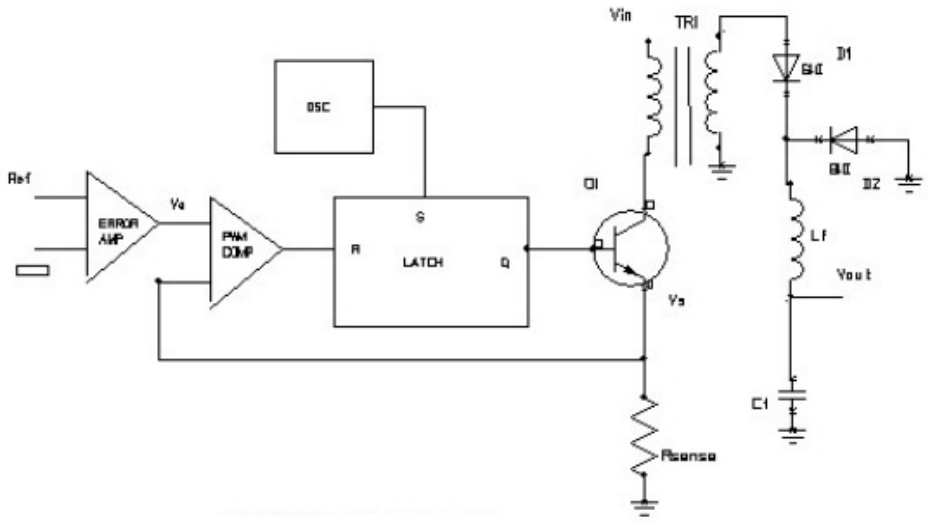


Figure 1.7.2 Current mode control

The current mode control method uses two control loops – an inner current control loop and an outer loop for voltage mode control. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when weighted equivalent of the output inductor current reaches a threshold established by the error signal. In this way error signal actually controls the inductor current. Thus the outer voltage control loop defines the level at which inner loop regulates peak current flowing through the switch and the inductor. Several performance advantages result from the use of current control:

(a) An input voltage feed forward characteristics is achieved; i.e., the control circuit instantaneously correct for input voltage variations without using any error amplifier's dynamic range. Therefore line regulation is excellent and error amplifier can be dedicated to correcting for load variations.

(b) Since the error amplifier is now used to command an output current rather than the voltage, the effect of the pole introduce by the output inductor is eliminated and the filter now offers only a single pole roll off in open loop converter's response. This allows the simpler compensation and wider gains bandwidth as compared to voltage mode control.

(c) Equal current sharing in parallel power stages is possible, if switching of both is derived from the same control signal.

(d) Pulse-by-pulse current limiting is inherent by this control scheme.

However this control scheme also comes with its own set of problems, which must be solved in the design process as:

(a) The control loop becomes unstable if the duty cycle exceeds 50% unless slope compensation is added.

(b) The turn on current spike caused by the reverse diode recovery of the output free wheeling diode may cause premature shutdown. The circuit can also become susceptible to noise generated by power switches.

1.8 Current Sensing Techniques:

In current mode control, theoretically it is required to sense and use the slope of the current flowing in the output inductor. However since the control circuit is referenced to the primary return and the output inductor is floating on the output line, it is difficult to sense and add the slope of the output current. The current flowing in the power switch at the input side of the circuit is closely following the output current, therefore though not accurate but easier to sense the current in the primary as representative of the output inductor current. Depending upon the magnitude of the current sensed, several current sense methods can be implemented. Direct Resistive Sensing is the simplest amongst all, however using a current sense resistor in the direct path of leads to the undesirable loss and efficiency degradation. It is difficult to implement very small value sense resistor and the power dissipation in a practical sense resistor could be too large.

A current sense transformer is a practical solution for all problems associated with sensing like, sensing the current with lowest possible insertion impedance, modifying the amplitude of the sensed current as per the need of the control IC and transferring the sensed voltage to the circuit with the difference reference potential. The current transformer circuit with proper reset mechanism and required current transfer ratio is designed and implemented.

1.9 Input Filter Design:

The input filter on a switching power supply has two primary functions. One is to prevent electromagnetic interference generated by the switching source from reaching the power line and affecting other equipment. The second purpose of the input filter is to prevent high frequency voltage on the power line from passing through the output of the power supply. An Undamped L-C filter is the simplest approach. Its greatest drawback is its poor damping factor that can influence the transfer function of the feedback control loop and can cause oscillations at the output of the power supply. A parallel damped filter consist of a resistor Rd in series with a capacitor Cd , all connected in parallel with the filter's capacitor Cf. The purpose of resistor Rd is to reduce the output peak impedance of the filter at the cutoff frequency. The capacitor Cd Blocks the dc component of the input voltage, and avoids the power dissipation on Rd. The capacitor Cd should have lower impedance than Rd at the resonant frequency and be a bigger value than the filter capacitor, to not effect the cutoff point of the main R-L filter.

The damping factor for this filter can be written as:

$$\zeta = \frac{(n+1)}{n} \times \frac{L}{2 \times R_d \times \sqrt{L \times C}}$$

The peaking is minimized with an optimum damping factor equal to:

$$\zeta_{opt} = \sqrt{\frac{(2+n) \times (4+3n)}{2 \times n \times n \times (4+n)}}$$

The optimum damping resistance value Rd at n=4 can be written as:

$$R_{d(opt)} = \sqrt{\frac{L}{C}}$$

$$C_d = 4 \times C$$

1.10 Literature survey:

This project work is mainly focused on the design of high efficiency DC-DC converter that includes boost pre regulator and half bridge converter. Zero voltage transition circuit is incorporated in boost preregulator. To understand the basics of the Zero Voltage Transition, various IEEE papers are refereed which are there in references.

- This DC-DC converter is designed at high frequency so the switching losses increases. Hence in order to increase the efficiency of the converter, ZVT circuit is connected in conventional Boost Converter. [1], [2], [3] and [4].
- To understand various soft switching techniques for PWM Converters, this paper is referred. [5]
- Zero voltage switching fundamental in DC-DC Converter is studied in this paper. [6]
- Various latest technologies for resonant techniques in PWM DC-DC converters are given in this paper. [7]
- In order to mitigate ripple from input supply voltage, filter is connected in input side of power supply. This paper explains the design of the input filter. [8]
- By connecting input filter to the switching power supply, various oscillations take place in switching power supply. This paper describes design technique for preventing input filter oscillations in power supply. [9]
- For designing compensation of the error amplifier of current mode or voltage mode ICs, it is required to know the stability criteria. This paper explains how to specify phase and gain of control loop. [10]
- Stability criteria states that at loop crossover frequency gain should be zero. This paper explains loop crossover frequency in detail. [11]
- Inductor is designed for Boost Converter and also for output filter. Its design is separate for both the applications that are explained in this paper. [12]
- Core selection for Transformer and Inductor is explained in this paper. [13]

2.1 Introduction of Boost preregulator's power stage:

The boost is a popular non-isolated power stage topology, sometimes called step up power stage. It is chosen because the required output voltage is always higher than the input voltage, is the same polarity and is also not isolated from input voltage. The input current for a boost power stage is continuous or non-pulsating because the input current is the same as the inductor current. The output current for a boost power stage is discontinuous or pulsating because the output diode conducts only during a portion of the switching cycle. The output capacitor supplies the entire load current for the rest of the switching cycle.

Figure 2.1.1 shows a simplified schematic of boost power stage with a drive circuit block included. Power switch Q1 is an n-channel MOSFET. The output diode is CR1. Inductor L and capacitor C make up the effective output filter. The capacitor equivalent series resistance (ESR), RC, and the inductor dc resistance, RL, are included in the analysis. Resistor R represents the load seen by the power supply output.

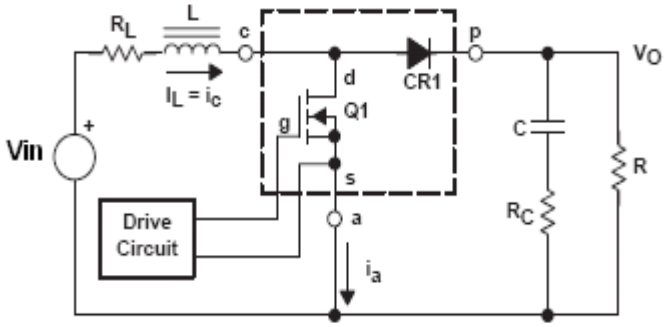


Figure 2.1.1 Boost Power Stage Schematic

During normal operation of the boost power stage, Q1 is repeatedly switched on and off with the on and off times governed by the control circuit. This switching action creates a train of pulses at the junction of Q1, CR1, and L. Although inductor L is connected to output capacitor C only when CR1 conducts, an effective LC output filter is formed. It filters the train of pulses to produce a dc output voltage, Vo.

A power stage can operate in continuous or discontinuous inductor current mode. In continuous inductor current mode, current flows continuously in the inductor during the entire switching cycle in steady-state operation. In discontinuous inductor current mode, inductor current is zero for a portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. It is desirable for a power stage to stay in only one mode over its expected operating conditions because the power stage frequency response changes significantly between the two modes of operation.

Here boost converter operating in continuous mode is analyzed and designed.
For this analysis, an n-channel power MOSFET is used, and a positive voltage, $V_{GS\ (ON)}$, is applied from the gate to the source terminals of Q1 by the drive circuit to turn on the MOSFET. The advantages of using an n-channel MOSFET are its lower $R_{DS\ (ON)}$ (compared to a p-channel MOSFET), and the ease of driving it in a boost power stage configuration. Transistor Q_1 and diode CR_1 are drawn inside a dashed-line box with terminals labeled a, p, and c. This is shown in figure 2.1.1.

The following is a description of steady-state operation in continuous conduction mode. Steady state implies that the input voltage, output voltage, output load current, and duty-cycle are fixed and not varying. Result of this analysis shows how the output voltage depends on duty cycle and input voltages or how, conversely, the duty cycle can be calculated based on input and output voltages.

In continuous conduction mode, the boost power stage assumes two states per switching cycle. In the on state, Q1 is on and CR1 is off. In the off state, Q1 is off and CR1 is on. A simple linear circuit can represent each of the two states where the switches in the circuit are replaced by their equivalent circuit during each state. Figure 2.1.2 shows the linear circuit diagram for each of the two states.

The duration of the on state is $D \times T_S = T_{ON}$, where D is the duty cycle set by the control circuit, expressed as a ratio of the switch on time to the time of one complete switching cycle, Ts. The duration of the off state is T_{OFF}. Since there are only two states per switching cycle for continuous conduction mode, T_{OFF} is equal to $(1–D) \times T_S$. The quantity (1–D) is sometimes called D'. These times are shown along with the waveforms in Figure 2.1.3.

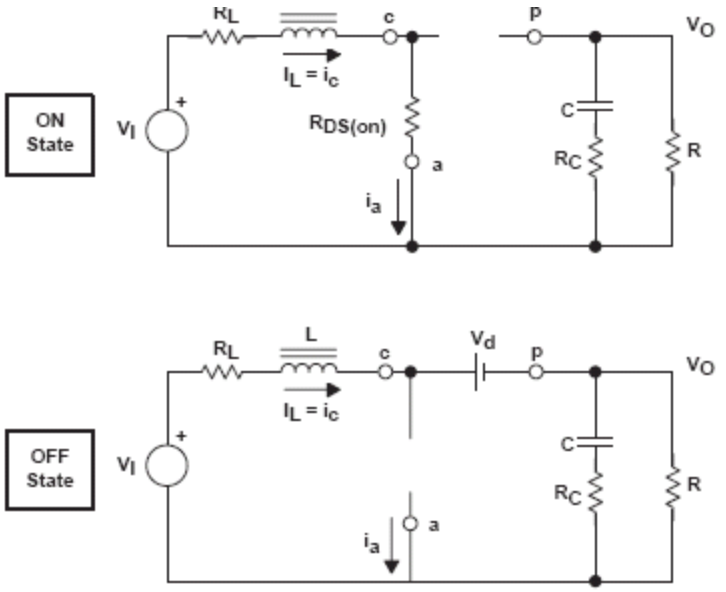


Figure 2.1.2 Boost Power Stage States

Referring to Figures 2.1.2 and 2.1.3, during the on state, Q1, which presents a low drain-to-source resistance, R_{DS} (on), has a small voltage drop of V_{DS}. There is also a small voltage drop across the dc resistance of the inductor equal to $I \times R_L$. Thus the input voltage, V_I, minus losses, ($V_{DS}+I_L \times R_L$), is applied across inductor L. Diode CR1 is off during this time because it is reverse biased. The voltage applied to the right side of L is the MOSFET on voltage, V_{DS}. The inductor current, I_L, flows from the input source, V_I, through Q1 to ground. During the on state, the voltage across the inductor is constant and equal to $V_I - (V_{DS} + I_L \times R_L)$. Adopting the polarity convention for I_L shown in Figure 2.1.2, the inductor current increases as a result of the applied voltage. Also, since the applied voltage is essentially constant, the inductor current increases linearly.

The inductor-current increase can be calculated by using a version of the familiar relationship:

$$V_L = L \times \frac{di_L}{dt} \Rightarrow \Delta I_L = \frac{V_L}{L} \times \Delta T$$

The inductor current increase during the on state is given by:

$$\Delta I_L (+) = \frac{V_I - (V_{DS} + I_L \times R_L)}{L} \times T_{ON}$$

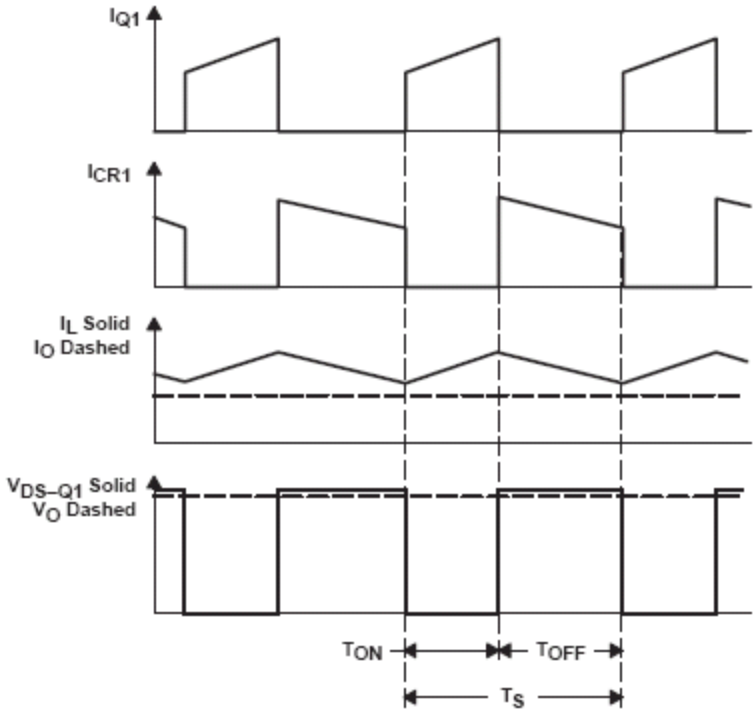


Figure 2.1.3 Continuous Mode Boost Power Stage Waveforms

The quantity ΔI_L (+) is the inductor ripple current. During this period, the entire output load current is supplied by output capacitor C.

When Q1 is off, it presents high drain-to-source impedance. Therefore, since the current flowing in inductor L cannot change instantaneously, the current shifts from Q1 to CR1. Due to the decreasing inductor current, the voltage across the inductor reverses polarity until rectifier CR1 becomes forward biased and turns on. The voltage applied to the left side of L remains the same as before at $V_I - I_L \times R_L$. The voltage applied to the right side of L is now the output voltage, V_O, plus the diode forward voltage, V_D. The inductor current, IL, now flows from the input source, V_I, through CR1 to the output capacitor and load resistor combination. During the off state, the voltage across the inductor is constant and equal to $(V_O + V_D + I_L \times R_L) - V_I$. Maintaining the same polarity convention, this applied voltage is negative (or opposite in polarity from the applied voltage during the on time). Hence, the inductor current decreases during the off time. Also, since the applied voltage is essentially constant, the inductor current decreases linearly.

The inductor current decrease during the off state is given by:

$$\Delta I_L\,(-) = \frac{\left(V_O + V_d + I_L \times R_L\right) - V_I}{L} \times T_{OFF}$$

The quantity ΔI_L (–) is also the inductor ripple current.

In steady-state conditions, the current increase, ΔI_L (+), during the on time and the current decrease, ΔI_L (–), during the off time are equal. Otherwise the inductor current would have a net increase or decrease from cycle to cycle which would not be a steady state condition. Therefore, these two equations can be equated and solved for Vo to obtain the continuous conduction mode boost voltage conversion relationship:

The steady-state equation for Vo is:

$$V_O = \left(V_I - I_L \times R_L\right) \times \left(1 + \frac{T_{ON}}{T_{OFF}}\right) - V_d - V_{DS} \times \left(\frac{T_{ON}}{T_{OFF}}\right)$$

And, using T_S for $T_{ON} + T_{OFF}$ and using $D = T_{ON} / T_S$ and $(1–D) = T_{OFF} / T_S$, the steady-state equation for Vo is:

$$V_O = \frac{V_I - I_L \times R_L}{1-D} - V_d - V_{DS} \times \frac{D}{1-D}$$

In the above equations for ΔI_L (+) and ΔI_L (–), the output voltage was implicitly assumed to be constant with no ac ripple voltage during the on and off times. This is a common simplification and involves two separate effects. First, the output capacitor is assumed to be large enough so that its voltage change is negligible. Second, the voltage due to the capacitor ESR is assumed to be negligible. These assumptions are valid because the ac ripple voltage is designed to be much less than the dc part of the output voltage. The above voltage conversion relationship for Vo illustrates that Vo can be adjusted by adjusting the duty cycle, D, and is always greater than the input because D is a number between 0 and 1. This relationship approach one as D approaches zero and increases without bound as D approaches one. A common simplification is to assume V_{DS}, V_D, and R_L are small enough to ignore. Setting V_{DS}, V_D, and R_L to zero, the above equation simplifies considerably to:

$$V_O = \frac{V_I}{1-D}$$

The relationship between the average inductor current and the output current for the continuous mode boost power stage is given by:

$$I_{L(Avg)} \times \frac{T_{OFF}}{T_S} = I_{L(Avg)} \times (1-D) = I_O$$

$$I_{L(Avg)} = \left(\frac{I_O}{1-D}\right)$$

Another important observation is that the average inductor current is proportional to the output current, and since the inductor ripple current, ΔI_L, is independent of output load current, the minimum and the maximum values of the inductor current track the average inductor current exactly.

2.2 Simulation of Boost Converter POWER 4-5-6 software:

Power 4-5-6, Release 8, is the only switching power supply design program that provides component design, large signal simulation, feedback control design, and small signal analysis. It includes various features such as Power Stage Design, Control Stage design, Magnetic Design and Power Stage loss and stress analysis for all major components.

This converter analysis has been carried out in POWER 4-5-6 software for better understanding of theoretical concepts of simple Boost Converter. Following are the simulation results. Simulation is carried out for higher input current 17A at 26V as minimum input and 44V as maximum output. Output voltage 50V of the Boost Converter is obtained that varies between 49.9V to 50.2V at maximum duty cycle 0.48 as shown in Figure 2.2.5.

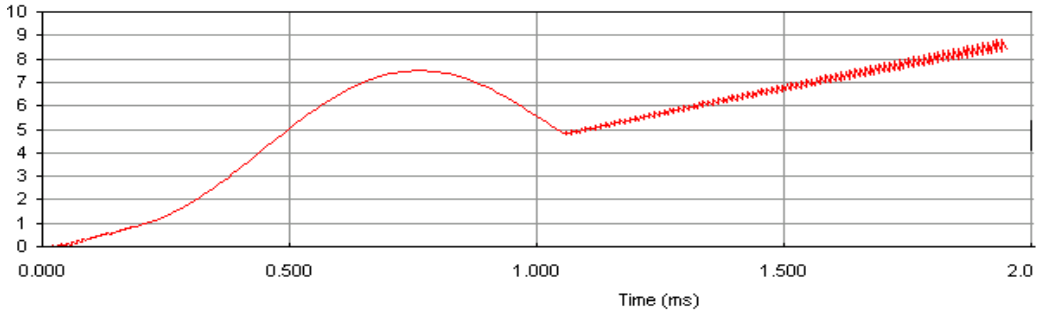


Figure 2.2.1 Startup current of Boost Inductor

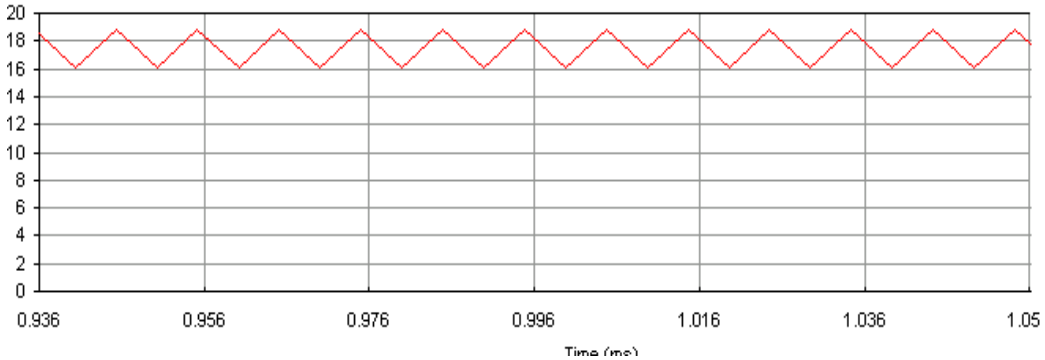


Figure 2.2.2 Boost inductor continuous steady state current for duty cycle D= 0.48

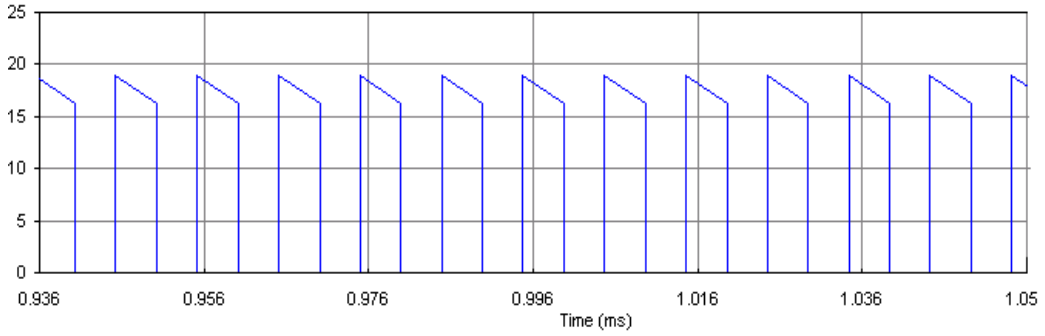


Figure 2.2.3 Boost Schottky Diode output current for D=0.48

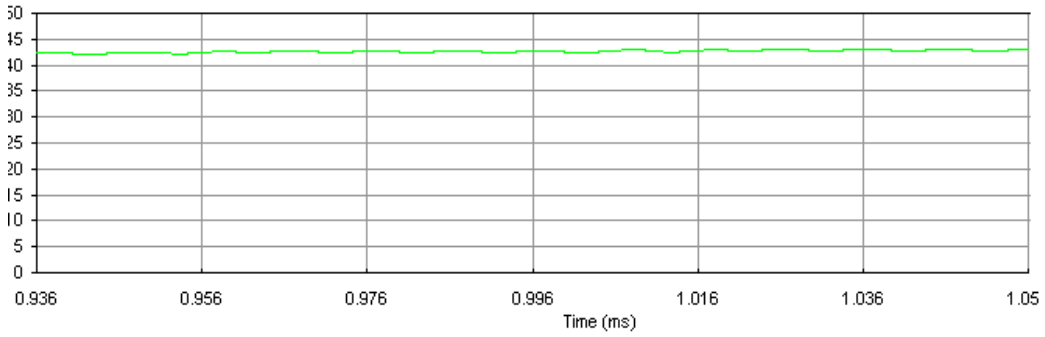


Figure 2.2.4 Output Voltage waveform of Boost Converter for D=0.09

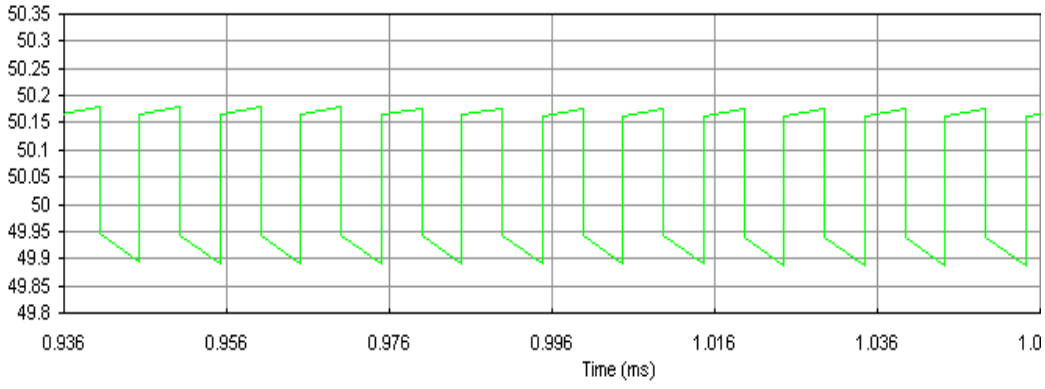


Figure 2.2.5 Output Voltage waveform of Boost Converter for D= 0.48

2.3 ZVT (Zero Voltage Transition) in Boost Converter:

Zero Voltage Transition is introduced in conventional Boost Converter by connecting a resonant inductor Lr, auxiliary switch M2 and capacitor C in parallel of main switch M1.Other ZVT circuit includes Dr, Da, Dc, Cb, Drr and Crr as shown in Figure 2.3.1.

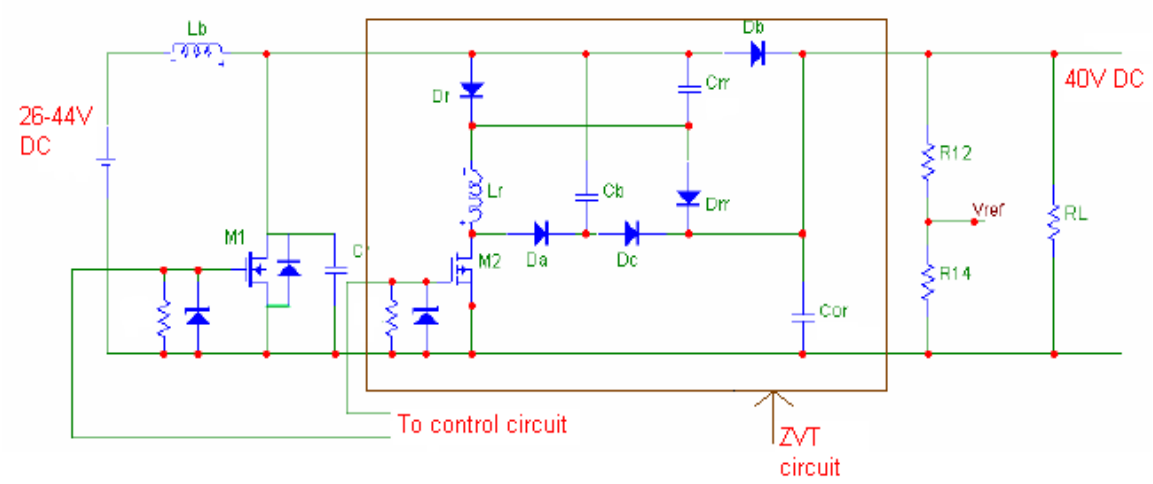


Figure 2.3.1 ZVT Boost converter

Unlike simple Boost converter, the performance of ZVT Boost Converter is divided into six stages shown in Figure 2.3.2.

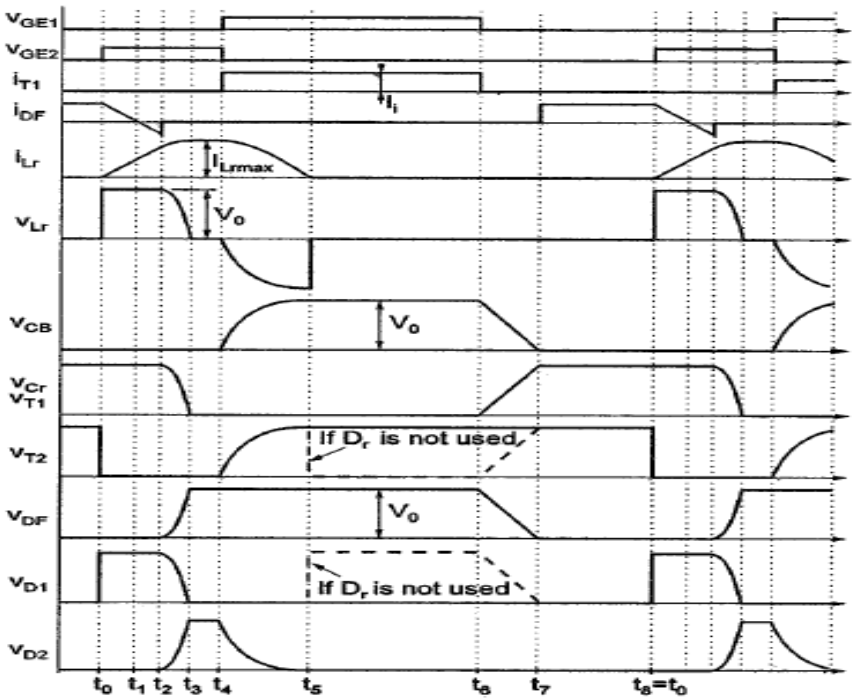


Figure 2.3.2 Waveforms of ZVT Boost converter

Stage 1

This stage begins with MOSFETs M1 (main) and M2 (auxiliary) turned off. Db is on and is conducting current I_{IN} of the main inductor Lb. The turn on signal is sent to transistor M2 from the microprocessor at which time Dr and M2 are turned on at near ZCS. The ZVT inductor Lr limits the rate of rise of the current through Dr and M2. As the current in M2 reaches I_{IN}, Db current falls to zero, and thus Db turns off under ZVS.

Stage 2

Diode Db and transistor M1 are now both in the off state. VCr =Vout. A parallel resonance between Lr and Cr begins to resonate through the path Cr–Dr–Lr–M2 under the input current Iin and with the initial current of ILr of the inductor Lr. When the transfer of energy stored in capacitor Cr to the inductor Lr is completed, and the current and energy values of the inductor Lr reach their maximum level at the same time. Now only transistor M2 is on and is conducting the maximum current of the inductor Lr. Also, the VCr = 0.

Stage 3

Transistor M1 receives a turn on signal and at the same time the turn on signal is removed from transistor M2. So, M1 turns on under ZVS and conducts current Iin and M2 is turns off under near ZVS through Cb. Serial resonance between Lr and Cb starts to resonate through Lr-Da-Cb-Dr under the maximum inductor current. Thus, throughout this stage the energy stored in the inductor Lr is transferred to capacitor Cb. As soon as the inductor current drops to zero, auxiliary diodes Dr and Da are turned off under ZCS through Lr, and Cb is charged to Vo.

Stage 4

Transistor M1 continues to conduct input current Iin, and ZVT circuit is not active. The duration of this stage is the ‘on’ time of the MOSFET M1 as a traditional normally operating boost converter and is determined by PWM control.

Stage 5

The gate signal of the main transistor M1 is removed and M1 turns off under ZVS. Auxiliary diode Dc turns on with ZVS because of capacitor Cb being charged to Vo. During this stage Cr is charged and Cb is discharged. When Cr voltage reaches Vo and Cb goes to zero simultaneously, diode Db is turned on with ZVS and the auxiliary

diode Dc is turned off with ZVS. Thus, Cb restricts the rise rate of transistor M1 voltage and M1 is turned off under near ZVS.

Stage 6

Main diode Db continues conducting the input current Iin and the snubber circuit is not active. This stages duration is the 'off' time of the transistor M1 as in a conventional PWM boost converter. At the end of stage 6, stage 1 would again begin starting another switching cycle.

2.4 Design of Power stage ZVT Boost Preregulator:

➢ Input voltage selection:

The required input voltage range of a power supply impacts its cost, size and performance significantly. The drawback of going to wider input voltage range is that it can force lower turns ratio or higher voltage stresses on switching devices. Hence a reasonable voltage range of 26-44 V is opted in present design.

➢ Switching frequency selection:

The switching frequency determines many of the converter performance merits. Choice of switching frequency is often dictated by the particular application and its size, cost and schedule risks constraints. Higher switching frequency leads to smaller magnetic and faster loop response of the converters. But the switch turn off losses, gate drive losses and output rectifier switching losses are proportional to switching frequency. The ZVT characteristics of Boost converter can be exploited to push the switching frequency higher without corresponding increase in switching losses. However, not all switching losses are eliminated in the ZVT circuit. For the purpose of prototype circuit switching frequency of 100 KHz is chosen for the design.

➢ Duty cycle Range selection:

The selection of D involves a tradeoff between the voltage and current stresses of the switches. For a given V_I, a smaller D corresponds to a smaller N, which results in higher current stresses of MOSFET. A larger D leads to higher voltage stresses of MOSFET. In order to minimize the stress over the input voltage range, the design goal should be to ensure that the stress at minimum ad maximum input voltages is equal.

Given the input voltage range of 26 – 44 V, the duty cycle D can be calculated as follows:

$$D = 1 - \frac{V_{in}}{V_{out}}$$

$D_{MAX} = 1 - 26V/40V = 0.40$

$D_{MIN} = 1 - 44V/40V = 0.1$

- **Components Selection:**

Power Supply Specifications determine the requirements of components to be used**.**

(a) Input Boost Critical Inductance:

The minimum value of inductor to maintain continuous conduction mode is determined by following procedure: -

The minimum value of average inductor current to perform continuous current mode operation is given by

$$I_{(min-avg)} = \frac{\Delta I_L}{2}$$

Now L is calculated such that above relationship is satisfied. To solve above equation ΔIL (+) relationship is used. The worst condition for the boost power stage is at input voltage equal to one-half of the output voltage because this gives the maximum ΔIL.

Now substituting and solving for L_{min}:

$$L_{min} \geq \frac{1}{2} \times \left(V_I + V_{DS} - I_L \times R_L \right) \times \frac{T_{ON}}{I_{L(min)}}$$

Above equation can be simplified as

$$L_{min} \geq \frac{V_O \times T_S}{16 \times I_{O(crit)}}$$

Substituting the values of *Vo, Ts* and $Io_{(crit)}$ in above equation,

$$L_{\min} = \frac{40V * 10\mu}{16 * 0.3}$$

$$L_{\min} = 83\mu H$$

Using above calculated inductance value ensure continuous current conduction above $I_{o(crit)}$.

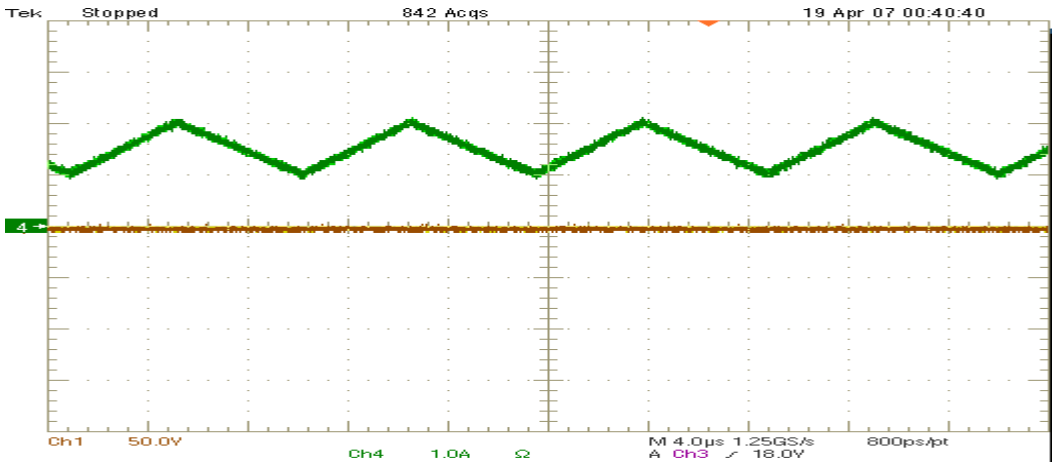


Figure 2.4 practically observed waveform of continuous conduction of Boost inductor from V_I= 26V to 42V

Figure 2.4 shows practically observed waveforms of Boost inductor current which shows continuous conduction of Boost converter.

(b) Output Capacitance:

In switching power supply power stages, the function of output capacitance is to store energy. The energy is stored in its electric field due to the voltage applied. Thus, qualitatively, the function of a capacitor is to attempt to maintain a constant voltage.

The output capacitance for a boost power stage is generally selected to limit output voltage ripple to the level required by the specification. The series impedance of the capacitor and the power stage output current determine the output voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C).

For continuous inductor current mode operation, to determine the amount of capacitance needed as a function of output load current, Io, switching frequency fs and desired output voltage ripple, ΔV_O, the following equation is used assuming all the output voltage ripple is due to the capacitor's capacitance. This is because the output capacitor supplies the entire output load current during the power stage on state.

$$C \geq \frac{I_{O(Max)} \times D_{Max}}{f_s \times \Delta V_O}$$

Where, Io (Max) is the maximum output current and D_{MAX} is the maximum duty cycle. Substituting values of $I_{O\,(MAX)}$, D_{MAX}, f_S and ΔV_O in above equation,

$$C \geq \frac{8.84A * 0.5}{100kHz * 500mV}$$

$$C \geq 88.4\mu F$$

In many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected.

For continuous inductor current mode operation and assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the ripple to peak-to-peak is:

$$ESR \leq \frac{\Delta V_O}{\left(\frac{I_{O(Max)}}{1-D_{Max}} + \frac{\Delta I_L}{2}\right)}$$

Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. Referring to Figure 2.1.1, the output capacitor ripple current is the output diode current, ICR1, minus the output current, Io. The RMS value of the ripple current flowing in the output capacitance (continuous inductor current mode operation) is given by:

$$I_{C\,RMS} = I_O \times \sqrt{\frac{D}{1-D}}$$

ESL can be a problem by causing ringing in the low megahertz region but can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor) and replacing one large device with several smaller ones connected in parallel.

(c) Power Switch:

In switching power supply power stages, the function of the power switch is to control the flow of energy from the input power source to the output voltage. In a boost power stage, the power switch (Q1 in Figure 2.1.1) connects the input to the output when the switch is turned on and disconnects when the switch is off. The power switch must conduct the current in the inductor while on and block the full output voltage when off. Also, the power switch must change from one state to the other quickly in order to avoid

excessive power dissipation during the switching transition. The type of power switch considered in this project is a n-channel power MOSFET APT20M22LVFR.

Other power devices are available but in most instances, the MOSFET is the best choice in terms of cost and performance (when the drive circuits are considered). The two types of MOSFET available for use are the n-channel and the p-channel. N-channel MOSFET is popular for use in boost power stages because gate drive of this n-channel MOSFET is simpler than the gate drive required for a p-channel MOSFET.

The power dissipated by the power switch, Q1, is given by:

$$P_{D(Q1)} = \left(\frac{I_O}{1-D}\right)^2 \times R_{DS(on)} \times D + \frac{1}{2} \times (V_O) \times \left(\frac{I_O}{1-D}\right)^2 (t_r + t_f) \times f_s + Q_{Gate} \times V_{GS} \times f_s$$

where t_r and t_f are the MOSFET turn-on and turn-off switching times.

C_{GS} is the MOSFET gate-to-source capacitance.

All these parameters are taken from datasheet and power dissipated calculated for APT20M22LVFR MOSFET is 61W.

Other than selecting p-channel versus n-channel, other parameters considered while selecting the appropriate MOSFET are the maximum drain-to-source breakdown voltage (V_{DSS}) and the maximum drain current $I_{D\ (MAX)}$.

The MOSFET selected should have a V_{DSS} rating greater than the maximum output voltage, and some margin should be added for transients and spikes. The one that is selected has 200V max V_{DSS}. The MOSFET selected should also have an $I_{D\ (MAX)}$ rating of at least two times the maximum inductor current. This one has 100A as maximum drain current.

However, many times the junction temperature is the limiting factor, so the MOSFET junction temperature should also be calculated to make sure that it is not exceeded. The junction temperature can be estimated as follows:

$$T_J = T_A + P_D \times R_{\Theta JA}$$

where T_A is the ambient or heat sink temperature and R©JA is the thermal resistance from the MOSFET chip to the ambient air or heat sink.

(d) Output Diode:

The output diode conducts when the power switch turns off and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, breakdown voltage, current rating, low forward-voltage drop to minimize power dissipation and appropriate packaging.

Usually a Schottky rectifier is used for low power applications. The breakdown voltage must be greater than the maximum output voltage and some margin should be added for transients and spikes. The current rating should be at least two times the maximum power stage output current (normally the current rating will be much higher than the output current because power and junction temperature limitations dominate the device selection). The voltage drop across the diode in a conducting state is primarily responsible for the losses in the diode. The power dissipated by the diode can be calculated as the product of the forward voltage and the output load current. The switching losses that occur at the transitions from conducting to non-conducting states are very small compared to conduction losses and are usually ignored.

The power dissipated by the output rectifier is given by:

$P_D = V_D \times I_O$

where V_D is the forward voltage drop of the output rectifier.

The one used in the project is 45CKQ100 and its ratings are:

V_{RRM} =100 V

$I_{F\,(AVG)}$ = 45 A

P_D = 7.87 W

(e) Selection of ZVT circuit components:

The value of L_r can be calculated using the following equation:

$$\frac{V_o}{L_r} 3t_{rr} \le I_{in,\max}$$

(where t_{rr} represents the reverse recovery time of the main diode Db. Db is a Schottky diode 45CKQ100 with a very fast recovery time.)

$Vo/L_r \times 3 \times t_{rr} < P/V_{INMIN}$

$L_r \geq 416$ nH

The value of C_b can be calculated using the following equation:

$$\frac{\pi}{2}\sqrt{L_r C_B} \geq t_{f2}$$

Where t_{f2} represents the fall time of the auxiliary MOSFET M2.

$$\frac{\pi}{2}\sqrt{150nH} * C_b \geq 10ns$$

$$C_b \geq 0.27nF$$

Selected value for C_B is 1 nF

The value of C_r can be calculated using the following equation:

$$\frac{C_r + C_B}{I_{in,\max}} V_o \geq t_{f1}$$

Where t_{f1} represents the fall time of the main MOSFET M1.

$$C_r + \frac{1nF}{17A} * 50 \geq 10ns$$

$$C_r \geq 2.4nF$$

These values of C_r, C_B, and L_r also satisfy the following equation:

$$\frac{1}{2}L_r(I_{in,\max} + I_{rr,\max})^2 + \frac{1}{2}C_r V_o^2 \cong \frac{1}{2}C_B V_o^2$$

A reference voltage of 5V required by the control circuit is provided through a voltage divider. R_{12} and R_{14} can be calculated as follows:

$R_{14}/ (R_{14} + R_{12})* V_O = V_{REF}$

Let R_{14} = 1K

1/ (1K + R_{12})* 40 = 5

R_{12} = 7K

Thus R_{12} = 1K

R_{14} = 7K

2.5 Design of Control circuit of ZVT Boost preregulator:

Current mode control has been preferred over voltage mode control as described in Chapter 1 and hence current mode control using UC1846 IC is applied here.

➢ Description of IC1846:

There are two feedback loops- an outer loop consisting of output voltage sensor (EA) and inner loop consisting primary peak current sensor (PWM) and current sensing resistor or current transformer which converts ramp on a step MOSFET currents to ramp on a step voltage.

Regulation against line load is done by variation of the power MOSFET on time. On time is determined by both EA and PWM voltage comparator that compare V_{error} to the voltage at the output of current transformer resistor or sensing resistor.

Power MOSFET on time is determined as follows. Referring Figure 2.5.2, an internal oscillator whose period is set by external discrete components Rt, Ct, pin 8 and 9, generate narrow clock pulses. Oscillator period is approximately 0.9RtCt. At every clock pulse, feed forward FF is reset causing its output Q to go low. The duration of low time at Q is the duration of high time at either of the chip outputs A or B and hence the duration of power MOSFET on times.

Now when PWM voltage comparator output goes high, FF is set, thus terminating the Q low and hence the high time at A or B and turns off the power MOSFET. Thus the instant at which PWM comparator goes high determines the end of the on time.

Now the PWM comparator compares the ramp on a step current sensing voltage from the pin 3 and 4 through current transformer and compares with V_{error}. When both these voltages are equal PWM goes high, sets FF, Q goes high and whichever of A or B had been high, goes back down.

A low output from FF occurs once per clock period. It starts low at every clock pulse and goes back high when PWM noninverting input equals the DC level of the EA output. N channel MOSFET require positive going signals for turn on.

➢ Programming IC1846:

(a)Oscillator Design:

$$f_{osc} = 2.2 / (Rt \times Ct)$$
$$= 2.2 / (10\ K \times 2.2\ nF)$$
$$= 100\ KHz$$

(Values of Rt and Ct selected from the graph given in datasheet of IC)

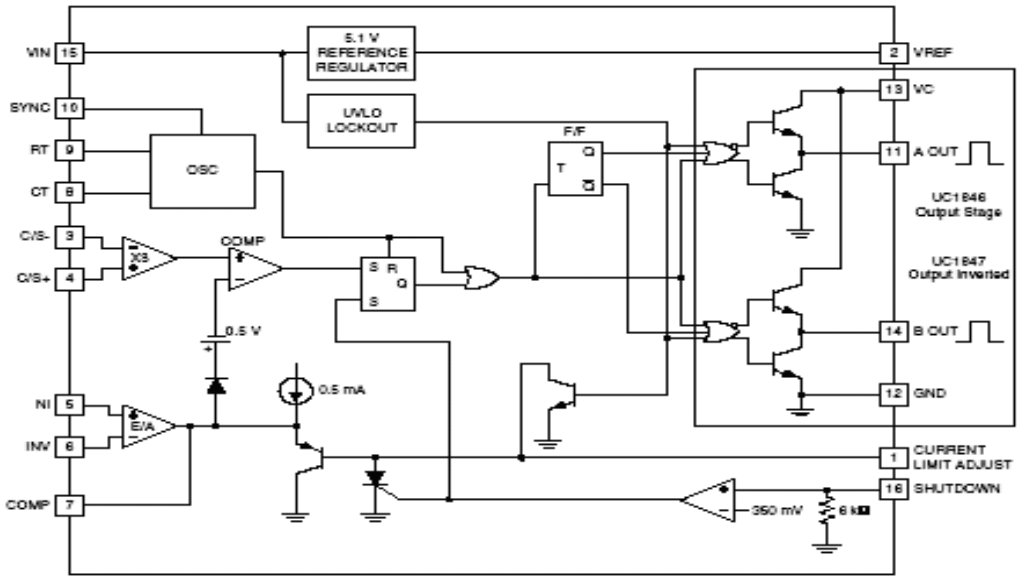


Figure 2.5.1 Block Diagram of IC 1846

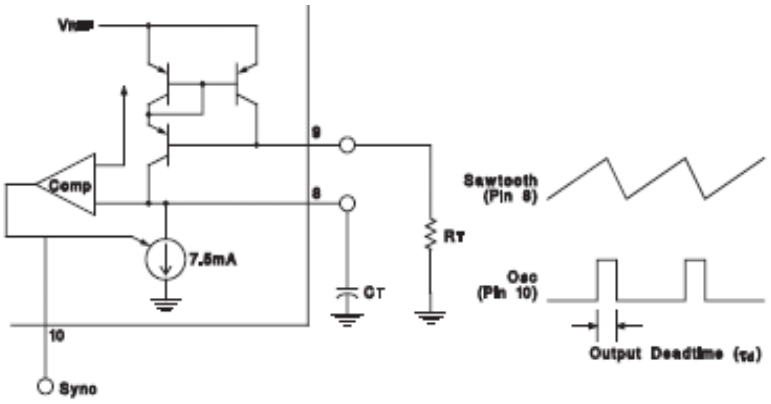


Figure 2.5.2 Oscillator circuit of 1846

Waveforms of oscillator output of 1846 as observed in laboratory are shown in Figure 2.5.3.

Td = dead time

= 145 Ct

= 145 × 2.2 nF

= 0.3 µs

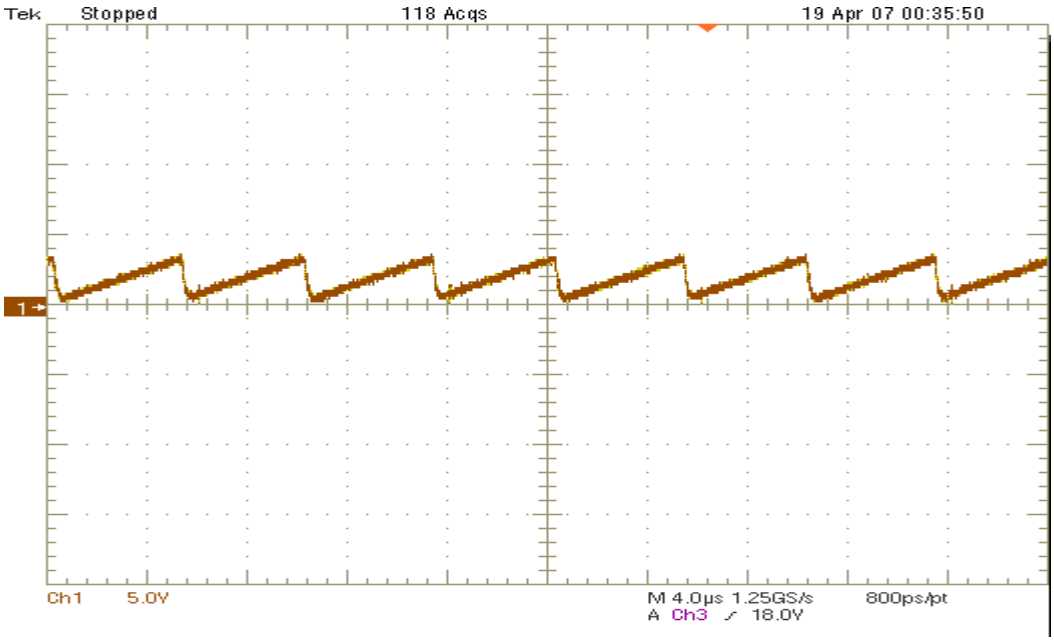


Figure 2.5.3 practically observed oscillator output of 1846

(b)Current Limit:

Peak current limit in 1846 turns the switch off when instantaneous current through it exceeds the maximum value and is activated when pin 1 is pulled below ground.

The current limit value is set by a simple voltage divider from the reference voltage to the current sense transformer. R1 and R2 are the resistors in voltage divider to set a predetermined voltage reference at pin 1.

V_{ref} = 5.1 V

R_s = 30 ohm

R1 = 10K

I_S = 60 mA

Peak current is given by,

$$I_s = \frac{R_2 V_{ref} - 0.5}{(R_1 + R_2)/(3 * R_s)}$$

Substituting values of above terms,

R_2 = 1.088 K

Thus, selected values are,

R_1= 10 K

R_2 = 1.088 K

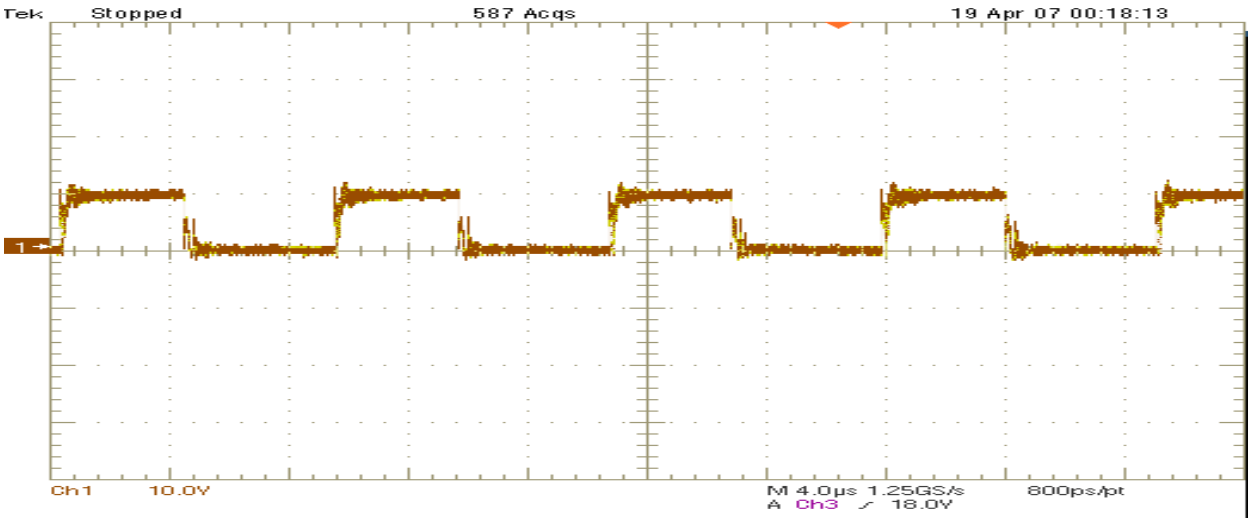


Figure 2.5.4 practically observed Gate drive pulses at the output of IC1846

- **Current Sensing with a current transformer:**

The sense resistor to the circuit can be connected through a current transformer.

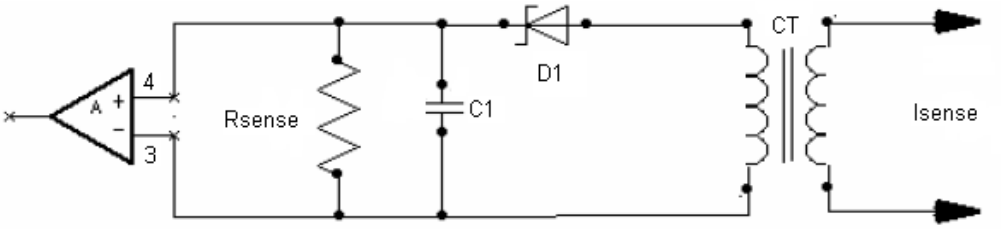


Figure 2.5.5 Current Sense transformer

The output ramp as observed by this current transformer on its secondary side is shown in Figure 2.5.6.

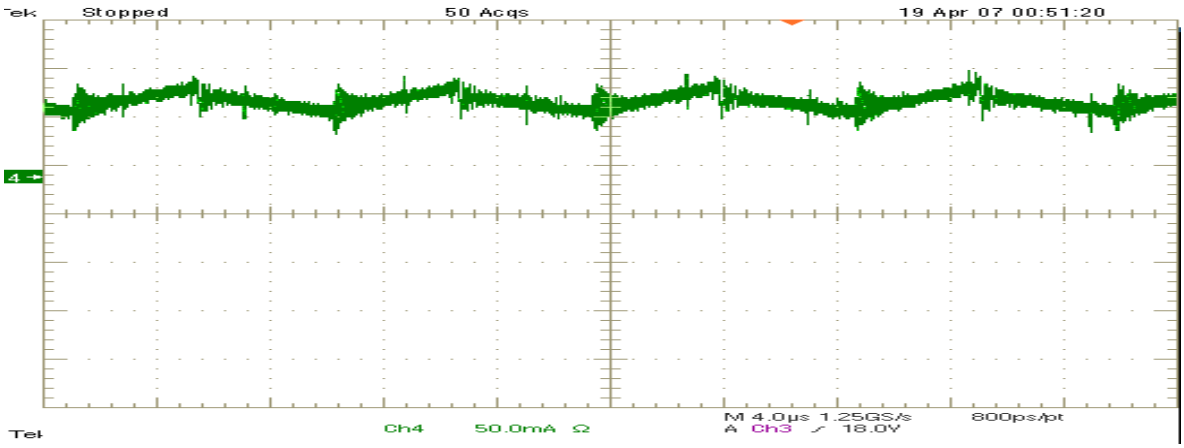


Figure 2.5.6 Output of current transformer

The primary current monitored by the current transformer is

$$I_{P(avg)} = \frac{P_{out}}{V_{in,\min} * 2 * D_{\max} * \eta}$$

$$I_{P(avg)} = 4.85A$$

Assuming power dissipation of 0.1W in primary winding, V_P can be calculated as

V_P = 0.1/4.85 = 0.0206V

Assume 1V as secondary is connected to current mode control circuit that requires 1 V

V_s = 1+0.7(diode drop)

= 1.7 V

Error amplifier controls the peak voltage across R_{sense} and turns ratio is given by,

$$\frac{N_s}{N_p} = \frac{Vs}{V_P} = \frac{1.7}{0.0206} = 83$$

Hence the value of sense resistor fixes on,

$$I_{S\,(AVERAGE)} = \frac{N_p * I_{P\,(AVERAGE)}}{N_s} = \frac{4.85}{83} = 0.0584\ A$$

$$R_{SENSE} = \frac{1.7}{0.0584} = 29\ \Omega$$

➢ Closed Loop Design:

The compensation technique adopted is single pole – single zero compensation since it is best suited for those topologies that exhibit a single filter response.

➢ Stability criteria:

"The criteria for stable loop are that at the frequency where the total open loop gain is unity (crossover frequency), the total open loop phase shift of all elements involved must be less than 360 degrees. The amount by which the total phase shift is less than 360, at the frequency where the total open loop gain is unity, is called the phase margin".

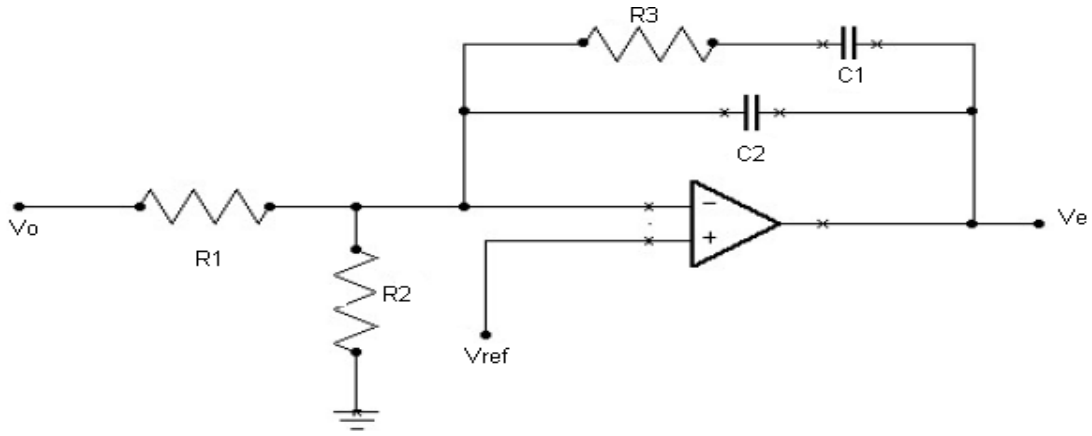


Figure 2.5.7 Error Amplifier Compensation

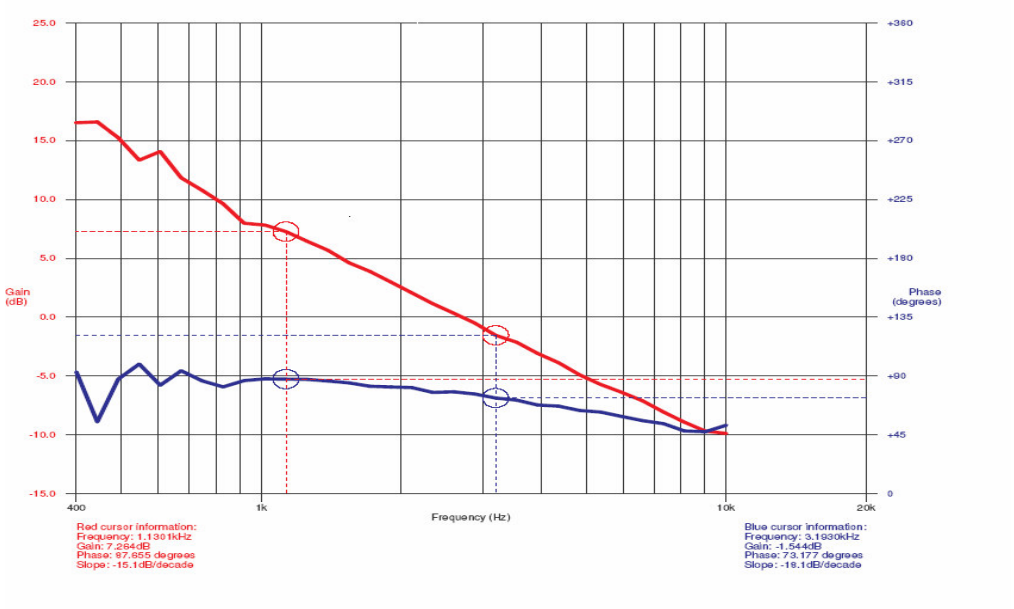


Figure 2.5.8 Phase and Gain response of feedback loop as shown by Phase sensitive meter

Error Amplifier compensation as shown in Figure 2.5.7 is done using following values.

Vo (R_2/ R_2+R_1) = V_{REF}

40 (R_2/ R_2+ 50K) = 5.1

R_2 = 7.3 K

Selected values:

R_1 = 50 K,

R_2 = 7.5 K,

R_3 = 50 K,

C2 = .212 nF,

C1 = 8 nF

With above values Phase and Gain responses are plotted which satisfies the stability criteria. Figure 2.5.8 shows the phase and gain response of the control stage of converter measured by phase sensitive meter. Phase shift of 73.177 degrees is observed and zero gain is obtained at crossover frequency 1.28 KHz.

➢ Control circuit Design for ZVT:

The control logic designed to get desired waveforms as shown in figure 2.5.9; following circuit has been added to the control circuit designed for Boost converter using PWM IC 1846.

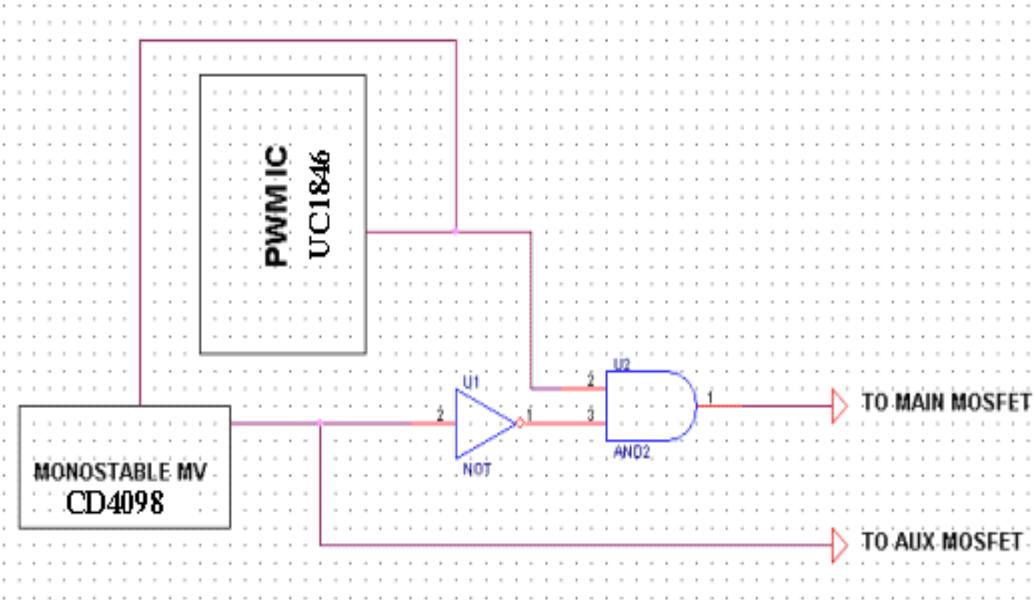


Figure 2.5.9 Control Logic for ZVT circuit

As shown in Figure 2.5.9, the output waveform of control IC 1846 is given to monostable multivibrator IC CD4098 and NAND gate IC 4093. Then output of monostable multivibrator is given to NAND gate and to the gate drive of auxiliary MOSFET. Thus NAND IC 4093 performs the NAND logic with its two inputs and its output is given to the main MOSFET.

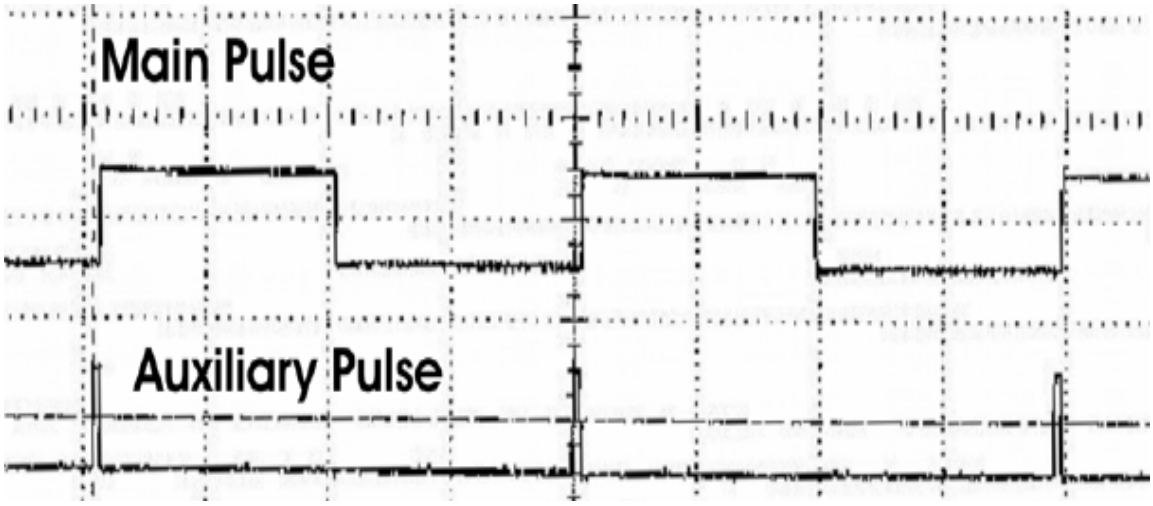


Figure 2.5.10 Waveforms of Control Logic circuit of ZVT circuit

The on time of the auxiliary MOSFET is set at 200ns to ensure the MOSFET was conducting for a long enough period of time. The on time of main MOSFET was calculated using operation switching frequency, 100 KHz and a 50% duty cycle.

Gate waveforms obtained by this logic are shown in Figure 2.5.10 where main pulse is given to gate of main MOSFET and Auxiliary Pulse to gate of the Auxiliary MOSFET.

$T_{OFF} = 0.5 * T = 5us$

$T_{ON} = T_{MAIN} + T_{AUX} = 4.8us + 200ns = 5us$

2.6 Breadboard model of ZVT Boost converter:

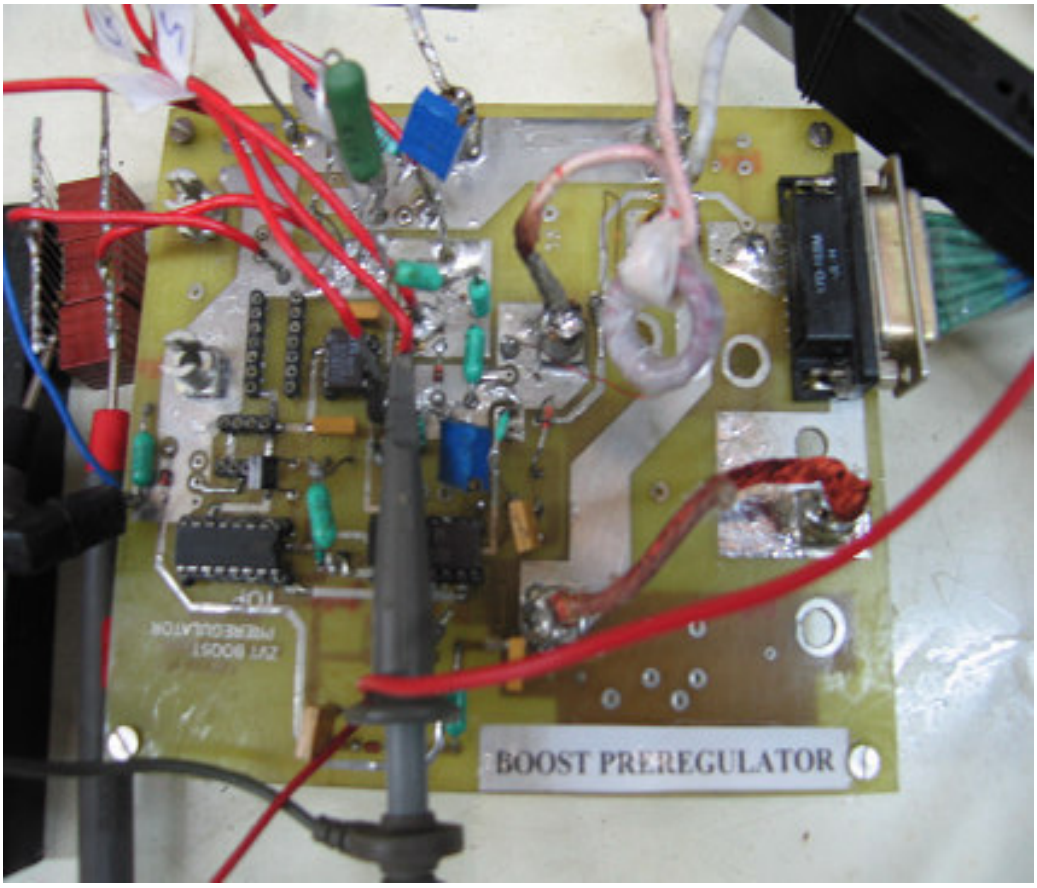


Figure 2.6 Picture of Breadboard model of ZVT Boost converter

2.7 Complete Schematic of ZVT Boost Converter:

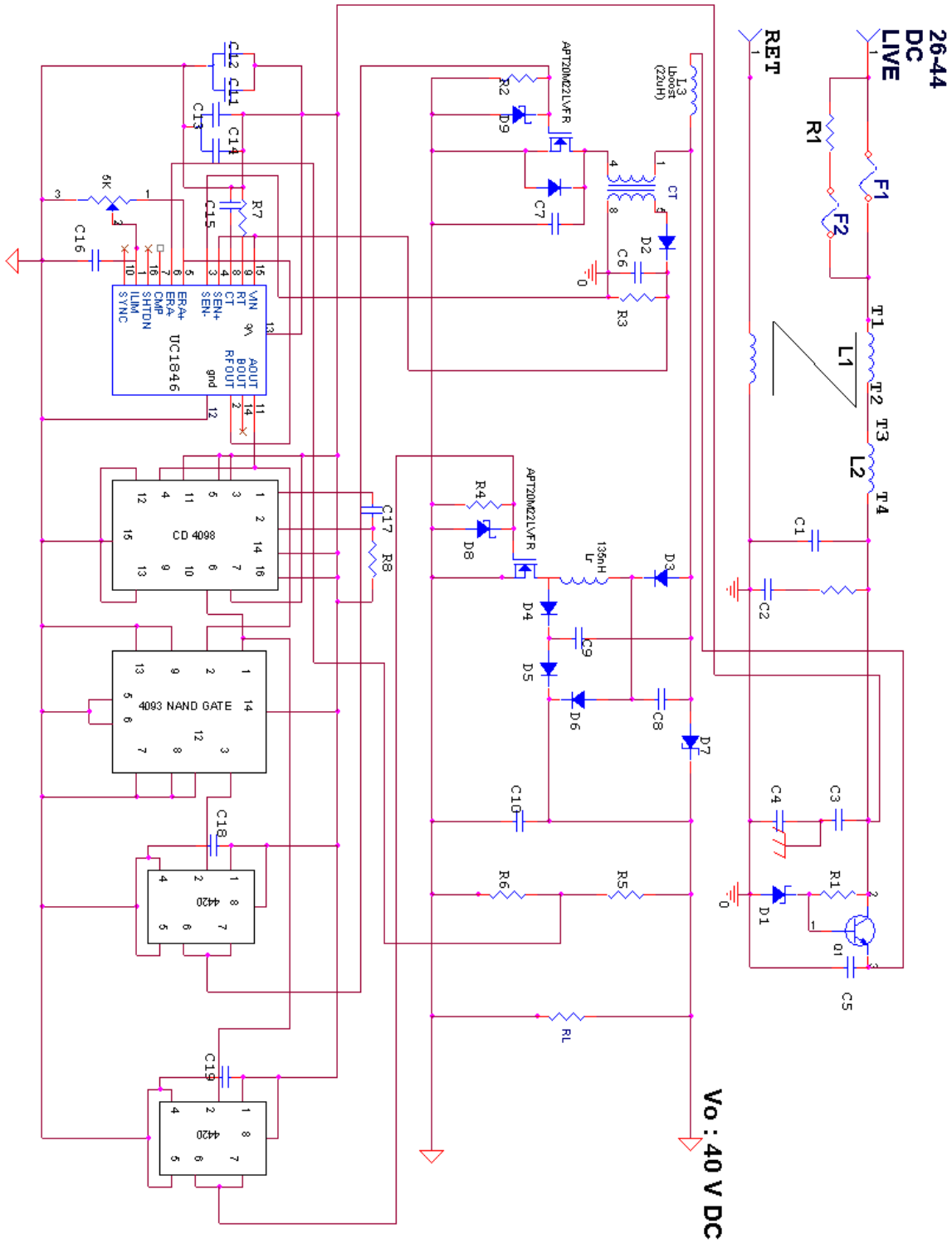


Figure 2.7 Schematic of ZVT Boost Converter

Table 2.7 Component List for ZVT Boost preregulator:

Serial No	Component	Description	Value
1	R1	Metal film oxide	6.8K, ¼ W
2	R2	Metal film oxide	1.5K, ¼ W
3	R3	Metal film oxide	30Ω, ¼ W
4	R4	Metal film oxide	1.5K, ¼ W
5	R5	Metal film oxide	9K, ¼ W
6	R6	Metal film oxide	1K, ¼ W
7	R7	Metal film oxide	10K, ¼ W
8	R8	Metal film oxide	1.5K, ¼ W
9	D1	ZENER	12V
10	D2	ZENER	10V
11	D3	SCHOTTKY	100V/45A
12	D4	SCHOTTKY	100V/45A
13	D5	SCHOTTKY	100V/45A
14	D6	SCHOTTKY	100V/45A
15	D7	45CKQ100,SCHOTTKY	100V/45A
16	D8	ZENER	10V
17	D9	ZENER	10V
18	C1	Tantalum (CLR)	22 uF/100V
19	C2	Tantalum (CLR)	88 uF/100V
20	C3	CKR06	.1uF/25V
21	C4	CKR06	.1 uF/25V
22	C5	CKR06	.1 uF/25V
23	C6	CKR06	.1 uF/25V
24	C7	Chip	3.3nF/100V
25	C8	Chip	20nF/100V
26	C9	Chip	300pF/100V
27	C10	Tantalum	88uF/100V
28	C11	CKR06	.1uF/25V
29	C12	CKR06	1uF/25V
30	C13	CKR06	.1uF/25V
31	C14	CKR06	1uF/25V
32	C15	CKR06	2nF/25V
33	C16	CKR06	.1uF/25V
34	C17	CKR06	1KpF/25V
35	C18	CKR06	.1uF/25V
36	C19	CKR06	.1uF/25V

2.8 Test Results:

Table 2.8 Test Results of ZVT Boost Converter without connecting Half Bridge Converter

Vin	Iin	Vo	Io	Efficiency(%)
26.3	4.49	40.217	2.87	97
28.1	4.19	40.231	2.873	98
30	3.91	40.261	2.875	98.6
32	3.66	40.277	2.876	98.9
34	3.44	40.297	2.878	98.9
36	3.25	40.313	2.879	99
38	3.07	40.316	2.879	99
40	2.90	40.250	2.875	99

2.9 Pragmatic Waveforms:

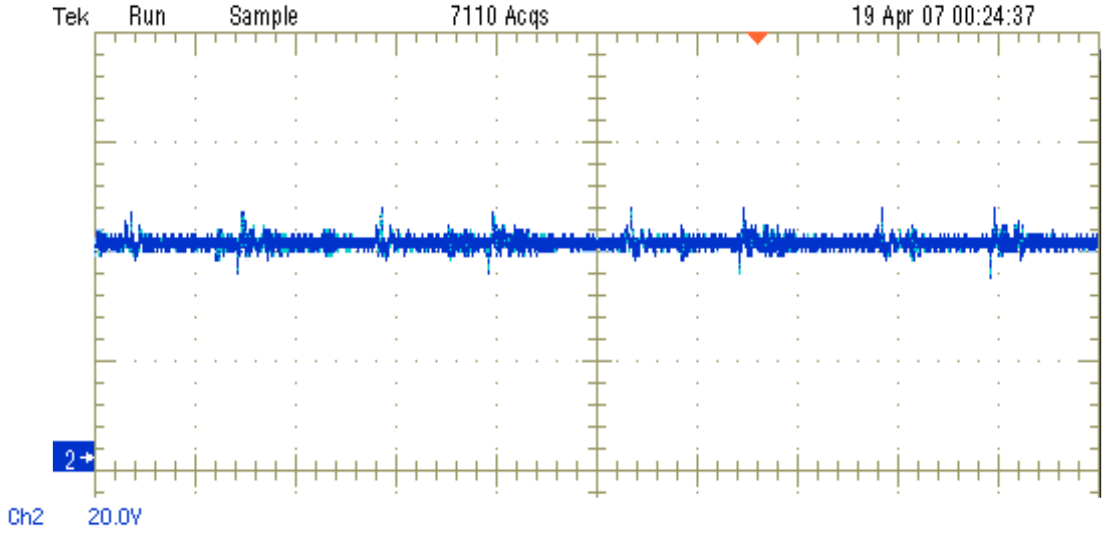


Figure 2.9.1 Output voltage waveform of Boost converter $V_O = 40V$

Channel 2 Output voltage waveform of Boost converter without connecting Half Bridge Converter

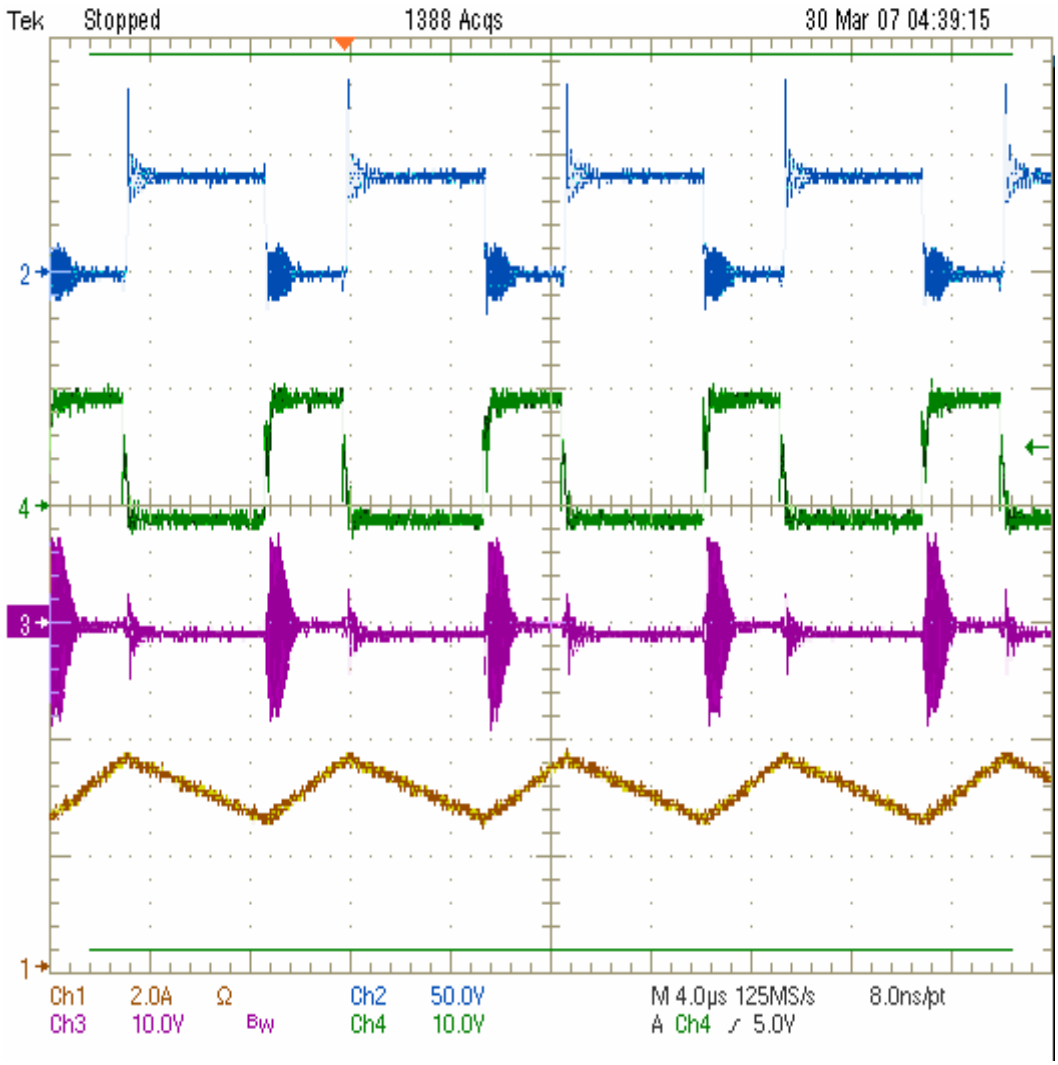


Figure 2.9.2 waveforms at D = 0.45 and V_{IN} = 26.3

Channel 1 Boost inductor current (Continuous current mode)
Channel 2 V_{DS} (40V)
Channel 3 Input current Ramp as seen at secondary of Current Transformer
Channel 4 V_{GS} (10V)

2.10 Design of EMI Filter:

A second order parallel damped filter is designed for providing 50 dB attenuation at 100 KHz. This makes the corner frequency of the common mode filter:

Where att = attenuation needed at the switching frequency in negative dB.

$$f_c = f_{sw} \times 10^{(\frac{att}{40})}$$

$f_C = f_{SW} \times 10^{(att/40)}$

$fc = 100\ KHz \times 10^{(-50/40)}$

$fc = 5.623\ KHz$

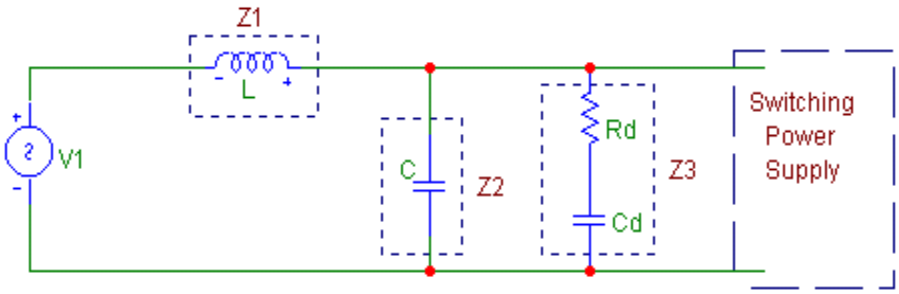


Figure2.10 Parallel Damped Filter

As mentioned above, the damping capacitor needs to be selected as four times the filter capacitor. The maximum value of capacitor available Cd = 86 μF and hence the value of the filtering capacitor C = 22 μF as Cd = 4*C. Thus the value of inductance required in designing the second order filter can be computed as:

$$L = \frac{1}{4\pi^2 f_c^{\,2} C}$$

$$L = 37\mu H$$

55929 core with winding area = 308,000 circular mills and A_L = 185 mH/1000 turns is selected for designing this choke. The number of turns required to obtain the above inductance can be calculated as:

$$N = \frac{1000^2 * 37 * 10^{-6}}{185 * 10^{-3}}$$

$$N = 20 turns$$

The maximum input current is calculated as:

$$I_{\max} = \frac{P_o}{\eta * V_{in,\min}}$$

$$I_{\max} = 2.42A$$

The bias level in oersteds is calculated as:

The bias level in oersteds is calculated as:

$$H = \frac{0.4\pi NI}{L_m}$$

$$H = 7 oersteds$$

There is negligible Roll – off in percent initial permeability for the above bias level. The largest feasible wire size selected, based on 16 % winding factor, is 350/40 litz wire (Aw = 3363.5 circular mills)

wf = (Aw * N)/W

Aw = (wf * W)/N = (0.16 *308000)/15 = 3285.33 circular mills.

3.1 Introduction of Half Bridge converter:

The second stage presented in this report is Half Bridge Converter followed by Boost preregulator. Half Bridge Topology subject their transistors in the off state to a voltage stress equal to the DC input voltage and not to twice as in push pull, single ended, interleaved forward converter topologies.

Its major advantage is that, just as the double ended forward converter, it subjects the off transistor to only V_{DC} and not twice that as do the push-pull single ended forward converter.

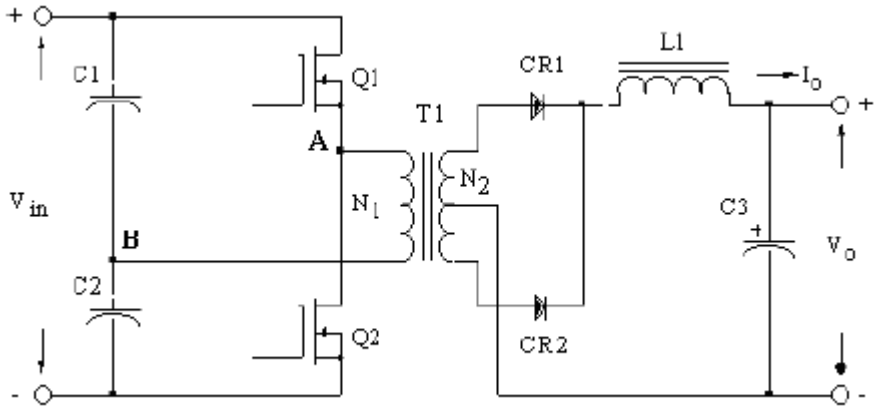


Figure 3.1 Power Stage of Half Bridge Converter

As shown in Figure 3.1, first the DC input is converter into the two equal half, by series connection of two capacitor C1 & C2.

In the first half of the cycle, Q1 is made ON. The voltage across capacitor C1, which is the half of the total DC input, is connected to the transformer. When Q1 is ON, Point A of the transformer is positive with respect to point B.

In the next half of the cycle, Q2 is made ON. The Transformer is connected to the voltage across C2. During this half of the operation positive point of capacitor C2 is connected to point B of the transformer, and point A of the transformer is connected to the negative terminal of capacitor C2 via switch Q2. The applied voltage across transformer is in the direction opposite to the direction of applied voltage in the first half. In the topology also transfer flux is balanced by bidirectional pulse voltage appearing to across the transformer.

3.2 Design of power stage of Half Bridge Converter:

3.2.1 Selection of input bridge capacitors:

Input Capacitors are connected in series as show in Figure 3.1. Selection of these capacitors can be made as follows: -

$$½ * C * V^2 = P_o * T_{on}$$

$$½ * C * (V_{max} – V_{min}) = P_o * T_{on}$$

Now,

$V_{MAX} = 40/2 = 20V$

$V_{MIN} = 19$

$P_o = 120$ W

$T_{on} = 5$ µs

Solving,

$C = 30.76$ µF

Selected capacitors are solid tantalum CT79-68 µF/100 V

3.2.2 Design of main Transformer:

Ferrites are the best core material choice for frequency from 10 KHz to 50 MHz because of several advantages over other types of magnetic material as high electrical resistivity, low eddy current losses, low cost, high stability and lowest volume. The half bridge converter allows flux excursion in the first and third quadrants of the B-H curve. This has the effect of making core loss consideration the limiting factor in B_{MAX} choice instead of the possibility of saturation. A good material for core loss at 100 KHz and saturation is VITROPERM 500F. In this design with 100 KHz switching frequency, limiting the core losses to an acceptable level allows the flux to operate at a maximum flux level (B_{MAX}) of 0.15 T (3000 G).

(a) Optimum Core size determination:

Knowing $\Delta B = 0.2$ Tesla and taking winding factor K=0.4, overall size of the core can be determined with following formula:-

$$P_o = (V_O + V_{RL} + V_D) * I_o$$

$V_O = 28V$

$V_{RL} = 10\%$ of $V_O = 2.8V$

$V_D = 1.5V$

Solving,

Po = 132.43 W

Now,

$$A_p = \frac{P_o\sqrt{2+(1/\eta)}}{4KJB_{\max}F}$$

$P_o = 132.43$ W

$J = 3.94A/mm^2$

$B_{MAX} = 0.2$ T

F = 100 KHz

K = 0.4

η= 0.8

Solving,

$A_P = 0.2798\ cm^4$

From datasheet of VITROPERM cores, W376 core is selected with $A_P = 0.48\ cm^4$

Where $A_P = Wa * Ac = 0.8 * 0.6 = 0.48\ cm^4$

(b) Computation of number of turns:

The number of turns on primary and secondary side is computed as:

$$N_p = \frac{V_{in} * 10^8}{4fA_cB_{\max}}$$

$$N_p = 5turns$$

$N_S = n*N_P$

$n = V_O / (2*D_{MAX})*V_{MIN}$

Solving, n = 1.61

So, Ns = 1.61 * 5 = 9 turns

(c) Wire Gauge Selection:

The wire size is selected to handle the secondary and primary current.

$$I_{\sec} = I_o\sqrt{D_{\max}}$$

$$I_{\sec} = 2.899A$$

$$I_{pri} = nI_o = 6.6A$$

Let a1= wire crossection of primary wire

& a2= wire crossection of secondary wire

Now, a1 = I_{PRIM}/J = 6.6/3.94 = 0.0167 cm^2

& a2 = I_{SEC}/J = 2.899/3.94 = 0.0076 cm^2

The litz wire is particularly suitable at high frequencies because of lower a.c resistance values. This is because Litz wire is a wire braid made up of very small diameter wires whose combined areas add up to the wire gauge desired. The smaller wires give the current flow a much greater surface area to flow within, thus lowering the current density and hence the a.c. resistance. Knowing the rule of thumb for current density as 250-750 circular mil/ampere for safe operation, 250/40 Litz wire is selected foe both primary and secondary windings.

3.2.3 Output filter choke design:

Typically the RMS o/p ripple current is less than 15% I_{DC}, or 0.9 A in this case. Delta I, the peak-to-peak ripple therefore is twice the RMS, or 1.8 Amps. The inductor loop equation during T_{OFF} can be written as:

$$V_L = V_o + V_D = \frac{L_o \Delta I_L}{T_{off}}$$

$$L = \frac{(V_o + V_D)T_{off}}{\Delta I_L}$$

Now, V_O = 28V

V_D = 0.6 V

T_{OFF} = 5 μs

ΔI_L = 1.78

Solving,

L = 80 μH

The core size selected here is 55929 core (μ = 147 and AL = 185 mH/1000 turns). Hence the number of turns required to obtain the above inductance can be calculated as:
The largest feasible wire size is decided, based on 15% winding factor is 350/40-litz wire.
K = Aw * N/W

$$N = \sqrt{\frac{1000^2 * 80 * 10^{-6}}{185 * 10^{-6}}}$$

$$N = 20 turns$$

$$Aw = \frac{K * W}{N} = \frac{0.15 * 308000}{15} = 3080$$

Hence 350/40 litz wire with Aw= 3363.5 circular mils is selected.

3.2.4. Selection of output capacitor:

Assuming a ripple of 13 mV peak-to-peak, the minimum capacitance required is

$$C = \frac{\Delta I_L T}{8 * \Delta V_{p-p}}$$

$$C = 168 \mu F$$

CT79 120+68 = 188 μF is selected.

3.3 Design of Control circuit of Half Bridge Converter:

3.3.1 Programming IC1525:

The SG1525 IC is designed to operate an oscillator. The error amplifier is designed with 100 gain. The design of internal oscillator is done at 200 KHz to obtain 100 KHz pulse at the output pins. From the datasheet, oscillator frequency vs. Rt, Ct and dead time curves:

F_O = 200 KHz

R_T = 3K

C_T = 2000 pF

R_D = 10 Ω, D_{MAX} = 0.4,

T_{ON} = 4 μs, T_{OFF} = 6 μs,

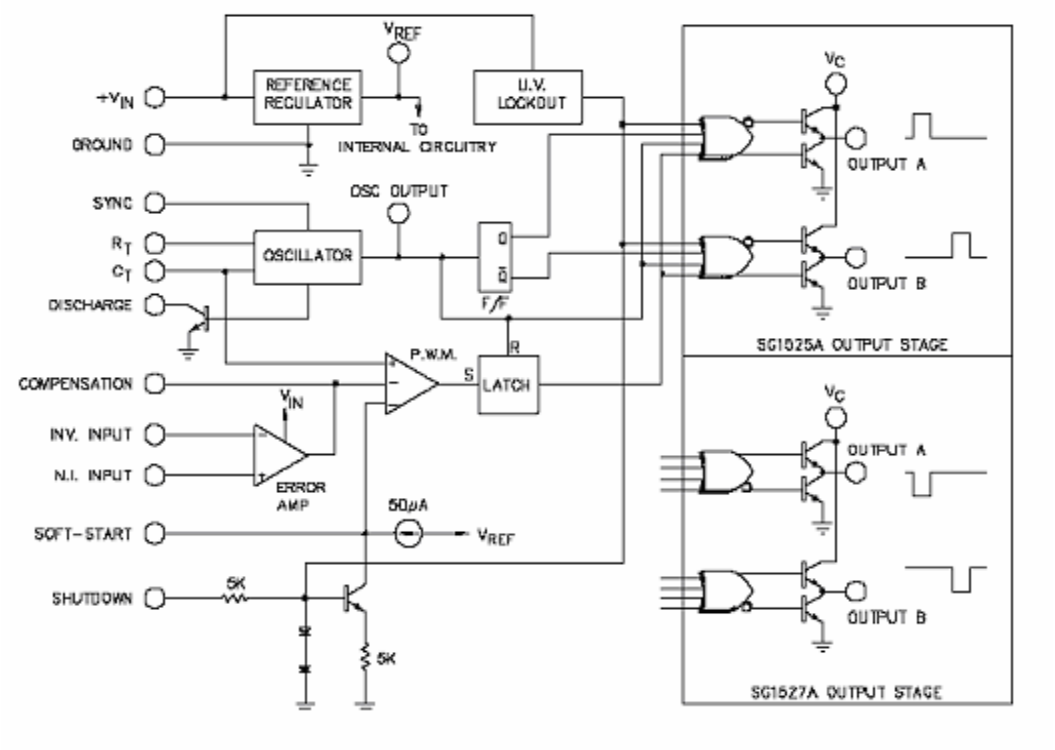


Figure 3.3.1 Block Diagram of SG1525 voltage mode control IC

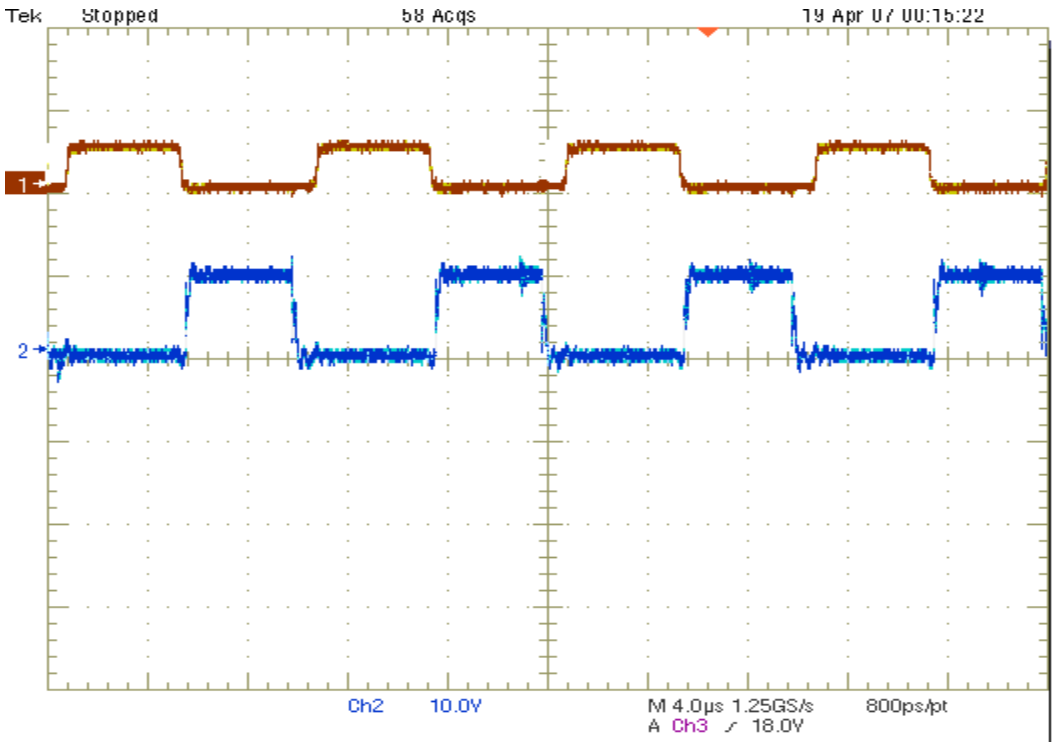


Figure 3.3.2 Gate Drive pulses of MOSFET of Half Bridge Converter

Output pulse as shown by channel 1 is the output pulse from gate drive transformer which is given to the floating switch and the output gate drive pulse of channel 2 is given to another nonfloating switch of Half Bridge Converter.

3.3.2 Gate Drive Selection:

As one of the switches in the Half Bridge converter is floating so the output of the IC1525 is given to gate drive transformer. Single – Ended transformer coupled Gate Drive approach is considered most suitable and hence followed in present design.

The Gate Drive Circuit design progresses in two stages as:

(a) Calculation of the coupling capacitors:

The method to calculate the coupling capacitor values is based on the maximum allowable ripple voltage and the amount of charge passing through the capacitor in steady state operation. The ripple has two components: one is related to the total gate charge (Q_g) of the main MOSFET and a second component due to the current flowing in the pull down resistor (R_{GS}). The minimum capacitance to guarantee to stay below the targeted ripple voltage under all operating conditions can be found by determining the maximum of the above expression which corresponds to the maximum on-time of the switch.

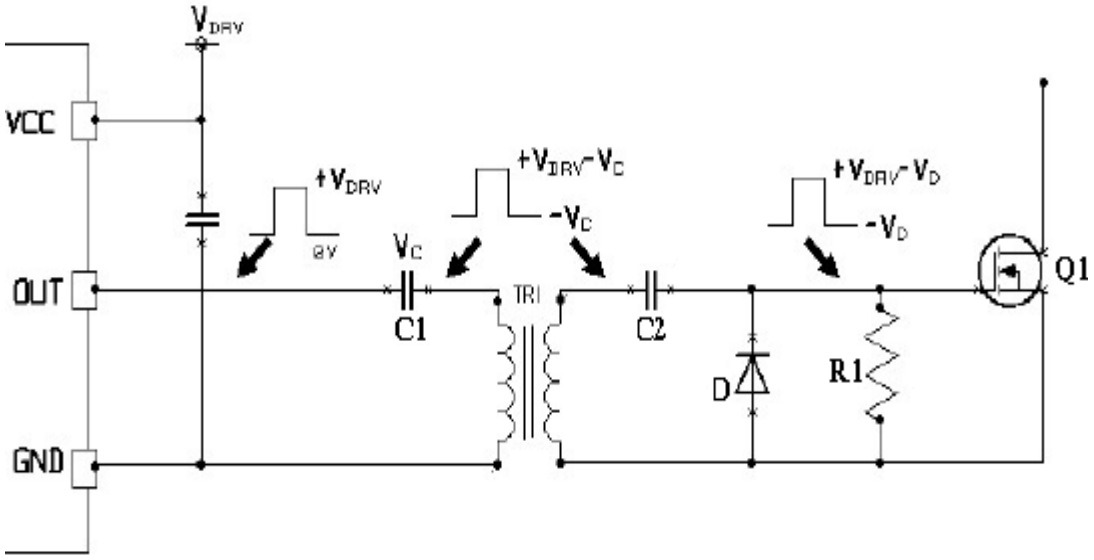
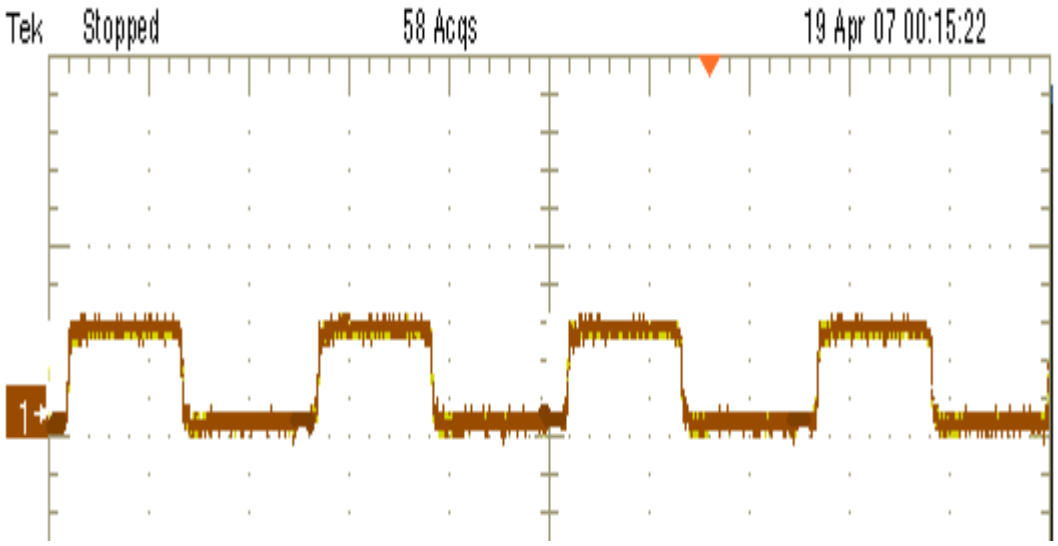


Figure 3.3.3 Gate drive Transformer

Output waveforms of this gate drive transformer observed in laboratory are as shown in figure 3.3.4.



Channel 1 20V

Figure 3.3.4 Output waveforms of Gate Drive Transformer

The expressions for the coupling capacitors on the primary and secondary side can be respectively written as:

$$C_{CP} = \frac{Q_G}{\Delta V_{CP}} + \frac{\left(V_{DRV} - V_D\right) D_{\max}}{\Delta V_{CP} R_{GS} F_{DRV}}$$

$$C_{CS} = \frac{Q_G}{\Delta V_{CS}} + \frac{\left(V_{DRV} - V_D\right) D_{\max}}{\Delta V_{CS} R_{GS} F_{DRV}}$$

C_{cp} is charged to maximum steady state voltage $V_{CP} = D_{MAX} * V_{DRV} = 0.5 * 12 = 6$ V

C_{cs} is charged to maximum steady state voltage $V_{CS} = V_{CP} - V_D = 6 - 0.5 = 5.5$ V

Assuming a ripple of 5% of the charging voltage, the ripple voltages on primary and secondary side can be computed as:

$\Delta V_{CP} = 5 * 6 / 100 = 0.30$V

$\Delta V_{CS} = 5 * 5.5/100 = 0.275$V

Hence the coupling capacitors can be calculated assuming the value of Gate pull down resistor R1 = 10K as shown in figure 3.3.3.

$C_{CP} = C1 = 300*10^{-9}/0.30 + (12-0.6) * 0.5 / (0.30 * 10 * 10^3 * 100 * 10^3) = 1\mu F$

$C_{CS} = C2 = 300*10^{-9}/0.275 + (12-0.6) * 0.5 /(0.275 * 10 * 10^3 * 100 * 10^3) = 1\mu F$

1 µF is selected as coupling capacitors on both primary and secondary side.

3.3.3 Gate Transformer Design:

The function of gate drive transformer is to transmit the ground referenced gate pulse across large potential differences to accommodate floating drive implementations. It handles low power but high peak currents to drive the gate of a power MOSFET and is driven by a variable pulse width as a function of the PWM duty ratio. Hence52403-1/2 F core is used in gate drive transformer design. The turns ratio is usually one. The number of turns on the primary winding can be calculated as:

$N_p = (12 * 5 * 100)/ (4000 * 0.013) = 115$ turns

$N_s/N_p = 1$

$N_s = 115$ turns

3.4. Breadboard model of Half Bridge Converter:

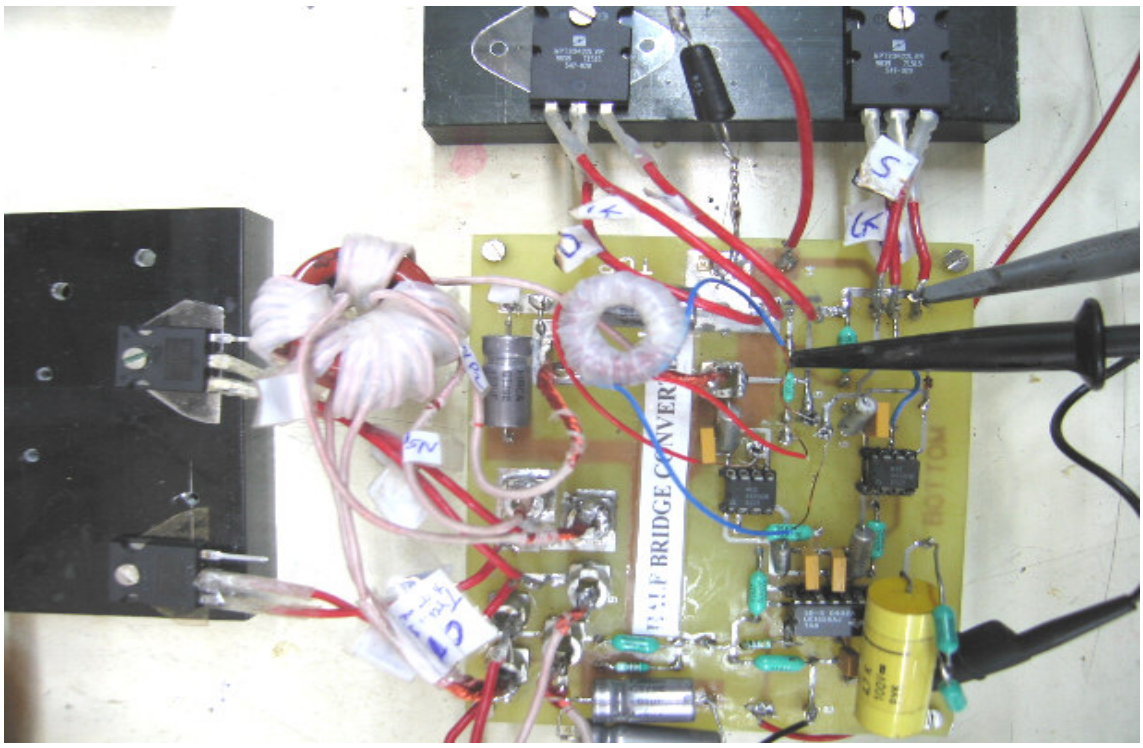


Figure 3.4 Picture of Breadboard model of Half Bridge Converter

3.5 Test Results:

Table 3.5 Test Results of Half bridge converter when connected with Boost preregulator

Boost Converter					Half Bridge Converter		
V_{IN}	I_{IN}	V_o	I_o	Eff (%)	V_o	I_o	Eff (%)
27.6	1.38	40.312	.88	93.13	26.393	1.319	91.98
29.655	1.28	40.324	0.908	96.45	26.278	1.313	94.23
31.733	1.196	40.333	0.908	96.49	26.30	1.315	94.44
33.71	1.124	40.336	0.912	97	26.316	1.315	94.07
35.746	1.056	40.337	0.912	97.45	26.324	1.316	94.16
37.641	1.004	40.339	0.912	97.34	26.331	1.316	94.18
39.431	0.956	40.340	0.912	97.59	26.347	1.317	94.316
40.403	0.940	40.48	0.912	98	26.456	1.322	94

3.6 Schematic of Half Bridge converter:

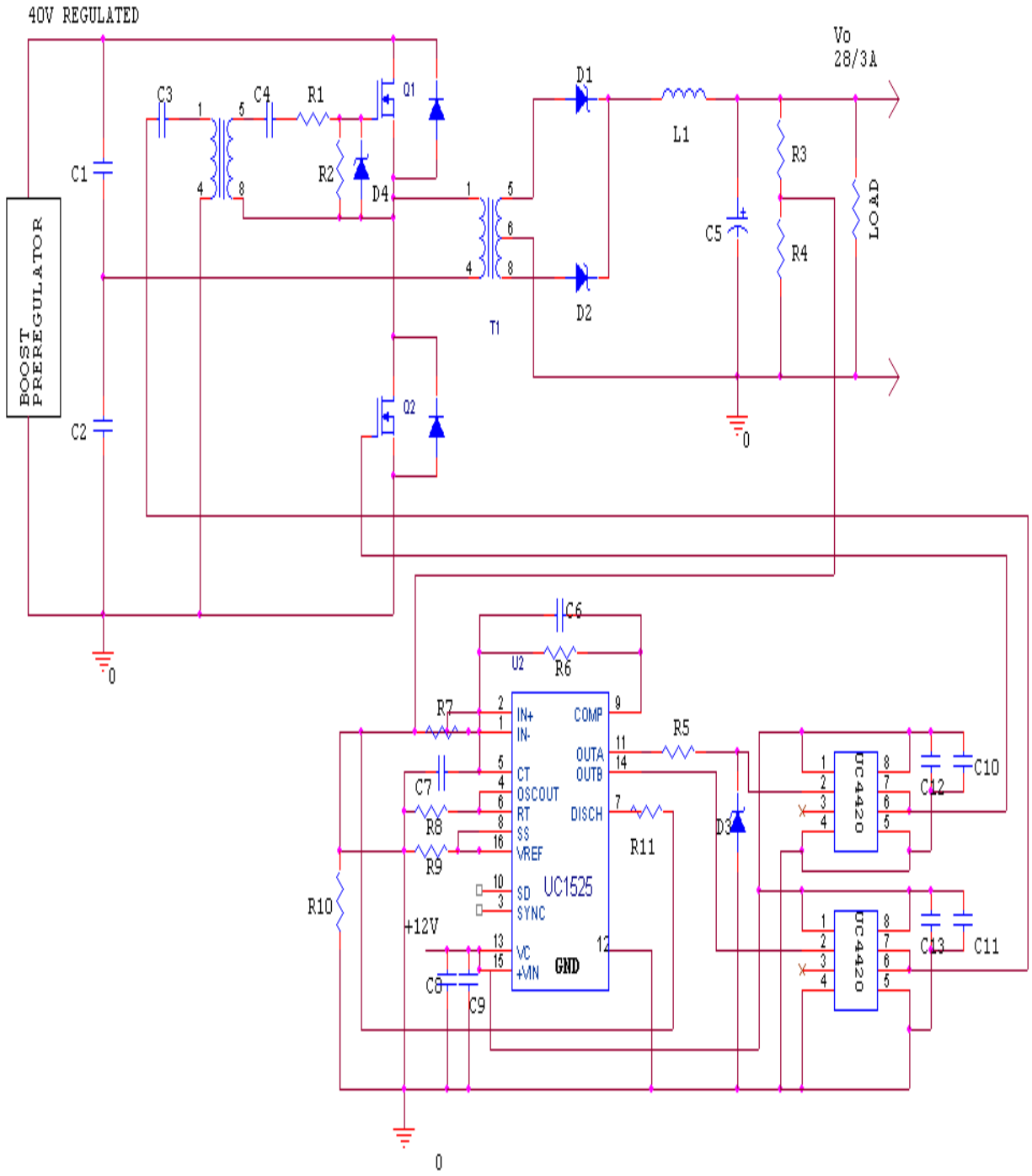


Figure 3.6 Schematic of Half Bridge Converter

Table 3.6 List of components of Half Bridge Schematic:

Serial no	Components	Description	Value
1	R1	Metal film oxide	10 Ω,1/4W
2	R2	Metal film oxide	10 KΩ,1/4W
3	R3	Metal film oxide	4.7 KΩ,1/4W
4	R4	Metal film oxide	56 KΩ,1/4W
5	R5	Metal film oxide	1.5 KΩ,1/4W
6	R6	Metal film oxide	100 KΩ,1/4W
7	R7	Metal film oxide	1 KΩ,1/4W
8	R8	Metal film oxide	3 KΩ,1/4W
9	R9	Metal film oxide	10 KΩ,1/4W
10	R10	Metal film oxide	10 KΩ,1/4W
11	R11	Metal film oxide	10Ω,1/4W
12	C1	Tantalum (CLR)	68 µF,100V
13	C2	Tantalum (CLR)	68 µF,100V
14	C3	Ceramic(CKR06)	0.82 µF,25V
15	C4	Ceramic (CKR06)	0.82 µF,25V
16	C5	Tantalum (CLR)	188 µF,100V
17	C6	Ceramic (CKR06)	4.7 µF,25V
18	C7	Ceramic (CKR06)	2.1 µF,25V
19	C8	Ceramic (CKR06)	0.1µF,25V
20	C9	Ceramic (CKR06)	1µF,25V
21	C10	Ceramic (CKR06)	0.1µF,25V
22	C11	Ceramic (CKR06)	1µF,25V
23	C12	Ceramic (CKR06)	0.1µF,25V
24	C13	Ceramic (CKR06)	1µF,25V
25	L1	Ceramic (CKR06)	33 µH
26	D1	(SCHOTKY)	HFA50PA60C/600V
27	D2	(SCHOTKY)	HFA50PA60C/600V
28	D3	Zener	10V
29	D4	Zener	10V
31	Q1, Q2	APT20M22LVR	200V/100A

3.7 Pragmatic waveforms:

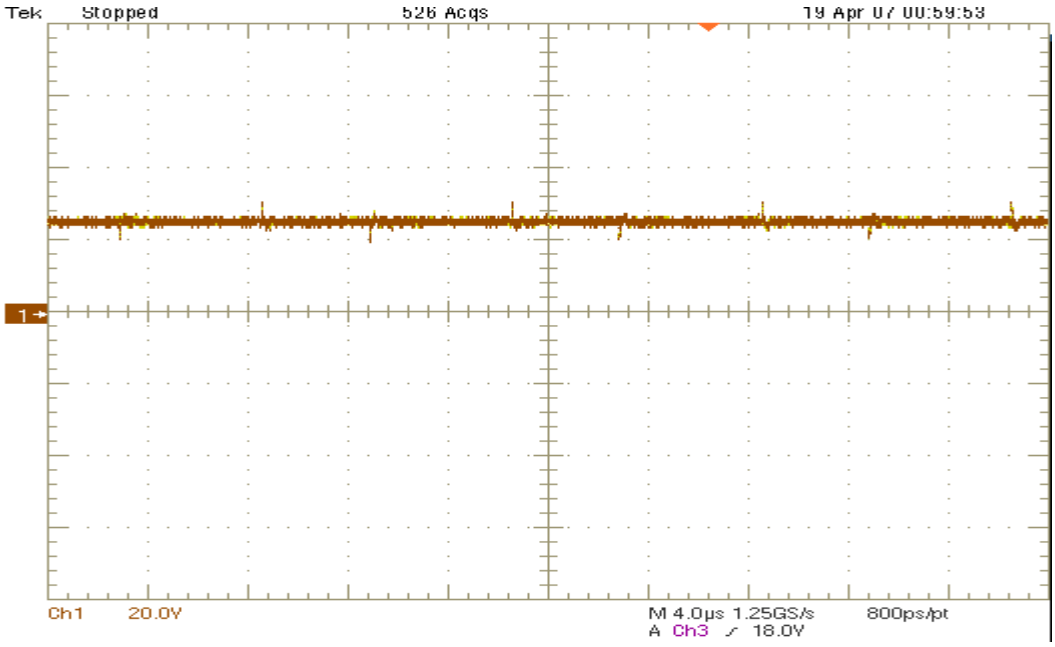


Figure 3.7.1 output voltage of Half Bridge Converter at V_{IN}=26V to 44V

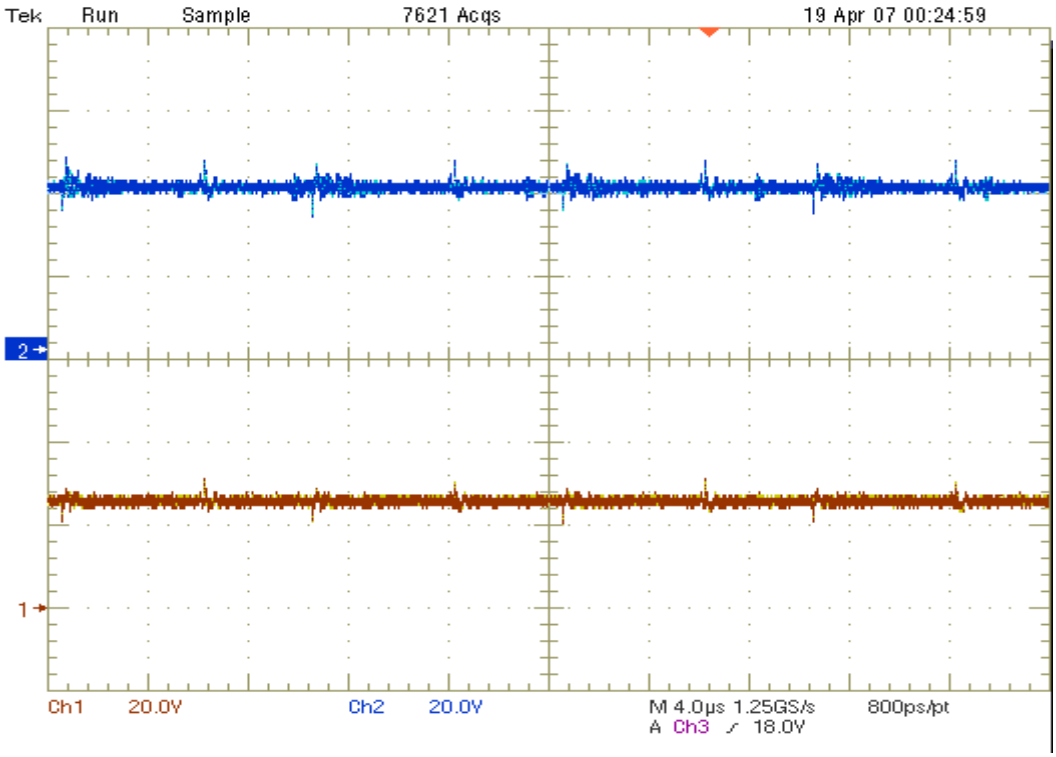


Figure 3.7.2 Output voltage waveform of Boost converter and Half Bridge Converter At Vin = 26V to 44V

3.8 Breadboard model of complete setup in laboratory:

Figure 3.8 Breadboard model of complete laboratory setup

CONCLUSION

The developed converter has 94% efficiency at 75W output power and 1% line regulation. The ZVT circuit implementation in conventional Boost Converter connected as preregulator to Half Bridge Converter reduces switching and conduction losses and this approach is a promising technology for designing high efficiency power converters with higher power output. Also the spikes and the noise associated with switching environment of power converter are mitigated because of connecting ZVT Boost preregulator.

This power converter when connected with telemetry circuit can be used as an Electronic Power Conditioner for supplying regulated 28V/3A DC to Gallium Arsenide FETs of power amplifier used in space applications.

FUTURE SCOPE

It can be designed further for 420W power output by changing PCB layout considering higher DC current and can be used for 100W UHF power amplifier. This EPC can be extended for multiple outputs by changing the design of main transformer of Half Bridge Converter.

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[4] www.microsemi.com

[5] www.fairchild.com

[6] www.ridleyengineering.com

[7] www.datasheetcatalog.com

- **Datasheets of ICs used:**

[1] UC1846

[2] SG1525

[3] UC4420

[4] CD4098

[5] 4093

- **Datasheets of Components used:**

[1] 45CKQ100 (Schottky diode)

[2] APT20M22LVFR (MOSFET)

[3] HFA50PA60C (Schottky diode)