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Development and Implementation of IP Core of PSK Modulator

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Abstract-- Digital Modulation techniques are essential to many digital communication systems, whether it is a telephone system, a mobile cellular communication system, or a satellite communication system. Several modulation techniques for digital transmission have recently been investigated for the purpose of achieving narrow signal spectra with power concentrated within a given bandwidth. While designing a communication system, particularly a satellite communication system, special attention is needed to use the primary resources viz., the transmitted power and channel bandwidth. Space communication links is power limited. Phase Shift Keying (PSK) modulation scheme is best suited for satellite communication since power required is optimum. This paper covers all the design and implementation details of the BPSK and QPSK Modulator. The MATLAB modeling of BPSK and QPSK Modulator is performed to help the VHDL part design. The Register Transfer Level (RTL) Design of the PSK Modulator is performed using VHDL. Test Bench is developed to simulate the IP Core. The simulation result of BPSK and QPSK Modulator using MATLAB Simulink Tool Box, MATLAB coding and VHDL coding are analysised and discussed. This IP
Core is implemented on XCV1000bg-6 Virtex FPGA. In addition, simulation results of VHDL Model are compared with output captured on Chipscope and Logic analyzer.

Keywords:
PSK, BPSK, QPSK, RTL, VHDL, MATLAB

I. INTRODUCTION

PSK is a digital Phase Modulation Techniques (PM) in which the information of the digital signal is transmitted in the phase of the modulated carrier. Phase modulation systems for transmission of digital signals show more resemblance to Amplitude Modulation (AM) systems than to digital Frequency modulation (FM), as opposed to analog systems where PM shows more resemblance to FM systems.

In PSK, the phase angle of the carrier is switched between two values in response to binary data. In PSK, the carrier signal is switched (keyed) between 0^o and 180^o phase states, depending on the binary data logic level 0 or 1. This is expressed as,

$$s_1(t) = A \cos 2\pi f_c t \quad \text{for logic 1} \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$s_1(t) = A \cos(2\pi f_c t + 180°)$$

$$= - A\cos 2\pi f_c t \quad \text{for data logic `0'} \ldots\ldots\ldots\ldots (2)$$

PSK signal can be generated by multiplying the input bipolar date b(t) with carrier signal. It is expressed as,

$$s_1(t) = b(t) * A \cos 2\pi f_c t \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where, b(t) represents a synchronous random binary baseband signal having a bit rate $R_b = \frac{1}{T_b}$ and levels -1 and +1. For equiprobable NRZ baseband signals time domain multiplication is equivalent to double sideband suppressed carrier amplitude modulation (DSB-SC-AM). Generation of BPSK is same as that of DSB-SC. Input bipolar data and carrier signal is multiplied using balanced ring modulator.

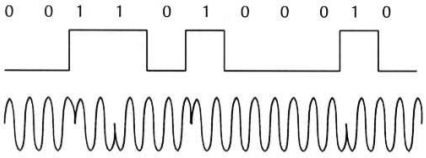

Figure1. Waveform of the PSK

BPSK (also sometimes called PRK, Phase Reversal Keying) is the simplest form of PSK. It uses two phases which are separated by 180° and so can also be termed 2-PSK. Binary data are represented by two signals with different phases in BPSK. Typically these two phases are 0 and π, the signals are defined as,

$$s_1(t) = A \cos 2\pi f_c t, \quad 0 \le t \le T, \text{ for 1} \ldots\ldots\ldots (4)$$

$$s_2(t) = -A \cos 2\pi f_c t, \quad 0 \le t \le T, \text{ for 0} \ldots\ldots (5)$$

However, in order to achieve the same bit-error probability as BPSK, QPSK uses twice the power (since two bits are transmitted simultaneously). Sometimes known as quaternary or quadriphase PSK, 4-PSK. QPSK uses four points on the constellation diagram, equispaced around a circle. With four phases, QPSK can encode two bits per symbol, shown in the diagram with Gray coding to minimize the BER twice the rate of BPSK. Analysis shows that this may be used either to double the data rate compared to a BPSK system while maintaining the bandwidth of the signal or to maintain the data-rate of BPSK but halve the bandwidth needed. Since QPSK is a special case of MPSK, its signals are defined as

$$s_i(t) = A\cos(2\pi f_c t + \theta_i), \ 0 \le t \le T, \ i = 1, 2, 3, 4 \ldots\ldots\ldots (6)$$

where $\theta_i = (2_i - 1)\pi/4$. The initial signal phases are $\pi/4$, $3\pi/4$, $5\pi/4$, $7\pi/4$. The carrier frequency is chosen as an integer multiple of the symbol rate, therefore in any symbol interval

[kT, (k+1)T], the signal initial phase is also one of the four phases.

The rest of the paper is organized as follows. Section 2 details of the MATLAB Modeling of BPSK and QPSK Modulator. It also consists of simulation results of the same. The IP Core design of BPSK and QPSK and simulation results of the same are presented in section 3. Finally, we close with conclusions.

II. MATLAB Modeling

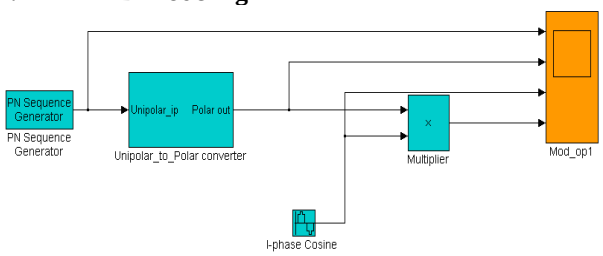

Figure 2: Model of BPSK Modulator using Simulink Toolbox.

The Implementation of BPSK Modulator using Simulink Toolbox of MATLAB is shown in Figure 2. It basically consists of PN Sequence Generator, Unipolar to Polar Converter, Cosine carrier source and Multiplier. From Figure 3 we can observed that carrier signal is phase shifted of 0° for binary input 1 and 180° for binary input 0.

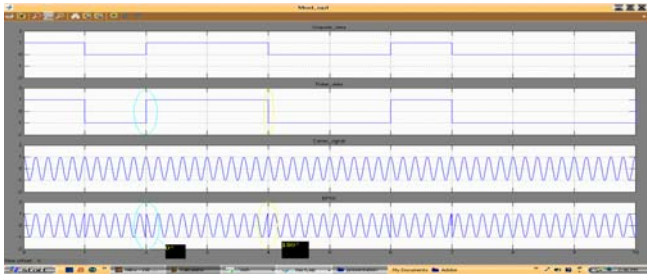

Figure 3: Simulation Result of BPSK

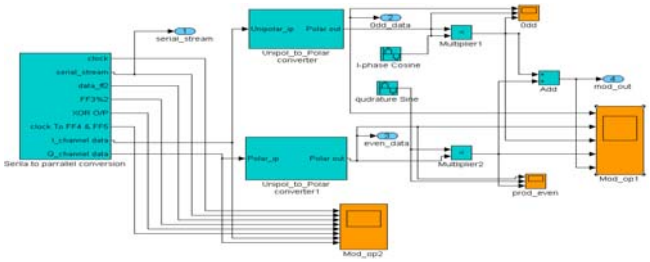

Figure 4: Model of QPSK Modulator using Simulink Toolbox.

The Implementation of QPSK Modulator using Simulink Toolbox of MATLAB is shown in Figure 4. The digital symbol outputs of the bit splitter are fed to the Unipolar to Polar conversion block, which converts unipolar NRZ data to polar NRZ data. The odd numbers bits are represented as in-phase data (I-channel) and even numbers bits are represented as quadrature data (Q-channel). I-channel data bits are multiplied with carrier signal and q-channel data bits are multiplied with 90° phase shifted carrier signal. The I channel modulated signal and Q channel modulated signal is shown in Figure 5. The output from multiplier of both channel are added by an adder. This adder will produce QPSK signal which is shown in Figure 5.

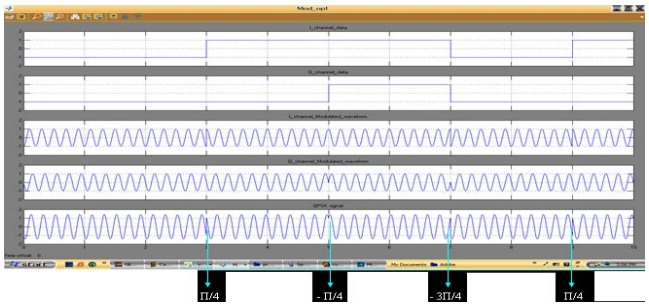

Figure 5. Simulation Result of QPSK

III Overview of IP Core of PSK Modulator

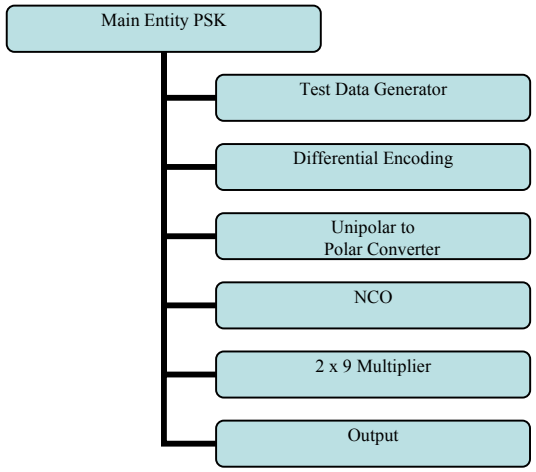

Figure 6 : Overview of IP Core of PSK Modulator

An overview of IP Core of PSK Modulator is shown in Figure 6. The main components of it are Test Data Generator, Differential Encoder, Unipolar to Polar Converter, NCO (Numerical Controlled Oscillator) and 2 x 9 Multiplier. Each Module is separately designed and optimized. . The basic theory of each module is studied and discussed in brief in the report. The main components of PSK Modulator are NCO and Signed Multiplier. The main feature of this IP core is that NCO is designed to generate Sine and Cosine carrier signal using the same LUT which stores 9 bit quantized value of 0° to 90° of sinusoidal wave. Different algorithms of Multiplier are studied and compared. Finally Signed Multiplier report is developed using * operator supported by VHDL. At last, all modules are integrated and complete IP Core of PSK Modulator is developed. This IP Core is implemented on

XCV1000bg560-6 FPGA. It is also verified by comparing output on I/O pins of FPGA using Logic Analyzer with the Test Bench simulation result obtained on Modelsim Simulator. This IP can work as BPSK or QPSK Modulator according to selection given by control bit. The selection of operation of IP Core is summarized in below Table.

Control Bit	Operation
control (0)=0	External Data
control (0)=1	Internal Data
control (1)=0	BPSK Modulation
control (1)=1	QPSK Modulation
control (2)=0	Differential Encoding off
control (2)=1	Differential Encoding on

Figure 7 shows Test Bench simulation result of IP core as BPSK Modulator observed on Modelsim Simulator. As shown in Figure 7 input data for i channel is generated using test bench and applied to input of the BPSK Modulator. Control (2)=1 is given to differential encoding of input data. Here control (1)=0 is given so IP Core will work as BPSK Modulator and control(0)=1 is given so Modulator will take test data generated by IP Core itself as shown in Figure 7.

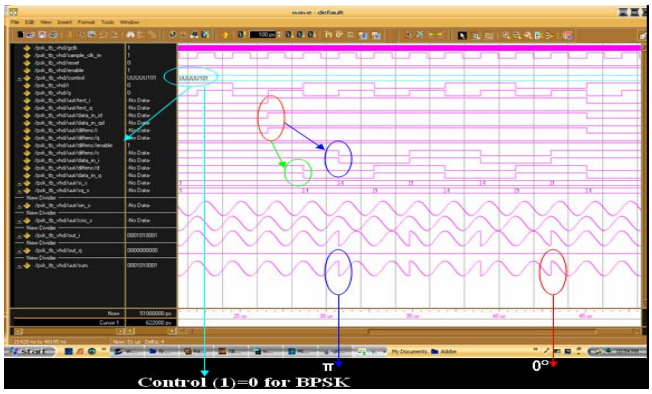

Figure 7 : Simulation Result of IP Core as BPSK

Figure 8 shows Test Bench simulation result of IP Core as QPSK Modulator observed on Modelsim Simulator. As shown in Figure 8 input data for i and q channels are generated form Test Bench and applied to input of QPSK Modulator. Control (2) = 0 is given to off differential encoding. Here control (1) = 1 is given so IP Core will work as QPSK and control (0)=1 is generated so QPSK Modulator will take test data generated by IP Core itself as shown in Figure 8.

Figure 8: Simulation of IP Core as QPSK

IV Conclusion:

The MATLAB modeling using Simulink toolbox is prepared for both BPSK and QPSK Modulator. VHDL coding of PSK Modulator is developed. The Design strategy has been decided for generic programming. This work provides a complete code in VHDL and functional for a BPSK/QPSK Modulator. The simulation results are shown for each component and complete IP Core. Test Bench is developed to simulate the IP Core. This Test Bench is developed with text I/O feature of VHDL to capture output values. This IP Core is implemented on Xilinx XCV1000bg 560-6 FPGA. At last, output of IP Core is verified using Logic Analyzer. The output of IP Core is also compared with the output obtained on Modelsim simulator during simulation of VHDL Code.

V. References:

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