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Design & Simulation of 1.8-V 2-Bit CMOS Flash ADC in 0.35µm

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***Abstract*--CMOS VLSI is progressing at fast rate for decades and dominating most of markets in digital circuit areas. The design and optimization of a high-speed low-voltage CMOS flash analog-to-digital converter (ADC) are presented in this paper. This paper describes a 2-bit Flash Analog to digital converter (ADC) implemented in 0.35 µm CMOS TSMC technology. Basic blocks of Flash ADC, comparator, encoder have been implemented. The used analog power supply is only 1.8 V. Power dissipation of the implemented ADC is 2.79mw. and total active area 0.0456 mm^2 Simulation result of each block as well as each stage is presented.**

***Key words*—Analog-to-digital converter (ADC), flash, low voltage.**

I INTRODUCTION

HIGH-SPEED analog-to-digital converters (ADC) are an essential part in a signal processing system. Analog-to-digital (A/D) and digital-to-analog (D/A) converters provide the link between the analog world of transducers and the digital world of signal processing, video, wideband communication or other fast signals in optical storage, computing, digital data collection, data storage.

Flash analog-to-digital converters also known as parallel ADCs are the fastest way to convert an analog signal into a digital signal. It is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors. Flash ADCs are ideal for the applications requiring large bandwidth however they typically consume more power than other ADC architectures and are limited to 8-bits resolution. Flash ADC advantages include: Very high speed, most efficient and provides proportional response.

II ARCHITECTURE

For an "N" bit converter, the circuit employs 2^N-1 comparators. A resistive divider with 2N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0".

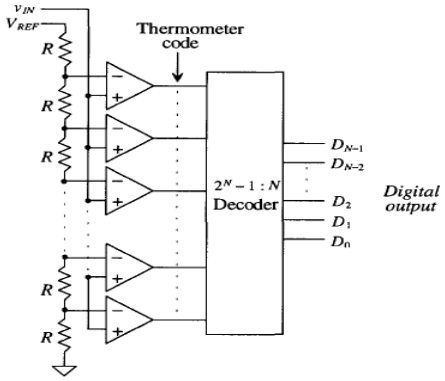

Fig.1 Architecture of N-bit Flash ADC

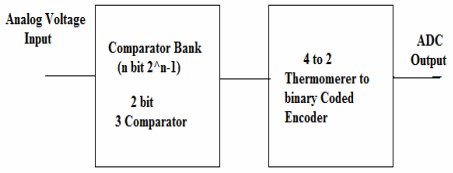

Fig.2 Block Diagram of ADC

Flash consist of bank of comparators and binary to gray coded encoder.

III COMPARATOR

In high-speed analog-to-digital converters, comparator design has a crucial influence on the overall performance that can be achieved. Converter architectures that incorporate a large number of comparators in parallel to obtain a high throughput rate impose stringent constraints on the delay, resolution, power dissipation, input voltage range, input impedance, and area of those circuits.

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator is widely used in the process of converting analog signals to digital signals. The sampled signal during the analog to digital conversion process is applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit ADC.

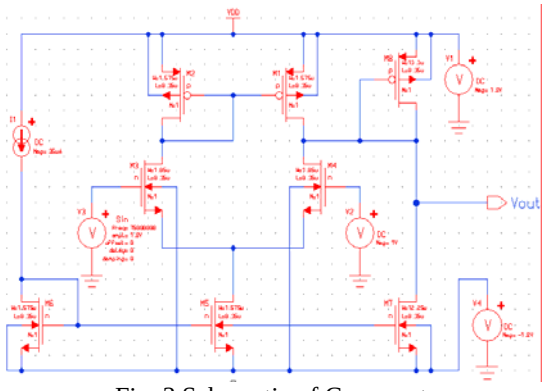

Fig. 3 Schematic of Comparator

IV Prelayout Simulation of Comparator

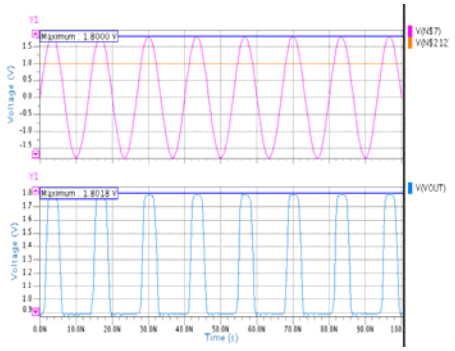

Fig.4 Transient Response of Comparator

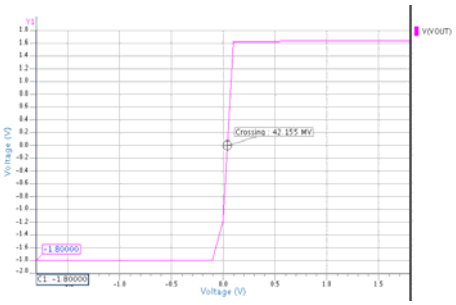

Fig.5 Offset of Comparator

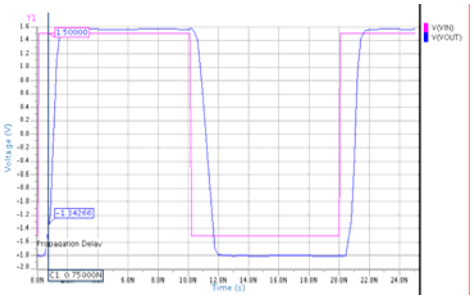

Fig. 6 Propagation Delay of Comparator

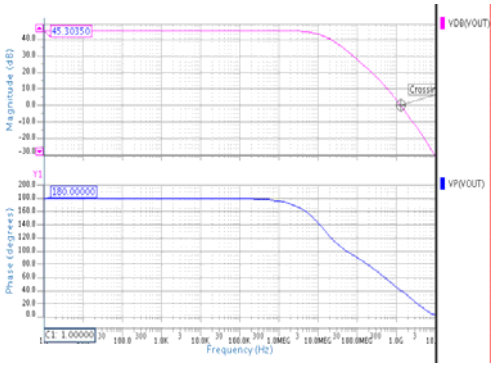

Fig.7 Frequency Responses of Comparator

V Encoder

The encoder is particularly for high speed and high resolution flash analog-to-digital converters. Here we used thermometer to binary coded encoder. Thermometer code, or base one, is numerical base system named because it works similarly to a thermometer.

Thermometer name is so called because it is similar to a mercury thermometer, where the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code.

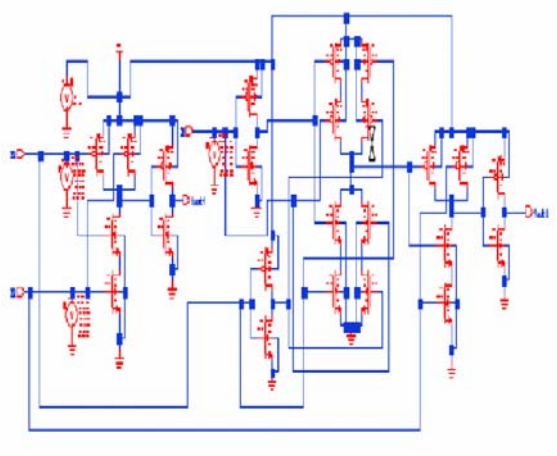

Fig. 8 Schematic of Encoder

VI Prelayout Simulation of Encoder

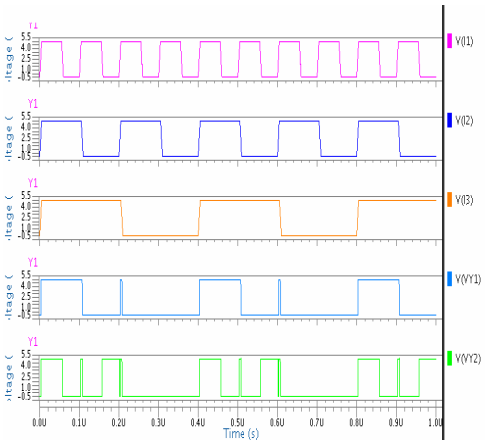

Fig. 9 Waveform of Encoder

VI FLASH ADC

Table 1 Specification of Flash ADC

Resolution	2-bit
Architecture	Flash
Power Supply	1.8V
Technology	0.35µm

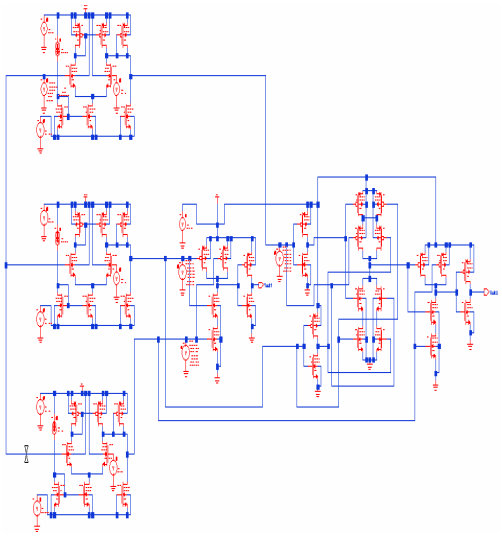

Fig. 10 Schematic of 2-bit Flash ADC

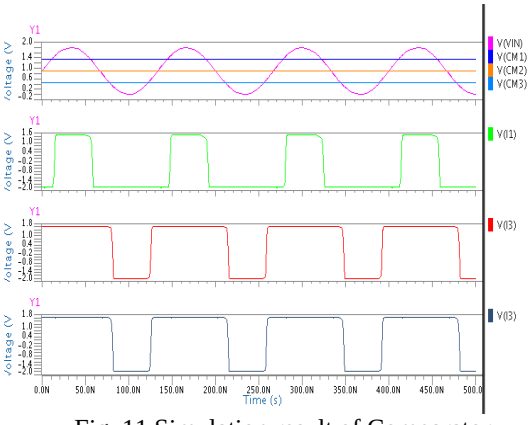

Fig. 11 Simulation result of Comparator

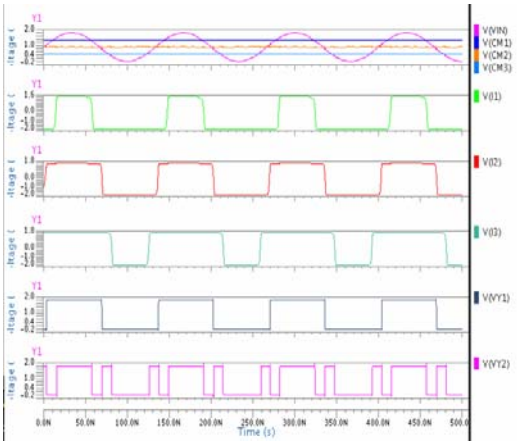

Fig. 12 Simulation result of 2-bit Flash ADC

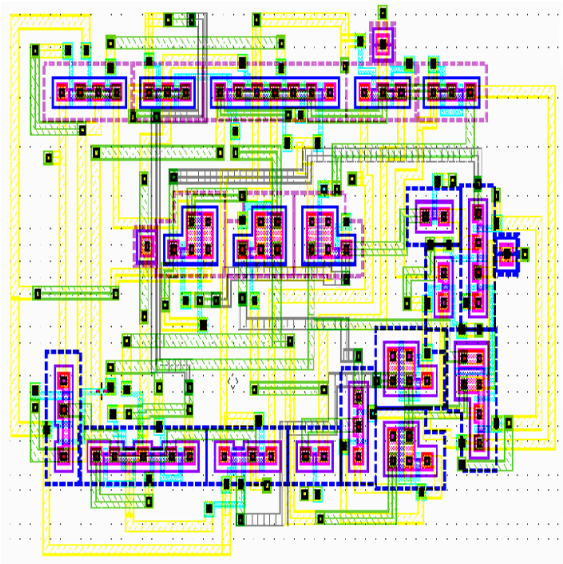

Fig. 13 Layout of the Flash ADC

VII CONCLUSION

In this project, low voltage 2-bit flash ADC is presented. Comparator and encoder architecture suitable for flash ADC applications are also presented. All the designs have been simulated with 0.35u technology. All the simulations have been carried out in the Mentor Graphics tool. The overall power dissipation comeing out is also very low.

This 2-bit low voltage flash ADC project can be extended depending upon the applications. Low voltage design is also useful in the higher density circuits.

Table 2 Summary of 2-bit CMOS Flash ADC design in 0.35µ technology

No.		Parameters	Simulation Results
1	Flash ADC	Resolution	2-bit
		Propagation Delay	4.91ns
		Power Dissipation	2.7962E-03W
1.1	Comparator	Offset	42.15mv
		Gain	45.3dB
		Power dissipation	1.6806E-04W
		Propagation Delay	0.75ns
1.2	Encoder	Power dissipation	2.9990E-09W

VIII REFERENCES

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