"DESIGN AND IMPLEMENTATION OF THREE LEVEL INVERTER USING DSP"

Major Project Report

Submitted in Partial Fulfillment of the Requirements for the degree of

MASTER OF TECHNOLOGY

IN

ELECTRICAL ENGINEERING

(Power Apparatus & Systems)

By

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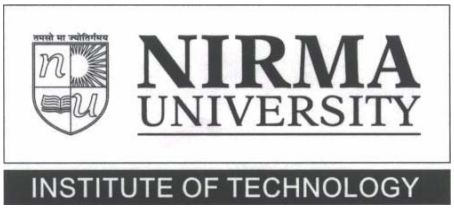

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CERTIFICATE

This is to certify that the Major Project Report entitled "Design and Implementation of Three-Level Inverter using DSP"submitted by Mr. Pinkalkumar Jashvantbhai Patel (06MEE011) towards the partial fulfillment of the requirements for the award of degree in Master of Technology (Electrical Engineering) in the field of Power Apparatus & Systems of Nirma University of Science and Technology is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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This is to certify that **Mr. Pinkalkumar J. Patel** (06MEE011), Student of M.TECH. Electrical Engineering (Power Apparatus & Systems) of Institute of Technology, Nirma University has done his project on **"Design and Implementation of Three Level inverter Using DSP"** at AMTECH ELECTRONICS (I) LIMITED, GANDHINAGAR, under the guidance of Mr. Vinod Patel (Manager, R&D) in the academic year 2007-2008.The duration of project work is 04-06-2007 to 26-04-2008.He had worked on his project sincerely and regularly.

We wish him all success in his future work.

For AMTECH ELECTRONICS (I) LIMITED,

Mr. VINOD PATEL
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Pinkal Patel

ABSTRACT

Three level voltage-fed inverters have gained importance in high power high performance industrial drive applications. Neutral point clamped (NPC) power topology mostly used for three-level inverter. Neutral point clamped (NPC) topology has problem of DC-link capacitor voltage balancing. It can be solved using self-balancing SVPWM scheme, and closed loop capacitor voltage balancing scheme.

The report explains different Multilevel Inverter topologies such as Neutral point clamped Inverter, Flying Capacitor Inverter, and H-Bridge Cascaded Inverter. Two modulation methods – Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM), used in Multilevel Inverters are explained in this report. The pulse based dead time compensation method for three-level inverter is also discussed in this thesis.

The PSIM simulation results of SPWM and SVPWM are included in this report. The Verification of SVPWM algorithm using PSIM Simulation, Code Composer Studio and R-C Low pass filter with DSP (TMS320F2811) Control Card are included in the report. This report includes experimental results of three-level inverter and two-level inverter for various conditions. Experimental results prove ability of self-balancing SVPWM scheme and pulse based dead time compensation scheme for stable operation. Finally, the THD analysis between three-level and two-level inverter are discussed in this report.

Index Terms: Neutral point clamped (NPC) Topology, Pulse Based Dead Time Compensation, SVPWM and Three-Level Inverter

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ABBREVIATION

PWM	:	Pulse Width Modulation
SVPWM	:	Space Vector Pulse Width Modulation
IGBT	:	Insulated Gate Bipolar Transistor
NPC	:	Neutral Point Clamped
DSP	:	Digital Signal Processor
NTV	:	Nearest Three Vectors
SPWM	:	Sinusoidal Pulse Width Modulation
SVM	:	Space Vector Modulation
MV	:	Medium Voltage
DLL	:	Dynamic Link Library
VSI	:	Voltage Source Inverter
TLI	:	Three-Level Inverter
EVA	:	Event Manager A
EVB	:	Event Manager B
THD	:	Total Harmonic Distortion
DTC	:	Dead Time Compensation
ADC	:	Analog to Digital Conversion
DAC	:	Digital to Analog Conversion
CCS	:	Code Composer Studio

NOMENCLATURE

k	:	No. of Steps in the voltage between two phases of the load
n	:	No. of voltage levels
Vdc	:	DC Link Voltage
V^*	:	Reference Voltage Vector
Vab	:	Output Line Voltage
Ia, Ib, Ic	:	Output Line Current
Vc1	:	Lower Capacitor Voltage
Vc2	:	Upper Capacitor Voltage
Δv_c	:	Change in Capacitor Voltage
T_{1p}	:	dwell time for Positive Small Stationary Vector
T_{1n}	:	dwell time for Negative Small Stationary Vector
Δt	:	incremental time interval
i_d	:	DC Link Current
ΔV_m	:	Maximum allowed DC voltage deviation
$d_{00\text{-}/+00}$	:	Duty Cycles for Stationary Vector
C	:	DC link Capacitance
R	:	Resistance
mi	:	Modulation index

CONTENTS

CHAPTER-1
INTRODUCTION

1.1 GENERAL

Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them. Three-level voltage fed PWM inverters is recently showing popularity for multi-megawatt industrial drive applications. The main reason for this popularity is that the output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion and large voltage between the series devices is easily shared. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently. This technique results in higher magnitude of fundamental output voltage available as compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states.

One of the advantages of multilevel inverters is that the voltage stress on each switching device is reduced [1]-[16]. In addition, multilevel waveforms feature have less harmonic content compared to two level waveforms operating at the same switching frequency.

In this chapter, scope of work, fundamental difference between two level, three level and n level inverter, basic block diagram, literature survey, and organization of thesis are discussed. In multilevel inverters, it is easy to reach high voltage levels in high power applications with lower harmonic distortion and switching frequency, which is very difficult to get this performance with conventional two level inverters.

1.2 SCOPE OF WORK

The multilevel inverter has wide scope in induction motor drive. A number of MV drive products are available on the market today. These drives come with different designs using various power converter topologies and control schemes. Each design offers some unique features but also has some limitations. The diversified offering

promotes the advancement in the drive technology and the market competition as well. A summary of the MV industrial drives is as follows [25].

TABLE-1.1
SUMMARY OF MV DRIVE PRODUCTS

Inverter Configuration	Switching Device	Power Range (MVA)	Manufacturer
Two-level voltage source inverter	IGBT	1.4 – 7.2	Alstom (VDM5000)
Three-level neutral point clamped inverter (NPC)	GCT	0.3 – 5	ABB (ACS1000)
		3 – 27	ABB (ACS6000)
		3 – 20	General Electric (Innovation Series MV-SP)
	IGBT	0.6 – 7.2	Siemens (SIMOVERT-MV)
		0.3 – 2.4	General Electric - Toshiba (Dura-Bilt5 MV)
Multilevel cascaded H-bridge inverter	IGBT	0.3 – 22	ASI Robicon (Perfect Harmony)
		0.5 – 6	Toshiba (TOSVERT-MV)
		0.45 – 7.5	General Electric (Innovation MV-GP Type H)
NPC/H-bridge inverter	IGBT	0.4 – 4.8	Toshiba (TOSVERT-300MV)
Flying-capacitor inverter	IGBT	0.3 – 8	Alstom (VDM6000 Symphony)
PWM current source inverter	Symmetrical GCT	0.2 – 20	Rockwell automation (Power Flex 7000)
Load commutated inverter	SCR	>10	Siemens (SIMOVERT S)
			ABB (LCI)
			Alstom (ALSPA SD7000)

PWM pulses produced by the three-level inverter have a voltage step height that is half that of ordinary two-level inverters. The lower ringing voltages in turn reduce surge voltage appearing at the motor terminals and common mode voltage that can produce pitting on motor shafts. The surge voltages are reduced in three level inverter compare to two-level inverter. So the motor insulation bearing life is increased in three-level inverters. Due to these advantages three-level inverter is also used in low voltage drive. Today in market Yaskawa G7 drive with three-level inverter is also available at low voltage and low power rating.

1.2.1 DRIVE APPLICATIONS

Industry	Application Examples
Petrochemical	Pipeline pumps, gas compressors, brine pumps, mixers/extruders, electrical submersible pumps, induced draft fans, boiler feed water pumps, water injection pumps.
Cement	Kiln-induced draft fans, forced draft fans, baghouse fans, preheat tower fans, raw mill induced draft fans, kiln gas fans, cooler exhaust fans, separator fans.
Mining and Metals	Slurry pumps, ventilation fans, de-scaling pumps, tandem belt conveyors, baghouse fans, cyclone feed pumps, crushers, rolling mills, hoists, coilers, winders.
Water/Wastewater	Raw sewage pumps, bio-roughing tower pumps, treatment pumps, freshwater pumps, storm water pumps.
Transportation	Propulsion for naval vessels, shuttle tankers, icebreakers, Cruisers. Traction drives for locomotives, light-track trains.
Electric Power	Feed water pumps, induced draft fans, forced draft fans, effluent pumps, compressors.
Forest Products	Induced draft fans, boiler-feed water pumps, pulpers, refiners, kiln drives, line shafts.
Miscellaneous	Wind tunnels, agitators, test stands, rubber mixers.

Three-Level inverter is not only used for low power and high power induction motor drives. It can be used for other applications also, which are given below.

Other applications of three-level inverter,

- Multi Megawatt synchronous motor drives for industrial applications
- Active harmonic filter
- Electrical Vehicles
- Static VAR compensation systems
- HVDC transmission system
- Applications in power conditioning systems for super conductive magnetic energy storage (SMES)

1.3 TWO-LEVEL, THREE-LEVEL AND N-LEVEL VOLTAGE SOURCE INVERTER (VSI)

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1.1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which an ideal switch with several represents the action of the power semiconductors positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor [see Fig. 1.1(a)], while the three-level inverter generates three voltages, and so on [1].

Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is,

$$k = 2m+1 \quad (1.1)$$

In 1980, early interest in three-level power conversion technology was triggered by the work of Nabae, et al., who introduced the neutral-point-clamped (NPC) inverter topology. It was immediately realized that this new inverter had many advantages over the more conventional two-level inverter. Subsequently, in the early nineties the concept

of the three-level inverter was extended further and some new multilevel topologies were proposed. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

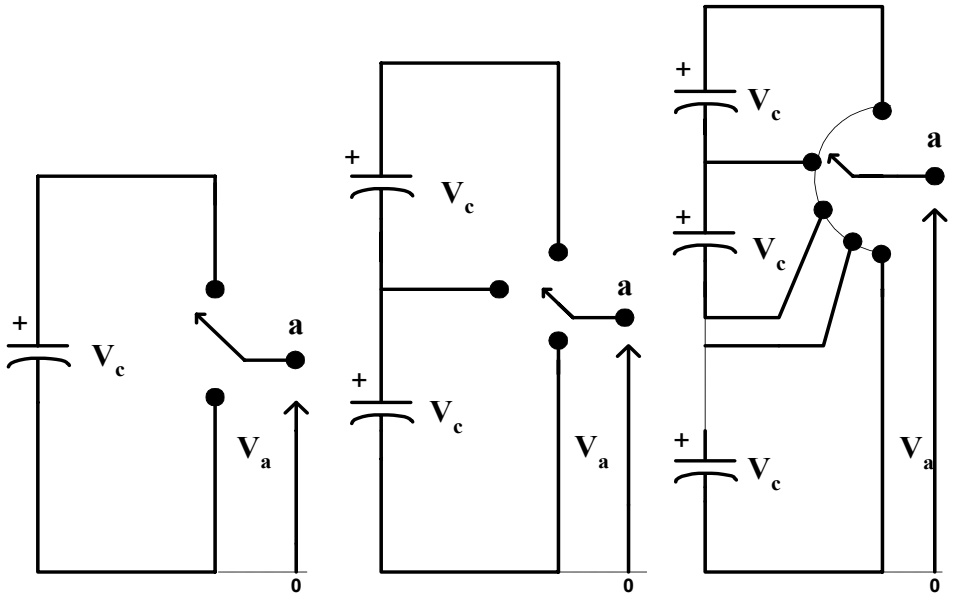


Fig.1.1 One phase leg of an inverter with (a) two level, (b) three level, and (c) n level

Advantages offered by the multilevel approach compared to two-level topology include [1]-[10].

- Draw input current with very low distortion
- Good power quality, due to greater availability of voltage levels
- Good electromagnetic compatibility (EMC)
- Low switching losses, as switching frequencies of the devices can be reduced
- Filters with smaller reactive components
- Ratings of the devices reduces
- Lower common-mode voltage
- Lower dV/dt

1.4 PERFORMANCE DIFFERENCE BETWEEN THREE-LEVEL AND TWO- LEVEL INVERTER

PWM pulses produced by the inverter have a voltage step height that is half that of ordinary two-level inverters. The lower ringing voltages in turn reduce surge voltage appearing at the motor terminals and common mode voltage that can produce pitting on motor shafts.

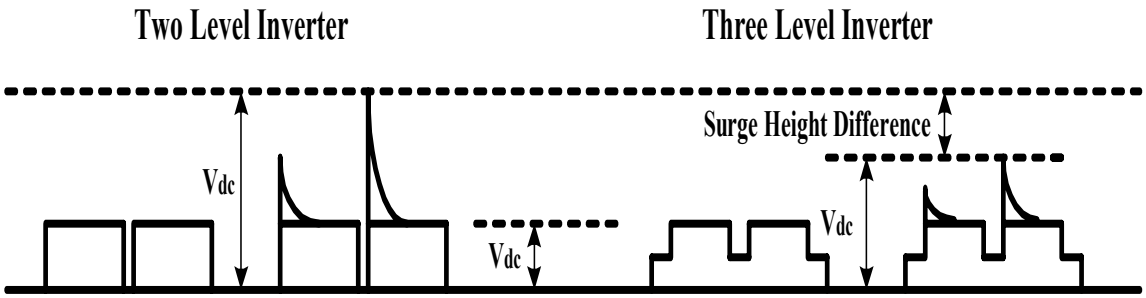


Fig.1.2 Surge voltage difference in two and three level inverters

A comparison of motor bearing life for three-level and two-level inverters illustrates the improvements that arise from the use of lower surge voltages as shown in fig.1.2 and fig.1.3. Recently a novel approach to IGBT switching has helped minimize surge voltage and bearing problems in an innovative way. The three-level inverter uses a circuit configuration consisting of 12 IGBTs and six additional clamp diodes instead of the usual six IGBTs with six diodes found in two-level inverters. The 12 IGBTs synthesize three dc bus levels (0, 300, and 600 Vdc) rather then the two (0 and 600 Vdc) that conventional two-level PWM converters employ. The resulting waveform more closely resembles a sinusoid than does the two-level pulse-width-modulated waveform.

Switching takes place in 300-Vdc steps compared to 600-Vdc steps in case of two level PWM drives. The reduction in the step size is instrumental in reducing common mode voltage level and hence the corresponding common mode current.

A smaller step size also reduces the probability of insulation breakdown. The amplitude of the surge voltage at the motor produced by an inverter depends on the length and impedance of the power cables as well as the rise time of the power switches. Specifically, high *dV/dt* can damage the first coil of the motor and cause the motor

insulation to deteriorate. Measurements of the three-level inverter confirm that it produces peak voltages in motor cables that are lower than what has been typical in two-level inverters.

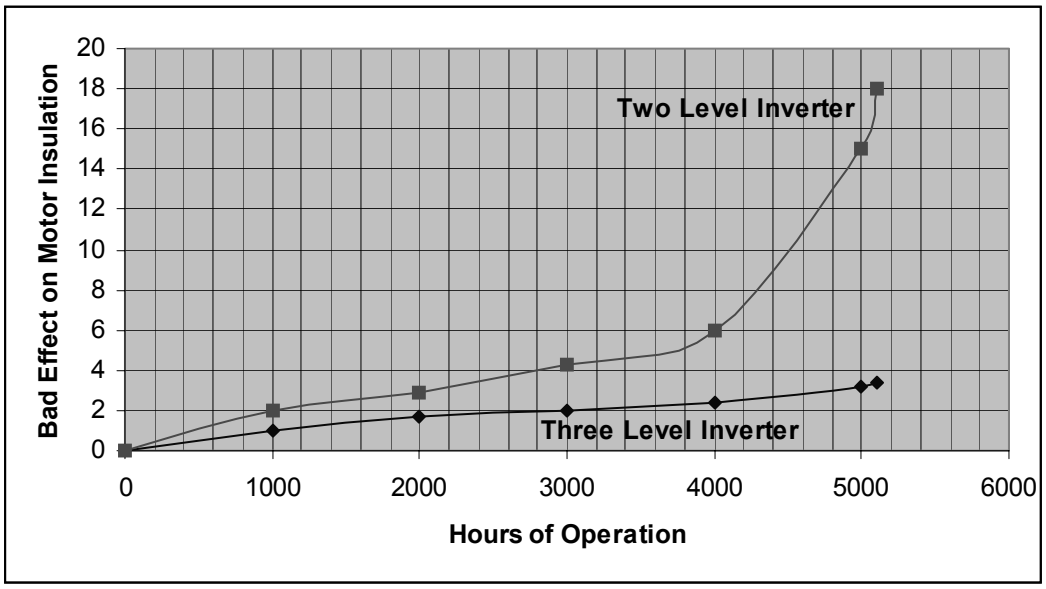


Fig.1.3 Motor-bearing life comparison between two-level and three-level inverter

Actual long period tests were conducted to verify the superiority of the three-level inverter from bearing life point of view. Tests prove that the use of three-level topology can result in a significantly longer bearing life.

1.5 BASIC BLOCK DIAGRAM

Fig.1.4 shows the block diagram of the three level voltage source inverter fed open loop induction motor drive. In the figure a three-phase bridge uncontrolled rectifier is fed from the three phase sinusoidal supply and it will be converted into controlled AC supply by controlling the gate pulses of the three-level inverter. DSP-TMS320F2811 control card will do the controlling the whole system as shown in fig.1.4. DSP will generate gate pulses for three-level inverter. Three-level inverter will give constant V/f control for induction motor drive.

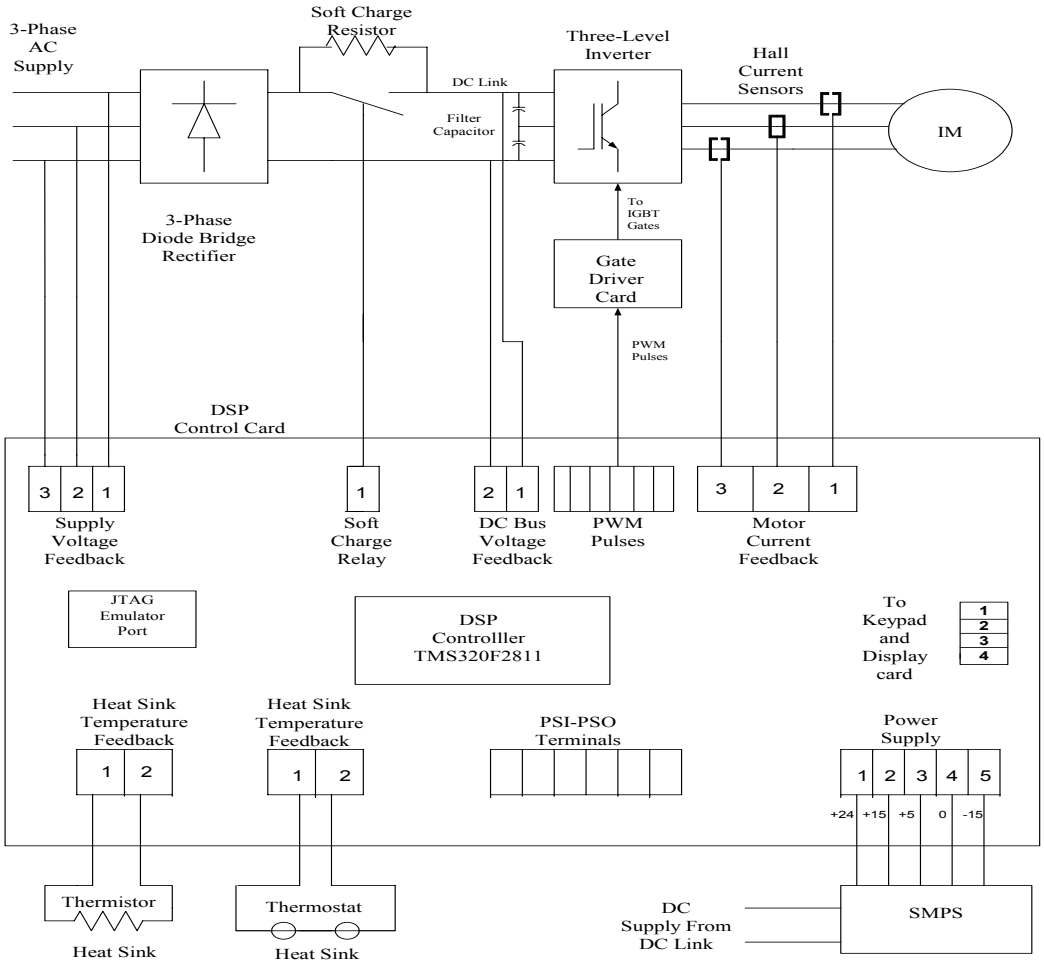


Fig.1.4 Block Diagram of three-level inverter fed Induction motor drive

1.6 LITERATURE SURVEY

Literature survey plays a very important role in the project. Literature survey consists of three level inverter related papers that includes different power topologies, control schemes, mathematical modeling, simulation and experiments. Papers ware taken from IEEE conference proceedings, journal proceedings and other standard publications. Three level inverter related data were taken from manufacturer that also includes power topologies, features and advantages.

José Rodriguez [1]

In this paper titled, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", described about the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multi cell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-

switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation.

Keith Corzine [2]

In this report titled, "Operation and Design of Multilevel Inverters", described the fundamentals of multilevel power conversion. Some background material is provided followed by the mathematical details of the power and control sections. The numerous topologies and modulation methods were discussed. An additional goal of this monograph was to introduce concepts related to reducing the number of isolated voltage sources and sensors.

Fei Wang [3]

In this paper titled, "Sine-Triangle versus Space-Vector Modulation for Three-Level PWM Voltage-Source Inverters", explained the inherent relations between sine-triangle and space-vector pulse width modulation schemes for three-level voltage-source inverters. It is shown that the two schemes can function equivalently through proper selection of common-mode injections in the case of sine-triangle modulation, or dwell times in equivalent redundant switching states in the case of space-vector modulation. Simulation and measurement results illustrate that understanding of these relations can lead to a more efficient and flexible three-level modulator with desired or optimal performance.

Kalpesh H. Bhalodi [4]

In this paper titled, "Space Vector Modulation with DC- Link Voltage Balancing Control for Three-Level Inverters", described the DC-link voltage balancing scheme for three-level inverter is proposed in this paper. Dependence of the DC link capacitor voltage deviation on DC-link current and inverter-switching states is established for proposed three-level inverter. Pulse pattern rearrangements for space vector PWM (SVPWM) using degree of freedom available in choice of redundant space vectors, sequencing of vectors, and splitting of duty cycles of vector are best exploited. Self neutral-point voltage deviation control in feed forward and simplified closed loop scheme

are proposed in this paper. Computer simulations verify the effectiveness of proposed scheme.

Aye Kocalmý [5]

In this paper titled, "Simulation of a Space Vector PWM Controller for a Three-Level Voltage-Fed Inverter Motor Drive", described a new simplified space vector PWM method for a three-level inverter fed induction motor drive. Simulation results are presented for various operation conditions using R-L load and motor load to verify the system model. This paper has explained in detail determining the sector, determining the region in the sector, calculating the switching times, Ta, Tb, and Tc, and finding the switching states.

Nikola Celanovic [6]

In this paper titled, "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters", explores the fundamental limitations of neutral-point voltage balancing problem for different loading conditions of three-level voltage source inverters. A new model in DQ coordinate frame utilizing current switching functions is developed as a means to investigate theoretical limitations and to offer a more intuitive insight into the problem. The low-frequency ripple of the neutral point caused by certain loading conditions is reported and quantified.

Josep Pou [7]

In this reference, Chapter-3 titled by "Space-Vector PWM" Technical University of Catalonia, described three dimensional vector representations, two dimensional vector representations, calculation of duty cycle, NTV modulation, and Symmetric modulation.

R.S. Kanchan [8]

In this paper titled, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages", proposed pulse width modulation (PWM) scheme for multilevel inverters. The proposed PWM scheme generates the inverter leg switching times, from the sampled reference phase voltage amplitudes and centers the switching times for the middle vectors, in a sampling interval, as in the case of conventional space vector PWM (SVPWM). The SVPWM scheme,

presented for multilevel inverters, can also work in the over modulation range, using only the sampled amplitudes of reference phase voltages.

P. N. Tekwani [9]

In this paper titled, "Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC Link Capacitor Voltage Balancing for an Open-End Winding Induction Motor Drive", described dc link capacitor voltage balancing scheme along with common mode voltage elimination is proposed for an induction motor drive, with open-end winding structure. The motor is fed from both the ends with three-level inverters generating a five level output voltage space phasor structure. Hysteresis Controller Based Closed Loop Dc Link Capacitor Voltage Balancing is used in this paper.

Bai Hua [10]

In this paper titled, "Comparison of Three PWM Strategies SPWM, SVPWM & One-cycle Control", explained Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are the most popular modulation strategies applied to variable frequency and adjusting speed systems, and there are diverges in comparing the merits and demerits of their own. Also there is another modulation strategy called One-cycle Control. This paper gathers the three strategies and does some comparisons through simulation based on a simulation tool-PSIM, and has drawn some profitable conclusions.

Hyo L. Liu [11]

In this paper titled, "DSP Based Space Vector PWM for Three Level Inverter with DC Link Voltage Balancing" described each voltage vector on space vector plane is classified in relation to charging discharging action DC capacitors and a new modulation method is suggested based on the voltage vector selection principle. The algorithm is implemented on Motorola DSP56000.

CHAPTER-2
MULTILEVEL INVERTER TOPOLOGIES

2.1 GENERAL

This chapter presents three power topologies of multilevel inverter. Advantages and disadvantages of topologies are also discussed. At the present time, the majority of research and development effort seems to concentrate on the development of three classes of inverters [2],

- The diode-clamped (neutral point clamped) multilevel inverter
- The flying capacitor inverter
- The Cascaded H-bridge inverters

2.2 DIODE-CLAMPED (NPC) MULTILEVEL INVERTER

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three-level. Because of industrial developments over the past several years, the three-level inverter is now used extensively in industry applications.

Fig. 2.1 shows the topology of the three-level diode-clamped inverter. Although the structure is more complicated than the two-level inverter, the operation is straightforward. Each phase node (*a*, *b*, or *c*) can be connected to any node in the capacitor bank (d_0, d_1, or d_2). Connection of the *a*-phase to junctions d_0 and d_2 can be accomplished by switching transistors T_{a1} and T_{a2} both OFF or both ON respectively. These states are the same as the two-level inverter yielding a line-to-ground voltage of zero or the dc voltage. Connection to the junction d_1 is accomplished by gating T_{a1} OFF and T_{a2} ON. In this representation, the labels T_{a1} and T_{a2} are used to identify the

transistors as well as the transistor logic (1=ON and 0=OFF). Since the transistors are always switched in pairs, the complements are labeled $\overline{T}_{a1}$ and $\overline{T}_{a2}$ accordingly.

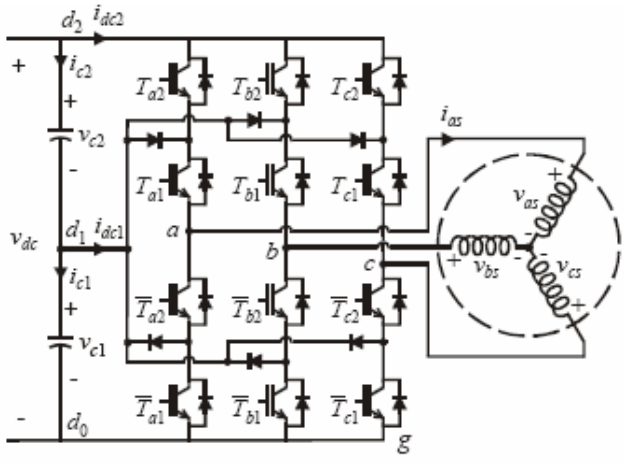


Fig.2.1 Three-level diode-clamped inverter topology

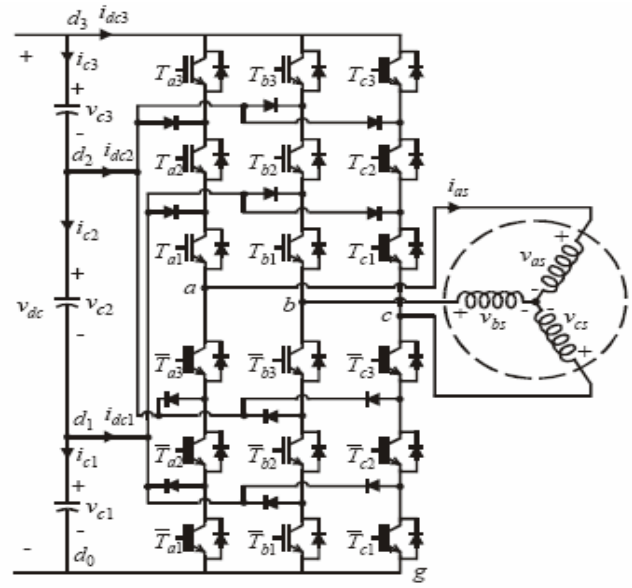


Fig.2.2 Four-level diode-clamped inverter topology

In a practical implementation, some dead time is inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition. From Fig. 2.1, it can be seen that, with this switching state, the *a*-phase current i_{as} will flow into the junction through diode D_{a1} if it is negative or out of the junction through diode D_{a2} if the current is

positive. According to this description, the inverter relationships for the *a*-phase are presented in Table -2.1.

TABLE – 2.1
THREE-LEVEL NPC INVERTER RELATIONSHIPS

S_a	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}
0	0	0	0	0	0
1	0	1	v_{c1}	i_{as}	0
2	1	1	$v_{c1} + v_{c2}$	0	i_{as}

The dc currents i_{adc1} and i_{adc2} are the *a*-phase components to the junction currents i_{dc1} and i_{dc2} in Fig. 2.1 respectively. Extending the diode-clamped concept to four levels results in the topology shown in Fig. 2.2. A pair of diodes is added in each phase for each of the two junctions. The operation is similar to the three-level inverter with the relationships described in Table -2.2.

TABLE – 2.2
FOUR-LEVEL NPC INVERTER RELATIONSHIPS

S_a	T_{a3}	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}	i_{adc3}
0	0	0	0	0	0	0	0
1	0	0	1	v_{c1}	i_{as}	0	0
2	0	1	1	$v_{c1} + v_{c2}$	0	i_{as}	0
3	1	1	1	$v_{c1} + v_{c2} + v_{c3}$	0	0	i_{as}

The advantages of diode-clamped multilevel inverter are,

- Voltages across the switches are only half of the dc-link voltage.
- The first group of voltage harmonics is centered around twice the switching frequency.
- The control method is simple.

The disadvantages of diode-clamped multilevel inverter are,

- This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress.
- For topologies with more than three levels the clamping diodes are subject to increased voltage stress equal to $V_{pn}(n-1)/n$. Therefore, series connection of diodes might be required. This complicates the design and raises reliability and cost concerns.

- The issue of maintaining the charge balance of the capacitors is still an open issue for NPC topologies with more than three-levels. Although the three-level NPC topology works well with high power factor loads, NPC topologies with more than three levels are mostly used for Static VAR Compensation circuits.

2.3 FLYING CAPACITOR MULTILEVEL INVERTER

Another fundamental multilevel topology, the flying capacitor, involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one dc source is needed.

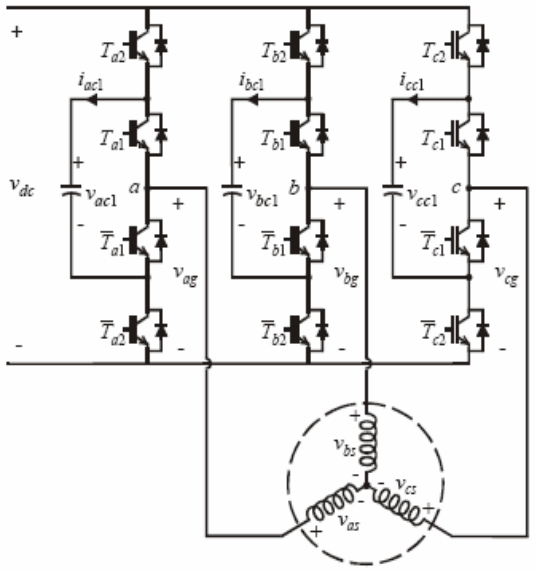


Fig. 2.3 Three-level flying capacitor topology

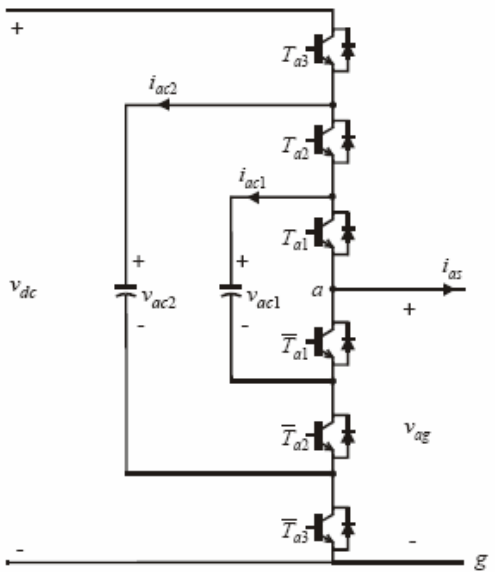


Fig. 2.4 Four-level flying capacitor topology

Fig. 2.3 shows the three-level flying capacitor inverter. The general concept of operation is that each flying capacitor is charged to one-half of the dc voltage and can be connected in series with the phase to add or subtract this voltage. Table -2.3 shows the relationships for the *a*-phase.

In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states which make up the level $S_a = 1$. Considering the direction of the *a*-phase flying capacitor current i_{ac1} for the redundant

states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. In Table-2.3, the current i_{adc} is the *a*-phase component of the dc current. The total dc current can be calculated by summing the components for all phases.

TABLE – 2.3
THREE-LEVEL FLYING CAPACITOR RELATIONSHIPS

S_a	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{adc}
0	0	0	0	0	0
1	0	1	v_{ac1}	$-i_{as}$	0
	1	0	$v_{dc} - v_{ac1}$	i_{as}	i_{as}
2	1	1	v_{dc}	0	i_{as}

Fig.2.4 shows the structure for the *a*-phase of the four-level flying capacitor inverter. For this inverter, the capacitors v_{ac1} and v_{ac2} are ideally charged to one-third and two-thirds of the dc voltage respectively. The four voltage levels are obtained by the relationships shown in Table -2.4.

TABLE – 2.4
FOUR-LEVEL FLYING CAPACITOR RELATIONSHIPS

S_a	T_{a2}	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{ac2}	i_{adc}
0	0	0	0	0	0	0	0
1	0	0	1	v_{ac1}	$-i_{as}$	0	0
	0	1	0	$v_{ac2} - v_{ac1}$	i_{as}	$-i_{as}$	0
	1	0	0	$v_{dc} - v_{ac2}$	0	i_{as}	i_{as}
2	0	1	1	v_{ac2}	0	$-i_{as}$	0
	1	1	0	$v_{dc} - v_{ac1}$	i_{as}	0	i_{as}
	1	0	1	$v_{dc} - v_{ac2+} v_{ac1}$	$-i_{as}$	i_{as}	i_{as}
3	1	1	1	v_d	0	0	i_{as}

The advantages of Flying Capacitor topology are,

- This topology naturally limits the *dV/dt* stress across the devices.
- Introduces additional switching states that can be used to help maintain the charge balance in the capacitors.

The disadvantages of Flying Capacitor topology are:

- The flying capacitor topology might require more capacitance than the equivalent diode clamped topology. In addition, it is obvious that rather large RMS currents will flow through these capacitors.

- High-level inverters are more difficult to package with the bulky power capacitors and are more expensive.

2.4 CASCADED H-BRIDGE INVERTERS

The series H-bridge inverter appeared in 1975, and several patents have been obtained for this topology. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. A two-cell series H-bridge inverter is shown in Fig. 2.5. The inverter consists of familiar H-bridge (sometimes referred to as full-bridge) cells in a cascade connection. Since each cell can provide three voltage levels (zero, positive dc voltage, and negative dc voltage), the cells are themselves multilevel inverters. Taking the *a*-phase, the relationship for a particular cell can be expressed as in Table -2.5.

TABLE – 2.5
CASCADED H-BRIDGE FIVE-LEVEL RELATIONSHIPS

S_{aHi}	T_{aLi}	T_{aRi}	v_{agi}	i_{adci}
-1	0	1	$-v_{adci}$	$-i_{as}$
0	0	0	0	0
	1	1	0	0
1	1	0	v_{adci}	i_{as}

* Where i = No. of Cell per leg. *i.e.* i^{th} Cell.

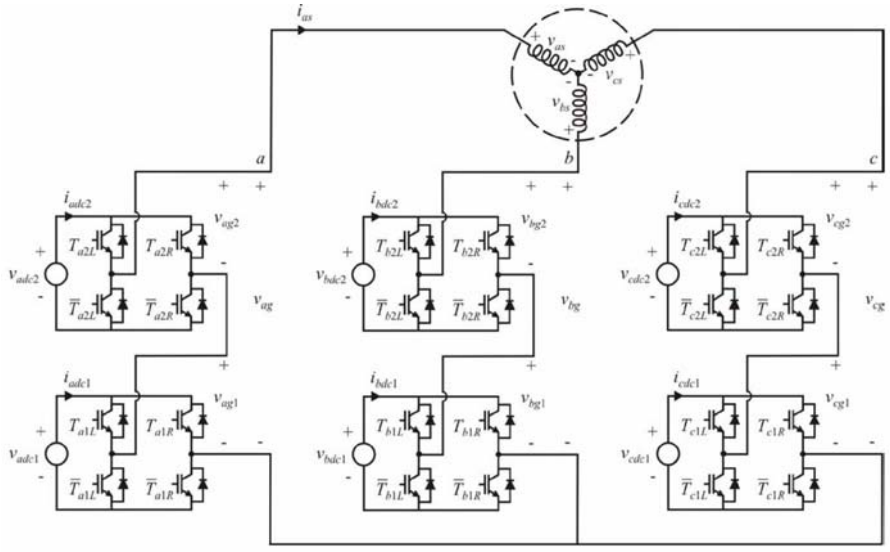


Fig. 2.5 Two-cell Cascaded Five-level H-bridge inverter

The advantages of Cascaded H-bridge topology are,

- It requires less number of components to achieve the same number of voltage levels.
- Optimized circuit layout and packaging are possible because each level has same structure.
- No extra clamping diodes and voltage balancing capacitors are required.
- Soft-switching techniques can be used to reduce switching losses and device stresses.
- H-bridge topology is that it provides the flexibility to increase the number of levels without introducing complexity into the power stage.

The disadvantages of Cascaded H-bridge topology are,

- It needs separate DC sources for real power conversions, thereby limiting its applications.
- The H-bridge configuration uses multiple dedicated dc-busses and often a complicated and expensive line transformer, which makes this a rather expensive solution.

TABLE – 2.6
COMPARISON OF COMPONENT REQUIREMENTS PER LEG OF THREE MULTILEVEL INVERTERS

Topology	Level	a	b	c	d	e
Diode Clamped	n = 3,4,5,6…	(n-1)*2	(n-1)*2	(n-1)*(n-2)	(n-1)	0
Flying Capacitors	n = 3,4,5,6…	(n-1)*2	(n-1)*2	0	1	(n-2)
Cascaded Inverters	n = 3,5,7,9…	(n-1)*2	(n-1)*2	0	(n-1)/2	0

Where, a : main switching devices

b : main diodes

c : clamping diodes

d : dc bus capacitors

e : balancing capacitors

CHAPTER-3
MODULATION METHODS FOR MULTILEVEL INVERTER

3.1 GENERAL

It is generally accepted that the performance of an inverter, with any switching strategies, can be related to the harmonic contents of its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms. In multilevel technology, the well-known modulation methods are as follows,

- Sinusoidal Pulse Width Modulation (SPWM)
- Space Vector Pulse Width Modulation (SVPWM)

3.2 SINUSOIDAL PULSE WIDTH MODULATION (SPWM)

Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. These methods have been extensively studied and are among the most popular in industrial applications. These methods involve a comparison of the reference sine signal with a triangular carrier waveform and the detection of crossover instances to determine switching events. The variations of these methods are essentially in the polarity and shape of the carrier waveforms.

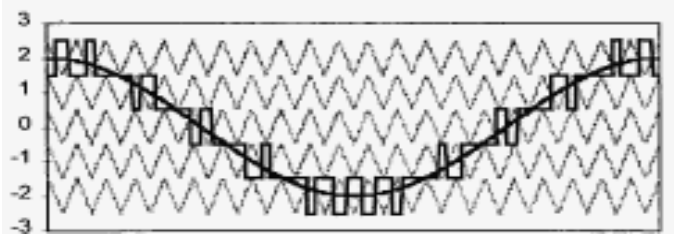


Fig. 3.1 Six–Level SPWM

For an n-level inverter, n-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference, or modulation, waveform has peak-to-peak amplitude A_m and frequency f_m, and it is centered in the middle of the carrier set. The three cases of triangular wave disposition are,

- Alternative phase opposition disposition, where each carrier band is shifted by 180^o from the adjacent bands,
- Phase opposition disposition, where the carriers above the zero reference are in phase, but shifted by 180^o from those carriers below the zero reference and
- In-phase disposition, where all the carriers are in phase.

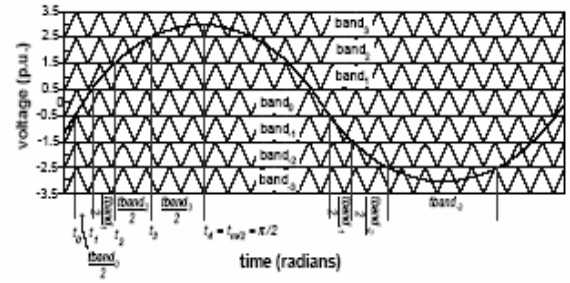


Fig. 3.2 SPWM for n = Even

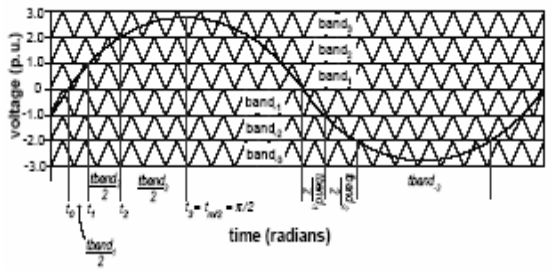


Fig. 3.3 SPWM for n = odd

Fig. 3.2 and 3.3 shows the SPWM for number of output levels even and odd respectively.

Advantages of SPWM,

- More flexible
- Simpler to implement

Disadvantages of SPWM,

- The maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage [8]
- The extension of the SPWM schemes into the over-modulation range is difficult

3.3 SPACE VECTOR PULSE WIDTH MODULATION (SVPWM)

The space-vector PWM method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications. Because of its superior performance characteristics, it has been finding widespread application in recent years.

It can be shown that the reference vector V^* with magnitude V rotates in a circular orbit at angular velocity ω, where the direction of rotation depends on the phase sequence of the voltages. With the sinusoidal three-phase command voltages, composite PWM fabrication at the inverter output should be such that the average voltages follow these command voltages with a minimum amount of harmonic distortion.

The space vector modulation uses averaging technique, as it uses the voltage vector such that their average value is equal to the instantaneous output voltage required. For averaging the value, the first step is identifying the nearest three voltage vectors (NTV) and using the redundancy. After identification the next step is to estimate the on-time period for each voltage vector. The final step is to determine the sequence of switching of each voltage vector. The help of fast DSP can implement the SVM.

3.3.1 SPACE VECTOR PWM FOR THREE-LEVEL DIODE CLAMPED INVERTER

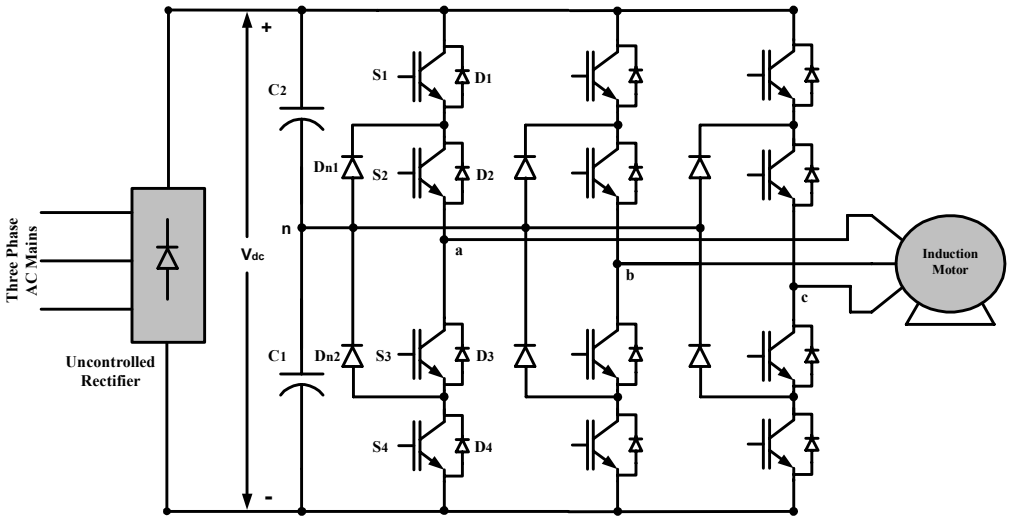


Fig.3.4 Three-level Diode clamped inverter topology for induction motor drive

In case of a two-level inverter there are total of 8-vectors (6-non zero vectors and 2-zero vectors).

The number of vectors for n-level inverter is given by,

$$\text{No. of space vector} = n^3 \tag{3.1}$$

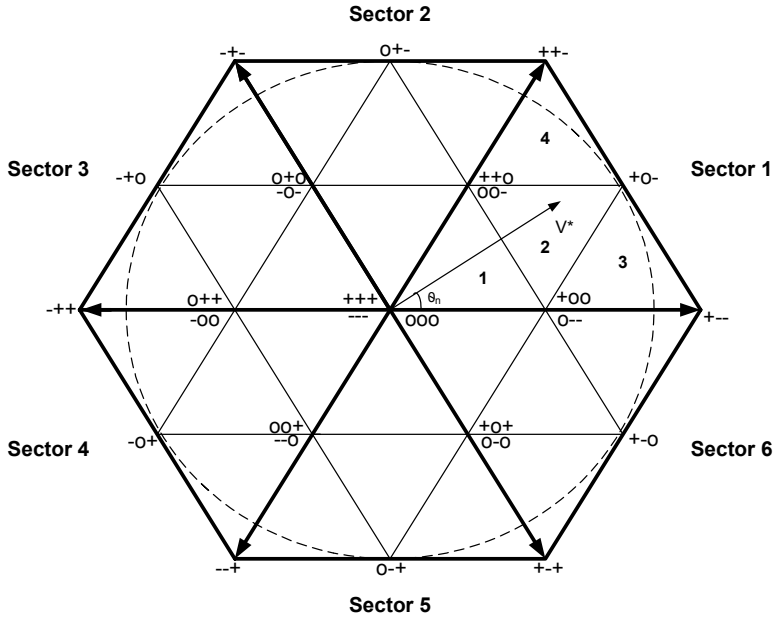


Fig. 3.5 Space (Stationary) Vector Diagram for Three-Level Inverter

Suitable vectors from the space vector diagram should be chosen for each modulation cycle in order to generate the reference vector V^*. The vectors nearest to V^* are the most appropriate selections in terms of their ability to minimize the switching frequencies of the power devices, improve the quality of the output voltage spectrum, and the electromagnetic interference (EMI). The switching states of the inverter are summarized in Table-3.1,

TABLE-3.1
DEFINITION OF SWITCHING STATES

Switching States	**Device Switching Status (Phase a)**				**Pole Voltage V_a**
	S_1	S_2	S_3	S_4	
+	ON	ON	OFF	OFF	$+V_{dc}/2$
O	OFF	ON	ON	OFF	O
-	OFF	OFF	ON	ON	$-V_{dc}/2$

In figure 3.5, the Space Vector diagram of the three-level inverter is divided into six sectors, and each sector is then divided into four triangular regions in order to show the vectors nearest to the reference.

Figure 3.6 represents the simplified model of the three-level diode clamped inverter, where Vc1 and Vc2 are the voltages across the lower and the upper capacitors voltages respectively.

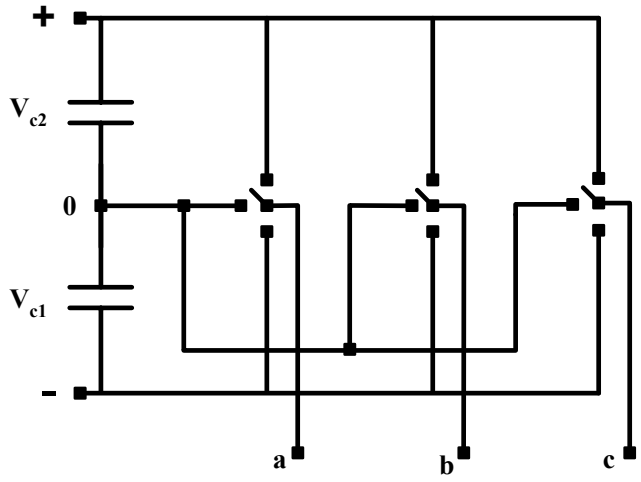


Fig. 3.6 Equivalent circuit of Three-Level Diode Clamped Inverter

Each leg has the following three-states, which are utilized to generate the required voltage,

Switching State '+': Upper switch ON.

Switching State 'O': Middle switch ON.

Switching State '-': Lower switch ON.

Four groups of space (stationary) vectors can be distinguished in this Space Vector diagram, as described in the following,

- The "large vectors" ('+--', '++-', '-+-', '-++', '--+' and '+-+') assign the output voltages of the inverter to either the highest or the lowest DC voltages levels. As they do not connect any output to the NP, they do not affect the voltage balance of the capacitors. These vectors can generate the highest AC voltage amplitudes because they have the greatest lengths. In fact, these six vectors are equivalent to the active ones of the two-level inverter.
- The "medium vectors" ('+0-', '0+-', '-+0', '-0+', '0-+' and '+-0') connect each output to a different DC-link voltage level. Under balanced conditions, their tip end in the middle of the segments that join two consecutive large vectors. The length of the medium vectors defines the maximum amplitude of the reference

vector for linear modulation and steady-state conditions, which is $\sqrt{3}/2$ the length of the large vectors. Since one output is always connected to the NP, the corresponding output current will define the NP current. This connection produces voltage imbalances in the capacitors, and these must be compensated.

- The "short vectors" ('0--/+00', '00-/++0', '-0-/0+0', '-00/0++', '--0/00+' and '0-0/+0+') connect the AC outputs to two consecutive DC-link voltage levels. Their length is half the length of the large vectors. They are double vectors, which means that two states of the converter can generate the same voltage vector. As they affect the NP current in opposite ways, proper utilization of these vectors will help the NP voltage to achieve balance.
- The "zero vectors" ('---', '000' and '+++') are in the origin of the diagram. They connect all of the outputs of the converter to the same DC-link voltage level, and therefore, they do not produce any current in the DC side.

Advantages of SVPWM:

- SVPWM scheme gives a more fundamental voltage and better harmonic performance compared to the SPWM schemes
- The maximum peak of the fundamental component in the output voltage obtained with space vector modulation is 15% greater than with the sine-triangle modulation scheme

Disadvantages of SVPWM:

- The conventional SVPWM scheme requires sector identification and look-up tables to determine the timings for various switching vectors of the inverter, in all the sectors. This makes the implementation of the SVPWM scheme quite complicated.
- Increase the computation time.

CHAPTER-4
CAPACITOR VOLTAGE CONTROL FOR NPC INVERTER

4.1 GENERAL

This chapter presents the effect of switching states on neutral voltage deviation, mathematical modeling of three-level inverter, open loop (self balancing) SVPWM scheme and close loop SVPWM balancing scheme [17]-[22]. The conventional seven segments and self balancing SVPWM switching pattern have been discussed in detail.

4.2 EFFECT OF SWITCHING STATES ON NEUTRAL VOLTAGE DEVIATION

The effect of switching states on neutral voltage deviation is illustrated in fig.4.1 When the inverter is operated with switching state [+++] of zero vector, the upper two switches in each of the three inverter legs are turned on, connecting the inverter terminals a, b, and c to the positive DC bus as shown in fig. 4(a). Since the neutral point 'n' is left unconnected, this switching state does not affect V_n. Similarly, the other zero switching states [000] and [---] do not cause V_n to shift either. Fig 4.1(b) shows the inverter operation with P-type switching state [+OO] of small vector. Since the three phase load is connected between the positive DC bus and neutral point 'n', the neutral current in1 flows in 'n', causing V_n to increase. On the contrary, the N-type switching state [O--] of small vector makes V_n to decrease as shown in fig. 4.1(c). For medium vector with switching state [+O-] in fig. 4.1(d), load terminals a, b, and c are connected to the positive bus, the neutral point, and the negative bus, respectively. Depending on the inverter operating conditions, the neutral-point voltage V_n may rise or drop. Considering a large vector with switching state [+--] as shown in fig. 4.1(e), the load terminals are connected between the positive and negative DC buses. The neutral point 'n' is left unconnected and thus the neutral voltage is not affected.

It is summarized that zero and large vectors do not affect the neutral point voltage. Medium vectors affect V_n, but the direction of voltage deviation is undefined so, redundant small vectors having dominant influence on V_n are used for neutral point voltage control. Above discussion is made under the assumption that the inverter is in

motoring mode. In addition to the influence of switching states, the neutral-point voltage may also be affected by a number of other factors like unbalanced DC capacitors due to manufacturing tolerances, inconsistency in switching device characteristics, unbalanced three-phase operation, motoring/regenerative mode of operation etc. As compared to motoring mode, an opposite capacitor voltage charging-discharging action takes place in the regenerative mode due to the reversal of current.

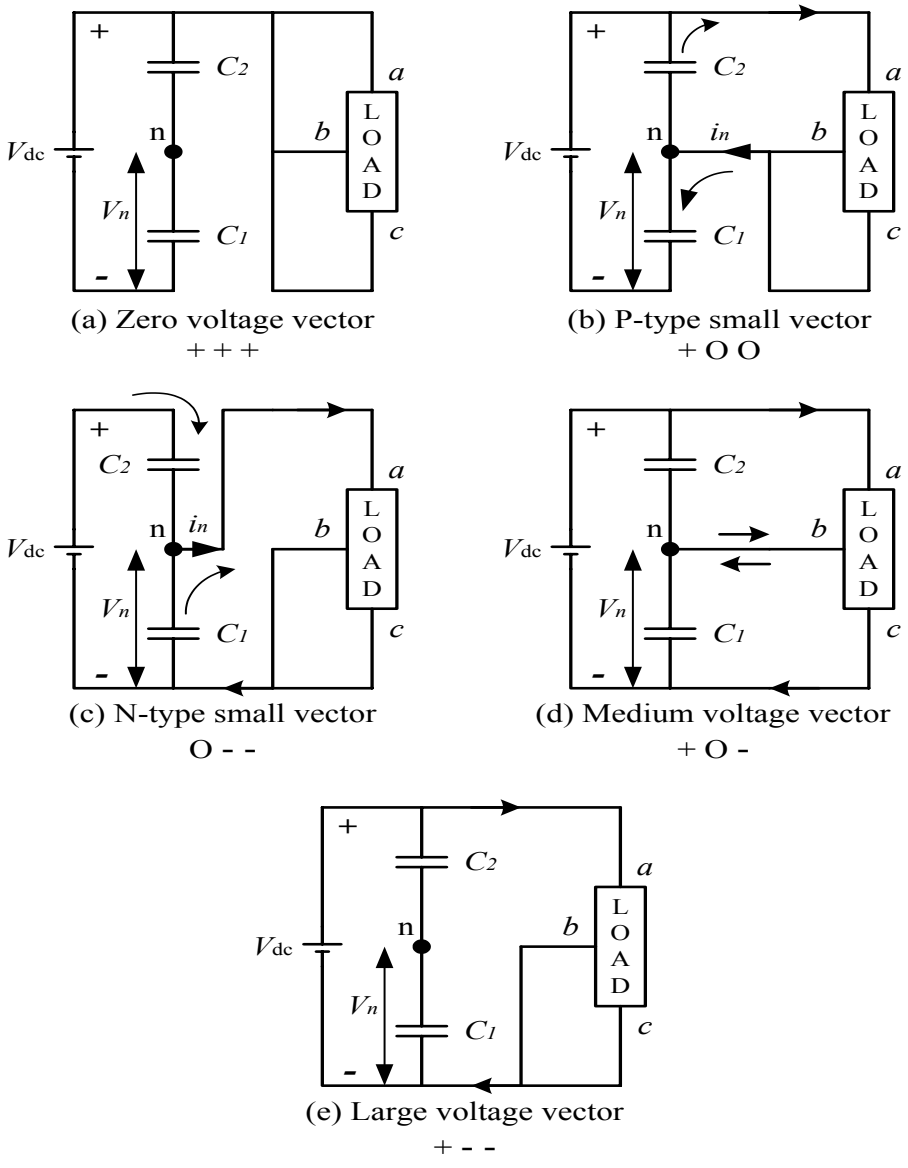


Fig.4.1 Effect of switching states on neutral point voltage deviation

4.3 MATHEMATICAL MODELING OF THREE-LEVEL INVERTER

The terminology in this report is explained with reference to fig.4.2, in which DC bus structure and each inverter phases is modeled as 3-pole switch. The inverter switching functions *Sa, Sb,* and *Sc*, assume value equal to 1, 2 or 3, which means that the pole of the switch in connected to bottom, middle or top DC-link respectively. The load currents are denoted as i_a, i_b, and i_c while the currents drawn by the inverter from bottom, middle and top rails of the DC-link are i_1, i_2, and i_3 respectively.

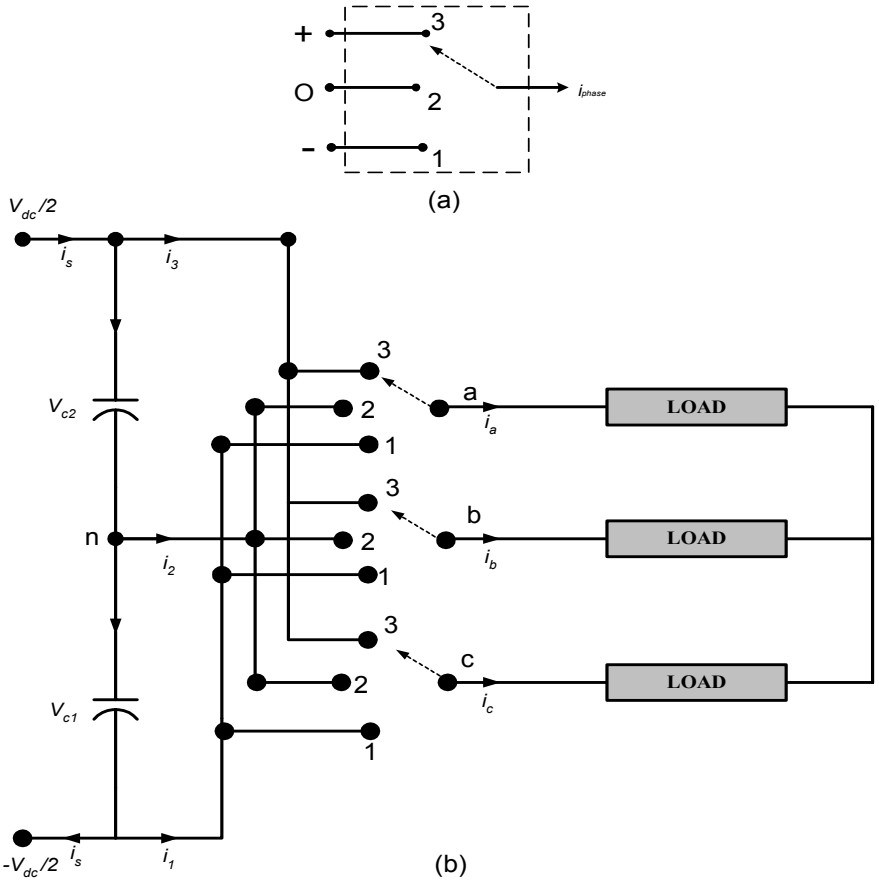


Fig. 4.2 Three-level inverter and load system model

In general the inverter pole voltage with respect to the negative DC bus can be written in terms of capacitor voltages and the switching functions as

$$v_{a1}(S_a) = \delta(S_a - 1)v_{c1} + \delta(S_a - 2)(v_{c1} + v_{c2})$$
$$v_{b1}(S_b) = \delta(S_b - 1)v_{c1} + \delta(S_b - 2)(v_{c1} + v_{c2}) \quad (4.1)$$
$$v_{c1}(S_c) = \delta(S_c - 1)v_{c1} + \delta(S_c - 2)(v_{c1} + v_{c2})$$

In (4.1) $\delta(.)$ is the Dirac delta function, v_{c1} and v_{c2} are the voltage across lower and upper capacitors. The currents drawn from the DC-link nodes can be represented in terms of the motor currents as shown in (4.2)

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} \delta(S_a-1) & \delta(S_b-1) & \delta(S_c-1) \\ \delta(S_a-2) & \delta(S_b-2) & \delta(S_c-2) \\ \delta(S_a-3) & \delta(S_b-3) & \delta(S_c-3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{4.2}$$

For the three wire load,

$$i_a + i_b + i_c = 0$$

$$i_1 + i_2 + i_3 = 0 \tag{4.3}$$

Substituting $i_c = -i_a - i_b$ and removing the dependent variable i_3, (4.2) gets reduced to

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} [\delta(S_a-1)-\delta(S_c-1)] \\ [\delta(S_a-2)-\delta(S_c-2)] \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{4.4}$$

The current flowing through capacitor is given by

$$i_{c2} = i_s - i_3 = i_s - (-i_2 - i_1) = i_s + i_2 + i_1$$

$$i_{c1} = i_s + i_1 \tag{4.5}$$

$$\begin{bmatrix} i_{c2} \\ i_{c1} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_s \\ i_2 \\ i_1 \end{bmatrix} \tag{4.6}$$

Thus, the currents flowing through capacitors is directly related to the voltage across the capacitors and the relationship is given by

$$\begin{bmatrix} v_{c2} \\ v_{c1} \end{bmatrix} = \frac{1}{C}\int \left\{ \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{c2} \\ i_{c1} \end{bmatrix} dt \right\} = \frac{1}{C}\int \left\{ \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_s \\ i_2 \\ i_1 \end{bmatrix} dt \right\} \tag{4.7}$$

Let Δv_c be the change in the capacitor voltage, Substituting value from (4.4) into (4.6), results in

$$\Delta v_c = v_{c1} - v_{c2} \tag{4.8}$$

$$\Delta vc = \frac{1}{C}\int i_2 dt \tag{4.9}$$

Thus the load current drawn from the middle node of the DC-link is responsible for the variation in the capacitor voltages. Whenever switching functions S_a, S_b, and S_c, assume value equal to 2, there exists a tendency of capacitor voltage unbalancing.

4.4 DC-LINK CAPACITOR VOLTAGE BALANCING SCHEMES

Various space vector modulation (SVM) schemes have been proposed for the three-level NPC inverter using either open loop scheme or closed loop scheme [4].

4.4.1 OPEN LOOP CAPACITOR VOLTAGE SELF BALANCING SCHEME

This section proposes modified SVM scheme for better neutral point stabilization. To reduce neutral-point voltage deviation, the dwell time of a given small vector can be equally distributed between the P-type and N-type switching states over a sampling period. For nearest three vectors (NTV) selection SVM either one small vector or two small vectors among the three selected vectors are available according to the triangular regions in which the reference vector V^* lies. When the reference vector V^* is in region 2 or 4, only one small vector is in NTV where as in region 1 or 3 two small vectors are in NTV. In conventional SVM seven segments pulse pattern is chosen for all regions. Its pulse pattern arrangement for region Al is shown in fig. 4.3.

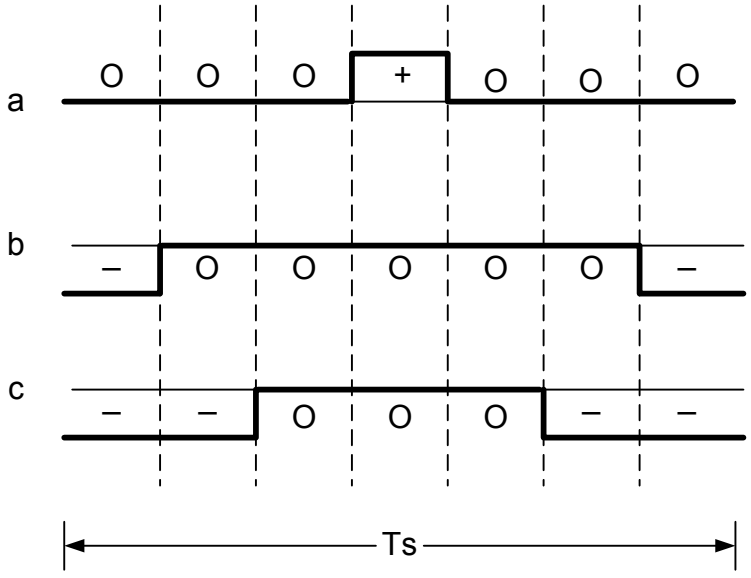


Fig. 4.3 Pulse pattern arrangement for conventional seven segment SVPWM in region-1

Seven segments SVM divide dwell time of only one small vector in P-type and N-type out of two small sectors available in region 1 and 3. So, neutral point deviation is not minimized in these regions. To reduce neutral-point voltage deviation according to location of region, optimized pulse pattern arrangement is proposed here. Negative sequences of modified SVM pulse pattern arrangement for regions l, 2, 3, and 4 of sector 1 are shown in fig 4.4. Here two redundant small vectors are used for neutral point voltage control for regions 1 and 3. Switching sequence in opposite sectors (1-4, 2-5 and 3-6) is selected to be of a complimentary nature for neutral point balancing.

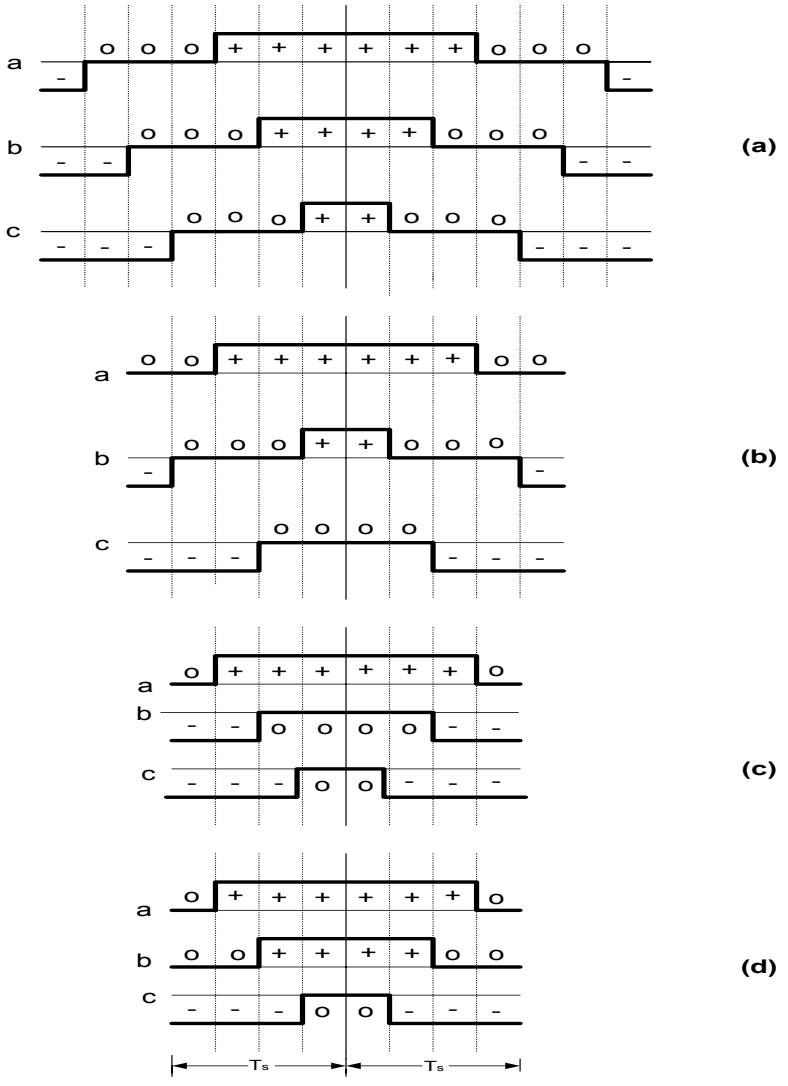


Fig.4.4 Self balancing switching patterns of Sector –1 for (a) Region-1, (b) Region-2, (c) Region-3, (d) Region-4

4.4.2 CLOSED LOOP CAPACITOR VOLTAGE BALANCING SCHEME

There always exists a small-voltage vector in each switching sequence, whose dwell time is divided into sub periods, one for its P-type and the other for its N-type switching state. For instance, the dwell time T_{1p} and T_{1n}, which is half/half split normally, can be distributed as,

$$T_1 = T_{1p} + T_{1n} \quad (4.10)$$

Where, T_{1p} = dwell time for Positive Small Space (Stationary) Vector
T_{1n} = dwell time for Negative Small Space (Stationary) Vector
Are given by,

$$T_{1p} = T_1 / 2(1+\Delta t) \quad (4.11)$$

$$T_{1n} = T_1 / 2(1-\Delta t) \quad (4.12)$$

where $-1 <= \Delta t <= 1$

The deviation of the neutral point voltage can be further reduced by adjusting the incremental time interval Δt in (4.11 and 4.12), according to the detected DC capacitor voltages V_{c1}, and V_{c2}. The input to the voltage balancing scheme is the difference in capacitor voltages ΔV_c where, $\Delta V_c = V_{c2} - V_{c1}$. For instance, if ΔV_c is greater than the maximum allowed DC voltage deviation ΔV_m for some reasons, it can be increase T_{1p} and decrease T_{1n} by Δt ($\Delta t>0$) simultaneously for the drive in a motoring mode. A reverse action ($\Delta t<0$) should be taken when the drive is in a regenerative mode. The relationship between the capacitor voltages and the incremental time interval Δt is summarized in Table 4.1.

TABLE-4.1
RELATIONSHIP BETWEEN CAPACITOR VOLTAGES AND INCREMENTAL TIME INTERVAL Δt

Neutral Point Deviation Level	Motoring Mode $i_d > 0$	Regenerating Mode $i_d < 0$
$(V_{c2} - V_{c1}) > \Delta V_m$	$\Delta t > 0$	$\Delta t < 0$
$(V_{c2} - V_{c1}) < \Delta V_m$	$\Delta t < 0$	$\Delta t > 0$
$(V_{c2} - V_{c1}) = \Delta V_m$	$\Delta t = 0$	$\Delta t = 0$

Where, ΔV_m = Maximum allowed DC voltage deviation ($\Delta V_m > 0$)
i_d = DC link current, Δt = Incremental time interval

CHAPTER-5
SIMULATION OF THREE LEVEL (NPC) INVERTER

5.1 GENERAL

Simulation is important before implementation of any scheme. The values of different components like capacitor value its voltage rating, and its current capacity simulation has been carried out in PSIM 6.0 software. This chapter shows simulation of three-level inverter with SVPWM and SPWM under different operating conditions like steady state and transient. This chapter has the simulation done with the DLL block and program of DLL block can directly used for the DSP programming after some modification.

5.2 SIMULATION OF NPC THREE-LEVEL INVERTER USING SPWM

5.2.1 SIMULATION OF SPWM FOR NPC THREE-LEVEL INVERTER

The simulation circuit of SPWM is shown in fig.5.1. In SPWM scheme the sine reference is compared with triangular carrier wave. For three-level inverter two triangular carrier waves are required. Here level shifted in phase disposition SPWM scheme has been simulated. Simulation conditions and results are described in below. Line voltage, line current and dc link voltages are shown in figures 5.3, 5.4 and 5.5.

Specifications of Motor, 10 hp, 2-pole, 415 V, 50 Hz, At No Load

Rs = 0.6338 Ω, Ls = 0.0035 H,

Rr = 0.6106 Ω, Lr = 0.0035 H,

Lm = 0.1965 H,

Moment of Inertia = 0.048 Kg – m^2

5.2.2 SIMULATION RESULTS OF LEVEL SHIFTED IN PHASE DISPOSITION (IPD) SPWM

Simulation Conditions, Carrier frequency f_{car} = 2 kHz

Reference frequency f_{ref} = 50 Hz

Simulation Time = 2 sec

Condition for gate pulse output $V_{ref} >= V_{cerrier}$

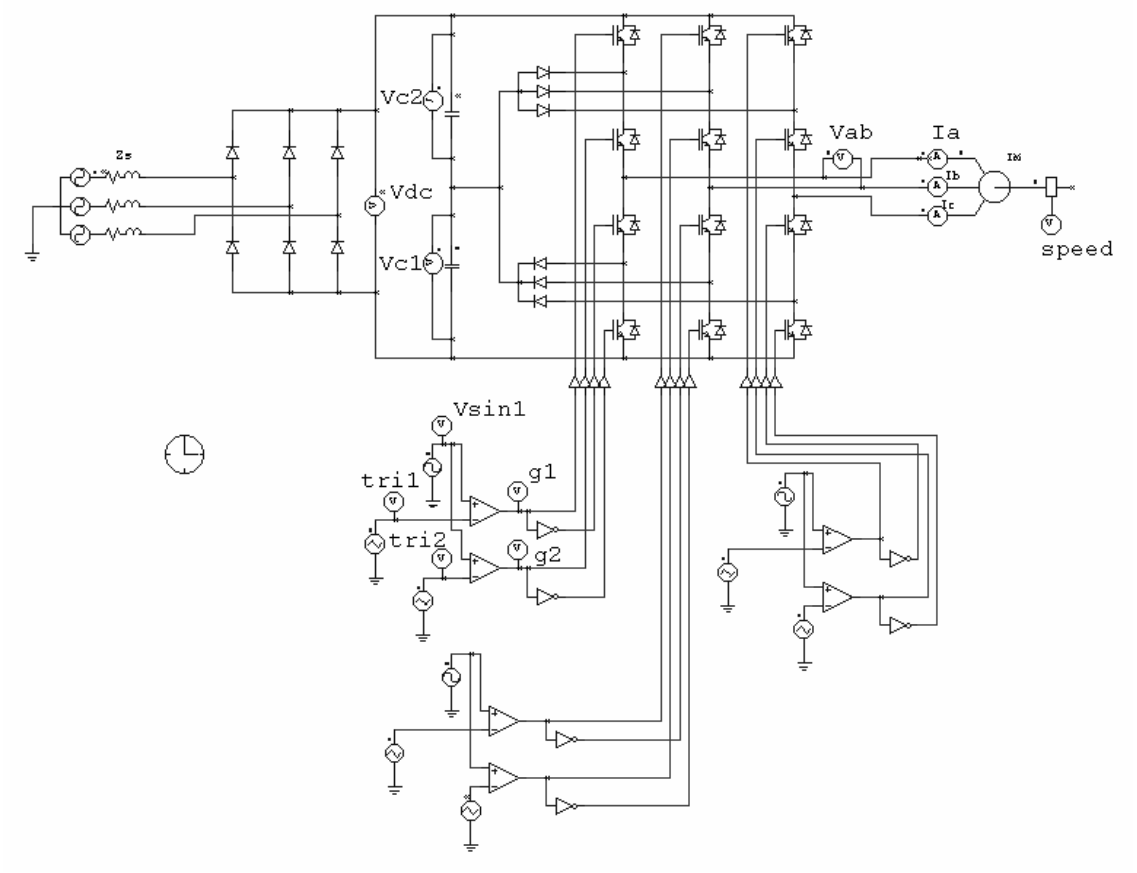


Fig. 5.1 Simulation circuit of SPWM for NPC three-level inverter

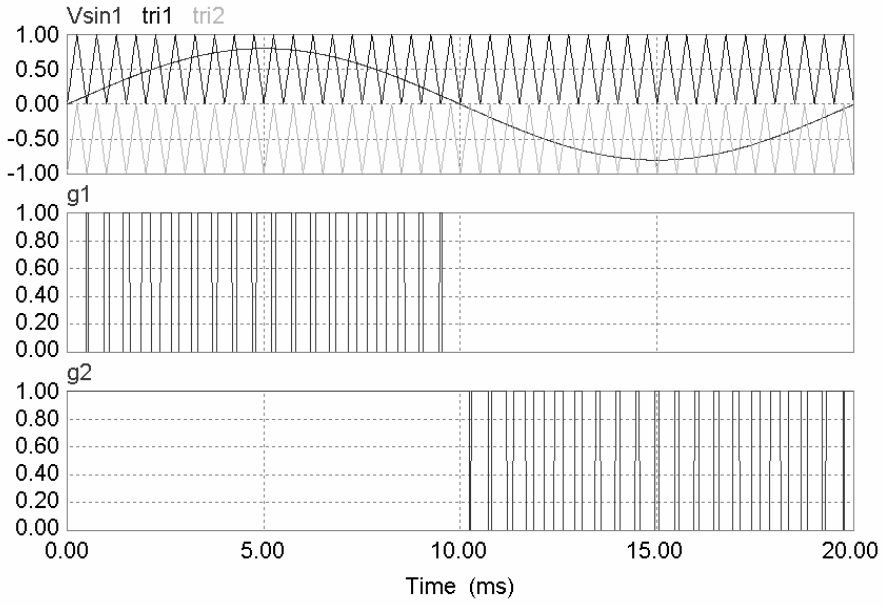


Fig.5.2 Level Shifted SPWM, Vsin1 = Reference Wave, tri1 and tri2 = Carrier Wave, g1 & g2 = Gate Pulses to IGBT

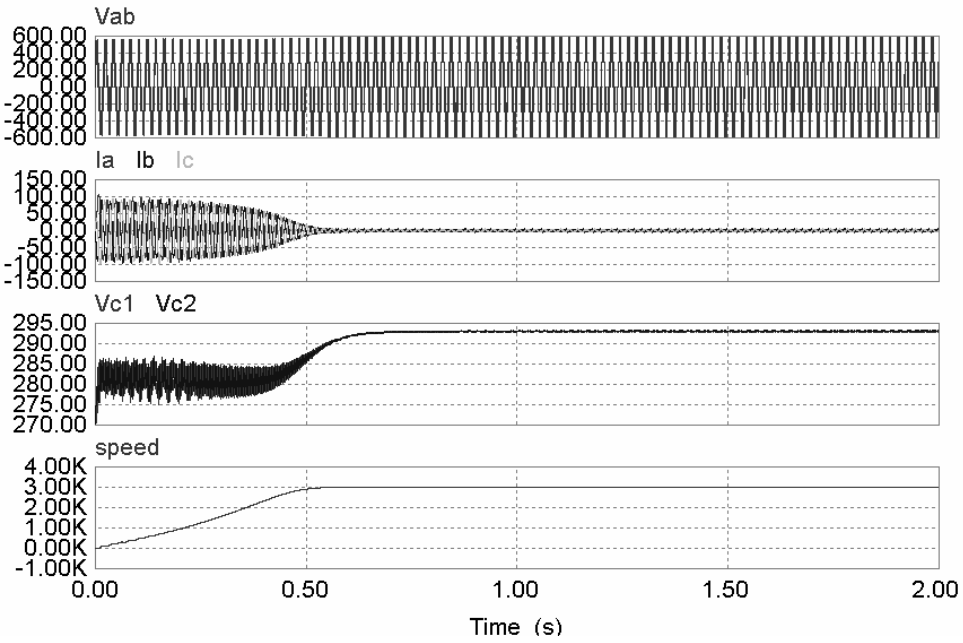


Fig.5.3 Simulation results of SPWM, Vab = Line Voltage, Ia, Ib, Ic = Line current, Vc1 = Lower Capacitor Voltage, Vc2 = Upper Capacitor Voltage, speed = Actual motor speed

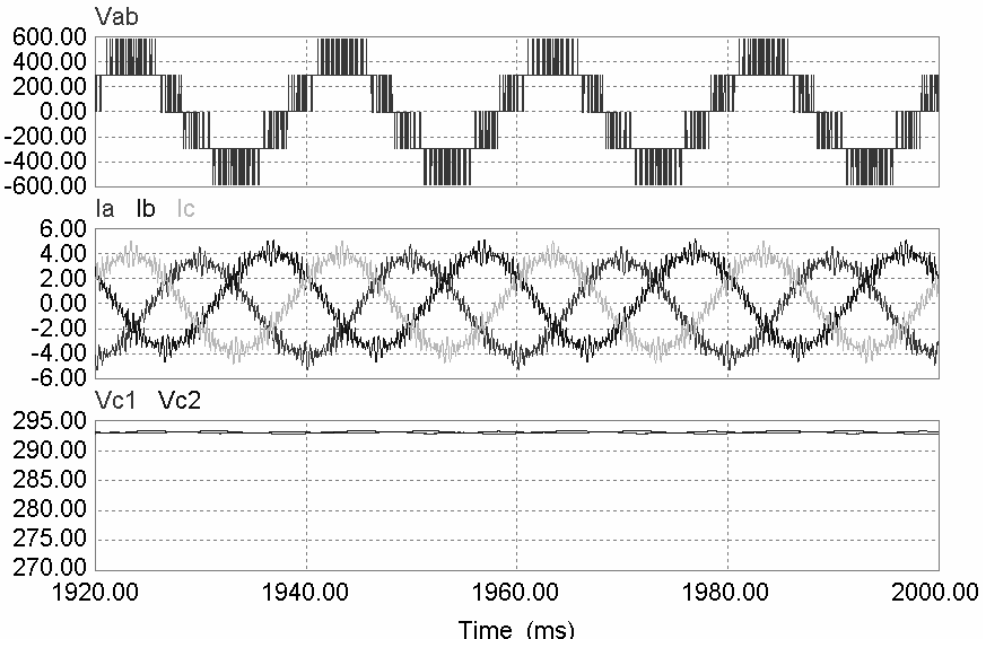


Fig.5.4 Expanded waveforms of SPWM simulation, Vab = Line Voltage, Ia, Ib, Ic = Line currents, Vc1 = Lower Capacitor Voltage, Vc2 = Upper Capacitor Voltage

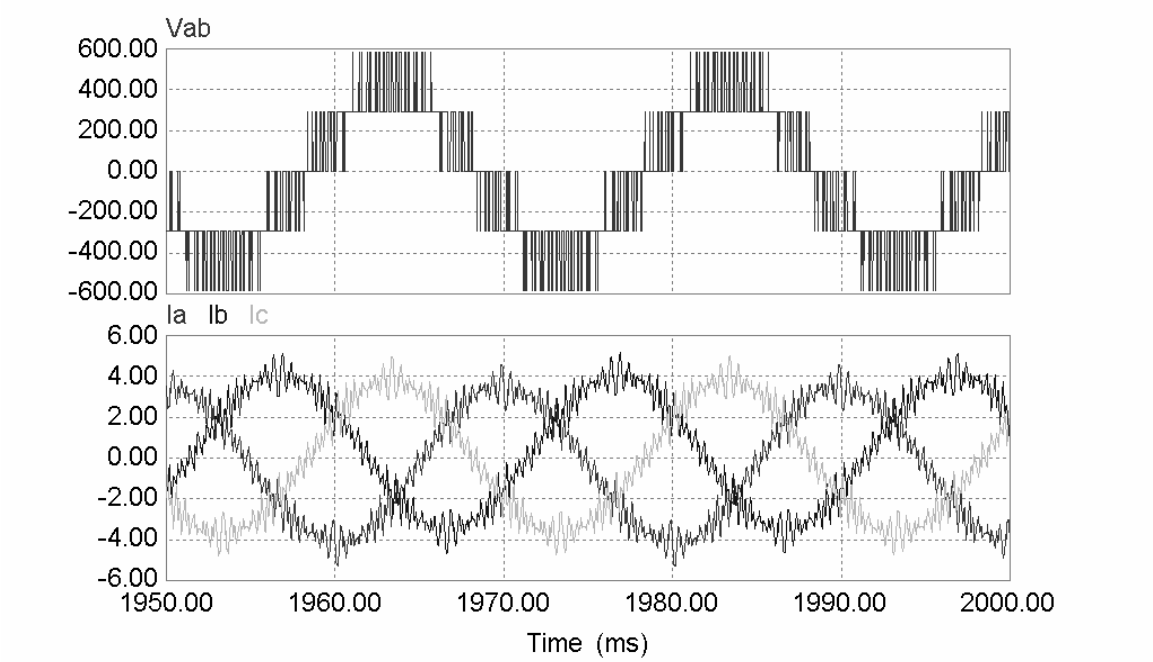


Fig.5.5 Expanded waveforms of line voltage and line currents for SPWM Simulation, Vab = Line Voltage, Ia, Ib, Ic = Line Current

5.3 SIMULATION OF NPC THREE-LEVEL INVERTER USING SVPWM

SVPWM simulation has been carried out using PSIM and Visual C/C++ software. The programming of SVPWM is done in Visual C/C++. This programming is used in DLL (Dynamic Link Library) block of PSIM. Algorithm of generation of SVPWM signals has been discussed.

5.3.1 ALGORITHM FOR GENERATION OF SPACE VECTOR PWM SIGNALS FOR THREE-LEVEL INVERTER

The principle of SVPWM method is that the command voltage vector is approximately calculated by using three adjacent vectors. The duration of each voltage vectors obtained by vector calculations;

$$T_a V_a + T_b V_b + T_c V_c = Ts V^* \quad (5.1)$$

$$T_a + T_b + T_c = Ts \quad (5.2)$$

Where V_a, V_b, and V_c are vectors that define the triangle region in which V* is located. T_a, T_b and T_c are the corresponding vector durations and Ts is the sampling time.

In a three-level inverter similar to a two-level inverter, each space vector diagram is divided into 6 sectors. For simplicity here only the switching patterns for Sector 1 will be defined so that calculation technique for the other sectors will be similar. Sector 1 is divided into 4 regions as shown in Fig.5.6 where all the possible switching states for each region are given as well. SVPWM for three-level inverters can be implemented by using the steps of sector determination, determination of the region in the sector, calculating the duty cycles, and finding the switching states.

5.3.1.1 Determining the sector

θ_n is calculated and then the sector, in which the command vector V^* is located, is determined as;

If θ_n is between $0° <= \theta_n < 60°$, then V^* will be in Sector 1,

If θ_n is between $60° <= \theta_n < 120°$, then V^* will be in Sector 2,

If θ_n is between $120° <= \theta_n < 180°$, then V^* will be in Sector 3,

If θ_n is between $180° <= \theta_n < 240°$, then V^* will be Sector 4,

If θ_n is between $240° <= \theta_n < 300°$, then V^* will be Sector 5,

If θ_n is between $300° <= \theta_n < 360°$, then V^* will be Sector 6,

5.3.1.2 Determining the Region & Simplified Calculation of Duty Cycles

Taking into account the symmetry of all the sextants, it is interesting to reflect the reference vector into the first sextant in order to reduce the number of relevant regions. Also, the amplitude of the reference vector must be normalized to fit into a diagram in which the triangular regions have unity lengths.

The theoretical maximum length of the normalized reference vector (m_i) is the two-unity value. However, in steady-state conditions, its length is limited to $\sqrt{3}$ due to the fact that longer lengths of this vector will be outside of the vector-diagram hexagon, and thus cannot be generated by modulation. Over modulation is produced if the normalized reference vector assumes lengths longer than $\sqrt{3}$ for some positions of this vector, but it can never be outside of the hexagon.

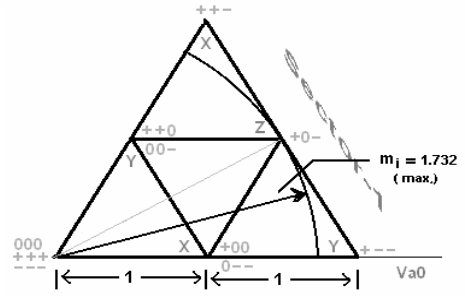


Fig. 5.6 Maximum length of the reference vector in steady-state conditions

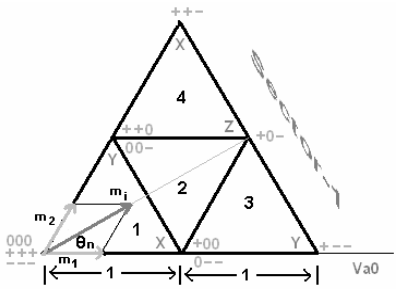


Fig. 5.7 Projections of the normalized reference vector in the region-1

In fig.5.6, the normalized reference vector is decomposed into the axes located at zero and sixty degrees, obtaining projections m_1 and m_2, respectively.

The lengths of the new vectors are determined as follows,

$$m_1 = \left(\sqrt{3}\right) * \left[\cos\theta_n - \frac{\sin\theta_n}{\sqrt{3}}\right] \tag{5.3}$$

$$m_2 = 2 * \sqrt{3} * \frac{\sin\theta_n}{\sqrt{3}} \tag{5.4}$$

In general, these values are the direct duty cycles of the vectors, as in the following,

$$d_{0--/+00} = m_1, \tag{5.6}$$

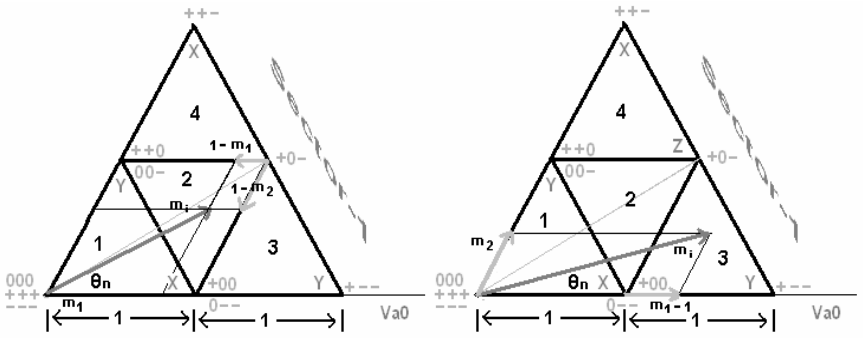
$$d_{00-/++0} = m_2 \text{ and} \tag{5.7}$$

$$d_{+++/000/---} = 1 - m_1 - m_2 \tag{5.8}$$

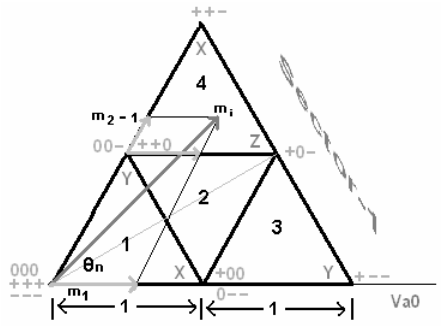
The cases for which the normalized reference vector is located in Regions 2, 3 and 4 are shown in figure 5.8 (a,b,c).

Table-5.1 summarizes the information needed to ascertain the region where the reference vector lies and the duty cycles of the nearest three vectors in the first sector. Same duty cycles can be used for others sectors of stationary vectors.

For all cases, it is assumed that the sum of m_1 and m_2 is not greater than 2. Otherwise, the reference vector would be outside of the hexagon, and thus could not be reproduced by modulation. It is also called over modulation of SVPWM scheme.



(a) Region-2 (b) Region-3



(c) Region-4

Fig. 5.8 Projections of reference vector in Regions – 2, 3 and 4

TABLE-5.1
SUMMARY OF DUTY CYCLES FOR SVPWM SCHEME

Case	Region	Duty Cycles
$m_1 \le 1$ $m_2 \le 1$ $m_1 + m_2 \le 1$	**1**	$d_{0--/+00} = m_1$ $d_{00-/++0} = m_2$ $d_{+++/000/---} = 1 - m_1 - m_2$
$m_1 \le 1$ $m_2 \le 1$ $m_1 + m_2 > 1$	**2**	$d_{0--/+00} = 1 - m_2$ $d_{00-/++0} = 1 - m_1$ $d_{+0-} = m_1 + m_2 - 1$
$m_1 > 1$	**3**	$d_{+--} = m_1 - 1$ $d_{+0-} = m_2$ $d_{0--/+00} = 2 - m_1 - m_2$
$m_2 > 1$	**4**	$d_{+0-} = m_1$ $d_{++-} = m_2 - 1$ $d_{00-/++0} = 2 - m_1 - m_2$

5.3.1.3 Finding the switching states

By considering the switching transition of only one device at any time, the switching orders given below are obtained for each region located in Sector 1 if all switching states in each region are used. Therefore, switching signals for Sector 1are,

Region 1: - ---, 0--, 00-, 000, +00, ++0, +++

Region 2: - 0--, 00-, +0-, +00, ++0

Region 3: - 0--, +--, +0-, +00

Region 4: - 00-, +0-, ++-, ++0

Fig.5.9illustrates direction of the switching sequences for all regions in the sectors.

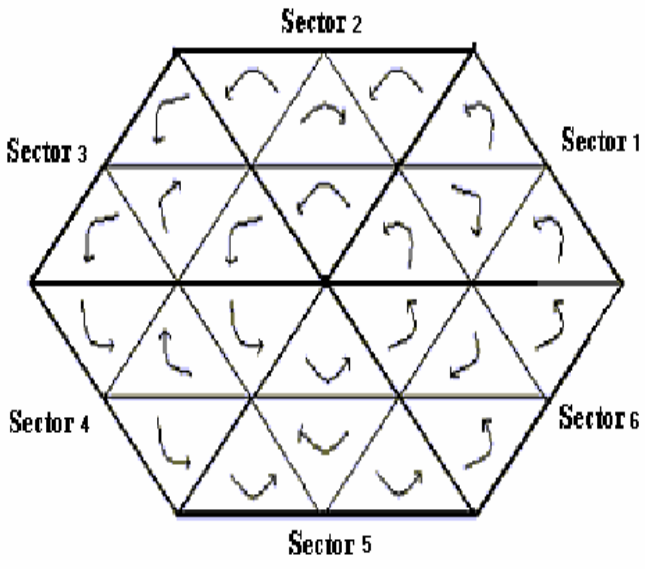


Fig.5.9 Switching sequence for three-level SVPWM inverter

5.2.2 FLOW CHART FOR PROGRAM OF SVPWM

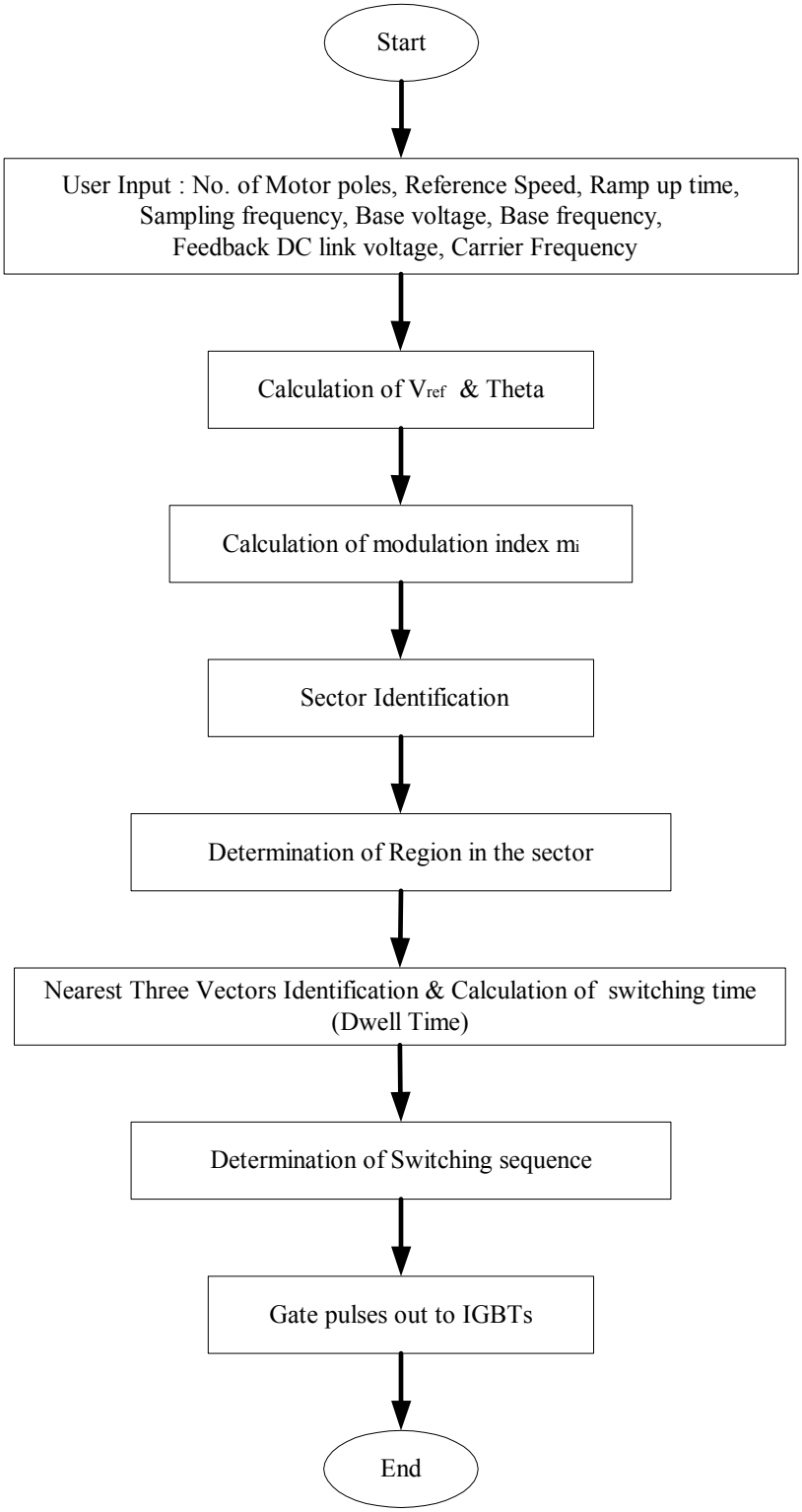


Fig. 5.10 Flow Chart for SVPWM Program

5.2.3 SIMULATION CIRCUIT OF SVPWM FOR NPC INVERTER

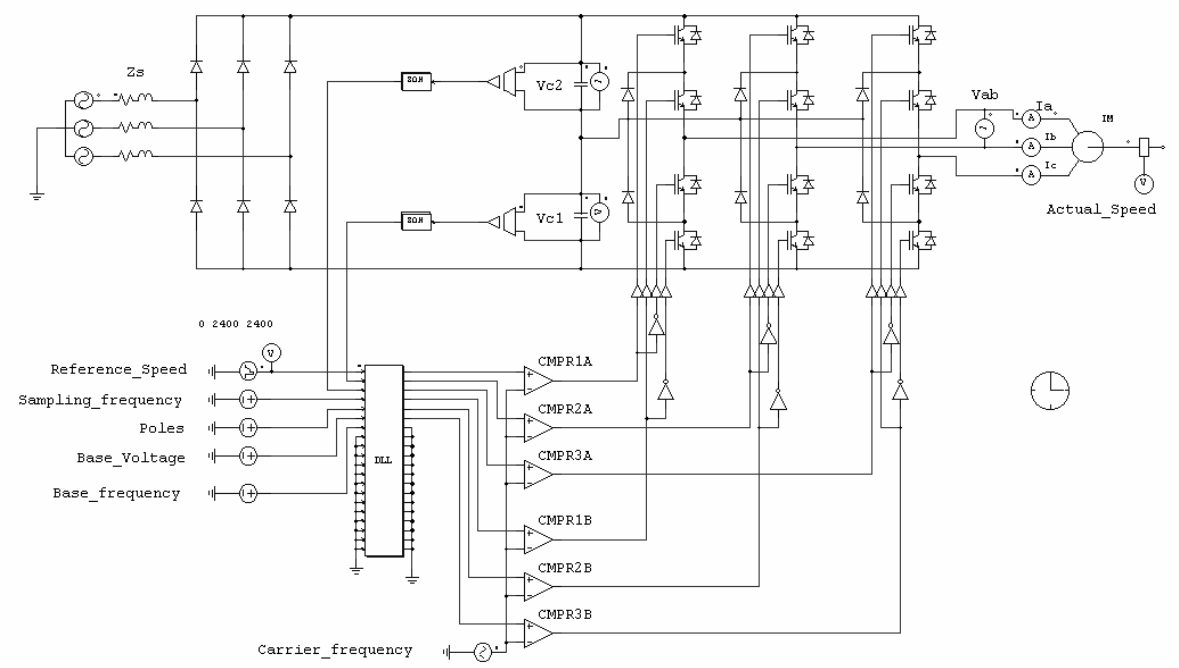


Fig.5.11 Simulation circuit of SVPWM for NPC three-level inverter

The simulation circuit is shown in fig.5.11 using PSIM simulation package. Reference speed, sampling frequency, motor poles, base voltage, base frequency and carrier frequency are input parameters for simulation.

5.2.4 SIMULATION RESULTS OF SVPWM

Induction motor specifications,

Squirrel cage induction motor,

45 kW (60 HP), 415 Volt, 50 Hz,

Rs = 0.07 Ω , Ls = 0.0008 H,

Rr = 0.025 Ω, Lr = 0.0008 H,

Lm = 0.0228 H, Poles = 4,

Moment of inertia = 0.42

Input data for simulation,

Carrier frequency = 2 kHz,

Sampling frequency = 5 kHz,

Ramp Up Time = 3 Sec.

Total Simulation Time = 5 Sec.

Base frequency = 50 Hz,

Base voltage = 415 Volt,

No. of poles = 4,

The proposed scheme is simulated on a 45 kW three-phase induction motor at no load with open loop V/f control for different modulation indices covering the entire speed range. The dc link voltage of around 600 V is used, thus the individual dc link capacitor voltages are kept around 300 V. The carrier frequency used for PWM generation is limited to 2 kHz. The simulation circuit for NPC three-level inverter is shown in fig. 5.11. The open loop dc link capacitor voltage-balancing scheme is implemented using DLL (Dynamic Link Library) block of PSIM simulation software package.

Output frequency can be varied according to the reference speed input in DLL (Dynamic Link Library) block. Base frequency and Base voltage input in DLL block is used to maintain V/f ratio constant. At low frequency the reference vector rotate in region-1 so the two levels in voltage are getting in inverter. In region-1 the use of redundant space (stationary) vector increases in switching pattern, so the difference in capacitor voltages is reduced at low output frequency.

The 3-level SVPWM scheme is used for the PWM signal generation, based on the sampled amplitudes of reference phase voltages. The line voltage, line current and dc link capacitor voltages waveforms for inverter operation in inner layer (two-level) are presented in Figs.5.15 and 5.16.

The line voltage, line current and dc link capacitor voltages waveforms for inverter operation in outer layer (three-level) operation are presented in Figs. 5.12, 5.13 and 5.14. The switching combinations have changed from Positive Small Vector and Negative Small Vector groups to bring back the capacitor voltages to their balanced condition. This proves the operation of the dc link capacitor self-balancing scheme. The maximum difference between capacitors voltage is observed 10 V at 50 Hz frequency as shown in fig.12. At 50 Hz frequency the reference voltage rotates in regions 2, 3 and 4, so the use of redundant vector is less. The simulation results prove the ability of open loop (self balancing) SVPWM scheme.

Input reference speed (1500, 1200, 900, 600, 300 rpm) can be varied to get different output frequency (50, 40, 30, 20, 10 Hz) respectively. Simulation results of line voltage, line current and dc link capacitor voltages are presented.

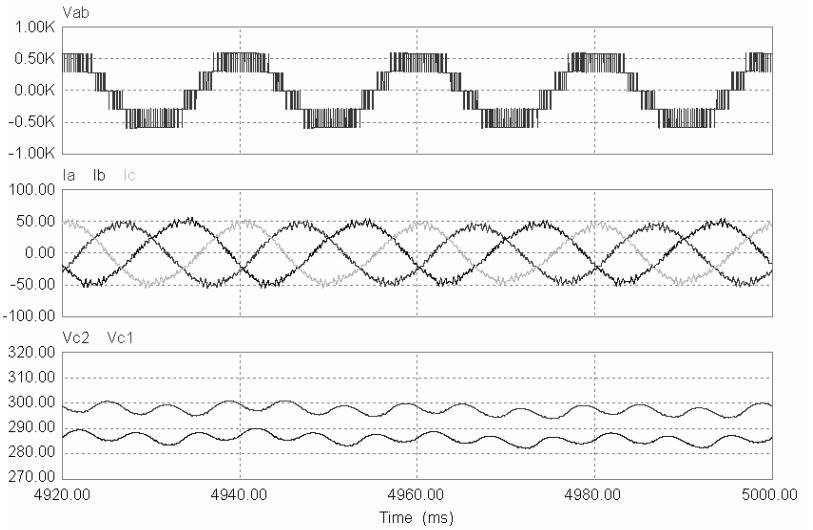


Fig.5.12 Line voltage, Line currents, and DC link capacitor voltages at 50 Hz, mi=1.73
Vab = Line Voltage, Ia, Ib & Ic = Line currents,
Vc2 = Upper Capacitor Voltage, Vc1 = Lower Capacitor Voltage,

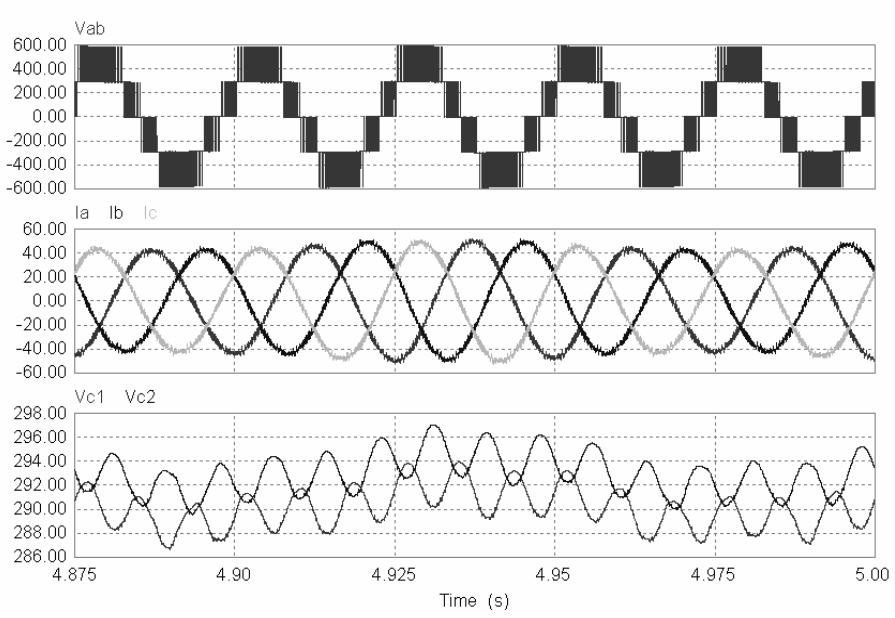


Fig. 5.13 Line voltage, Line currents, and DC link capacitor voltages at 40 Hz, mi=1.38
Vab = Line Voltage, Ia, Ib & Ic = Line currents,
Vc2 = Upper Capacitor Voltage, Vc1 = Lower Capacitor Voltage,

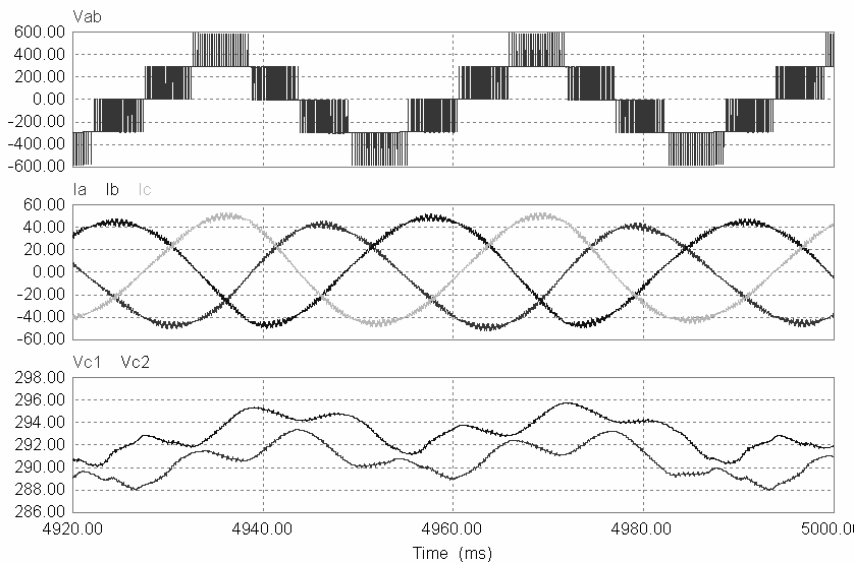


Fig. 5.14 Line voltage, Line currents, and DC link capacitor voltages at 30 Hz, mi=1.03
Vab = Line Voltage, Ia, Ib & Ic = Line currents,
Vc2 = Upper Capacitor Voltage, Vc1 = Lower Capacitor Voltage,

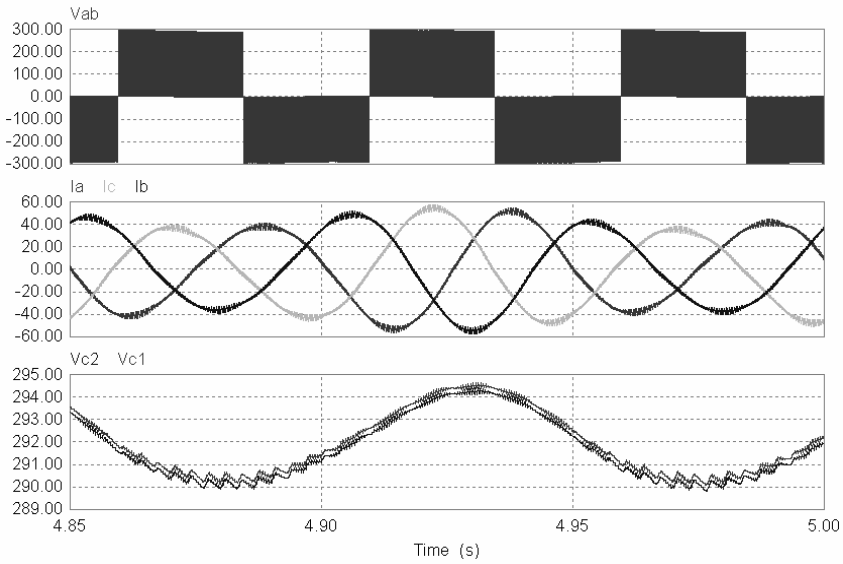


Fig. 5.15 Line voltage, Line currents, and DC link capacitor voltages at 20 Hz, mi=0.69
Vab = Line Voltage, Ia, Ib & Ic = Line currents,
Vc2 = Upper Capacitor Voltage, Vc1 = Lower Capacitor Voltage,

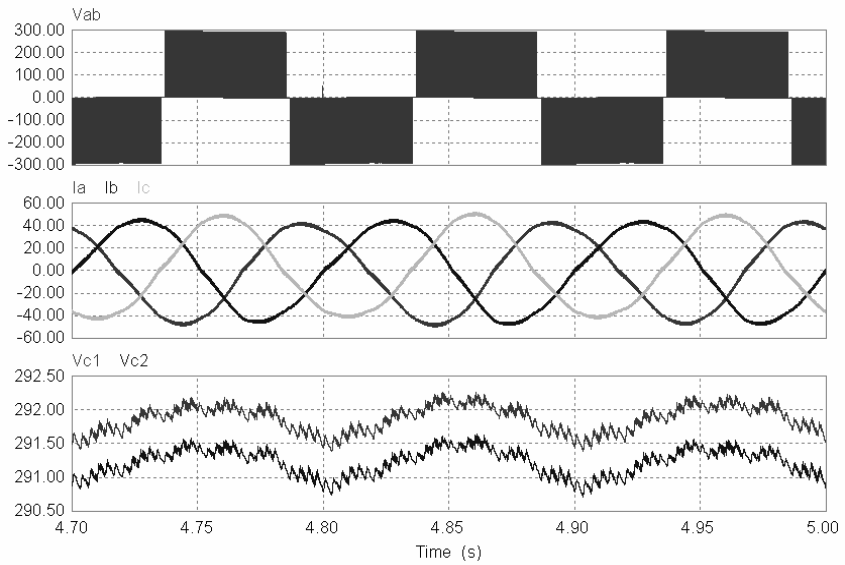


Fig. 5.16 Line voltage, Line currents, and DC link capacitor voltages at 10 Hz, mi=0.34
Vab = Line Voltage, Ia, Ib & Ic = Line currents,
Vc2 = Upper Capacitor Voltage, Vc1 = Lower Capacitor Voltage,

CHAPTER-6
VERIFICATION OF SVPWM ALGORITHM

6.1 GENERAL

This chapter presents the verification of SVPWM algorithm using simulation and DSP-TMS320F2811 control card. The reference generated by SVPWM algorithm is third order harmonics injected in sine wave with fundamental frequency [26]. The triangular carrier wave compared with this reference and PWM pulses developed for IGBTs. Using R-C low pass filter at PWM output in simulation and control card, the SVPWM algorithm is verified. The SVPWM algorithm is also verified using code composer studio (CCS). Code composer studio is software package from Texas Instrument (TI) for conversion of C code into hex code for DSP.

6.2 VERIFICATION OF SVPWM ALGORITHM USING PSIM

The Program of SVPWM is loaded in DLL (Dynamic Link Library) block in PSIM and verified. The fundamental frequency and the third order harmonic are inherently generated by the space vector method, are clearly shown in fig.6.1. As expected, the three phase waveforms are shifted from one another by 120 degrees [13].

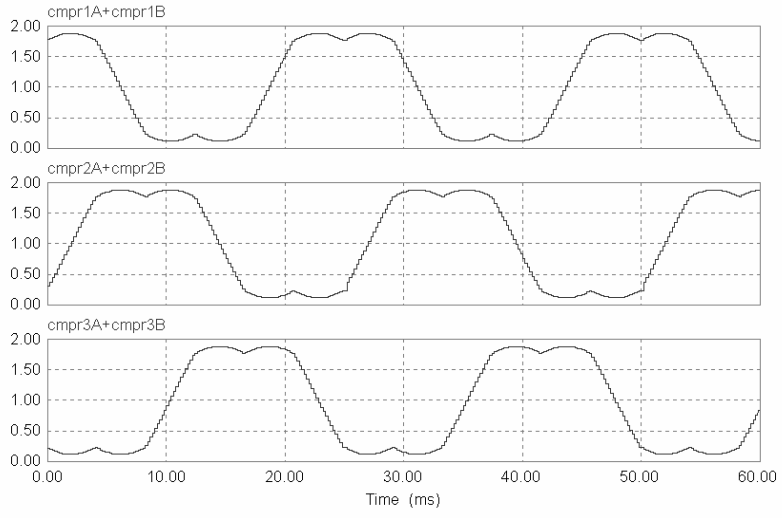


Fig.6.1 Simulation Waveforms of (cmpr1A+ cmpr1B), (cmpr2A+ cmpr2B) and (cmpr3A+ cmpr3B)

6.3 VERIFICATION OF SVPWM ALGORITHM USING CODE COMPOSER STUDIO AND DSP CONTROL CARD

The Program of SVPWM is loaded in DSP-TMS320F2811 Control Card and verified in code composer studio using Graphical Display. The fundamental frequency and the third order harmonic are inherently generated by the space vector method, are clearly shown in below figures. As expected, the three phase waveforms are shifted from one another by 120 degrees [13]. The CCS waveforms are shown in figures 6.2, 6.3 and 6.4. These waves are same as PSIM waveforms shown in fig.6.1. So simulation results are matched with practical results, which verify the SVPWM algorithm.

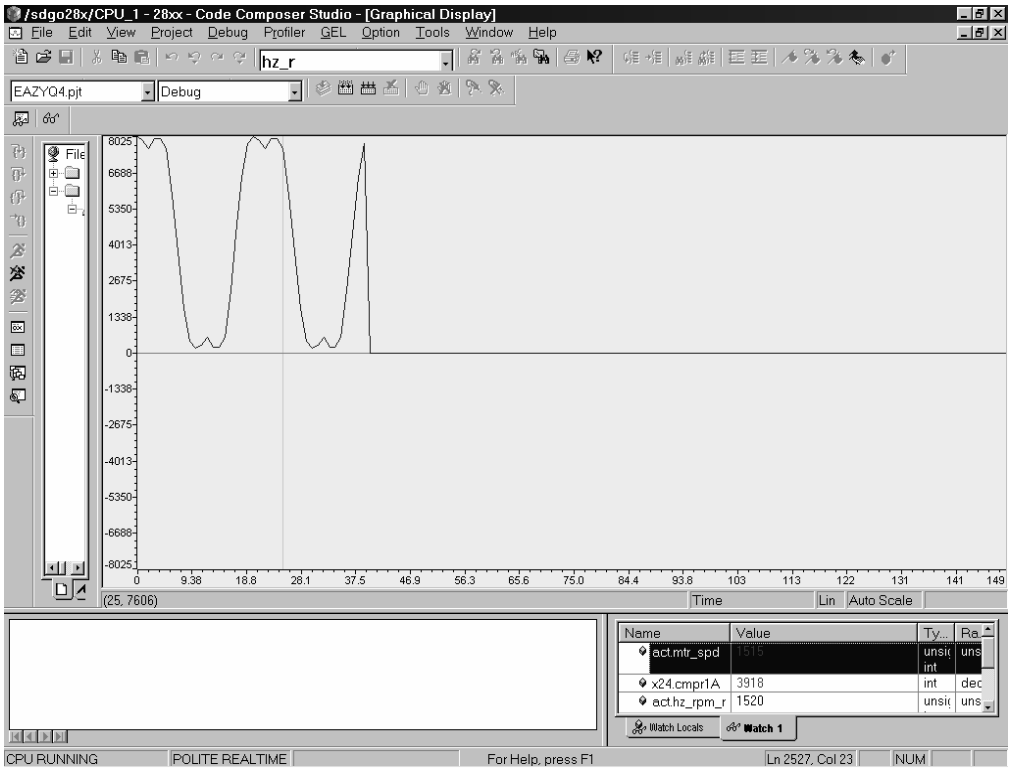


Fig.6.2 Code Composer Studio waveform of (cmpr1A+ cmpr1B)

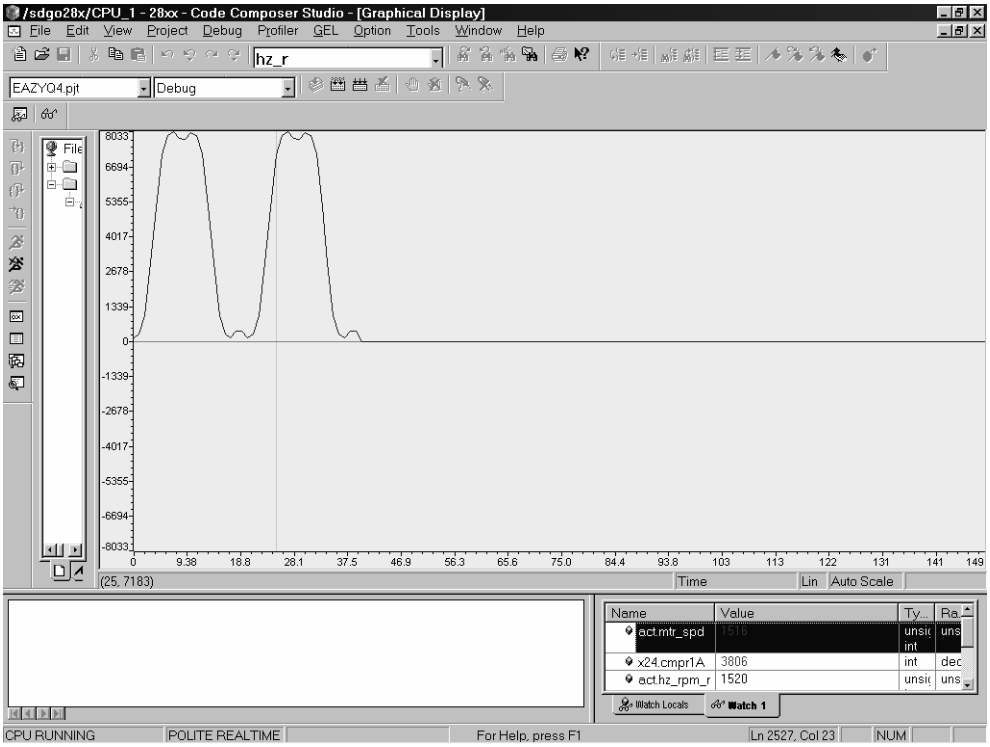


Fig.6.3 Code Composer Studio waveform of (cmpr2A+ cmpr2B)

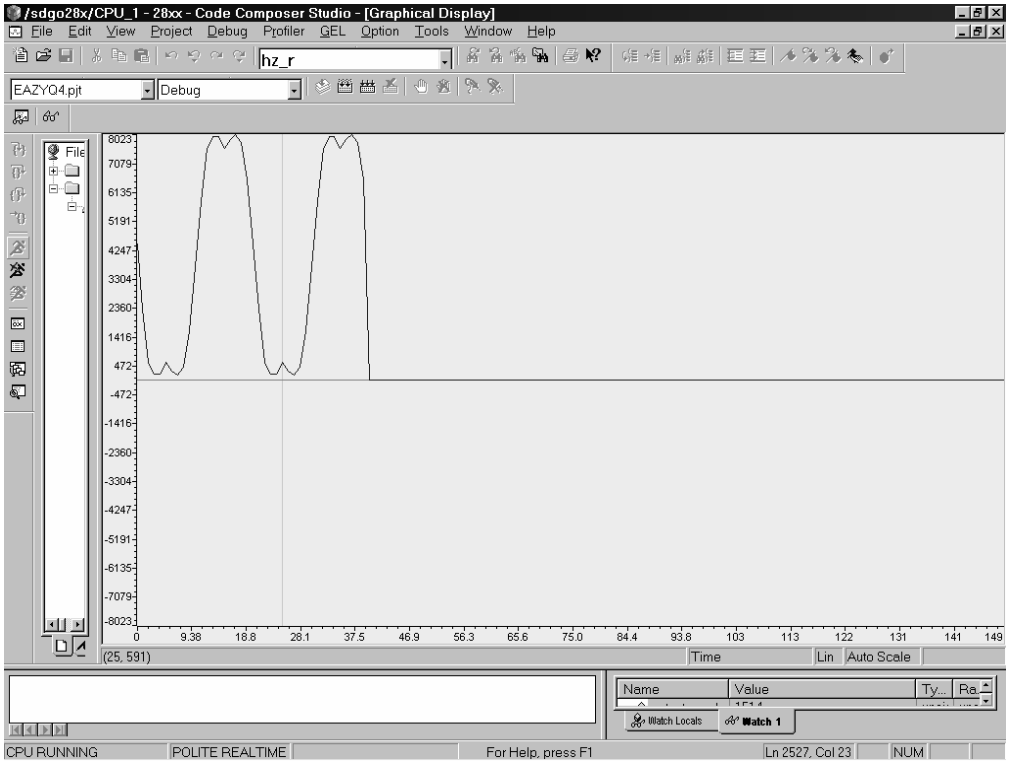


Fig.6.4 Code Composer Studio waveform of (cmpr3A+ cmpr3B)

6.3 VERIFICATION OF SVPWM ALGORITHM USING R-C LOW PASS FILTER

The reference wave cannot be seen at output of DSP control card. So to see the reference wave, R-C low pass filters have been used at the output of DSP control card. The SVPWM Algorithm is verified on PSIM using R-C low pass filter for Three Level Inverter. It is also verified on DSP-TMS320F2811 Control Card using R-C low pass filter for Three Level Inverter. The Simulation circuit with R-C low pass filter shown in fig.6.5. The value of R and C taken as, R = 1.2 kΩ, C = 0.1 μF.

The output results of control card have been taken on Scope as shown in fig.6.6. The fundamental frequency and the third order harmonic are inherently generated by the space vector method, are clearly shown in below figures 6.7 and 6.8. The results are same by PSIM and DSP control card. The Simulation and Practical results have been verified the SVPWM algorithm.

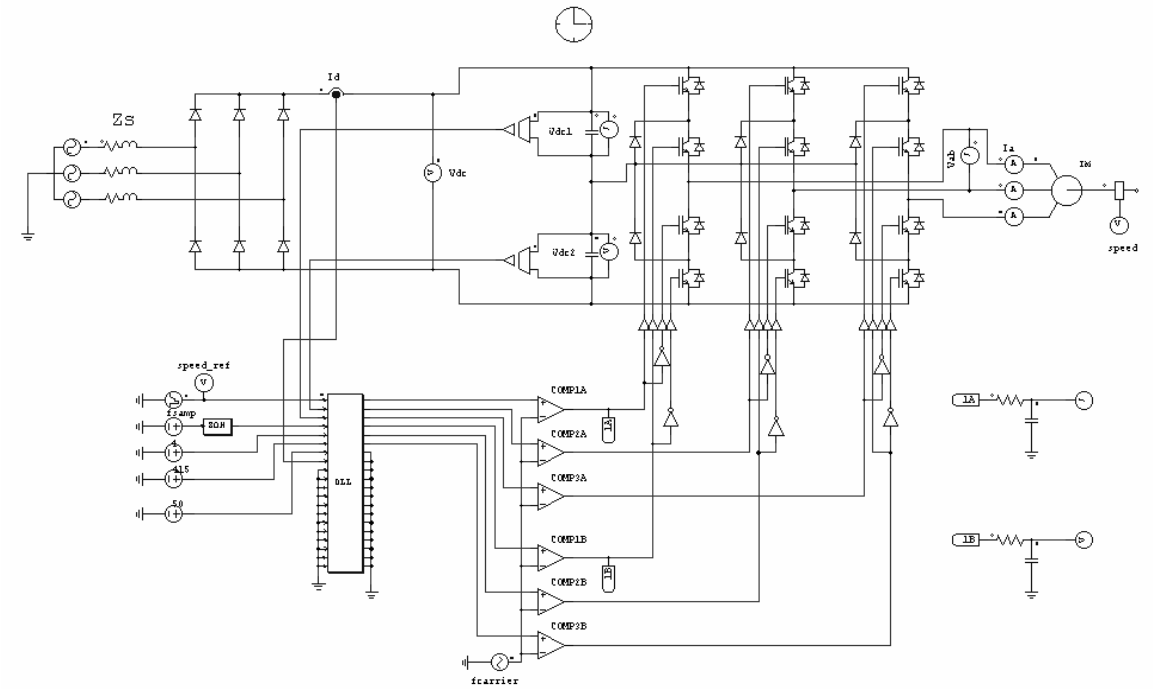


Fig. 6.5 Simulation circuit of SVPWM algorithm with R-C low pass filter

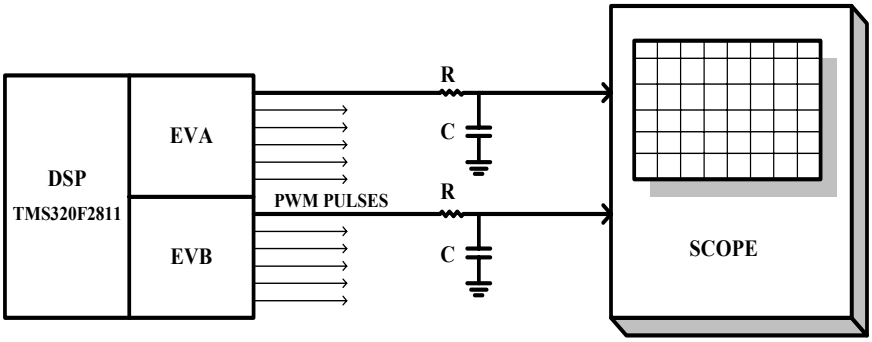


Fig.6.6 DSP TMS320F2811 output PWM pulses with R-C Low Pass filter

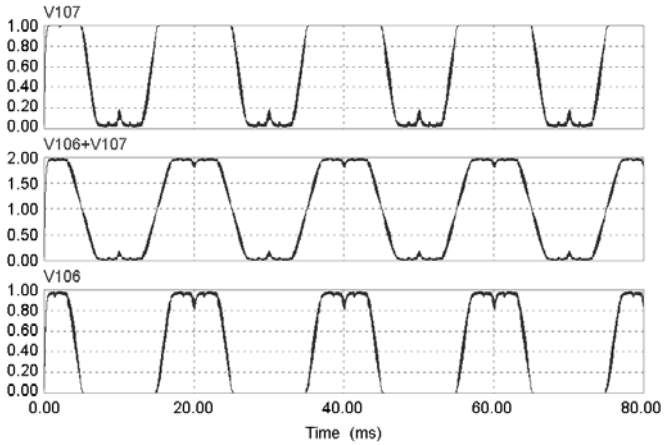


Fig. 6.7 Simulation results of reference waves for SVPWM, V107= cmpr1A and V106=cmpr1B

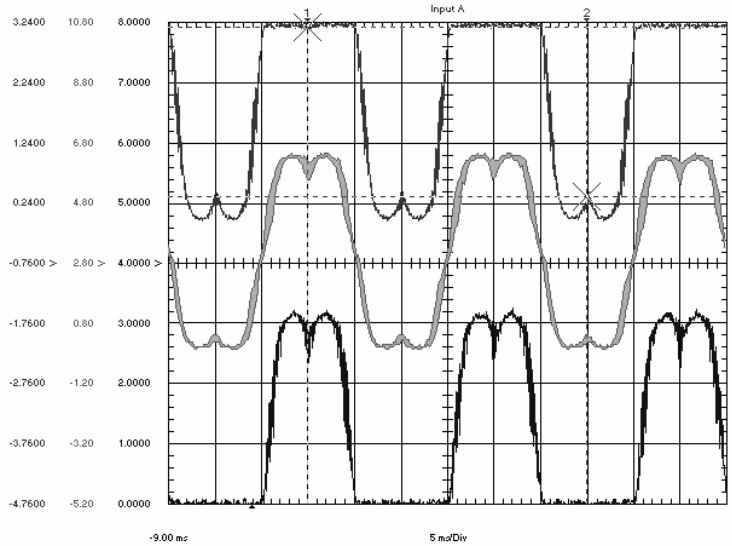


Fig.6.8 DSP control card results on scope for cmpr1A, cmpr1B and (cmpr1A+ cmpr1B)

CHAPTER- 7
DEAD TIME COMPENSATION

7.1 GENERAL

The state of the art in motor control provides an adjustable voltage and frequency to the terminals of the motor through a pulse width modulated (PWM) voltage source inverter drive. As the power devices change switching states, a dead time exists. Although the dead time is short, it causes deviations from the desired fundamental output voltage. While each deviation does not appreciably affect the fundamental voltage, the accumulated deviations result in reduced fundamental output voltage, distorted machine currents, and torque pulsations [23], [24].

Applications will expose the inadequacies of a particular compensation technique. Fractional horsepower drives exhibit dead time-induced instabilities to a lesser extent than integral horsepower drives. Consequently this can lead to a masking of the inherent problems associated with the dead time effect. For example, a dead time compensated ac drive may perform well on a fan or pump application with an induction motor.

This chapter describes a pulse-by-pulse compensation technique that adjusts the symmetric PWM pulses to correct for the voltage distortion due to the dead time effect. The proposed method compensates for the dead time without significant magnitude and phase errors in the terminal voltage of the PWM voltage source inverters. The technique is evaluated through experimental results.

7.2 VOLTAGE DEVIATIONS DUE TO DEAD TIME EFFECT

7.2.1 DEAD TIME EFFECTS

When ac induction, synchronous reluctance, or synchronous pm motors are operated using open-loop adjustable frequency drives, system instabilities may occur for certain frequency ranges and loading conditions. The cause of these instabilities can be inherent low-frequency motor instabilities, instability due to the interaction between the motor and the PWM inverter, or the choice of PWM strategy.

When the voltage source inverter feeds the ac induction motor, the applied stator voltage waveforms contain harmonics generated by the PWM algorithm. The system stability will be affected by these harmonics, especially at low frequencies and no load conditions, causing additional machine losses and reduced efficiency. The magnitude of these losses will depend on the magnitude of the harmonic content in the applied voltage and are compounded by induced harmonics. Excessive harmonics will increase motor heating and torque pulsations. Even the smallest of harmonics as a percent of the fundamental, when coupled with the motor, can result in unstable operation. The choice of the PWM strategy is then important to minimize the voltage and current harmonics. Defects in the PWM strategy will result in voltage deviations at the motor terminals and will be intensified by the addition of the inverter dead time.

The use of fast switching devices in the inverter such as IGBTs or MOSFETs, which use high carrier frequencies (2K to 10K hertz) with lower dead time values (in the area of 2 to 5 microseconds), will not rid the system of instability problems. Higher carrier frequencies improve waveform quality by raising the order of principle harmonics; but low frequency sub harmonics may persist in the output voltage due to the dead time, thus producing beat components and oscillations.

7.2.2 PULSE DEVIATIONS

The effects of the dead time on the output voltage can best be examined from one phase of the PWM inverter. The basic single leg three-level inverter configuration is shown in Fig.7.1 consists of upper power devices S1 and S2, lower power devices S1' and S2' and reverse recovery diodes D1, D2, D3 and D4, connected between the positive and negative rails of the power supply. Commutation of the power devices comes from the PWM generator, which creates the complimentary base drive signals. Output terminal a is connected to motor phase a and the current ia is positive with respect to the motor.

Examining the power device switching sequence as S1 is turning OFF and S1' turning ON, or S1' is turning OFF and S1 turning ON, there exists a time when both power devices cease to conduct. The dead time exists also between S2 and S2'. During the dead time output a appears to be floating, but the current ia must conduct through reverse recovery diodes D1, D2, D3 and D4. Depending on the motor current polarity, the reference voltage may be delayed by the dead time.

Consider the four possible commutation sequences. In the first condition, the current ia is positive. S1 transitions from ON to OFF and S1' from OFF to ON. S2 transitions from ON to OFF and S2' from OFF to ON. During the dead zone, D3 and D4 conducts and diode D1 and D2 blocks the flow of current to the positive rail. This condition results in the correct voltage applied to the motor terminals.

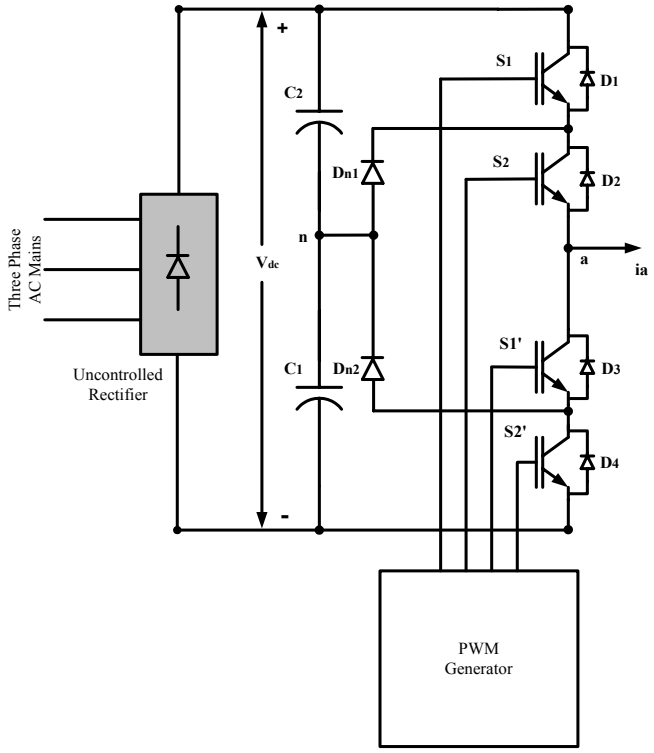


Fig.7.1 Single leg representation of three-level inverter

In the second condition, the current ia is positive, S1 transitions from OFF to ON and S1' from ON to OFF and S2 transitions from OFF to ON and S2' from ON to OFF. During the dead zone, D3 and D4 conducts and diode D1 and D2 blocks the flow of current to the positive rail. Current conducts in D3 and D4 until the dead time elapses, then S1 and S2 turns ON. This condition results in a loss of voltage at the motor terminals.

In the third condition, the current ia is negative, S1 transitions from OFF to ON and Sa' from ON to OFF and S2 transitions from OFF to ON and S2' from ON to OFF. During the dead zone, D1 and D2 continue conduction and D3 and D4 blocks the flow of current to the negative rail. This condition results in the correct voltage applied to the motor terminals.

For the fourth condition, the current ia is negative. S1 transitions from ON to OFF and S1' from OFF to ON and S2 transitions from ON to OFF and S2' from OFF to ON . During the dead zone, D1 and D2 continue conduction and D3 and D4 blocks the flow of current to the negative rail. Current conducts in D1 and D2 until the dead time elapses, then S1' and S2' turns ON. This condition results in a gain in voltage at the motor terminals. All conditions are summarized in Table-7.1.

TABLE-7.1
EFFECT OF DEAD TIME ON MOTOR TERMINAL VOLTAGE FOR DIFFERENT CONDITIONS

Condition No.	Motor Current Ia	Switch S1	Switch S1'	Switch S2	Switch S2'	Diode D1	Diode D2	Diode D3	Diode D4	Effect on motor terminal voltage
1	Positive	ON to OFF	OFF to ON	ON to OFF	OFF to ON	Blocks	Blocks	Conducts	Conducts	Correct
2	Positive	OFF to ON	ON to OFF	OFF to ON	ON to OFF	Blocks	Blocks	Conducts	Conducts	Loss
3	Negative	OFF to ON	ON to OFF	OFF to ON	ON to OFF	Conducts	Conducts	Blocks	Blocks	Correct
4	Negative	ON to OFF	OFF to ON	ON to OFF	OFF to ON	Conducts	Conducts	Blocks	Blocks	Gain

Fig.7.2 shows the effect of dead time on hypothetical pulse times for power devices S1 and S1'. Trace 7.2a and 7.2b are the ideal pulse times; if applied, the resulting fundamental voltage would be of the correct magnitude and phase. In trace 7.2c, S1 transitions from ON to OFF, but there must be a delay time before S1' in trace 4d can turn from OFF to ON. Likewise as S1' in trace 7.2d transitions from ON to OFF, S1 in trace 7.2c must delay before it can turn on.

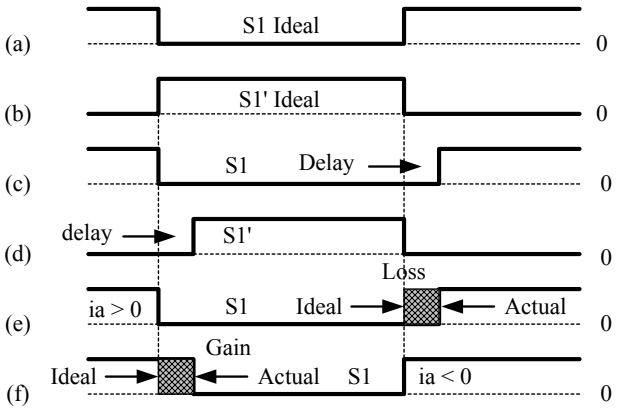


Fig.7.2 Ideal and Corrupted Pulse Patterns for Power Devices Sa and Sa'

Consider ia positive in trace 7.2e, as S1 transitions from ON to OFF, there is no reduction or gain to the pulse time as compared to the ideal pulse time. As S1 transitions

from OFF to ON, the pulse time decreases from the ideal resulting in a deviation to the pulse time and an incorrect fundamental voltage to the load.

When ia is negative as in trace 7.2f, S1 is held on longer than the ideal, resulting in an increase in pulse time, and an incorrect fundamental voltage applied to the load. As S1 transitions from OFF to ON, there is no reduction or gain to the pulse as compared to the ideal pulse. To compensate for the dead time effect, a Pulse Based Dead Time Compensator method has been developed. The Pulse Based Dead Time Compensator method compensates for the pulse deviations due to the dead time effect on a pulse-by-pulse basis. By modifying the switching times to compensate for the dead time effect, the output voltage can be properly controlled in magnitude and phase.

7.3 PULSE BASED METHOD OF CORRECTION

The Pulse Based Dead Time Compensator updates the turn-on time of the power device at the beginning of a PWM cycle and the turn-off time of the device at the midpoint of the PWM cycle by software correction. Correction is based on the polarity of the currents, independent of operating or carrier frequencies.

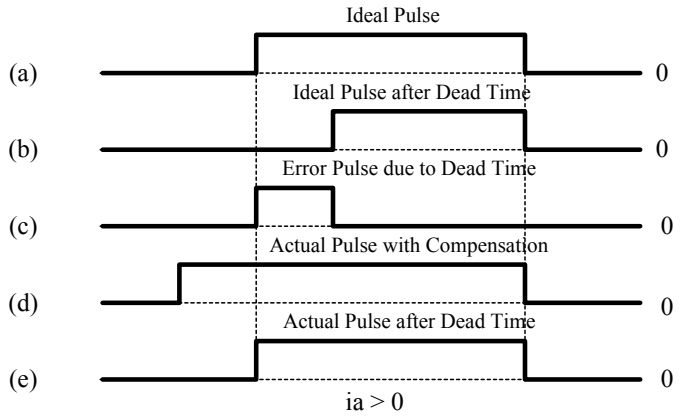


Fig.7.3 Pulse Based Dead Time Compensator for ia > 0

The method does not need current phase detection, thus eliminating the a/d converters and software overhead of other methods. Simple current polarity detectors interfaced to the data bus make it compatible with microprocessor or DSP I/O architecture's, which yields an inexpensive dead time compensator. Fig.7.3 shows the pulse time correction using the Pulse Based Dead Time Compensator for ia > 0. Trace 7.3a is the ideal pulse time for Sa as Sa transitions from OFF to ON and from ON to OFF.

Trace 7.3b shows the pulse after the dead time counter if allowed to be processed by the PWM waveform generator without correction. Trace 7.3c shows the error pulse (7.3a – 7.3b) due to the dead time.

To correct the error, the software algorithm adjusts the pulse time width. For ia > 0, time is added to the pulse before the dead time generator creating an unsymmetrical pulse. The increased pulse time (7.3d), is processed through the dead time counter. The actual pulse (7.3e) is identical to the ideal pulse time (7.3a) in width and position.

Fig.7.4 shows the operation of the Pulse Based Dead Time Compensator for ia < 0. The correction is similar to ia > 0 in Fig.7.4, except time is subtracted from the pulse. Trace 7.4a is the ideal pulse time. Trace 7.4b shows the ideal pulse time after the dead time. Trace 7.4c shows the error pulse (7.4a – 7.4b) due to the dead time. The reduced pulse time (7.4d) is processed through the dead time counter. The actual pulse (7.4e) is identical to the ideal pulse time (7.4a) in width and position.

The Pulse Based Dead Time Compensator uses a minimal amount of software code space as compared to other techniques, which require angle calculations to determine the proper magnitude and phase of the corrected voltage command. This advantage allows the user more processor power for other control functions. The Pulse Based Method offers the ability to modify the switching dead times to account for dissimilar turn-on and turn-off characteristics of the power devices, thus eliminating the need for power device measurements.

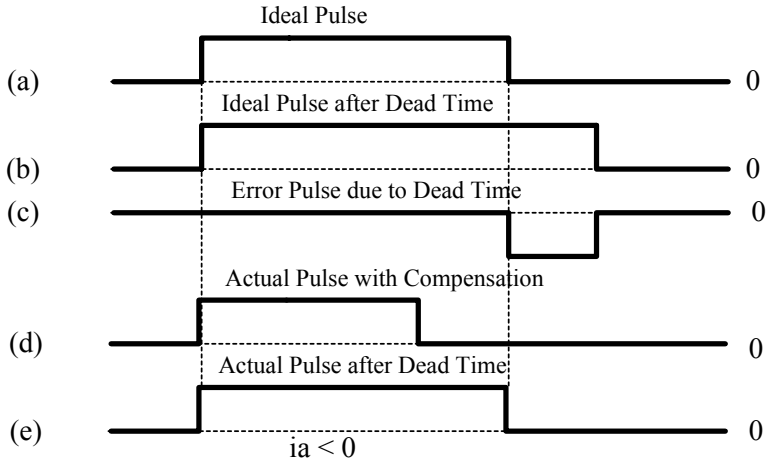


Fig.7.4 Pulse Based Dead Time Compensator for ia < 0

7.4 IMPLEMENTATION OF PULSE BASED DEAD TIME COMPENSATION METHOD

The Pulse Based Dead Time Compensator was implemented in a DSP TMS320F2811, which includes an internal PWM waveform generator. Compensation for the dead time effects is accomplished by adjusting the pulse times of the waveform generator to correct for the gain or loss of pulse time. The method is independent of operating and carrier frequency, but dependent on current polarity.

Fig. 7.5 shows the reduced block diagram of the Pulse Based Dead Time Compensation. For simplicity, discussion will be limited to the u phase switching signal generation. Decisions for correction are based on current polarity at the beginning of each PWM period.

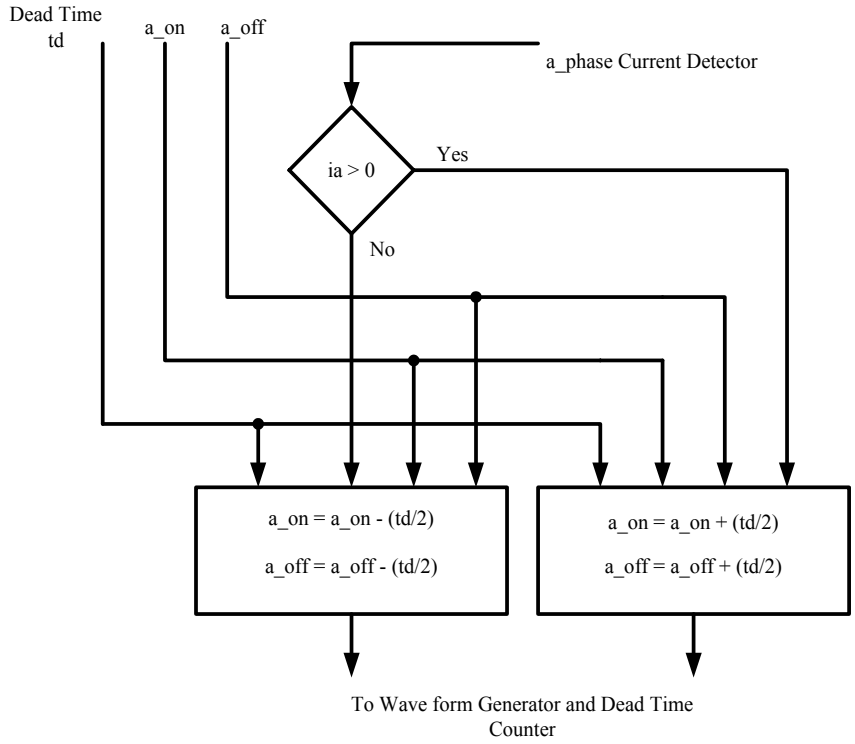


Fig.7.5 Flowchart of Carrier Rate Pulse Based Dead Time Compensation using DSP TMS320F2811

The software algorithm generates the ideal a_phase pulse times, a_on and a_off, for the desired operating point. a_on and a_off are stored in the compensation software routine. The predetermined dead time value is loaded into the dead time control register

of the waveform generator. Because it restricts pulse times to symmetrical center aligned methods, only one-half the dead time value is stored in the compensation software routine. The a_phase current detector continuously updates current polarity information via the DSP data bus. An interrupt signal is sent to the compensation software at the beginning of each PWM period.

If ia > 0, the compensation software adds one-half the dead time to a_on and a_off increasing the pulse time, and the corrected value is stored in a_on and a_off. The corrected a_on and a_off are sent to the waveform generator and the dead time counter. The corrected pulse time is processed through the dead time counter, but the resultant pulse position is shifted by one-half the dead time. If ia < 0, the compensation software subtracts one-half the dead time from a_on and a_off decreasing the pulse time. The correction is then the same as for ia > 0.

The position shift in the Pulse Based method is enough to reduce the applied fundamental voltage and induce instabilities in low impedance and high voltage motors.

7.5 EFFECT OF DEAD TIME COMPENSATION AT LOW FREQUENCY IN TLI

The effect of dead time compensation at 15 Hz on motor current can be seen from below figs. 7.6 and 7.7. Without dead time compensation the motor current is distorted. Pulse based dead time compensation method gives better results in motor current.

The Pulse Based Dead Time Compensation method applies the correct fundamental voltage to the motor terminals. The motor current is stable with the correct no load flux current for the 60 HP, 415 V ac induction machine. The steady state waveform is excellent due to pulse based dead time compensation. More experimental results of three-level and two-level inverter for dead time compensation are discussed in chapter-9.

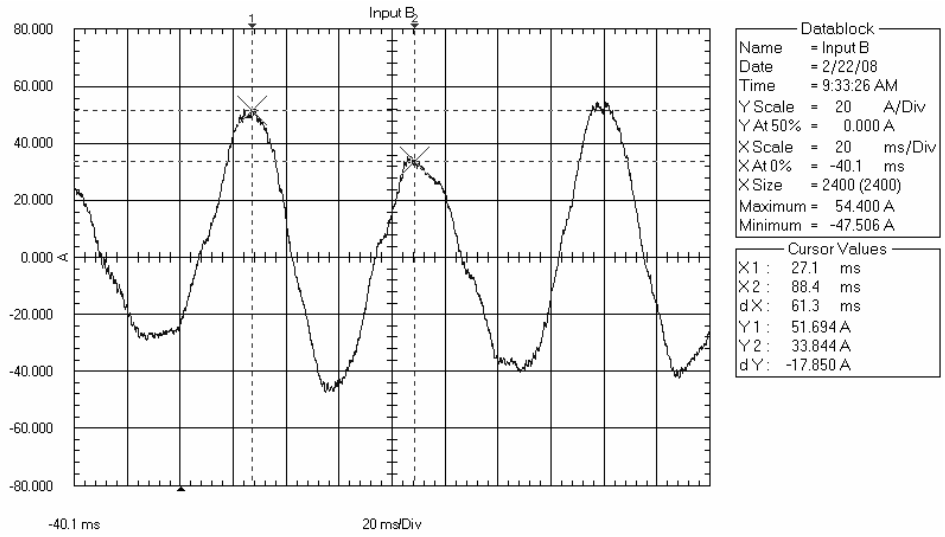


Fig.7.6 Line Current Waveform at 15 Hz, DTC Gain = 0
(Without Dead Time Compensation) (X- axis: 1 div = 20 ms, Y- axis: 1 div= 20 A)

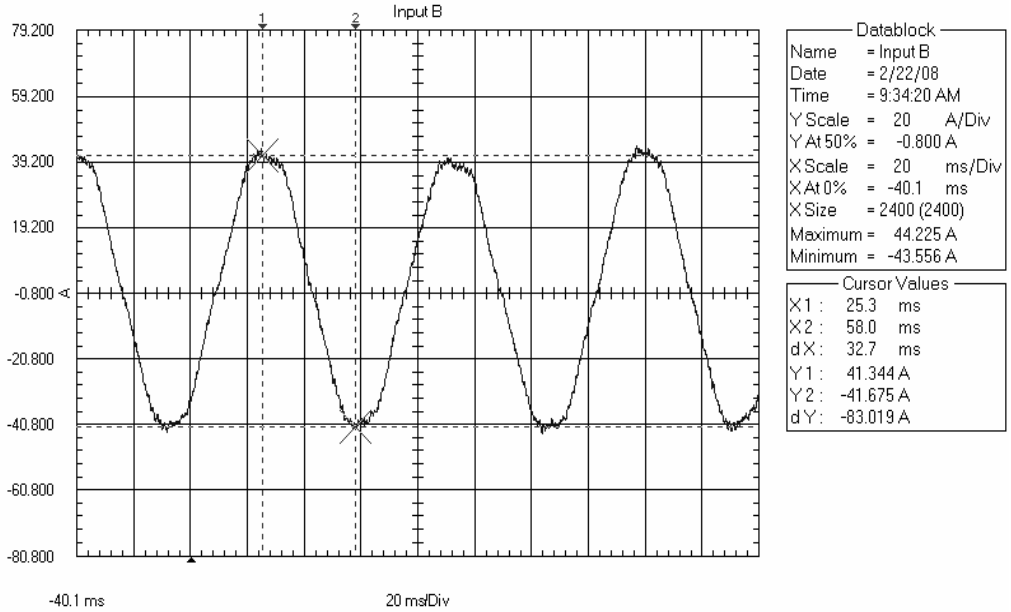


Fig.7.7 Line Current Waveform at 15 Hz, DTC Gain=110,
(With Dead Time Compensation) (X- axis: 1 div = 20 ms, Y- axis: 1 div= 20 A)

CHAPTER-8
DESIGN OF THREE LEVEL NPC INVERTER

8.1 GENERAL

Design of three-level inverter is divided into two parts. One is hardware design and other is software design. Hardware design include component-rating selection, control card and power circuit. Software design includes the various controlling algorithms to control NPC three-level inverter operations.

This chapter provides the basic block diagram showing the hardware and control card interfacing. Further the hardware design and software design has been discussed in detail. Component selection like DC link capacitor and IGBTs has been discussed. Control card to control the three-level inverter operation, driver card used for turn on of IGBTs, display software used for observing various quantities and changing the maximum value and hardware setup for prototype testing have been discussed in detail. Various control algorithms like core algorithm, soft-charge of DC link during the starting of three-level inverter, overload protection algorithm for protecting the TLI from overload have been discussed in detail for proper under standing.

8.2 BASIC BLOCK DIAGRAM

Fig. 8.1 shows the single line block diagram of TLI. Main hardware design is associated with the heat sink for IGBTs, DC link capacitance, IGBT gate driver circuit, sandwich layer for DC link and current sensors. Major part is software design, which involves various processes described in detail in following section.

DSP performing the every controlling process required to control the switching action, gating pulse generation, harmonic reference current generation, DC link stabilization, Soft-charge of DC link during turn on process and generation of turn off pulse for protection during the faulty condition. DSP requires various feedback signals for performing the above-mentioned actions as shown in the fig. 8.1. DC link voltage, input voltage and output current are sensed and feed back to control card. The rest of the algorithm within the DSP performing the required action to be taken for proper working

of the TLI and generates the required pulses like PWM gating pulse, soft-charge pulse and shut down pulse. For cooling of heat sink fan is required. The rating of fan is 230 V single phase ac. At the drive input three phase ac supply is available. So step down transformer is used to convert 415 V to 230 V as shown in fig.8.1. This 230 V supply is also used for supply of contactor coil, which is used for soft charging of capacitor bank. SMPS is used for the stable dc supply of +24 V, +15 V, +5 V and -15 V for DSP control card. Two IGBT gate driver cards are used for twelve IGBT gate pulses come out from EVA and EVB of DSP as shown in fig.8.1.

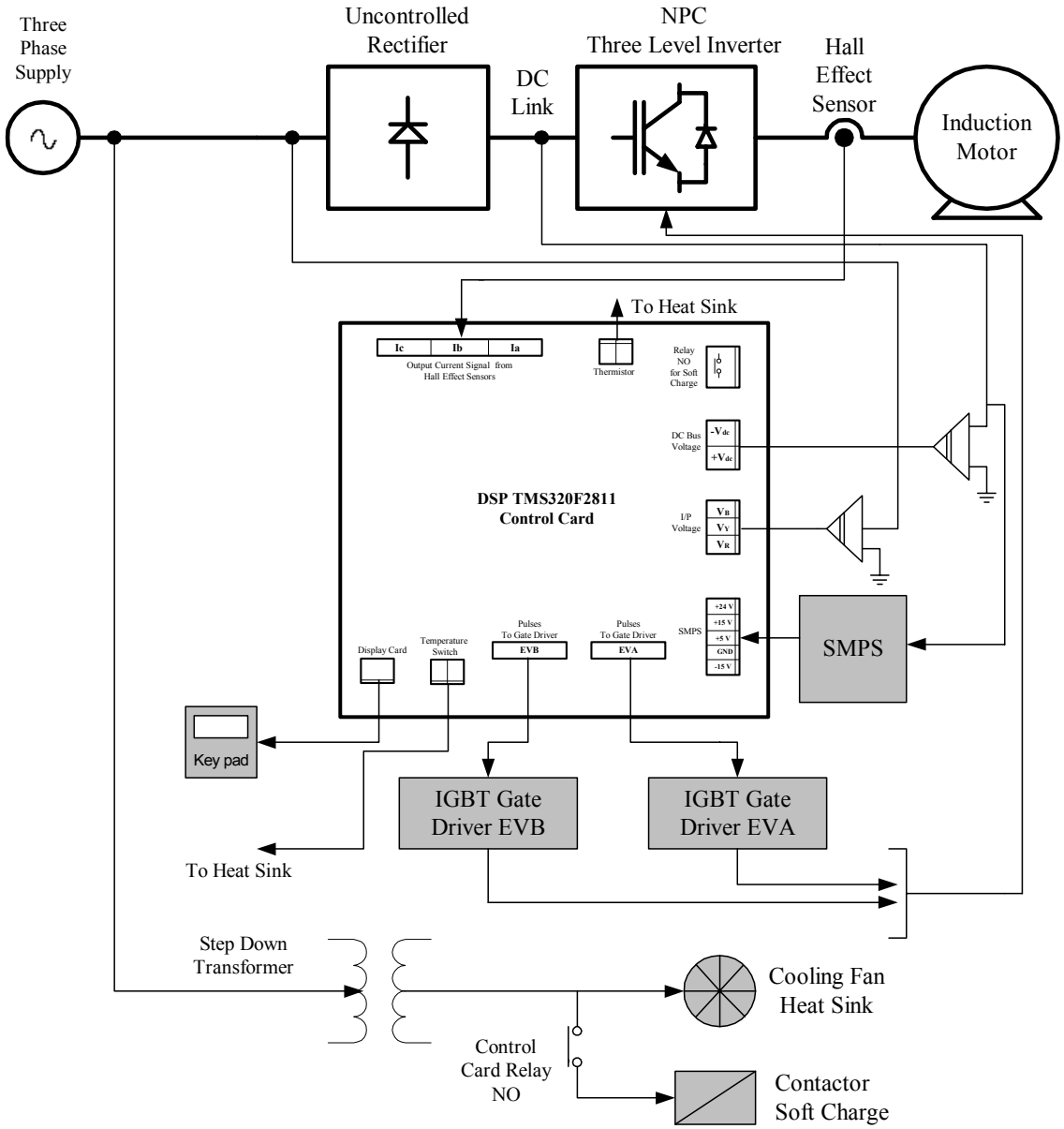


Fig. 8.1 Single line block diagram of three-level inverter illustrating the hardware modules required

10 kΩ thermister has been used for monitoring heat sink temperature. Thermister is placed on the heat sink. If temperature is increased more than 87 ºC, the control card will stop the three-level inverter drive. Temperature switch is also used for back up protection of over temperature. Keypad with display is used for changing input parameters and for monitoring of various parameters of TLI.

8.3 HARDWARE DESIGN

Hardware design is one of the most important criteria in any project. Each and every component requires the special attention according to the required rating of the model. To design the three-level inverter following designing criteria should be keep in mind.

8.3.1 COMPONENT RATING

8.3.1.1 Bus-Bar

Generally the rating of three-level inverter is expressed in terms of power and voltage. The power rating of inverter is 45 kW and voltage rating is 415 V. It can run motor of 45 kW with full load current of 87 A. So the bus-bar design should be adequate for current of 87 A. Copper bus bar is selected for the three-level inverter. For positive and negative dc links sandwiched copper plates have been used to minimize inductance and its boost effect at high switching frequency.

8.3.1.2 Dc Link Capacitor

The choice of the DC capacitor is an important criterion. A small DC capacitor value may result in large ripple during transient states. Whereas on the contrary, although a high DC capacitor value may reduce the ripples, cost and size may become an issue in justifying its use. Using following equation (8.1) capacitance can be selected for dc link capacitors.

$$\Delta vc = \frac{1}{C}\int i_2\,dt \tag{8.1}$$

Where, C = Capacitance

i_2 = Load current

Δvc = Change in capacitor voltage

Voltage rating of capacitors is selected form the dc link voltage to be used for three-level inverter. Capacitors voltage rating is 400 V and capacitance is 4700 μF have been selected for the three-level inverter.

8.3.1.3. Rating of IGBT

The selection of IGBT rating is one of the most important design aspects. The current rating of the IGBT should be 1.5 times the full load current capacity. Voltage rating of IGBT can be selection on the basis of the supply voltage and ultimately based on the maximum allowable DC link voltage. CM200DY12NF Mitsubishi Japan IGBT has been used for this project. IGBT current rating is 200 A and voltage rating is 600 V.

8.3.1.3. Rating of Clamping Diode

Fast recovery diode has been used as clamping diode. The full load 87 A current will pass through the diode. So the IGBT's inbuilt diode has been used for the three-level inverter. The gate and emitter terminals of IGBT have to short to use IGBT's inbuilt diode.

8.4 HARDWARE DESCRIPTION

8.4.1 CONTROL CIRCUIT (PCA-2004A)

The main heart of the control signal board PCA-2004A is DSP 'TMS320F2811'. The block diagram of the control signal Board PCA-2004A is shown in fig. 8.2. This card has been used to control the various operations of three-level inverter. The main concern with this card is DSP programming and the interfacing of the card with the Axpert communicator and the keypad. The power supply to the PCA-2004A is provided through an SMPS with voltage input of 600 V dc and output dc of '+24V/0.5Amp', '+15 V/2.2 A', '+5 V/1 A', '0/COM' and '-15 V/0.5 A'. The '3.3 V/1.9 V' supply voltage for the DSP 'TMS320F2811' is regulated with '+5V' input from SMPS. The programming for the DSP 'TMS320F2811' is done in the Code Composer Studio. The program is written in the 'C-Language'. The program is transferred from PC to DSP 'TMS320F2811' from an 'Emulator' through a 'JTAG'.

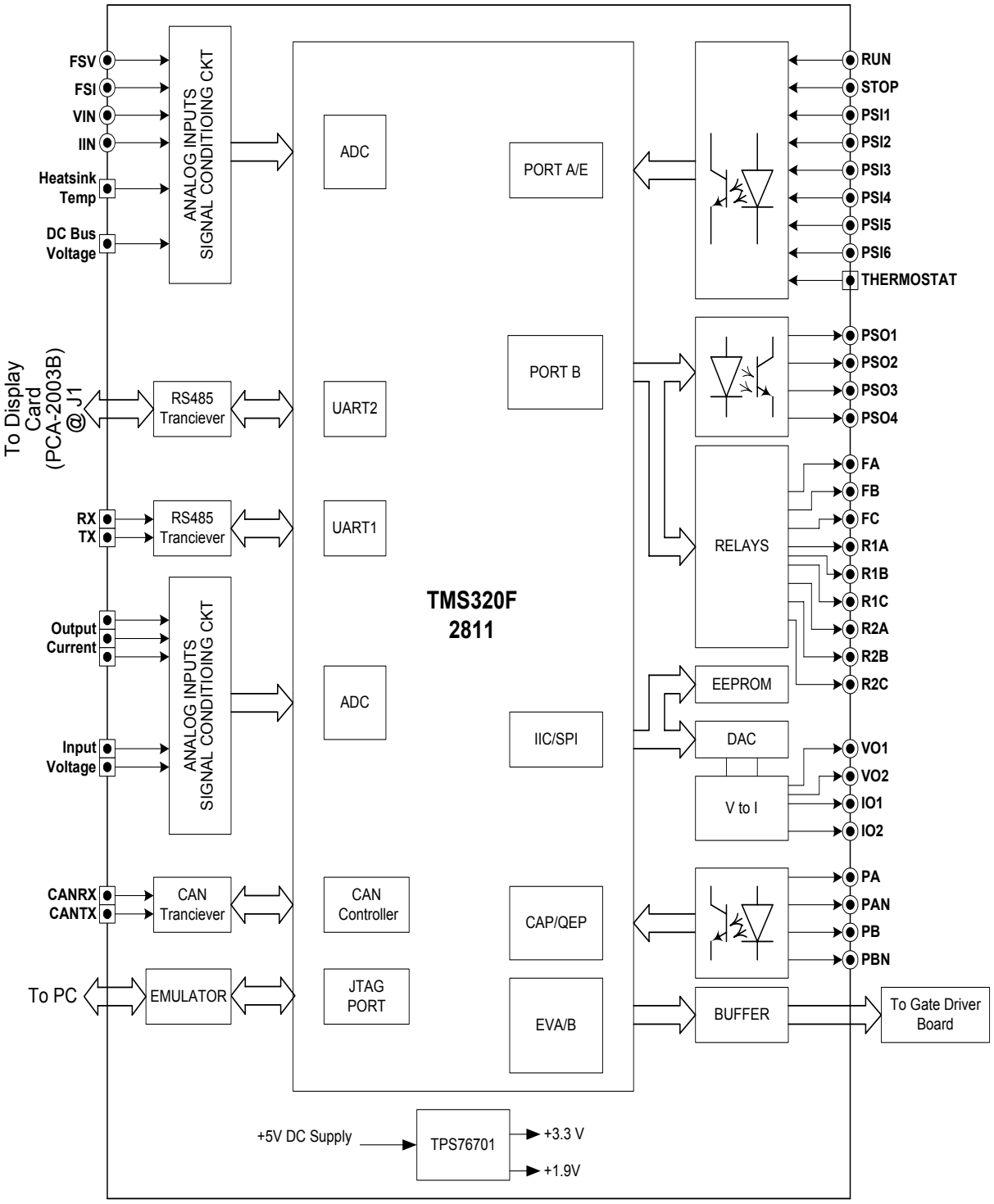


Fig.8.2 Block diagram of control card PCA-2004A

8.2.2 IGBT GATE DRIVER CIRCUIT (PCA-1015)

The Driver card used to drive IGBT is made from the six driver IC made by SHARP. Driver card is designed to convert logic level control signals into optimal IGBT gate drive. Input signals are isolated from the IGBT. It also provides a short circuit protection by monitoring the collector emitter voltage of the IGBT. A collector feedback is taken for this purpose. The driver initiates a controlled slow turn-off and generates a fault signal when a short circuit is detected. The slow turn off helps to control dangerous transient voltages that can occur when high short circuit currents are interrupted. This card allows a faster Turn-Off during normal operation. The output of the driver will remain disabled and the fault signal will remain active for minimum 20μsec (determined by the C) after a short circuit has been detected. The input signal of the driver must be in its off state in order for the fault signal to be reset. In case of the fault both the IGBTs are turned-off immediately and an error signal is fed to the control circuit. In order to achieve efficient and reliable operation of high current, high voltage IGBT modules, gates drive with high pulse current capability and low output impedance is required. The output booster stage is used for this purpose.

8.2.3 DISPLAY

For display of various quantities graphical LCD display has been used. This software has been developed on visual basic. The quantities like output frequency, dc link voltage, input ac voltage, heat sink temperature, and output current have been displayed on keypad. It is easy to change parameter value through this keypad. Dead time compensation gain and switching frequency can be adjusted for proper operation of three-level inverter.

8.5 SOFTWARE DESIGN

The three-level inverter can be controlled with the help of Digital Signal Processor (DSP) due to its high speed of operation. DSP-TMS320F2811 has the Event Manager module in it and it is for the PWM generation. So implementation of PWM operation is easily achieved through processor. The program can write in assembly language or in C language for DSP. C language is well known and it can be easily

implemented. To make the software module for the three-level inverter following modules needs to be made.

- ADC scanning
- Interrupt service routine
- SVPWM algorithm
- PWM gating pulse generation for IGBTs
- DAC if needed

Unlike analog control circuit, digital control has much outstanding advantages, such as reliability and flexibility. However, its performance is likely weakened by time delays and phase shift in the process of signal sampling, conditioning and computing. Elaborate design of digital system is needed to ensure satisfactory dynamic response of the three-level inverter.

The core of the digital controller for three-level inverter is a 32-bits fixed-point DSP (TMS320F2811) operating with a 150 MHz clock [21]. In order to cut down cost, the built-in two independent A/D units of DSPs whose maximum conversion time is not more than 80ns are used for acquisition of the current and voltage. The main role of the DSP is to calculate the reference compensating current according to the algorithm based on the SVPWM.

8.5.1 CORE ALGORITHM

Core algorithm is the heart of three-level inverter control algorithm. The core algorithm is the main routine in which the different control algorithms like SVPWM and DC link stabilization are called. The time required to execute the core algorithm should be less than the sampling time set for the ADC. The core algorithm is depicted in the flowchart shown in fig. 5.9 (in chapter-5) and fig. 8.4.

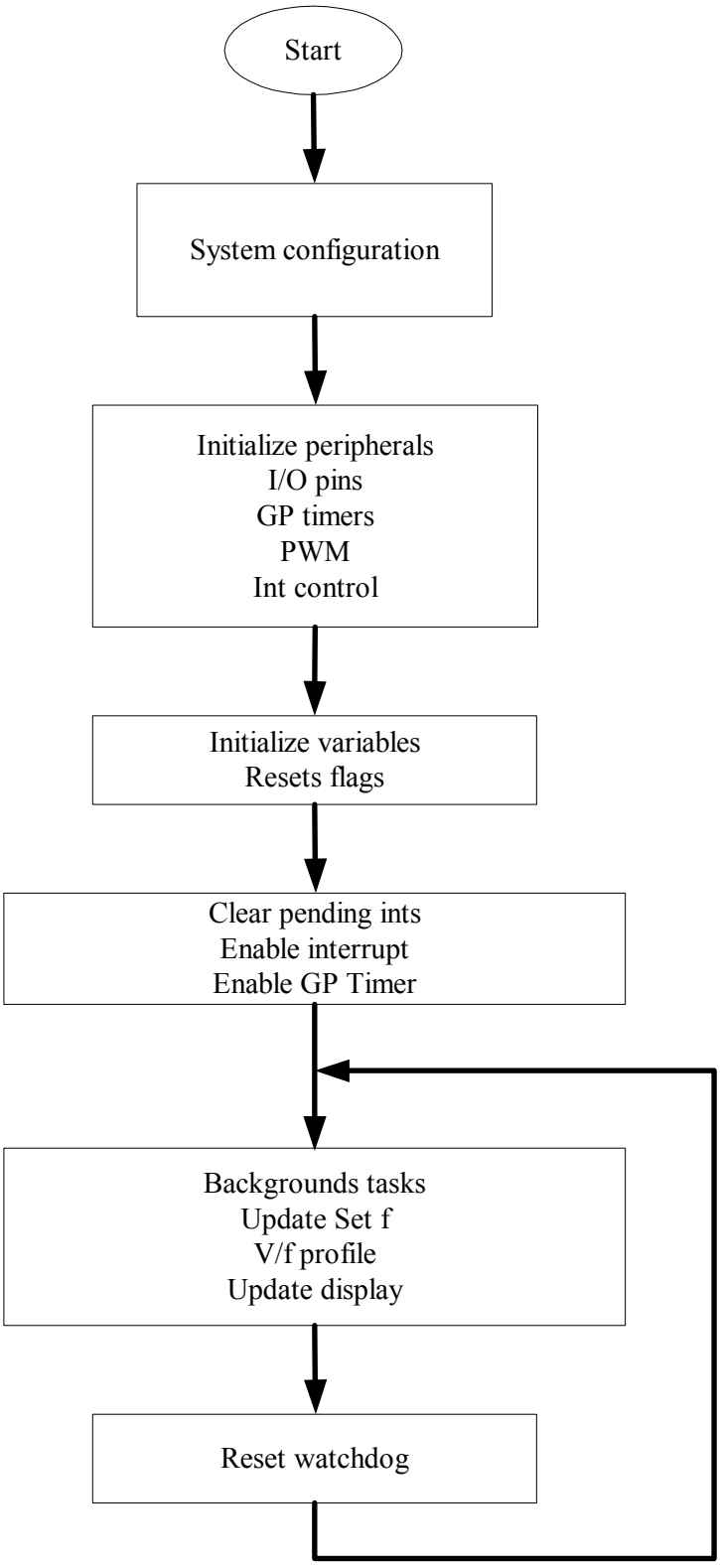


Fig.8.3 Flow chart of core algorithm used for DSP in TLI prototype

8.5.2 SOFT CHARGE ALGORITHM

For proper functioning of the three-level inverter DC link voltage should be equal to the predefined value. During starting of three-level inverter DC link voltage should be charge up to its predefined value (Reference DC link voltage). For this purpose soft-charge algorithm has been used to charge the DC link before turning on the three-level inverter. Figure 8.5 shows the flow chart for Soft-charge of DC link used in three-level inverter.

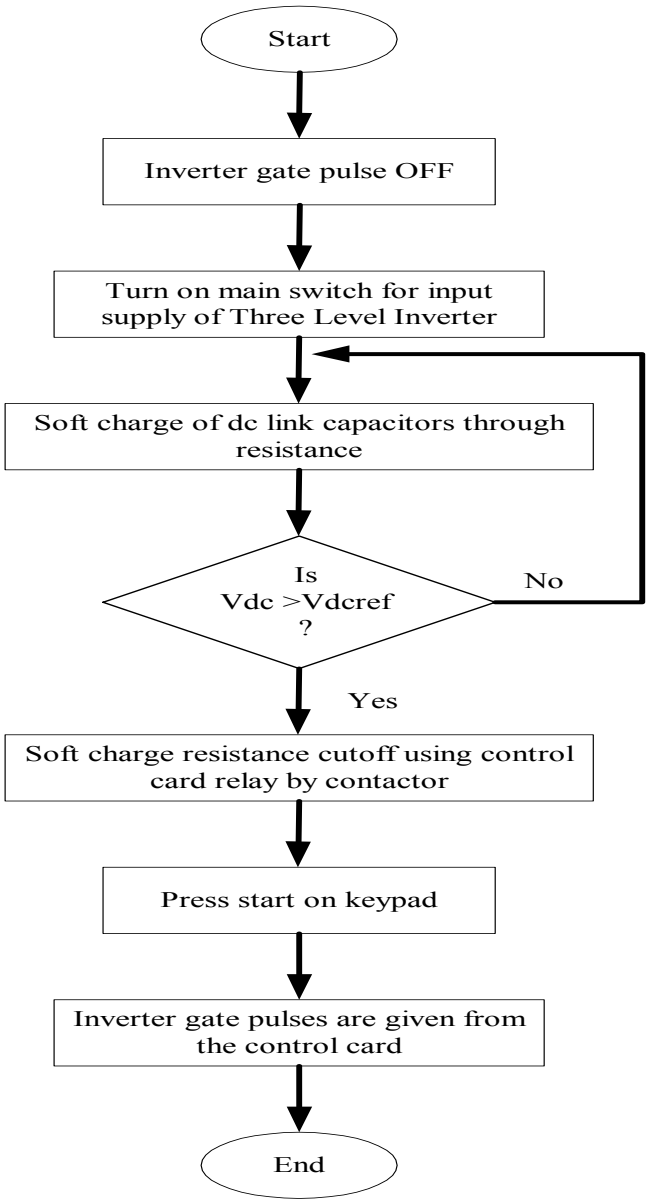


Fig.8.4 Flow chart for Soft-charge of DC link used in TLI prototype

8.5.3 OVER LOAD PROTECTION ALGORITHM

The three-level inverter should be protected against the overload condition. If capacity of three-level inverter 100 Arms and load requires 150 Arms then three-level inverter should be overload and may not work properly. The following flowchart shown in fig. 8.6 can be used to protect three-level inverter from overload condition.

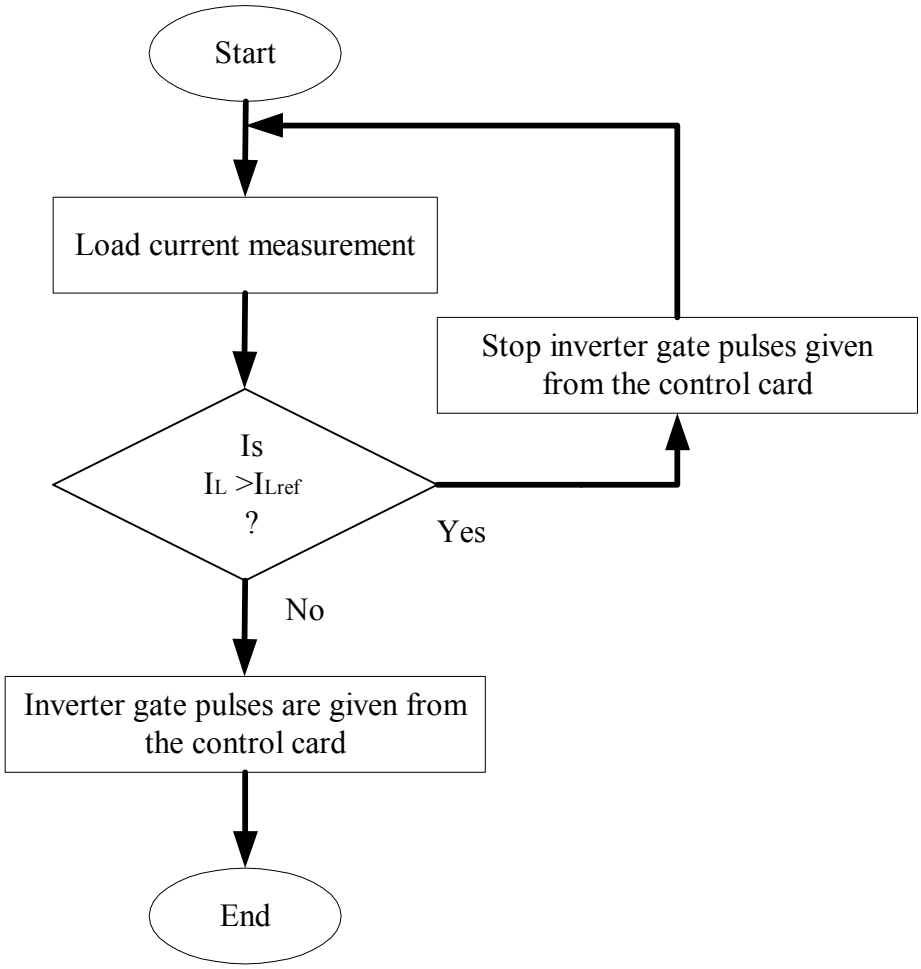


Fig.8.5 Flow chart for protection against overload used in TLI prototype

CHAPTER-9
EXPERIMENTAL RESULTS

9.1 GENERAL

The prototype testing of the three-level inverter has been carried out and the results have been found. Various quantities and waveforms have been observed and recorded for the further analysis. The photographs of prototype test setup are shown in Appendix-A.

The proposed scheme is tested on a 2 HP, 10 HP and 60 HP three-phase induction motor drive with open loop V/f control for different modulation indices covering the entire speed range. The dc link voltage of around 600 V is used, thus the individual dc link capacitor voltages are kept around 300 V. The carrier frequency used for PWM generation is limited to 2 kHz. The open loop dc link capacitor voltage-balancing scheme is implemented using DSP-TMS320F2811 control card. The 3-level SVPWM scheme is used for the PWM signal generation, based on the sampled amplitudes of reference phase voltages. The line voltage and line current waveforms for inverter operation in inner layer (two-level) and outer layer (three-level) operation are presented in Figs. 9.2 and 9.3, respectively. The switching combinations from Positive Small Vector or Negative Small Vector groups to bring back the capacitor voltages to their balanced condition as shown in Fig.9.6. This proves the operation of the dc link capacitor voltage-balancing scheme.

The Results includes Output Line Voltage, Output Line Current, DC Link voltages for no load condition and full load condition of Induction motor in this chapter. Varying Local Set Frequency using Keypad can vary output frequency of Inverter.

9.2 DEAD TIME IMPLEMENTATION

When an ac motor is operated using open loop adjustable frequency drives, system instabilities may occur at certain frequency and under certain loading conditions. The cause of these instabilities can be inherent low frequency motor instabilities, instability due to interaction between the motor and the PWM inverter, or the choice of PWM strategy.

When the voltage source inverter feeds an ac motor, the applied stator voltage waveforms contain harmonics generated by the PWM algorithm. The system stability will be affected by these harmonics, especially at low frequencies and under no load conditions, causing additional machine losses and reduced efficiency. The use of fast switching devices in the inverter such as IGBTs or MOSFETs, which use high carrier frequencies (2KHz to 10KHz) with lower dead time values (2 to 5 micro seconds) will improve the current waveform, but will not rid the system of instability problems. Higher carrier frequency improves the quality of waveform by raising the principal harmonics; but the low frequency sub-harmonics may persist in the output voltage due to the dead time, thus producing beat components and oscillations.

Test result of PWM gate pulses for complimentary switches with dead time is shown in below fig.9.1. The practical result of dead time of 3.2 μsec has been taken.

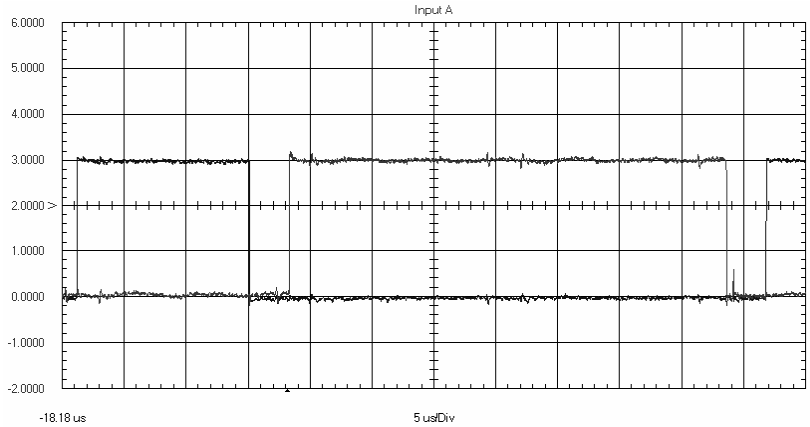


Fig.9.1 DSP control card result of PWM gate pulses for complimentary switches

9.3 RESULTS ON 2 HP INDUCTION MOTOR

The three-level inverter is tested on open circuit. The waveforms of line voltages are observed on scope for different frequencies. Then first three-level inverter prototype is loaded using 2 HP induction motor. The testing waveforms are shown in below figures for different frequencies.

Motor Specification, 2 HP, 2- Pole, 415 V, 50 Hz (With No Load)

Input Parameter By Keypad,

Carrier Frequency = 2 KHz

DTC (Dead Time Compensation) Gain = 70,

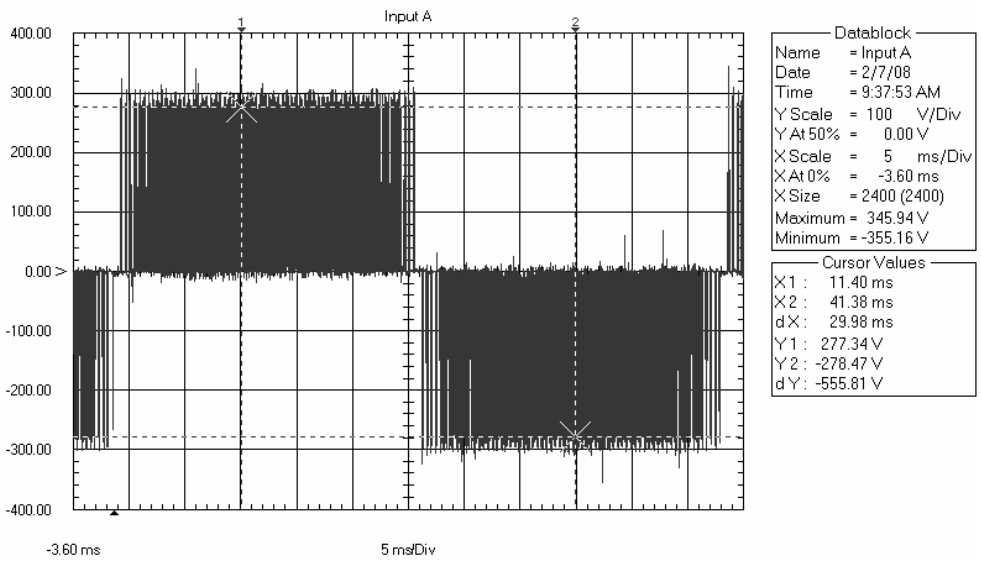


Fig.9.2 Line Voltage waveform at 20 Hz, mi = 0.69,
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 100 V)

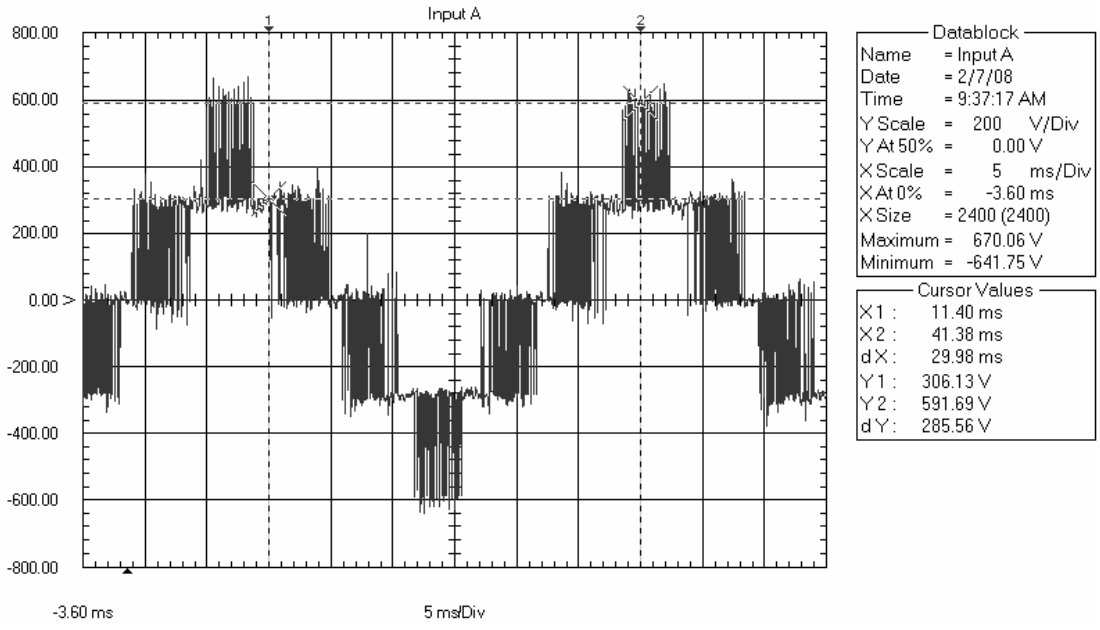


Fig.9.3 Line Voltage waveform at 30 Hz, mi = 1.03,
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 200 V)

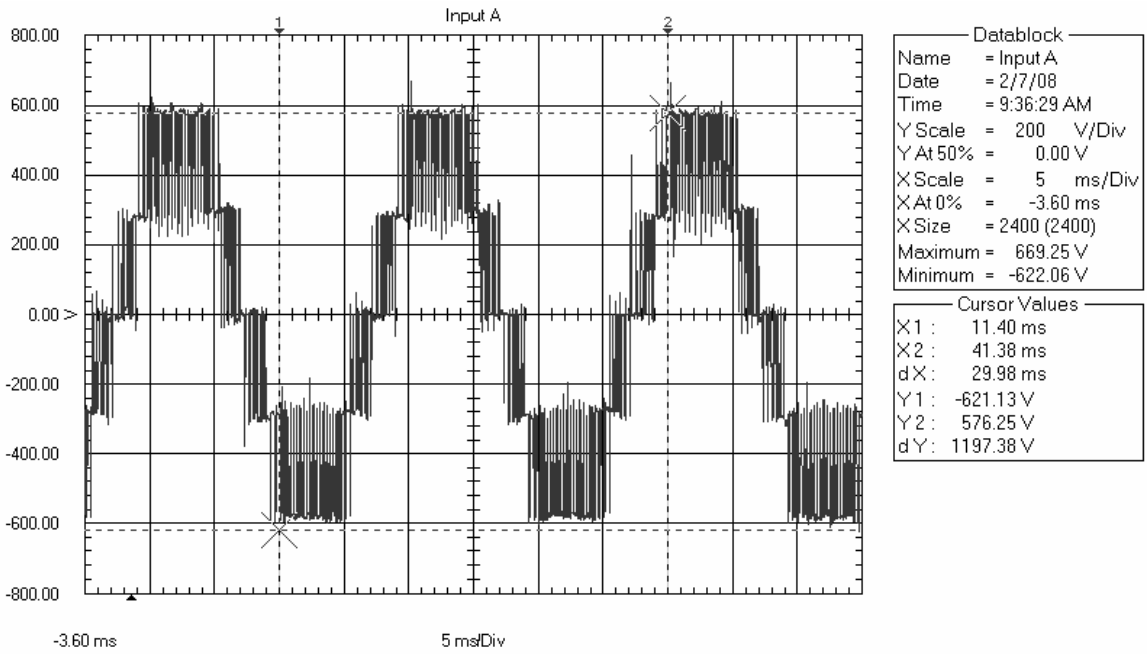


Fig.9.4 Line Voltage waveform at 50 Hz, mi = 1.73,
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 200 V)

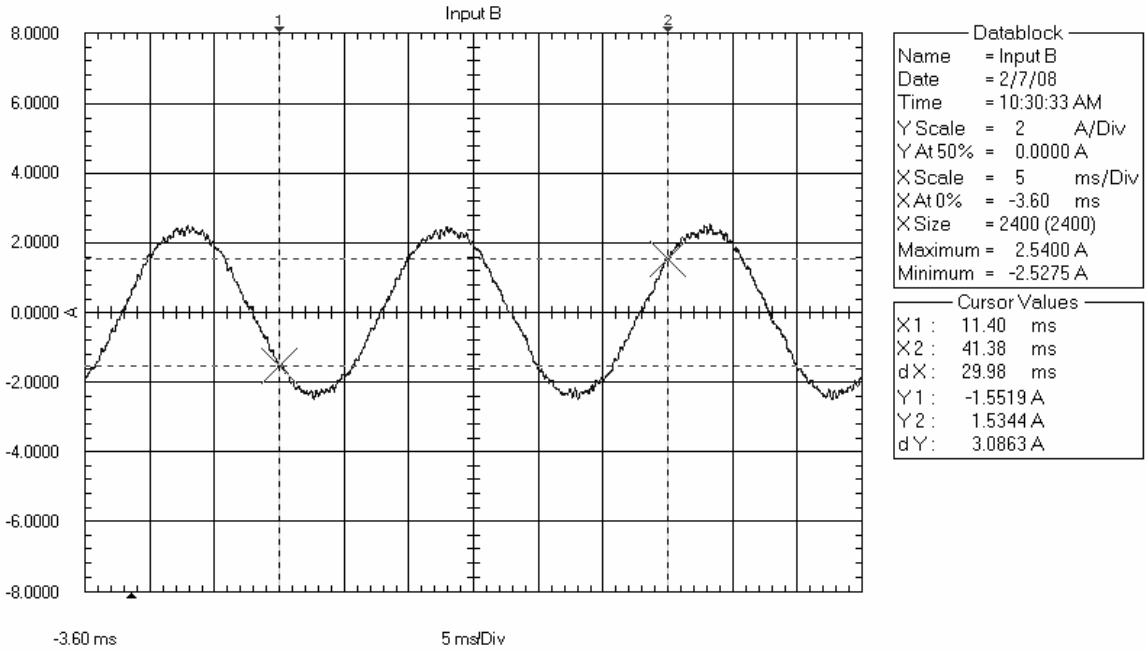


Fig.9.5 Line Current waveform at 50 Hz for 2 HP induction motor, mi = 1.73,
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 2 A)

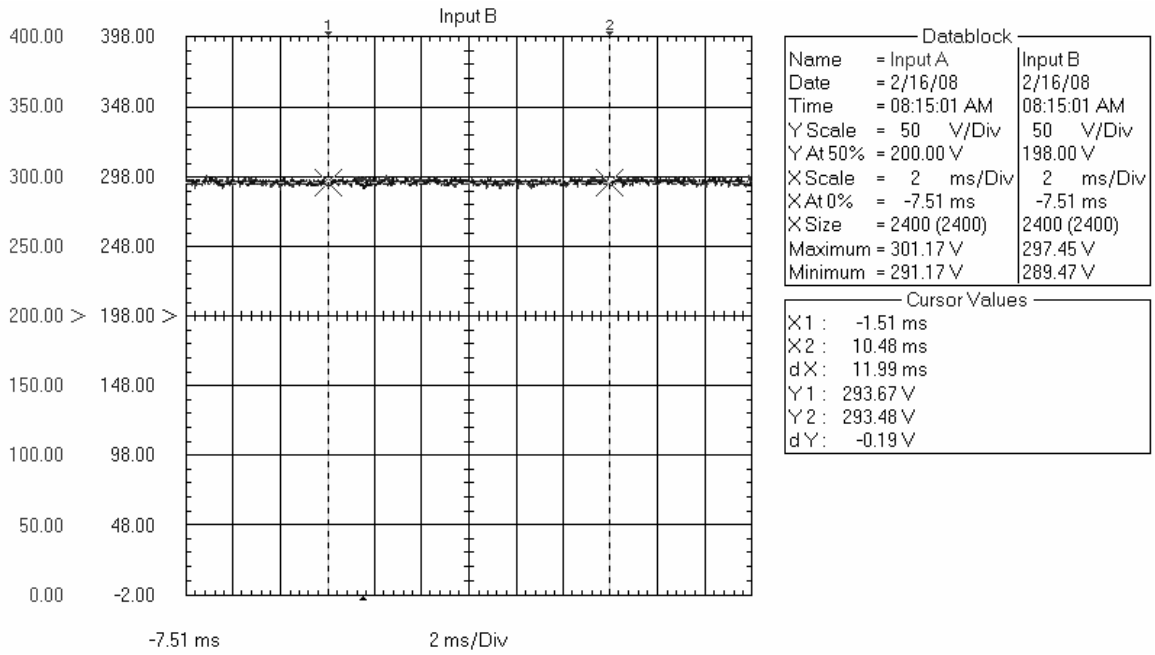


Fig.9.6 DC Link Capacitors Voltages Vc1 and Vc2
(X- axis: 1 div = 2 ms, Y- axis: 1 div= 50 V)

9.4 RESULTS ON 10 HP INDUCTION MOTOR

After testing of three-level inverter on 2 HP induction motor, it is tested on 10 HP induction motor. The current drawn by 10 HP induction motor is more than 2 HP induction motor. The effect of load current on dc link capacitors can be observed. The results are taken for different operating frequencies shown in below figures. Various results of line voltage, line current and dc link capacitor voltage have been presented. Dc link capaciror voltages are stable as shown ib fig. 9.10. The difference in capacitor voltages is less than 5 Volt.

Motor Specification, 10 HP, 2- Pole, 415 V, 50 Hz (With No Load)

Input Parameter By Key Pad,

Carrier Frequency = 2 kHz

DTC (Dead Time Compensation) Gain = 70,

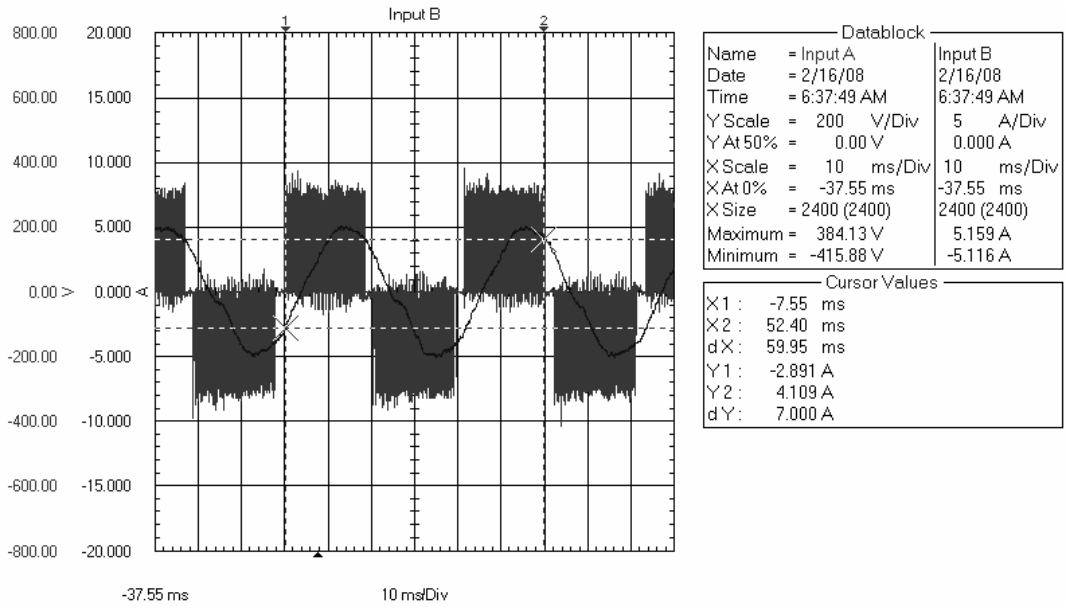


Fig.9.7 Line Voltage & Line Current waveforms at 25 Hz for 10 HP induction motor, mi = 0.865, (X- axis: 1 div = 5 ms, Y- axis: 1 div= 5 A, 1 div= 200 V)

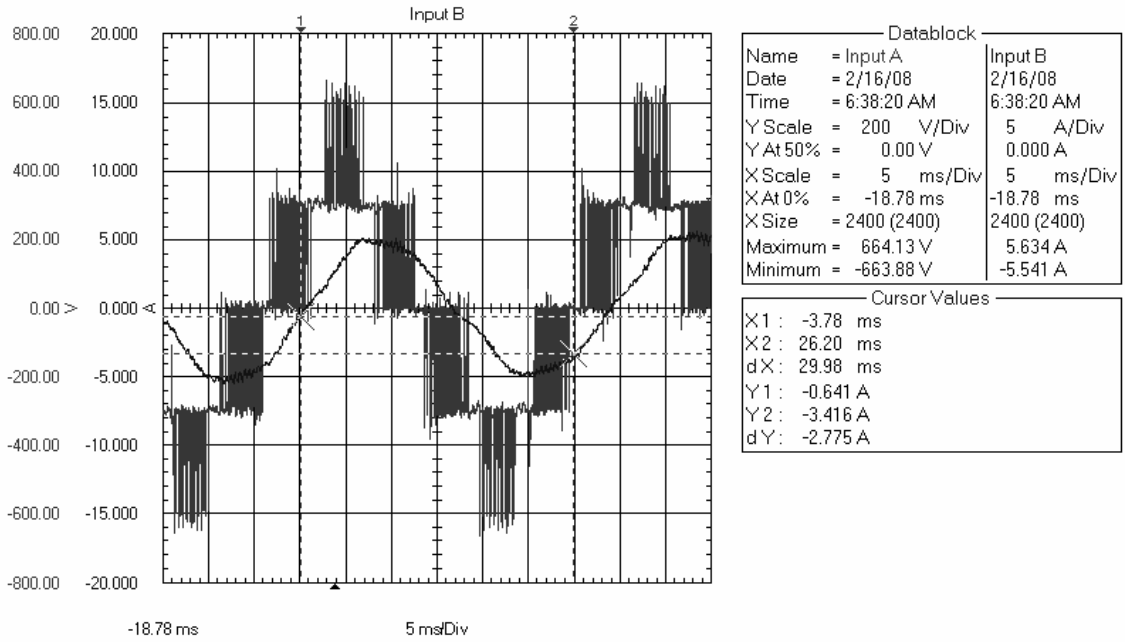


Fig.9.8 Line Voltage & Line Current waveforms at 30 Hz, mi = 1.03, (X- axis: 1 div = 5 ms, Y- axis: 1 div= 5 A, 1 div= 200 V)

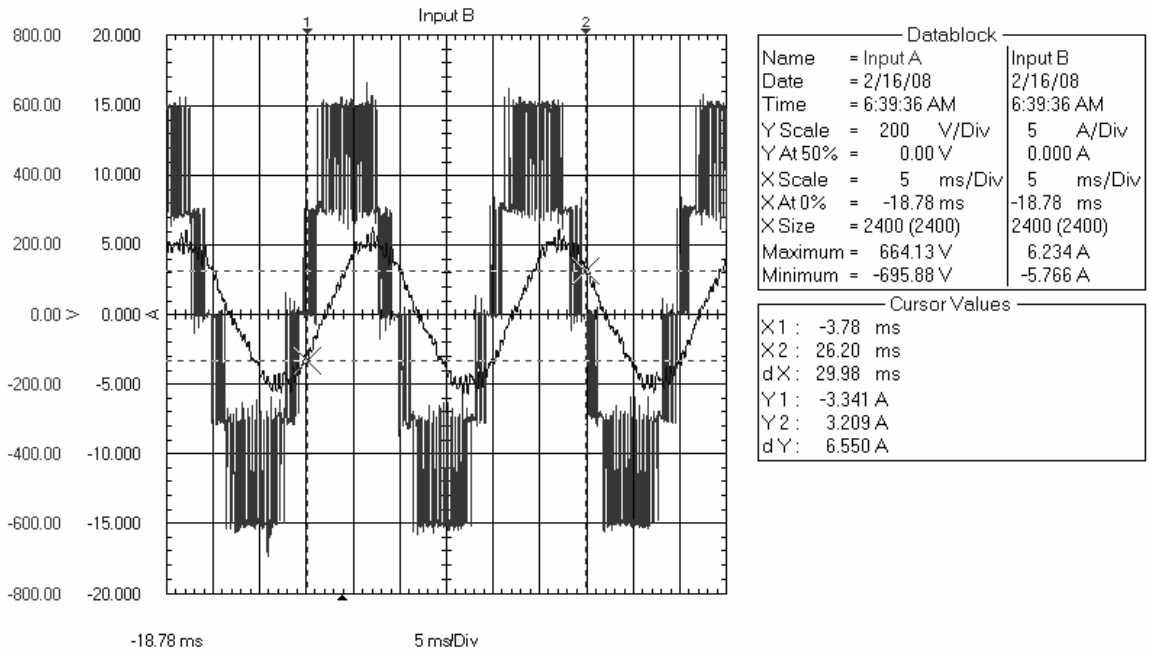


Fig.9.9 Line Voltage & Line Current waveforms at 50 Hz, mi = 1.73,
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 5 A, 1 div= 200 V)

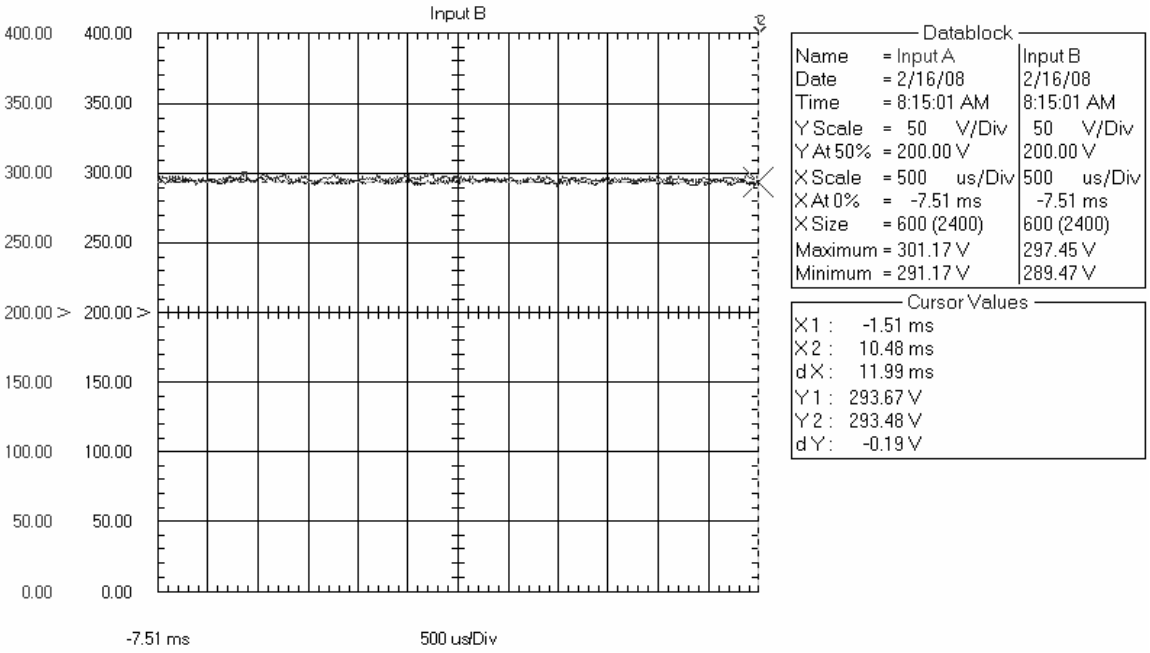


Fig.9.10 DC Link Capacitors Voltages Vc1 and Vc2,
(X- axis: 1 div = 2 ms, Y- axis: 1 div= 50 V)

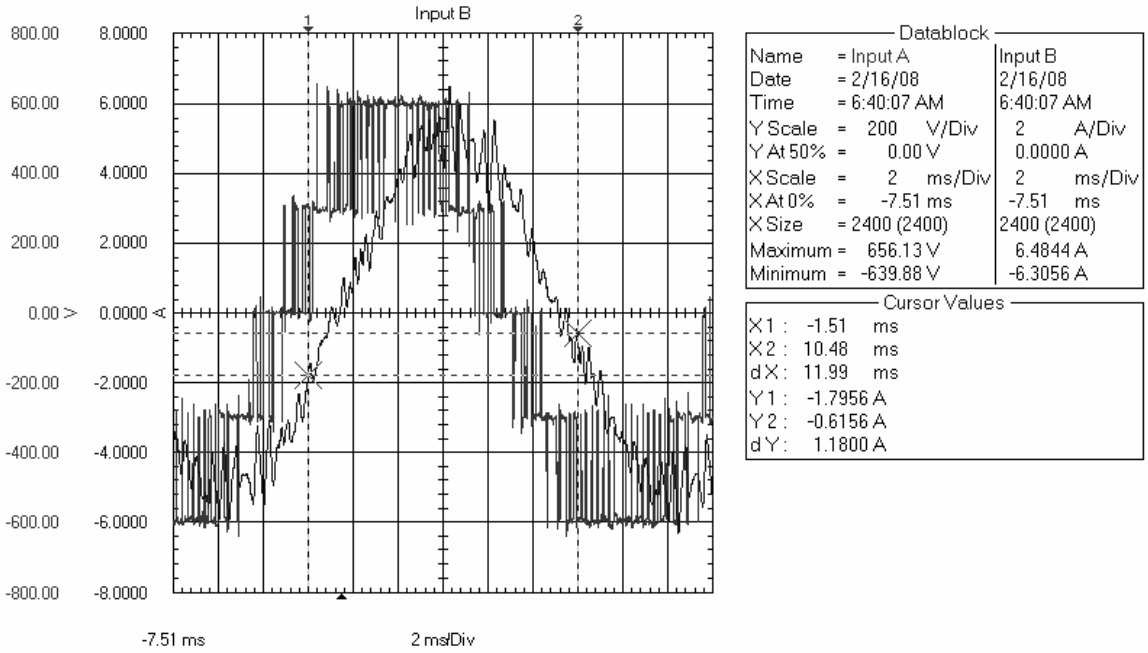


Fig.9.11 Expanded Line Voltage and Line Current waveforms at 50 Hz, mi = 1.73, Carrier frequency = 2 KHz, (X- axis: 1 div = 2 ms, Y- axis: 1 div= 2 A, 1 div= 200 V)

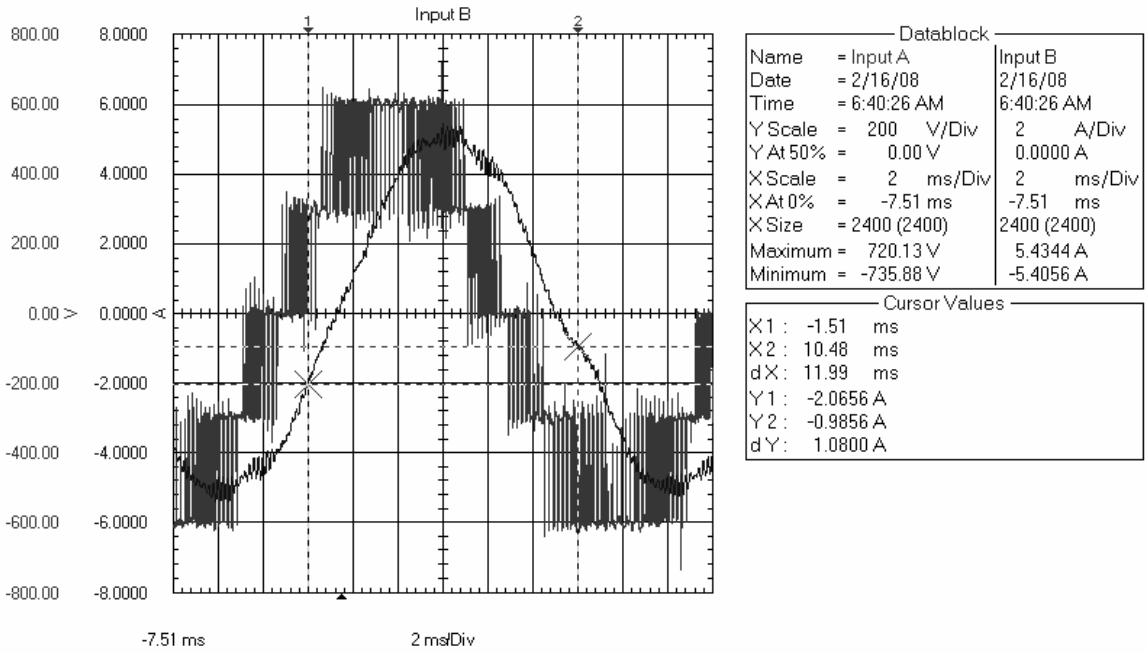


Fig.9.12 Expanded Line Voltage and Line Current waveforms at 50 Hz, mi = 1.73, Carrier frequency = 5 KHz, (X- axis: 1 div = 2 ms, Y- axis: 1 div= 2 A, 1 div= 200 V)

9.5 RESULTS ON 60 HP INDUCTION MOTOR

After success on 10 HP motor three-level inverter is tested on 60 HP induction motor and results are presented.

Motor Specification, 60 HP, 4- Pole, 415 V, 50 Hz (With No Load)

Input Parameter By Key Pad, Carrier Frequency = 2 KHz

DTC (Dead Time Compensation) Gain = 70,

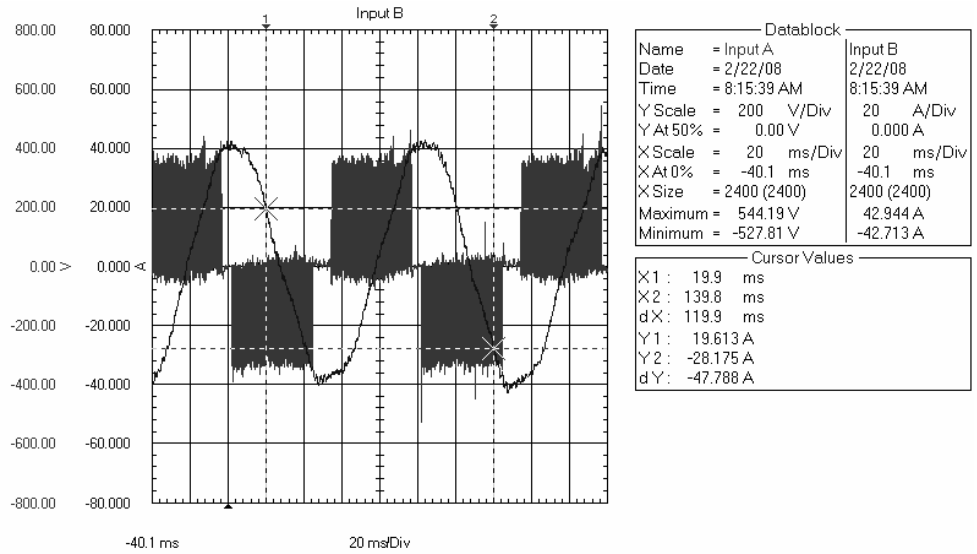


Fig.9.13 Line Voltage & Line Current Waveforms at 10 Hz, mi = 0.34,
(X- axis: 1 div = 20 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

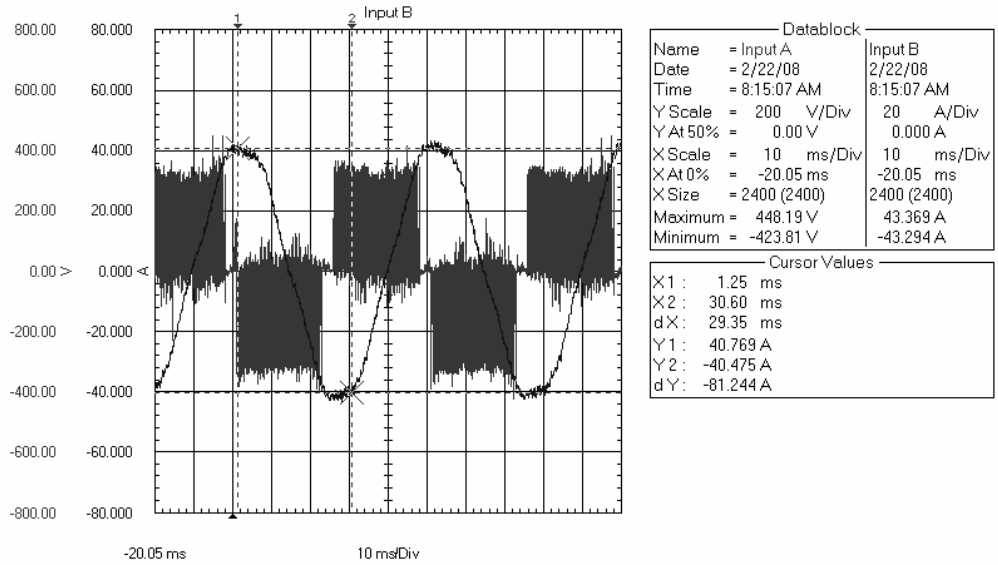


Fig.9.14 Line Voltage & Line Current Waveforms at 20 Hz, mi = 0.69,
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

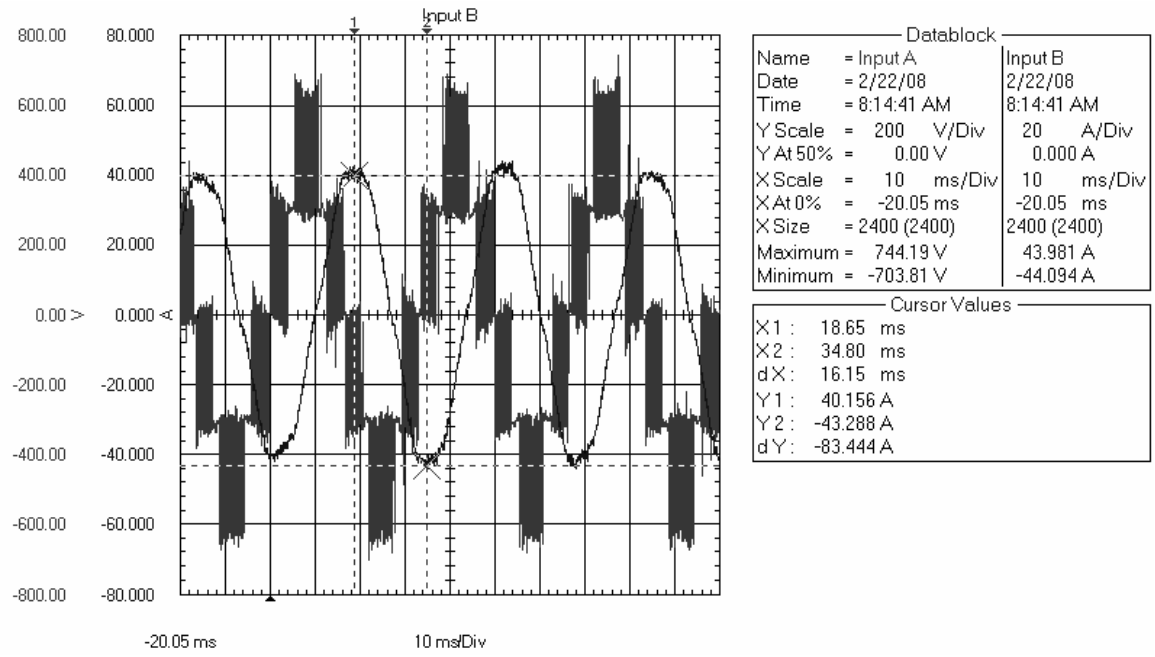


Fig.9.15 Line Voltage & Line Current Waveforms at 30 Hz, mi = 1.03,
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

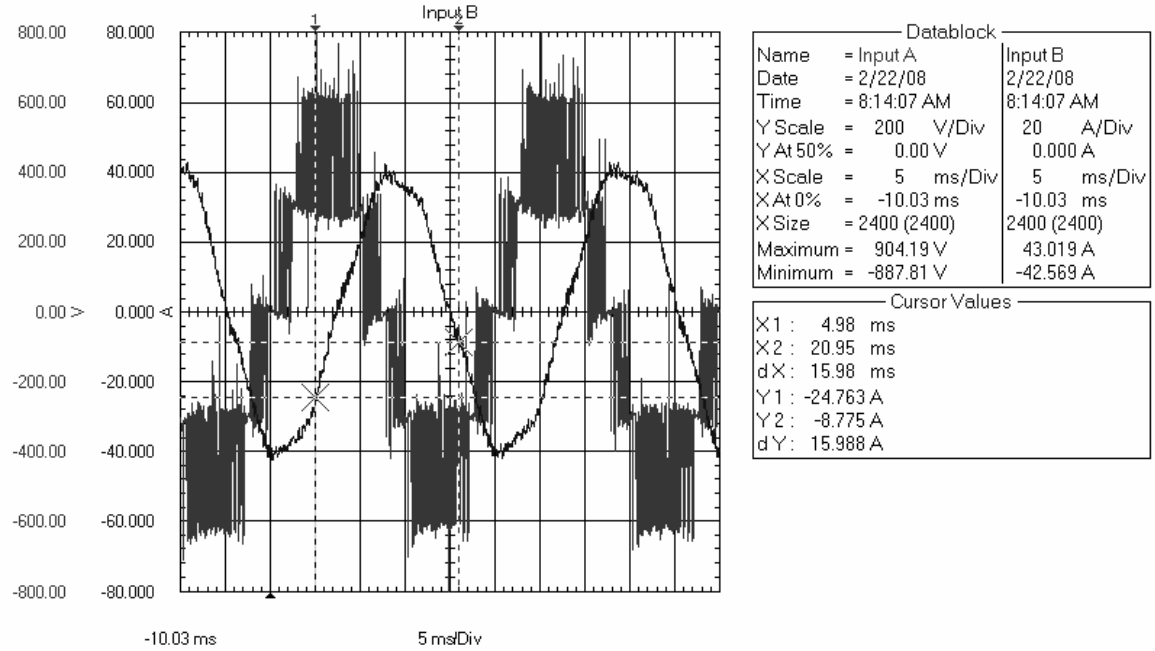


Fig.9.16 Line Voltage & Line Current Waveforms at 40 Hz, mi = 1.38,
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

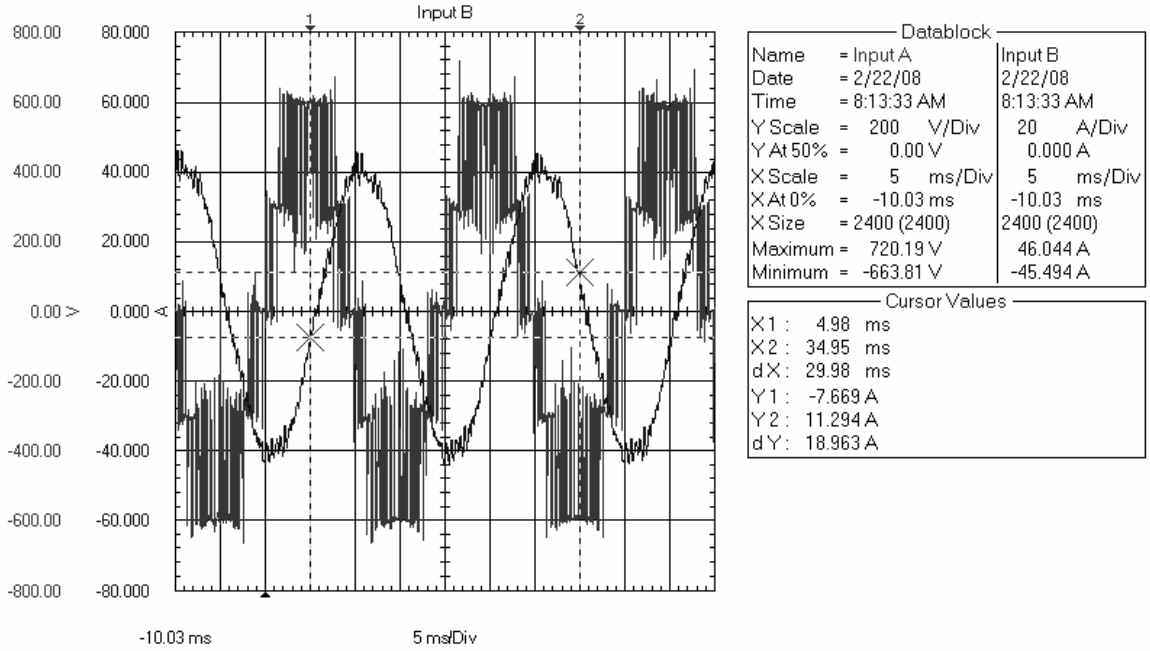


Fig.9.17 Line Voltage & Line Current Waveforms at 50 Hz, mi = 1.73,
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

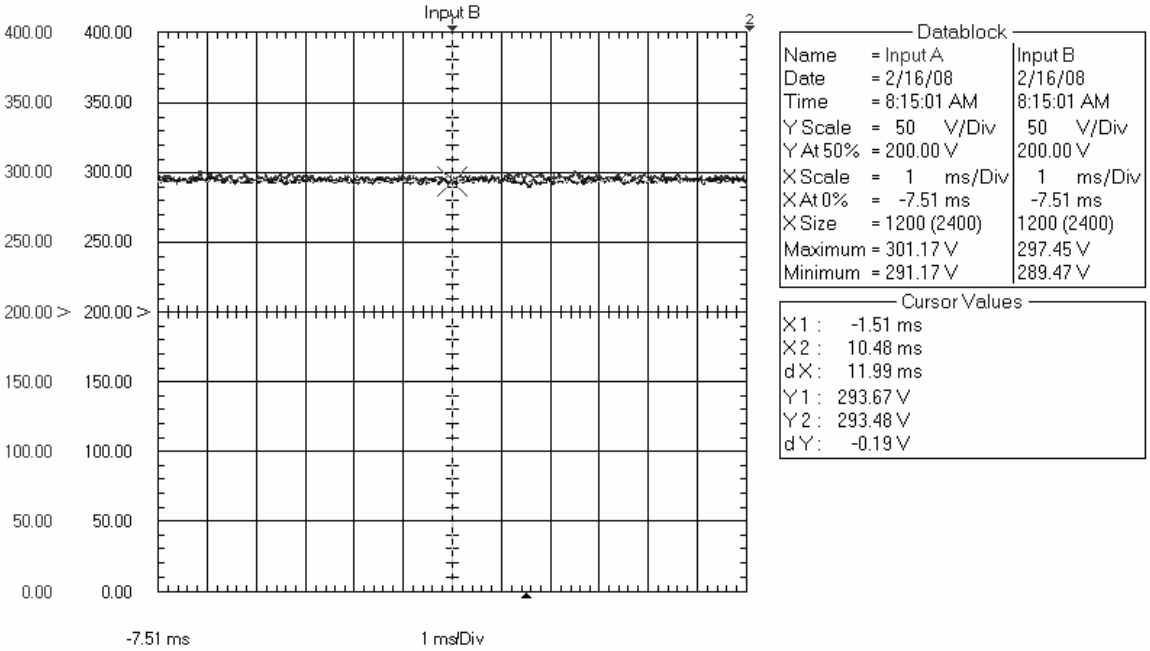


Fig.9.18 DC Link Capacitors Voltages Vc1 and Vc2,
(X- axis: 1 div = 2 ms, Y- axis: 1 div= 50 V)

9.6 RESULTS OF HEAT RUN TEST FOR THREE-LEVEL INVERTER

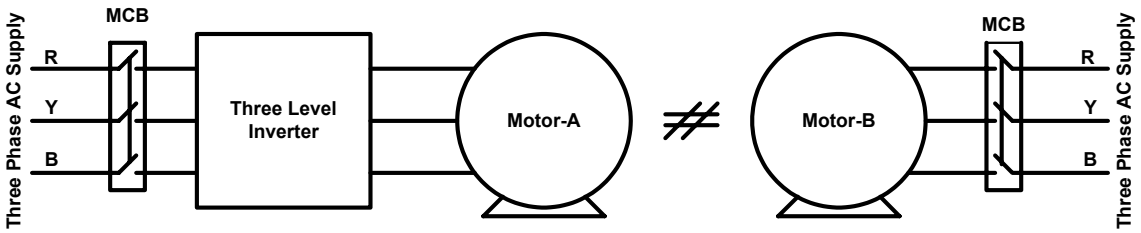


Fig.9.19 Block Diagram of Motor- Motor Set

9.6.1 PROCEDURE FOR HEAT RUN (FULL LOAD) TEST OF TLI

Connect Circuit as per shown in fig. two identical mechanically coupled three phase induction motors are required for this test. Measure mains supply frequency. Set three-level inverter frequency more than mains supply frequency in fraction. Then start the three-level inverter, so motor-A will start and run more than rated speed. Switch on motor-B, when motor-A gets its full speed. Motor-B will operate as an induction generator and feed power in the mains. Motor-A operates as a prime mover. Motor-A will run at its rated current. Continuously monitor motor-A three-level inverter output current, because mains frequency should be very with time. If Motor-A current is going to be decrease from its rated current, increase frequency of three-level inverter in fraction (more than mains frequency). If loading of motor-A increase more than 100 %, Decrease TLI set frequency in fraction but it should be more than mains frequency. During this test also note down dc link voltages Vc1 and Vc2. The difference between Vc1 and Vc2 should be less than 10 volt.

9.6.2 HEAT RUN TEST CONDITIONS AND RESULTS

Motor Specification: 60 HP, 4- Pole, 415 V, 50 Hz (With Load)

Input Parameter By Key Pad, Carrier Frequency = 2.5 KHz,

DTC (Dead Time Compensation) Gain = 110,

The test results of line voltage and current are shown in fig.2.2, fig.2.3 and fig.2.4 for three-level inverter. The readings are noted by computer is given in Table-9.1. The axpert communicator software is used for recording results. The test is carried out for

four hours. During this test the maximum temperature rise is noted 31 ºC, which can be allowable. During this test the dc link capacitor voltages are also stable, so it proves ability of self balancing SVPWM scheme. FFT of line voltage and line current waves are shown in fig. using fluke software. The THD for current is 1.68 % and THD for voltage is 7.78 %.

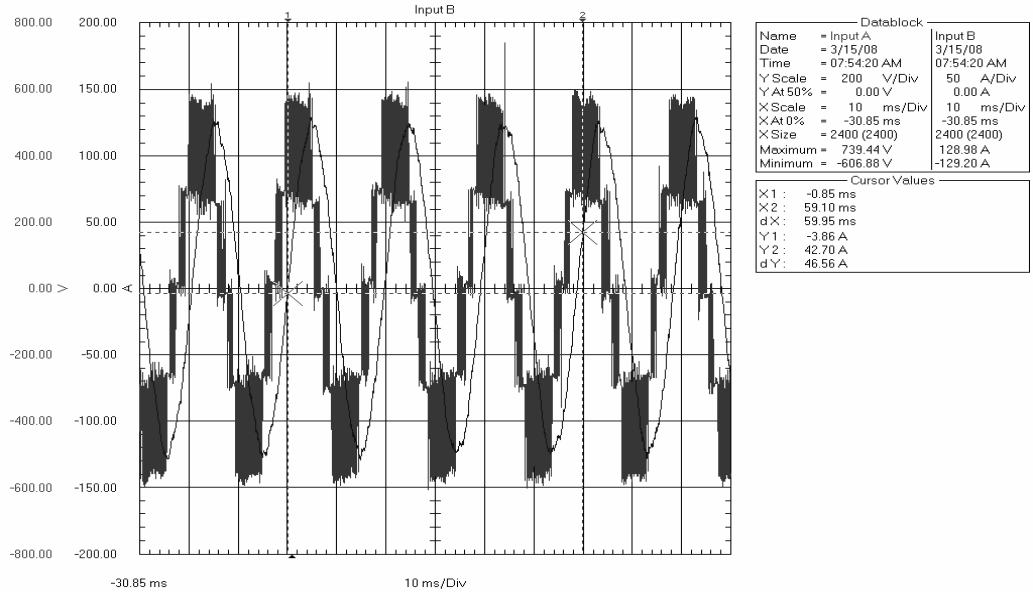


Fig.9.20 Line Voltage & Line Current Waveforms of heat run test,
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 50 A, 1 div= 200 V)

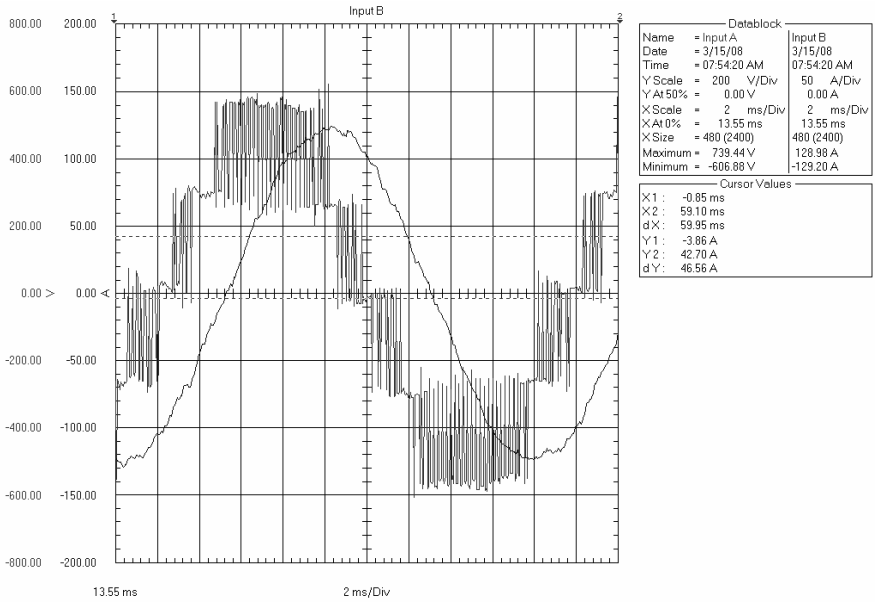


Fig.9.21 Expanded Line Voltage & Line Current Waveforms of heat run test,
(X- axis: 1 div = 2 ms, Y- axis: 1 div= 50 A, 1 div= 200 V)

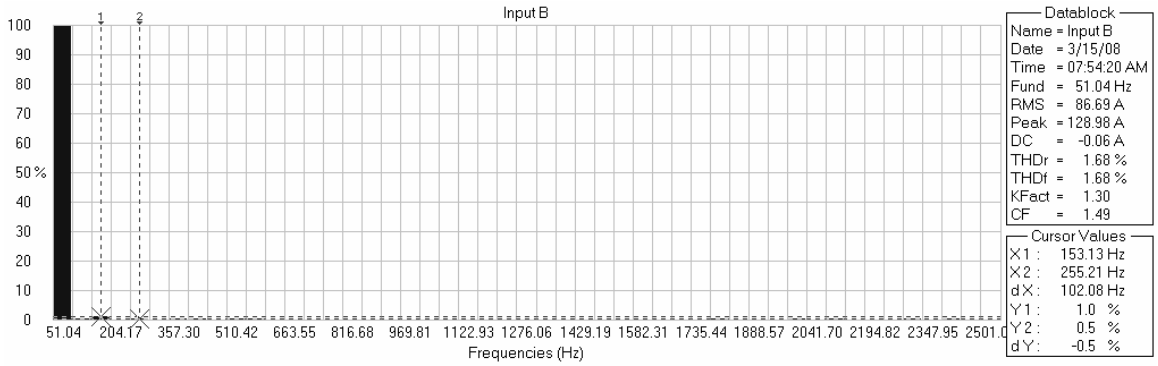


Fig.9.22 Spectrum of line current of three-level inverter at 50 Hz, DTC gain = 110

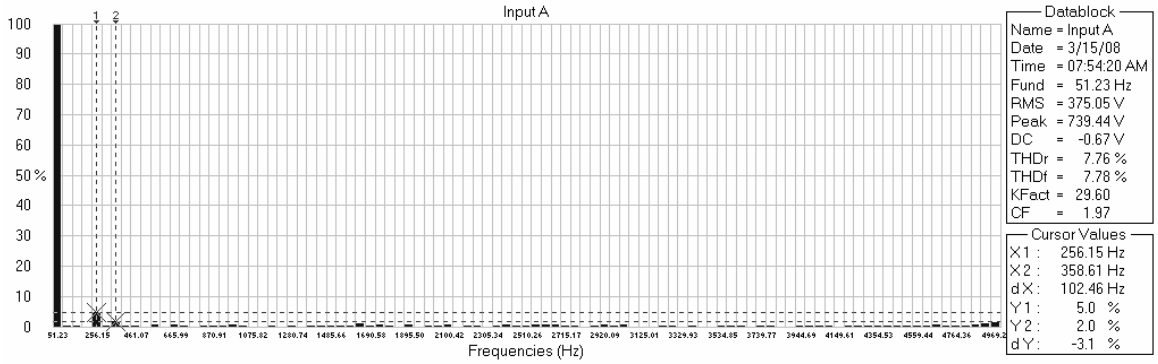


Fig.9.23 Spectrum of line voltage of three-level inverter at 50 Hz, DTC gain = 110

TABLE –9.1
THREE-LEVEL INVERTER HEAT RUN TEST

Time	Output frequency	Output Current	Input Voltage	Input Voltage	DC Bus Voltage	Heat Sink Temperature	Ambient Temperature
	Hz	Amp	Vry	Vyb	Vdc	Deg. C	Deg.C
	M101	M103	M201	M202	M204	M208	Ta
11:45:39 AM	50.26	85.8	405	405	571	52	22
12:00:39 PM	50.62	88.8	409	411	570	52	22
12:15:39 PM	50.83	83.8	413	415	575	50	22
12:30:39 PM	50.71	89.9	400	399	555	54	23
12:45:39 PM	50.79	83.3	404	404	565	53	23
1:00:39 PM	50.96	83.1	406	406	555	53	23
1:15:39 PM	51.65	85.9	410	412	579	52	23
1:30:39 PM	51.17	88.9	406	406	561	54	23
1:45:39 PM	50.96	89.8	403	403	553	54	23
2:00:39 PM	51.1	84.1	402	403	560	53	23
2:15:39 PM	50.74	85	398	399	548	55	24
2:30:39 PM	51.09	85.5	398	398	553	54	24
2:45:39 PM	51.28	85.2	398	398	544	54	24
3:00:39 PM	51.19	86.8	396	397	558	54	24
3:15:39 PM	51.07	88.9	397	397	545	55	24
3:30:39 PM	51.02	86.6	396	397	549	55	24
Maximum temperature rise = 31 ºC							

9.7 RESULTS ON 60 HP INDUCTION MOTOR WITH AND WITHOUT DEAD TIME COMPENSATION FOR TLI

The effect of dead time compensation for different operating frequency on line voltage and line current are shown in below figures. The effect of dead time compensation on motor current is more at 20 Hz frequency. When DTC gain is zero at 20 Hz the line current of motor is distorted, so the vibration in motor is also increased. Motor Specification, 45 kW (60 HP), 4- Pole, 415 V, 50 Hz (With No Load)

Input Parameter by Key Pad, Carrier Frequency = 2.5 KHz

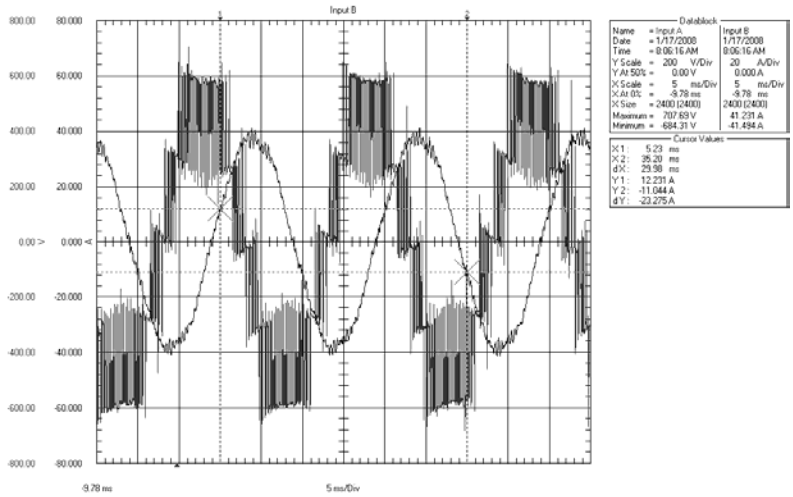


Fig.9.24 Line Voltage and Line Current Waveforms at 50 Hz, DTC Gain =110
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

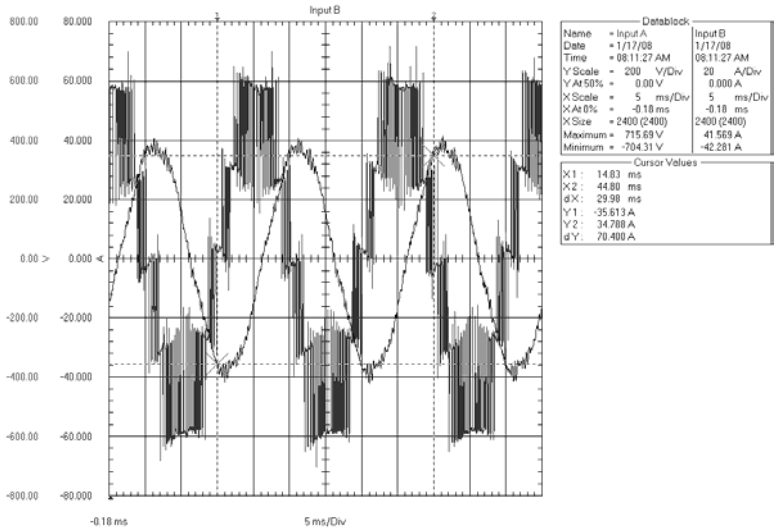


Fig.9.25 Line Voltage and Line Current Waveforms at 50 Hz, DTC Gain =0
(X- axis: 1 div = 5 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

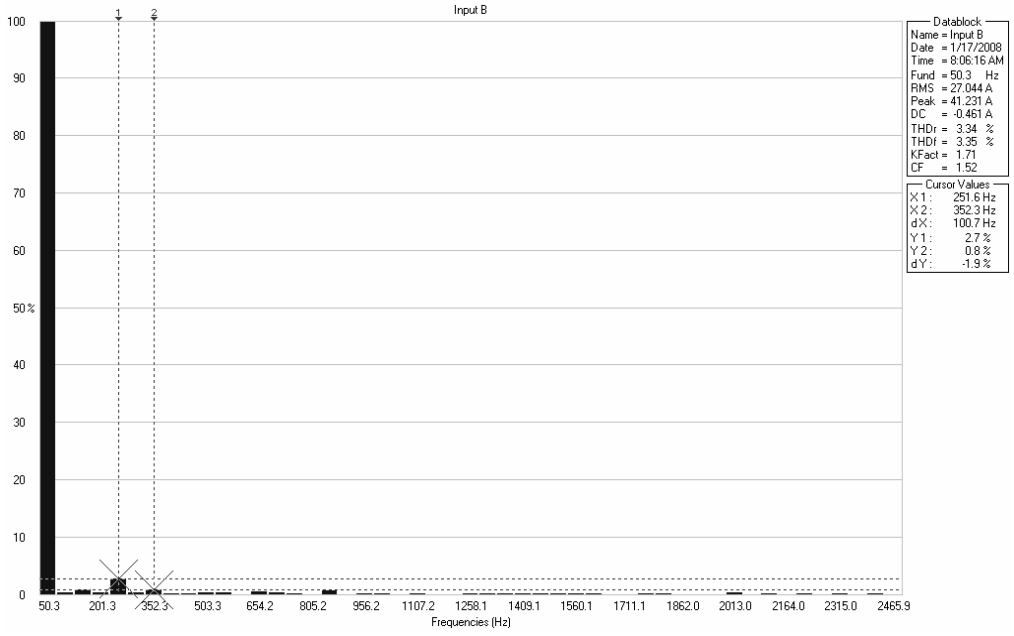


Fig.9.26 Spectrum of line current at 50 Hz, DTC gain = 110

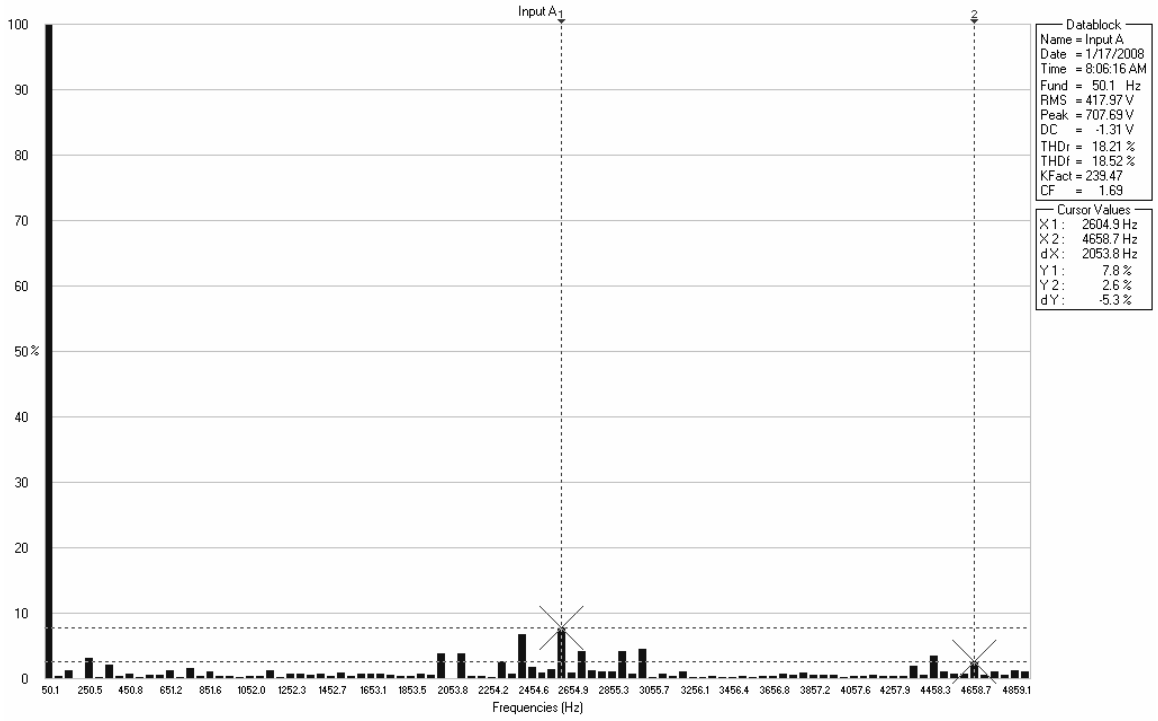


Fig.9.27 Spectrum of line voltage at 50 Hz, DTC gain = 110

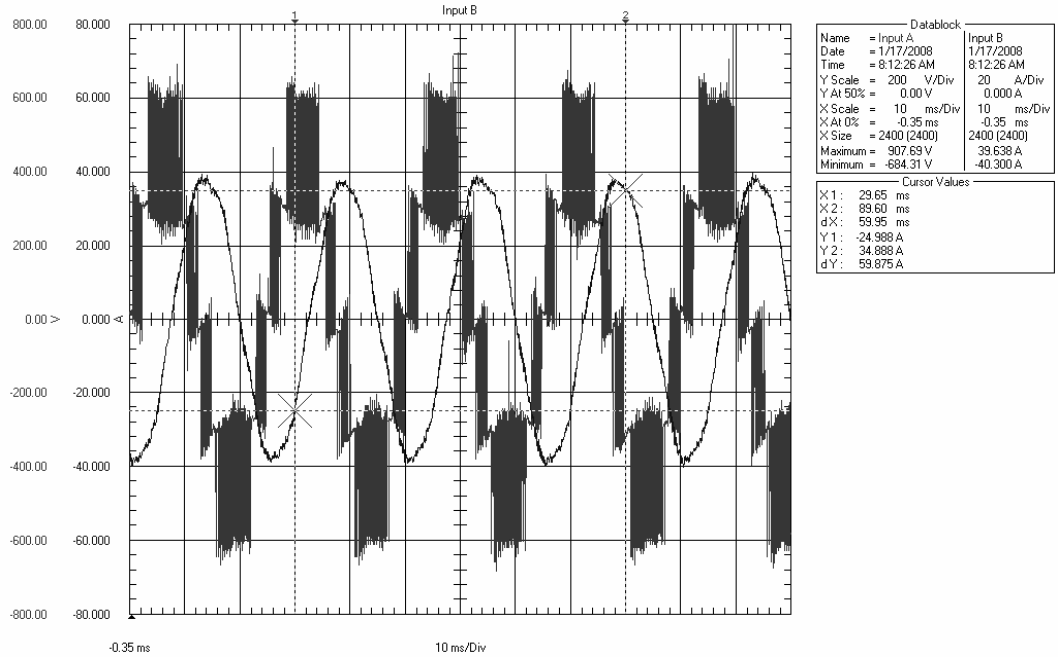


Fig.9.28 Line Voltage and Line Current Waveforms at 40 Hz, DTC Gain =110
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

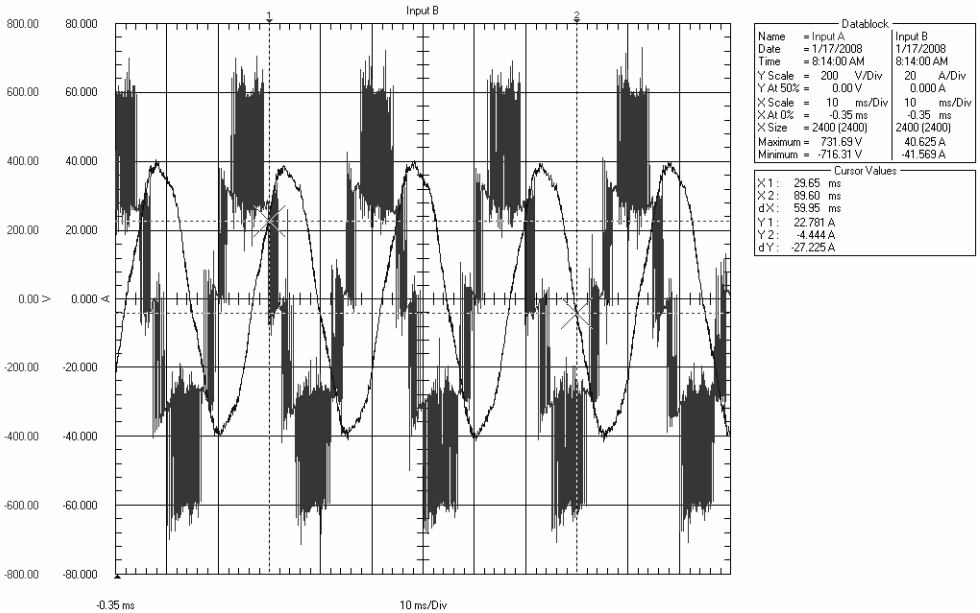


Fig.9.29 Line Voltage and Line Current Waveforms at 40 Hz, DTC Gain =0
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

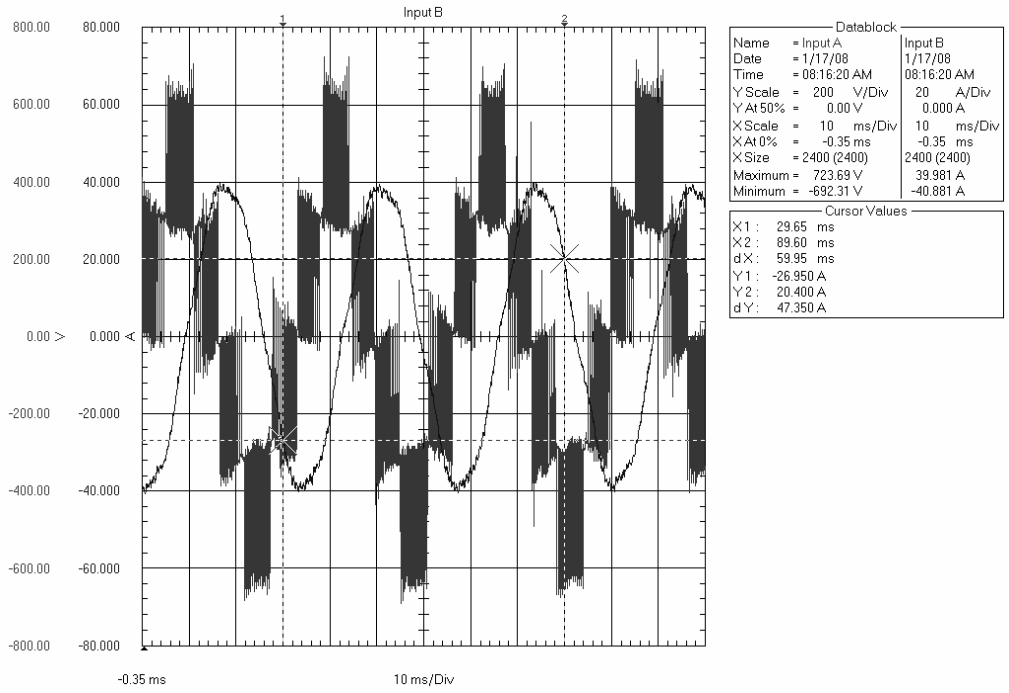


Fig.9.30 Line Voltage and Line Current Waveforms at 30 Hz, DTC Gain =110
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

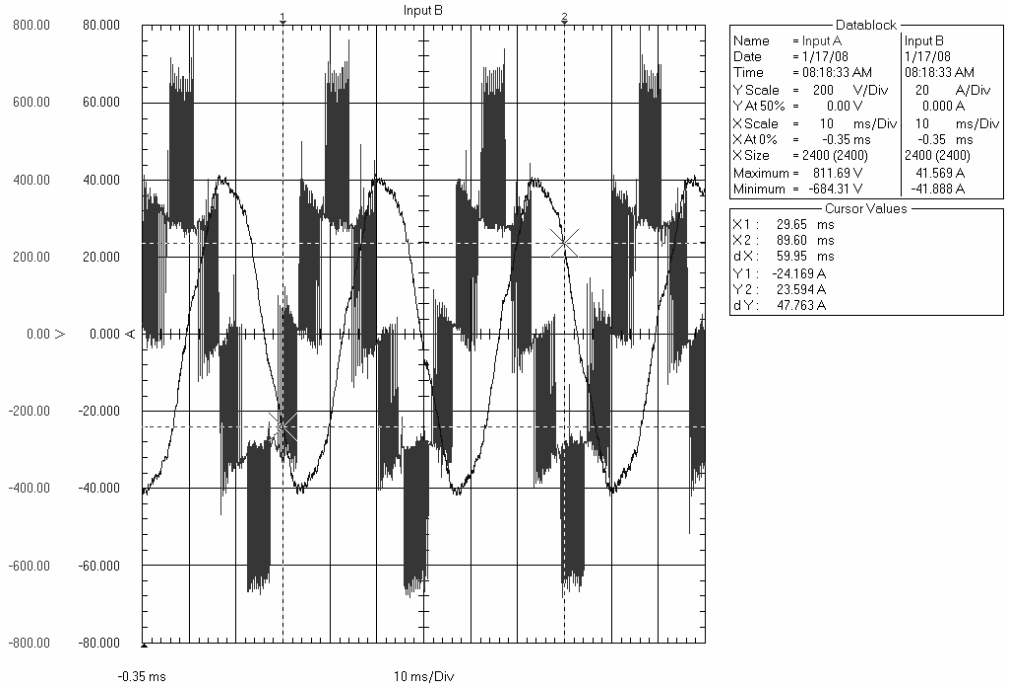


Fig.9.31 Line Voltage and Line Current Waveforms at 30 Hz, DTC Gain =0
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

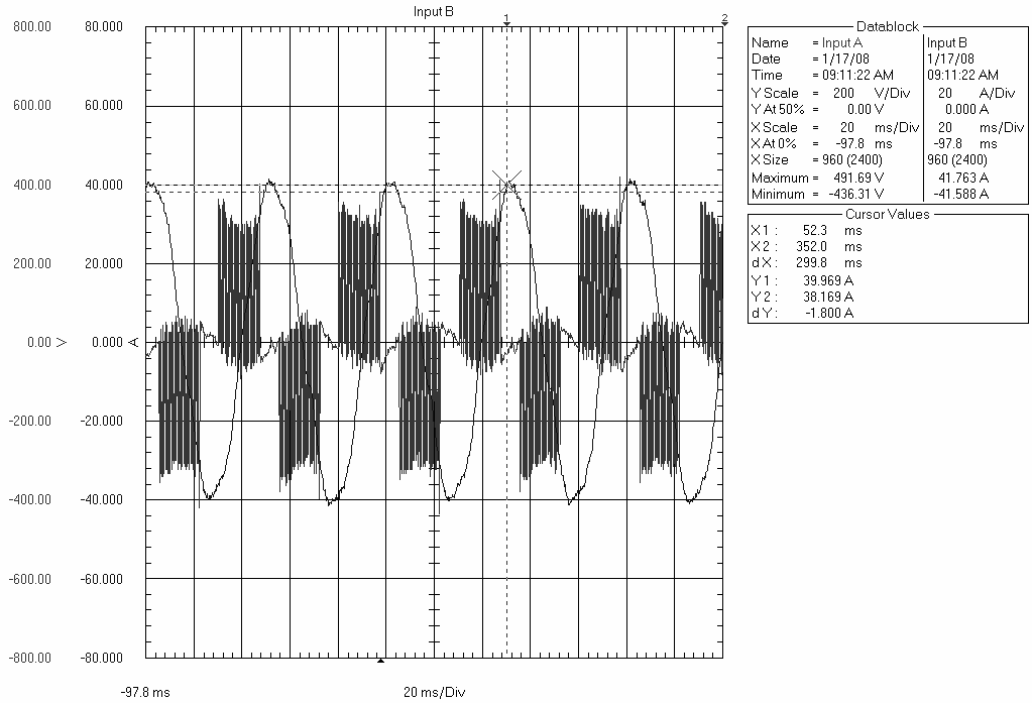


Fig.9.32 Line Voltage and Line Current Waveforms at 20 Hz, DTC Gain =110
(X- axis: 1 div = 20 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

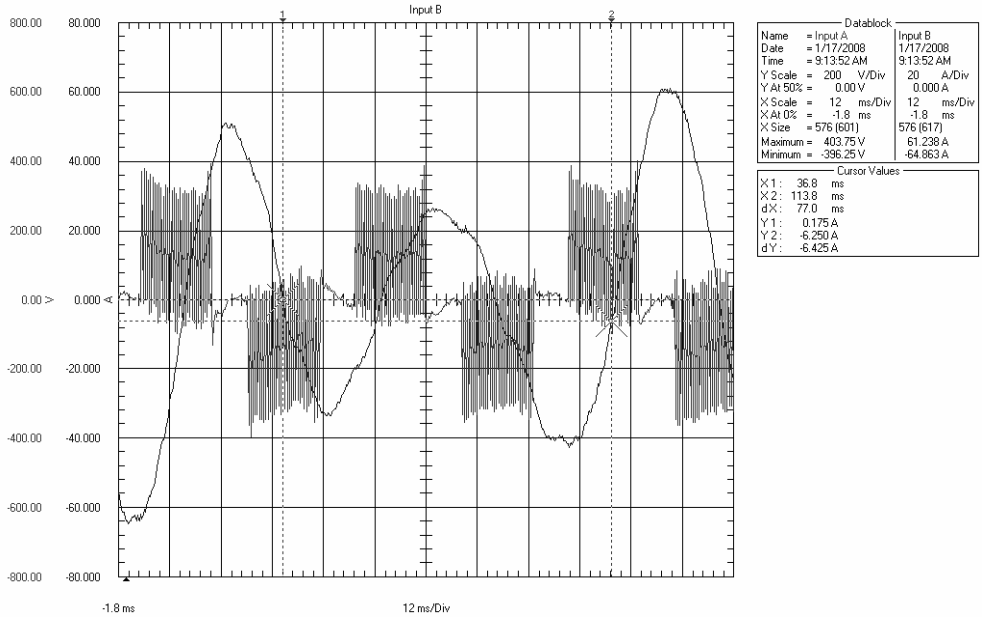


Fig.9.33 Line Voltage and Line Current Waveforms at 20 Hz, DTC Gain =0
(X- axis: 1 div = 12 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

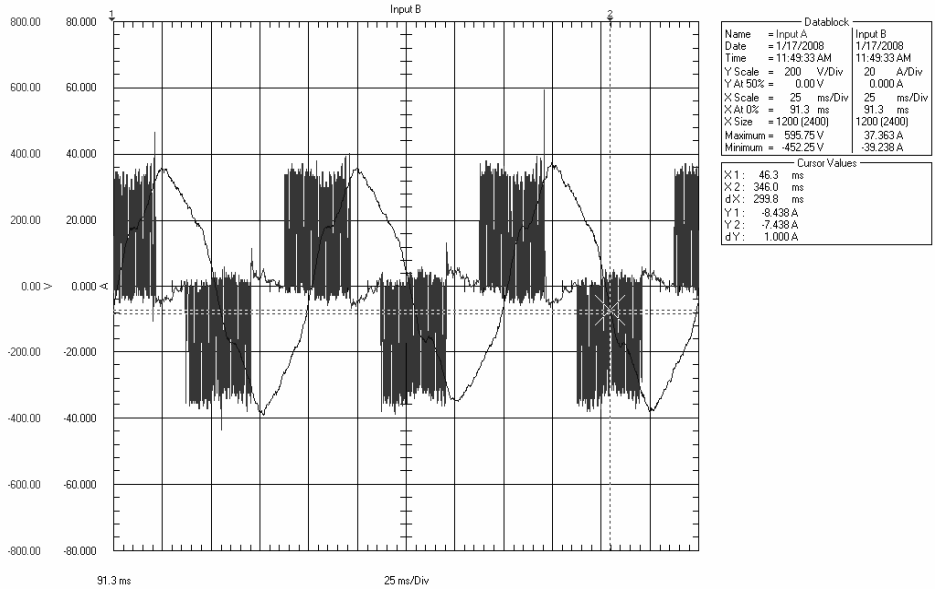


Fig.9.34 Line Voltage and Line Current Waveforms at 10 Hz, DTC Gain =110
(X- axis: 1 div = 25 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

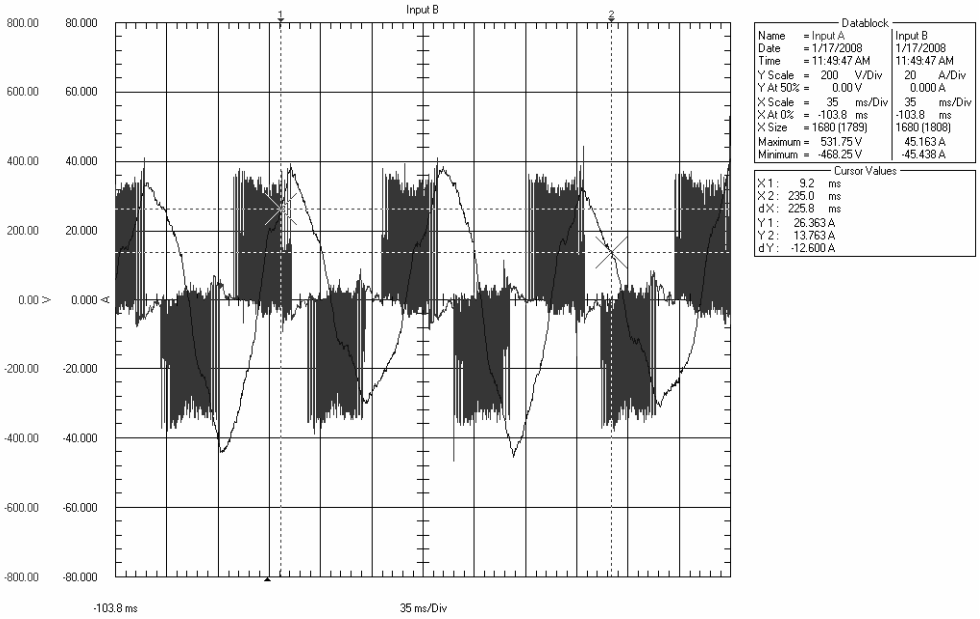


Fig.9.35 Line Voltage and Line Current Waveforms at 10 Hz, DTC Gain =0
(X- axis: 1 div = 35 ms, Y- axis: 1 div= 20 A, 1 div= 200 V)

Below 20 Hz frequency the effect of dead time compensation is more on motor current. So the dead time compensation must used at low frequency. Without dead time compensation at low frequency the pulsation in current wave results in torque pulsation.

9.8 RESULTS FOR TWO-LEVEL INVERTER WITH AND WITHOUT DEAD TIME COMPENSATION

To find performance difference between two-level inverter and three-level inverter, testing of two-level inverter has been carried out. The test results of two-level inverter with same rating of three-level inverter have been shown in below figures. The results also present effect of dead time compensation for two-level inverter.

Motor Specification, 45 kW (60 HP), 4- Pole, 415 V, 50 Hz (With No Load)

Input Parameter By Key Pad, Carrier Frequency = 2.5 KHz

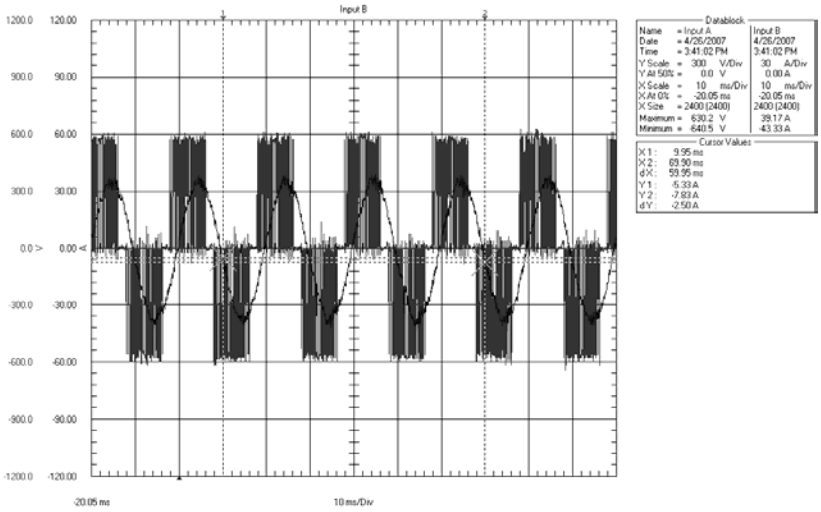


Fig.9.36 Line Voltage and Line Current Waveforms at 50 Hz for two-level inverter, DTC Gain =70 (X- axis: 1 div = 10 ms, Y- axis: 1 div= 30 A, 1 div= 300 V)

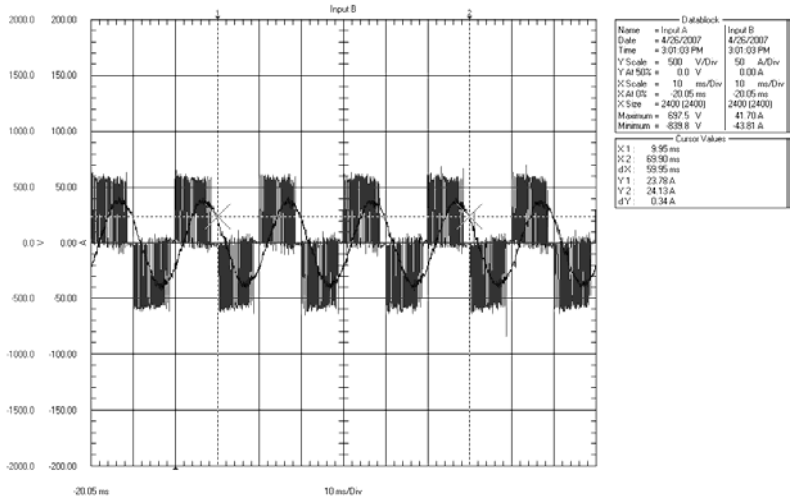


Fig.9.37 Line Voltage and Line Current Waveforms at 50 Hz, DTC Gain =0 (X- axis: 1 div = 10 ms, Y- axis: 1 div= 50 A, 1 div= 500 V)

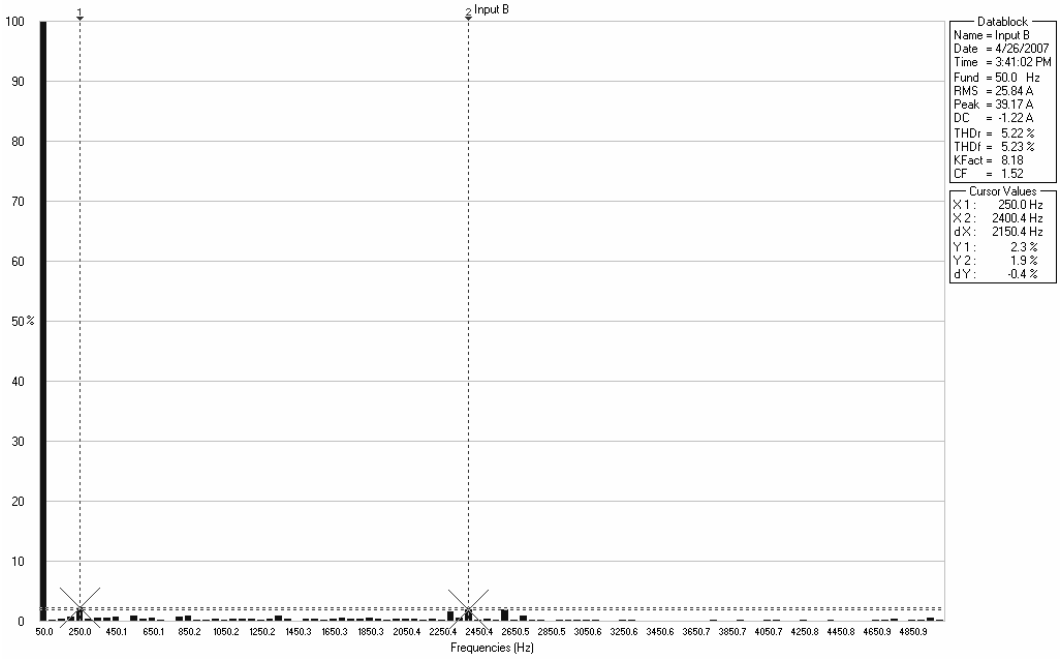


Fig.9.38 Spectrum of line current for two-level inverter at 50 Hz, DTC gain = 70

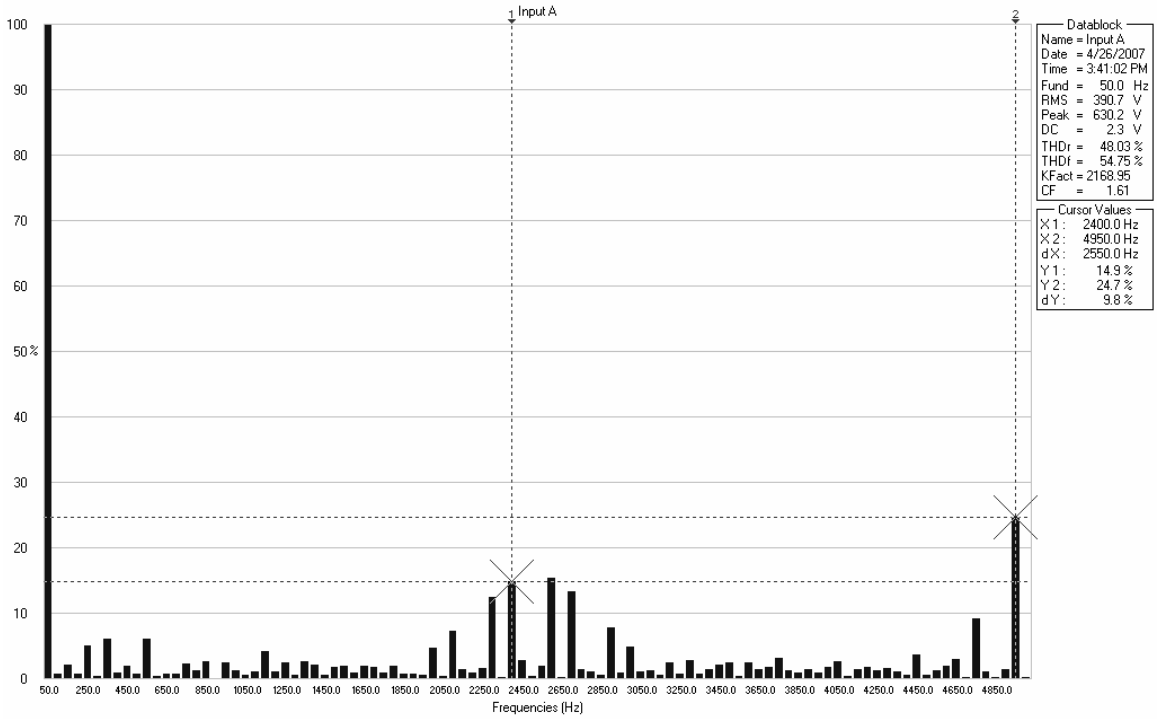


Fig.9.39 Spectrum of line voltage for two-level inverter at 50 Hz, DTC gain = 70

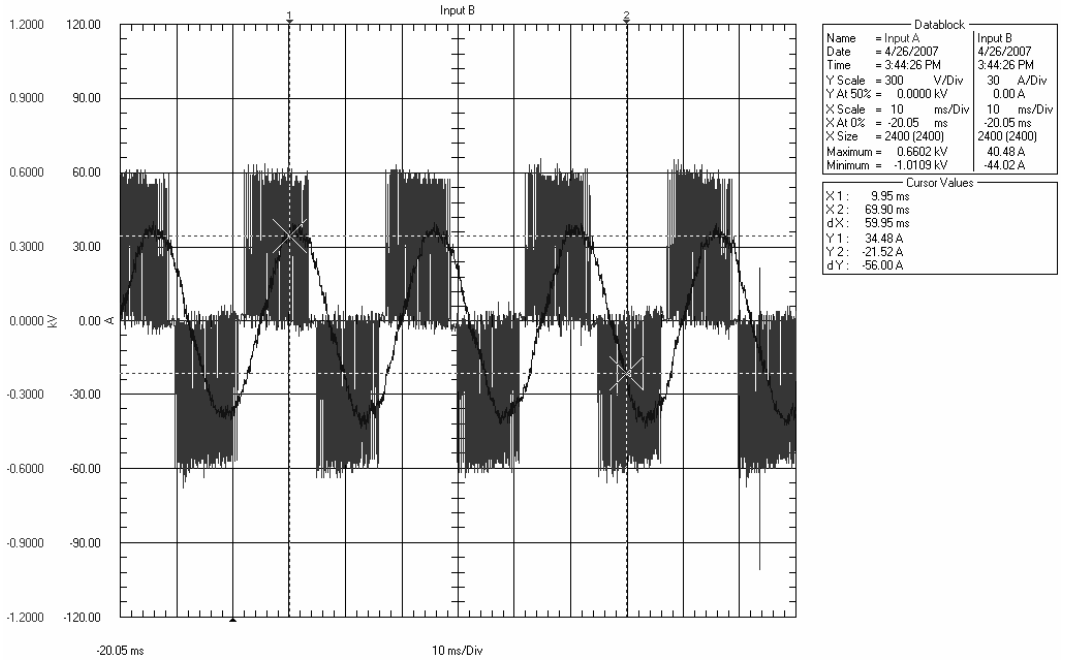


Fig.9.40 Line Voltage and Line Current Waveforms at 40 Hz, DTC Gain =70
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 30 A, 1 div= 300 V)

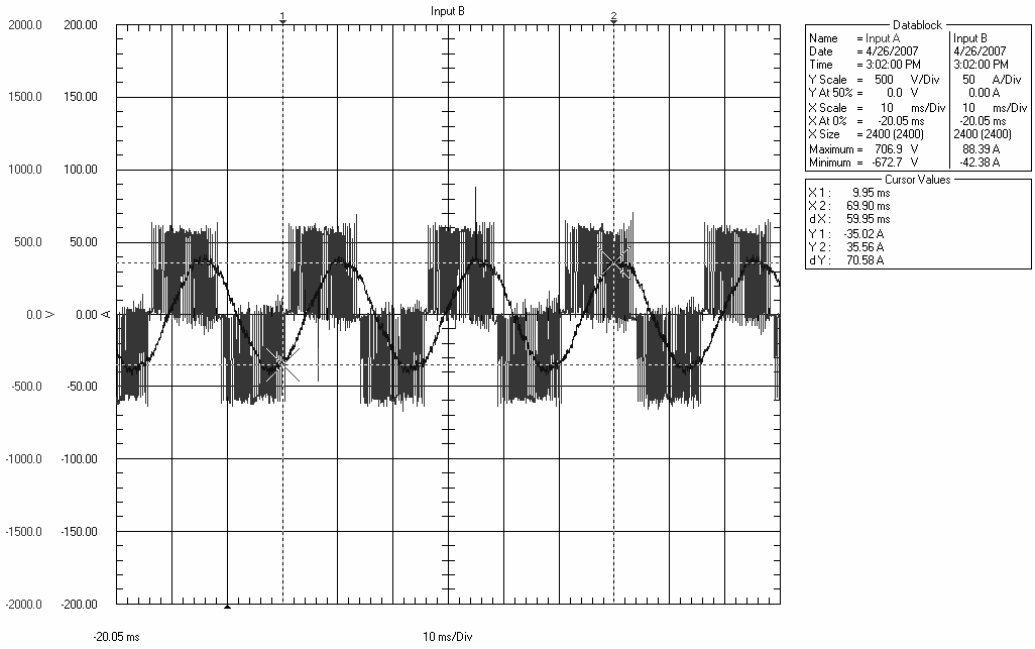


Fig.9.41 Line Voltage and Line Current Waveforms at 40 Hz, DTC Gain =0
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 50 A, 1 div= 500 V)

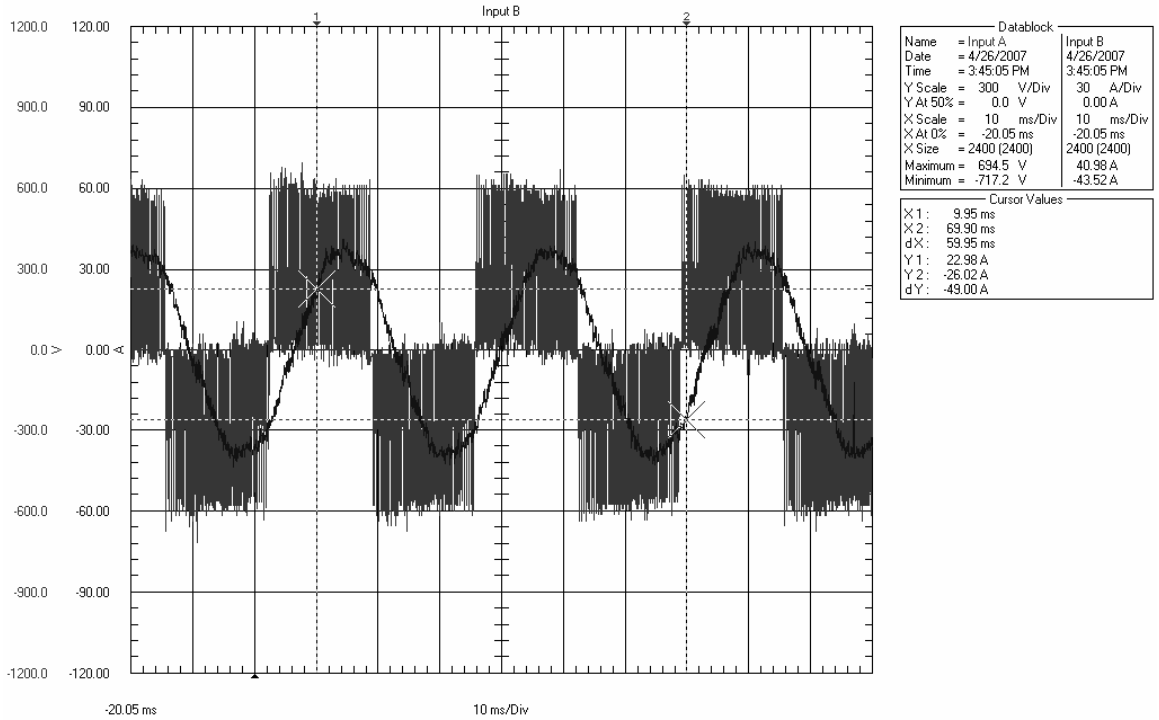


Fig.9.42 Line Voltage and Line Current Waveforms at 30 Hz, DTC Gain =70
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 30 A, 1 div= 300 V)

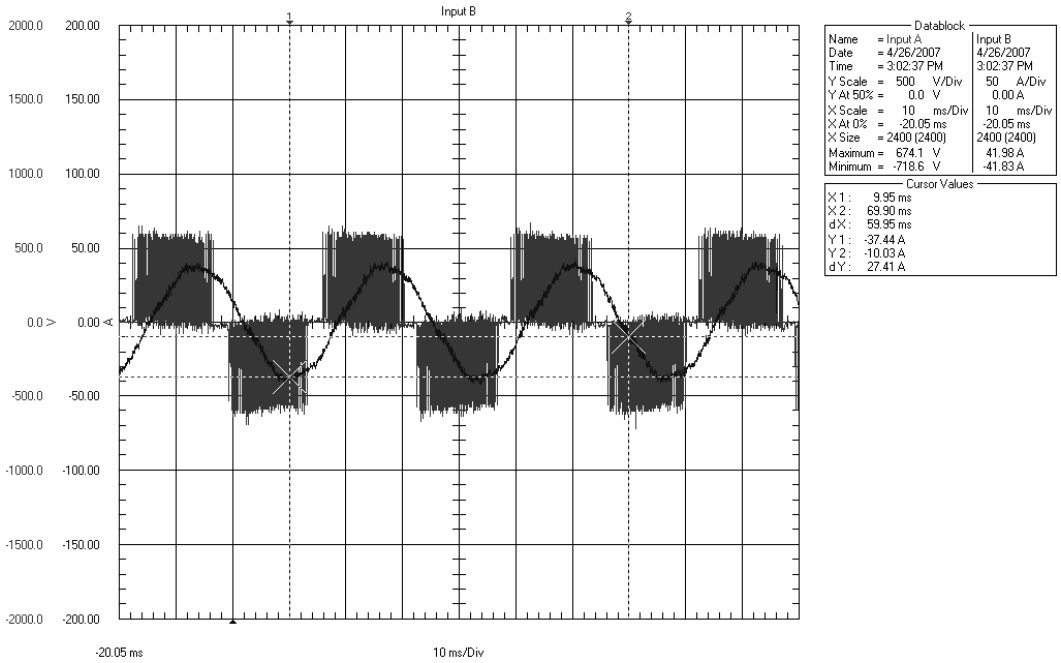


Fig.9.43 Line Voltage and Line Current Waveforms at 30 Hz, DTC Gain =0
(X- axis: 1 div = 10 ms, Y- axis: 1 div= 50 A, 1 div= 500 V)

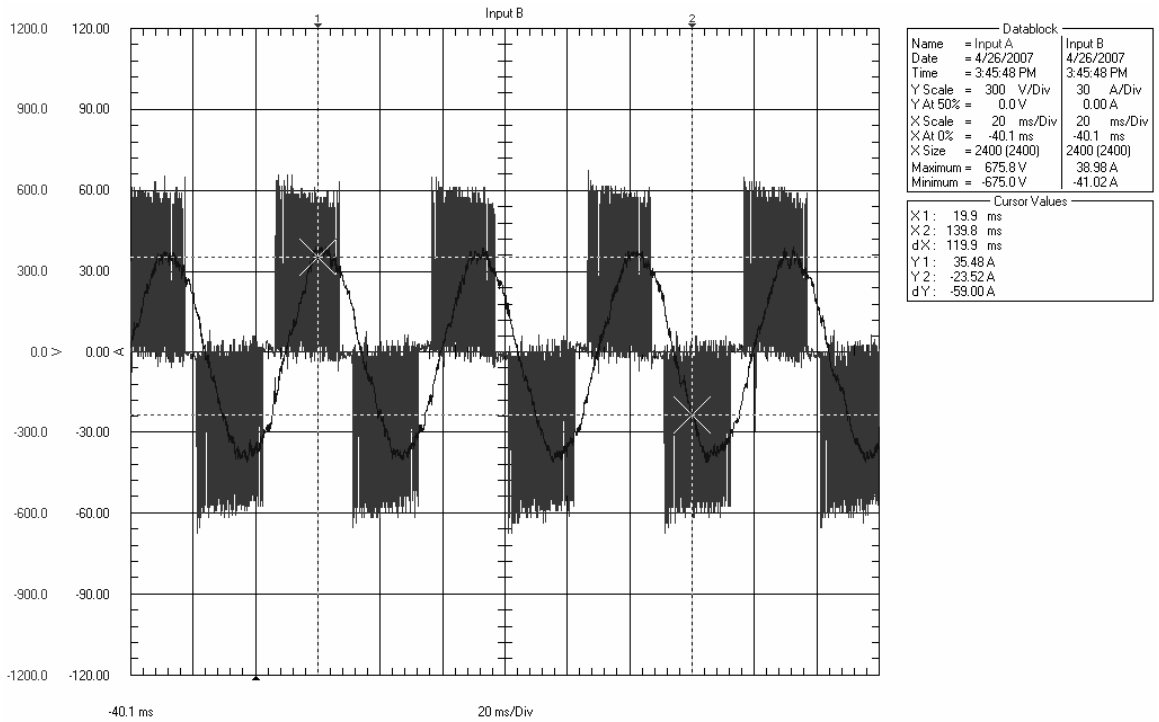


Fig.9.44 Line Voltage and Line Current Waveforms at 20 Hz, DTC Gain =70
(X- axis: 1 div = 20 ms, Y- axis: 1 div= 30 A, 1 div= 300 V)

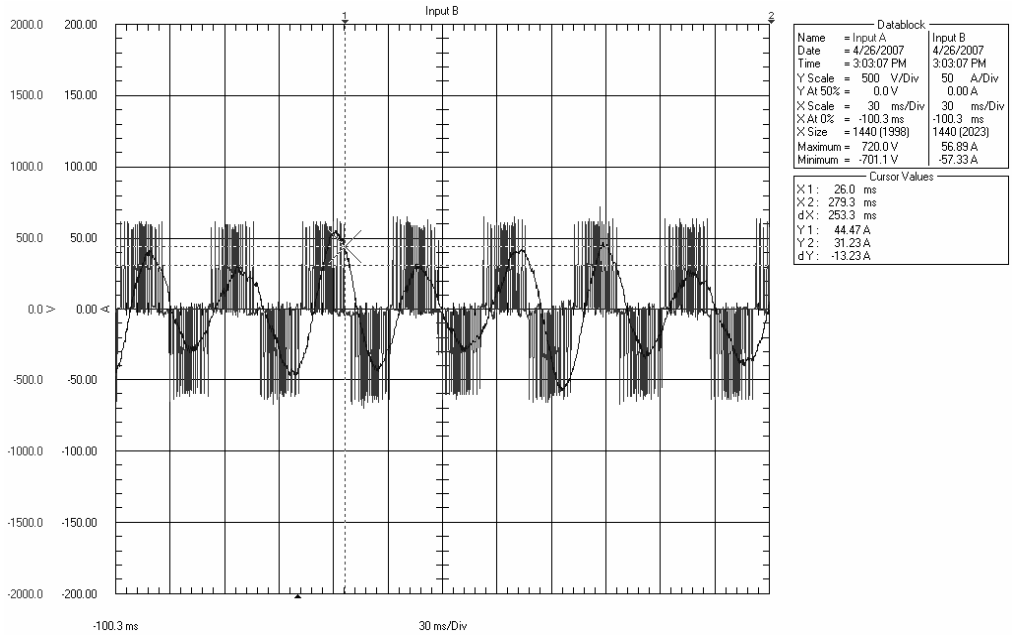


Fig.9.45 Line Voltage and Line Current Waveforms at 20 Hz, DTC Gain =0
(X- axis: 1 div = 30 ms, Y- axis: 1 div= 50 A, 1 div= 500 V)

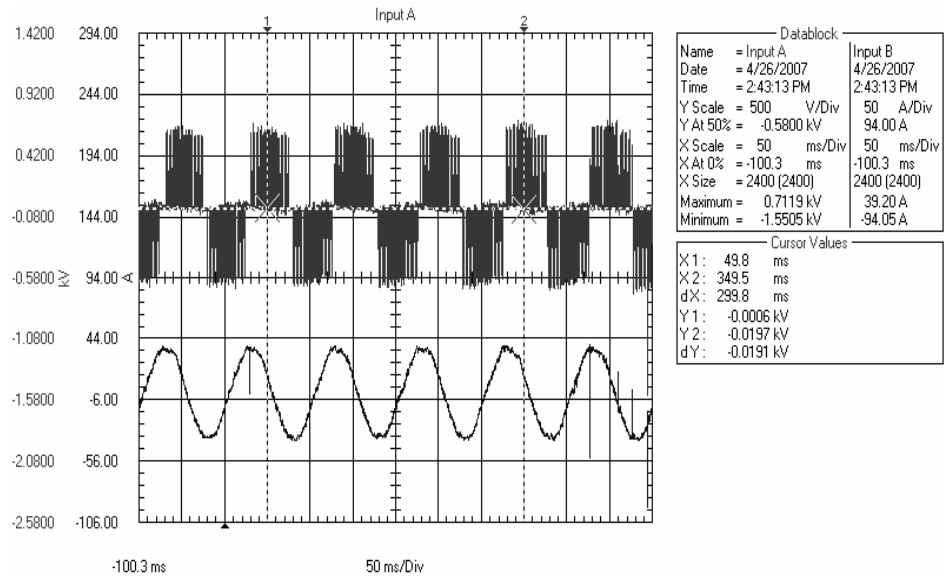


Fig.9.46 Separated Line Voltage and Line Current Waveforms at 10 Hz, DTC Gain =70
(X- axis: 1 div = 50 ms, Y- axis: 1 div= 50 A, 1 div= 500 V)

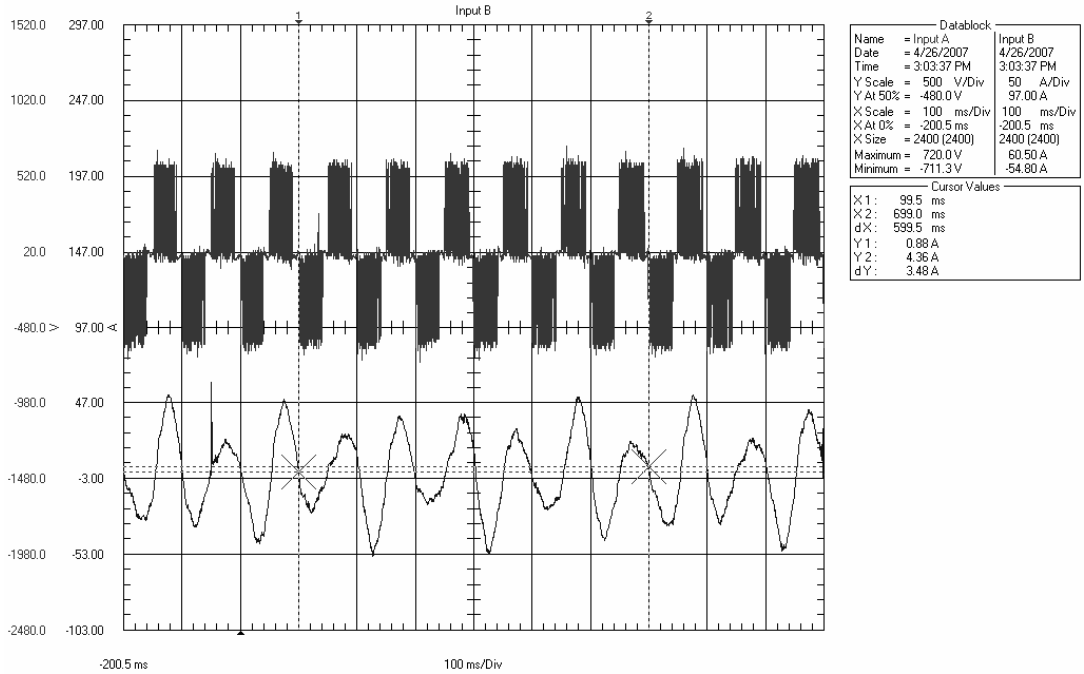


Fig.9.47 Line Voltage and Line Current Waveforms at 10 Hz, DTC Gain =0
(X- axis: 1 div = 100 ms, Y- axis: 1 div= 50 A, 1 div= 500 V)

9.9 ANALYSIS OF THD FOR THREE-LEVEL AND TWO-LEVEL INVERTERS

The THD of three-level and two-level inverter has been found using fluke software for different frequencies. The analyses of THD are summarized in Table-9.2 and Table-9.3 for three-level and two-level inverter respectively. THD for line voltage and line current waves in two-level inverter is more than three-level inverter.

TABLE – 9.2
THD FOR THREE-LEVEL INVERTER

Sr. No.	Input by Keypad			THD Voltage (%)	THD Current (%)
	A101 Set Freq. (Hz)	B110 Carrier Freq. (KHz)	B111 DTC Gain		
1	50	2.5	110	18.52	3.35
2	40	2.5	110	34.97	4.38
3	30	2.5	110	27.47	4.46
4	20	2.5	110	39.09	5.03
5	10	2.5	110	61.97	8.50

TABLE – 9.3
THD FOR TWO-LEVEL INVERTER

Sr. No.	Input by Keypad			THD Voltage (%)	THD Current (%)
	A101 Set Freq. (Hz)	B110 Carrier Freq. (KHz)	B111 DTC Gain		
1	50	2.5	70	54.75	5.23
2	40	2.5	70	47.33	5.12
3	30	2.5	70	31.07	5.12
4	20	2.5	70	68.18	4.80
5	10	2.5	70	31.93	5.74

CHAPTER-10
CONCLUSION AND SCOPE FOR FUTURE WORK

10.1 GENERAL

This chapter includes important conclusions drawn for this project work. It also included scope for future work and research.

10.2 CONCLUSION

From experimental result, it is concluded that Neutral point Clamped topology can be used for three-level inverter. It has problem of DC-link capacitor voltage balancing. It can be solved using SVPWM open loop (self balancing) & closed loop capacitor voltage balancing scheme. The results presented in this report demonstrate the ability of the open loop (self-balancing) SVPWM and the Pulse Based Dead Time Compensation Method to provide stable operation for ac induction motor. The pulse based dead time compensation method is independent of operating frequency, carrier frequencies, and the load. Pulse Based Dead Time Compensation Method is software intensive, so it is easy to implement.

Following points to be concluded from analysis,

- The neutral point clamped (NPC) topology is optimum solution for three-level inverter. Three-level inverter can be used for medium voltage drive.
- The SVPWM Scheme gives two-level operations on 25 HZ (at modulation index mi=0.865).
- The pulse based dead time compensation method gives good results for three-level inverter for any operating frequency.
- The optimum dead time compensation gain should be 110. The effect of dead time compensation is significant on motor current at low frequency (below 20 Hz).
- The open loop (self balancing) SVPWM scheme should provide stable voltage across upper and lower capacitors for NPC topology.

- DC Link voltage deviation between upper and lower capacitors should be less than 10 volt. If DC Link voltage deviation increased more than 10 volt, closed loop SVPWM capacitor voltage balancing scheme can be used.
- Increasing carrier frequency should reduce output motor current ripple.
- THD in voltage and current is reduced at higher frequency.
- During heat run test the maximum temperature rise is 31 ˚C, which can be allowable.
- Optimum DTC gain for two-level inverter is 70.
- The THD in line voltage and line current is less in three-level inverter than two-level inverter.
- The surge voltage in three-level inverter is less in PWM output line voltage than two-level inverter. So the motor insulation bearing life has been increased.

10.3 SCOPE FOR FUTURE WORK

Following points propose future scope and research,

- Development of three-level inverter for high input voltage and high power as per customer's requirement.
- Development of vector controlled three-level inverter fed induction motor drive.

REFERENCES

[1] José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", IEEE Transactions On Industrial Electronics, Vol. 49, No. 4, pp.724-738, August 2002.

[2] Keith Corzine, "Operation and Design of Multilevel Inverters", University of Missouri – Rolla, Revised June 2005

[3] Fei Wang, "Sine-Triangle versus Space-Vector Modulation for Three-Level PWM Voltage-Source Inverters", IEEE Transactions On Industry Applications, Vol. 38, No. 2, March/April 2002.

[4] Kalpesh H. Bhalodi, and Pramod Agrawal, "Space Vector Modulation with DC-Link Voltage Balancing Control for Three-Level Inverters", IEEE Conf. PEDES, Dec.2006, pp.1-6.

[5] Aye Kocalmý and Sedat Sünter, "Simulation of a Space Vector PWM Controller For a Three-Level Voltage-Fed Inverter Motor Drive", IEEE- 2006, pp.1915-1920

[6] Nikola Celanovic, and Dushan Boroyevich, "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters", Vol. 15, No. 2, March 2000

[7] Josep Pou, "Chapter-3 Space-Vector PWM" Technical University of Catalonia

[8] R.S. Kanchan, M.R. Baiju, K.K. Mohapatra, P.P. Ouseph and K. Gopakumar "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages", IEE Proc.-Electr. Power Appl., Vol. 152, No. 2, pp.297-309, March 2005.

[9] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC Link Capacitor Voltage Balancing for an Open-End Winding Induction Motor Drive" IEEE Transactions On Power Electronics, Vol. 21, No. 6, November 2006.

[10] Bai Hua, Zhao Zhengming, Meng Shuo,Liu Jianzheng, Sun Xiaoying "Comparison of Three PWM Strategies SPWM,SVPWM & One-cycle Control", 2003 IEEE.

[11] Hyo L. Liu, Nam S. Choi, and Gyu H. Cho, "DSP Based Space Vector PWM for Three Level Inverter with DC Link Voltage Balancing" IECON-1991, IEEE.

[12] David Leggate, and Russel J. Kerkman, "Pulse Based Dead Time Compensator for PWM Voltage Inverters", IEEE.

[13] Zhichao Liu, Pengju Kong, Xuezhi Wu and Lipei Huang **"**Implementation of DSP-based three-level inverter with dead time compensation", Power Electronics and Motion Control Conference, IPEMC 2004, Volume 2, Aug. 2004, pp. 782 - 787

[14] Dongsheng Zhou and Rouaud, D.G**. "**Dead-time effect and compensations of three-level neutral point clamp inverters for high-performance drive applications" IEEE Transactions on Power Electronics,Volume 14,Issue4, pp.782 – 788, Jul.1999

[15] J. 0. P. Pinto, B. K. Bose, L. E. B. Da Silva and M. P. Kazmierkowski, "Neural-network-based space-vector PWM controller for voltage-fed inverter induction motor drive", IEEE Trans. Ind. App., vol. 36(6), pp. 1628-1636, Nov/Dec 2000.

[16] H. L. Liu, N. S. Choi, and G. H. Cho, "DSP based space vector PWM for three-level inverter with DC-link voltage balancing," in Proc. IEEE IECON Conf., 1991, pp. 197–203.

[17] K. R. M. N. Ratnayake, Y. Murai, T. Watanabe, "Novel PWM scheme to control neutral point voltage variation in three-level voltage source inverter", in proc. 1999 of IEEE Ind. App. 34h IAS Annual Meeting Conf:, vol. 3, pp.1950 - 1955.

[18] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM Inverters", in Proc. 1993IEEE Industrial Applications Society Conf:, pp. 965-970.

[19] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral point clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523,Sep./Oct. 1981.

[20] Nikola Celanovic and Dushan Boroyevich, "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped

Voltage Source PWM Inverters", IEEE transactions on power electronics, vol. 15, no. 2, pp.242-249, March 2000.

[21] C. Newton and M. Summer, "Neutral point control for multi-level inverters: Theory, design and operation limitations," in Proc. 1997 IEEE IAS Conf: Rec., pp. 1336-1343.

[22] K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga and T. J. Kume, "A novel neutral potential stabilization technique using the information of output current polarities and voltage vector," IEEE Trans. on Ind. App., vol. 38(6), pp. 1572-1580, Nov/Dec. 2002.

[23] D. Leggate and R. J. Kerkman, "Pulse-based dead-time compensator for PWM voltage inverters," IEEE Trans. Ind. Electron., vol. 44, pp. 191–197, Apr. 1997.

[24] Jong-Lick Lin,"A New Approach of Dead-Time Compensation for PWM Voltage Inverters", IEEE Transactions On Circuits And Systems,Fundamental Theory And Applications, Vol. 49, No. 4, pp. 476 – 483, April 2002

[25] Bin Wu, "High Power converters and AC Drives", 2006, IEEE Press, Chapter-7-8, pp 119-177.

[26] Hamid A. Toliyat and Steven Campbell, "DSP Based Electromechanical Motion Control", CRC Press.

[27] Muhammad. H. Rashid, "Power Electronics; Circuits, Devices, and applications", 3rd edition, Prentice Hall of India, chapter-9, pp 406-430.

[28] Ned Mohan, Tore M. Undeland, William P. Robbins, "Power Electronics, Converters, Applications and Design", 2nd edition, John Wiley & Sons (India).

[29] Bimal K. Bose, "Modern Power Electronics and AC Drives", International edition, Prentice Hall (PTR), Upper Sadle River, New Jersy.

[30] "Digital Motor Control", Software Library, Digital Control System (DCS) Group, SPRU-485, August 2001, Texas Instruments, page no. 190.

[31] "TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 Digital Signal Processors Data Manual" Literature Number: SPRS174N.

LIST OF PAPERS PUBLISHED AND UNDER REVIEW

PAPER PUBLISHED:

[1] Pinkal J. Patel, Rakesh A. Patel, Vinod Patel, and P. N. Tekwani, "Simulation of Self Balancing Space Vector Switching Modulator for Three-Level Inverter," CIPS-2008, 2nd National Conference on Computational Intelligence in Power Apparatus and Systems, IEEE Madras Section, SRM University, Chennai,pp.67-72, 18-19/April/ 2008.

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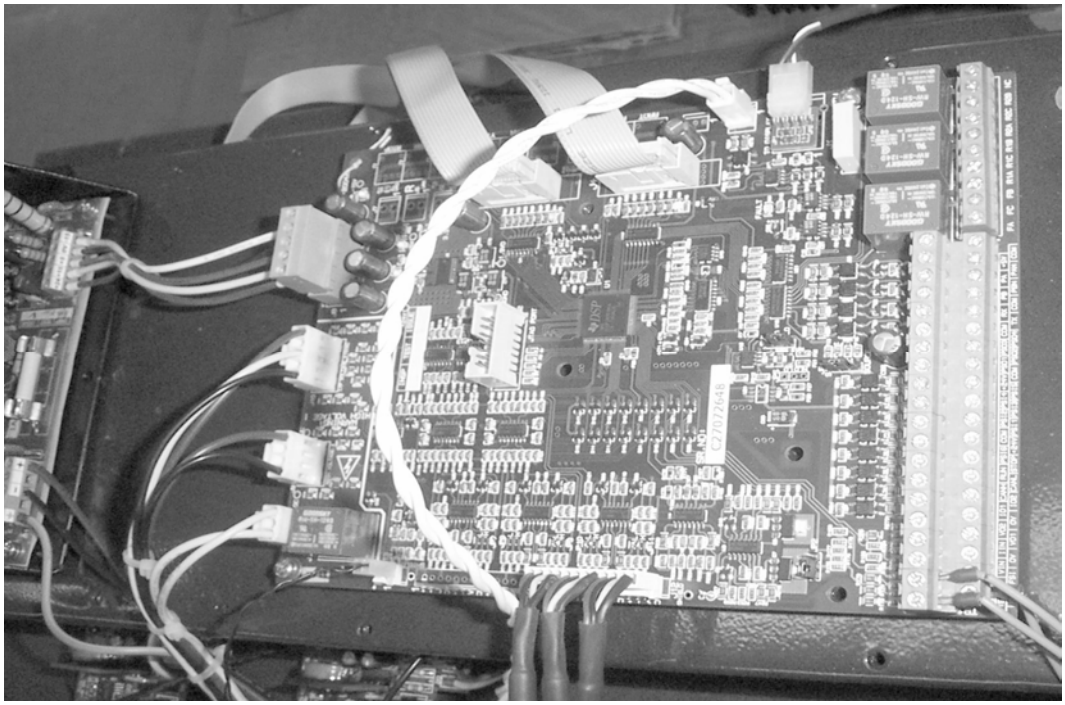
[1] Pinkal J. Patel, Rakesh A. Patel, Vinod Patel, and P. N. Tekwani, "Implementation of Self Balancing Space Vector Switching Modulator for Three-Level Inverter"

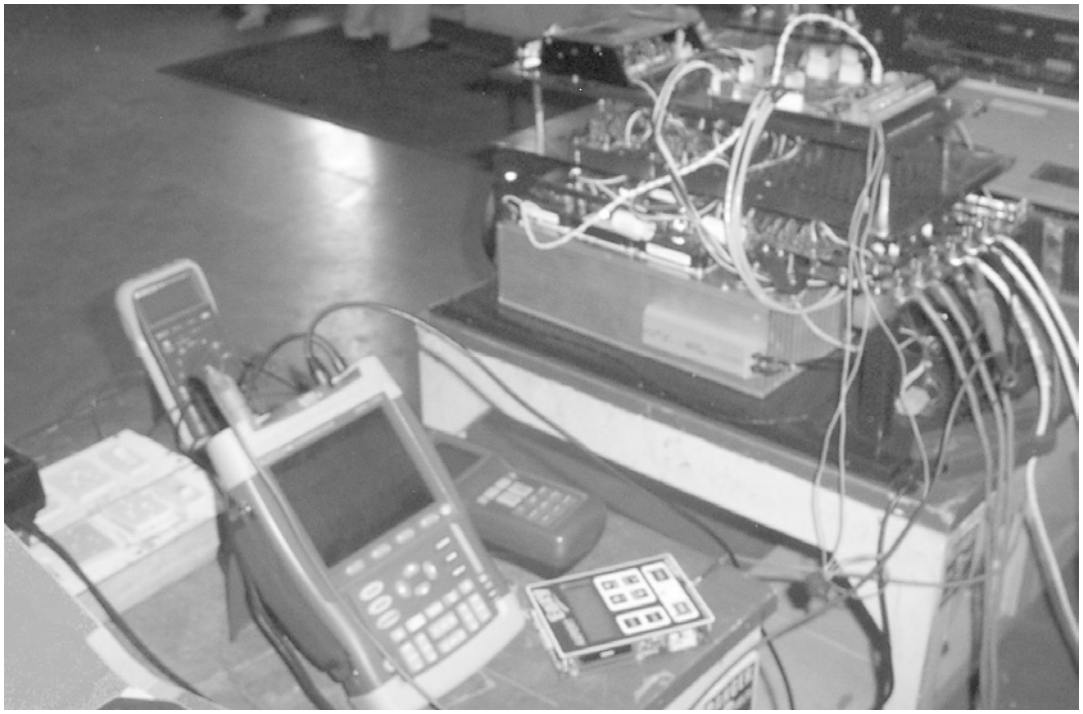
[2] Pinkal J. Patel, Rakesh A. Patel, Vinod Patel, and P. N. Tekwani, "Pulse based Dead Time Compensation Method with SVPWM Scheme for Three-Level Inverter"

APPENDIX-A
PHOTOGRAPHS OF HARDWARE

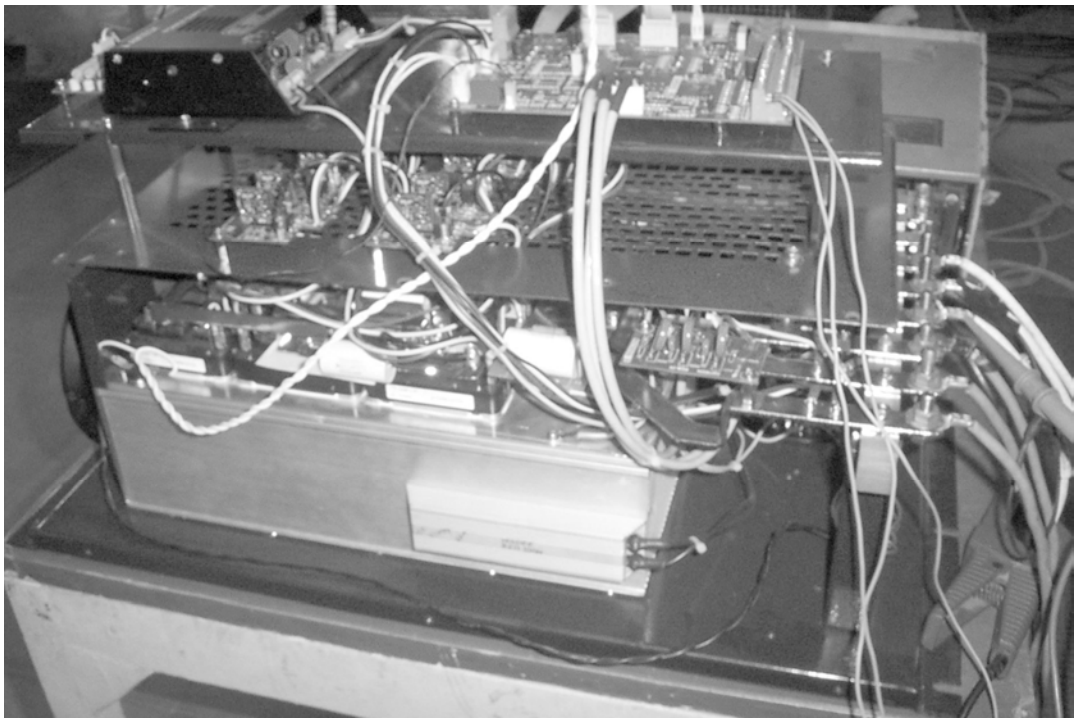
CONTROL CARD



HARDWARE SETUP



THREE-LEVEL INVERTER



APPENDIX-B
TMS320 FAMILY OVERVIEW

The TMS320 family consists of fixed point, floating point, multiprocessor digital signal processors and fixed point DSP controllers. TMS320 DSP's have architecture designed specifically for real time signal processing. The 'F28xx' series of DSP controllers combines this real time processing capability with controller peripherals to create an ideal solution for control system applications. The following characteristics make the TMS320 family the right choice for a wide range of applications.

- Very flexible instruction set
- Inherent operational flexibility
- High-speed performance
- Innovative parallel architecture
- Cost effectiveness

TMS320F28xx SERIES OF CONTROLLERS

Designers have recognized the opportunity to redesign the existing systems to use advanced algorithms that yield better performance and reduce system component count. DSP's enable:

- Design of robust controllers for a new generation of inexpensive motors
- Elimination or reduction of memory looks up tables through real time polynomial calculations, there by reducing system cost.
- Use of advanced algorithms that can reduce the number of sensors required in a system.
- Control of power switching inverters, along with control algorithm processing
- Single processor control of multi motor systems

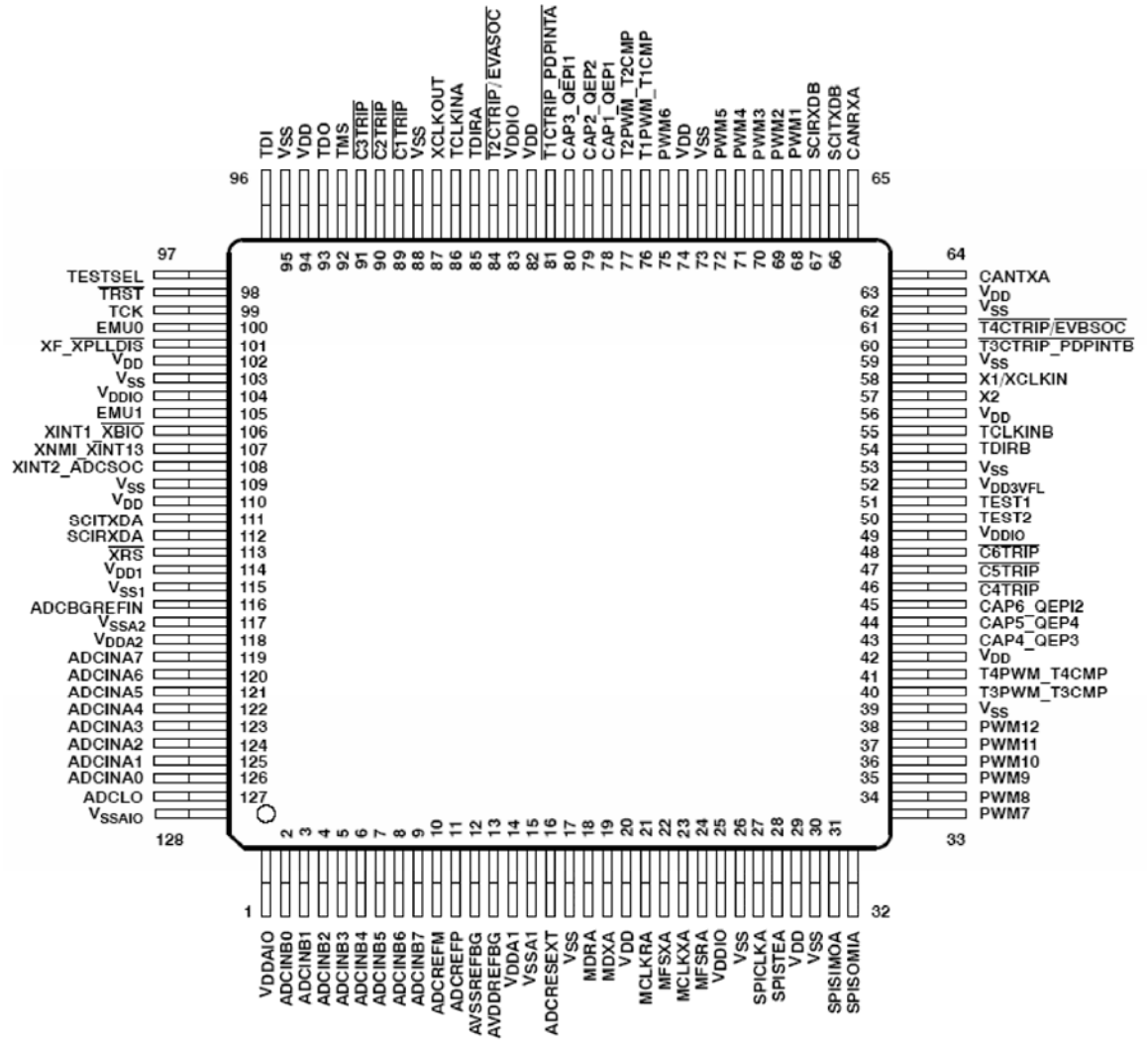
FEATURES OF TMS320F2811

- High-Performance Static CMOS Technology
  150 MHz (6.67-ns Cycle Time)
  Low-Power (1.8-V Core @135 MHz, 1.9-V Core @150 MHz, 3.3-V I/O) design
- High-Performance 32-Bit CPU (TMS320C28x)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - 4M Linear Program/Data Address Reach
  - Code-Efficient (in C/C++ and Assembly)
  - TMS320F24x/LF240x Processor Source Code Compatible
- On-Chip Memory
  - Flash Devices: Up to 128K x 16 Flash
  - ROM Devices: Up to 128K x 16 ROM
  - 1K x 16 OTP ROM
  - L0 and L1: 2 Blocks of 4K x 16 Each Single-Access RAM (SARAM)
  - H0: 1 Block of 8K x 16 SARAM
  - M0 and M1: 2 Blocks of 1K x 16 Each SARAM
- Boot ROM (4K x 16)
  - With Software Boot Modes
  - Standard Math Tables
- Clock and System Control
  - Dynamic PLL Ratio Changes Supported
  - On-Chip Oscillator
  - Watchdog Timer Module
- Three External Interrupts
- Peripheral Interrupt Expansion (PIE) Block That Supports 45 Peripheral Interrupts
- Three 32-Bit CPU-Timers
- 128-Bit Security Key/Lock
  - Protects Flash/ROM/OTP and L0/L1 SARAM
  - Prevents Firmware Reverse Engineering
- Motor Control Peripherals
  - Two Event Managers (EVA, EVB)
  - Compatible to 240xA Devices
- Serial Port Peripherals
  - Serial Peripheral Interface (SPI)
  - Two Serial Communications Interfaces (SCIs), Standard UART
  - Enhanced Controller Area Network (eCAN)
  - Multichannel Buffered Serial Port (McBSP)

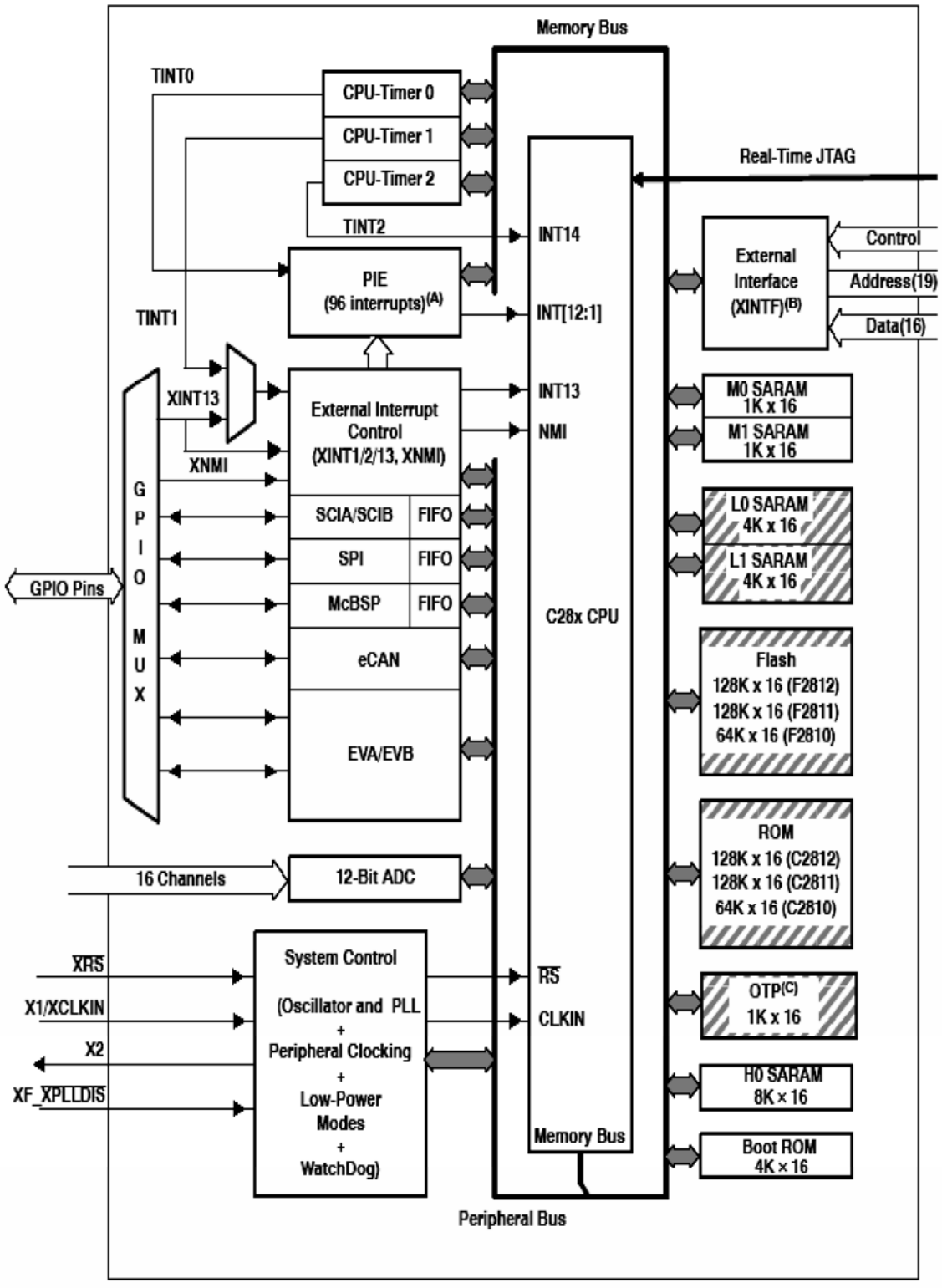
- 12-Bit ADC, 16 Channels
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Fast Conversion Rate: 80 ns/12.5 MSPS

- Up to 56 General Purpose I/O (GPIO) Pins
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Temperature Options:
  - A: -40°C to 85°C (GHH, ZHH, PGF, PBK)
  - S/Q: -40°C to 125°C (GHH, ZHH, PGF, PBK)

PIN DIAGRAM



FUNCTIONAL OVERVIEW



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