Design and Simulation of 2.4 GHz Frequency Synthesizer

Major Project Report

Submitted in partial fulfillment of the requirements

For the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Patel Dharmesh Babubhai

(11MECV08)

Department of Electrical Engineering

Electronics & Communication Programme

Institute of Technology,

Nirma University, Ahmedabad-382 481

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Under the Guidance of

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MAY 2013

Declaration

This is to certify that

(i) The thesis comprises my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

(ii) Due acknowledgement has been made in the text to all other material used.

Patel Dharmesh Babubhai

Certificate

This is to certify that the Major Project entitled **"DESIGN AND SIMULATION OF 2.4 GHz FREQUENCY SYNTHESIZER** submitted by **Patel Dharmesh B.(11MECV08)**,towards the partial fulfillment of the requirements for the degree of **Master of Technology (VLSI Design)** in the field of **Electronics and Communication** of Nirma University is the record of work carried out by him under our supervision and guidance. The work submitted has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, have notbeen submitted to any other University or Institution for award of any degree or diploma.

Date: Place:Ahmedabad

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Acknowledgement

I would like to thank Dr.N.M Devashrayee Co ordinator M.Tech VLSI & Design program and Prof.N.P Gajjar Associate Professor in M.Tech in E.C Department for all their timely and useful guidance and help which resulted in the successful completion of thesis report.

I would like to thank Dr. P.N.Tekwani Head of Department of Electrica Engineering. I would like to express my gratitude and sincere thanks to Prof.Amisha Naik Assstant Professor in Electronics & Communication Engineering Department for allowing me to undertake this thesis work and for his guidelines during the review process.

I would like to thank to Dr K Kotecha Director of Institute of Technology Nirma University.

Iwould like to thank all the faculty members of Department of Electronics & Communication Engineering and my co students, for providing me all the necessary guidance through out the term which provides lots of help in course of my project work. I am also thankful to the authors whose works I have consulted and quoted in this work. My affectionate thanks are due to my family who made me able to do such work.

-Patel Dharmesh B.

(11MECV08)

Abstract

A PLL(Phase locked loop) [1]is a closed loop frequency system that locks the phase of an output signal to an Input reference signal. The term lock refers to a constant or zero phase difference between two signals. The signal from the feedback path, F_{fb}, is compared to the Input reference signal,F_{ref}, until the two signals are locked. If the phase is unmatched, this is called the unlocked state, and the signal is sent to each component in the loop to correct the phase difference. These components consist of the Phase Frequency Detector (PFD)[1][2],Charge pump (CP)[1], Low pass filter (LPF)[1], and The Voltage controlled oscillator (VCO) and Frequency Divider. The PFD detects any phase differences in fref and ffb and then generates an error signal. According to that error signal the CP either increases or decreases the amount of charge to the LPF. This amount of charge either speeds up or slows down the VCO. The loop continues in this process until the phase difference between fref and ffb is zero or constantthis is the locked mode. After the loop has attained a locked status, the loop still continues in the process but the output of each component is constant. The output signal, fout, has the same phase and/or frequency as fref.

PLLs (Phase Locked Loop) are commonly used in communications systems in wireless application and wireless sensor the frequency synthesizer is designed to operate using a reference signal 20 MHz producing an output signal 2.4 GHz A 1.8 V CMOS 2.4 GHz frequency synthesizer with low phase noise and power is presented. Low power consumption and phase noise is achieved by using a Current Starved VCO. The synthesizing frequencies 2.4GHz The divider network is designed using dynamic true single-phase logic (TSPC) for low power operation. The 2.4 GHz frequency synthesizer is designed using 0.18μm TSMC CMOS 1P6M Technology.

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Chapter 1

Introduction

1.1 Motivation

The popularity of wireless technology in the area of communications and growth in very large-scale system integration (VLSI) low cost technology has opened doors for a variety of phase-locked loop (PLL) based complementary metal-oxide semiconductor(CMOS) frequency synthesizers. One of the key elements of the PLL frequency synthesizers is the voltage-controlled oscillator (VCO). The Current Starved oscillators are preferred for frequency synthesizers used in radio frequency (RF) applications. The Current staved (Ring oscillator) is achieves important VCO criteria of low phase noise, low power dissipation, and a large tuning range. True single-phase clock (TSPC) dynamic logic divider circuit, has the advantages of fast operation, low area, and power dissipation. The synthesizer design and circuit implementation was performed for a wireless applications, wireless sensor network, medical application etc.

1.2 Application: Clock Generator and Frequency synthesizer

The input of the PLL is a reference frequency, fref from the user. The VCO sends another input frequency, ffb into the PFD to compare the reference frequency with the VCO frequency. After the PLL corrects the frequency to have zero offset phase, or to be in the lock mode, the frequency is taken as an output at the VCO, fout. Therefore, a frequency is synthesized. (Note: Constraints on the input frequency, fref, must be within the tuning range of the VCO and the PLL as a whole system. The tuning range is the range in which the VCO functions properly. If fref isnt within this tuning range, a divider is necessary). A divider can be used in the feedback path to synthesize a frequency different than that of the reference signal. Furthermore, since the reference signal is a clock signal, the output is also a clock signal thus a clock generator.

1.3 Scope

The frequency synthesizer[2] generates 2.4 GHz signal for wireless applications. The Taiwan semiconductor manufacturing company (TSMC) 0.18μm CMOS technology is used. The design goals are low phase noise, small area, and low power consumption. The phase frequency detector (PFD) is dead zone free for improved performance The schematics and layouts for Ring oscillator, TSPC divider[11], PFD, charge pump (CP), and low pass filter (LPF) were Designed with Design Architect and IC Station, simulated using Eldo tool(Mentro Graphics).

1.4 Outline of Thesis

This thesis presents the design and Simulation of a 2.4GHz frequency synthesizer for Wireless applications. The contents of this document have been organized in a

logical sequence. A brief description of the contents of each chapter is given below.

Chapter 2 Explain the introduction of PLL Architecture.

Chapter 3 Explain the Brief Overview of Frequency Synthesizer.

Chapter 4 Explain an Overview of the design and Simulation Result of the Frequency Synthesizer

Chapter 5 Conclusion and Future work

1.5 Design Specification of 2.4 GHz Frequency Synthesizer.

Sr.No	Parameter	Specification
1	Technology	0.18μm TSMC CMOS
2	Supply Voltage	1.8V
3	Reference Frequency	20MHz
4	OutPut Frequency	2.4 GHz
5	Charge Pump Current	50μA
6	Loop Filter Component	C1 10pF C2 110 pF R2 10kΩ R3 20kΩ C3 5 pF
7	Cutoff Frequency(f_c)	1.72MHz
8	Dumping (ξ)	0.76
9	Settling Time	<1.6μs
10	Divide Ratio	120

Table 1.1: Design Specification of 2.4 GHz Frequency Synthesizer[2]

Chapter 2

Basic PLL Architecture

A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals (refer to Figure 2.1). The overall goal of the PLL is to match the reference and feedback signals in phase this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant. A basic form of a PLL consists of four main blocks:

- Phase Detector(PD/PFD)
- Loop Filter
- Voltage Control Oscillator(VCO)

A block diagram of the basic component of the PLL is shown in figure

2.1 Phase Detector

It compares the phase of the incoming signal with the phase of the output signal of the Voltage Controlled Oscillator(VCO) and produces an output voltage, which is

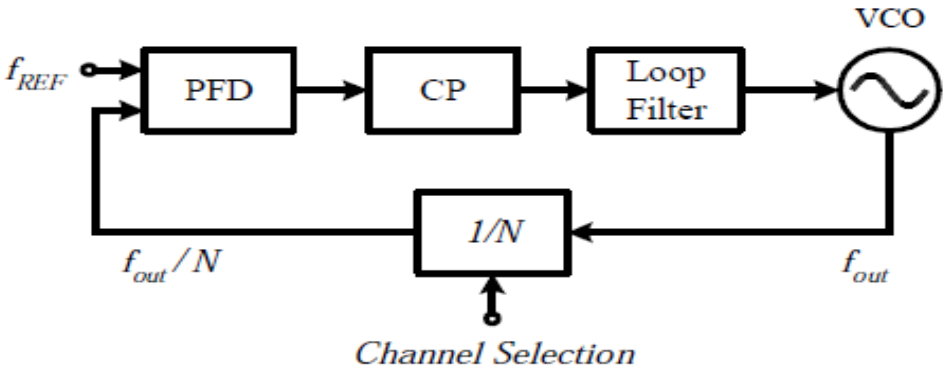

Figure 2.1: PLL architecture[12]

proportional to the phase difference between the two signals. For digital application two types phase detector widely used.

- XOR Phase Detector (XOR PD)
- Phase Frequency Detector(PFD)

2.2 Loop Filter

A filter is typically needed between the phase detector and voltage controlled oscillator to achieve the desired lock characteristics.

2.3 Voltage Controlled Oscillator

A voltage controlled oscillator (VCO) has a oscillatory output with a frequency proportional to an input voltage. The VCO allows the on-chip frequency to vary. In DPLL applications this feature allows the VCO to be used a feedback look to sync with (or lock on) to the reference signal

Chapter 3

Overview of Frequency Synthesizer

3.1 Introduction

In this chapter different frequency synthesizer[8][6] architectures are discussed. The role of radio frequency (RF) communication frequency synthesizers is highlighted. The general terms and considerations used in RF frequency synthesizers are discussed with an emphasis on critical parameters, such as phase noise, chip area, and power dissipation.

3.2 Synthesizer Architectures

There are many ways to implement frequency synthesizers. The desired frequency synthesizer used for Bluetooth RF communication should be able to generate giga hertz frequencies with low phase noise, low power, and minimum chip area. The frequency synthesizer design architecture is selected based on application. The direct digital frequency synthesizer (DDFS) is used for the applications where fast frequency switching is required. It is suitable for the low frequency applications. It has no of-chip components and hence meets minimum chip area constraints. But

the power Requirements are very large due to the requirement for a RF frequency DAC and not feasible for 2.4 GHz frequency applications.

3.3 Direct Digital Frequency Synthesizers (DDFS)

The direct digital frequency synthesizer[7] consists of a digital phase accumulator, read-only memory (ROM) containing a look-up table, and digital to analog converter (DAC). The digital phase accumulator accumulates phase at every clock cycle until its maximum count is reached. Depending on the accumulated phase, a word is set at the end of every clock cycle. This word is then translated into a corresponding frequency by the look-up table stored in the ROM. This digital word is then fed to the digital to analog converter, which gives the desired output frequency . In this architecture, digital to analog converter consumes very large power and hence DDFS is not used for Bluetooth RF synthesizer applications. The clock is typically three times greater than the output frequency. frequency . In this architecture, digital to analog converter consumes very large power and hence DDFS [7]is not used for Bluetooth RF synthesizer applications. The clock is typically three times greater than the output frequency. The block diagram is shown in Figure 2.

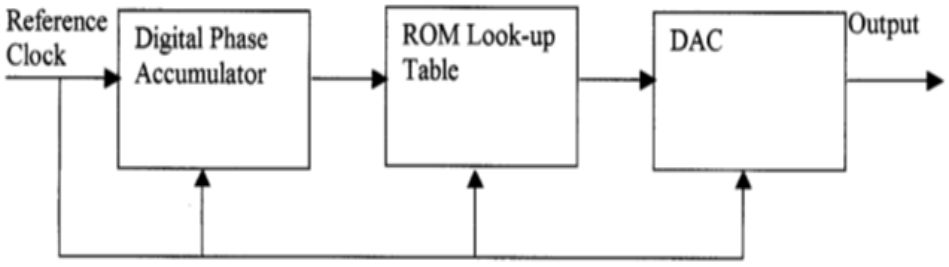

Figure 3.1: Direct digital frequency synthesizer[7]

3.4 PLL Based Frequency Synthesizers

3.4.1 PLL Based integer N Frequency Synthesizer

PLL based integer N frequency synthesizers [2]consist of a phase frequency detector (PFD), a charge pump (CP)[1], a low pass filter (LPF)[1], a voltage controlled oscillator (VCO), and The feedback loop usually contains a integer N divider. The VCO output is a high frequency signal and the phase Frequency detector compares low frequency digital signals. The block diagram is given below.

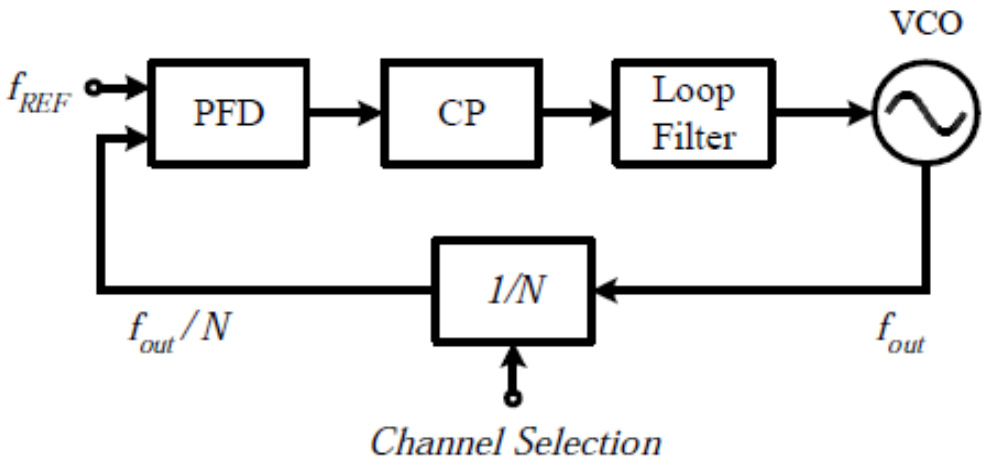

Figure 3.2: Integer N Frequency Synthesizer Architecture[12]

$$F_{ref} = \frac{F_{out}}{N} \tag{3.1}$$

The most popular technique of frequency synthesis is based on the use of a phase-locked loop (PLL). The loop is synchronized or locked when the phase of the input signal and the phase of the output from the frequency divider are aligned. As shown in Fig. 4.32 the output of the VCO in the integer-N synthesizer is divided and phase-locked to a stable reference signal. Once the loop is locked, the output frequency Integer-N architecture is the preferred solution for minimizing power consumption

and die area due to its simplicity. The integer-N architecture[11]8, however, lacks the flexibility of arbitrarily choosing F_{ref} as is possible in more complex architectures. Since F_{ref} is fixed by channel spacing requirements, the loop bandwidth can be severely limited, especially since it has to be significantly lower than F_{ref} for stability considerations. Although, the integer-N synthesizers can generate output frequencies in steps of F_{ref} , the channel spacing is not necessarily equal to F_{ref} . The maximum possible fREF can be calculated as follows: First, the channel frequencies must be integer multiples of F_{ref} as shown in Eq. (3.1), but at the same time the channel spacing also has to be an integer multiple of F_{ref}. To satisfy both conditions, the F_{ref} has to be the greatest common divisor (GCD) of the channel frequency and the channel spacing. For example, Wireless LAN 802.11b standard specifies channels from 2412 MHz to 2472 MHz in steps of 5 MHz. Thus, the maximum possible F_{ref} is GCD(2412 MHz, 5 MHz) = 1 MHz. For a different example, Wireless LAN 802.11a standard specifies a channel at 5805 MHz and a step of 20 MHz. In this case, the maximum possible $F_{ref}$is GCD(5805 MHz, 20 MHz) = 5 MHz.

3.4.2 PLL Based fractional N Frequency Synthesizer

An inherent shortcoming of the integer-N synthesizer is the limited option for the reference frequency, F_{ref}, because of the integer-only multiplication. A fractional- N synthesizer architecture solves this problem by allowing fractional feedback ratios. Shown in Fig. 3.3 the fractional-N synthesizer has a dual modulus divider that can switch its division ratio between N and N + 1. An inherent shortcoming of the integer-N synthesizer is the limited option for the reference frequency, F_{ref} , because of the integer-only multiplication. A fractional- N synthesizer architecture solves this problem by allowing fractional feedback ratios. Shown in Fig. 7, the fractional-N synthesizer has a dual modulus divider that can switch its division ratio between N and N + 1. By dividing the VCO frequency by N during K VCO cycles and N + 1

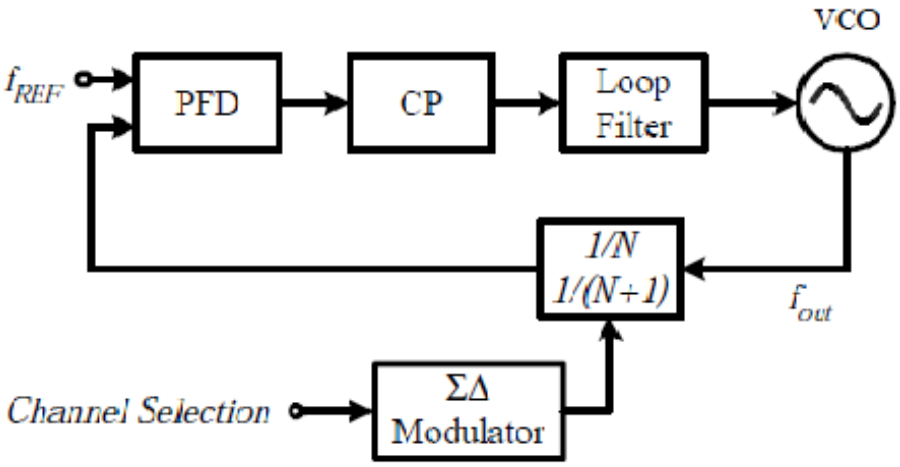

Figure 3.3: Fractional N Frequency Synthesizer Architecture[12]

during $(2^k - K)$ VCO cycles, it is possible to make the average division ratio equal to$(N + K/2^k)$ assuming a k bits accumulator controlling the prescaler. Thus,

$$F_{out} = (N + \alpha.F_{ref}), where \;\; 0 < \alpha < 1 \tag{3.2}$$

Chapter 4

Circuit Design and Simulation.

A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals (refer to Figure 4.1)The overall goal of the PLL is to match the reference and feedback signals in phase this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

A basic block of the Frequency Synthesiszer.

- Phase Detector or Phase Frequency Detector (PD or PFD)
- Charge Pump (CP)
- Low Pass Filter (LPF)
- Voltage Controlled Oscillator (VCO)
- Divide by N

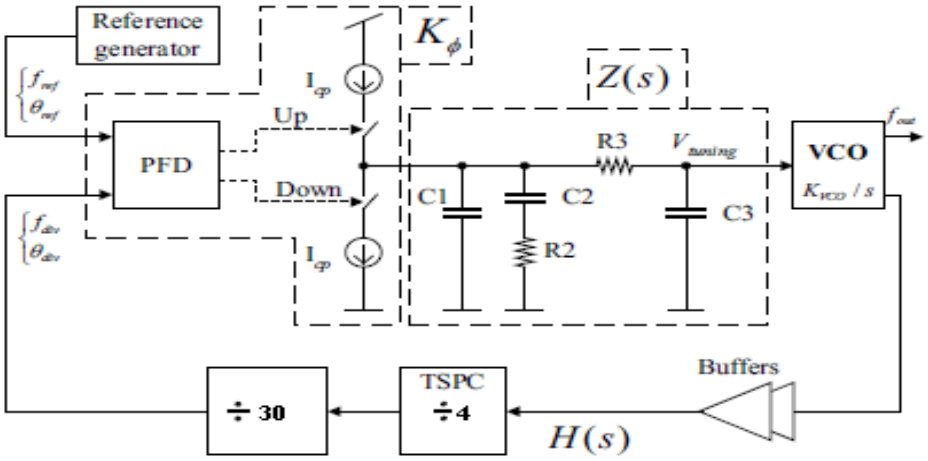

Figure 4.1: Bolck Diagram of the Frequency Synthesisizer.[2]

4.1 Phase Detector

The first component in our PLL is the phase detector. The two types of phase detectors, an XOR gate and a phase frequency detector (PFD), have significantly different characteristics. This makes understanding the limitations and performance very important. Selection of the type of phase detector is the first step in a PLL design.

4.1.1 The XOR Phase Detector

The XOR PD[1] is simply an exclusive OR gate. When the output of the XOR is a pulse train with a 50 percent duty cycle (square wave), the PLL is said to be in lock; or in other words, the clock signal out of the PLL is synchronized to the incoming data, provided the conditions stated below are met. Consider the XOR PD shown in Fig. 4.3 Let's begin by assuming that the incoming data are a string of zeros and that a divide by two is used in the feedback loop[1]. The output of the phase detector is simply a replica of the dclock signal. Since the dclock signal has a 50 percent duty cycle, it would appear that the PLL is in lock. If a logic " 1" is

suddenly applied, there is no way to know if the clock signal is synchronized (the clock rising edge coincides with the center of the data bit) to the data.

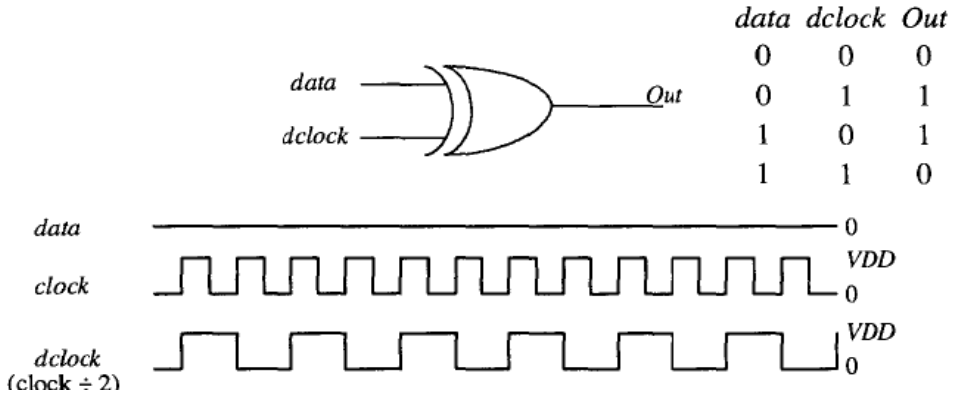

Figure 4.2: Operation of the XOR phase detector.

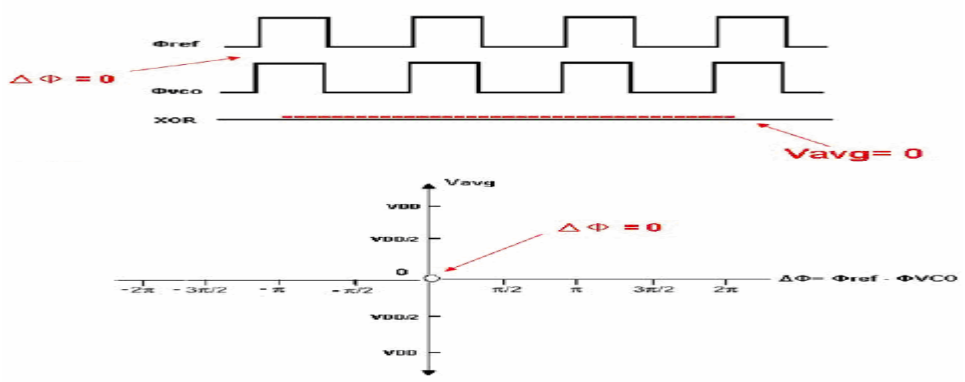

Figure 4.3: Phase Diffrence = 0

In Figure 4.4 the phase difference between the two signals is zero locked phase. The average output,V_{avg}, from the XOR gate is zero for this case. The XOR input Vs output characteristic graph is a plot of V_{avg} versus the phase difference. Figures 4.4 and Figure 4.5 plot the accumulation of points from the phase differences zero, $\pi/2$, andπ. The final graph is shown in Figure 4.7This is the XOR PD characteristic plot. This plot enables us to observe the PD output for a range of phase differences.

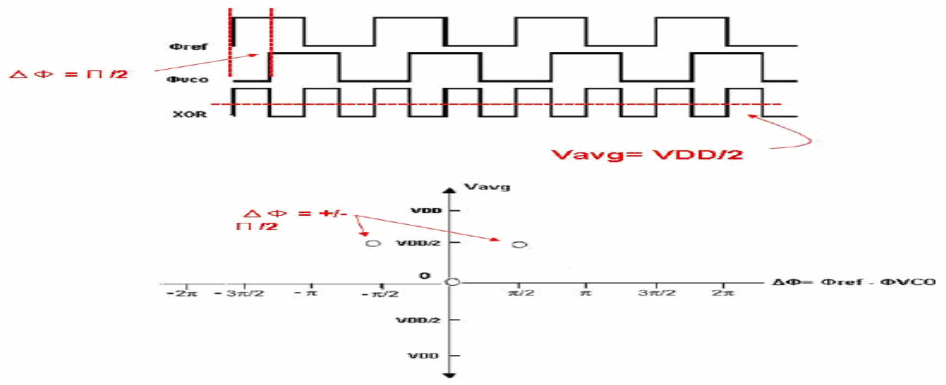

Figure 4.4: Phase difference $=\pi/2$

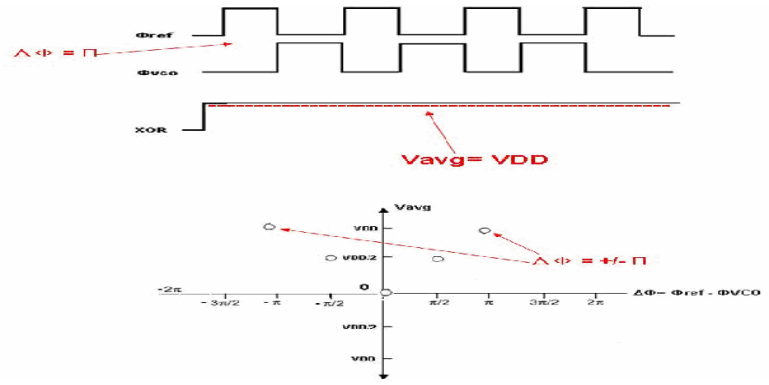

Figure 4.5: Phase difference $=\pi$

The XOR PD as shown above in Figure 4.4-4.7 is a very simple implementation of a PD, however; its major Disadvantage is that it can lock on to harmonics of the reference signal and most importantly it cannot detect a difference in frequency

The Characteristics of XOR Phase Detector.

1. The incoming data must have a minimum number of transitions over a given time interval
2. With no input data, the filtered output of the phase detector is VDD/2.
3. The time it takes the loop to lock is dependent on the data pattern input to the PLL and the loop-filter characteristics.

4. The XOR PLL has good noise rejection.
5. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO.

The Gain of PD

$$K_{pd} = \frac{VDD}{\pi}(V/radians) \tag{4.1}$$

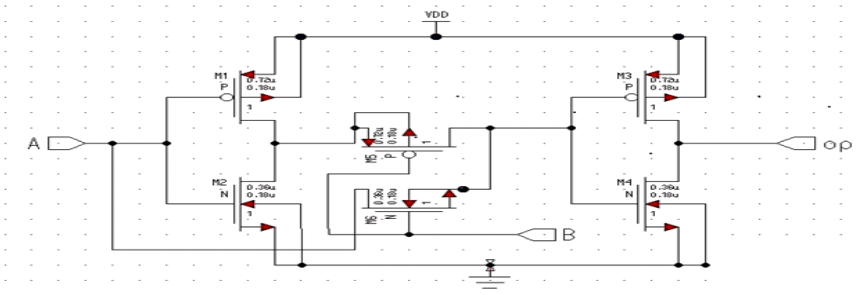

Figure 4.6: CMOS Implementation of XOR PD

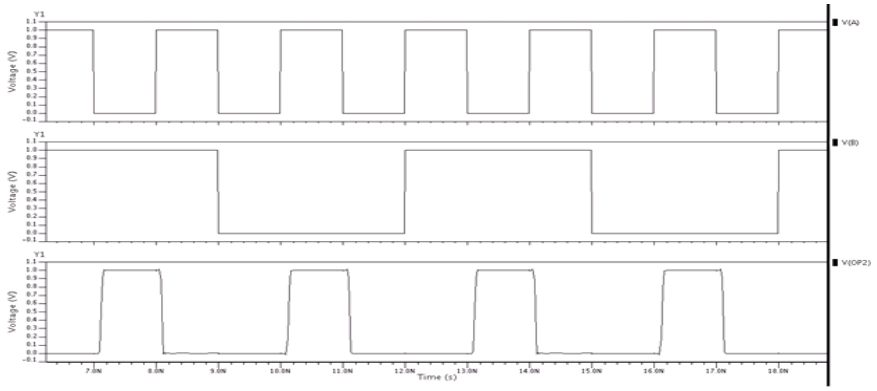

Figure 4.7: Simulation Result of XOR PD

4.1.2 Phase Frequency Dectector(PFD)

To take care of these disadvantages, we implemented the Phase Frequency Detector,[1]2 which can detect a difference in phase and frequency between the reference and feed-

back signals. Also, unlike the XOR gate PD, it responds to only rising edges of the two inputs and it is free from false locking to harmonics. Furthermore, the PFD outputs either an UP or a DOWN to the CP. The circuit schematic and Simulation Result are shown below in Figure4.8

The phase frequency detection (PFD) module is implemented with the TSPC(True Single Phase Clock) logic [1][11]as shown in Fig.2 The phase frequency detector(PFD) provide the zero dead zone. The PFD implemented with the TSPC (True Single Phase Clock) logic on the upper latch, the M1 to M6 are basically a modified version of the standard doubled n-CMOS latch with pre charge technique. The theory ofoperation is as follows .Assume f1 and f2 are both low at the start. Node A is pre charged to logic high. As f1 transition from low to high and f2 stays low, M5 is turned on and M5 turns on the inverter formed by M4 and M6. Node B is pulled low. M7 and M8 is an inverter to give the Up signal. M9 is added to fix one special problem in this architecture. Because the top and bottom latches cant be perfectly matched in delay, there will be narrow pulse for both Up and Down output even with no input phase difference. With M9, node A is discharged to GND. As f1 rises from low to high, node B is pulled up to logic high. Thus Up output will be pulled down. The bottom latch works on the same theory and Simulation wave form as shown in fig4.9

The Gain Of PFD

$$K_{pdI} = \frac{I_{pump}}{2\pi}(amp/radian) \tag{4.2}$$

The characteristics of PFD.

1. A rising edge from the dclock and data must be present when doing a phase comparison.
2. The width of the dclock and the data is irrelevant.
3. The PFD will not lock on a harmonic of the data.

4. The outputs (Up and Down) of the PFD are both logic low when the loop is in lock, eliminating ripple on the output of the loop filter.
5. This PFD has poor noise rejection; a false edge on either the data or the dclock inputs will drastically affect the output of the PFD.

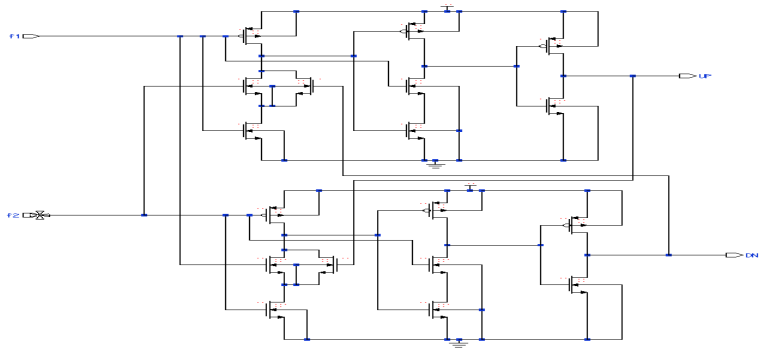

Figure 4.8: Schematic of PFD

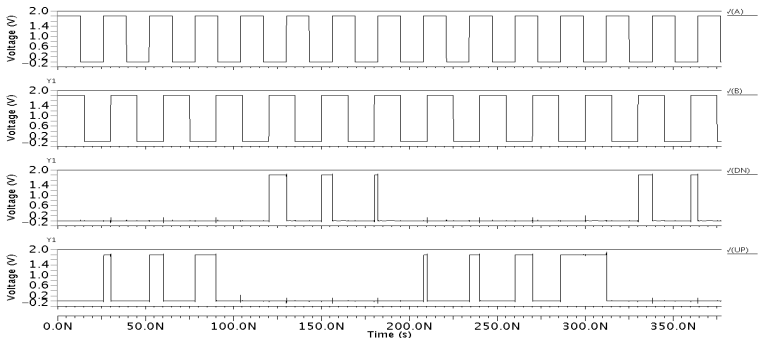

Figure 4.9: Simulation Result of PFD

	Width	**Length**
PMOS	**0.9μm**	**0.18μm**
NMOS	**0.36μm**	**0.18μm**

Table 4.1: Parameter of PFD

Layout of PFD:

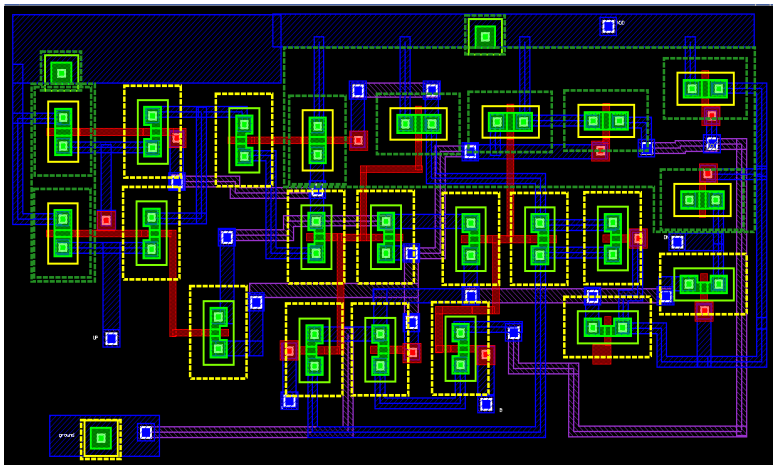

Figure 4.10: Layout of PFD

Design Rules Check Report:

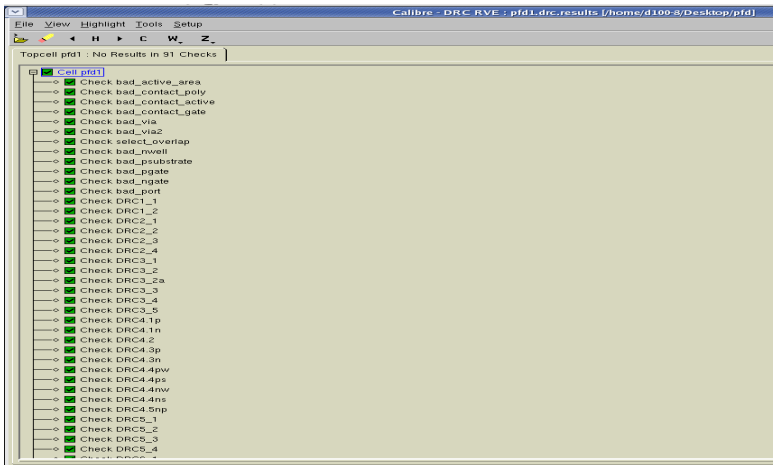

Figure 4.11: DRC Result of PFD

Layout Vs Schematic:

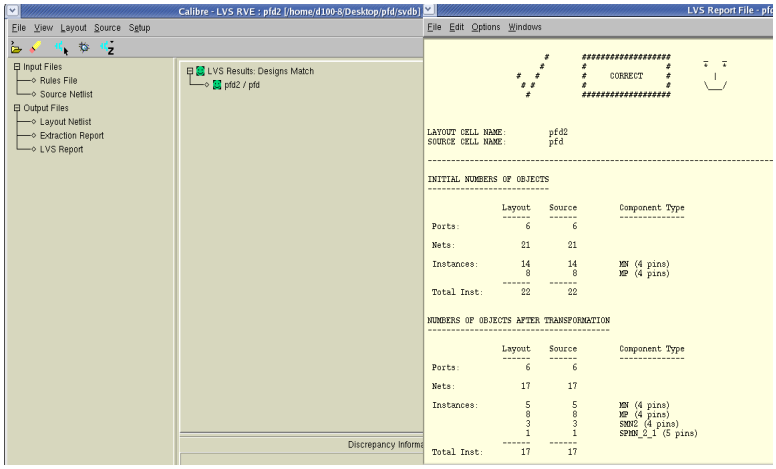

Figure 4.12: LVS Result of PFD

PEX Report:

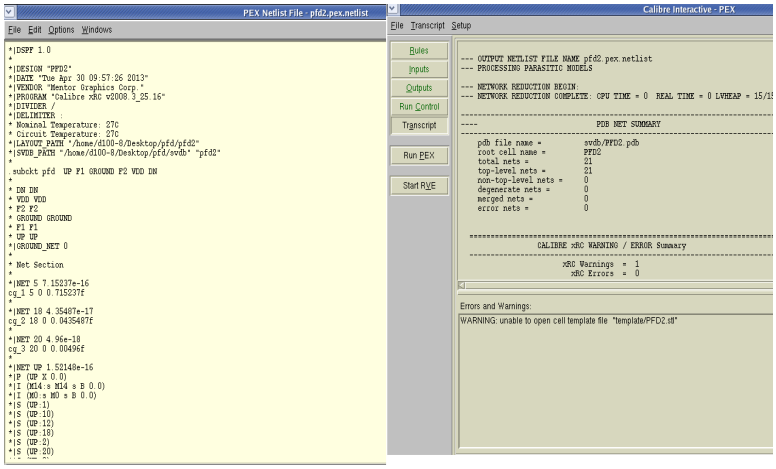

Figure 4.13: PEX Result of PFD

4.2 Charge Pump(CP)

The output of the PFD should be combined into a single output for driving the loop filter. There are two methods of doing this, both of which are shown in Fig. 4.11 The first method is called a tri-state output. When both signals, Up and Down, are low, both MOSFETs are off and the output is in a high-impedance state. If the Up signal goes high, M2 turns on and pulls the output up to VDD while if the Down signal is high the output is pulled low through Ml. The main problem that exists with this configuration is that the power supply variations can significantly affect the output voltage when M2 is on. The effect is to modulate the VCO control voltage. This wasn't as big a problem when the XOR PFD was used because of the averaging taking place. The second configuration shown in this figure is the so-called charge pump. MOS current sources are placed in series with Ml and M2. When the PFD Up signal goes high, M2 turns on, connecting the current source to the loop filter. Since the current source can be made insensitive to supply variations, modulation of the VCO control voltage is absent and Charging and discharging current of charge pump is shown in fig.4.12

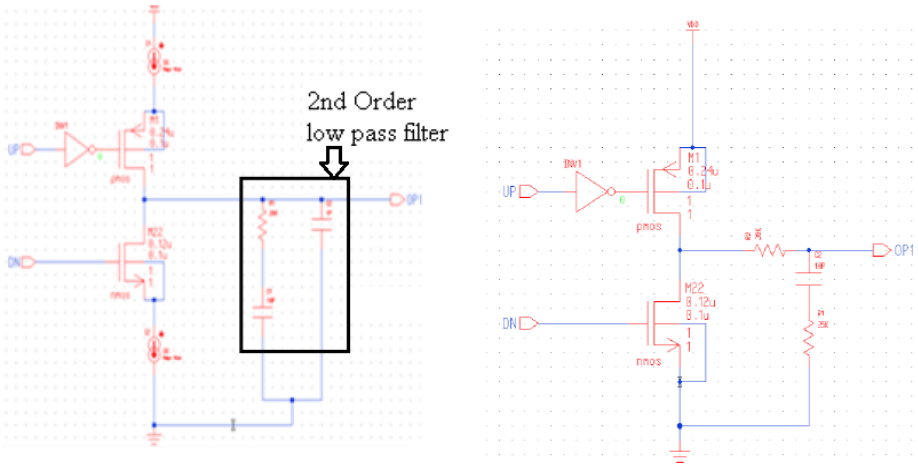

Figure 4.14: Charge pump and Tristate.[4]

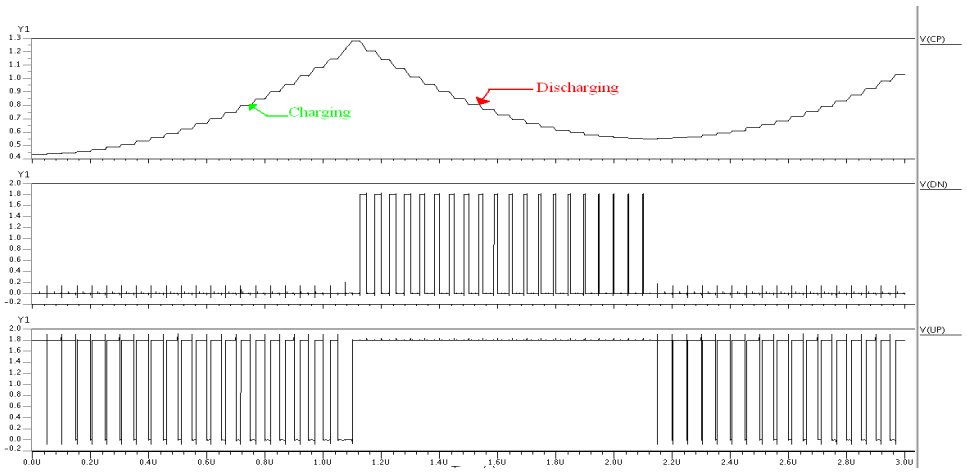

Figure 4.15: Charging and Discharging Current of Charge Pump.

State	M1	M2	Vout
UP	ON	OFF	Rise/Charge
HOLD	OFF	OFF	Hold/Lock
DN	OFF	ON	Fall/Discharge

Table 4.2: Three State Of CP/PFD

This charge pump[4][7]consists of two switched current sources that pump charge into or out of the loop filter according to the PFD output. When the reference leads the feedback signal, the PFD detects a rising edge on the reference frequency and it will produce an up signal. This up signal from the PFD will turn the UP switch on, and it will cause the CP to inject current into the loop filter, increasing Vcntrl. When the feedback leads the reference signal, the PFD detects a rising edge on the feedback signal and will produce a down signal. This down signal from the PFD will turn the DOWN switch on, and the CP will sink current out of the loop filter; thus, decreasing Vcntrl. The current through the UP switch, Iup, and the current through the down switch, Idown , need to be equal in order to avoid any current mismatch. The minimum charge pump current is limited by the switching speed requirements. Figure 4.13 shows the CP implementation using Mentor Graphics 0.18μm technology. The UP and DOWN switches, M4 and M3, operate in the

triode region and they act like resistors (thermal noise occurs). They should have a large W/L ratio for faster switching time and wider voltage range. When the W/L ratio (transistor size) is large, the on resistance will be small. As the resistance is smaller, the voltage across the resistor will be small, which will allow for a wider voltage range at the output. The transistors M2 and M1 are current mirror sources and sinks.

Transistor No.	**Type**	**Width**	**Length**
M1,M2	**PMOS**	**5μm**	**0.18μm**
M3,M4,M5,M6	**NMOS**	**2.5μm**	**0.18μm**
M7,M8,M9,M10	**PMOS**	**10μm**	**0.18μm**
M11,M12	**NMOS**	**5μm**	**0.18μm**
M13,M14,M15,M16	**NMOS**	**2.5μm**	**0.18μm**

Table 4.3: Parameter of the Charge Pump

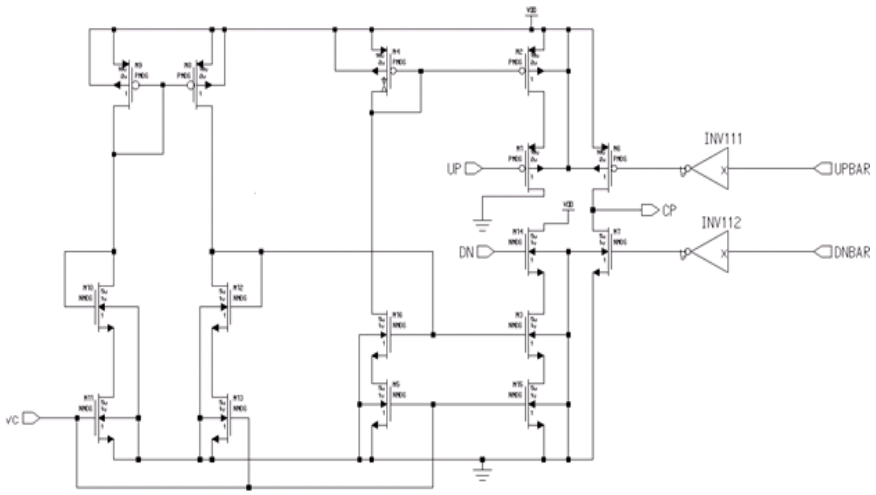

Figure 4.16: Schematic of Charge pump[2]

Figure 4.17: Simulation result of Charge Pump

Layout of Charge Pump :

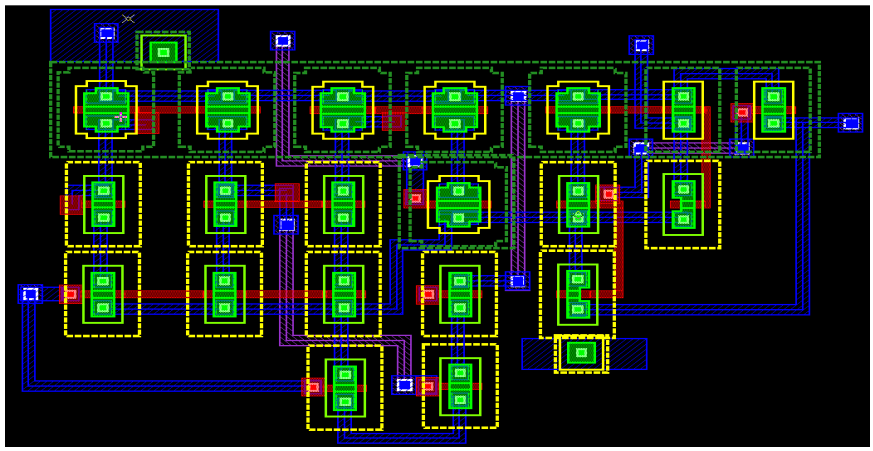

Figure 4.18: Layout of Charge Pump

Design Rules Check Report :

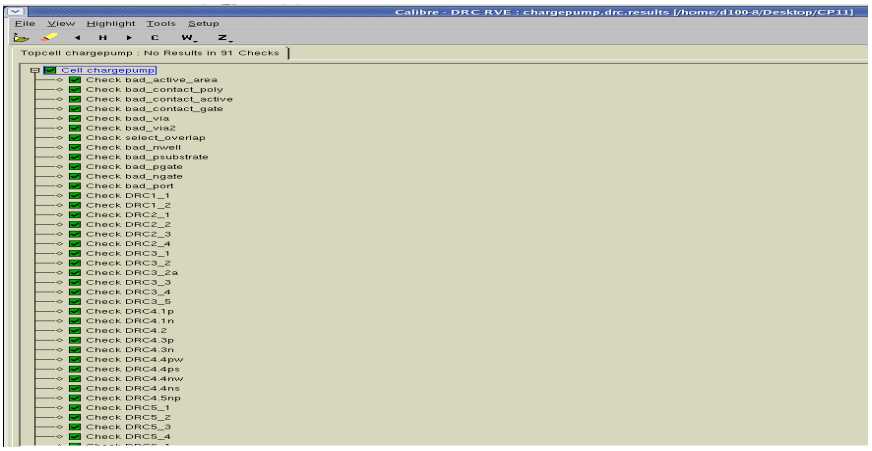

Figure 4.19: DRC Result of Charge Pump

Layout Vs Schematic :

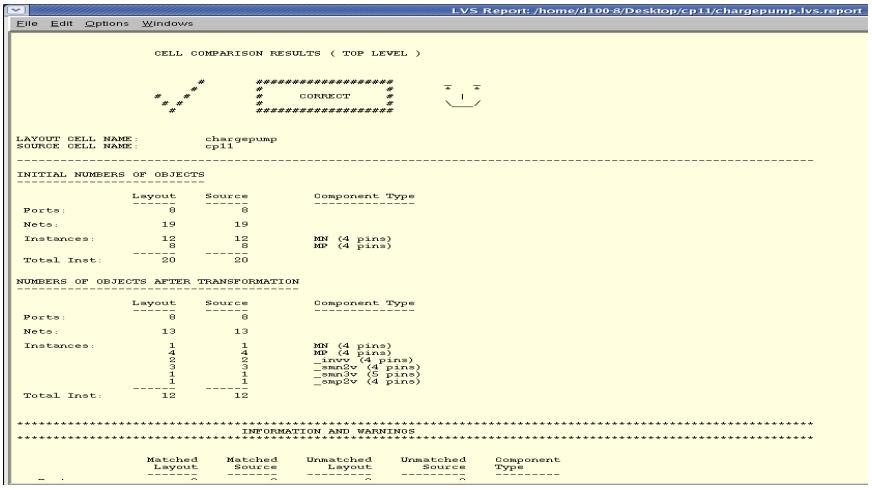

Figure 4.20: LVS Result of Charge Pump

PEX Report :

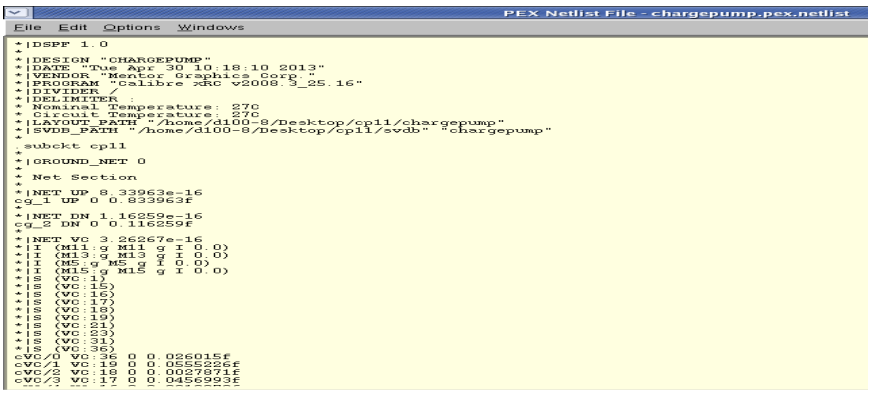

Figure 4.21: PEX Result of Charge Pump

4.3 Loop Filter

The loop filter[7][2] is the brain of the PLL. In this section, we discuss how to select the loop-filter values in order to keep the PLL from oscillating (i.e. keep the vinVCO voltage from oscillating, causing the frequency out of the VCO to wander). If the loop-filter values are not selected correctly, it may take the loop too long to lock, or once locked small variations in the input data may cause the loop to unlock. The third order loop is implemented using passive component. Passive loop-filter (LF), composed by a second order section (C1, C2 and R2) and a first order section (C3 and R3), providing an additional pole. The first order filter reduces spurs caused by the multiples of reference frequency, whose consequence is the increasing of the phase noise at the output. The stability is guaranteed by putting this last pole five times above the PLL band width and below the reference. A bandwidth of approximately two times the difference between the maximum and minimum frequencies generated by the VCO was used. The stability of the loop is guarantee with a phase margin at least of $\pi/4$ rad.

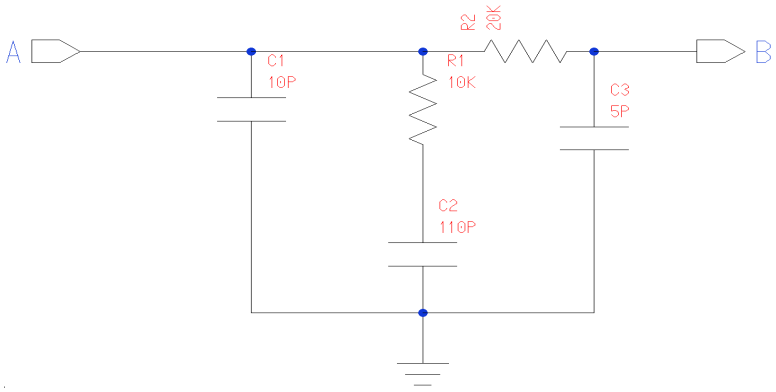

Figure 4.22: Passive Loop filter

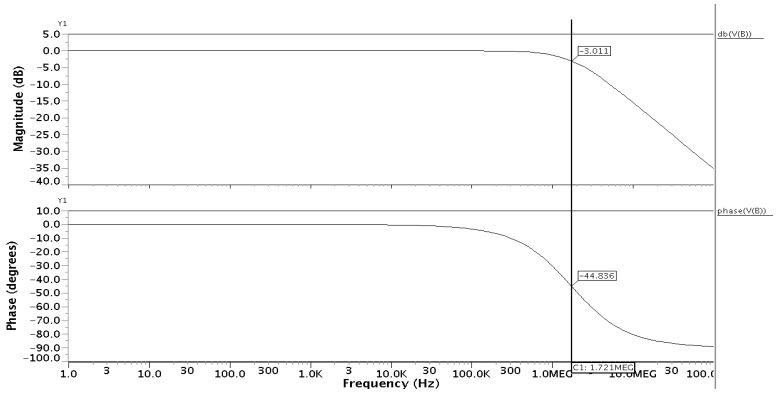

Figure 4.23: Phase Margin and Cutoff frequency of Loop filter

4.4 Voltage Control Oscillator

The purpose of the VCO [1]is to vary an output frequency proportional to the Vcntrl input.

VCO Architecture

The most popular type of the VCO circuit is the current starved voltage controlled oscillator. In this circuit the number of inverter stages is fixed with 5. The simplified view of a single stage current starved oscillator is shown in theFig.4.16 Transistors M2 and M3 operate as an inverter whileM1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 andM3;

in other words, the inverter is starved for current. The desired centre frequency of the designed circuit is 2.4GHz with a supply of 1.8V. The CSVCO is designed both in usual manner as mentioned in and also by using geometric programming. In the traditional manne the design of the inverter stages in CSVCO are carried out to give a delay of100ps. The length of all the transistors is fixed with 180nm.The design parameters of the VCO circuit are listed in the fig The general circuit diagram of the current starved voltage controlled oscillator is shown in the

Vco input votage

$$VinVCO = I_{PDI}.\frac{(1+j\omega RC1)}{j\omega(C1+C2)[1+j\omega R\frac{(C1C2)}{(C1+C2)}]} = KF.IPDI \tag{4.3}$$

The oscillation frequency of the current-starved VCO for N of stages is given by

$$N = \frac{ID_{Centre}}{Ctot.fosc.Vdd} \tag{4.4}$$

Where,ID=ID3=ID4

N = Number of Stage

Ctot = total capacitance

VDD = Supply Voltage.

The total capacitance is given by

$$Ctot = \frac{5}{2}Cox(W_P.L_p + W_n.L_n) \tag{4.5}$$

The gain of the vco is given by

$$KVCO = 2\pi.\frac{f_{max} - f_{min}}{V_{max} - V_{min}}(radians/S.V) \tag{4.6}$$

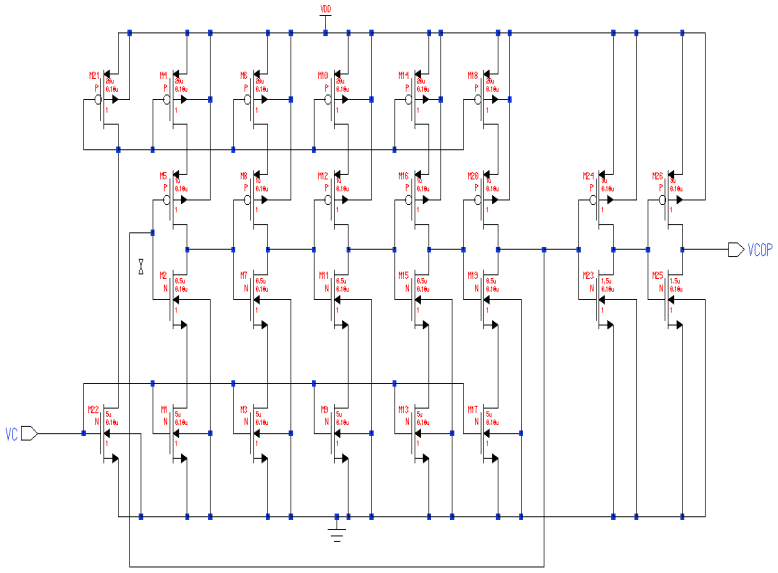

Figure 4.24: Schematic of Current starved VCO[4]

Parameter	Value
Width of Current starved PMOS(WPCS)	**20um**
Width of Current Starved NMOS(WnCS)	**5um**
Width of PMOS in Inverter(WP)	**1um**
Width of NMOS in Inverter(Wn)	**0.5um**
LPCS = LnCS = LP = Ln = L	**180nm**

Table 4.4: Parameter of Current Straved VCO

Voltage Control at Input Of VCO[V]	**Frequency at Output of VCO[GHz]**
0	**0**
0.2	**0**
0.4	**1.8**
0.6	**2**
0.8	**2.2**
1	**2.4**
1.2	**2.5**
1.4	**2.6**
1.6	**2.7**

Table 4.5: The Working Characteristics of VCO

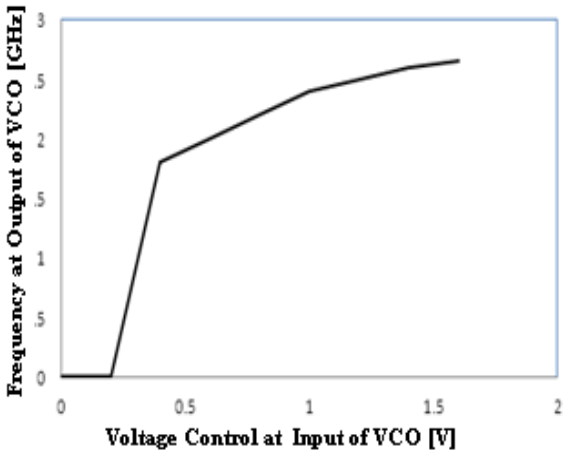

Figure 4.25: The Working Characteristics of VCO

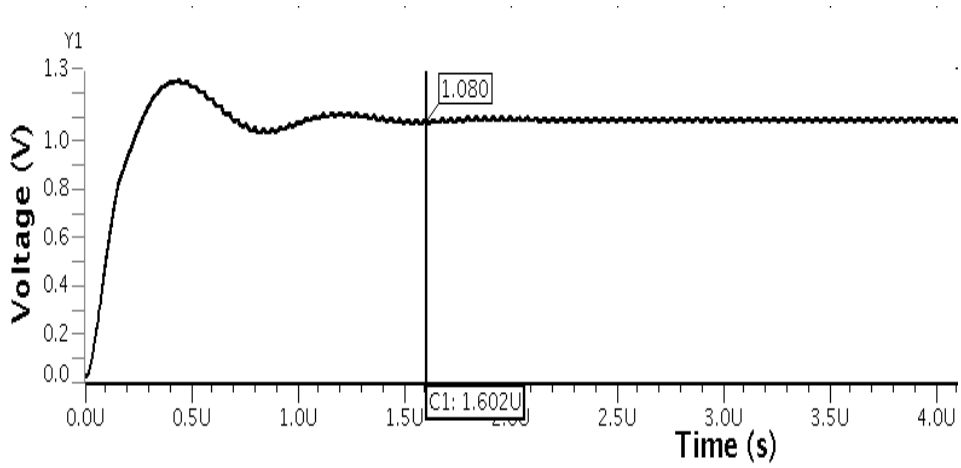

Figure 4.26: Control Voltage of VCO

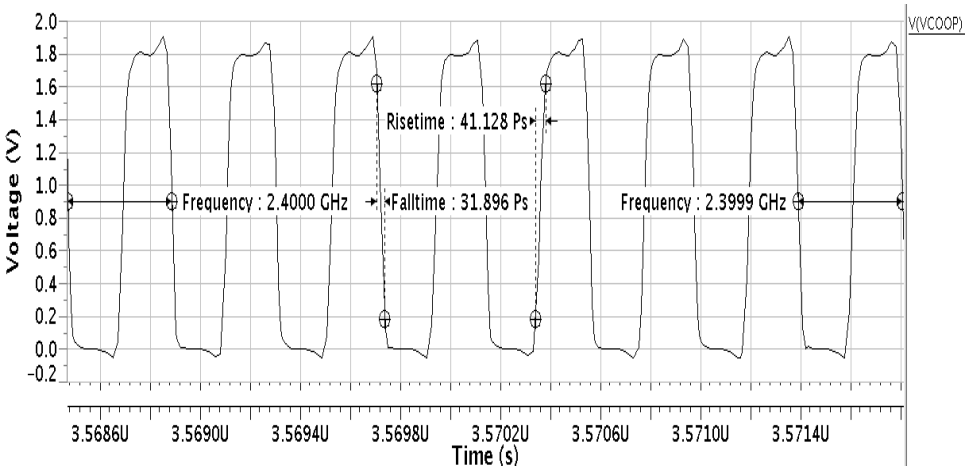

Figure 4.27: Simulation result of Current starved VCO

Layout of VCO :

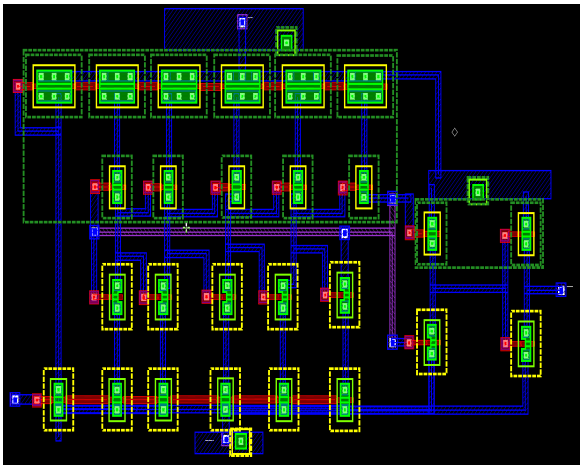

Figure 4.28: Layout of VCO

Design Rules Check Report :

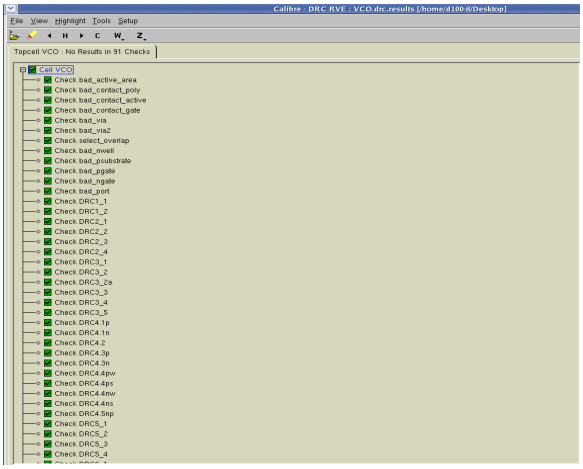

Figure 4.29: DRC Result of Voltage Controlled Oscillator

Layout Vs Schematic:

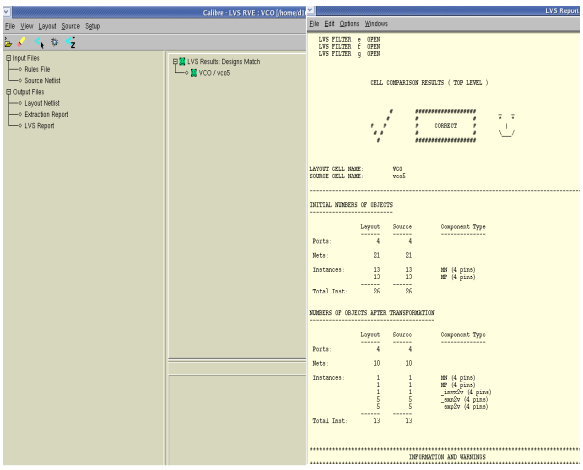

Figure 4.30: LVS Result of Voltage Controlled Oscillator

PEX Report :

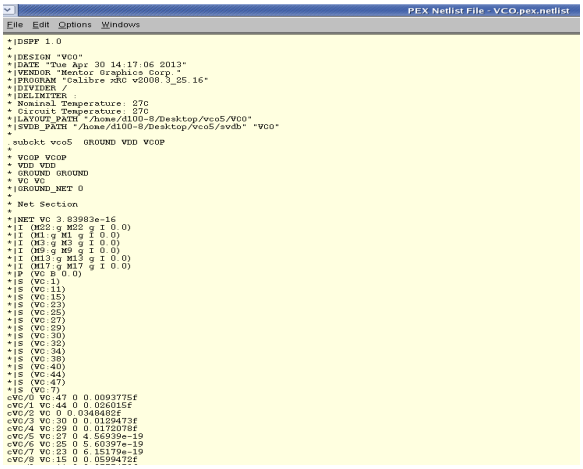

Figure 4.31: PEX Result of Voltage Controlled Oscillator

4.5 Frequency Divider

The frequency divider[8][11] may be integer or fractional ,and programmable divide counter is used for the frequency divider implemented by true single phase clock (TSPC) the divider perform good at high frequency with less jitter is produce.the Schematic of divide by two as shown in fig4.27 the divider by 4 implemented with help of the cascading of two stage of the divide by two as shown in fig.4.1 The division by 120 in the feedback path is done with a cascade constituted by one half divider implemented with a true single phase clock (TSPC) logic one divider by 30 followed by a toggle flip-flop to ensure a duty-cycle of 50and simulation result shown in fig4.28

The divide by 30 is implemented with help of 2/3 divider cell 2/3 divider dell implemented with positive edge trigger D flip-flop.2/3 divider cell is modulus control Divider. when M1=0 2/3 Divide Cell works as a Divided by 2 and when M1=1that time 2/3 cell works as a Divided by 3 and in case of the Divided by 30. The 2/3 divide cell connected as shown in fig.9 when M1=1 and M4 =0 It works as a divide by30 as sown in fig 4.34

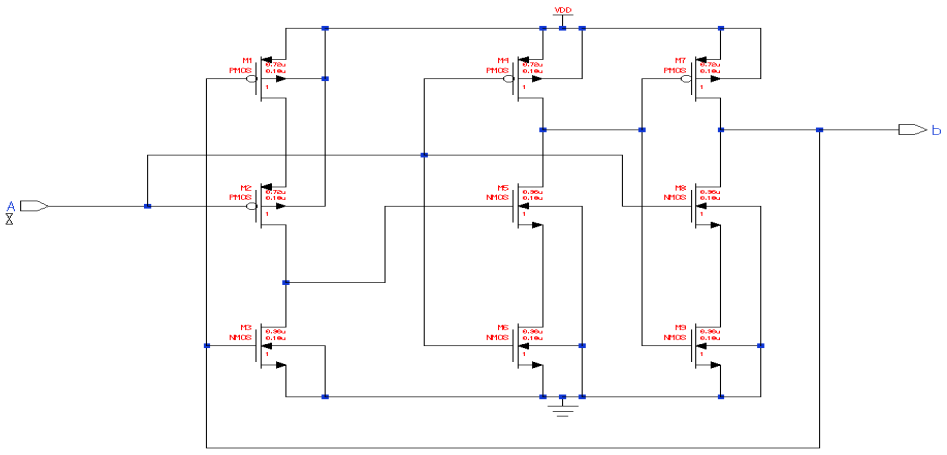

Figure 4.32: Schematic of Divide By 2[4]

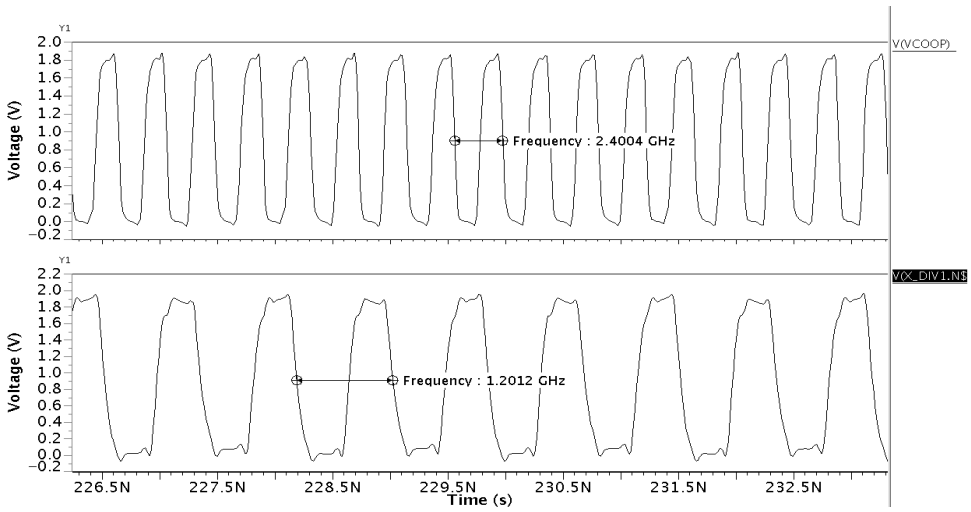

Figure 4.33: Simulation result of divide by 2

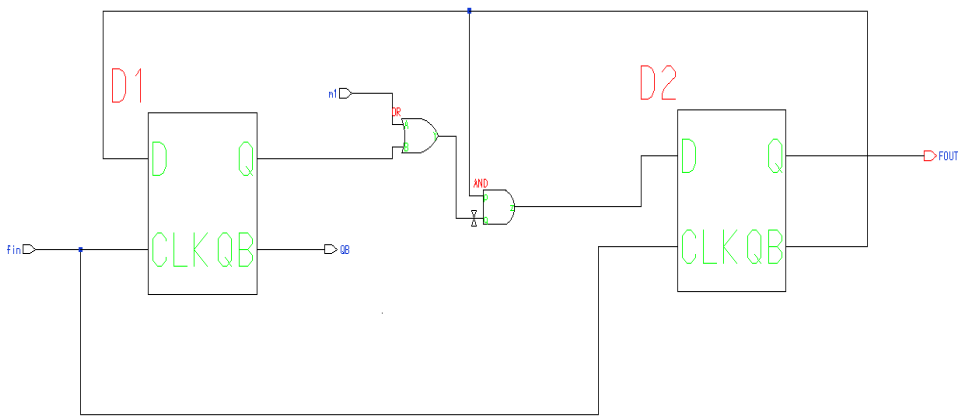

Figure 4.34: Schematic of 2/3 Cell[2]

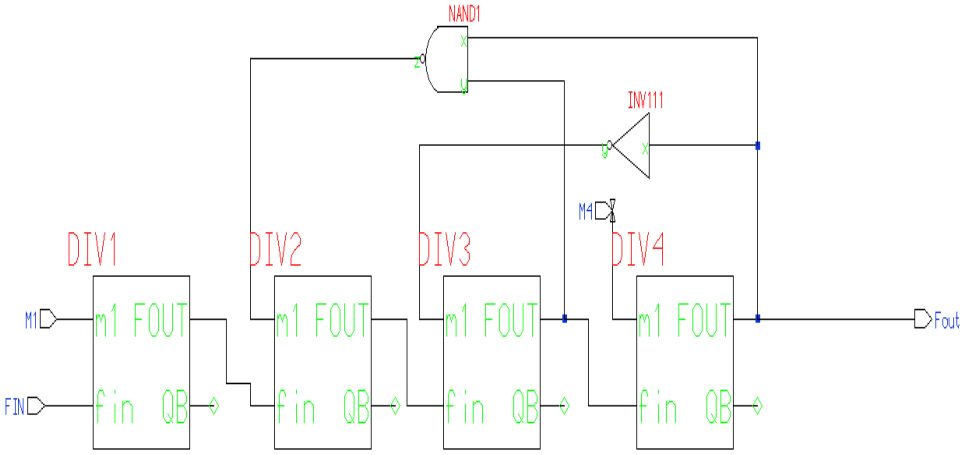

Figure 4.35: Schematic of divide by 30[2]

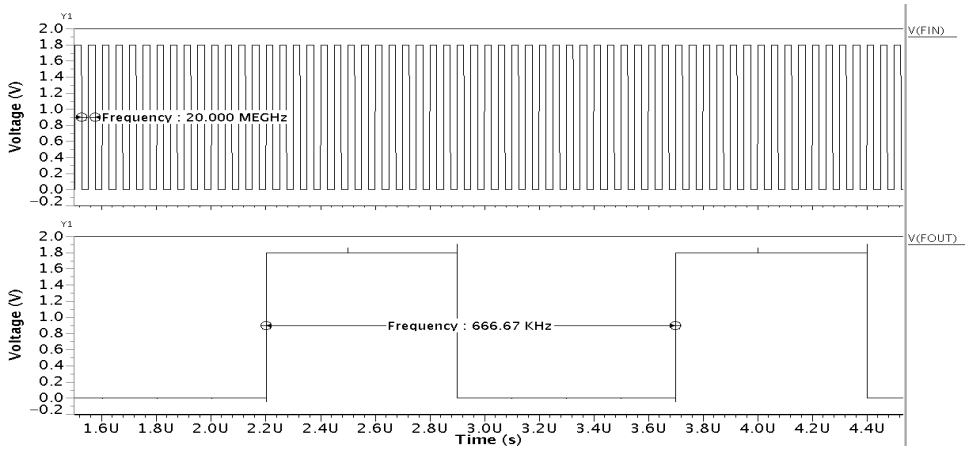

Figure 4.36: Simulation result of Divide by 30

Layout of Divide by 2:

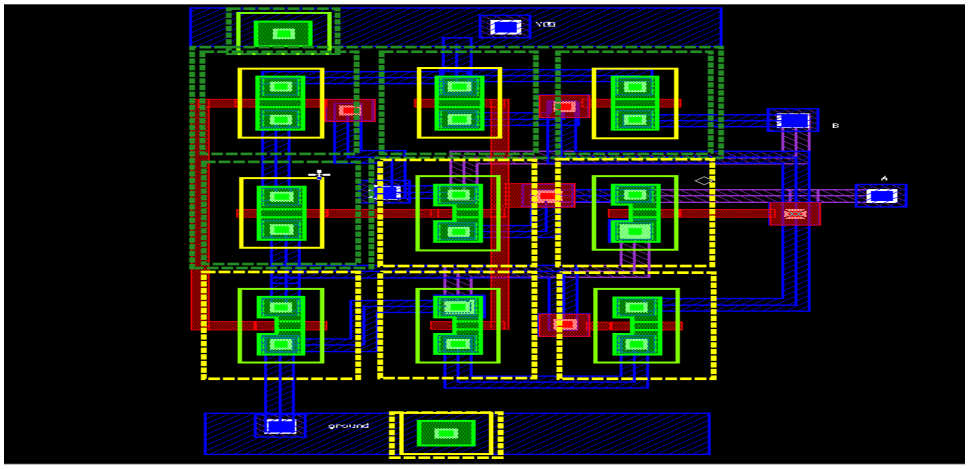

Figure 4.37: Layout of Divide by 2

Design Rules Check Report:

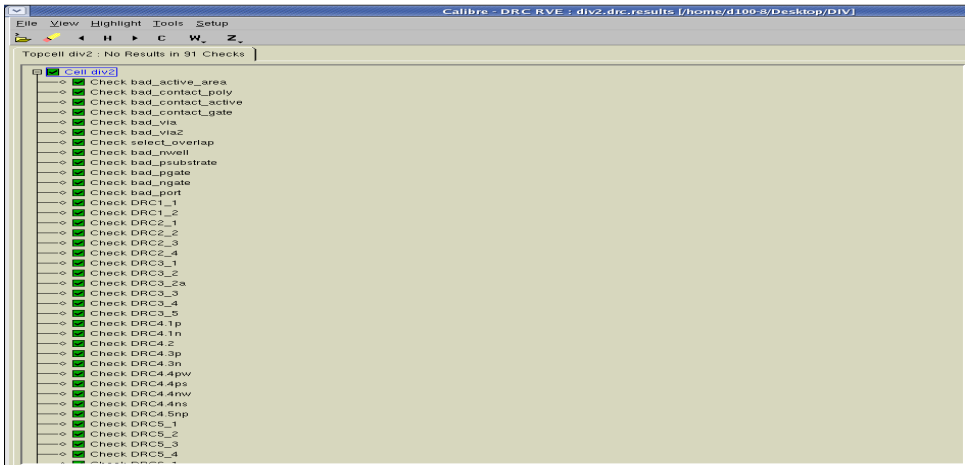

Figure 4.38: DRC Result of Divide by 2

Layout Vs Schematic:

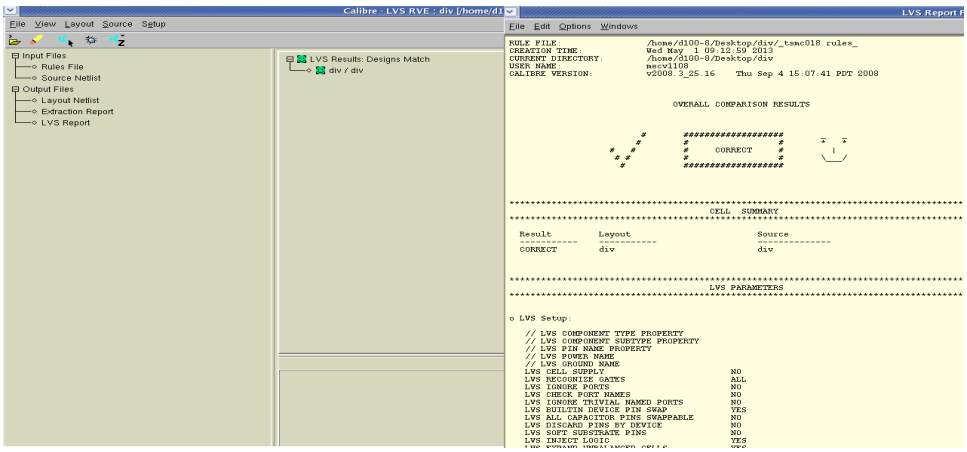

Figure 4.39: LVS Result of Divide by 2

PEX Report:

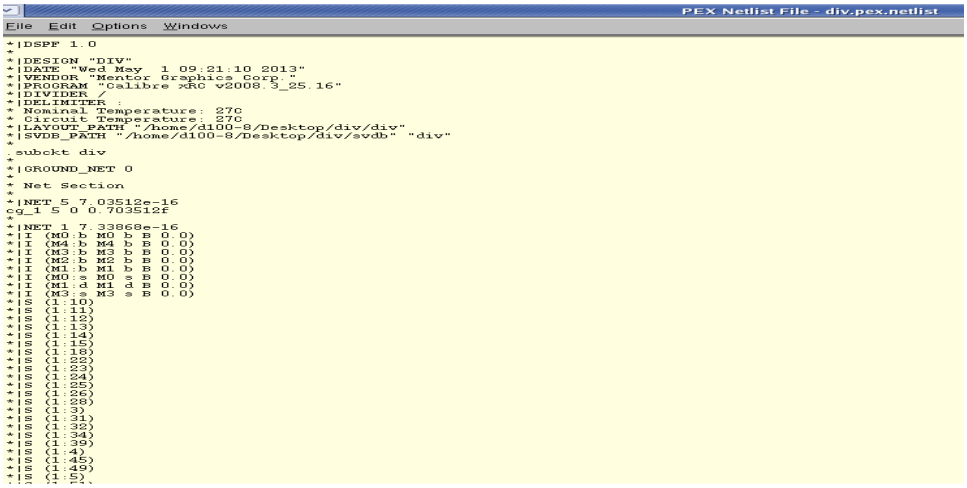

Figure 4.40: PEX Result of Divide by 2

Layout of Divide by 4:

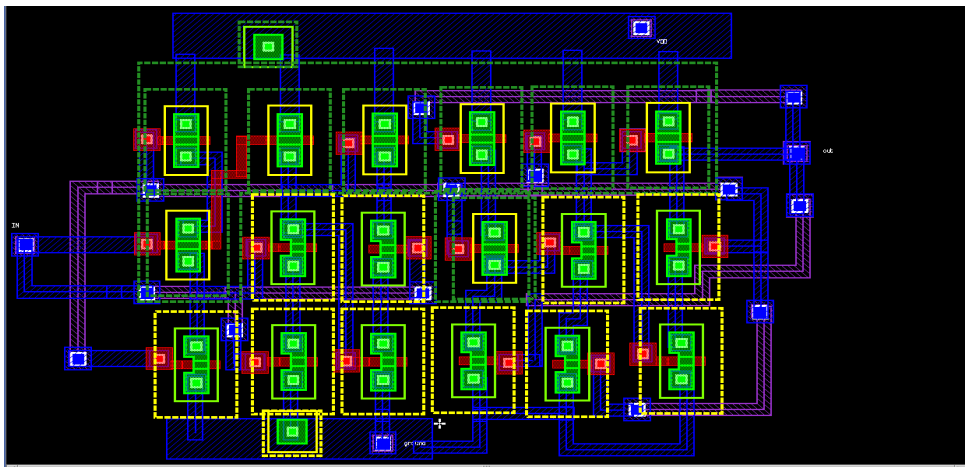

Figure 4.41: Layout of divide by4

Design Rules Check:

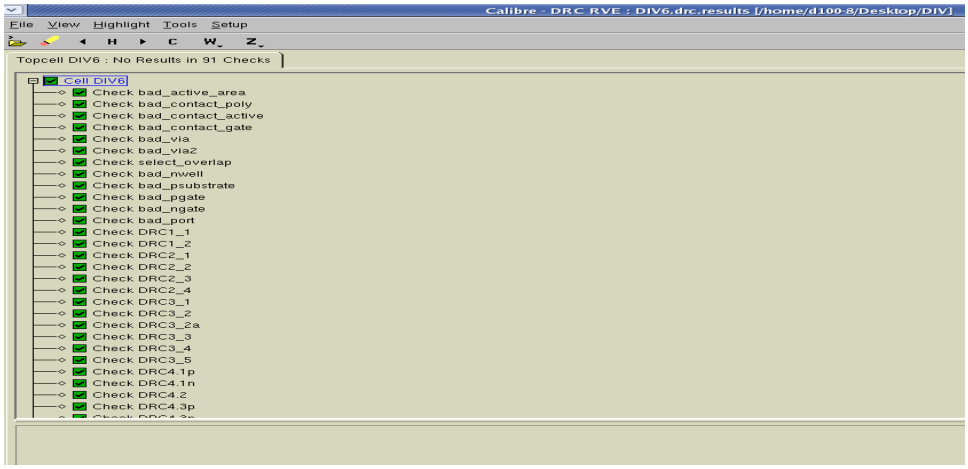

Figure 4.42: DRC Result of Divide by 4

Layout Vs Schematic:

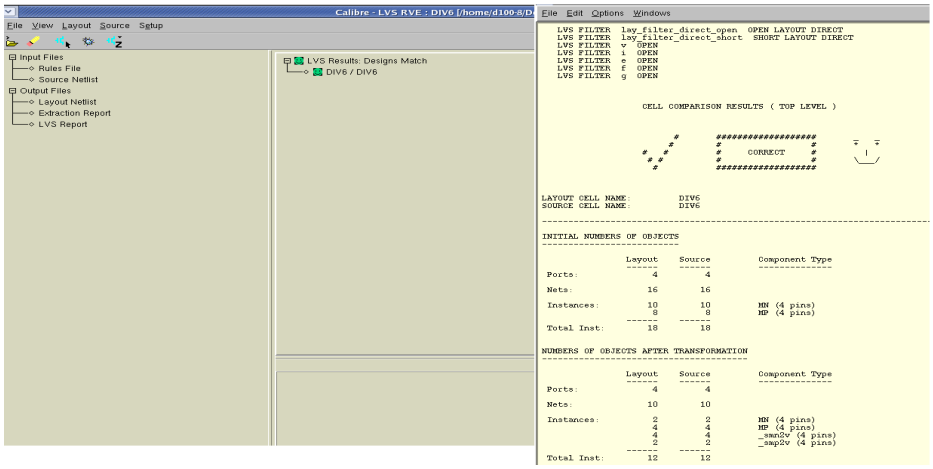

Figure 4.43: LVS Result of Divide by 4

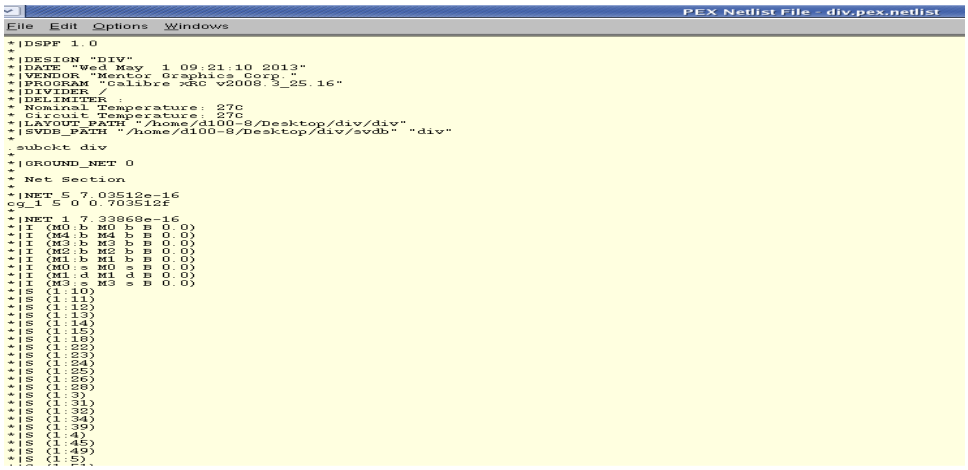

Figure 4.44: PEX Result of Divide by 4

Transistor No.	Type	Width	Length
M1,M2,M4,M7,M10,M11,M12,M13	PMOS	0.9μm	0.18μm
M3,M5,M6,M8,M9,M14,M15,M16,M17,M18	NMOS	0.36μm	0.18μm

Table 4.6: Parameter of the Divideby4

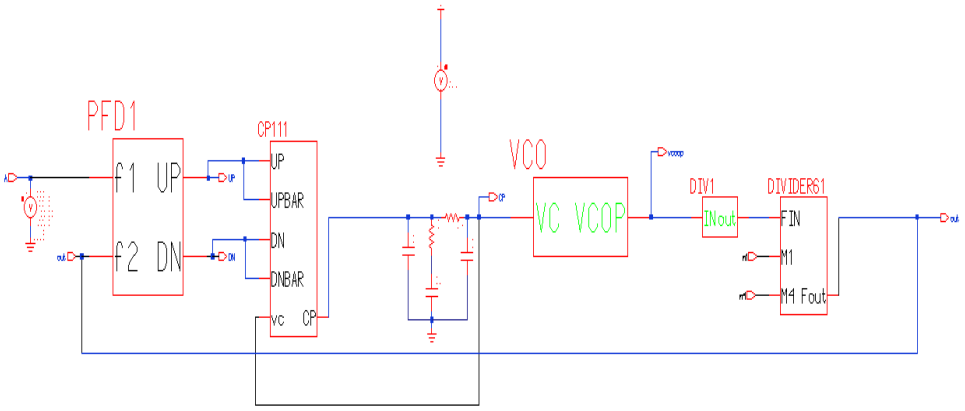

Figure 4.45: Block Diagram of 2.4 GHz Frequency Synthesiszer

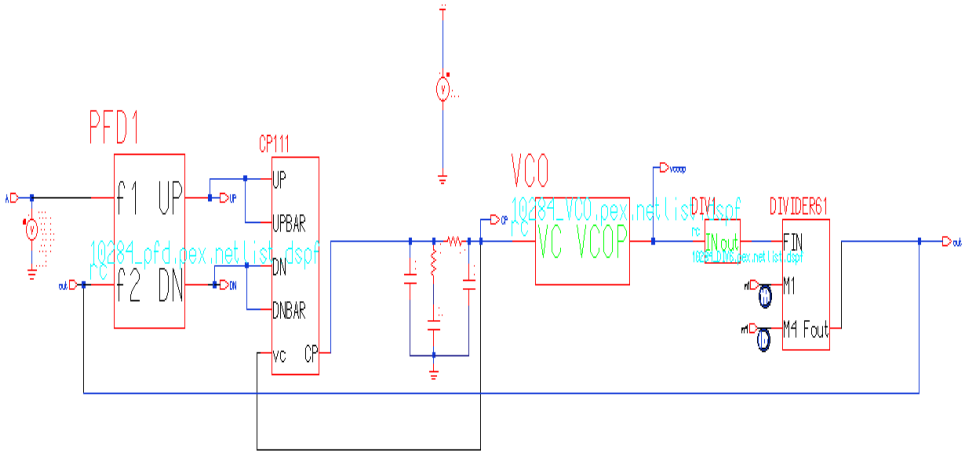

Figure 4.46: Block Diagram of 2.4 GHz Frequency Synthesiszer with parasitics

Post Simulation Result:

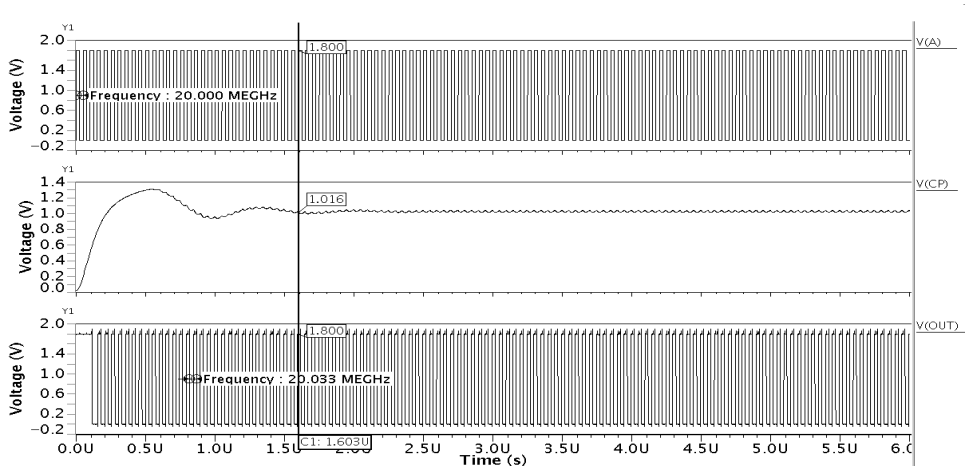

Figure 4.47: Post Simulation Result of dividerand Control Voltage.

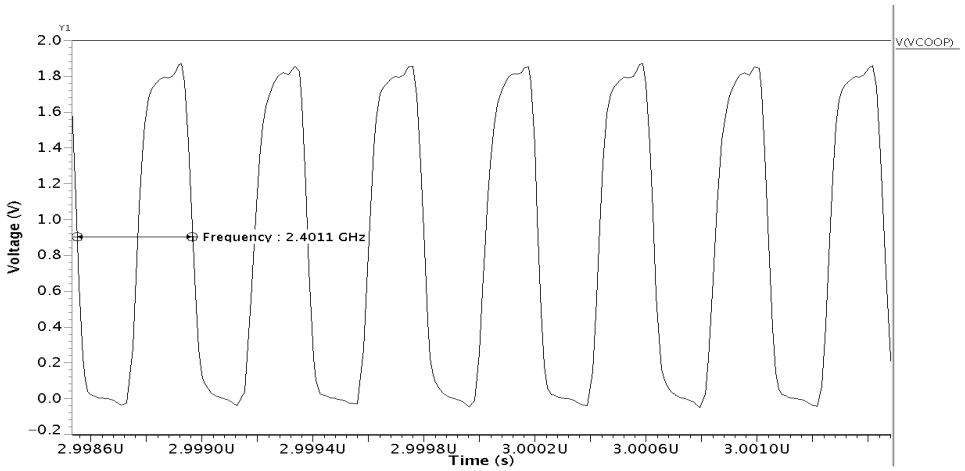

Figure 4.48: Post Simulation Result of VCO

Parameter	**PreLayout**	**Post Layout**
VCO frequency	**2.399GHz**	**2.4011GHz**
Rise time	**41.128Ps**	**57.982Ps**
fall time	**31.869Ps**	**50.47Ps**
frequecy of divider	**20MHz**	**20.33MHz**
Settling time	**1.643μ**	**1.603μ**
Power Dissipation	**4.20mWμ**	**4.02mWμ**

Table 4.7: Post Layout Result

Chapter 5

Conclusion and Future work

In the present work a PLL based frequency synthesizer for 2.4 GHz design has been done. A VCO is a major building block of the PLL and requires large design time. An inverter based ring oscillator is used for the realization of VCO as this occupies less area compared to other architectures. A polynomial has been developed that provides the tuning range of the VCO for the given control voltage. Also, the variation of frequency with control voltage for different supply voltages, different inverter dimensions has been done and the physical design of the VCO has been done. The Low-Pass Filter has been realized using passive filter. The phase detector has been realized using PFD/CP. A PFD/CP provides phase locking compared to the XOR based PD which provides only frequency locking. Therefore, PFD/CP can be used in frequency synthesis.and Divider by N counter is Perform at High frequency. Phase-detector must be chosen depending upon the application of PLL.

1. A 1.8 V 2.4 GHz frequency synthesizer use for wireless application and wireless sensor networkwireless standard protocol like Bluetooth with 1 MHz channel spacing also develop for the Zigbee application with 5MHz channel spacing in each channel

2. Reduce power

3. To minimize glitch in output and Phase Noise in VCO.

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APPENDIX 1- TSMC 0.18um TSMC Data Shee

```
 T44E SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jul  8/04
* LOT: T44E                  WAF: 6009
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3694291
+K1      = 0.5887715      K2      = 3.059696E-3    K3      = 1E-3
+K3B     = 4.5379416      W0      = 1E-7           NLX     = 1.859182E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 1.3484262      DVT1    = 0.3669657      DVT2    = 0.0321807
+U0      = 262.597552     UA      = -1.45346E-9    UB      = 2.388329E-18
+UC      = 6.065042E-11   VSAT    = 1.049851E5     A0      = 1.8958229
+AGS     = 0.4217527      B0      = 1.405467E-7    B1      = 5E-6
+KETA    = -5.710529E-3   A1      = 3.800448E-4    A2      = 0.8605984
+RDSW    = 114.1849719    PRWG    = 0.5            PRWB    = -0.2
+WR      = 1              WINT    = 0              LINT    = 1.38756E-8
+XL      = 0              XW      = -1E-8          DWG     = -1.403515E-8
+DWB     = 1.403585E-8    VOFF    = -0.0923188     NFACTOR = 2.3339618
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.976763E-3    ETAB    = 9.401588E-6
+DSUB    = 0.0147417      PCLM    = 0.7500199      PDIBLC1 = 0.1481831
+PDIBLC2 = 2.164741E-3    PDIBLCB = -0.1           DROUT   = 0.6836492
+PSCBE1  = 4.02605E10     PSCBE2  = 2.319101E-9    PVAG    = 9.51717E-3
+DELTA   = 0.01           RSH     = 6.6            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 8.88E-10       CGSO    = 8.88E-10       CGBO    = 1E-12
+CJ      = 9.738002E-4    PB      = 0.8            MJ      = 0.3806198
+CJSW    = 2.656147E-10   PBSW    = 0.8007021      MJSW    = 0.1397059
+CJSWG   = 3.3E-10        PBSWG   = 0.8007021      MJSWG   = 0.1397059
+CF      = 0              PVTH0   = -1.627734E-4   PRDSW   = -1.9138777
+PK2     = 9.037624E-5    WKETA   = 3.850841E-3    LKETA   = -5.396657E-3
+PU0     = 8.1162291      PUA     = 1.139148E-11   PUB     = 0
+PVSAT   = 1.247309E3     PETA0   = 1.003159E-4    PKETA   = 3.393907E-3     )
```

Figure 5.1: NMOS Model Parameter of 0.18um Technology

```
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27               TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17        VTH0    = -0.3944719
+K1      = 0.5828995    K2      = 0.0266823        K3      = 0
+K3B     = 14.3383713   W0      = 1E-6             NLX     = 1.373459E-7
+DVT0W   = 0            DVT1W   = 0                DVT2W   = 0
+DVT0    = 0.6336613    DVT1    = 0.2409053        DVT2    = 0.1
+U0      = 112.690631   UA      = 1.417849E-9      UB      = 1.12483E-21
+UC      = -1E-10       VSAT    = 1.850699E5       A0      = 1.7532818
+AGS     = 0.375203     B0      = 3.569636E-7      B1      = 1.12458E-6
+KETA    = 0.0205518    A1      = 0.4474986        A2      = 0.3631955
+RDSW    = 243.82298    PRWG    = 0.5              PRWB    = 0.5
+WR      = 1            WINT    = 0                LINT    = 2.551606E-8
+XL      = 0            XW      = -1E-8            DWG     = -4.374325E-8
+DWB     = 2.595671E-10 VOFF    = -0.0937437       NFACTOR = 2
+CIT     = 0            CDSC    = 2.4E-4           CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.1136843        ETAB    = -0.0748821
+DSUB    = 1.0613195    PCLM    = 2.4303317        PDIBLC1 = 7.845168E-4
+PDIBLC2 = 0.0239307    PDIBLCB = -1E-3            DROUT   = 0
+PSCBE1  = 3.207414E9   PSCBE2  = 9.282296E-10     PVAG    = 15
+DELTA   = 0.01         RSH     = 7.5              MOBMOD  = 1
+PRT     = 0            UTE     = -1.5             KT1     = -0.11
+KT1L    = 0            KT2     = 0.022            UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11         AT      = 3.3E4
+WL      = 0            WLN     = 1                WW      = 0
+WWN     = 1            WWL     = 0                LL      = 0
+LLN     = 1            LW      = 0                LWN     = 1
+LWL     = 0            CAPMOD  = 2                XPART   = 0.5
+CGDO    = 6.34E-10     CGSO    = 6.34E-10         CGBO    = 1E-12
+CJ      = 1.148543E-3  PB      = 0.8476511        MJ      = 0.4067434
+CJSW    = 2.382898E-10 PBSW    = 0.8222976        MJSW    = 0.3300124
+CJSWG   = 4.22E-10     PBSWG   = 0.8222976        MJSWG   = 0.3300124
+CF      = 0            PVTH0   = 3.507137E-3      PRDSW   = 17.811338
+PK2     = 3.610481E-3  WKETA   = 0.0334716        LKETA   = -3.202602E-3
+PU0     = -2.0541594   PUA     = -8.93082E-11     PUB     = 1E-21
+PVSAT   = -50          PETA0   = 1.003159E-4      PKETA   = -1.696047E-3
*
```

Figure 5.2: PMOS Model Parameter of 0.18um Technology