

Design and Simulation of Current Mirror Circuits

Major Project Report

Submitted in partial fulfillment of the requirements

For the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Saiyed FaizAhmed.J

(11MECV15)



Department of Electrical Engineering
Electronics & Communication Programme

Institute of Technology,

Nirma University, Ahmedabad-382 481

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Under the Guidance of

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MAY 2013

Declaration

This is to certify that

(i) The thesis comprises my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

(ii) Due acknowledgement has been made in the text to all other material used.

Saiyed FaizAhmed.J

Certificate

This is to certify that the Major Project entitled "**DESIGN AND SIMULATION OF CURRENT MIRROR CIRCUITS**" submitted by **Saiyed Faiz Ahmed. J (11MECV15)**, towards the partial fulfillment of the requirements for the degree of **Master of Technology (VLSI Design)** in the field of **Electronics and Communication** of Nirma University is the record of work carried out by him under our supervision and guidance. The work submitted has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, have not been submitted to any other University or Institution for award of any degree or diploma.

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Place:Ahmedabad

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such work.

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Abstract

A current Mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of circuit, keeping the output current constant regardless of loading. The current being copied can be, and sometime is a varying signal current. Conceptually an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current controlled current source (CCCS). The current mirror is used to provide bias current and active loads to circuits.

For modern CMOS technologies with shorter channel lengths, smaller voltage gain and lower supply voltage impose many constraints on the performance and circuit structures of the current mirrors. Current mirror is the core structure for almost all analog and mixed mode circuits determine the performance of analog structures, which largely depends on their characteristics. For high performance analog circuit application, the performance of the current mirror. An efficient implementation of a CMOS current mirror suitable for low voltage application and achieve low input resistance, high accuracy and high output resistance. In this report advance current mirror, like wide swing is characterized, simulated and analyzed with different aspects and these topologies are also compared with basic current mirror, like simple and cascode current mirror. To support the circuit design, simulation and layout design, TSMC 0.18 μ m CMOS technology is used here. Whole work is carried out by Eldo Spice Design Architect and IC Station (Mentor Graphics).

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Chapter 1

Introduction

1.1 Motivation

Current Mirrors are one of the most important building blocks in analog and mixed signal IC design. They can be used as current sources, biasing circuits and active loads. The biggest challenge is the current offset in the output node, while maintaining a low voltage low power consumption and high current range. Biasing conditions are one of the factors that determine the accuracy of the current replica. As the input range increases the accuracy of a current copy in a current mirror decreases.

1.2 purpose

Current Mirror made using active devices have been widely used in analog integrated circuits both as biasing circuit and as load device for amplifier stages. Current mirror are frequently more economical than resistors in terms of die area required to provide bias current of certain value, particularly when the required value of bias current is small. Ideally, the output impedance of a current mirror should be infi-

nite and capable of generating or drawing a constant current over a wide range of voltage. However, finite values of r_0 and a limited output swing required to keep device in saturation will ultimately limit the performance of the mirror.

1.3 Scope

Current Mirror Circuits are the widely used in analog circuits design. The Taiwan semiconductor manufacturing company (TSMC) 0.18 μ CMOS technology is used. The design goals are low power, small area, and low power consumption. Current Mirror Circuits are giving constant output currents. Circuits were Designed with Design Architect and IC Station, simulated using Eldo tool(Mentor Graphics).

1.4 Outline of Thesis

This thesis presents the design and implementation of different types of Current Mirror Circuits for Analog applications. The contents of this document have been organized in a logical sequence. A brief description of the contents of each chapter is given below.

Chapter 2 Explain the literature survey of the current source/sink (or mirrors) like, its characteristics, graphical properties, classification, literature review of basic current mirrors, application of it and the VLSI Back End Design flow.

Chapter 3 Cover the Simple and Cascode Current Mirrors with pre and post layout simulation results. This chapter also contains the literature survey about Wilson and Regulated cascode current mirror.

Chapter 4 Explain the advanced current mirrors, in which Wide Swing Current Mirror Circuit are described here. Layout design pre and post layout simulation is carried out here for these topologies.

Chapter 5 presents detail analysis and comparisons of the different current mirror topologies, which are proposed here.

Chapter 6 presents conclusions and the future work that can be introduced to improve the performance of this system proposed architecture of mirror

Chapter 2

Literature Survey

,

2.1 Introduction

Current mirrors are employed in many applications such as operational amplifiers, analog to digital and digital to analog converters. Current mirrors mimic the performance of an ideal current source. Therefore their design must fulfill the following requirements: (1) Input impedance should be zero, (2) Output impedance should be infinite, (3) Output current should be constant over wide swing of voltage, (4) Output current should be constant against supply or temperature variation and, (5) Accurate input current copy[4]

On an IC chip with a number of amplifier stages, a constant DC current is generated at one location and replicated at various points. In this application, the biasing of the current mirror doesn't need a dynamic biasing scheme. Having a DC voltage to bias the circuit provide the desired range and accuracy. In the case of current sensors the input of a current mirror is an AC value. For this a DC biasing will affect the accuracy of the current copy.

As the name itself suggests a current mirror is used to generate a replica (if necessary, it may be attenuated or amplified) of a given reference current. If we

look at the electric function of the circuit, a current mirror is a current controlled current source (CCCS). Figure 2.1, shows its ideal representation. It consists of a branch that measures the reference current and the CCCS. In real circuits, as we will see shortly, current mirrors are not able to accomplish the function of a CCCS exactly. The current gain factor can only be positive while the output impedance, the dynamic range and the speed are finite. Moreover, the current to be copied is not measured ideally as it would be necessary to show a short circuit. Instead, to measure the reference current, a diode connected MOS transistor is normally used.[9]



Figure 2.1: Current Replica

2.2 Current Source/Sink or Mirrors

Characterization of Current source /sink,

- (1) Minimum voltage (V_{min}) across sink or source for which the current is no longer Constant.
- (2) Output resistance which is a measure of the flatness of the current sink or source.[1]

$$r_{out} = \frac{1}{\lambda I_d} \quad (2.1)$$

$$V_{min} = V_{ds} = V_{on}, \text{ where } V_{on} = V_{gs} - V_t \quad (2.2)$$

Here, figure 2.2 and 2.3, shows the current sink and current source circuit example and it's graphical characteristic.

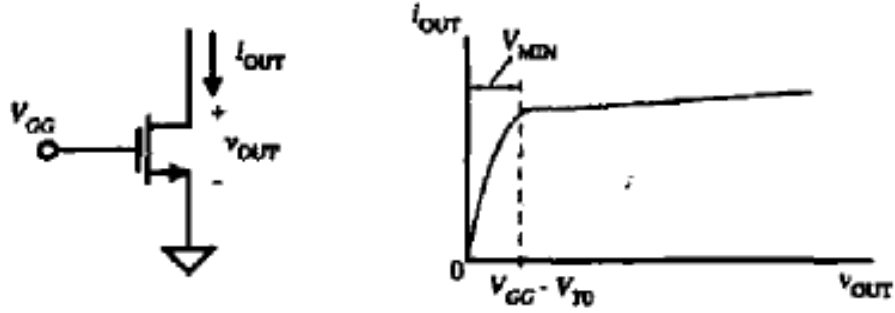


Figure 2.2: Current Sink and Its Graphical Characteristics

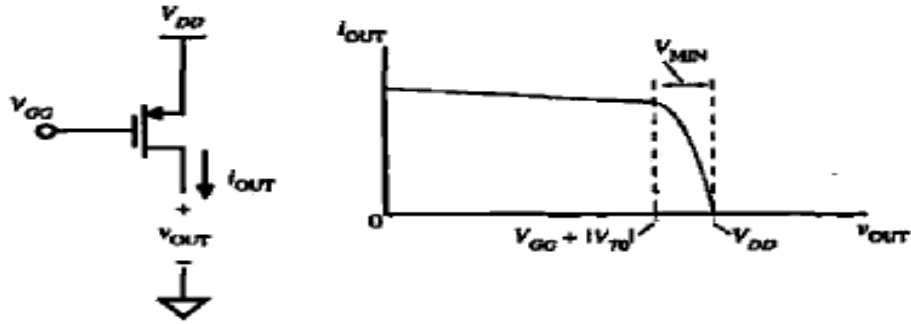


Figure 2.3: Current Source and Its Graphical Characteristics

2.2.1 characteristics

In general, characteristics of Current Mirror are:

- Input impedance should be zero.

- Output impedance should be infinite.
- Output Current should be constant over wide swing of voltage.
- Output Current should be constant against supply voltage and Temperature[4]

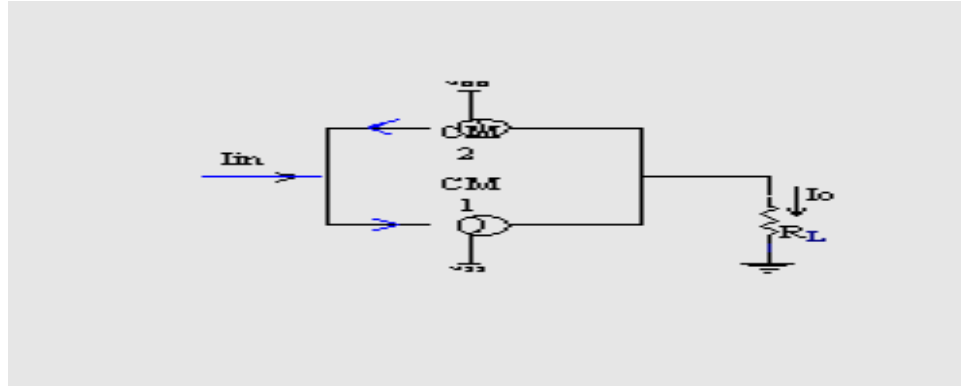


Figure 2.4: Current Amplifier

2.2.2 Graphical Properties

Here figure 2.5, shows the i/p and o/p impedance characteristics of the current mirror while figure 2.6 shows the current linearity.[1]

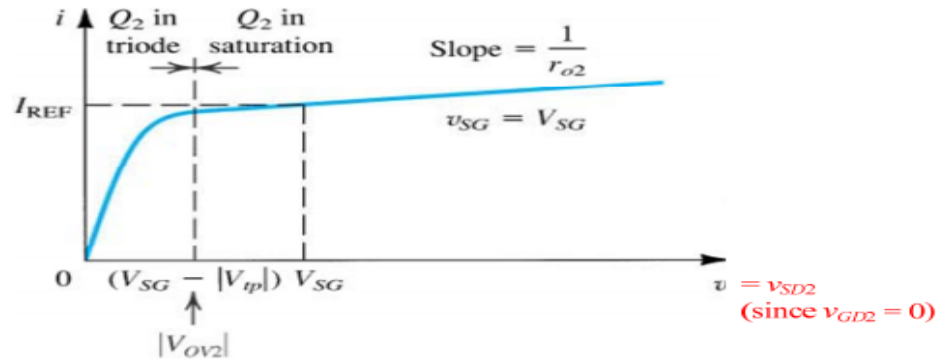


Figure 2.5: O/P Impedance Characteristics.

2.3 Classification

Classification of current mirror is based on feedback topology. There are two types of current mirrors.

- (a) Close loop current mirror (With Feedback).
- (b) Open loop current mirror (Without Feedback).

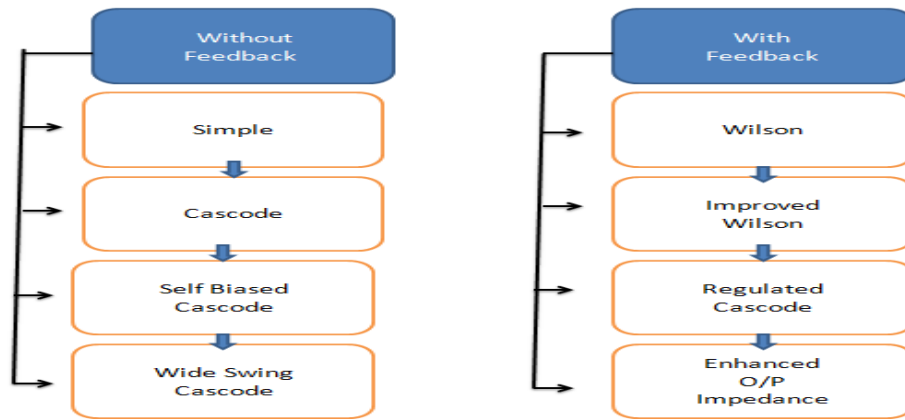


Figure 2.6: Classification of Current Mirror

2.4 Application

Current Mirror is the basic building block in analog circuits. Current Mirror is used in analog as

- Biasing Circuit.
- Active Load.
- Current Mode Circuits.
- Current Generator.

2.5 VLSI Back End Design Flow

- Specification.
- Circuit Design-To calculate W/L ratio for given specification.
- Pre layout Simulation Schematic level or spice level simulation.

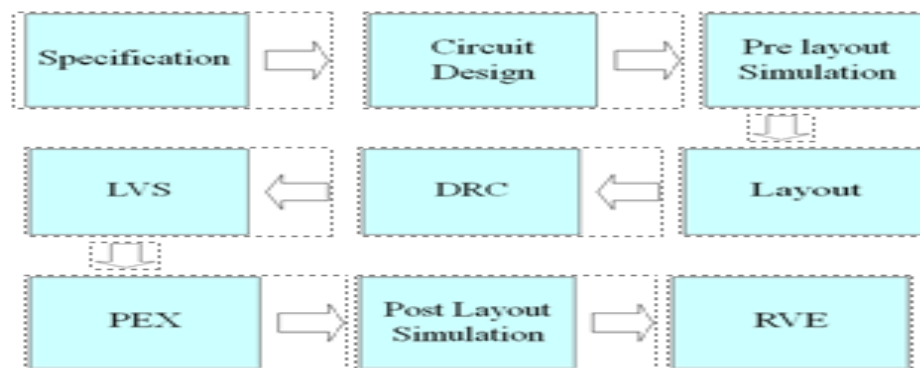


Figure 2.7: VLSI Back End Design Flow.

- Layout Design.
- DRC.
- LVS.
- PEX.
- Post Layout Simulation.
- RVE.

Chapter 3

Basic Current Mirror

3.1 Simple Current Mirror

3.1.1 Circuit Description

The basic NMOS current mirror is shown in figure 3.1, the diode connection in transistor M1 guarantees operation in saturation mode. The voltage between gate and source (V_{gs}) in both transistor should be the same, thus I_{out} is a replica of I_{in} . [4]

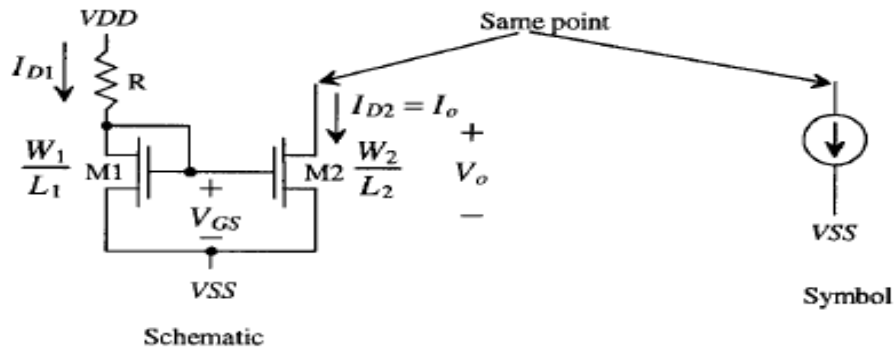


Figure 3.1: Simple Current Mirror

Now current at transistor M1:

$$I_{d1} = \left(\frac{\beta}{2}\right)(V_{gs} - V_{th})^2(1 + \lambda V_{ds1}) \quad (3.1)$$

Current at transistor M2:

$$I_{d2} = \left(\frac{\beta}{2}\right)(V_{gs1} - V_{th})^2(1 + \lambda V_{ds1}) \quad (3.2)$$

In general,

$$\frac{i_0}{i_1} = \left(\frac{W_2 L_1}{W_1 L_2}\right) \left(\frac{V_{gs} - V_{t2}}{V_{gs} - V_{t1}}\right)^2 \left(\frac{1 + \lambda V_{ds2}}{1 + \lambda V_{ds1}}\right) \left(\frac{\mu_{02} C_{ox2}}{\mu_{01} C_{ox1}}\right) \quad (3.3)$$

If the device are matched

$$\frac{i_0}{i_1} = \left(\frac{W_2 L_1}{W_1 L_2}\right) \left(\frac{1 + \lambda V_{ds2}}{1 + \lambda V_{ds1}}\right) \quad (3.4)$$

If, $V_{ds1} = V_{ds2}$, then

$$\frac{i_0}{i_1} = \left(\frac{W_2 L_1}{W_1 L_2}\right) \quad (3.5)$$

$$I_{out} = \left(\frac{W_2 L_1}{W_1 L_2}\right) * I_{in} \quad (3.6)$$

Therefore the sources of error are:

[1] $V_{ds1} \neq V_{ds2}$

[2] M1 and M2 not matched ($\Delta\beta$ & ΔV_{th})

3.1.2 Small Signal Analysis

The small signal output impedance of this current mirror (CM) is relatively low, (see eq 3.7), typically hundreds of $K\Omega$. This factor contributes greatly to the current offset in the output node of this current mirror.[4]

$$r_0 = r_{02} = \left(\frac{1}{\lambda} * I_{d2}\right) \quad (3.7)$$

The simple current mirror is a self bias architecture. The diode connection in the input transistor allow changes in the biasing node to be proportional to change in the input current. One of the advantage of this architecture is that it is low input requirement $V_{dd(min)}=V_{gs}$. However, the disadvantages mention before do not make it suitable for many application.[1]

3.1.3 Simple Mirror Circuit

Figure 3.2 shows the simple mirror circuit and its output characteristics. In which mirror circuit is used as load element.

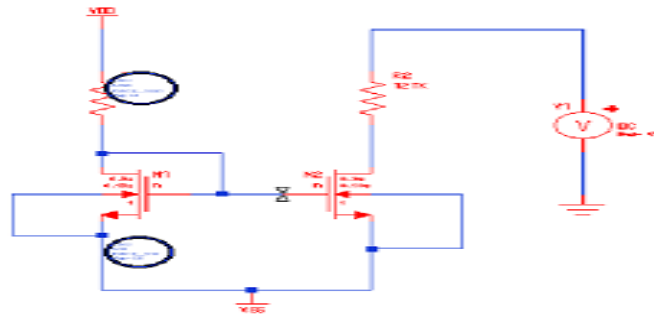


Figure 3.2: Simple Current Mirror Circuit

3.1.4 Pre Layout Simulation

[1] Specification

Power Supply	Vdd=1.8v & Vss= -1.8
Technology	TSMC 0.18 μ m
Model File	LEVEL 53
Spice Simulator	Eldo Spice, Design Architect and IC Station(Mentor Graphics)

Table 3.1: Technology parameters

[2] Mirror Characteristics Simulation

Here simple current mirror is used to achieve $10\mu\text{A}$ reference (or input) current at the transistor M1 and M2 using $127\text{K}\Omega$. Figure 3.3 shows the current drawn through transistor M1 and M2.

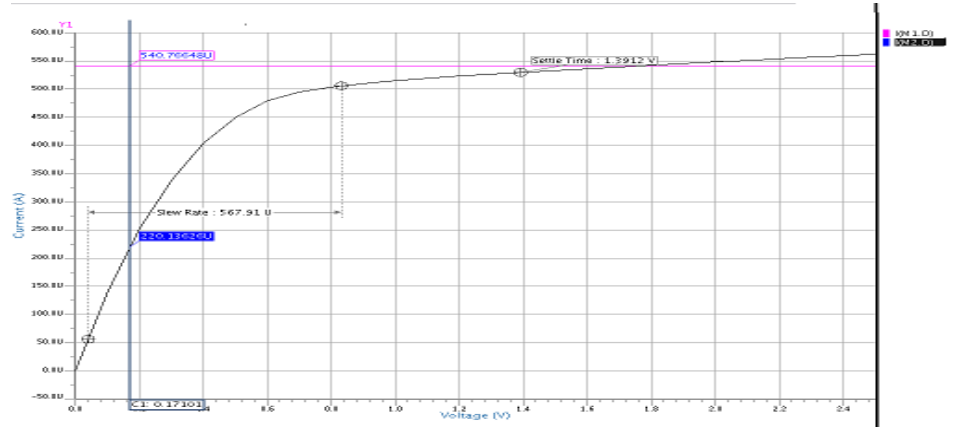


Figure 3.3: I_{out} Vs I_{in}

3.1.5 Layout Making Processes

[1] Design Consideration

Table 3.2 Shows the transistor aspect ratios for simple current mirror and for the test circuit respectively.

Transistor	$W(\mu\text{m})$	$L(\mu\text{m})$
M1	0.9	0.18
M2	0.9	0.18

Table 3.2: Transistors aspect ratios for Simple Circuit

[2] Layout

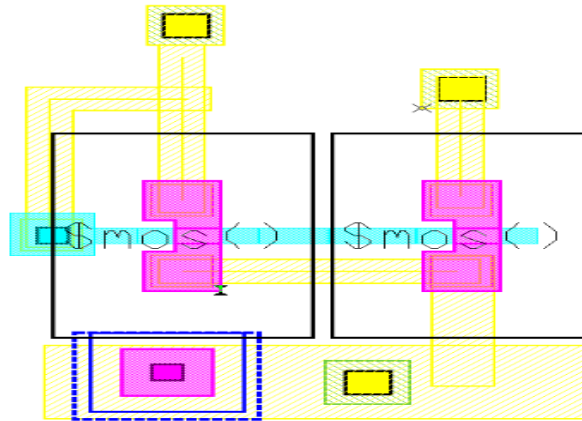


Figure 3.4: layout for Simple Current Mirror Circuit

[3] Design Rule Check (DRC)

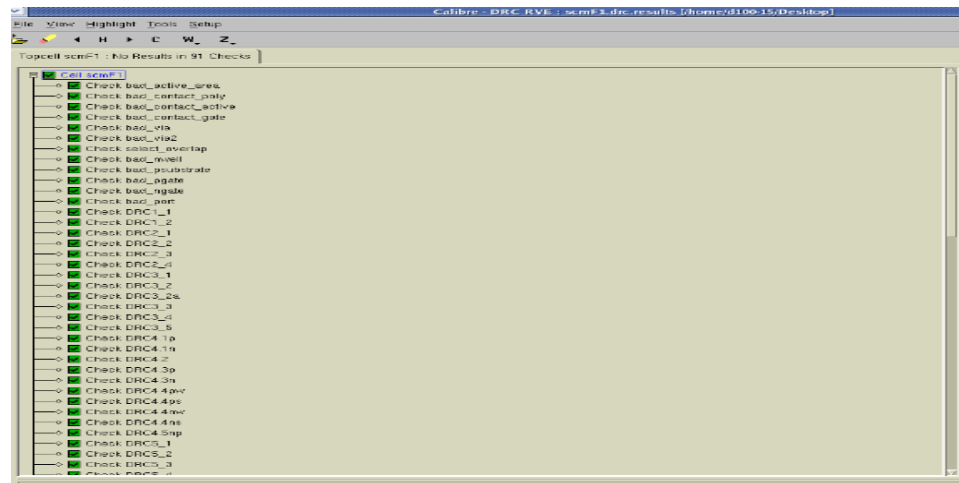
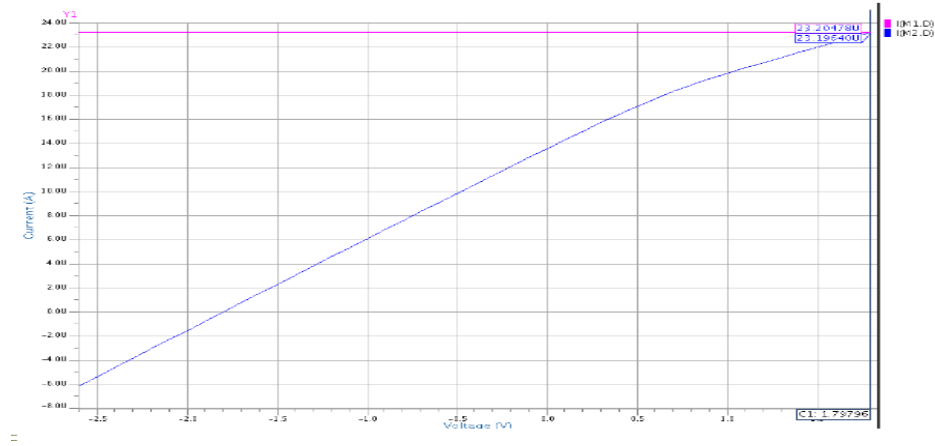


Figure 3.5: DRC for Simple Current Mirror Circuit

[2] Mirror Characteristics Simulation

Same Specification of pre layout simulation is used here for Post layout Simulation Processes. The post layout simulation graph shown below.

Figure 3.8: I_{out} Vs. I_{in}

3.2 Cascode Current Mirror

3.2.1 Circuit Description

An alternative way to increase the output resistance is to use a cascode configuration. Figure 3.15, shows a possible scheme. The output stage consists of two transistors (M2-M4) in the cascode arrangement [6]. Their biases result from two other transistor (M1-M3) which are diode-connected. Again, as for the previously studied current mirrors, the V_{gs} voltage of M1 and M2 are set equal. Therefore, a replica of the current in M1 is generated by M2. The output resistance increases because of the cascode arrangement.[2]

Calculating the minimum voltage across the current source begins by defining the gate-source biasing voltage in terms of the excess gate-source voltage ΔV as

$$V_{gs} = \Delta V + V_{th,n} \quad (3.8)$$

Since $V_{gs}=1.2V$ the n-channel excess gate voltage, neglecting the body effect, is $\Delta V = 0.37 V$ (see Figure 3.15) and the p-channel excess gate voltage is $0.290V$. The gate voltage of M4 is $2(\Delta V + V_{th,n})=2.4V$, While the source voltage of M4 is $\Delta V + V_{th,n}$

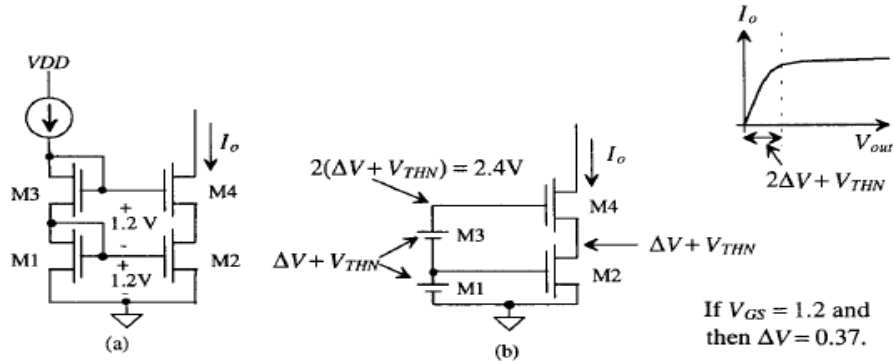


Figure 3.9: Cascode Current mirror

The minimum voltage on the drain of M4 and thus the minimum voltage across the current source are limited by the requirement that M4 remain in the saturation region.

$$V_{ds4} \geq V_{gs4} - V_{th,n} \text{ or } V_{ds} \geq \Delta V \quad (3.9)$$

The minimum voltage across the cascode current mirror is significantly larger than the minimum voltage across the basic current mirror. ($\Delta V=0.37V$)

[A] Small Signal Analysis

Figure 3.10 shows the small signal equivalent circuit for the cascode current mirror and calculation of the output resistance.[2]

$$V_0 = V_4 + V_2 = r_{ds4}[i_0 - g_{m4}(V_3 + V_1 - V_2) + g_{mbs4}V_2] + r_{ds2}(i_0 - g_{m2}v_1) \quad (3.10)$$

$$V_0 = i_0 r_{ds2} \quad (3.11)$$

$$V_0 = i_0[r_{ds4} + (g_{m4}r_{ds2})r_{ds4} + (r_{ds2}g_{mbs4})r_{ds4} + r_{ds2}]V_0 = i_0[r_{ds4} + (g_{m4}r_{ds2})r_{ds4} + (r_{ds2}g_{mbs4})r_{ds4} + r_{ds2}] \quad (3.12)$$

$$r_{out} = \frac{v_0}{i_0} = r_{ds4} + r_{ds2}r_{ds4}(g_{m4} + g_{mbs4}) \quad (3.13)$$

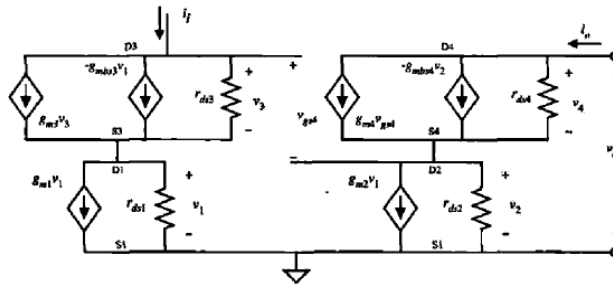


Figure 3.10: Small signal equivalent of Cascode current Mirror

3.2.2 Cascode Mirror circuit

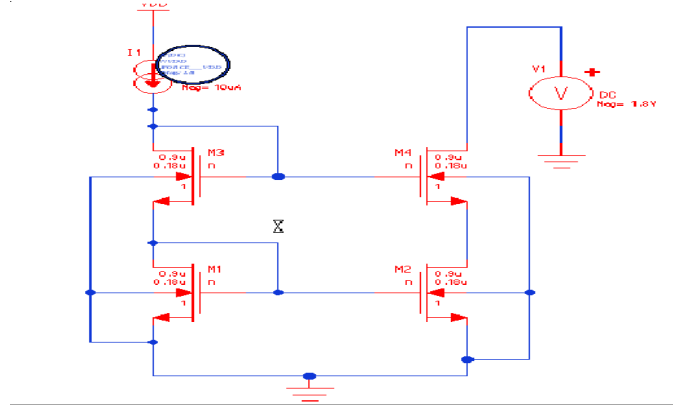


Figure 3.11: Cascode Mirror circuit

3.2.3 Pre Layout Simulation

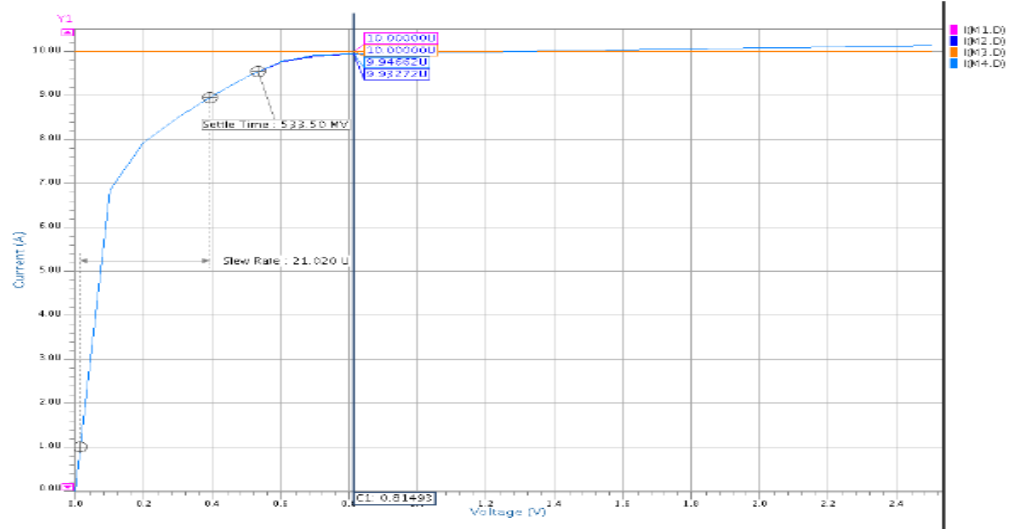
[1] Specification

Power Supply	Vdd=1.8v & Vss= -1.8v
Technology	TSMC 0.18 μ m
Model File	LEVEL 53
Spice Simulator	Eldo Spice, Design Architect and IC Station(Mentor Graphics)

Table 3.3: Technology parameters

[2] Mirror Characteristics Simulation

Here Cascode current mirror is used to achieve 10 μ A reference (or input) current at the transistor M1 and M2. Figure 3.12 shows the current through transistor M1 and M2.

Figure 3.12: I_{out} Vs. I_{in}

3.2.4 Layout making Processes

[1] Design Consideration

Table 3.4 shows the transistor aspect ratios for cascode current mirror circuit respectively.

Transistor	$W(\mu m)$	$L(\mu m)$
M1	0.9	0.18
M2	0.9	0.18
M3	0.9	0.18
M4	0.9	0.18

Table 3.4: Transistors aspect ratios for Cascode Circuit

[2] layout

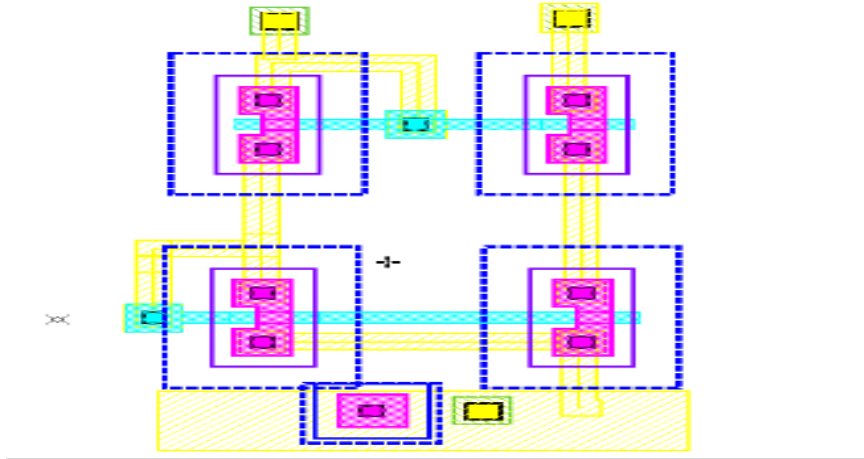


Figure 3.13: layout for Cascode Current Mirror Circuit

[3] Design Rule Check(DRC)

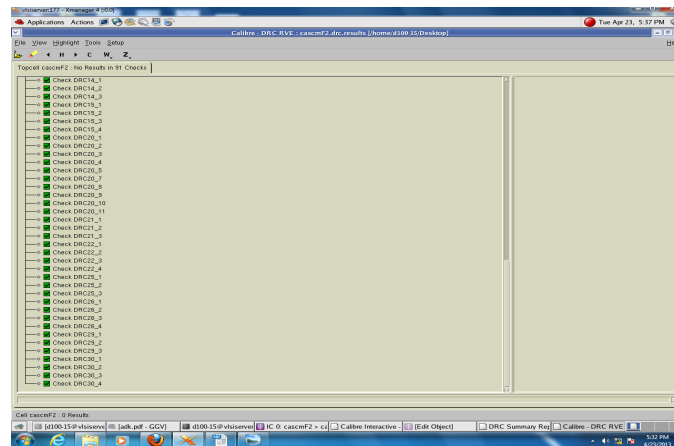


Figure 3.14: DRC for Cascode Current Mirror Circuits

[4] Layout Vs.Schematic(LVS)

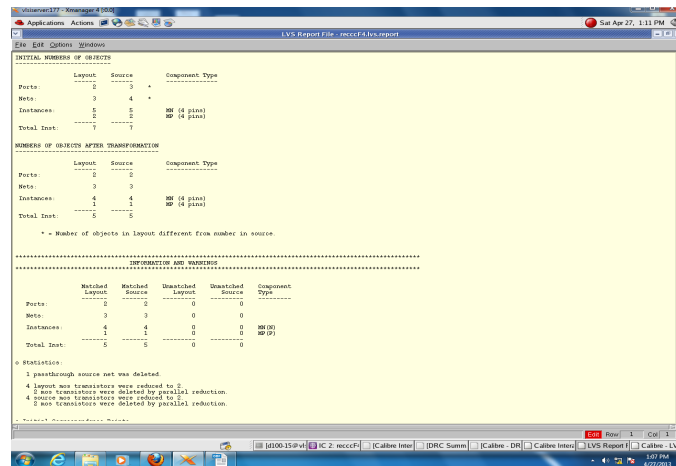


Figure 3.15: LVS for Cascode Current Mirror Circuit

[5] Parasitic Extraction(PEX) Result

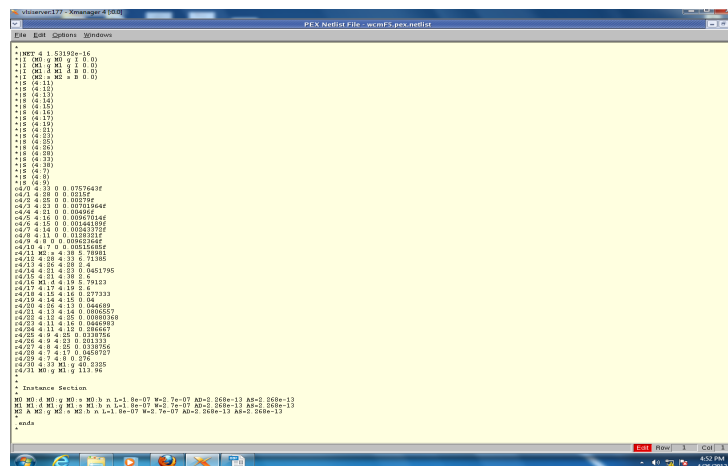


Figure 3.16: PEX Result for Cascode Current Mirror Circuit

3.2.5 Post Layout Simulation

[1] Specification

Same Specification of pre layout simulation is used here for post layout simulation process.

[2] Mirror Characteristics Simulation

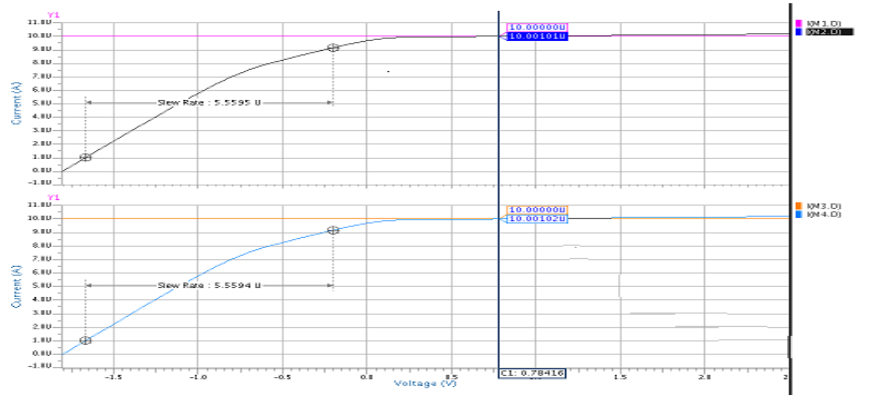


Figure 3.17: Iout Vs Iin

3.3 Wilson Current Mirror

The basic current mirror can be improved significantly with negative feedback. There are two widely used current mirrors of this type, known as a Wilson current mirror and the regulated cascode. Both offer stable current values for wide voltage swings and enhanced output impedance.[9]

Series sampling is used at the output to increase output impedance and stabilize the drain current I_{d4}

[1]suppose I_{d1} (stable reference current) constant and the voltage V_0 increase

[2]so, I_{d4} will also increase.

[3]Transistor M2 will conduct.

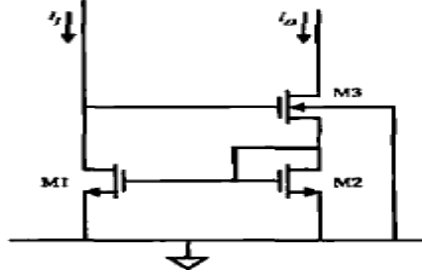


Figure 3.18: Wilson Mirror circuit

[4] I_{d4} (Current at M2) will increase by same amount while I_{d1} will constant.

As a result the voltage at node A decrease. Thus decreasing V_{gs4} and stabilizing the current through M4.

3.3.1 Small Signal analysis

Figure 3.19 shows the small signal equivalent circuit for the wilson current mirror.[1]

$$V_{sb4} = V_{gs2} \quad (3.14)$$

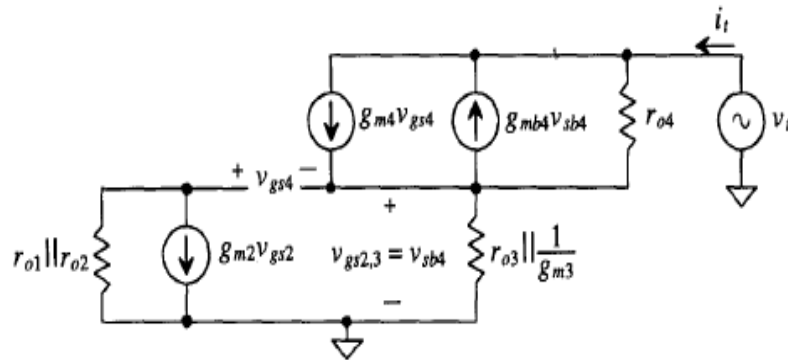


Figure 3.19: Small Signal equivalent circuit for Wilson Current Mirror

$$V_{gs2} = i_t(r_{03} \parallel (\frac{1}{g_{m3}}))V_{gs} = i_t(r_{03} \parallel (\frac{1}{g_{m3}})) \quad (3.15)$$

$$V_{gs4} = -V_{gs2}[1 + g_{m2}(r_{01} \parallel (\frac{1}{g_{m3}}))] = -i_t(r_{03} \parallel (\frac{1}{g_{m3}}))[1 + g_{m2}(r_{01} \parallel r_{02})] \quad (3.16)$$

$$i_t = g_{m4}V_{gs4} - g_{mb4}V_{sb4} + (\frac{v_t - v_{gs2}}{r_0}) \quad (3.17)$$

$$R_{out} = (\frac{v_t}{i_t}) = r_{04}[1 + g_{m4}(r_{03} \parallel (\frac{1}{g_{m3}}))(1 + g_{m2}(r_{01} \parallel r_{02}))] + g_{mb4}[(r_{03} \parallel (\frac{1}{g_{m3}})) + (\frac{1}{r_{04}})(r_{03} \parallel (\frac{1}{g_{m3}}))] \quad (3.18)$$

$$R_{out} = r_{04}[(1 + g_{m2}(r_{01} \parallel r_{02})) + g_{mb4}(\frac{1}{g_{m3}}) + (\frac{1}{r_{04}g_{m3}})] \quad (3.19)$$

It assume that and $g_{m3}=g_{m4}$ then eq.3.19 can be further reduced.

$$R_{out} = r_0 + g_{m2}(\frac{r_0^2}{2}) \quad (3.20)$$

Now, minimum voltage require to keep i_0 constant

$$V_0(min) = V_{gs3} + V_{ds4}(sat) = V_{gs3} + V_{gs4} - V_{thn,4} \quad (3.21)$$

3.3.2 Wilson Mirror circuit

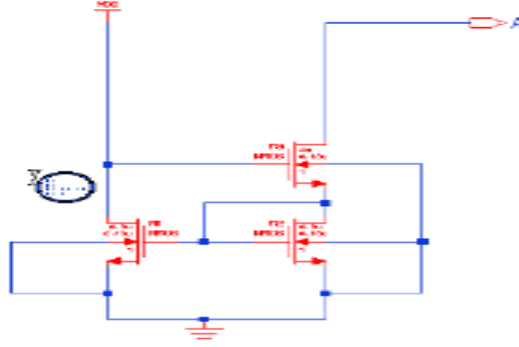


Figure 3.20: Wilson Current Mirror Circuit

3.3.3 Pre Layout Simulation

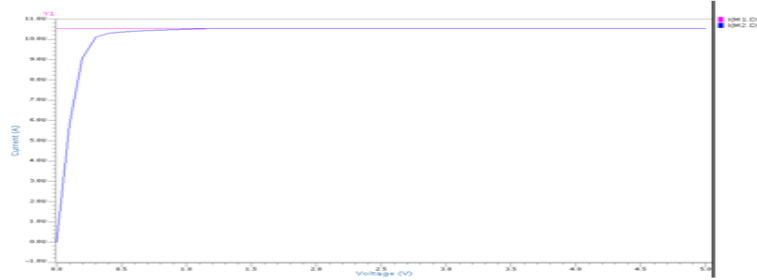
[1] Specification

Power Supply	Vdd=1.8v & Vss= -1.8v
Technology	TSMC 0.18 μ m
Model File	LEVEL 53
Spice Simulator	Eldo Spice, Design Architect and IC Station(Mentor Graphics)

Table 3.5: Technology parameters

[2] Mirror Charateristics Simulation

Here Wilson Current Mirror is used to achieve constant and stable current in saturation region.its output resistance should be infinite.

Figure 3.21: I_{out} Vs, I_{in}

3.3.4 Layout Making Process

[1] Design Consideration

Table 3.6 Shows the transistor aspect ratios for Wilson current mirror.

Transistor	$W(\mu\text{m})$	$L(\mu\text{m})$
M1	0.9	0.18
M2	0.9	0.18
M3	0.9	0.18

Table 3.6: Transistors aspect ratios for Wilson Circuit

[2] Layout

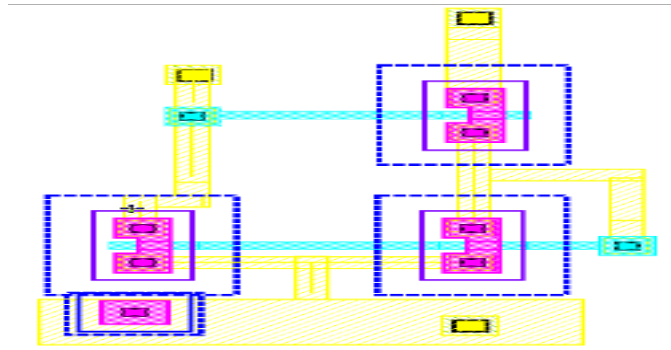


Figure 3.22: Layout of Wilson Current Mirror

[3] Design Rule Check(DRC)

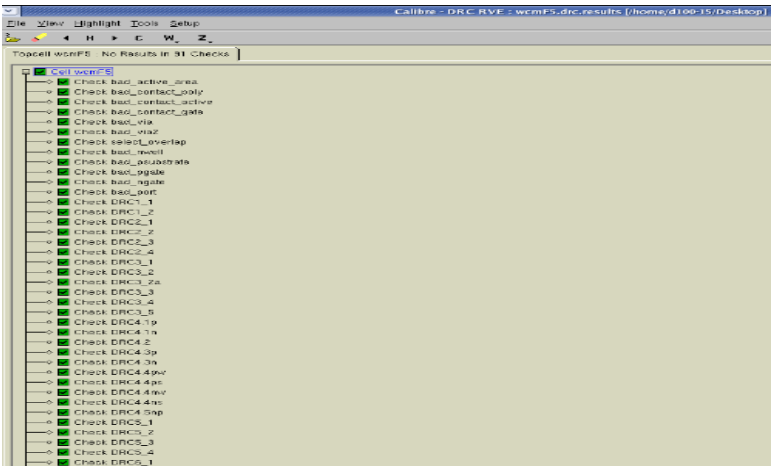


Figure 3.23: DRC for Wilson Current Mirror

[4] Layout Vs. Schematic(LVS)

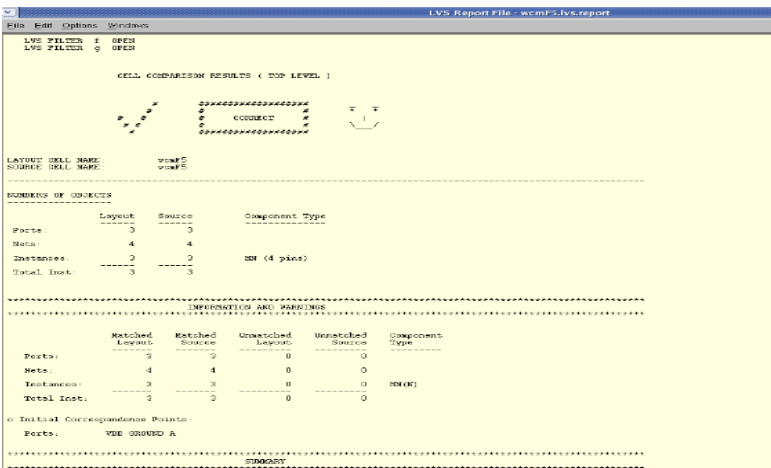


Figure 3.24: LVS for Wilson Current Mirror

[5] Parasitic Extraction(PEX))

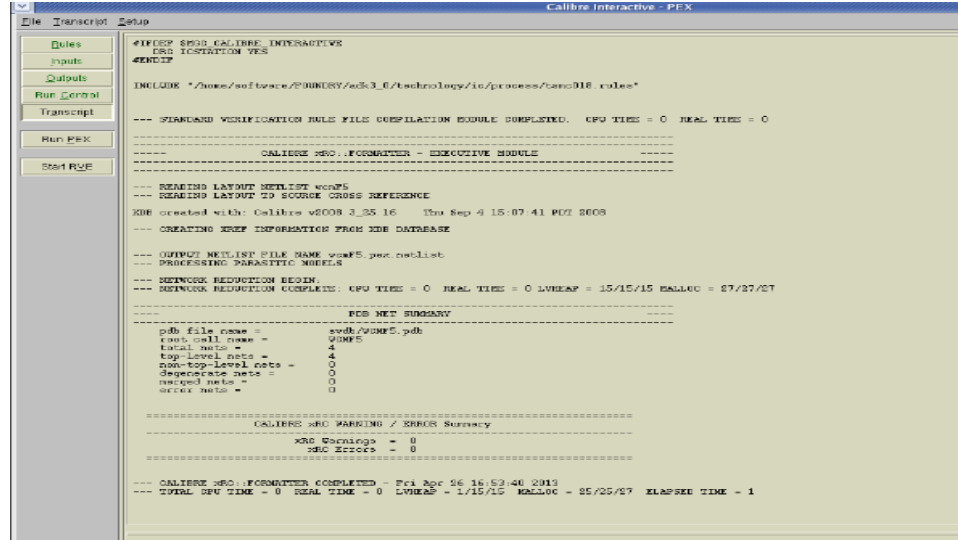


Figure 3.25: PEX Result for Wilson Current Mirror

3.4 Regulated Cascode Current Mirror

Another popular type of current mirror is the regulated cascode current mirror. This current mirror also uses negative feedback to stabilize the output current and increase the output impedance to a higher degree than the Wilson mirror. Figure 3.26 illustrates a regulated cascode current mirror.[4]

The transistor M2 and M4 make up the negative feedback loop, which stabilizes I_0 . If I_0 were to increase then since a constant current flows through M3, the voltage on node A would rise, which in turn would increase the current through M2. Since the current through M1 is also a constant amount the voltage at node B would decrease, thereby offsetting the increase in I_0 by decreasing V_{gs3} .

This current mirror offers some significant advantages over any of the previously discussed current mirrors. First the output impedance of this current mirror is significantly higher.

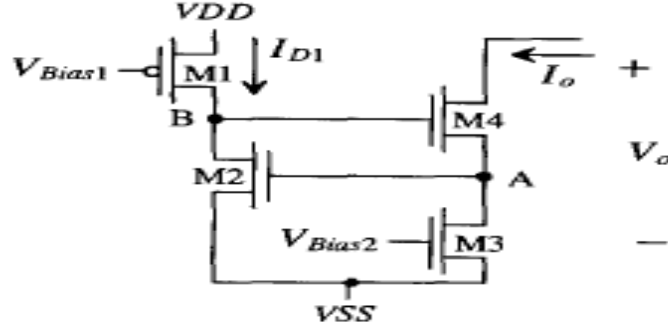


Figure 3.26: Regulated cascode Current Mirror

3.4.1 Small Signal Analysis

Figure 3.27 shows the small signal equivalent circuit for the regulated cascode current mirror.

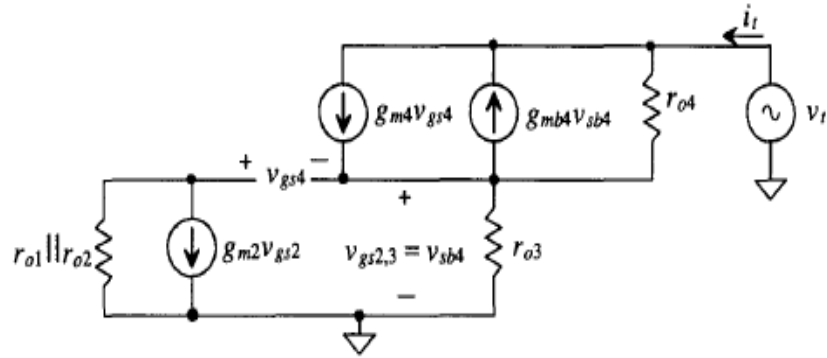


Figure 3.27: Small Signal Circuit For Regulated cascode Current Mirror

$$R_{out} = \left(\frac{v_t}{i_t} \right) = r_{o4} \left[1 + g_{m4} r_{o3} \left(1 + g_{m2} (r_{o1} \parallel r_{o2}) + g_{mb4} r_{o3} + \frac{r_{o3}}{r_{o4}} \right) \right] \quad (3.22)$$

$$R_{out} = \left(\frac{v_t}{i_t} \right) = g_{m2}g_{m4}(r_{01} \parallel r_{02})r_{03}r_{04} = \frac{g_{m2}r_{03}}{2} \quad (3.23)$$

This is approximate the same value as the Wilson current mirror.

Now we move on the next chapter, which is advance current mirror which have all beneficial performance compare to all these type of the mirrors.

Chapter 4

Advance Current Mirror

4.1 Introduction

As newer technologies with shorter channel lengths are used, it becomes more difficult to achieve reasonable op amp gain due to transistor output impedance degradation caused by short-channel effects. As a result, designers are often to use cascade current mirrors. Unfortunately, the use of conventional cascode current mirrors limits the signal swing available, which may not be tolerated in certain application. Fortunately circuits exist that do not limit the signal swings as much as current mirrors discussed in chapter3.[5]

4.2 Wide Swing Caascode Current Mirror

4.2.1 Circuit Description

The basic idea of this current mirror is to bias the drain-source voltage of transistors M2 and M3 to be close to minimum possible without them going into the triode region . Specifically, if the size shown in figure 4.1 is used, and assuming the classical squarelaw equation for long channel device are valid,transistors M2 and M3 will be biased right at the edge of the triode region. Before seeing how these biased voltage

created, note that the transistor pair M3, M4 acts like a single diode-connected transistor in creating the gate-source voltage for M3. These two transistor operate very similarly to how M3 alone would operate if its gate were connected to its source. The reason for including M4 is to lower the drain-source voltage of M3 so that it is matched to the drain-source voltage of M2. These matching makes the output current, I_0 more accurately match the input current I_{in} . If M4 were not included then the output current would be a little smaller than the input current due to the finite output impedance of M2 and M3. Other than this M4 has little effect on the circuits operation.[7]

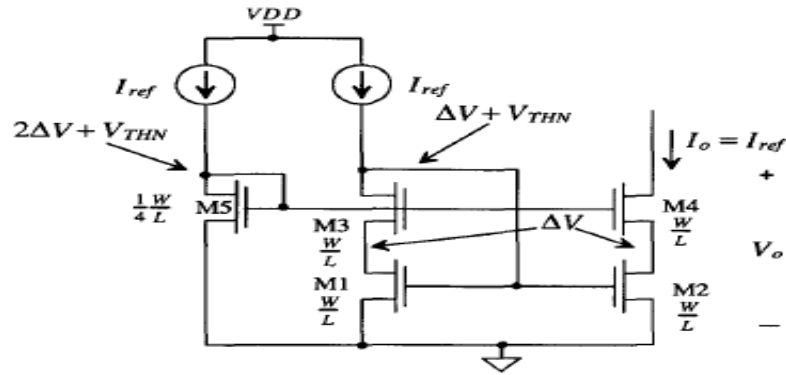


Figure 4.1: Wide Swing Cascode Current Mirror Circuit

Cascode current mirror is a variant on the cascode that can operate on a lower bias voltage. Its small-signal behavior is identical to the regular cascode, but its biasing is interesting. The extra MOSFET M5 is simply to ensure the rest stay in saturation.[7]

[A] Minimum Voltage requirement working in saturation result

To determine the bias voltage for this circuit, let V_{eff} be the effective gate-source voltage of M2 and M3, and assume all of the drain current are equal. We therefore

have

$$V_{eff} = V_{eff2} = V_{eff3} \quad (4.1)$$

Furthermore, Since M5 has the same drain current but is $(n + 1)^2$ times smaller, we have

$$V_{eff5} = (n + 1)V_{eff} \quad (4.2)$$

Similar reasoning in the effective gate-source voltage of M1 and M4 being given by

$$V_{eff5} = nV_{eff} \quad (4.3)$$

Thus

$$V_{G5} = V_{G4} = V_{G1} = (n + 1)V_{eff} + V_{th} \quad (4.4)$$

Furthermore

$$V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (nV_{eff} + V_{th}) = V_{eff} \quad (4.5)$$

This drain source voltage puts both M2 and M3 right at the edge of the triode region. Thus, minimum allowable output voltage is now

$$V_{out} > V_{eff1} + V_{eff2} = (n + 1)V_{eff} \quad (4.6)$$

A common choice for n might be simply unity, in which case the current mirror operates correctly as long as

$$V_{out} > 2V_{eff} \quad (4.7)$$

with a typical value of V_{eff} between 0.2V and 0.25V, the wide swing current mirror can guarantee that all of the transistor are in the active region even when

the voltage drop across the mirror is as small as 0.4V and 0.5V.[7] However, there is one other requirement that must be met to ensure there all transistor are in the active region. Specifically, we need

$$V_{DS4} > V_{eff} = nV_{eff} \quad (4.8)$$

To guaranteed that M4 is in the active region. To find V_{ds4} , we note that the gate of M3 is connected to the drain of M4, resulting in

$$V_{ds4} = V_{g3} - V_{ds3} = (V_{eff} + V_{thn}) - V_{eff} = V_{thn} \quad (4.9)$$

As a result, one need only ensure that V_{tn} be greater than nV_{tn} for M4 to remain in the active region not a difficult requirement. It should be noted that this circuit we analyzed assuming the bias current I_{bias} equals the input current I_{in} may be a varying current level, there is some choice as to what I_{bias} value should be chosen. One choice is to set I_{bias} to the largest expected value for I_{in} . Such a choice will ensure that none of the device exist their active region, through the drain-source voltage of M2 and M3 will be larger than necessary expect when the maximum I_{in} . is applied. As a result some voltage swing will be lost. Perhaps the more common choice in a wide swing op-amp is to let I_{bias} equal the nominal value of I_{in} . With this setting, some devices will enter triode and the output impedance will be reduced for larger I_{in} value, but such an effect during transient conditions can often be tolerated.[5]

4.2.2 Wide Swing Mirror Circuit

Figure 4.2 shows the circuit for the wide swing cascode current mirror and its output characteristics.

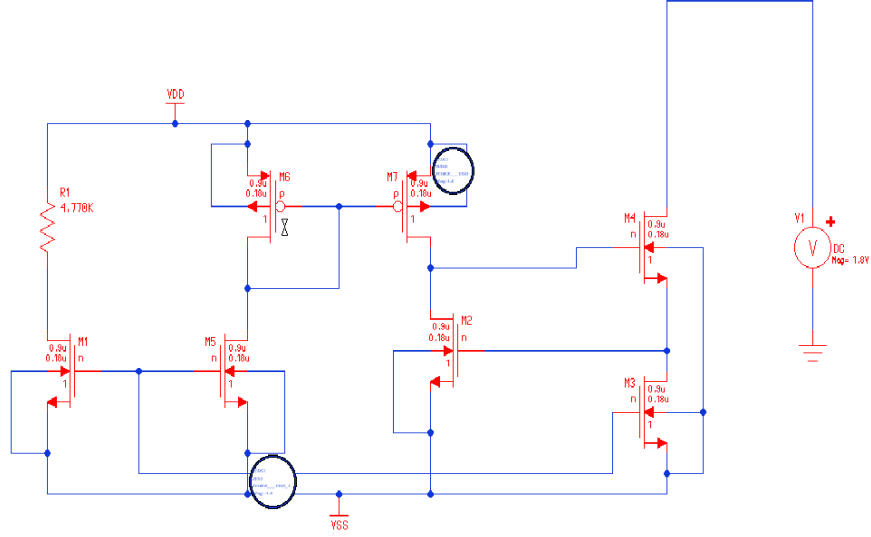


Figure 4.2: wide swing cascode Circuit

4.2.3 Pre Layout Simulation

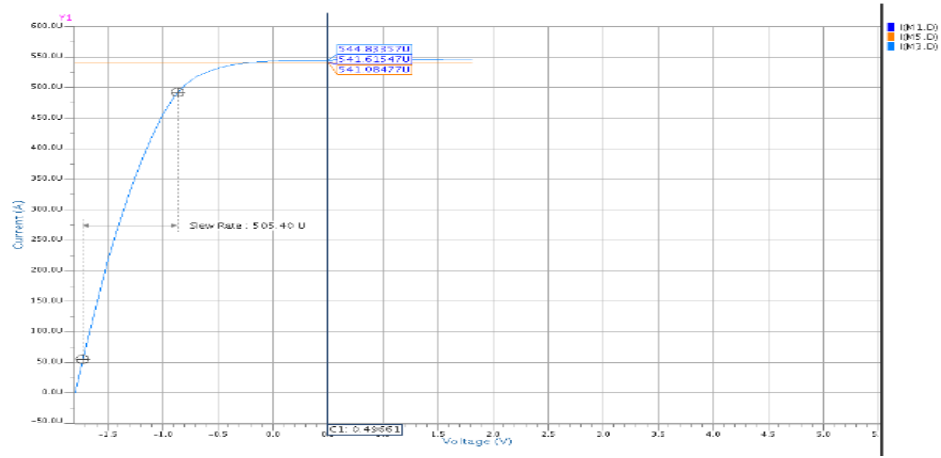
[1] Specification

Power Supply	Vdd=1.8v & Vss= -1.8v
Technology	TSMC 0.18 μ m
Model File	LEVEL 53
Spice Simulator	Eldo Spice, Design Architect and IC Station(Mentor Graphics)

Table 4.1: Technology parameters

[2] Mirror Characteristics Simulation

Here Wide Swing current mirror is used to achieve $10\mu\text{A}$ reference (or input) current at the transistor M1 and M3 using $4.770\text{K}\Omega$. Figure 3.3 shows the current drawn through transistor M1 and M2.

Figure 4.3: I_{out} Vs I_{in}

4.2.4 Layout Making Processes

[1] Design Consideration

Table 4.2 shows the transistor aspect ratios for wide swing mirror circuit

Transistor	W(μm)	L(μm)
M1	0.9	0.18
M2	0.9	0.18
M3	0.9	0.18
M4	0.9	0.18
M5	0.9	0.18
M6	0.9	0.18
M7	0.9	0.18

Table 4.2: Transistors aspect ratios for wide swing Circuit

[2] Layout

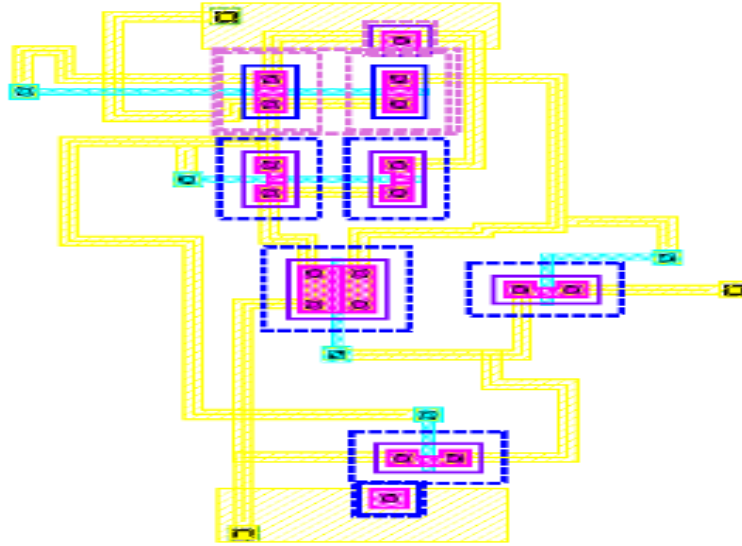


Figure 4.4: layout for Wide Swing Current Mirror Circuit

[3] Design Rule Check(DRC)

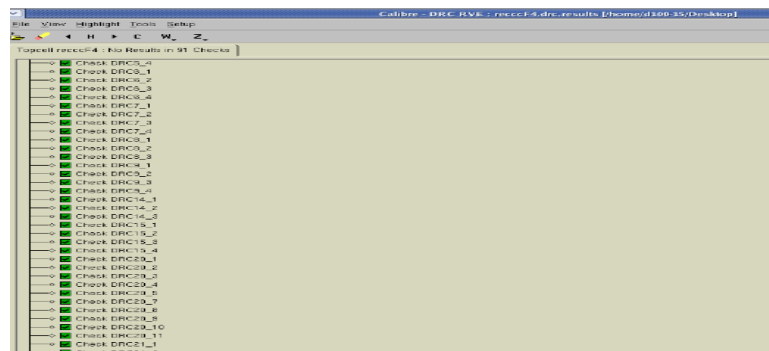
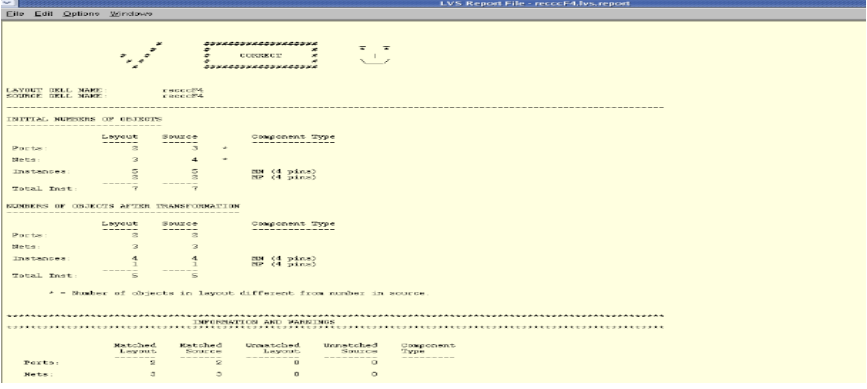


Figure 4.5: DRC for Wide Swing Current Mirror Circuit

[4] Layout Vs. Schematic(LVS)



The image shows a screenshot of a software window titled "LVS Report File - recceF4.lvs.report". At the top, there is a small schematic diagram of a circuit. Below the diagram, the report contains the following text:

LAYOUT CELL NAME: recceF4
SOURCE CELL NAME: recceF4

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Packs:	0	0	
Cells:	0	4	*
Instances:	0	0	NM (4 pins)
Total Inst:	0	0	NM (4 pins)

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Packs:	0	0	
Cells:	0	0	
Instances:	4	4	NM (4 pins)
Total Inst:	4	4	NM (4 pins)

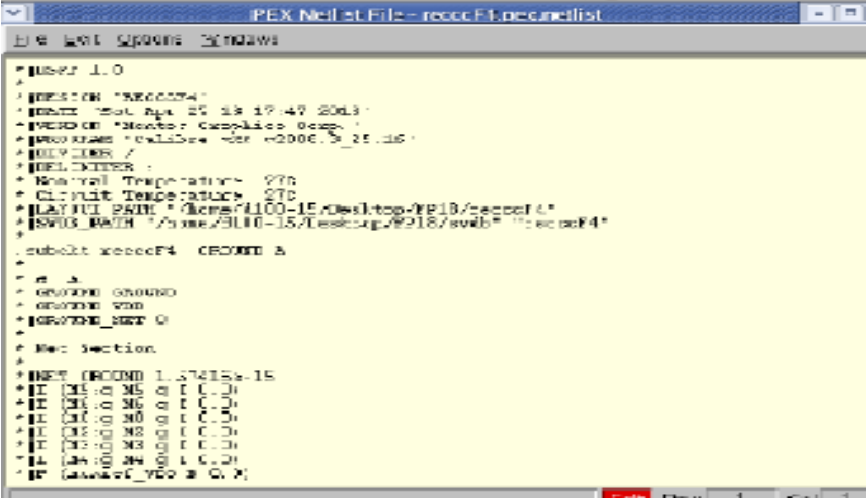
* = Number of objects in layout different from number in source.

UNMATCHED LAYOUT AND SOURCE INFORMATION

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Packs:	0	0	0	0	
Cells:	0	0	0	0	

Figure 4.6: LVS for Wide Swing Current Mirror Circuit

[5] Parasitic Extraction(PEX) Result



The image shows a screenshot of a software window titled "PEX Netlist File - recceF4.lvs.netlist". The window displays a netlist for a circuit. The netlist includes the following lines:

```

*USP7 1.0
*SECTION "RECEIVED"
*DATE "Sat Apr 25 13:19:47 2003"
*VERSION "Mentor Graphics 0comp"
*PROJECT "CellSet" "ver 2000.3 25.115"
*FILE "RECEIVED"
*FILE "RECEIVED"
* Model Temperature: 270
* Circuit Temperature: 270
* LAYOUT PATH: "/home/BUU-15/Desktop/PEX/recceF4"
* SPICE PATH: "/home/BUU-15/Desktop/PEX/recceF4"
*subckt recceF4 CROOND 5
*
* 5
* GROUND GROUND
* GROUND VDD
* GROUND_NXT 0
*
* Net section
*
* NET CROOND 1.57415e-15
* I1 M1 M5 0 1 0 0
* I2 M2 M6 0 1 0 0
* I3 M3 M7 0 1 0 0
* I4 M4 M8 0 1 0 0
* I5 M5 M9 0 1 0 0
* I6 M6 M10 0 1 0 0
* I7 M7 M11 0 1 0 0
* I8 M8 M12 0 1 0 0
* I9 M9 M13 0 1 0 0
* I10 M10 M14 0 1 0 0
* I11 M11 M15 0 1 0 0
* I12 M12 M16 0 1 0 0
* I13 M13 M17 0 1 0 0
* I14 M14 M18 0 1 0 0
* I15 M15 M19 0 1 0 0
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* I17 M17 M21 0 1 0 0
* I18 M18 M22 0 1 0 0
* I19 M19 M23 0 1 0 0
* I20 M20 M24 0 1 0 0
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* I24 M24 M28 0 1 0 0
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4.2.5 Post Layout Simulation

[1] Specification

Same Specification of pre layout simulation is used here for post layout simulation process.

[2] Mirror Characteristics Simulation

In post layout simulation we can achieve almost same as pre layout simulation result.

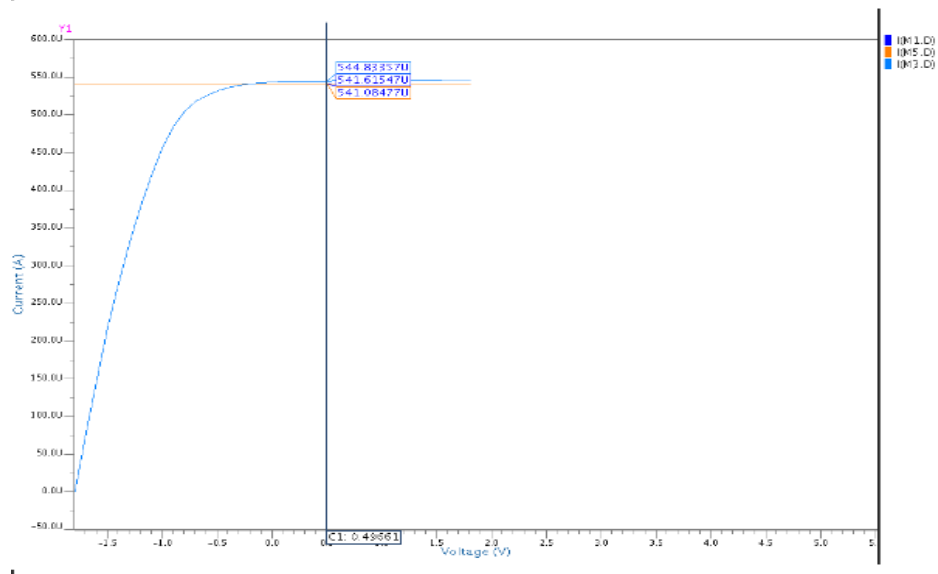


Figure 4.8: I_{out} Vs. I_{in}

Chapter 5

Proposed Current Mirror Circuit

5.1 Test Circuit [1]

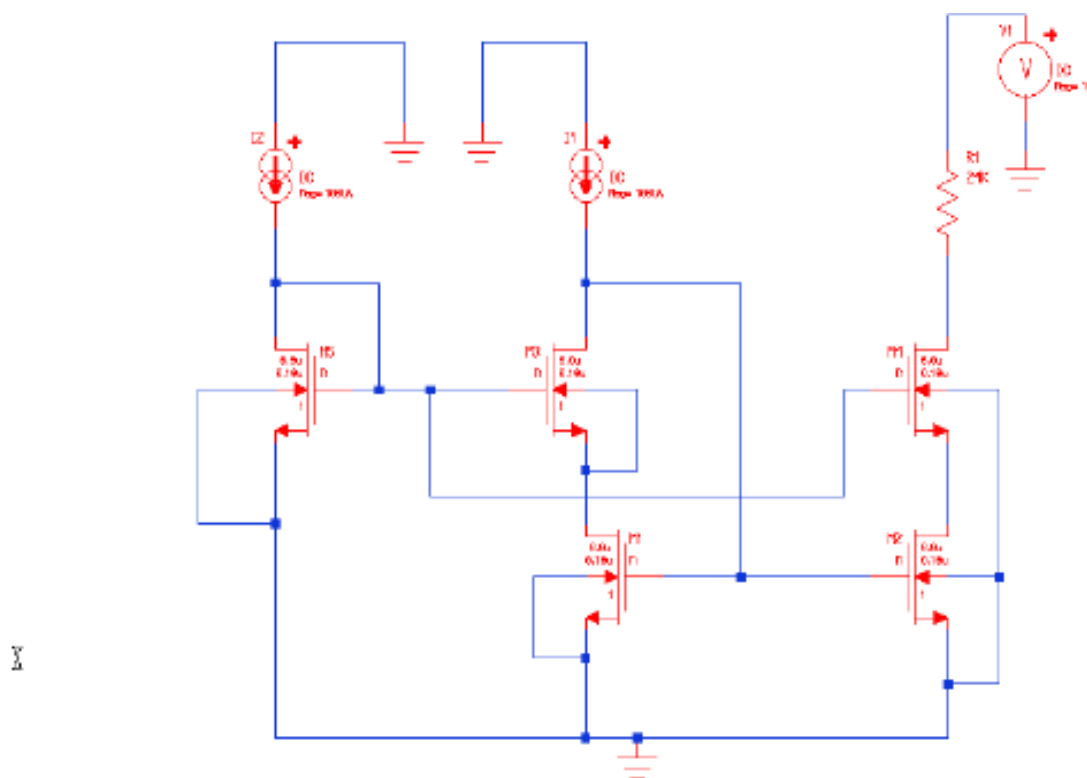


Figure 5.1: Proposed Mirror Circuit[8]

5.1.1 Simulation Waveform

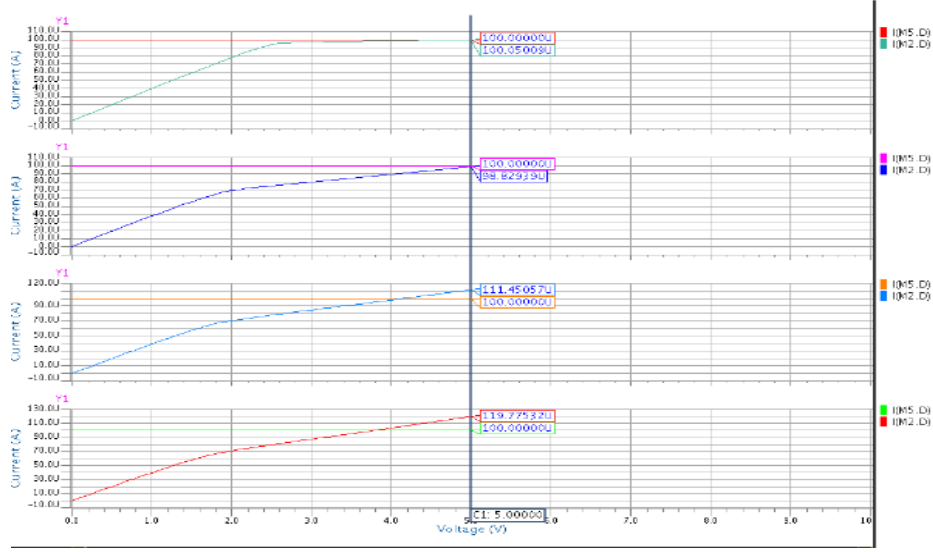


Figure 5.2: Proposed Mirror Circuit[8]

5.2 Pre Layout Simulation

[1] Specification

Power Supply	Vdd=1.8v & Vss= -1.8v
Technology	TSMC 0.18 μ m
Model File	LEVEL 53
Spice Simulator	Eldo Spice, Design Architect and IC Station(Mentor Graphics)

Table 5.1: Technology parameters

5.3 Layout Making Processes

[1] Design Consideration

Transistor	W(μm)	L(μm)
M1	0.9	0.18
M2	0.9	0.18
M3	0.9	0.18
M4	0.9	0.18
M5	0.9	0.18

Table 5.2: Transistors aspect ratios for Proposed Circuit[8]

[2] Layout

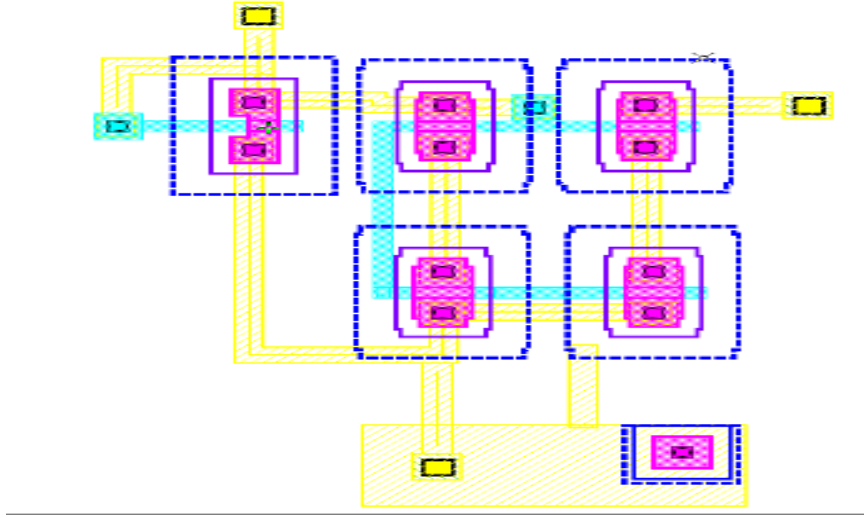


Figure 5.3: Proposed Mirror Circuit[8]

[3] Design Rule Check(DRC)

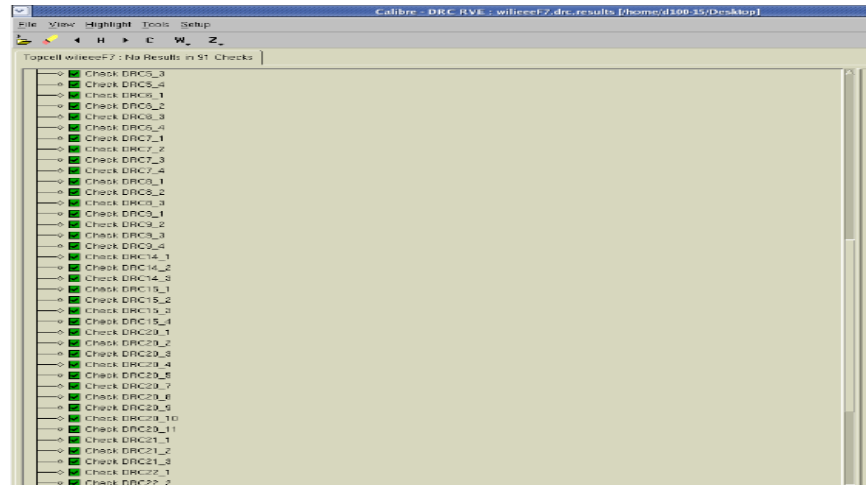


Figure 5.4: DRC for Proposed Mirror Circuit[8]

[4] Layout Vs. Schematic(LVS)

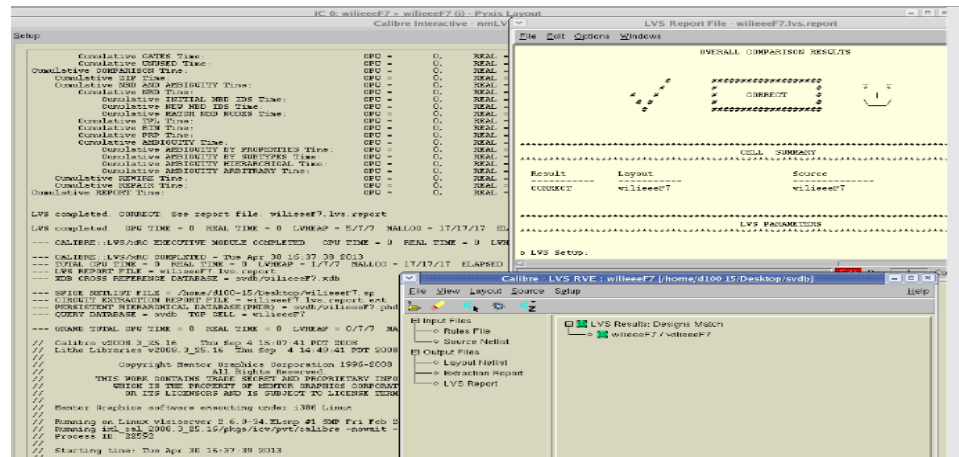


Figure 5.5: LVS for Proposed Mirror Circuit[8]

[5] Parasitic Extraction(PEX) Result

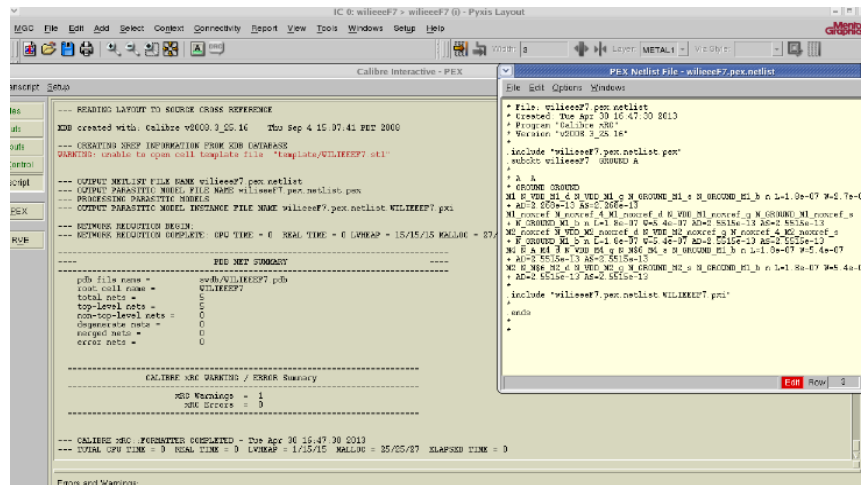


Figure 5.6: PEX Result for Proposed Mirror Circuit[8]

5.3.1 Post Layout Simulation

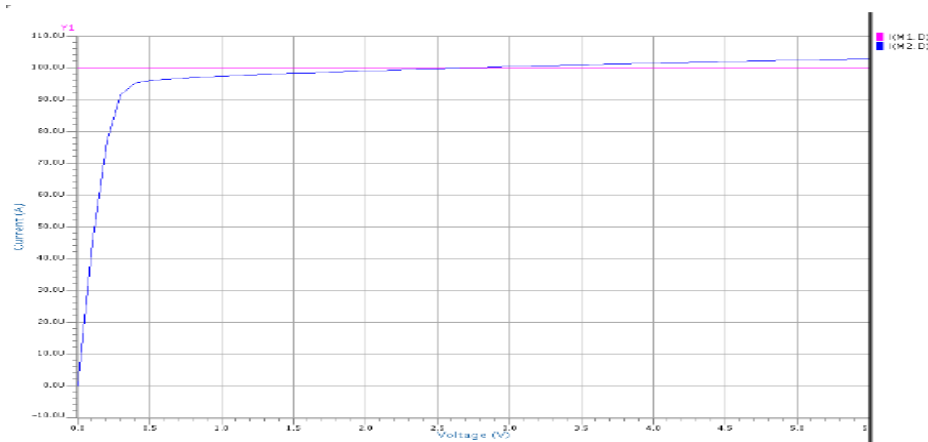


Figure 5.7: I_{out} Vs. I_{in} for Proposed Mirror Circuit[8]

5.4 Test Circuit [2]

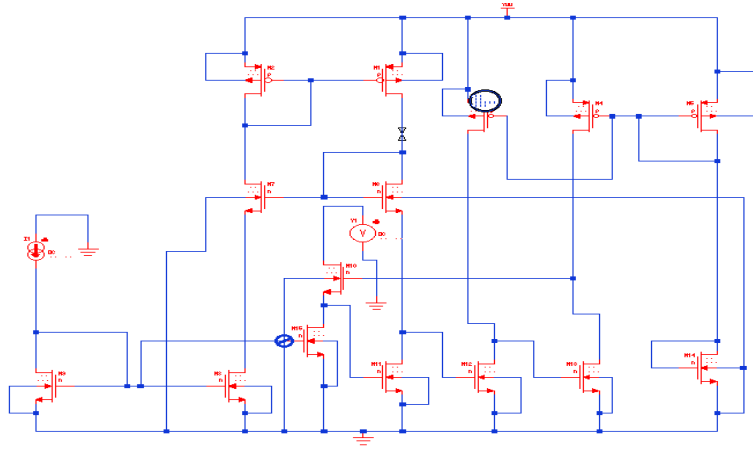


Figure 5.8: Proposed Mirror Circuit[3]

Pre Simulation Result

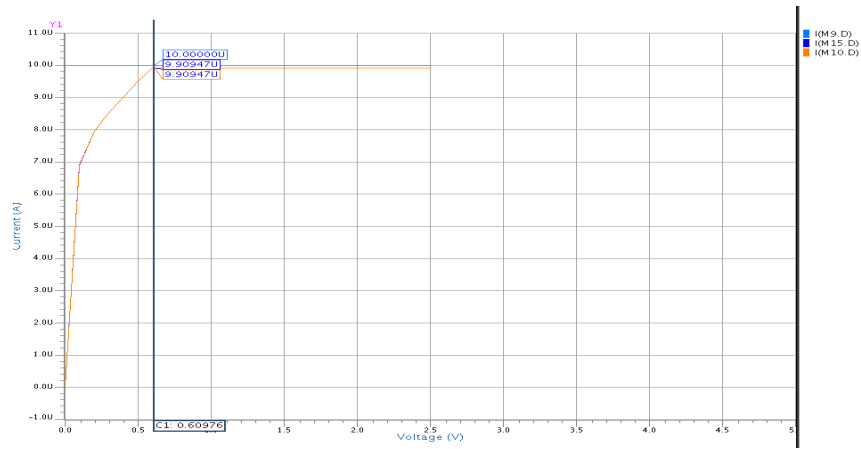


Figure 5.9: Proposed Mirror Circuit[3]

5.5 Test Circuit [3]

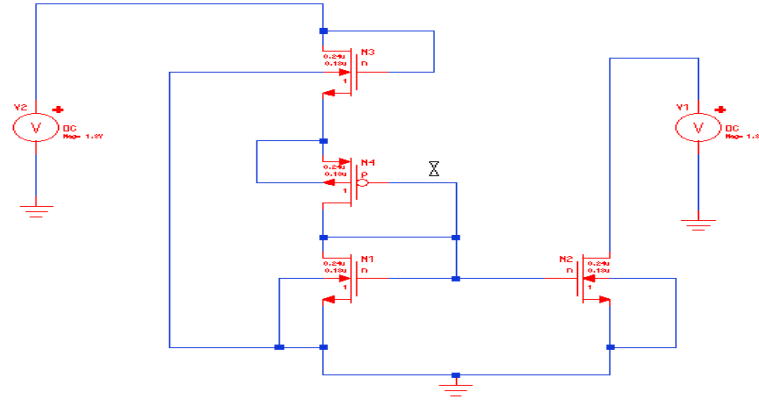


Figure 5.10: Proposed Mirror Circuit[3]

Pre Simulation Result

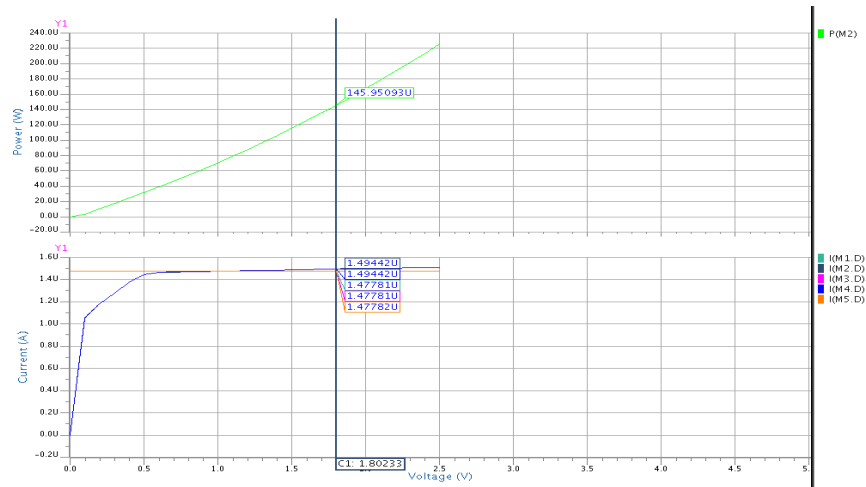


Figure 5.11: Proposed Mirror Circuit[3]

5.5.1 Transistor aspect ratios for Current Mirror Circuits

Topology	Transistor	$W(\mu\text{m})/L(\mu\text{m})$
Simple	M1,M2	0.9/0.18,0.9/0.18
Cascode	M1,M2,M3,M4	0.9/0.18,0.9/0.18,0.9/0.18,0.9/0.18
Wilson	M1,M2,M3	0.9/0.18,0.9/0.18,0.9/0.18
Wide Swing	M1,M2,M3,M4,M5,M6,M7	0.9/0.18 (M1 to M7)

Table 5.3: Transistor aspect ratios for all current mirror circuits

[A] Transistor aspect ratios for Test Mirror Circuits

Topology	Transistor	$W(\mu\text{m})/L(\mu\text{m})$
Test Circuit[1]	M1,M2,M3,M4,M5	0.9/0.18,0.9/0.18
Test Circuit[2]	M1,2,3,4,5[p] & M6toM15[n]	2.7/0.18[p] & 0.9/0.18[n]
Test Circuit[3]	M1,M2,M3,M4p	0.9/0.18,0.9/0.18,0.9/0.18,2.7/0.18p

Table 5.4: Transistor aspect ratios for current mirror circuits

[B] Analysis of Mirror Circuits

Analysis	Simple	Cascode	Wilson	Wide Swing Cascode
Power Supply	1.8v	1.8v	1.8v	1.8v
Technology	TSMC 0.18 μ	TSMC 0.18 μ	TSMC 0.18 μ	TSMC 0.18 μ
Model File	LEVEL 53	LEVEL 53	LEVEL 53	LEVEL 53
No. of Transistor	2	4	3	7
Power Consume	13.0555 μW	28.7606 μW	51.7361 μW	61.2562 μW
O/P Resistance	1.34K Ω	1.88K Ω	6.97K Ω	33.76K Ω

Table 5.5: Parameters of Mirror Circuits

[C] Analysis of Test Circuits

Analysis	Test Cir- cuit[1]	Test Cir- cuit[2]	Test Cir- cuit[3]
Power Supply	1.8v	1.8v	1.8v
Technology	TSMC 0.18 μ	TSMC 0.18 μ	TSMC 0.18 μ
Model File	LEVEL 53	LEVEL 53	LEVEL 53
No. of Transistor	5	15	4
Power Consumption	151.8483 μ W	428.1156 μ W	18.3238 μ W
O/P Resistance	39.37K Ω	227.27K Ω	19.1866K Ω

Table 5.6: Parameters of Test Mirror Circuits

[D] Summary

Topology	Accuracy	Output Resistance	Min. O/P Volt.
Simple	Poor	r_{ds}	V_{ON}
Cascode	Excellent	$g_m r_{ds}^2$	$V_T + 2V_{ON}$
Wilson	Excellent	$r_{ds} + g_m r_{ds}^{3/2}$	$2V_{ON}$
Wide Swing Cas- code	Excellent	$g_m r_{ds}^2$	$2V_{ON}$

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The design of current mirrors is one of the most challenging aspects in the analog and mixed signal design. They are one of the most widely used building block in analog IC design. They are used as current sources and as active loads in many devices. The most important issue is the offset in the current replica of the current mirror. As was exposed, this is one of the biggest challenges in the design of these devices.

The purpose of this work was to improve the accuracy of the current replica in the current mirror presented. The approach consists in dynamically controlling a biasing node to copy with changes in current input and reduce the offset. To test this approach the current mirror with one of the highest accuracy in literature was used. Number of Transistor are same for different current mirror circuits. We can achieve $10\mu\text{A}$ by using TSMC $0.18\mu\text{m}$ CMOS technology. Thus area requirement is more and power dissipation is high for advanced current mirror.

Output current variation against supply changes is low for advanced current mirror topologies compare to basic current mirror circuits.

6.2 Future Work

Design, simulation and characterization of following topology

- Enhanced-Output impedance Current Mirror.
- Wide-swing constant transconductance bias circuit.

Pre and Post Layout simulation of all topologies.

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- [10] Dhaval S.Shukla, Design, Characterization and Simulation of Advanced Current Mirror. Project Thesis, May 11.

APPENDIX 1- TSMC 0.18um TSMC Data Shee

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T44E SPICE BSIM3 VERSION 3.1 PARAMETERS

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+VERSION = 3.1 TNOM = 27 LEVEL = 49
+XJ = 1E-7 NCH = 2.3549E17 TOX = 4.1E-9
+K1 = 0.5887715 K2 = 3.059696E-3 VTH0 = 0.3694291
+K3B = 4.5379416 W0 = 1E-7 K3 = 1E-3
+DVT0W = 0 DVT1W = 0 NLX = 1.859182E-7
+DVT0 = 1.3484262 DVT1 = 0.3669657 DVT2W = 0
+U0 = 262.597552 UA = -1.45346E-9 DVT2 = 0.0321807
+UC = 6.065042E-11 VSAT = 1.049851E5 UB = 2.388329E-18
+AGS = 0.4217527 B0 = 1.405467E-7 A0 = 1.8958229
+KETA = -5.710529E-3 A1 = 3.800448E-4 B1 = 5E-6
+RDSW = 114.1849719 PRWG = 0.5 A2 = 0.8605984
+WR = 1 WINT = 0 PRWB = -0.2
+XL = 0 XW = -1E-8 LINT = 1.38756E-8
+DWB = 1.403585E-8 VOFF = -0.0923188 DWG = -1.403515E-8
+CTT = 0 CDSC = 2.4E-4 NFACTOR = 2.3339618
+CDSCB = 0 ETA0 = 2.976763E-3 CDSCD = 0
+DSUB = 0.0147417 PCLM = 0.7500199 ETAB = 9.401588E-6
+PDIBLC2 = 2.164741E-3 PDIBLCB = -0.1 PDIBLC1 = 0.1481831
+PSCBE1 = 4.02605E10 PSCBE2 = 2.319101E-9 DROUT = 0.6836492
+DELTA = 0.01 RSH = 6.6 PVAG = 9.51717E-3
+PRT = 0 UTE = -1.5 MOBMOD = 1
+KT1L = 0 KT2 = 0.022 KT1 = -0.11
+UB1 = -7.61E-18 UC1 = -5.6E-11 UA1 = 4.31E-9
+WL = 0 WLN = 1 AT = 3.3E4
+WWN = 1 WWL = 0 WW = 0
+LLN = 1 LW = 0 LL = 0
+LWL = 0 CAPMOD = 2 LWN = 1
+CGDO = 8.88E-10 CGSO = 8.88E-10 XPART = 0.5
+CJ = 9.738002E-4 PB = 0.8 CGBO = 1E-12
+CJSW = 2.656147E-10 PBSW = 0.8007021 MJ = 0.3806198
+CJSWG = 3.3E-10 PBSWG = 0.8007021 MJSW = 0.1397059
+CF = 0 PVTH0 = -1.627734E-4 MJSWG = 0.1397059
+PK2 = 9.037624E-5 WKETA = 3.850841E-3 PRDSW = -1.9138777
+PU0 = 8.1162291 PUA = 1.139148E-11 LKETA = -5.396657E-3
+PVSAT = 1.247309E3 PETA0 = 1.003159E-4 PUB = 0
PKETA = 3.393907E-3 )

```

Figure 6.1: NMOS Model Parameter of 0.18um Technology

```

.MODEL CMOSF PMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL = 49
+XJ          = 1E-7      NCH     = 4.1589E17    TOX    = 4.1E-9
+K1          = 0.5828995 K2     = 0.0266823    VTH0   = -0.3944719
+K3B        = 14.3383713 W0     = 1E-6          K3     = 0
+DVT0W      = 0         DVT1W  = 0          NLX    = 1.373459E-7
+DVT0       = 0.6336613 DVT1  = 0.2409053    DVT2W  = 0
+U0         = 112.690631 UA     = 1.417849E-9    DVT2   = 0.1
+UC         = -1E-10    VSAT   = 1.850699E5    UB     = 1.12483E-21
+AGS        = 0.375203 B0     = 3.569636E-7    A0     = 1.7532818
+KETA       = 0.0205518 A1     = 0.4474986    B1     = 1.12458E-6
+RDSW      = 243.82298 PRWG   = 0.5          A2     = 0.3631955
+WR         = 1         WINT   = 0          PRWB   = 0.5
+XL         = 0         XW     = -1E-8       LINT   = 2.551606E-8
+DWB        = 2.595671E-10 VOFF  = -0.0937437    DWG    = -4.374325E-8
+CIT        = 0         CDSC   = 2.4E-4      NFACTOR = 2
+CDSCB      = 0         ETA0   = 0.1136843    CDSCD  = 0
+DSUB       = 1.0613195 PCLM  = 2.4303317    ETAB   = -0.0748821
+PDIBLC2    = 0.0239307 PDIBLCB = -1E-3      PDIBLC1 = 7.845168E-4
+PSCBE1     = 3.207414E9 PSCBE2 = 9.282296E-10 DROUT  = 0
+DELTA      = 0.01     RSH    = 7.5        PVAG   = 15
+PRT        = 0         UTE    = -1.5       MOBMOD = 1
+KT1L       = 0         KT2    = 0.022      KT1    = -0.11
+UB1        = -7.61E-18 UC1     = -5.6E-11    UA1    = 4.31E-9
+WL         = 0         WLN    = 1          AT     = 3.3E4
+WWN        = 1         WWL    = 0          WW     = 0
+LLN        = 1         LW     = 0          LL    = 0
+LWL        = 0         CAPMOD = 2          LWN    = 1
+CGDO       = 6.34E-10 CGSO   = 6.34E-10    XPART  = 0.5
+CJ         = 1.148543E-3 PB     = 0.8476511    CGBO   = 1E-12
+CJSW       = 2.382898E-10 PBSW  = 0.8222976    MJ     = 0.4067434
+CJSWG      = 4.22E-10  PBSWG = 0.8222976    MJSW  = 0.3300124
+CF         = 0         PVTH0  = 3.507137E-3    MJSWG = 0.3300124
+PK2        = 3.610481E-3 WKETA  = 0.0334716    PRDSW  = 17.811338
+PU0        = -2.0541594 PUA    = -8.93082E-11 LKETA  = -3.202602E-3
+PVSAT      = -50      PETA0  = 1.003159E-4    PUB    = 1E-21
                                PKETA  = -1.696047E-3
*)

```

Figure 6.2: PMOS Model Parameter of 0.18um Technology