Design and Simulation of Third Generation Current Conveyor and Its Application

Major Project Report

Submitted in partial fulfillment of the requirements

For the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Shah Payal Dineshkumar

(11MECV16)

Department of Electronics & Communication Engineering

Institute of Technology,

Nirma University, Ahmedabad-382 481

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Under the Guidance of

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MAY 2013

Declaration

This is to certify that

(i) The thesis comprises my original work towards the degree of Master of Technology in Electronics & Communication Engineering(VLSI Design) at Nirma University and has not been submitted elsewhere for a degree.

(ii) Due acknowledgement has been made in the text to all other material used.

Shah Payal Dineshkumar

Certificate

This is to certify that the Major Project entitled **"DESIGN AND SIMULATION OF THIRD GENERATION CURRENT CONVEYOR AND ITS APPLICATION** submitted by **Shah Payal D.(11MECV16)**,towards the partial fulfillment of the requirements for the degree of **Master of Technology (VLSI Design)** in the field of **Electronics and Communication** of Nirma University is the record of work carried out by her under our supervision and guidance. The work submitted has reached a level required for being accepted for examination. The results embodied in this major project, to the best of our knowledge, have not been submitted to any other University or Institution for award of any degree or diploma.

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Acknowledgement

The work presented in this report could only be realized with the aid and support of many people.It is therefore a great honor to me to express my gratitude to them.

First of all,I am extremely grateful to my research guide,Dr.Amisha Naik,who taught me many fundamental theories of current mode ckts.Without her valuable guidance,scholarly inputs and consistent encouragement,I cannot make such wonderful work.She supported me with valuable advices and helped me to overcome many problems.

This work was possible only because of the unconditional support provided by Dr.N.M.Devashrayee.A person who established VLSI design course in the Nirma University.A person with friendly and positive disposition,he always guide me in proper way with provision of freedom to take my decision by myself.I really thankful to the GOD who give me opportunity to work under such great personality.

I would like to thank Dr.Usha Mehta for her encouragement and support.She always give me valuable suggetions on presentation skill which make my presentation more effective.

I would like to thank Prof.N.P.Gajjar for his valuable suggetions on the application of CCIII,which are very useful for the further research.

I would like to thank Mr.Prasann Shukla for his valuable help in laboratory.I would like to thank Ms.Krupaxi Patel for the administrative help.

I would like to express my gratitude towards my parents who helped me and encouraged me to the every phase of my personal and professional life.Without their support,I can not finish my work.

I would like to extend my gratitude towards my husband and my family for their moral support.

Finally,I would like to express my gratitude to all my team members who always showered blessings on me.

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Abstract

This project report deals with the design of first generation current conveyor,second generation current conveyor and third generation current conveyor. Current controlled conveyor-II is also designed with trans linear structure. By using CCC-II,its X and Z node trans impedance will vary and it will be useful for filter application. By combining two second generation current conveyors(CCII+),we achieve third generation current conveyor. This allows to achieve very good results in the systems with a very low power supply.This design of third generation current conveyor is simulated using a standard 0.18um TSMC 1P,6M CMOS process in design architect and IC station from Mentor Graphics.Its DC,AC and Transient analysis is carried out with ELDO tool.Its pre layout and post layout results are compared which show 3.67% variation between functions. The versatility of this circuit will find applications in many areas. In this report,current sensing application is designed with CCIII. This application will use to find current flowing in to the signal. Therefore,it is very useful in low voltage low power current measuring devices.Furthermore,Its applications as integrator and differentiator are designed and simulated.

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Chapter 1

Introduction

The current-conveyor, published in 1968 by Adel Sedra, represented the first building block intended for current signal processing. In 1970 appeared the enhanced version of the current-conveyor: the second-generation current-conveyor CCII. The current-mode approach[15, 16] which considers the information flowing on time-varying currents. Current-mode techniques are characterized by signals as typically processed in the current domain. Current-mode circuits have some recognized advantages over voltage mode circuits:

(1)When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits[14]. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances[14]. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques[14]. Current-mode interconnection circuits in particular show promising performance[14].

(2)When the signal is conveyed as a current, the voltages in MOS-transistor circuits are proportional to the square-root of the signal, if saturation region operation is assumed for the devices[14]. Similarly, in bipolar transistor circuits the voltages

are proportional to the logarithm of the signal[14]. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible[14]. This feature is utilized for example in log-domain filters, switched current filters, and in nonlinear current-mode circuits in general[14]. Unfortunately, as a consequence of the device mismatches this non-linear operation may generate an excessive amount of distortion for applications with high linearity requirements[14]. Thus, in certain current-mode circuits, linearisation techniques are utilized to reduce the non linearity of the transistor trans conductance, in which case the voltage signal swing is not reduced[14].

(3)Voltage-mode operational amplifier circuits have limited bandwidth at high closed-loop gains due to the constant gain-bandwidth product[14]. Furthermore, the limited slew-rate of the operational amplifier affects the large-signal, highfrequency operation[14]. When wide bandwidth, low power consumption and low voltage operation are needed simultaneously, the voltage-mode operational amplifier easily becomes too complex[14].

(4) Current mode circuits do not require a high voltage gain, so high performance amplifiers are not needed[12].

(5)Current mode circuits do not need high precision passive components, so they can be designed almost entirely with transistors[12]. This makes the current mode circuits compatible with typical digital processes[12].

Finally, they show high performance in terms of speed, bandwidth and accuracy[12].

Chapter 2

First Generation Current Conveyor

2.1 Introduction

CCI is a three-terminal device, schematically represented in figure 2.1.

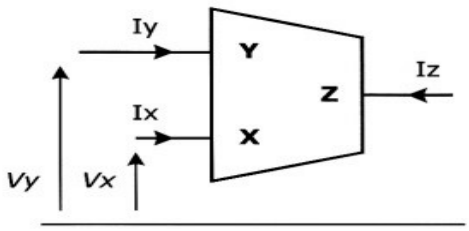


Figure 2.1: CCI block representation[12]

A voltage is applied to Y node, the same voltage will appear at X node, while the opposite happens to currents[12]. In fact, the current flowing at Y node is equal to the one flowing at X node; this current is CONVEYED to the output Z node[12].

Current at Z node can flow in the direction of Ix or in the opposite one[12]. In the matrix description reported in figure 2.2, we assume that sign + stays for currents

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} Vy \\ Ix \\ Vz \end{bmatrix}$$

CCI Node	Impedance level
X	Low (ideally 0)
Y	Low (ideally 0)
Z	High (ideally ∞)

Figure 2.2: CCI characteristics

flowing in the same direction, while sign stays for the opposite situation, considering CCI as reference[12]. In the first case we have a positive CCI (named CCI+), in the second case a negative CCI (or CCI-). X and Y nodes have a low impedance level, ideally zero, whereas Z node shows a high impedance level, ideally infinite[12].

2.2 Specification:

CCI characteristics(90nm technology)	
Data	**Simulated Value**
Voltage supply	**$\pm$ 1.8V**
Power consumption	**112.2005Uwatts**
Dynamic Range	**-0.2mV,0.2mV**
Voltage Gain	**2.5**
Current Gain	**1.04**
Biasing Current(I0)	**25 μA**

Table 2.1: Specification of CCI

2.3 Schematic:

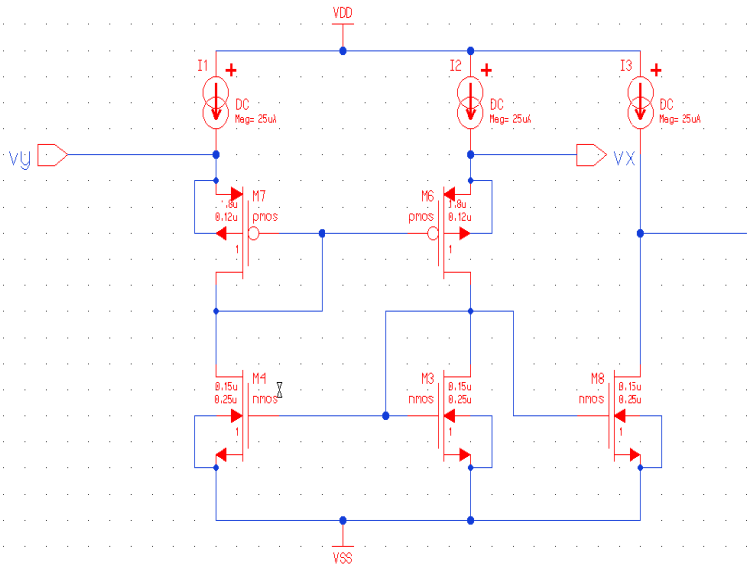


Figure 2.3: Schematic of First Generation Current Conveyor

2.4 Simulation Results:

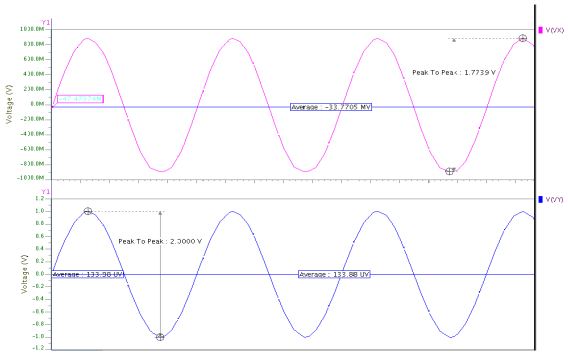


Figure 2.4: Transient response of voltages at node X,Y in 90nm CMOS technology

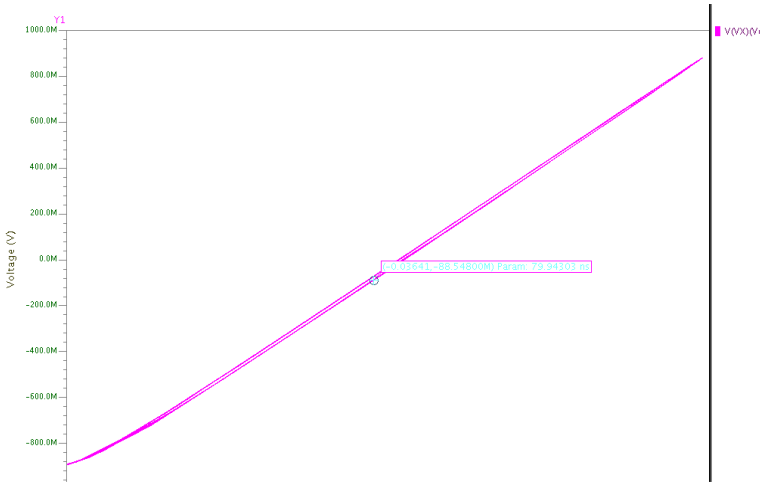


Figure 2.5: Voltage transfer characteristic for CCI in 90nm CMOS technology

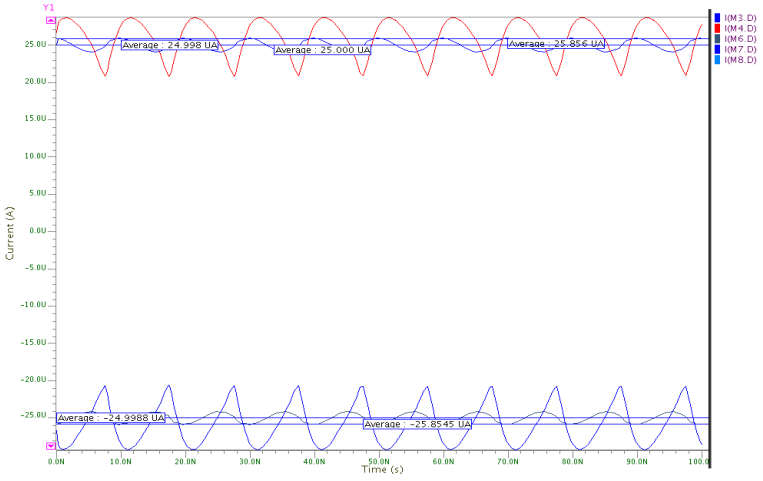


Figure 2.6: Transient response of currents at node X,Y,Z for 90nm CMOS technology

Chapter 3

Second Generation Current Conveyor

3.1 Introduction

CCII is also three terminal device described below:

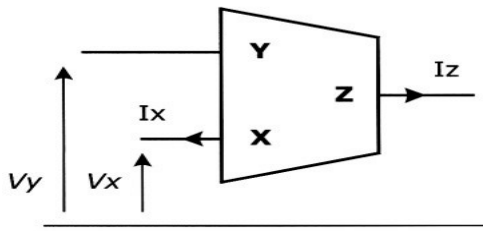


Figure 3.1: Block Representation of CCII[12]

A voltage is applied to Y node, the same voltage will appear at X node, current flowing at X node is CONVEYED to the output Z node. Node Y is high impedance node therefore it is represented by absence of current.

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} Vy \\ Ix \\ Vz \end{bmatrix}$$

CCII Node	Impedance level
X	Low (ideally 0)
Y	High (ideally ∞)
Z	High (ideally ∞)

Figure 3.2: Characteristics representation of CCII

3.2 NMOS transistor as a CCII:

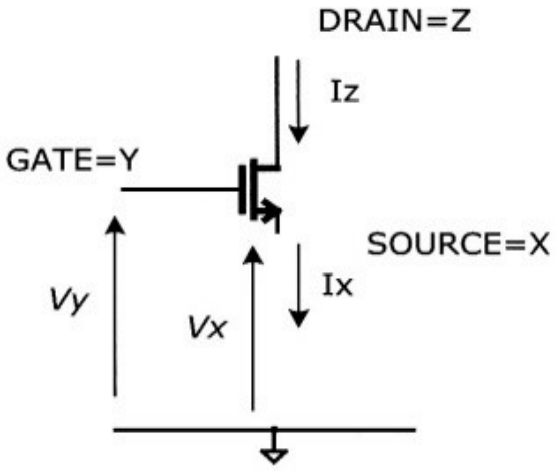


Figure 3.3: Schematic representation of NMOS transistor[12]

in above figure,whatever voltage is applied to Y node is appeared to the X node,and whatever current is flowing through X node,same current is also flowing through Z node but directions are opposite. Therefore,it fulfills the requirement of CCII(-).

3.2.1 Schematic and simulation results:

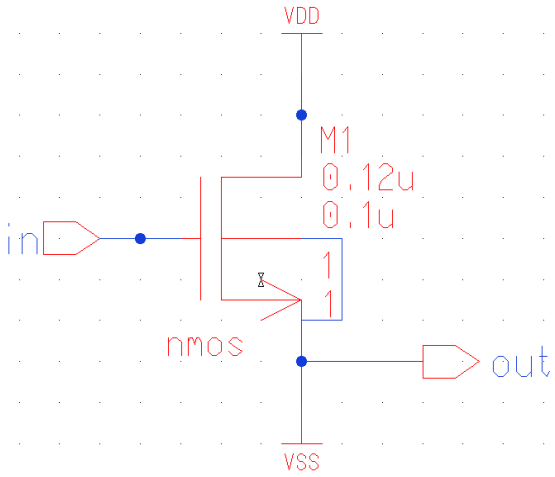


Figure 3.4: Schematic of NMOS transistor as CCII in 90nm CMOS technology

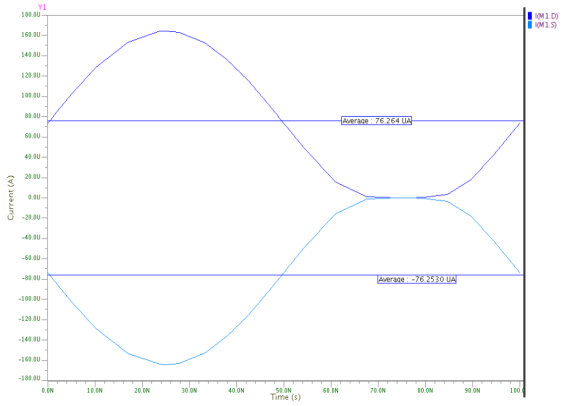


Figure 3.5: transient response of Id and Is currents for NMOS in 90nm CMOS technology

3.3 Current Controlled Current Conveyor CCCII

The operation of the CCCII is described by the following matrix:

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} Vy \\ Ix \\ Vz \end{bmatrix}$$

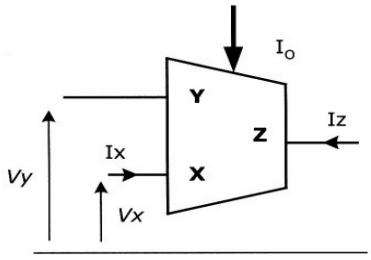


Figure 3.6: Block representation and matrix presentation of CCCII[7]

The current output at port Z (iz) that is conveyed from the input current at port X (ix) is expressed as , Ix = Iz = (Vx-Vy)/ Rx[7] Current controlled conveyor II is used for filter application. Its trans linear structure is used to utilize the parasitic floating intrinsic trans resistance at port X(Rx)[7]. Trans resistance at port X can be tuned electronically by adjusting the bias current[7].

3.3.1 Translinear structure:

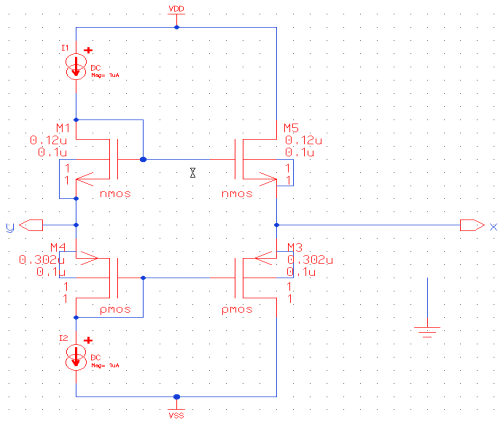


Figure 3.7: Schematic of translinear structure[7]

3.3.2 Mathematical Expression:

to draft a linear relationship between Vxy and Ix , the matching condition is

$$U_p \cdot W_p/L_p \cong U_n \cdot W_n/L_n[7] \tag{3.1}$$

The trans resistance at X-port is approximated as

$$V_X \cong V_Y + \frac{i_x}{\sqrt{2I_0C_{ox}}\left(\sqrt{\frac{\mu_p W_p}{L_p}} + \sqrt{\frac{\mu_n W_n}{L_n}}\right)} \quad [7]$$

$$R_x \cong \frac{1}{\sqrt{2I_0C_{ox}}\left(\sqrt{\frac{\mu_p W_p}{L_p}} + \sqrt{\frac{\mu_n W_n}{L_n}}\right)} \quad [7]$$

3.4 Specification:

Translinear structure's characteristics(90nm technology)	
Data	**Simulated Value**
Voltage supply	**± 1.8V**
Power consumption	**296.4198Uwatts**
Dynamic Range	**-0.2V,0.4V**
Voltage Gain	**0.95**
Current Gain	**1.16**
Biasing Current(I0)	**50μA**
(W/L) for NMOS	**W=0.16u,L=0.1u**
(W/L) for PMOS	**W=0.57u,L=0.2u**

Table 3.1: Specification of translinear structure

3.5 Simulation Results:

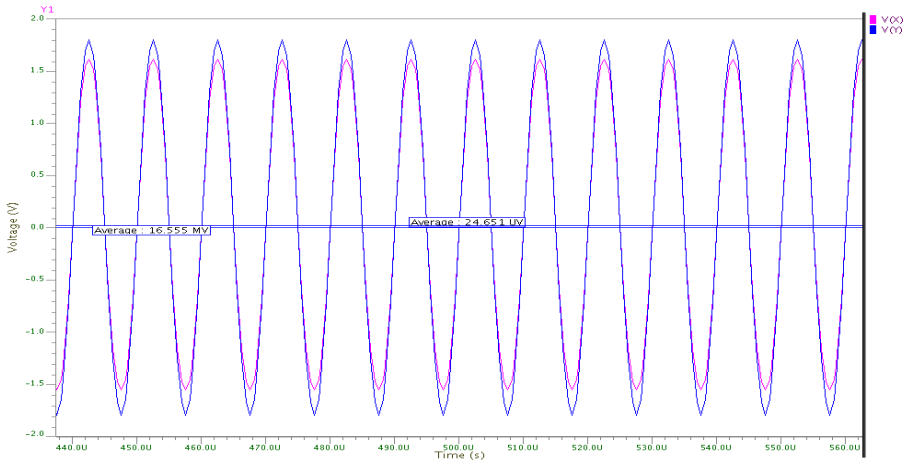


Figure 3.8: Transient response of voltages at node X,Y in 90nm CMOS technology

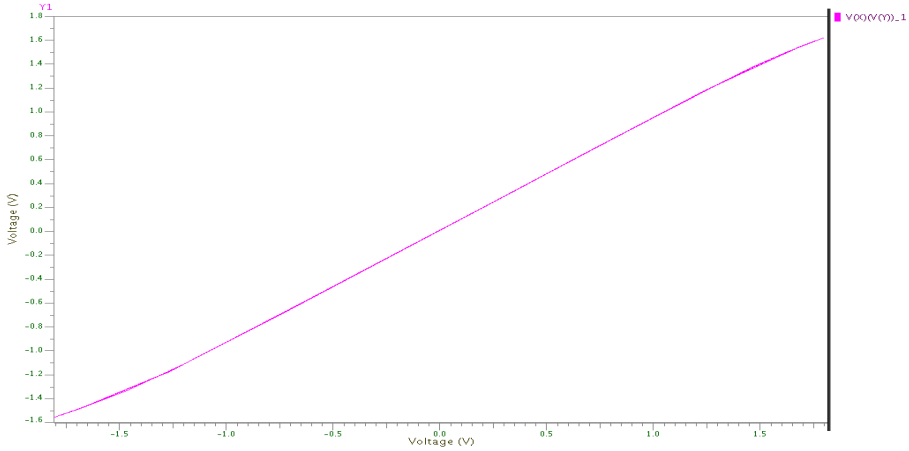


Figure 3.9: voltage tranfer characteristic of nodes X,Y in 90nm CMOS technology

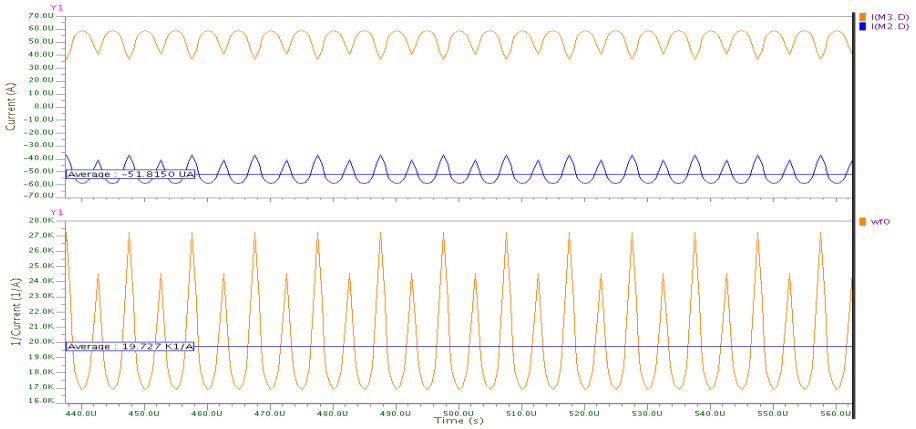
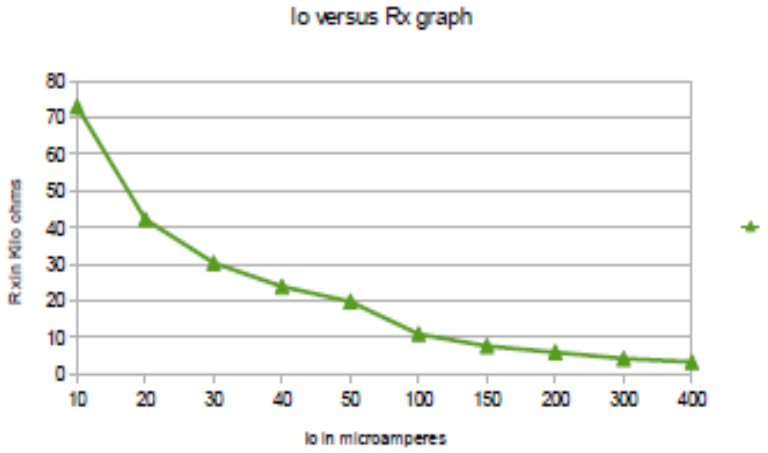


Figure 3.10: Transient response of currents at nodeX,Y and transimpedance for node X in 90nm CMOS technology

3.5.1 Observation:

I0 in μAmp	**Rx in KΩ**
10	**72.97**
20	**42.17**
30	**30.27**
40	**23.81**
50	**19.72**
100	**10.84**
150	**7.57**
200	**5.86**
300	**4.11**
400	**3.22**

3.5.2 Io versus Rx Graph:



3.6 Translinear based CCCII:

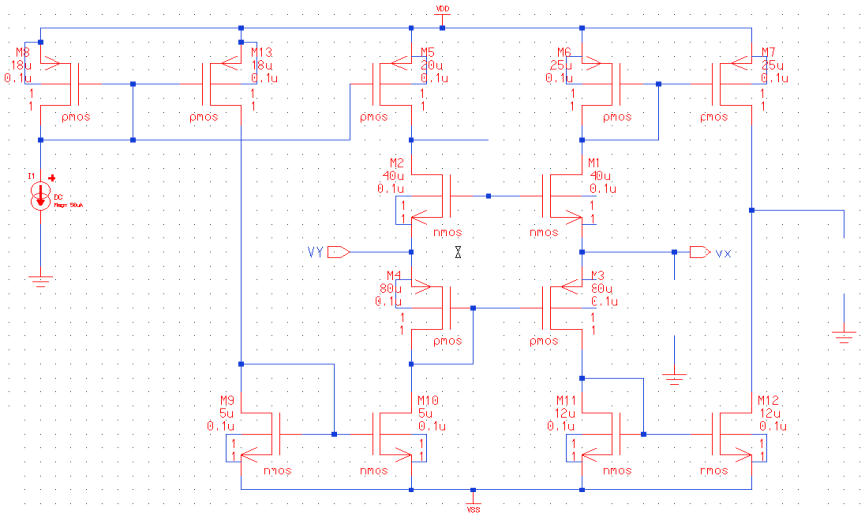


Figure 3.11: Schematic of translinear based structure of CCCII

3.7 Specification:

CCCII structure's characteristics(90nm technology)	
Data	**Simulated Value**
Voltage supply	**± 1.8V**
Power consumption	**30.6970M WATTS**
Dynamic Range	**-0.3V,0V**
Voltage Gain	**0.87**
Current Gain	**0.97**
Biasing Current(I0)	**50μA**
-3 dB frequency	**57Mhz**
Rx in KΩ	**1.30KΩ**
Rz in KΩ	**968.66Ω**

Table 3.2: Specification of CCCII structure

3.7.1 Simulation Waveforms:

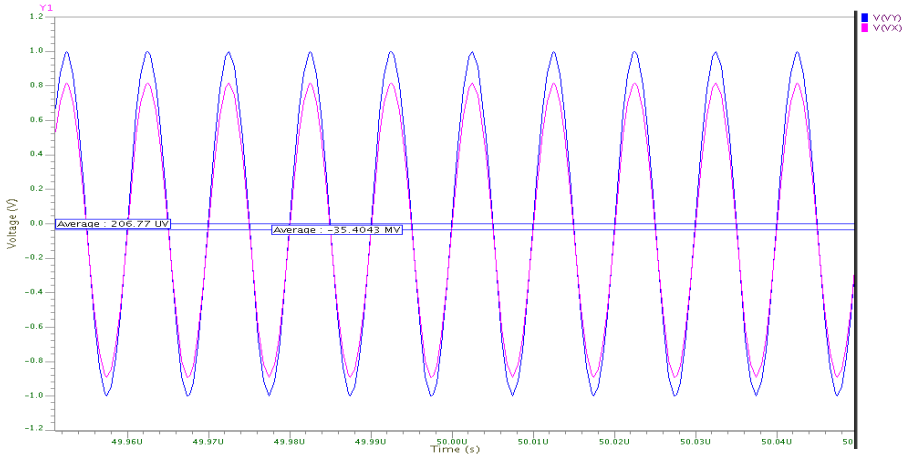


Figure 3.12: Transient response of voltages at node X and Y for 90nm CMOS technology

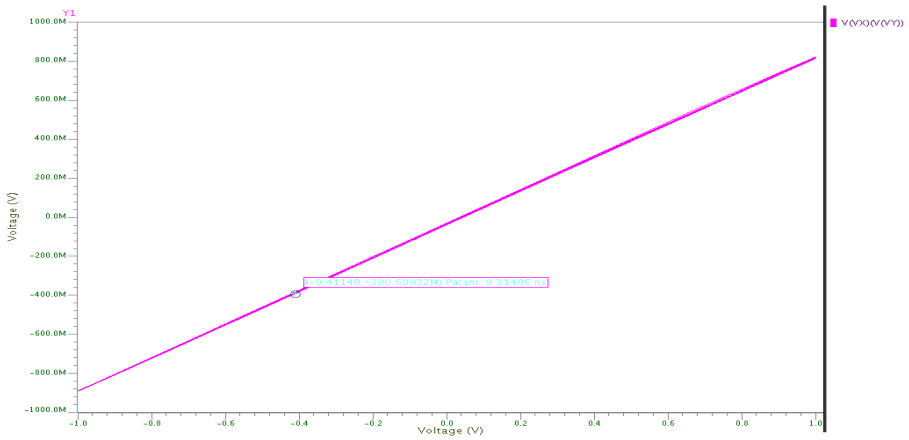


Figure 3.13: Voltage transfer characteristic for CCCII in 90nm CMOS technology

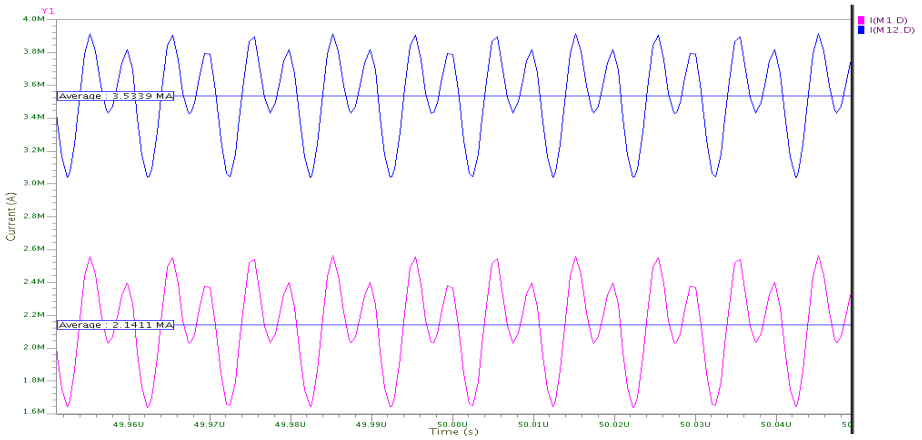


Figure 3.14: Transient response of currents for node X,Z for CCCII in 90nm CMOS technology

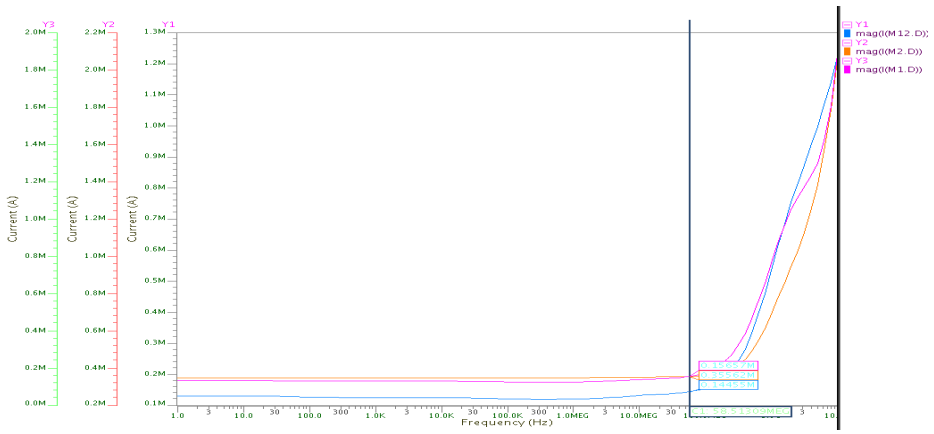


Figure 3.15: AC response of currents at node X,Y and Z for CCCII in 90nm CMOS technology

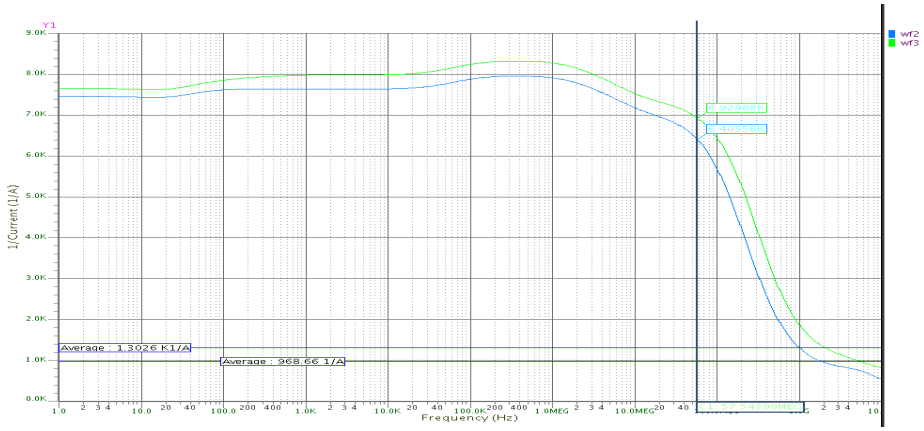


Figure 3.16: Frequency response of transresistance at node X and Z for CCCII in 90nm CMOS technology

Chapter 4

Third Generation Current Conveyor

4.1 Introduction

CCIII is schematically represented by the following figure:

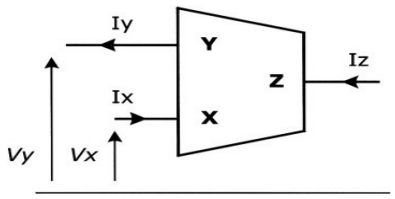


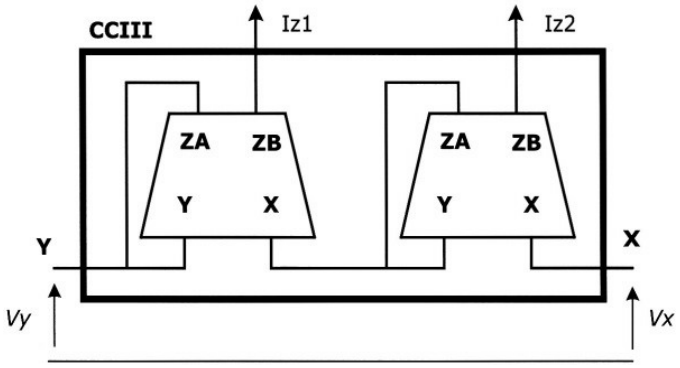
Figure 4.1: Block representation of CCIII

Matrix representation and block representation is shown below:

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{bmatrix} \begin{bmatrix} Vy \\ Ix \\ Vz \end{bmatrix}$$

In the above matrix,a is negative for CCIII and b is positive for (CCIII+) and negative for (CCIII-)[12].

CCII based CCIII representation[12]:



4.2 Schematic of CCIII(+):

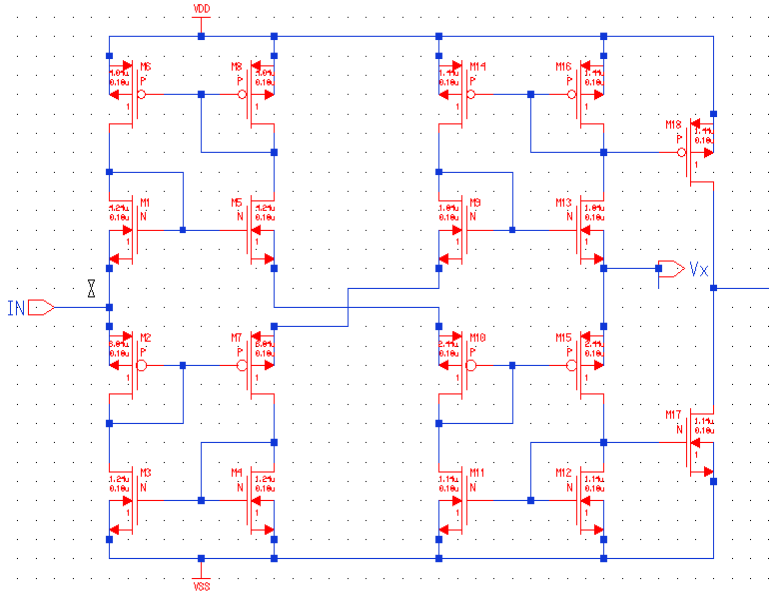


Figure 4.2: Schematic of CCIII(+)[13]

4.3 Aspect ratio of transistors

Transistor	W(in μm)	L(in μm)
M2,M7	6.84	0.35
M1,M5	4.24	0.35
M3,M4	1.24	0.35
M6,M8	4.04	0.35
M10,M15	2.50	0.35
M11,M12	1.20	0.35
M9,M13	1.40	0.35
M14,M16,M18	1.44	0.35
M17	1.14	0.35

Table 4.1: (W/L) ratios of CCIII

4.4 Specification

CCIII structure's characteristics(180nm technology)	
Data	Simulated Value
Voltage supply	$\pm$ 1.8V
DC bias current	5 μA
Dynamic swing Vx-Vy	-1.14V to 1.14V
Dynamic swing Iz+-Ix	-0.39mA to 0.93mA
Vx/Vy accuracy(voltage gain)	0.95
Current Gain(Iz+/Ix)	1.05
Current Gain(Ix-Iy)	0.95
Vx/Vy f-3db	1.24Ghz
Iz+/Ix f-3db	80.65Mhz
Output resistance(Rx)	26.988KΩ
Output resistance(Rz)	25.68KΩ
Power dissipation	256.64μwatt

Table 4.2: Specification of CCIII structure

4.5 Simulation Results:

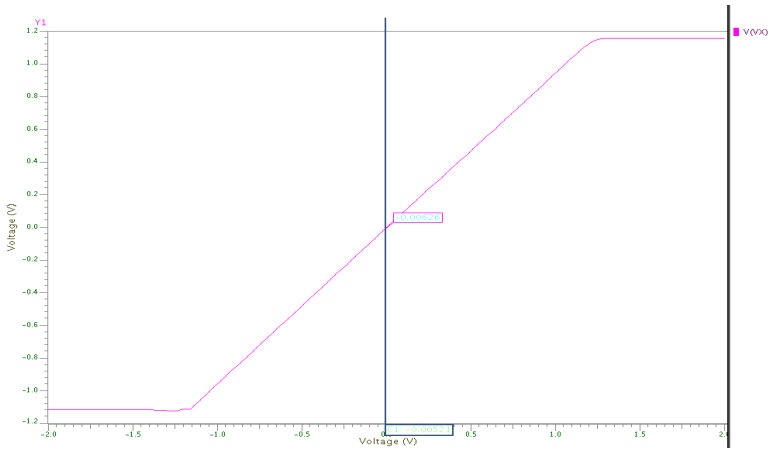


Figure 4.3: DC transfer characteristic of Vx versus Vy

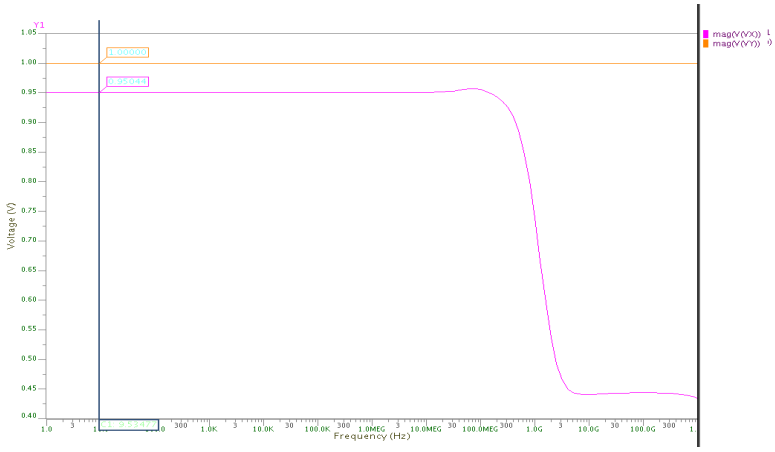


Figure 4.4: DC transfer characteristic of Iy,Ix and Iz+

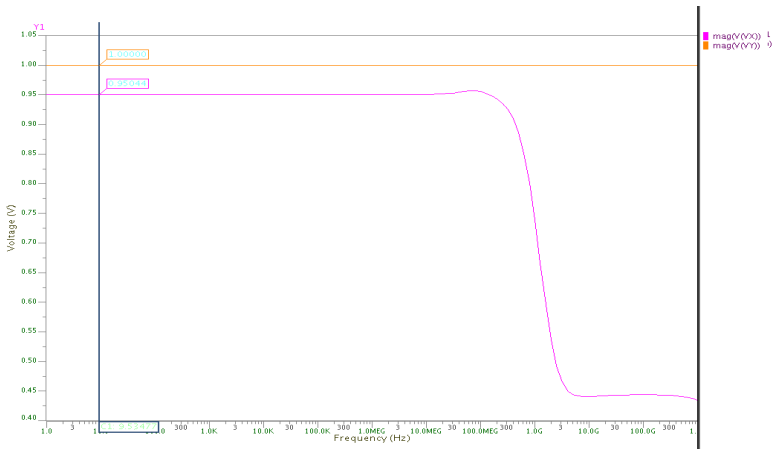


Figure 4.5: AC response of voltages Vx,Vy

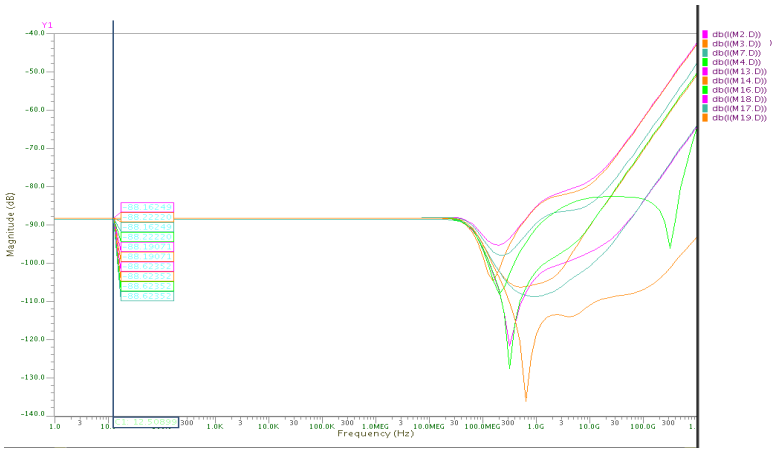


Figure 4.6: AC response of currents Ix,Iy,Iz+

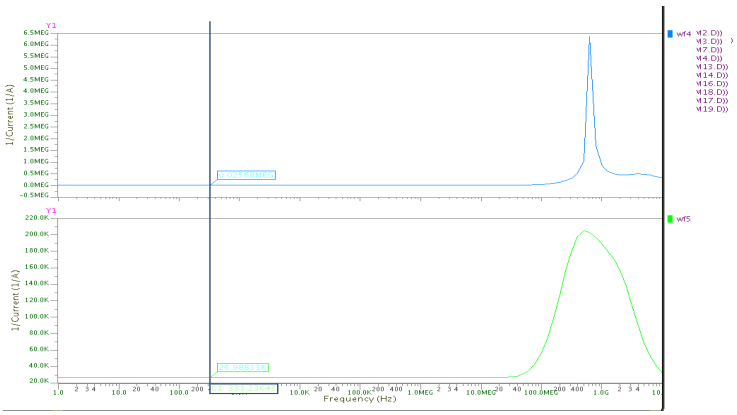


Figure 4.7: AC response of output resistance Rx,Rz

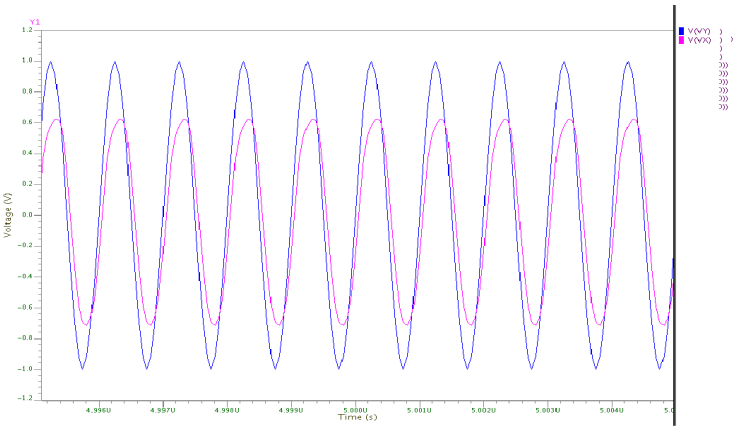


Figure 4.8: Transient analysis of Vx,Vy

4.6 Layout of CCIII

This layout is simulated using IC station of mentor graphics.

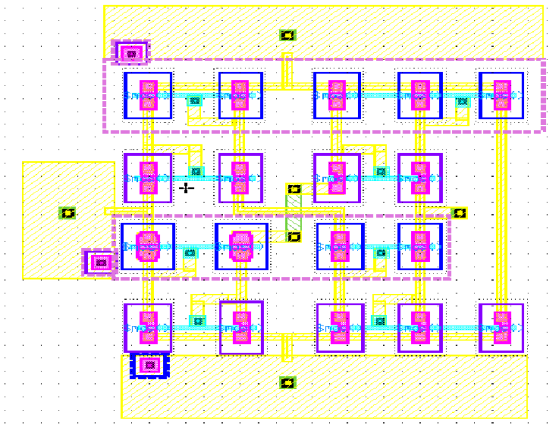


Figure 4.9: Layout of third generation current conveyor

4.7 DRC analysis of CCIII

DRC analysis of third generation current conveyor is carried out using IC station of mentor graphics in 180nm technology.

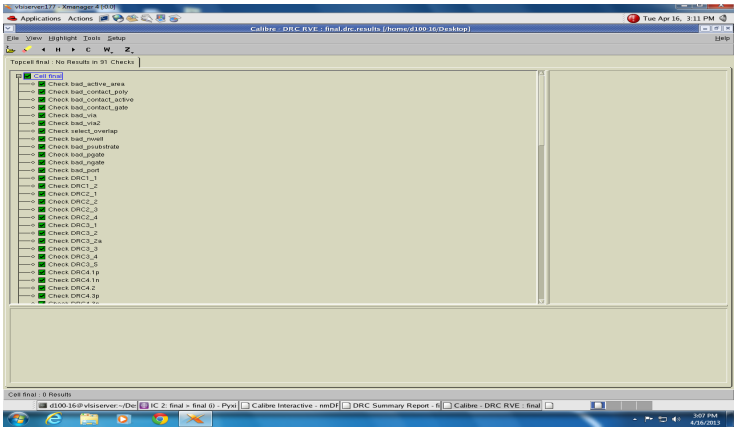


Figure 4.10: DRC report of CCIII

4.8 LVS analysis of CCIII

layout versus schematic analysis is also carried out using IC station of mentor graphics.

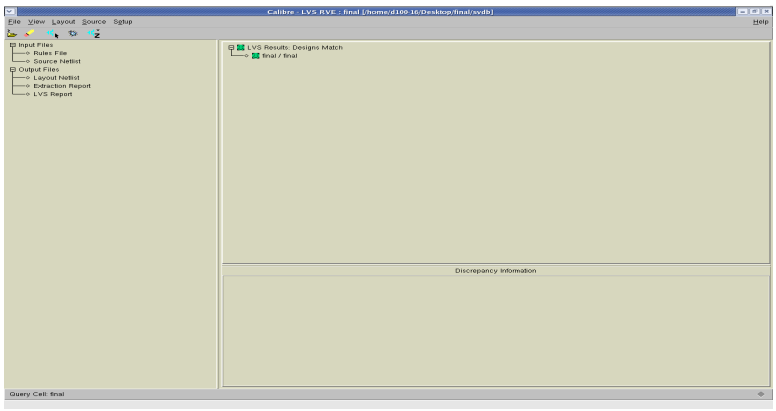


Figure 4.11: LVS report of CCIII

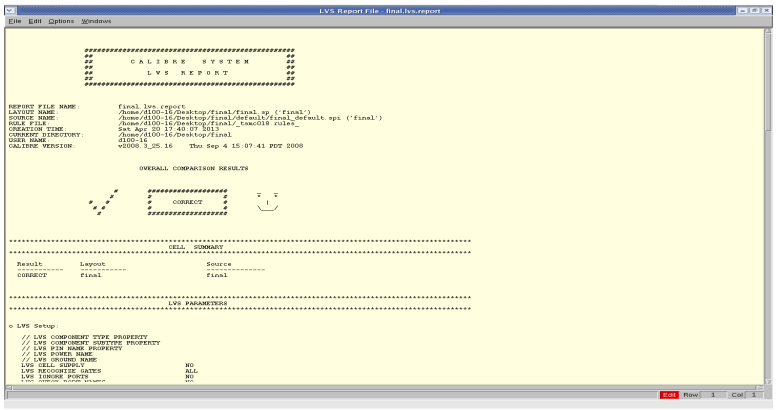


Figure 4.12: LVS report of CCIII

4.9 PEX analysis of CCIII

PEX analysis is done using IC station of mentor graphics.

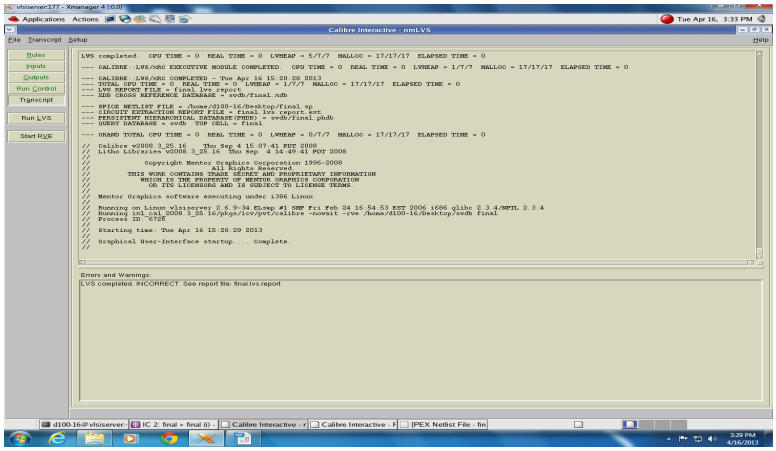


Figure 4.13: PEX report of CCIII

4.10 Comparison analysis of pre layout and post layout results

Parameter	Pre layout results	Post layout results
CMOS technology	0.18 μm	0.18 μm
Voltage supply	$\pm$1.8V	$\pm$1.8V
DC bias current	5μA	5μA
Dynamic swing Vx-Vy	-1.14V to 1.14V	-1.14V to 1.14V
Dynamic swing Iz+-Ix	0.93mA to -0.39mA	0.93mA to -0.39mA
Vx/Vy accuracy	0.95	0.95
Iz+/Ix accuracy	1.05	1.05
Ix/Iy accuracy	0.95	0.95
Vx/Vy f-3db	1.24Ghz	1.22Ghz
Iz+/Ix f-3db	80.65Mhz	77.81Mhz
output resistance(Rx)	26.988KΩ	26.988KΩ
output resistance(Rz)	25.68KΩ	26.988KΩ
Power dissipation	256.64μwatt	256.67Kμwatt

Table 4.3: Comparison table of pre and post layout of CCIII

To conclude pre layout and post layout results which show 3.67% variation between functions.

Chapter 5

Applications of CCIII

5.1 CCIII as a current sensor

The third generation current conveyors (CCIIIs) can he considered as a current controlled current source with a unity gain[17].It will be very useful to take out the current flowing through a floating branch of a circuit[3]. The third-generation current conveyor (CCIII) as a result of its IY=-IX and virtual short circuit between X and Y input ports characteristics, is very suitable especially for the current sensing application. It may also be advantageously used as the input cell of probes and current measuring devices[3].

CCIII as a current sensor:

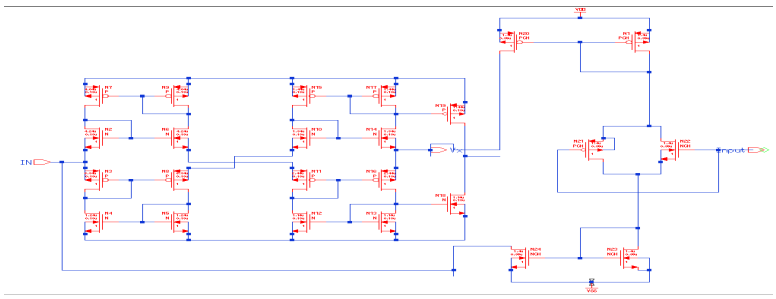


Figure 5.1: Schematic of CCIII as a current sensor

In the above circuit,input signal is applied to input terminal,transmission gate structure is transfer its equivalent current to the current mirror, CMs connected to X and Y terminals of third generation current conveyor. Therefore,final output is mirrored in to the Z terminal of CCIII. Therefore,above circuit is used to measure current flowing in to the signal.

5.2 CCIII as a current integrator

Here figure5.2 represent current conveyor schematic and its CMOS implementation is represented by fig.5.3. Its expression of the output current is easily evaluated considering the ideal CCIII characteristics,as follows:

Iout=Iz=Ix=Vx/R=Vy/R=Iin/sCR[12]

CCIII is applicable in current mode as well as voltage mode operations[14].

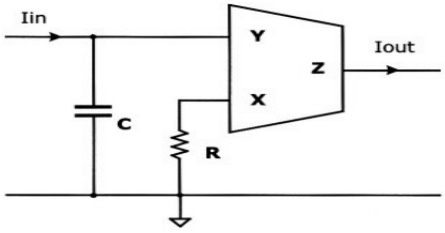


Figure 5.2: Block diagram representation of current integrator[12]

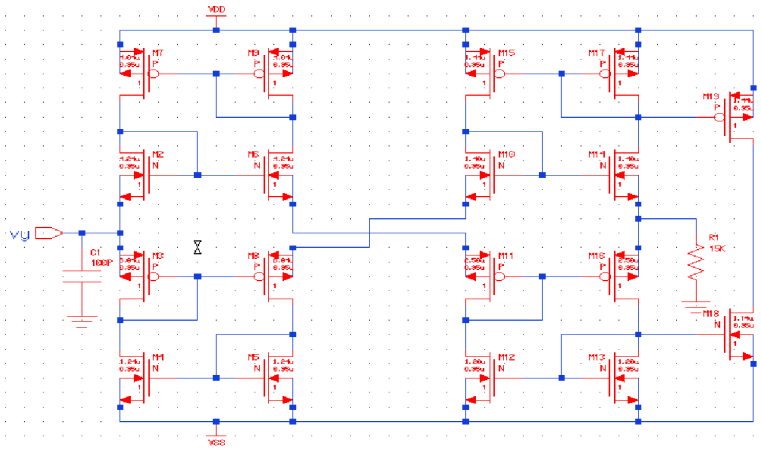


Figure 5.3: Schematic of Integrator

5.2.1 Simulation results of integrator

Fig.5.4 shows Transient response of current integrator for T >>RC,in which R=15K,C=100PF,input pulse period=1e-6 and pulse width=5e-7.In this waveform,output follows the input signal. Fig.5.5 shows transient response for RC >>T,in which input sine wave frequency is 1 Ghz ,2Vp-p amplitude. In this,output voltage is reduced and it is phase shifted. Fig.5.6 shows AC response of integrator. It has f-3db frequency is 858.59Mhz.

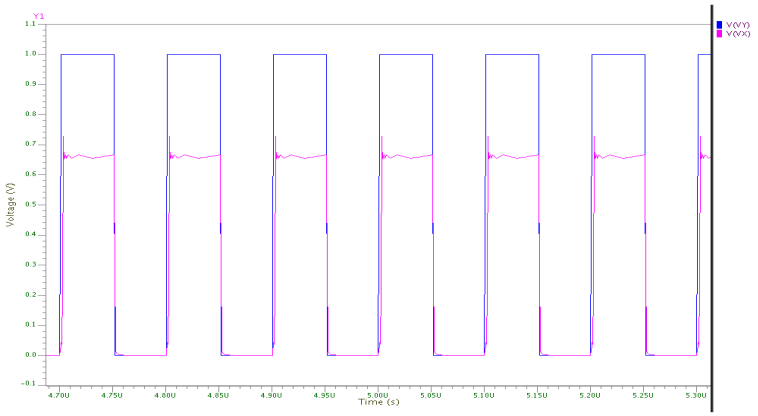


Figure 5.4: Transient response of integrator(T >>RC)

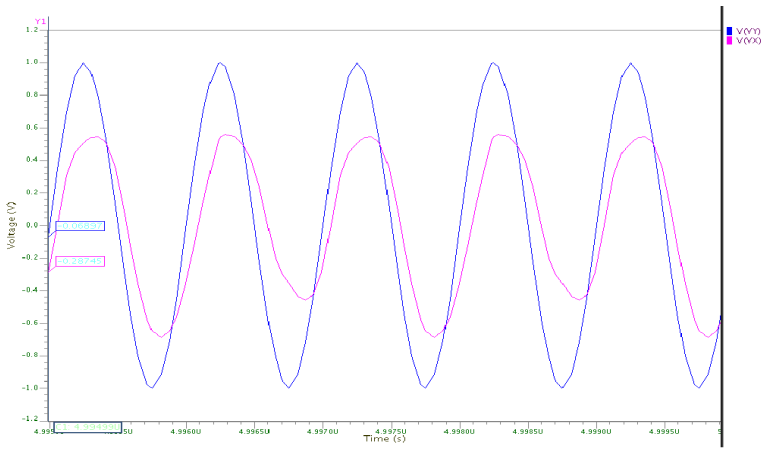


Figure 5.5: Transient response of integrator(RC >>T)

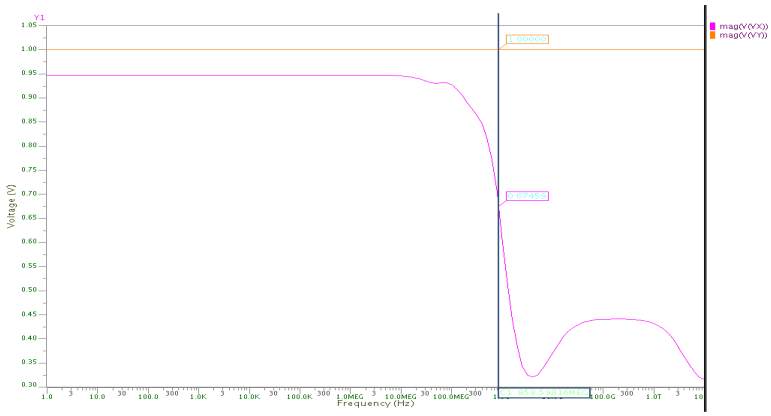


Figure 5.6: AC response of current integrator

5.3 CCIII as a voltage differentiator

Fig.5.7 represent voltage differentiator block diagram and its CMOS implementation is presented in fig.5.8 .The output voltage expression confirms that the circuit behaves as required.

Vout=Vx2=Vy2=RIz1=RIx1=sRCVx1=sRCVy1=sRCVin[12]

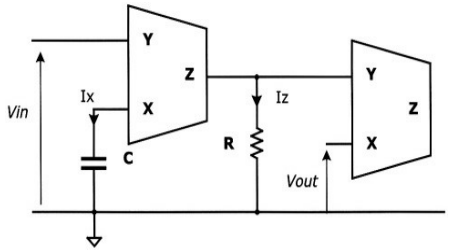


Figure 5.7: Block diagram of voltage differentiator

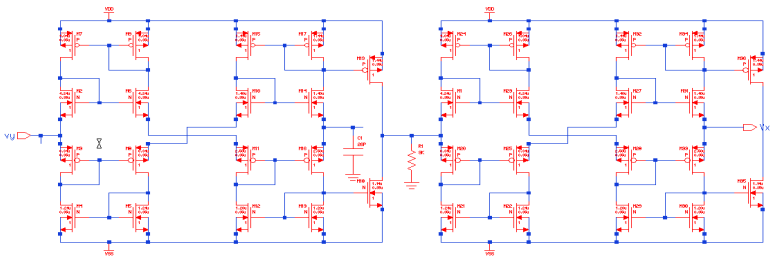


Figure 5.8: CMOS implementation of voltage differentiator

5.3.1 Simulation results of voltage differentiator

Fig. shows transient response of voltage differentiator for T >>RC ,in which R=9K,C=26PF,T=1e-06 and pulse width=5e-07.In this ,output voltage is charged and discharged rapidly.

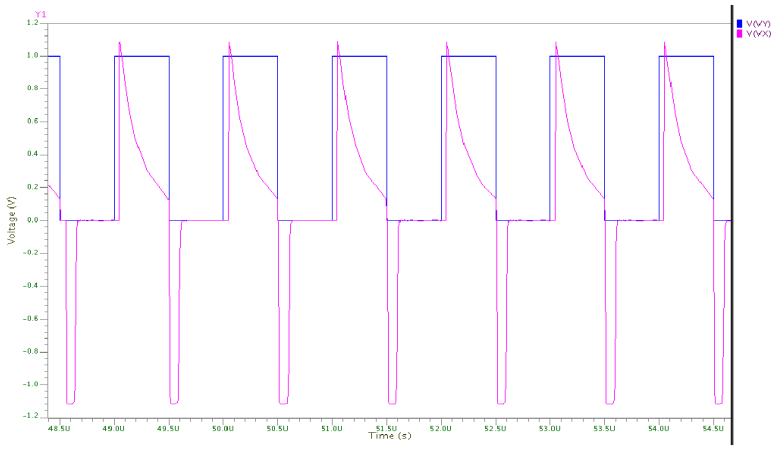


Figure 5.9: Transient response of differentiator(T >>RC)

Chapter 6

Conclusion and Future Scope

6.1 Conclusion:

In this project,basic topologies of CCI,CCII and CCIII is designed and simulated. For CCI,results shows that voltage gain is not unity. To obtain unity voltage gain, (W/L) ratios of transistors should be changed. Trans linear based current controlled conveyor-II is designed and simulated. for trans linear based structure we are getting satisfactory results of voltage and current gains. Trans impedance of trans linear structure is measured with different biasing currents. Low voltage CCIII is designed and simulated. For$\pm$0.75V power supplies,we are not getting satisfactory results for CCIII.Therefore,here $\pm$1.8V power supply is applied.CCIII is simulated and analyzed for pre layout and post layout design.It has good gain and high bandwidth.It uses low voltage ans consumes low power.Here,current gain will be improved by increasing output resistance at X and Z terminals.Voltage gain will be improved by using modified topologies.Its application as current sensor is designed.by doing improvement on the design of integrator and differentiator ,current mode filters will be designed.By analyzing results,it is assured that current mode circuits give better performance in low voltage low power applications as compared with voltage mode circuits.

6.2 Future Scope:

In future,applications of CCIII as current mode low pass filter and high pass filter will be achieved by improving on the design of integrator and differentiator.Modified topologies will be designed to achieve applications such as various multifunction filters,inductance simulation and all pass section.

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APPENDIX 1- TSMC 0.18um TSMC Data Shee

```
 T44E SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jul  8/04
* LOT: T44E                  WAF: 6009
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3694291
+K1      = 0.5887715      K2      = 3.059696E-3    K3      = 1E-3
+K3B     = 4.5379416      W0      = 1E-7           NLX     = 1.859182E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 1.3484262      DVT1    = 0.3669657      DVT2    = 0.0321807
+U0      = 262.597552     UA      = -1.45346E-9    UB      = 2.388329E-18
+UC      = 6.065042E-11   VSAT    = 1.049851E5     A0      = 1.8958229
+AGS     = 0.4217527      B0      = 1.405467E-7    B1      = 5E-6
+KETA    = -5.710529E-3   A1      = 3.800448E-4    A2      = 0.8605984
+RDSW    = 114.1849719    PRWG    = 0.5            PRWB    = -0.2
+WR      = 1              WINT    = 0              LINT    = 1.38756E-8
+XL      = 0              XW      = -1E-8          DWG     = -1.403515E-8
+DWB     = 1.403585E-8    VOFF    = -0.0923188     NFACTOR = 2.3339618
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.976763E-3    ETAB    = 9.401588E-6
+DSUB    = 0.0147417      PCLM    = 0.7500199      PDIBLC1 = 0.1481831
+PDIBLC2 = 2.164741E-3    PDIBLCB = -0.1           DROUT   = 0.6836492
+PSCBE1  = 4.02605E10     PSCBE2  = 2.319101E-9    PVAG    = 9.51717E-3
+DELTA   = 0.01           RSH     = 6.6            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 8.88E-10       CGSO    = 8.88E-10       CGBO    = 1E-12
+CJ      = 9.738002E-4    PB      = 0.8            MJ      = 0.3806198
+CJSW    = 2.656147E-10   PBSW    = 0.8007021      MJSW    = 0.1397059
+CJSWG   = 3.3E-10        PBSWG   = 0.8007021      MJSWG   = 0.1397059
+CF      = 0              PVTH0   = -1.627734E-4   PRDSW   = -1.9138777
+PK2     = 9.037624E-5    WKETA   = 3.850841E-3    LKETA   = -5.396657E-3
+PU0     = 8.1162291      PUA     = 1.139148E-11   PUB     = 0
+PVSAT   = 1.247309E3     PETA0   = 1.003159E-4    PKETA   = 3.393907E-3     )
```

Figure 6.1: NMOS Model Parameter of 0.18um Technology

```
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27               TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17        VTH0    = -0.3944719
+K1      = 0.5828995    K2      = 0.0266823        K3      = 0
+K3B     = 14.3383713   W0      = 1E-6             NLX     = 1.373459E-7
+DVT0W   = 0            DVT1W   = 0                DVT2W   = 0
+DVT0    = 0.6336613    DVT1    = 0.2409053        DVT2    = 0.1
+U0      = 112.690631   UA      = 1.417849E-9      UB      = 1.12483E-21
+UC      = -1E-10       VSAT    = 1.850699E5       A0      = 1.7532818
+AGS     = 0.375203     B0      = 3.569636E-7      B1      = 1.12458E-6
+KETA    = 0.0205518    A1      = 0.4474986        A2      = 0.3631955
+RDSW    = 243.82298    PRWG    = 0.5              PRWB    = 0.5
+WR      = 1            WINT    = 0                LINT    = 2.551606E-8
+XL      = 0            XW      = -1E-8            DWG     = -4.374325E-8
+DWB     = 2.595671E-10 VOFF    = -0.0937437       NFACTOR = 2
+CIT     = 0            CDSC    = 2.4E-4           CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.1136843        ETAB    = -0.0748821
+DSUB    = 1.0613195    PCLM    = 2.4303317        PDIBLC1 = 7.845168E-4
+PDIBLC2 = 0.0239307    PDIBLCB = -1E-3            DROUT   = 0
+PSCBE1  = 3.207414E9   PSCBE2  = 9.282296E-10     PVAG    = 15
+DELTA   = 0.01         RSH     = 7.5              MOBMOD  = 1
+PRT     = 0            UTE     = -1.5             KT1     = -0.11
+KT1L    = 0            KT2     = 0.022            UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11         AT      = 3.3E4
+WL      = 0            WLN     = 1                WW      = 0
+WWN     = 1            WWL     = 0                LL      = 0
+LLN     = 1            LW      = 0                LWN     = 1
+LWL     = 0            CAPMOD  = 2                XPART   = 0.5
+CGDO    = 6.34E-10     CGSO    = 6.34E-10         CGBO    = 1E-12
+CJ      = 1.148543E-3  PB      = 0.8476511        MJ      = 0.4067434
+CJSW    = 2.382898E-10 PBSW    = 0.8222976        MJSW    = 0.3300124
+CJSWG   = 4.22E-10     PBSWG   = 0.8222976        MJSWG   = 0.3300124
+CF      = 0            PVTH0   = 3.507137E-3      PRDSW   = 17.811338
+PK2     = 3.610481E-3  WKETA   = 0.0334716        LKETA   = -3.202602E-3
+PU0     = -2.0541594   PUA     = -8.93082E-11     PUB     = 1E-21
+PVSAT   = -50          PETA0   = 1.003159E-4      PKETA   = -1.696047E-3
*
```

Figure 6.2: PMOS Model Parameter of 0.18um Technology