4096 PIXEL LINEAR CCD VISIBLE IMAGER
and
DEVELOPMENT OF SWITCHED CAPACITOR AMPLIFIER FOR ROIC

A Major Project Report

This is submitted in Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY
IN
ELECTRONICS & COMMUNICATION ENGINEERING
(VLSI Design)

By

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Certificate

This is to certify that the Major Project Report entitled **"4096 Pixels linear CCD Visible Imager *and* Development of Switched Capacitor Amplifier for ROIC"** Submitted by **Mr. G. Venkata Penchala Reddy (03MEC05)** towards the partial fulfillment of the requirements for the award of Degree of **Master of Technology** in Electronics & Communication Engineering **(VLSI Design)** of Nirma University of Science and Technology is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma

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G. Venkata Penchala Reddy

ABSTRACT

This REPORT is basically divided into two parts.

The first part is about **4096 pixels linear CCD visible imager.** This part contains introduction to imaging systems. Electronic imaging systems based on solid-state image sensors have received tremendous attention in the past few years. The many advantages of the sold-state image sensors have opened up a wide variety of new imaging possibilities applications, ranging from high resolution, space borne electronic camera to PC peripheral camera, were costly, if not possible, using earlier technology.

This part will explains the basic theory of CCD, CDS, pre-amplifier, ADC, design of architecture that converts the four shift registers pixel output data of CCD into single line of data using VHDL and lastly interfacing of FPGA output to PC using serial port (RS232).

The second part is about **Development of Switched Capacitor Amplifier for an ROIC.** This is about analysis and design of *op-amp* & thereafter offset compensated *Switched Capacitor (SC) amplifier* which is one of the functionality needed in development of Readout Integrated Circuit (ROIC). The implementation of active pixel based image sensors in CMOS technology is becoming increasingly important for producing imaging systems that can be manufactured with low cost, low power, simple interface, and with good image quality. The major obstacle in the design of CMOS imagers is Fixed Pattern Noise (FPN) and Signal-to-Noise-Ratio (SNR) of the video output.

This part will explains the basic introduction to CMOS sensor, description about block diagram of Read Out Integrated Circuit (ROIC), integration and operating modes of ROIC. This part also contains ***buffer design*** with load of 10PF using two stage operational amplifier and ***Autozeroing (offset compensation)*** Technique implementation using ***non-inverting*** and ***inverting*** Switched Capacitor voltage amplifier circuits. The use of offset compensated switched capacitor amplifier removes the effect of unpredictable offset, which develop in amplifier after fabrication.

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NOMENCLATURE

CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
VMC	Visual Monitoring Camera
HDTV	High Definition TV
IC	Integrated Circuit
ADC	Analog to Digital Converter
Pre-Amp	Pre Amplifier
CTE	Charge Transfer Efficiency
SCCD	Surface Channel CCD
BCCD	Buried Channel CCD
QE	Quantum Efficiency
CDS	Correlative Double Sampling
SIPO	Serial In Parallel Out register
PISO	Parallel In Serial Out register
MUX	Multiplexer
DPRAM	Dual Port Random Access Memory
VHDL	Very High Speed Integrated Circuit Hardware Description Language
FPGA	Field Programmable Gate Array
SPP	Standard Parallel Port
UART	Universal Asynchronous Receiver and Transmitter
DTE	Data Transmission Equipment
DCE	Data Transmission Equipment
EIA	Electronic Industry Association
TD	Transmit Data
RD	Receive Data
CTS	Clear To Send
DCD	Data Carrier Detect
DSR	Data Set Ready
DTR	Data Terminal Ready
RTS	Request To Send
RI	Ring Indicator
SG	Signal Ground

KBPS	Kilo Bits Per Second
IRQ	Interrupt Request
COMM	Communication port
DLAB	Divisor Latch Access Bit
IER	Interrupt Enable Register
IIR	Interrupt Identification Register
FIFO	First In First Out
FCR	First In/First Out Control Register
LCR	Linear Control Register
MCR	Modem Control Register
LSR	Linear Status Register
MSR	Modem Status Register
IEEE	Institute of Electrical and Electronics Engineers
VLSI	Very Large Scale Integration
ROIC	Read Out Integrated Circuit
QWIP	Quantum Well Infrared Photo Detector
FPN	Fixed Pattern Noise
DSP	Digital Signal Processing
ASIC	Application Specific Integrated Circuit
CTIA	Capacitive Trans impedance Amplifier
CMI	Current Mirroring Integration
DI	Direct Injection
ITR	Integrate then Read Mode
IWR	Integrate while Read Mode
op-amp	Operational Amplifier
GBW	Gain Bandwidth
PM	Phase Margin
GM	Gain Margin
PSRR Power	Supply Rejection Ratio
SR	Slew Rate
CMRR	Common Mode Rejection Ratio
AZ	Auto zeroing
CHS	Chopper Stabilization
SC	Switched Capacitor

CONTENTS

PART-II

Development of Switched Capacitor Amplifier for ROIC

ABOUT COMPANY

SEMICONDUCTOR COMPLEX LIMITED
SAS NAGAR, MOHALI
PUNJAB

History:

The Government of India recognized the importance of self sufficiency in microelectronics in 1971. In January 1972, the Department of Electronics constituted a semiconductor panel to study semiconductors in depth. This panel submitted its report in November 1972, with a strong recommendation for establishing a public sector enterprise for research and development. The project got final clearance in 1977. The government of Punjab came forward and allotted 50.8 acres of land for the project.

SCL was registered as company on 12 January, 1978. The plant was successfully commissioned on 2nd October, 1983 in the green unpolluted environment on the out strikes of Chandigarh – a city designed by the French Architect "Le Corbusier", just 250 kms, north-west of Indian Capital "New Delhi". With its objective to design, develop, and manufacture VLSI based products and to create strong R&D base, SCL entered into technical collaboration with American Microsystems Inc. USA and in 1984 commenced commercial production in 5 micron CMOS technology. Through intensive in house R&D efforts SCL developed and productionised the next generation 3 micron, 2 micron, 1.2 micron as well as EEPROM and CCD technology.

Today SCL is India's leading microelectronics endeavor into 21st century by making fully operational a six inch wafer facility. And to this, the plan is to upgrade as well as the capacity and one has the vision of an emerging player in the global microelectronics arena.

SCL's vertically integrated semiconductor operations offer design wafer fabrication, testing, VLSI based systems and applications support, all under one roof. With in this framework, SCL places a lot of emphasis on its semiconductor operations consistently building its specializations in areas like mixed signal devices, micropower technology, etc. This fulfils the demand of its customers in consumers and industrial electronics.

SCL has technical collaborations with following foreign companies:

MOS-LSI: American Micro System Inc., Japan

Digital Electronic Watch Module: Hitachi Ltd., Japan

Electronics Modules for Quartz Analog Watches: Citizen and Seiko, Japan

Electronics Module for Clocks: Rivanzle, Germany

Microprocessors 6502: Rockwell International, USA

PC: Acron Computers, U.K.

SCL as an Organization:-

Company Profile:

Incorporated in 1978 by Department of Electronics, Government of India.

Particulars:

Name	:	Semiconductor Complex Limited
Workplace	:	SAS Nagar, Punjab
Year of Incorporation	:	1972
Constitution	:	Public Sector Undertaking
Assets	:	More than 100 billion
Area Covered	:	26,000 sq. ft.
Air Conditioning	:	2600 tones of refrigeration
Electricity	:	8.5 MVA substation

Ultra cleaned rooms with temperature as humidity control and a water body with lots of fountains are maintained. The centralized air conditioning system.

The first indigenous LSI chip had been rolled out by 9 march 1984. By 16 Jan.1986 R&D Engg. Succeeded in developing 3 micron CMOS silicon technology indigenously. Many achievement and landmarks are being constantly added by the member if the SCL.

SCL Activities:

Sustaining business operation by keeping its customers fully satisfied by fulfilling commitment. A dedicated team of experienced professionals is undertaking these activities. Production work's being lead by engineers. A few area of production are as under:

- Fabrication of IC's
- Testing and assembly of IC's
- PCB assembly

SCL is having computerized LSI / VLSI facilities which have been established after its destruction in 1989 mishap. LSI / VLSI department had taken over the designing of

- 1.2 micron standard cells
- 3 micron standard cells
- Analog cell library
- 8 bit microcontroller
- 8bit micro gate array
- Tone pulse switchable dialer
- Signal processor

A research and development activity at SCL covers all the facts of LSI/VLSI technology including:

- Process development
- Device physics
- Modeling and design
- Development of CAD tools
- Reliability testing and failure analysis
- R&D working areas
- BIMOS technology
- Tech. For images
- .8 micron technology
- 1.2 standard cell library
- Microcontroller based ASIC capability

Products of SCL:

SCL offers products for following market segments:-

Telecommunications

Data Processing & Computation

Consumer Electronic Industrial & Process Control

Defense Aerospace

Health

Power

Banking

An Introduction to Various Departments in SCL:

SCL is divided into a number of departments in order to carry production process efficiently. The employees in the company work as the members of a well-knit family under the dynamic leadership of Mr. M.J.Zarabi (Director of SCL).

The various departments are:

- CMD Secretariat
- VLSI Departments:
- System Division:
- Information Technology
- Marketing
- Finance
- Material Management
- Facilities, Maintenance & Control
- Human Resource Development
- Quality Control
- Purchase

Chapter -1

INTRODUCTION

Due to the recent enormous improvement in solid state technology, especially in imaging sensor regime, it's helpful to update the knowledge base regarding this field for the scientific applications — in our case, Astrophysics, Solar Physics, space applications and imaging (scanner). Astronomy observation was always keeping up with the up-to-date technology in imaging technology due to it scientific research philosophy. Ever since the invention of Charge-Couple-Device (CCD), researchers developed numerous imaging systems based on this technology to substitute the old film imaging system. The obvious advantages of CCD over film are: convenience to use, rapid image capturing, digitalized data ready for computer analysis, extremely high spatial/temporal resolution, high sensitivity to principally whole spectrum, etc. There are many new discoveries were made through using CCD technology in the past decades.

For scientific applications, new features of solid state sensors are always in focus. Consequently, CMOS sensor as a newly improved technology draws more and more attentions in scientific research due to the new features it offers —random readout, low drive power, low noise level. Based on these new features, the frame rate can be increased dramatically and battery life endures much longer at the same time. The possible high temporal resolution shows great potential in research areas such as, speckle reconstruction. Furthermore, both low power and miniaturization of camera is also a critical advantage of CMOS pixel, for example, in the application of space borne cameras. There are already successful applications of CMOS pixel in space mission. XMM-Newton Spacecraft (ESA) carried Visual Monitoring Camera (VMC) with IRIS-1 color sensor, launched in 10th December, 1999, by Ariane 4. Also, CMOS APS found its usage in high energy particle detection (Lawrence Berkeley National Laboratory).

Let along the scientific research, the solid state image sensors can always be seen in social lives. CCD Cameras, Camcorder, HDTV, Cellular Phone, are everywhere in people's life. And CMOS sensor technology is under extensive development towards the applications in automotive industry and wireless industry. In this report, the author will explore the basic physics of both CCD pixel, and CMOS pixel with primary focus on the later technology. The fabrication process in semiconductor industry will also be enumerated in order to complete the picture of semiconductor material as mentioned in Physics-687. In spite of the

consideration regarding material, circuit structure design is also mentioned due to the fact that IC design plays the same important role in the final semiconductor products.

An overview of the global market of CCD/CMOS ICs market is also given at the end of the report to complete the discussion. Due to the fact that the application of solid-state image sensors are closely related to the basic principles of scientific research areas, it will be helpful to achieve certain background knowledge in solar physics in the next paragraph.

1.1 Solar Physics Background

In solar physics, one of the primary task is to explain the mechanism of the generation of solar energy and predict future solar activities. One of the important example is the prediction of solar wind, which is threatening the satellites, telecommunication network, power supply system on earth (blackout). Solar cycle describes the activity fluctuation on the Sun. By observing the luminosity of solar radiation, it's found that the solar irradiance (Wm-2) has variance in period of around 11 years. The peak of this variance is called solar maximum, when the number of sunspot reaches peak as well. The luminosity (total irradiance energy) of sun has relative variations of up to 0.2% over days; on the order of 10-6 over minutes. These variations show the energy exchange in solar. Solar Constant refers to the total irradiance at mean distance,

S = 1367 ± 3W/m2[3].

Solar magnetic field is a window to the understanding of the structure and undergoing activities of Sun. Therefore, measuring magnetic field on the Sun is the second final step the understand solar physics — the last step is to do prediction. Due to atomic physics, it's possible to build up relations between intensity of polarized sunlight at certain wavelength with solar magnetic field, which is the goal of observation. Zeeman Splitting is one of the most often used phenomena in solar observation. It builds up the link between spectrum line splitting and magnetic field.

$$\Delta\lambda_z = \frac{e}{4\pi m_e c^2}\lambda^2 gB = 18.52\left(\frac{\lambda}{6302^o A}\right)^2 g\frac{B}{kG}m^o A \qquad \text{---------- (1.1)}$$

Where, **g** is Land´e factor of atomic level,

M is quantum number of the level,

B is magnetic field strength.

Since FeI line at 6302.5°A is a simple triplet with Land´e factor equal to 2.5, it can be taken as a reference in the equation to eliminate physical constants.

Taken polarization of light into account, the intensity of weak (unsaturated) spectral line can be shown in equations as:

$$I_{RCP}(\lambda) = 0.125I(\lambda + \Delta\lambda_Z)(1-\cos\gamma)^2 + 0.25I(\lambda)\sin^2\gamma + 0.125I(\lambda - \Delta\lambda_Z)(1+\cos\gamma)^2$$

---------- (1.2)

$$I_{LCP}(\lambda) = 0.125I(\lambda + \Delta\lambda_Z)(1+\cos\gamma)^2 + 0.25I(\lambda)\sin^2\gamma + 0.125I(\lambda - \Delta\lambda_Z)(1-\cos\gamma)^2$$

---------- (1.3)

Where, **γ** is inclination angle (the angle between the magnetic field lines and line of sight). Consider the filling factor 1, the observed light intensity I_{RCP} can be expressed as:

$$I^*_{RCP} = f.I_{RCP} + 0.5(1-f)I_n$$ ---------- (1.4)

Where, $\mathbf{I_n}$ is nonmagnetic components in light observed. This is in fact the definition of the filling factor **f**. Therefore, it's natural to record the polarized light intensity with certain correction and image processing, so that the magnetic field information can be derived.

So as explained above mainly there are two types of imagers (CCD, CMOS). Selection of imager is depending on application and on following parameters.

1. Responsivity, the amount of signal the sensor delivers per unit of input optical energy.
2. Dynamic range, the ratio of a pixel's saturation level to its signal threshold.
3. Uniformity, the consistency of response for different pixels under identical illumination conditions.
4. Shuttering, the ability to start and stop exposure arbitrarily.
5. Speed
6. Windowing. One unique capability of CMOS technology is the ability to read out a portion of the image sensor. This allows elevated frame or line rates for small regions of inter
7. Antiblooming, the ability to gracefully drain localized overexposure without compromising the rest of the image in the sensor.
8. Biasing and clocking
9. Reliability

1.2 Feature and Performance Comparison

Feature	**CCD**	**CMOS**
Signal out of pixel	Electron packet	Voltage
Signal out of chip	Voltage (analog)	Bits (digital)
Signal out of camera	Bits (digital)	Bits (digital)
Fill factor	High	Moderate
Amplifier mismatch	N/A	Moderate
System Noise	Low	Moderate to High
System Complexity	High	Low
Sensor Complexity	Low	High
Camera components	PCB + multiple chips + lens	Chip + lens
Relative R&D cost	Depends on Application	Depends on Application
Relative system cost	Depends on Application	Depends on Application
Performance	**CCD**	**CMOS**
Responsivity	Moderate	Slightly better
Dynamic Range	High	Moderate
Uniformity	High	Low to Moderate
Uniform Shuttering	Fast, common	Poor
Uniformity	High	Low to Moderate
Speed	Moderate to High	Higher
Windowing	Limited	Extensive
Antiblooming	High to none	High
Biasing and Clocking	Multiple, higher voltage	Single, low-voltage

Chapter -2

BLOCK DIAGRAM OF BOARD

The block diagram of board to process output data of CCD is shown in **Figure2**

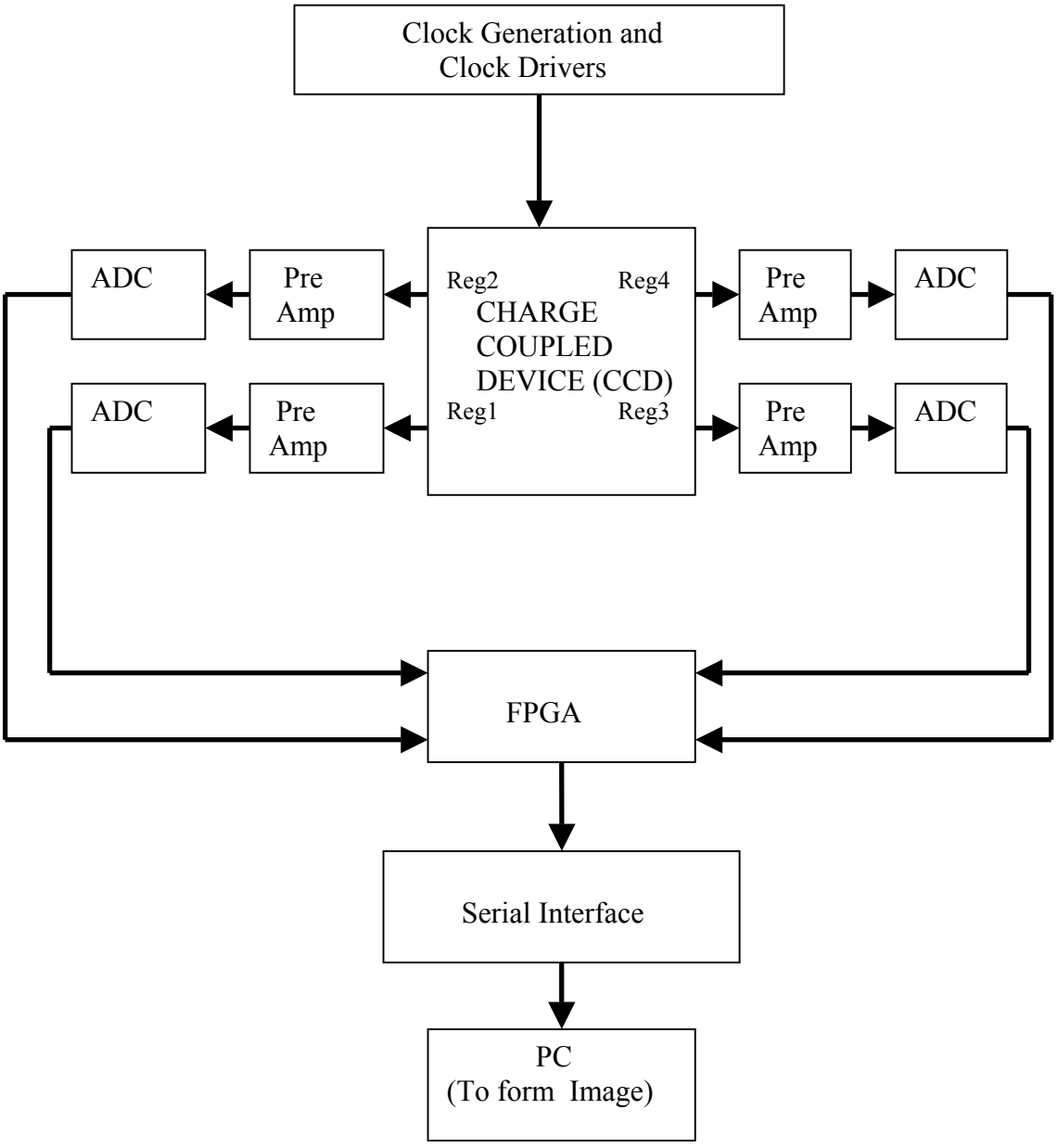


Figure 2: Block Diagram of Board

Pre Amp --- Pre Amplifier

ADC --- Analog to Digital Converter

FPGA --- Field Programmable Gate Array

PC --- Personal Computer

2.1 CHARGE COUPLED DEVICE (CCD)

2.1.1 CCD Pixel

Charge Coupled Device (CCD) belongs to a broader group of IC structure — Charge Transfer Device, which is one application of the MOS transistor. CCDwas invented by W.S. Boyle, G.E. Smith and G.G. Amelio, Bell Lab, 1970. By 1972, R.H. Walden, et. al., Bell Lab, devised Buried Channel CCD, which was Intended to solve poor Charge Transfer Efficiency (CTE) problem. Depending on the gate material, CCD can have

- Single Layered Metal Gate
- Single Layered Polysilicon Gate
- Multiple Layered Poly silicon Gate. Or

Based on wafer material doping type:

- p-type
- n-type (preferred type due to the higher mobility of electrons). Or

Based on channel depth:

- Surface Channel CCD (SCCD)
- Buried Channel CCD (BCCD). Or

Based on driving methods:

- 3,4,multi-Phase CCD;
- Pseudo 1,2-Phase CCD;
- Ripple Transfer;
- Accordion Transfer.

2.1.2 MOS Structure

CCD works based on Metal-Oxide-Semiconductor (MOS) structure. Due to the difference between work functions Φ_m and Φ_s, there will be a depletion region in which a potential well is built up. The depth of the well — threshold voltage is:

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F \qquad \text{---------- 2.1}$$

where $\phi_{ms} = \phi_m - \phi_s$, Q_i and C_i are interface charge and capacitance respectively.

Q_d is depletion charge; $\phi_F = E_i - E_{FS}$

In equilibrium, given work function difference $\phi_{ms} < 0$ as shown in **Figure2.1**.

The metal side is positively charged and semiconductor side is negatively charged. This extra electrical field compensates the work functions difference. Therefore, the bands bend down near surface of semiconductor in equilibrium. In order to bend it over, a bias voltage is needed, which corresponds to V_T.

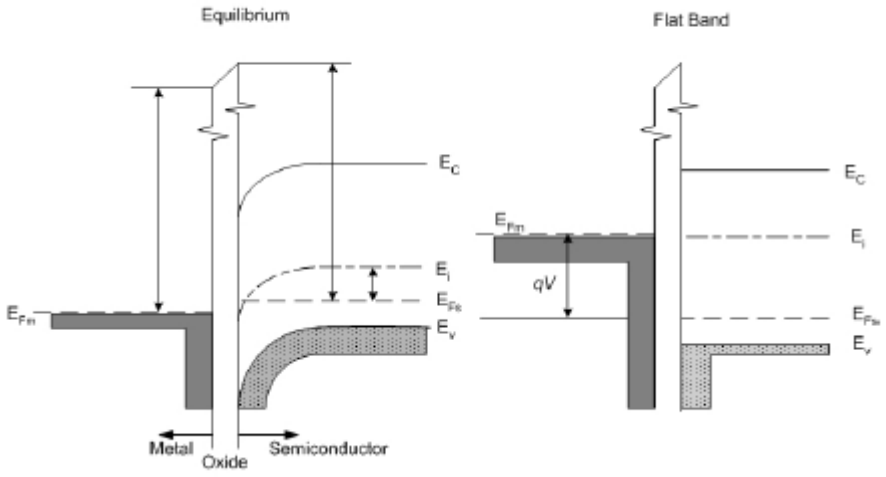


Figure 2.1: MOS Band Structure.

In flat band situation, $V=V_{FB}-Ø_{ms}$ This situation corresponds to the dispearance of potential well in depletion region, i.e., all collected charges will be "poured" out the well. Given n+ polysilicon gate, $Ø_{ms}$= -0.95V for Na = 1016, interface charge of 5 × 1010q · C/cm2, V_T can be calculated as: V_T = -0.14V.

This is an example of p-type semiconductor with n-channel. The basic principle of CCD is dynamic charge storage & withdrawal in CMOS capacitors array. Charges generated/injected electronically or by exposure to light can be stored in MOS capacitor temporarily. After collecting (integration), by clocking positive voltage on metal electrode of single MOS capacitor, it's possible to transfer charges collected in one MOS well to the next adjacent MOS well. The whole process can be put in analogy with fluid flow. **Figure2.2** shows a 3-Phase CCD image array. Due to the gap (related to "feature size" of semiconductor fabrication) between polysilicon electrodes in Fig.3.2, the charges transfer process turns out to be a big charge-losing process, i.e., low Charge Transfer efficiency (CTE). To solve this problem, Walden, et.al at Bell Lab designed Buried Channel CCD (BCCD) in 1972, ref **Figure2.3**.

The polysilicon electrodes are buried by SiO2, and Al is used to fill the gap between polysilicon electrodes. These additional electrodes create extra potential wells, which combined with the potential wells due to polysilicon, form a potential well of stair shape. In this way, in the process of charge transfer, charges occupy on or more steps of well-stair so that they won't move without constraints, i.e., charges are always hold in potential wells. By clocking the voltage on electrodes, charges are moved "smoothly" to the readout node.

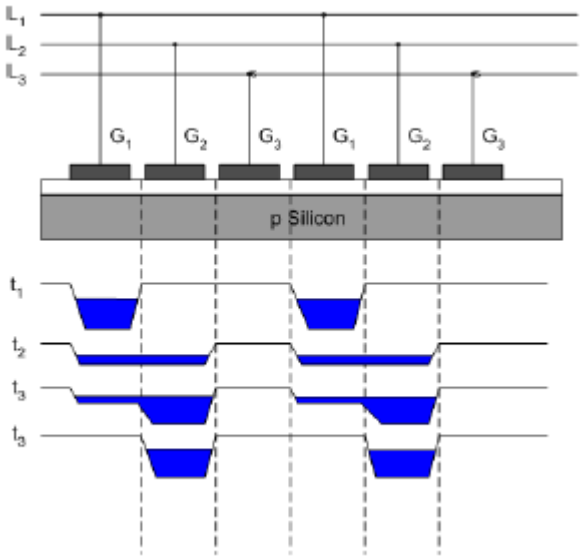


Figure 2.2: Basic CCD Structure

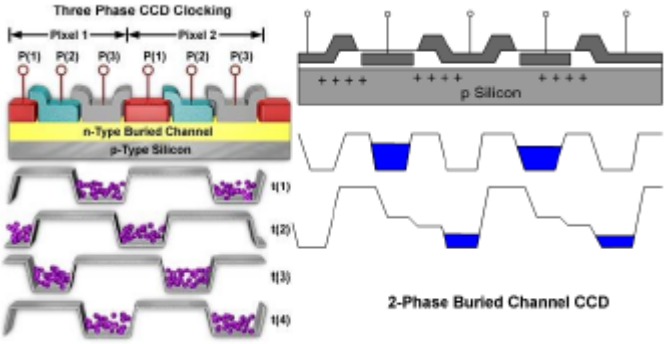


Figure 2.3: Buried Channel CCD (BCCD)

Note: On the left, a cartoon of 3- phase buried channel CCD.

The right panel is a 2-phase BCCD, with extra potential wells (stairs) on the right of each pixel. Polysilicon gates are buried by SiO2, and SiO2 is covered by Al electrodes. There are some other technologies which are necessary to specific applications of CCD. They include channel stops (to achieve lateral confinement for stored charge), regeneration points (to refresh the signal after it has been degraded).

2.1.3 Charge Generation in CCD

When light is shinning on CCD pixels, photons pass through polysilicon gate and reach photodiode (front side illumination) or reach photodiode directly (backside illumination). Generally the longer the wavelength is, the deeper photon can reach into silicon photodiode. As photons are absorbed by photodiode, charge carriers are generated and stored in MOS capacitor provided that they are generated in depletion regions of the epitaxial layer. During this charge generation process, depends on the wavelength, CCD image sensors can be evaluated base on Quantum efficiency. Polysilicon gate is reasonably thin which makes it transparent to longer wavelength, but become opaque at wavelength shorter than 400nm. By using acid-etching techniques, it's possible to thin CCD to 10μm, and use backside illumination to improve Visible-UV QE. AR coating is also a desirable technique. For blue-visible and ultraviolet wavelength (200nm to 400nm), Metachromae II can also be used, which is a technology developed by Roper Scientific — coating CCD with proprietary phosphor. It's shown that QE of CCD with phosphor coating can reach 10% in blue-visible and ultraviolet. Organic phosphor films such as coronene have been used for the CCDs flying in the Hubble Space Telescope (although effective, but QE was still not high).

Although QE of backside illumination could be as high as 90%, the thinning process is very hard and low yield. Except for the general process of CCD chip, additional processing is required to mask BI chip from similar FI chips. QE of front side illumination (FI) tops to 60%. There are some arguments regarding the thinning devices in application of infrared imaging. Due to the high refractive index of Si, there are inevitably significant reflections from any interfaces. Silicon-air, silicon-glass, etc. In red, silicon becomes more transparent, and multiple internal reflections can occur. Fringing pattern happens in this situation. This is inevitable problem in thinning devices for red light imaging. Therefore, thinning devices are generally not used for infrared imaging. UV light imaging could complicate things, since UV light ionized surface molecular on thinning devices. Texas Instruments, Inc. did some research on this. However, the CCDs application in UV light is still not fully understood. Despite the collection of these signal charges, there are also unwanted signals. One of the most prominent unwanted signals is dark current. Dark current due to thermal activity of materials comes from different sources: O-S interface, defects in bulk of silicon. It follows Diode Law:

$$I = Ae^{-B/KT} \qquad \text{---------- (2.2)}$$

Where, A and B are material constants.

Therefore, cooling devices is an efficient way to reduce dark current. Generally, 100°C change in device temperature gives a factor of 3% change in dark current. In the application of astronomy, the working temperatures of CCDs are –160°C to 60°C by using Liquid Nitrogen. Principally, dark current can always be subtracted by taking dark frame, as long as the dark current can be decided. However, this is not usually the case due to the fluctuation of dark current — dark current noise. Another unwanted signal are from cosmic-ray events. This is extremely harmful to space telescope. The last source of unwanted signal is luminescence due to the shorts (circuit) between electrodes or voltage limits of device (not blooming). A low impedance path can act like a light-emitting diode and saturate the device in only a few minutes.

2.1.4 Charge Transfer in CCD

After charge generation beneath electrodes, the charge is hold in the potential well temporarily. Before they are transferred to readout node, recombination could happen to these charge carriers. The recombination will therefore degrade the overall charge collection, i.e., quantum efficiency. Hence, the QE is not only a photoelectrical measurement, but a electron-hole interaction as well. In case of direct recombination, the process is spontaneous for electron and holes (EHPs). The recombination process can be described by the following equation:

$$\frac{dn(t)}{dt} = \alpha_r (n_i^{\,2} - n(t)p(t)) = \alpha_r [n_o + \delta n(t)][p_o + \delta p(t)] \cong \alpha_r p_o \delta n(t) \qquad \text{--------- (2.3)}$$

with the assumption $p_0 >> n_0$.

The solution to this equation is:

$$\delta n(t) = \Delta n e^{-\alpha\, p_o t} = \Delta n e^{-t/\tau_n} \qquad \text{---------- (2.4)}$$

The recombination life time of excess electrons in p-type semiconductor is $\tau_n = \frac{1}{\alpha_r p_o}$. Therefore, for heavily doped p-type silicon (n-channel), the lifetime of excess electron is extremely short. Given GaAs (intrinsic carriers 10^6 cm^{-3}) with $Na=10^{15}$ acceptors/cm^2; hence the minority concentration is $n_o=n_i^2/p_o=10^{-3}$ cm^{-3}; assume at $t=0.10^{14}$EHP/cm^2 is generated. The lifetime calculated is $\tau_n = \tau_p = 10^{-8} s$. So unless the generated charges are put into well (voltage bias), they disappear swiftly.

In charge transfer process, there are several events can stop or delay the process. First one is blooming — potential well is full. In this case, charge overflowed outside the well could move randomly up or down to adjacent pixels. Blooming can be minimized by using

anti-blooming gates. The anti-blooming gates decrease the filling factor of CCD and reduce the full well depth, but it will prevent blooming. This is extremely important when the contrast in the scene is large. The other issue can happen is the wafer defects in CCD. Defects will block or delay the charge transfer process. Observation with defected CCD is difficult to deal with, since the photoelectrical properties around defects (traps) are nonlinear and unpredictable. The low-level CTE (deferred charge problem) can be minimized by pre-charging (overdrive) the device before readout. Charging the device with constant charges, generally a few tens to hundreds of electrons per pixel, is called fat zero or skinny zero.

The major disadvantages of this method are:

1) The added charge increases the effective readout noise of the frame,

2) Devices that need this treatment usually have residual charge transfer problems that continue to affect performance at low light levels.

2.1.5 Charge Readout in CCD

Any number of rows in CCD chip can be added together and send to the serial output register; then any number of output register pixels can be added onto CCD output gate. Adding pixels together is called binning. Binning process increases the sensitivity of CCD, or is used to match with long focal length telescope. However, it decreases spatial resolution as well. What happens at the output node is, charges passed through the output gate are integrated by the node capacitance. To minimize the variations on output transistor, the node capacitor is usually recharged to a fixed potential before the next coming charge packet. The recharging is realized by briefly pulsing the gate of the reset transistor. Once the reset transistor is relaxed to its high impedance 1 (“off” state), the voltage across the node capacitor is established with an uncertainty (noise) of pkTC. At 300K, this value is 400pC node rms, and it drops to 250pC node rms at 120K. This noise converted to electron number is 80 to 125 electrons, which is much higher than the noise of output transistor itself. In addition, the output transistor has an intrinsic noise spectrum.

At low frequency it increases as 1/f. Therefore, it’s dominated by low frequency. High frequency noise is mainly thermal noise from channel resistance. Due to kTC noise and low-frequency noise, there exist additional signal processing circuits (filters) to suppress them. Calibration of readout noise in CCD. For given systems, depending on the signal integration levels, there are several different noise regimes.

1. Lowest level, Readout noise dominates;

2. Medium level, the shot noise of signal charge in with intrinsic readout noise. And eventually the readout noise becomes negligible and SNR is ∞. $\sqrt{N_{signal}}e^-$;

3. Highest level, SNR rises more slowly with signal, due to the onset of nonlinearity near saturation.

Astronomer can learn much about the CCD system by constructing parts on the variance diagram by taking pairs of flat-field exposures at several different signal levels when direct imaging. In spectroscopy, the continuum calibration lamp often gives a considerable variation in signal level, so several points in the variance curve may be determined from ta single exposure, and a smaller number of exposure pairs will be satisfactory. Since X-ray of a few **keV** is detected efficiently in silicon, it can be used as a cross-check on the calibration in laboratory.

2.1.6 Noise Level

Some of these discussions on noise are applicable to both CCD and CMOS if it's not specifically pointed out to either of two.

Reset Noise (kTC): This is due to the capacitance of gate and defined in electron number as: $N_{e^-} = \frac{\sqrt{kTC}}{e^-}$. After every reset action, the capacitance of the floating diffusion is recharged through a "noisy" resistor, being the reset transistor. This reset noise can be that high that is sets the performance limit on the S/N ratio of the imager. In principle it is relatively easy to cancel out the reset noise. It can be minimized by CDS or the use of uni-directional MOS reset switch in pixel (Hewlett-Packard Company).

Dark Current Noise: Dark current can always be corrected by subtracting dark frame from signal image. However this is based on the assumption that dark frame is static. In reality, the dark current has certain variance which can be characterized as dark current noise σ — standard deviation of total temporal noise.

If one writes total grey level on the image as: $g = g_E + g_D$, in which g_E is signal grey value and g_D is dark current induced grey value. Statistically, there two grey values are uncorrelated. Therefore their standard deviations can be added directly as:

$$\sigma = \sqrt{(\sigma_E{}^2 + \sigma_D{}^2)}$$

Which, σ_E is from the CCD chip response to shot signal (photon shot noise).

Further more, the dark current noise σ_D is from reset noise of sense node σ_r, and electronic thermal noise of readout circuit (for CCD readout circuit is outside of pixel; shot noise pf dark current is σ_i.

In comparison of CCD with CMOS, dark current noise of CMOS is much lower than CCD. The paper compared the Dark Current Noise of Kodak's TM-1001/1010 (CCD 1024×1024) and Photonfocus's MV-D1024 (CMOS 1024 × 1024, which uses same CMOS sensor as Dalsa's DS-1x-01M28). CMOS is approximately half of CCD in this case.

Photon Shot Noise: Photon shot noise come from the nature of illumination. The event that a photon striking on object follows Poisson Statistics, which means the uncertainty of the amount of the photon falling on the pixel/eyes, is given by $\sqrt{N_{photon}}$. Photon shot noise degrades SNR. If one assume $SNR_{effective} = \frac{N_E}{N_D + \sqrt{N_E}} = 1024$, then full well capacity fwc=$SNR_{effective}^2$=$10^6 e^-$.

Dark current shot noise: Shot noise associated with photodiode leakage current is most depending on exposure time. Since this noise is due to dark current, there is no way it can be cancelled. Minimize the dark current is the only approach to minimize this noise. It's been reported that CMOS technology can suppress this leakage current to100pA/cm2(HP). In fact, the technology is transferred from CCD industry.

Fixed Pattern Noise (Dark Current Non-Uniformity): This noise is due to the non-uniformity from pixel to pixel on the chip. It's interesting that the more pixels included into average grey level calculation, the smaller variance can be found in CMOS. But this is not the case for CCD, which has a constant (low) variance for any number of pixels include in average calculation. On the other hand, this shows that the variances in CMOS pixels are very high frequency. When the averaged number of pixel increases, these high frequency variance is filtered out, Fig.3.4. These high frequency variances appear in the imaging as blurring or spiking. This is frequency variance appear in the imaging as blurring or spiking. This is the major disadvantage of CMOS pixel over CCD. This is probably due to the fact that each CMOS pixel has independent amplifier, reset gate. To overcome this noise, one can only depend on future improvements in semiconductor processing and IC fabrication.

Thermal Noise: With respect to thermal noise, the CMOS pixel readout sequence is very attractive. The readout speed of every pixel is relatively low (one read cycle for every frame), thus the bandwidth of the amplifier within every pixel is very small. This results in a very small thermal noise component for the CMOS pixels.

The most recent detailed temporal noise modeling and analysis can be shown in below **Figure 2.4**. Thos figure is between pixel number and Pattern Noise (PN).

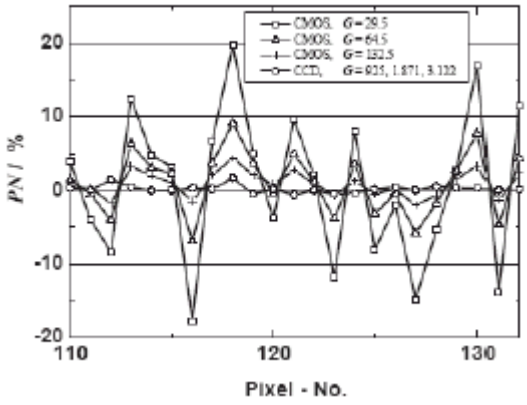
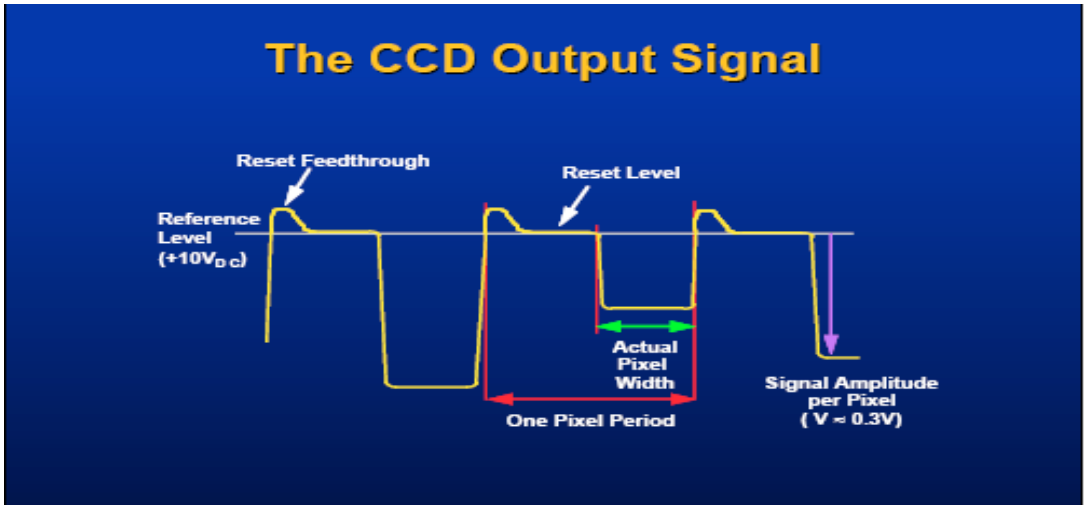


Figure 2.4: Fixed Pattern Noise of CMOS vs. CCD

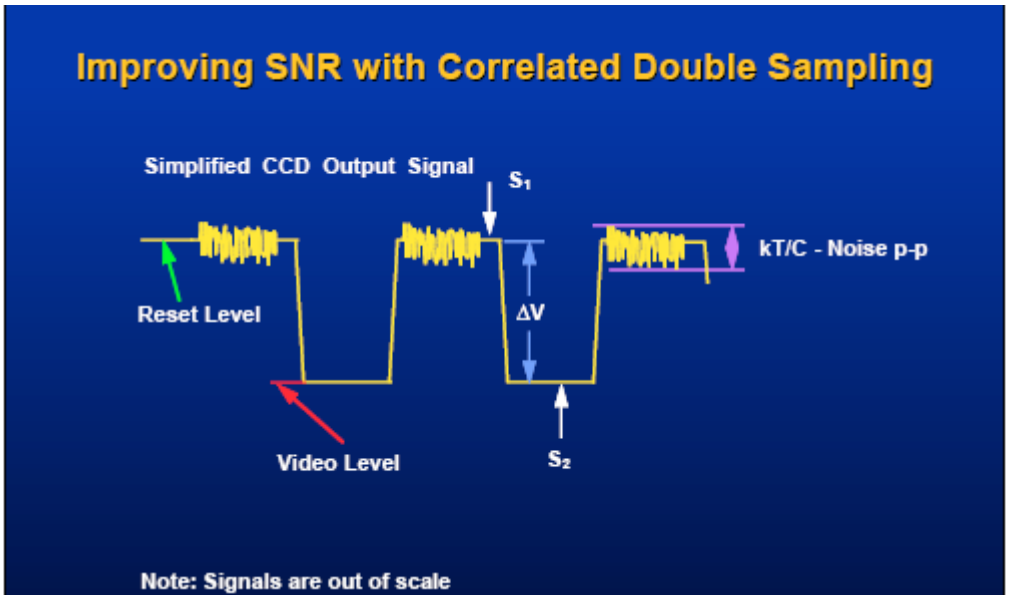


This is a typical output voltage waveform from a CCD element. The signal can be described by five characteristics: the Reset Feedthrough, the Reset Level, the Signal Amplitude, the Pixel Period and the actual Pixel Width. As mentioned before, this CCD signal is not a continuous sinusoidal waveform, but rather is a sequence of stepped DC levels. The sequence for one pixel is as follows:

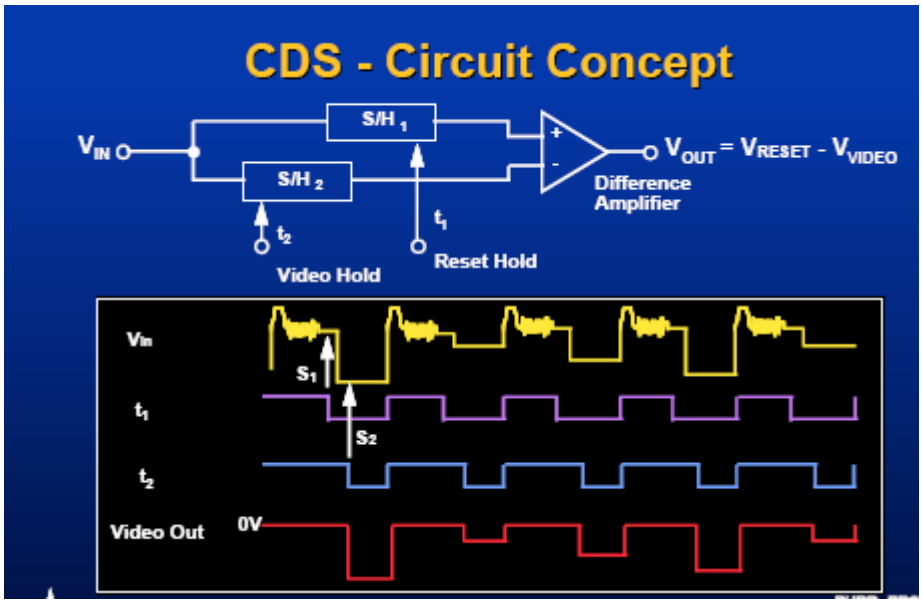
- Reset Feedthrough: This can be a relatively large pulse, as a result of capacitive coupling through the FET.
- Reset Level: The “Sense Capacitor” will be charged to this final reset voltage. This level can be in the order of +10V or more, creating the requirement for a DC-decoupling capacitor at the output of the CCD element.
- Pixel Level: After the reset period, the pixel is transferred. The amplitude corresponds to the charge representing the incident light level of the addressed pixel.

Because of the electron charge (e^-) the CCD output signal is inherently uni-polar (negative).Typical CCD pixel rates can vary between 1Mpixel/sec up to 20Mpixel/sec, depending on the application.

2.1.7 Noise Suppression



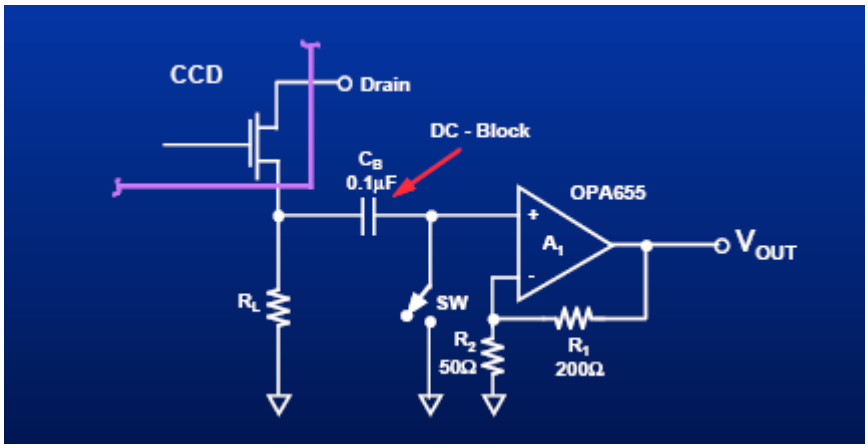
Correlated Double Sampling, or CDS, is a sampling sequence specifically designed to reduce reset noise in FPN. This algorithm originated at Westinghouse in early 1970's through the work of M. White, D. McCarn, I. Mack, F. Blaha. They collectively applied for a patent on CDS concept in 1972 and granted in 1973 under US Patent 3,781,574. As shown before, the noise is the limiting factor for the resolution in a CCD system, where the kT/C noise is dominant. To reduce this noise, imaging systems use a circuit called a "Correlated Double Sampler" (CDS). It should be mentioned that CDS is a mature technology widely used in CCD/CMOS circuitry. CDS first samples the reset voltage of a pixel, then samples the signal voltage, the difference of these two voltage is output voltage. The name comes from the double sampling technique of the CCD charge signal. The first sample (S1) is taken at the end of the reset period. When the reset switch opens again, the effective noise bandwidth changes because of the large difference in the switch's R_{ON} and R_{OFF} resistance. This causes the dominating kT/C noise essentially to "freeze" in its last point. The other sample (S2) is taken during the video portion of the signal. Ideally, the two samples differ only by a voltage corresponding to the transferred charge signal. This is the video level minus the noise (DV). The CDS function will eliminate the kT/C noise as well as much of the 1/f and white noise.



Here is a block diagram of a CDS circuit. Two sample and hold amplifiers and one difference amplifier constitute the correlated double sampler. The signal coming from the CCD is applied to the two sample and hold, with their outputs connected to the difference amplifier. The timing diagram will clarify the operation. At time t1, the sample & hold (S/H1) goes into the hold mode, taking a sample of the reset level including the noise. This voltage (V_{RESET}) is applied to the non-inverting input of the difference amplifier. At time t2, the sample and hold (S/H2) will take a sample of the video level, which is V_{RESET} -V_{VIDEO} . The output voltage of the difference amplifier is defined by the equation $V_{OUT} = VIN^{+} - VIN^{-}$.

The sample of the reset voltage contains the kT/C noise, which is eliminated by the subtraction of the difference amplifier. The double sampling technique also reduces the white noise. The white noise is part of the reset voltage (V_{RESET}) as well as of the video amplitude (V_{RESET} - V_{VIDEO}). With the assumption that the noise of the second sample was unchanged from the instant of the first sample, the noise amplitudes are the same and are correlated in time. Therefore, the noise can be reduced by the CDS function.

2.2 PREAMPLIFIER



The CCD output signal is immediately gained up by the preamplifier, as shown in this circuit schematic. The amplifier itself uses the wideband FET input op amp OPA655, set in a gain of +5V/V. With a -3dB bandwidth of 400MHz for a gain of +1, the bandwidth of the OPA655, in a gain of +5V/V, is 75MHz. The specified 12-bit settling time for this part is about 16ns. To estimate the total response time, the slewing time for the 1Vp-p output needs to be added to the 16ns settling time. With a slewing time of 3.3ns, this adds up to a total of about 20ns. Considering a system with a 5MHz readout frequency, one pixel period takes 200ns. The actual pixel width will be approximately half of that time, or 100ns. The OPA655 will take only 1/5 of the pixel time and still be accurate to 12 bits. The fast response of the OPA655 leaves sufficient time for the subsequent stages and for the acquisition time of the A/D converter. As discussed previously, the pixel information rides on the reference voltage, which can be +10V or more. This could cause unwanted common-mode effects or even saturation. The series capacitor, CB, blocks this DC component from the video signal and the reference of the baseline is lost. A new baseline can be established with the switch, SW, to ground. For each reset period the switch closes and grounds one side of the capacitor, setting its charge to a defined potential, ground or 0V, in this case.

2.3 ANALOG TO DIGITAL CONVERTER

As in previous explain, we get voltage level of signal from pre-amplifier circuit. This voltage is converted into digital form using analog to digital converter (ADC). So, the analog voltage value is converted into digital of 8 bit for pixel level.

2.4 FPGA BLOCK

As shown in block diagram, we get output of CCD from four channels. That pixel level is amplified and converted into digital format. In this block we convert those four channel output is converted into single channel data of one bit (explained in next section).

2.5 INTERFACING BLOCK (Serial)

The output of FPGA is one bit per single clock, but these are coming continuously for the period (read period in FPGA). In this, we interface the output of FPGA block to PC through serial port communication (RS-232),(explained in following section).

Chapter -3

DESIGN

Basically this imager gets the image information in 4096 pixels. These pixels data are coming out through four shift registers. So from each channel we get the data 1024 pixel in different manner. From shift registers 1&3, we get the odd pixels data (1,3,5,7----------,4093,4095) and form shift registers 2&4, we get the even pixels data (2,4,6,8------,4094,4096). For every clock pulse we get four pixel data at a time, But form these shift registers we get the pixel data in the following form.

From register1 we get data of pixels 1,3,5----------,2045,2047.

From register2 we get data of pixels 2,4,6----------,2046,2048.

From register3 we get data of pixels 4095,4093----------,2051,2049.

From register4 we get data of pixels 4096,4094----------,2052,2050.

That is, form shift registers (channels) 1&2 we get data in normal order but form shift register (channels) 3&4 we get the data in reverse order. To convert these pixels data into straight form of data that is data of pixels1,2,3,4----------,4095,4096, we use the block which is shown below.

3.1. Pin Description:

Pin Description: The pin diagram of Design is shown in **Figure3.1.**

Figure 3.1: Pin diagram of Design

clock : Global clock (40 MHz)

pix0 : data from 1st channel i,e. the data of pixels 1,3,5,-------,2045,2047.

pix1 : data from 2nd channel i,e. the data of pixels 2,4,6-------,2046,2048.

pix4096 : data from 3rd channel i,e. the data of pixels 4095,4093,-------,2051,2049.

pix4095 : data from 4th channel i,e. the data of pixels 4096,4094-------,2050,2048.

reset : Global reset, to reset the all modules in FPGA

dataout : data output (1bit)

clamp, phir, phit, phix, sclock, vidsamp : different clock signals to CCD

3.2. Block diagram

The different module used in Design are shown in **Figure3.2**

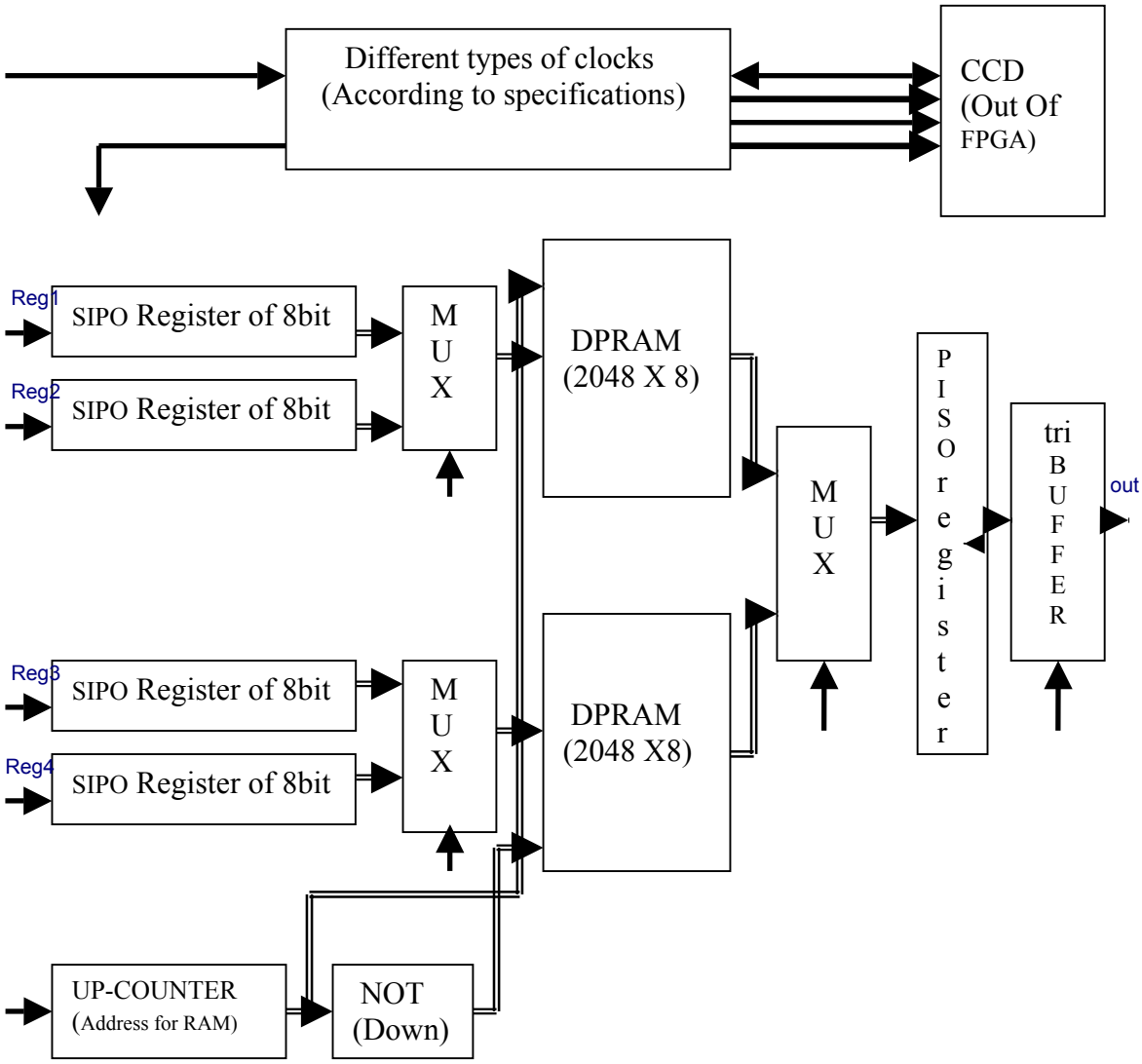


Figure 3.2: Different modules in Block Diagram of Design

SIPO - Serial In Parallel Out

MUX - Multiplexer

DPRAM - Dual Port Random Access Memory

PISO - Parallel Input Serial Output

FPGA - Field Programmable Gate Array

Tri Buffer -Tri-state Buffer

3.3. Description of individual Modules

SIPO Register : This register converts serial pixel data (1 bit) into parallel data of eight (8) bits w.r.t clock signal. For this block has two input pins (pixel, clock) and output of 8 pins.

Multiplexer(MUX) : This block is selects the one of input signal and send as output.

DPRAM : This block is used to store the pixel data according to address generated by Up-Counter. In upper DPRAM data is stored in the increasing manner where as in lower DPRAM data is stored in decreasing manner.

Up-Counter : This block generates the addresses for upper DPRAM, for Lower DPRAM addresses, we complement the up-counter O/P.

PISO Register : This register converts parallel data of 8 bits into serial output of one bit and also in this we add one bit (0) to LSB and one bit(1) to MSB for serial port interfacing.

Tri-Buffer : This block places the input as output if enable to this is high otherwise its output is in high impedance state (Z).

Results:

The results of Pre-synthesis simulation, Synthesis, Post-Synthesis simulation Results are shown in **Result section**. These results are getting from Modules in Design by using the following tools/Languages,

VHDL for Coding of Modules

Modelsim5.5f for Simulation

Leonardo Spectrum for Synthesis

QuartusII for Implementation

FPGA used - **Altera (EP20K300EQC240-3)**

Chapter -4

SERIAL PORT INTERFACING

4.1. Introduction to serial port (RS-232)

The Serial Port is harder to interface than the Parallel Port. In most cases, any device you connect to the serial port will need the serial transmission converted back to parallel so that it can be used. This can be done using a UART. On the software side of things, there are many more registers that you have to attend to than on a Standard Parallel Port. (SPP)

So what are the advantages of using serial data transfer rather than parallel?

1. Serial Cables can be longer than Parallel cables. The serial port transmits a '1' as -3 to -25 volts and a '0' as +3 to +25 volts where as a parallel port transmits a '0' as 0v and a '1' as 5v. Therefore the serial port can have a maximum swing of 50V compared to the parallel port which has a maximum swing of 5 Volts. Therefore cable loss is not going to be as much of a problem for serial cables than they are for parallel.
2. You don't need as many wires than parallel transmission. If your device needs to be mounted a far distance away from the computer then 3 core cable (Null Modem Configuration) is going to be a lot cheaper that running 9 or 25 core cable. However you must take into account the cost of the interfacing at each end.
3. Infra Red devices have proven quite popular recently. You may of seen many electronic diaries and palmtop computers which have infra red capabilities build in. However could you imagine transmitting 8 bits of data at the one time across the room and being able to (from the devices point of view) decipher which bits are which? Therefore serial transmission is used where one bit is sent at a time. IrDA-1 (The first infra red specifications) was capable of 115.2k baud and was interfaced into a UART. The pulse length however was cut down to 3/16th of a RS232 bit length to conserve power considering these devices are mainly used on diaries, laptops and palmtops.
4. Microcontroller's have also proven to be quite popular recently. Many of these have in built SCI (Serial Communications Interfaces) which can be used to talk to the outside world. Serial Communication reduces the pin count of these MPU's. Only two pins are commonly used, Transmit Data (TXD) and Receive Data (RXD) compared with at least 8 pins if you use a 8bit Parallel method (You may also require a Strobe).

4.1.1. Hardware Properties

Devices which use serial cables for their communication are split into two categories. These are DCE (Data Communications Equipment) and DTE (Data Terminal Equipment.) Data Communications Equipment is devices such as your modem, TA adapter, plotter etc while Data Terminal Equipment is your Computer or Terminal.

The electrical specifications of the serial port are contained in the EIA (Electronics Industry Association) RS232C standard. It states many parameters such as -

1. A "Space" (logic 0) will be between +3 and +25 Volts.
2. A "Mark" (Logic 1) will be between -3 and -25 Volts.
3. The region between +3 and -3 volts is undefined.
4. An open circuit voltage should never exceed 25 volts. (In Reference to GND)
5. A short circuit current should not exceed 500mA. The driver should be able to handle this without damage. (Take note of this one!)

Above is no where near a complete list of the EIA standard. Line Capacitance, Maximum Baud Rates etc are also included. For more information please consult the EIA RS232-E standard. It is interesting to note however, that the RS232C standard specifies a maximum baud rate of 20,000 BPS!.

Serial Ports come in two "sizes", There are the D-Type 25 pin connector and the D-Type 9 pin connector both of which are male on the back of the PC, thus you will require a female connector on your device. Below is a table of pin connections for the 9 pin and 25 pin D-Type connectors.

4.1.2. Serial Pinouts (D25 and D9 Connectors)

The pin function names of two D-type connectors are shown in **Table4.1**

D-Type-9 Pin No.	Abbreviation	D-Type-25 Pin No.	Full Name
Pin 3	TD	Pin 2	Transmit Data
Pin 2	RD	Pin 3	Receive Data
Pin 7	RTS	Pin 4	Request To Send
Pin 8	CTS	Pin 5	Clear To Send
Pin 6	DSR	Pin 6	Data Set Ready
Pin 5	SG	Pin 7	Signal Ground
Pin 1	CD	Pin 8	Carrier Detect
Pin 4	DTR	Pin 20	DataTerminal Ready
Pin 9	RI	Pin 22	Ring Indicator

Table 4.1: D Type 9 and D Type25 pin conectors

Pin Functions:

The pin functions of connector are shown in **Table4.2**

Abbreviation	Full Name	Function
TD	Transmit Data	Serial Data Output (TXD)
RD	Receive Data	Serial Data Input (RXD)
CTS	Clear to Send	This line indicates that the Modem is ready to exchange data.
DCD	Data Carrier Detect	When the modem detects a "Carrier" from the modem at the other end of the phone line, this Line becomes active.
DSR	Data Set Ready	This tells the UART that the modem is ready to establish a link.
DTR	Data Terminal Ready	This is the opposite to DSR. This tells the Modem that the UART is ready to link.
RTS	Request To Send	This line informs the Modem that the UART is ready toexchange data.
RI	Ring Indicator	Goes active when modem detects a ringing signal from the PSTN.

Table 4.2: Pin Functions of connector

Null Modems

A Null Modem is used to connect two DTE's together. This is commonly used as a cheap way to network games or to transfer files between computers using Zmodem Protocol, Xmodem Protocol etc. This can also be used with many Microprocessor Development Systems. In my preferred method of wiring a Null Modem. It only requires 3 wires (TD → RD, RD ←TD & SG → SG) to be wired straight through thus is more cost effective to use with long cable runs. The theory of operation is reasonably easy. The aim is to make to computer think it is talking to a modem rather than another computer. Any data transmitted from the first computer must be received by the second thus TD is connected to RD. The second computer must have the same set-up thus RD is connected to TD. Signal Ground (SG)

must also be connected so both grounds are common to each computer. The Data Terminal Ready is looped back to Data Set Ready and Carrier Detect on both computers. When the Data Terminal Ready is asserted active, then the Data Set Ready and Carrier Detect immediately become active. At this point the computer thinks the Virtual Modem to which it is connected is ready and has detected the carrier of the other modem.

All left to worry about now is the Request to Send and Clear To Send. As both computers (devices) communicate together at the same speed, flow control is not needed thus these two lines are also linked together on each computer. When the computer wishes to send data, it asserts the Request to Send high and as it's hooked together with the Clear to Send, It immediately gets a reply that it is ok to send and does so.

DTE / DCE Speeds

We have already talked briefly about DTE & DCE. A typical Data Terminal Device is a computer and a typical Data Communications Device is a Modem. Often people will talk about DTE to DCE or DCE to DCE speeds. DTE to DCE is the speed between your modem and computer, sometimes referred to as your terminal speed. This should run at faster speeds than the DCE to DCE speed. DCE to DCE is the link between modems, sometimes called the line speed. Most people today will have 28.8K or 33.6K modems. Therefore we should expect the DCE to DCE speed to be either 28.8K or 33.6K. Considering the high speed of the modem we should expect the DTE to DCE speed to be about 115,200 BPS. This is where some people often fall into a trap. The communications program which they use have settings for DCE to DTE speeds. However they see 9.6 KBPS, 14.4 KBPS etc and think it is your modem speed.

Flow Control

So if our DTE to DCE speed is several times faster than our DCE to DCE speed the PC can send data to your modem at 115,200 BPS. Sooner or later data is going to get lost as buffers overflow, thus flow control is used. Flow control has two basic varieties, Hardware or Software. Software flow control, sometimes expressed as Xon/Xoff uses two characters Xon and Xoff. Xon is normally indicated by the ASCII 17 character where as the ASCII 19 character is used for Xoff. The modem will only have a small buffer so when the computer fills it up the modem sends a Xoff character to tell the computer to stop sending data. Once the modem has room for more data it then sends a Xon character and the computer sends more data. This type of flow control has the advantage that it doesn't require any more wires as the characters are sent via the TD/RD lines. However on slow links each character requires 10 bits which can slow communications down.

Hardware flow control is also known as RTS/CTS flow control. It uses two wires in your serial cable rather than extra characters transmitted in your data lines. Thus hardware flow control will not slow down transmission times like Xon-Xoff does. When the computer wishes to send data it takes active the Request to Send line. If the modem has room for this data, then the modem will reply by taking active the Clear to Send line and the computer starts sending data. If the modem does not have the room then it will not send a Clear to Send.

4.2. Port Addresses & IRQ's

The standard port addresses of different COMM ports are shown in **Table4.3**

Name	Address	IRQ
COM1	3F8	4
COM2	2F8	3
COM3	3E8	4
COM4	2E8	3

Table 4.3: Standard Port Address of COMM ports

Above is the standard port addresses. These should work for most P.C's. If you just happen to be lucky enough to own a IBM P/S2 which has a micro-channel bus, then expect a different set of addresses and IRQ's. Just like the LPT ports, the base addresses for the COM ports can be read from the BIOS Data Area.

Start Address	Function
0000:0400	COM1's Base Address
0000:0402	COM2's Base Address
0000:0404	COM3's Base Address
0000:0406	COM4's Base Address

Table 4.4: COM Port Addresses in the BIOS Data Area

The above table shows the address at which we can find the Communication (COM) ports addresses in the BIOS Data Area. Each address will take up 2 bytes. The following sample program in C Language, shows how you can read these locations to obtain the addresses of your communications ports.

```
#include <stdio.h>
#include <dos.h>
void main(void)
{
unsigned int far *ptraddr; /* Pointer to location of Port
Addresses */
unsigned int address; /* Address of Port */
int a;
ptraddr=(unsigned int far *)0x00000400;
for (a = 0; a < 4; a++)
{
address = *ptraddr;
if (address == 0)
printf("No port found for COM%d \n",a+1);
else
printf("Address assigned to COM%d is %Xh\n",a+1,address);
*ptraddr++;
}
}
```

4.2.1 Table of Registers

The different registers used in serial port interfacing are shown in **Table4.5**

BaseAddress	DLAB	Read/Write	Abr.	Register Name
+0	=0	write	---	Transmitter Holding Buffer
	=0	read	---	Receiver Buffer
	=1	Read/write	---	Divisor Latch Low Byte
+1	=0	Read/write	IER	Interrupt Enable Register
	=1	Read/write	---	Divisor Latch High Byte
+2	---	Read	IIR	Interrupt Identification Register
	---	write	FCR	FIFO Control Register
+3	---	Read/write	LCR	Line Control Register
+4	---	Read/write	MCR	Modem Control Register
+5	---	Read	LCS	Line Status Register
+6	---	Read	MCS	Modem Status Register
+7	---	Read/write	---	Scratch Register

Table 4.5: Table of Registers

DLAB?

You will have noticed in the table of registers that there is a DLAB column. When DLAB is set to '0' or '1' some of the registers change. This is how the UART is able to have 12 registers (including the scratch register) through only 8 port addresses. DLAB stands for Divisor Latch Access Bit. When DLAB is set to '1' via the line control register, two registers become available from which you can set your speed of communications measured in bits per second. The UART will have a crystal which should oscillate around 1.8432 MHZ.Assuming we had the 1.8432 MHZ clock signal, that would leave us with a maximum, 115,200 hertz signal making the UART capable of transmitting and receiving at 115,200 Bits Per Second (BPS). That would be fine for some of the faster modems and devices which can handle that speed, but others just wouldn't communicate at all. Therefore the UART is fitted with a Programmable Baud Rate Generator which is controlled by two registers.

Lets say for example we only wanted to communicate at 2400 BPS. We worked out that we would have to divide 115,200 by 48 to get a workable 2400 Hertz Clock. The "Divisor", in this case 48, is stored in the two registers controlled by the "Divisor Latch Access Bit". This divisor can be any number which can be stored in 16 bits (ie 0 to 65535). The UART only has a 8 bit data bus, thus this is where the two registers are used. The first

register (Base + 0) when DLAB = 1 stores the "Divisor latch low byte" where as the second register (base + 1 when DLAB = 1) stores the "Divisor latch high byte." Below is a table of some more common speeds and their divisor latch high bytes & low bytes. Note that all the divisors are shown in Hexadecimal.

Speed (BPS)	**Divisor (Dec)**	**Divisor Latch High Byte**	**Divisor Latch Low Byte**
50	2304	09h	00h
300	384	01h	80h
600	192	00h	C0h
2400	48	00h	30h
4800	24	00h	18h
9600	12	00h	0Ch
19200	6	00h	06h
38400	3	00h	03h
57600	2	00h	02h
115200	1	00h	01h

Table 4.6: Table of Commonly Used Baudrate Divisors

Interrupt Enable Register (IER)

Bit	**Notes**
Bit 7	Reserved
Bit 6	Reserved
Bit 5	Enables Low Power Mode (16750)
Bit 4	Enables Sleep Mode (16750)
Bit 3	Enable Modem Status Interrupt
Bit 2	Enable Receiver Line Status Interrupt
Bit 1	Enable Transmitter Holding Register Empty Interrupt
Bit 0	Enable Received Data Available Interrupt

Table 4.7: Interrupt Enable Register

The Interrupt Enable Register could possibly be one of the easiest registers on a UART to under-stand. Setting Bit 0 high enables the Received Data Available Interrupt which generates an interrupt when the receiving register/FIFO contains data to be read by the CPU. Bit 1 enables Transmit Holding Register Empty Interrupt. This interrupts the CPU when the transmitter buffer is empty. Bit 2 enables the receiver line status interrupt. The UART will interrupt when the receiver line status changes. Likewise for bit 3 which enables the modem status interrupt. Bits 4 to 7 are the easy ones. They are simply reserved. (If only everything was that easy!)

Interrupt Identification Register (IIR)

Bit	Notes
Bits 6 : 7	Bit6 Bit7
	0 0 No FIFO
	0 1 FIFO Enabled
	1 1 FIFO Enabled
Bit 5	64Byte FIFO Enabled (16750 only)
Bit 4	Reserved
Bit 3	0 Reserved on 8250, 16450
	1 16550 Time-out Interrupt Pending
Bits 1 : 2	Bit2 Bit1
	0 0 Modem Status Interrupt
	0 1 Transmitter Holding Register Empty Interrupt
	1 0 Received Data Available Interrupt
	1 1 Receiver Line Status Interrupt
Bit 0	0 Interrupt Pending
	1 No Interrupt Pending

Table 4.8: Interrupt Identification Register

The interrupt identification register is a read only register. Bits 6 and 7 give status on the FIFO Buffer. When both bits are '0' no FIFO buffers are active. This should be the only result you will get from a 8250 or 16450. If bit 7 is active but bit 6 is not active then the UART has it's buffers enabled but are unusable. This occurs on the 16550 UART where a bug in the

FIFO buffer made the FIFO's unusable. If both bits are '1' then the FIFO buffers are enabled and fully operational. Bits 4 and 5 are reserved. Bit 3 shows the status of the time-out interrupt on a 16550 or higher. Lets jump to Bit 0 which shows whether an interrupt has occurred. If an interrupt has occurred it's status will shown by bits 1 and 2. These interrupts work on a priority status. The Line Status Interrupt has the highest Priority, followed by the Data Available Interrupt, then the Transmit Register Empty Interrupt and then the Modem Status Interrupt which has the lowest priority.

First In / First Out Control Register (FCR)

Bit	Notes
Bits6:7	Bit7 Bit6 Interrupt Trigger Level 0 0 1 Byte 0 1 4 Bytes 1 0 8 Bytes 1 1 14 Bytes
Bit 5	Enable 64 Byte FIFO (16750 only)
Bit 4	Reserved
Bit 3	DMA Mode Select. Change status of RXRDY & TXRDY pins from mode 1 to mode 2.
Bit 2	Clear Transmit FIFO
Bit 1	Clear Receive FIFO
Bit 0	Enable FIFO's

Table4.9: FIFO Control Register

The FIFO register is a write only register. This register is used to control the FIFO (First In / First Out) buffers which are found on 16550's and higher. Bit 0 enables the operation of the receive and transmit FIFO's. Writing a '0' to this bit will disable the operation of transmit and receive FIFO's, thus you will loose all data stored in these FIFO buffers. Bit's 1 and 2 control the clearing of the transmit or receive FIFO's. Bit 1 is responsible for the receive buffer while bit 2 is responsible for the transmit buffer. Setting these bits to 1 will only clear the contents of the FIFO and will not affect the shift registers. These two bits are self resetting, thus you don't need to set the bits to '0' when finished. Bit 3 enables the DMA mode select which is found on 16550 UARTs and higher. More on this later. Bits 4 and 5 are those easy type again, Reserved. Bits 6 and 7 are used to set the triggering level on the

Receive FIFO. For example if bit 7 was set to '1' and bit 6 was set to '0' then the trigger level is set to 8 bytes. When there is 8 bytes of data in the receive FIFO then the Received Data Available interrupt is set. See (IIR)

Line Control Register (LCR)

Bit	Notes
Bit7	1 Divisor Latch Access Bit
	0 Access to Receiver buffer, Transmitter Enable Register
Bit6	Set Break Enable
Bits3:5	Bit5 Bit4 Bit3 Parity Select
	X X 0 No Parity
	0 0 1 Odd Parity
	0 1 1 Even Parity
	1 0 1 High Parity (Sticky)
	1 1 1 Low Parity (Sticky)
Bit 2	Length of Stop Bit
	0 One Stop Bit
	1 2 Stop bits for words of length 6,7 or 8 bits or 1.5 Stop
Bits 0:1	Bits for Word lengths of 5 bits.
	Bit1 Bit0 Word Length
	0 0 5 Bits
	0 1 6 Bits
	1 0 7 Bits
	1 1 8 Bits

Table 4.10: Line Control Register

The Line Control register sets the basic parameters for communication. Bit 7 is the Divisor Latch Access Bit or DLAB for short. We have already talked about what it does. (See DLAB?) Bit 6 Sets break enable. When active, the TD line goes into "Spacing" state which causes a break in the receiving UART. Setting this bit to '0' Disables the Break. Bits 3,4 and 5 select parity. If you study the 3 bits, you will find that bit 3 controls parity. That is, if it is set to '0' then no parity is used, but if it is set to '1' then parity is used. Jumping to bit 5, we can see that it controls sticky parity. Sticky parity is simply when the parity bit is always transmitted and checked as a '1' or '0'. This has very little success in checking for errors as if

the first 4 bits contain errors but the sticky parity bit contains the appropriately set bit, then a parity error will not result. Sticky high parity is the use of a '1' for the parity bit, while the opposite, sticky low parity is the use of a '0' for the parity bit. If bit 5 controls sticky parity, then turning this bit off must produce normal parity provided bit 3 is still set to '1'. Odd parity is when the parity bit is transmitted as a '1' or '0' so that there is a odd number of 1's. Even parity must then be the parity bit produces and even number of 1's. This provides better error checking but still is not perfect, thus CRC-32 is often used for software error correction. If one bit happens to be inverted with even or odd parity set, then a parity error will occur, however if two bits are flipped in such a way that it produces the correct parity bit then an parity error will no occur. Bit 2 sets the length of the stop bits. Setting this bit to '0' will produce one stop bit, however setting it to '1' will produce either 1.5 or 2 stop bits depending upon the word length. Note that the receiver only checks the first stop bit. Bits 0 and 1 set the word length. This should be pretty straight forward. A word length of 8 bits is most commonly used today.

Modem Control Register (MCR)

Bit	**Notes**
Bit 7	Reserved
Bit 6	Reserved
Bit 5	Autoflow Control Enabled (16750 only)
Bit 4	LoopBack Mode
Bit 3	Aux Output 2
Bit 2	Aux Output 1
Bit 1	Force Request to Send
Bit 0	Force Data Terminal Ready

Table 4.11: Modem Control Register

The Modem Control Register is a Read/Write Register. Bits 5,6 and 7 are reserved. Bit 4 activates the loopback mode. In Loopback mode the transmitter serial output is placed into marking state. The receiver serial input is disconnected. The transmitter out is looped back to the receiver in. DSR, CTS, RI & DCD are disconnected. DTR, RTS, OUT1 & OUT2 are connected to the modem control inputs. The modem control output pins are then place in an inactive state. In this mode any data which is placed in the transmitter registers for output is received by the receiver circuitry on the same chip and is available at the receiver buffer.

This can be used to test the UARTs operation. Aux Output 2 maybe connected to external circuitry which controls the UART-CPU interrupt process. Aux Output 1 is normally disconnected, but on some cards is used to switch between a 1.8432MHZ crystal to a 4MHZ crystal which is used for MIDI. Bits 0 and 1 simply control their relevant data lines. For example setting bit 1 to '1' makes the request to send line active.

Line Status Register (LSR)

Bit	**Notes**
Bit 7	Error in Received FIFO
Bit 6	Empty Data Holding Registers
Bit 5	Empty Transmitter Holding Register
Bit 4	Break Interrupt
Bit 3	Framing Error
Bit 2	Parity Error
Bit 1	Overrun Error
Bit 0	Data Ready

Table 4.12: Line Status Register

The line status register is a read only register. Bit 7 is the error in received FIFO bit. This bit is high when at least one break, parity or framing error has occurred on a byte which is contained in the FIFO. When bit 6 is set, both the transmitter holding register and the shift register are empty. The UART's holding register holds the next byte of data to be sent in parallel fashion. The shift register is used to convert the byte to serial, so that it can be transmitted over one line. When bit 5 is set, only the transmitter holding register is empty. So what's the difference between the two? When bit 6, the transmitter holding and shift registers are empty, no serial conversions are taking place so there should be no activity on the transmit data line. When bit 5 is set, the transmitter holding register is empty, thus another byte can be sent to the data port, but a serial conversion using the shift register may be taking place. The break interrupt (Bit 4) occurs when the received data line is held in a logic state '0' (Space) for more than the time it takes to send a full word. That includes the time for the start bit, data bits, parity bits and stop bits. A framing error (Bit 3) occurs when the last bit is not a stop bit. This may occur due to a timing error. You will most commonly encounter a framing error when using a null modem linking two computers or a protocol analyzer when the speed at which the data is being sent is different to that of what you have the UART set to receive it at. A overrun error normally occurs when your program can't read from the port fast enough.

If you don't get an incoming byte out of the register fast enough, and another byte just happens to be received, then the last byte will be lost and a overrun error will result. Bit 0 shows data ready, which means that a byte has been received by the UART and is at the receiver buffer ready to be read.

Modem Status Register (MSR)

Bits	**Notes**
Bit 7	Carrier Detect
Bit 6	Ring Indicator
Bit 5	Data Set Ready
Bit 4	Clear To Send
Bit 3	Delta Data Carrier Detect
Bit 2	Trailing Edge Ring Indicator
Bit 1	Delta Data Set Ready
Bit 0	Delta Clear to Send

Table 4.13: Modem Status Register

Bit 0 of the modem status register shows delta clear to send, delta meaning a change in, thus delta clear to send means that there was a change in the clear to send line, since the last read of this register. This is the same for bits 1 and 3. Bit 1 shows a change in the Data Set Ready line where as Bit 3 shows a change in the Data Carrier Detect line. Bit 2 is the Trailing Edge Ring Indicator which indicates that there was a transformation from low to high state on the Ring Indicator line. Bits 4 to 7 show the current state of the data lines when read. Bit 7 shows Carrier Detect, Bit 6 shows Ring Indicator, Bit 5 shows Data Set Ready & Bit 4 shows the status of the Clear To Send line.

Scratch Register

The scratch register is not used for communications but rather used as a place to leave a byte of data. The only real use it has is to determine whether the UART is a 8250/8250B or a 8250A/16450 and even that is not very practical today as the 8250/8250B was never designed for AT's and can't hack the bus speed.

4.3. Interfacing Devices to RS-232 Ports

RS-232 Waveforms

So far we have introduced RS-232 Communications in relation to the PC. RS-232 communication is asynchronous. That is a clock signal is not sent with the data. Each word is synchronized using it's start bit, and an internal clock on each side, keeps tabs on the timing. The Rs-232 serial logic waveform with start and stop bits are shown in **Figure4.**1

Start bit	0	1	2	3	4	5	6	7	Stop bit

Figure 4.1: RS-232 Serial Logic Waveform

The diagram above shows the expected waveform from the UART when using the common 8N1 format. 8N1 signifies 8 Data bits, No Parity and 1 Stop Bit. The RS-232 line, when idle is in the Mark State (Logic 1). A transmission starts with a start bit which is (Logic 0). Then each bit is sent down the line, one at a time. The LSB (Least Significant Bit) is sent first. A Stop Bit (Logic 1) is then appended to the signal to make up the transmission. The diagram, shows the next bit after the Stop Bit to be Logic 0. This must mean another word is following, and this is it's Start Bit. If there is no more data coming then the receive line will stay in it's idle state(logic 1). We have encountered something called a "Break" Signal. This is when the data line is held in a Logic 0 state for a time long enough to send an entire word. Therefore if you don't put the line back into an idle state, then the receiving end will interpret this as a break signal. The data sent using this method, is said to be *framed*. That is the data is *framed* between a Start and Stop Bit. Should the Stop Bit be received as logic 0, then a framing error will occur. This is common, when both sides are communicating at different speeds. The above diagram is only relevant for the signal immediately at the UART. RS-232 logic levels uses +3 to +25 volts to signify a "Space" (Logic 0) and -3 to -25 volts for a "Mark" (logic 1). Any voltage in between these regions (ie between +3 and -3 Volts) is undefined. Therefore this signal is put through a "RS-232 Level Converter".

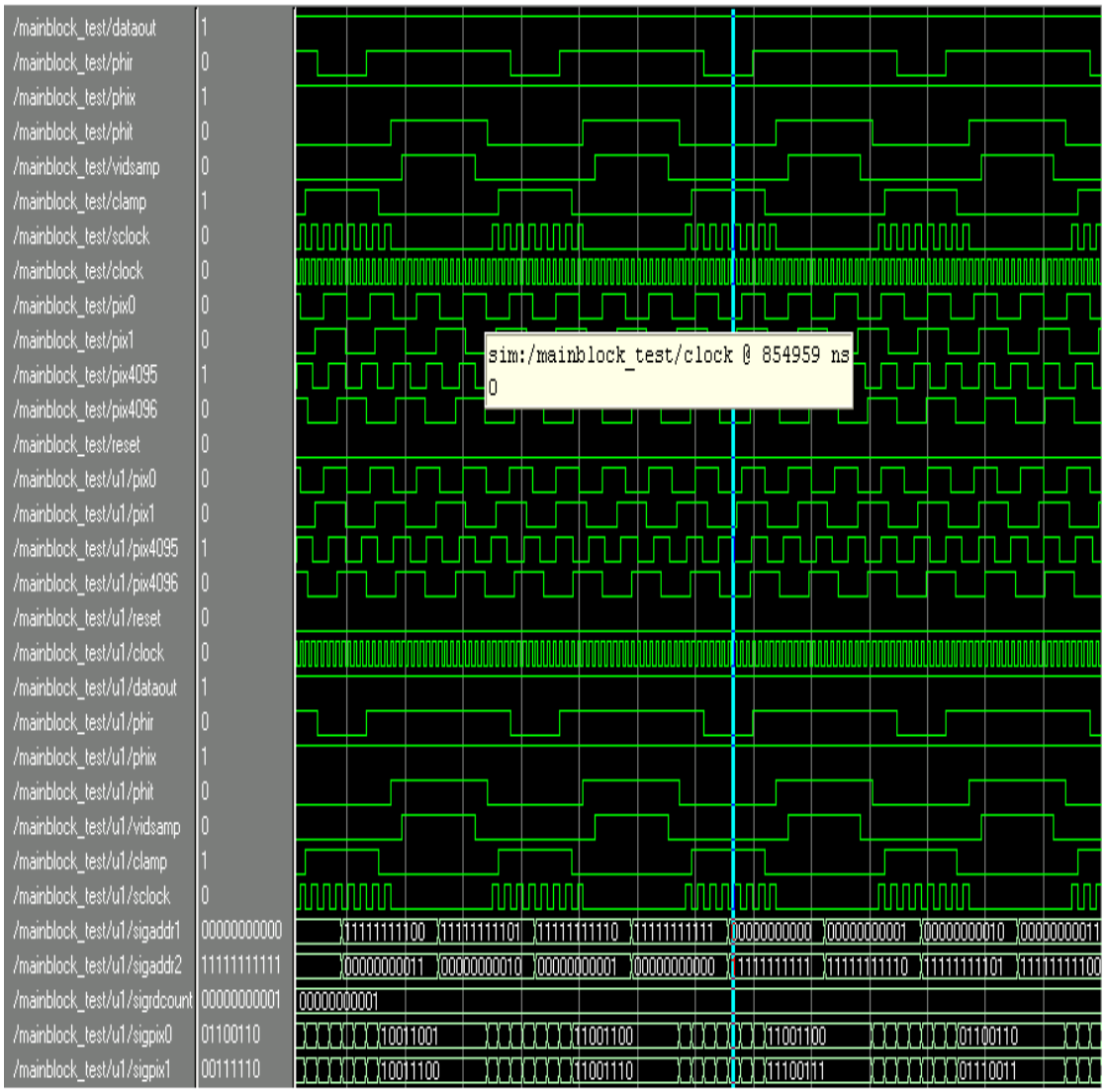
The C program which is used to interface the output data of FPGA to computer is shown below

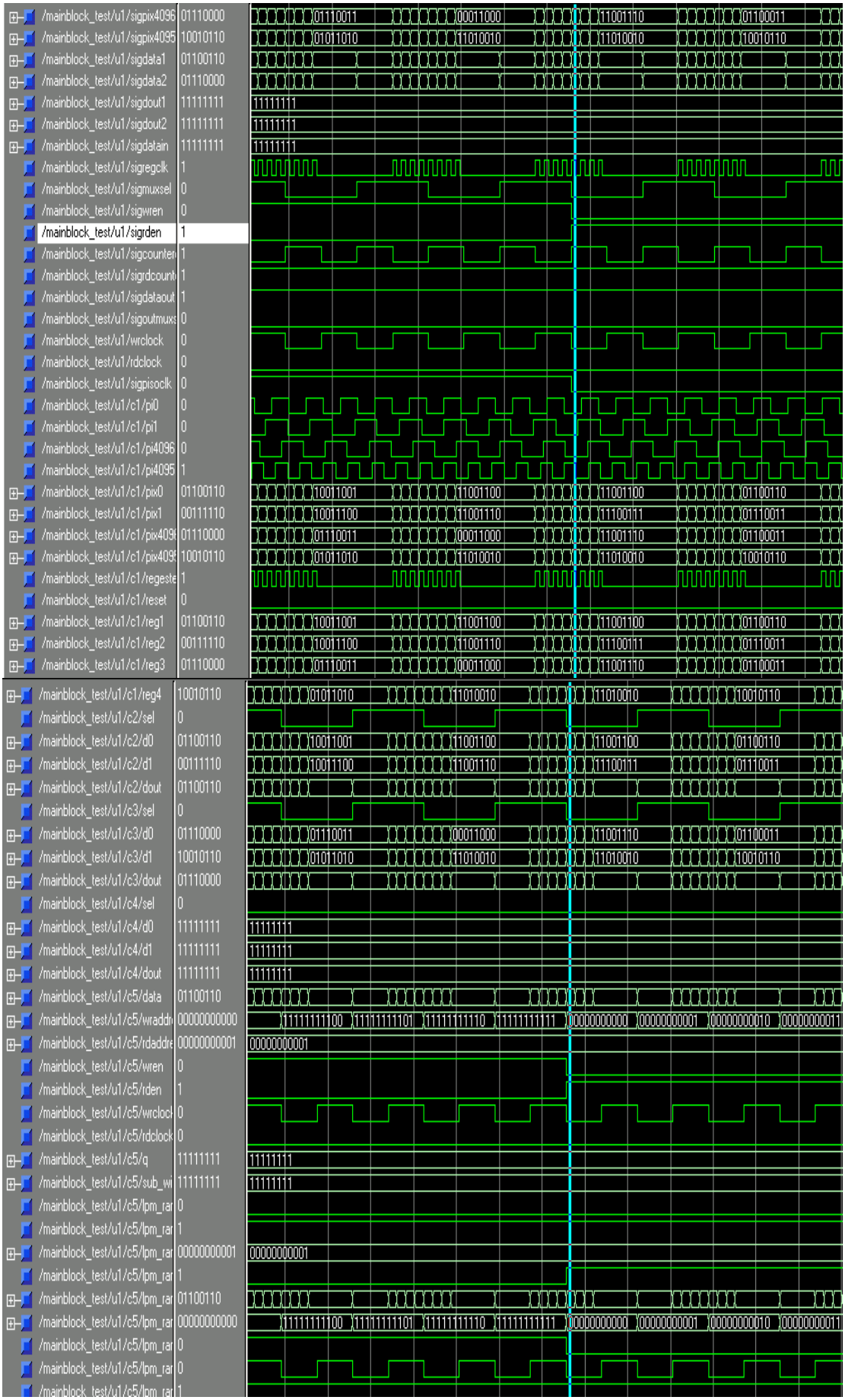
```
#define COM1BASE 0X3F8
#define TXDATA COM1BASE
#define LCR (COM1BASE+1)
#define LSR (COM1BASE+2)
#include<conio.h>
#include<dos.h>
#include<stdio.h>
#include<math.h>
#include<io.h>
#include<bios.h>

void setup_serial(void);
int get_char(void);

int main(void)
{
int inchar,s,p,i;
FILE *fp;
clrscr();
setup_serial();
fp=fopen("data1.c","w");
while(!kbhit())
{
   s=0;
   for(i=1;i<=8;i++)
   {
   p= pow(2,(8-i));
   inchar=get_char();
   s=s+(inchar*p);
   }
   printf("The grey level for recieved pixel is %d\n",s);
   fprintf(fp,"%d",s);
   fprintf(fp," ");
}
fclose(fp);
return (0);
}
void setup_serial()
{
outportb(LCR,0X80);
outportb(TXDATA,0X06);
outportb(TXDATA+1,0X00);
outportb(LCR,0X0A);
}
int get_char(void)
{
 while(!inportb(LSR)&0X01);
 return((int)inportb(TXDATA));
}
```

Chapter -5
RESULTS and DISSCUSSION

In every design, we first developed individual modules those are shown in block diagram and all these modules are combined (structural design). Here all modules are coded in VHDL, simulated using Modelsim, synthesized using Leonardo Spectrum and then the back annotated file simulated (post synthesis simulation). The simulation and synthesis results are shown below.

5.1. Pre-synthesis simulation results:




/mainblock_test/u1/sigpix4096 01110000
/mainblock_test/u1/sigpix4095 10010110
/mainblock_test/u1/sigdata1 01100110
/mainblock_test/u1/sigdata2 01110000
/mainblock_test/u1/sigdout1 11111111
/mainblock_test/u1/sigdout2 11111111
/mainblock_test/u1/sigdatain 11111111
/mainblock_test/u1/sigregclk 1
/mainblock_test/u1/sigmuxsel 0
/mainblock_test/u1/sigwren 0
/mainblock_test/u1/sigrden 1
/mainblock_test/u1/sigcounter 1
/mainblock_test/u1/sigrdcount 1
/mainblock_test/u1/sigdataout 1
/mainblock_test/u1/sigoutmux 0
/mainblock_test/u1/wrclock 0
/mainblock_test/u1/rdclock 0
/mainblock_test/u1/sigpisoclk 0
/mainblock_test/u1/c1/pi0 0
/mainblock_test/u1/c1/pi1 0
/mainblock_test/u1/c1/pi4096 0
/mainblock_test/u1/c1/pi4095 1
/mainblock_test/u1/c1/pix0 01100110
/mainblock_test/u1/c1/pix1 00111110
/mainblock_test/u1/c1/pix409 01110000
/mainblock_test/u1/c1/pix409 10010110
/mainblock_test/u1/c1/regeste 1
/mainblock_test/u1/c1/reset 0
/mainblock_test/u1/c1/reg1 01100110
/mainblock_test/u1/c1/reg2 00111110
/mainblock_test/u1/c1/reg3 01110000
/mainblock_test/u1/c1/reg4 10010110
/mainblock_test/u1/c2/sel 0
/mainblock_test/u1/c2/d0 01100110
/mainblock_test/u1/c2/d1 00111110
/mainblock_test/u1/c2/dout 01100110
/mainblock_test/u1/c3/sel 0
/mainblock_test/u1/c3/d0 01110000
/mainblock_test/u1/c3/d1 10010110
/mainblock_test/u1/c3/dout 01110000
/mainblock_test/u1/c4/sel 0
/mainblock_test/u1/c4/d0 11111111
/mainblock_test/u1/c4/d1 11111111
/mainblock_test/u1/c4/dout 11111111
/mainblock_test/u1/c5/data 01100110
/mainblock_test/u1/c5/wradd 00000000000
/mainblock_test/u1/c5/rdaddr 00000000001
/mainblock_test/u1/c5/wren 0
/mainblock_test/u1/c5/rden 1
/mainblock_test/u1/c5/wrclock 0
/mainblock_test/u1/c5/rdclock 0
/mainblock_test/u1/c5/q 11111111
/mainblock_test/u1/c5/sub_wi 11111111
/mainblock_test/u1/c5/lpm_ra 0
/mainblock_test/u1/c5/lpm_ra 1
/mainblock_test/u1/c5/lpm_ra 00000000001
/mainblock_test/u1/c5/lpm_ra 1
/mainblock_test/u1/c5/lpm_ra 01100110
/mainblock_test/u1/c5/lpm_ra 00000000000
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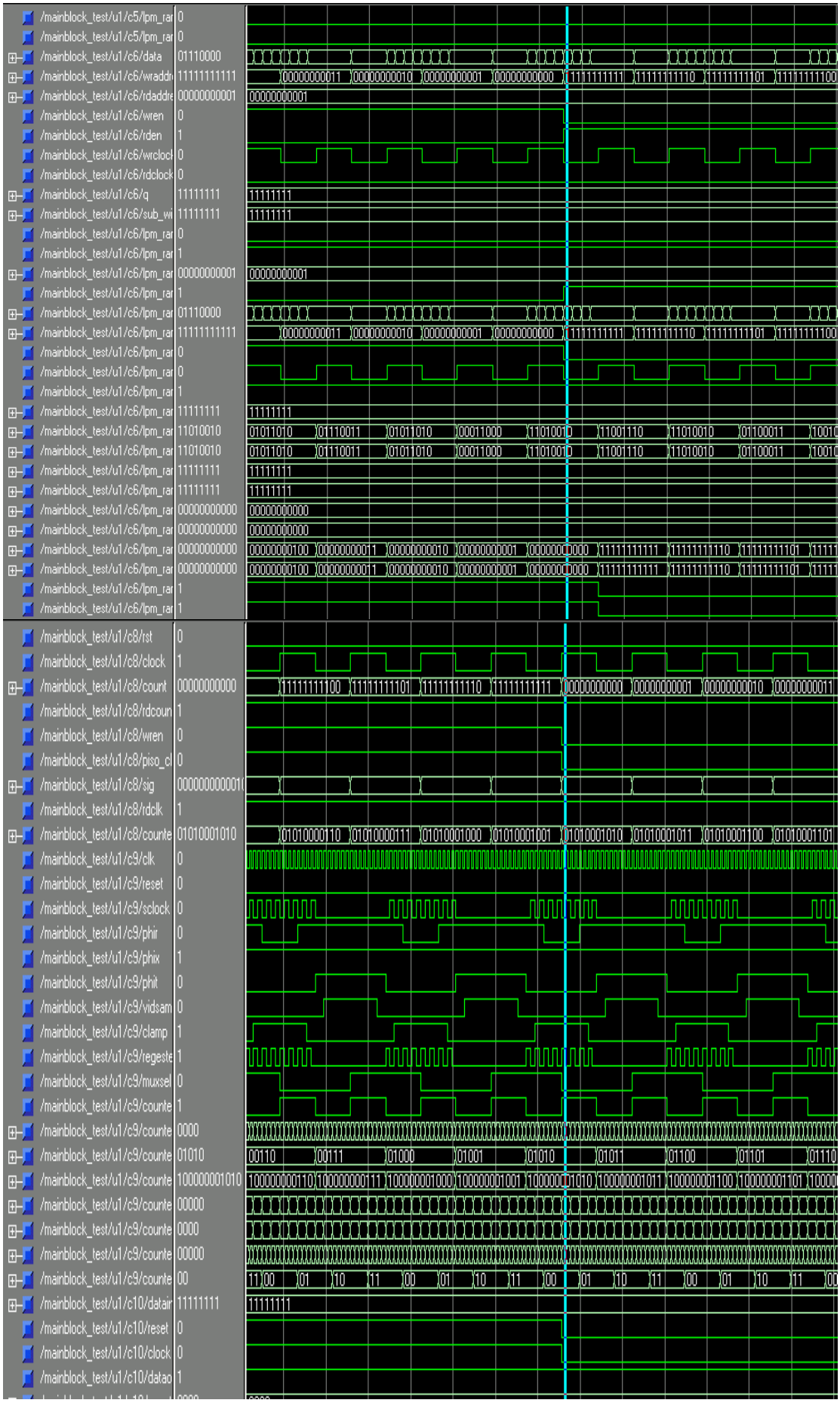
/mainblock_test/u1/c5/lpm_ra 0
/mainblock_test/u1/c5/lpm_ra 1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/mainblock_test/u1/c6/data
/mainblock_test/u1/c6/wraddr
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/mainblock_test/u1/c6/wren
/mainblock_test/u1/c6/rden
/mainblock_test/u1/c6/wrclock
/mainblock_test/u1/c6/rdclock
/mainblock_test/u1/c6/q
/mainblock_test/u1/c6/sub_wi
/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c6/lpm_rar
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/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c6/lpm_rar
/mainblock_test/u1/c8/rst
/mainblock_test/u1/c8/clock
/mainblock_test/u1/c8/count
/mainblock_test/u1/c8/rdcoun
/mainblock_test/u1/c8/wren
/mainblock_test/u1/c8/piso_cl
/mainblock_test/u1/c8/sig
/mainblock_test/u1/c8/rdclk
/mainblock_test/u1/c8/counte
/mainblock_test/u1/c9/clk
/mainblock_test/u1/c9/reset
/mainblock_test/u1/c9/sclock
/mainblock_test/u1/c9/phir
/mainblock_test/u1/c9/phix
/mainblock_test/u1/c9/phit
/mainblock_test/u1/c9/vidsam
/mainblock_test/u1/c9/clamp
/mainblock_test/u1/c9/regeste
/mainblock_test/u1/c9/muxsel
/mainblock_test/u1/c9/counte
/mainblock_test/u1/c9/counte
/mainblock_test/u1/c9/counte
/mainblock_test/u1/c9/counte
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/mainblock_test/u1/c9/counte
/mainblock_test/u1/c9/counte
/mainblock_test/u1/c10/datair
/mainblock_test/u1/c10/reset
/mainblock_test/u1/c10/clock
/mainblock_test/u1/c10/datao

5.2. Synthesis report and schematic view:

5.2.1 Synthesis Report:

-- Start optimization for design .work.mainblock.mainblock

Using default wire table: apex20e_default

Pass	LCs	Delay	DFFs	TRIs	PIs	POs	--CPU-- min:sec
1	166	11	49	1	6	7	00:01
2	163	11	49	1	6	7	00:01
3	162	11	49	1	6	7	00:01
4	162	11	49	1	6	7	00:01

Info, Pass 3 was selected as best.

-- Writing file .work.counter.INTERFACE_delay.xdb

-- Writing XDB version 1999.1

-- Writing file .work.lpm_ram_dp_8_11_TRUE_UNUSED_REGISTERED_REGISTERED_REGISTERED_UNREGISTERED_ON_LPM_RAM_DP.INTERFACE_delay.xdb

-- Writing XDB version 1999.1

-- Writing file .work.mainblock.mainblock_delay.xdb

-- Writing XDB version 1999.1

Reading library file `C:\Exemplar\LeoSpec\LS2002a_49\\lib\apex20e.syn`...

Library version = 2.4

Delays assume: Process=3

-- Reading file __first.xdb

-- Reading XDB version 1999.1

-- optimize -single_level -target apex20e -effort standard -macro -area -hierarchy=auto

Using default wire table: apex20e_default

-- optimize -single_level -target apex20e -effort standard -macro -area -hierarchy=auto

Using default wire table: apex20e_default

-- optimize -single_level -target apex20e -effort standard -chip -area -hierarchy=auto

Using default wire table: apex20e_default

-- Start optimization for design .work.mainblock.mainblock

Using default wire table: apex20e_default

Pass	LCs	Delay	DFFs	TRIs	PIs	POs	--CPU-- min:sec
1	165	11	49	1	6	7	00:01
2	165	11	49	1	6	7	00:01
3	161	11	49	1	6	7	00:01
4	160	11	49	1	6	7	00:01

Info, Pass 3 was selected as best.

-- Area mode had better result for design .work.mainblock.mainblock

-- Delay mode had better result for design .work.lpm_ram_dp_8_11_TRUE_UNUSED_REGISTERED_REGISTERED_REGISTERED_UNREGISTERED_ON_LPM_RAM_DP.INTERFACE

-- Reading file .work.lpm_ram_dp_8_11_TRUE_UNUSED_REGISTERED_REGISTERED_REGISTERED_UNREGISTERED_ON_LPM_RAM_DP.INTERFACE_delay.xdb

-- Reading XDB version 1999.1

-- Delay mode had better result for design .work.counter.INTERFACE

-- Reading file .work.counter.INTERFACE_delay.xdb

-- Reading XDB version 1999.1

Using default wire table: apex20e_default

-- Start timing optimization for design .work.mainblock.mainblock

No critical paths to optimize at this level

****

****

Cell: mainblock View: mainblock Library: work

Cell: mainblock View: mainblock Library: work

****

****

Number of ports:	13
Number of nets:	285
Number of instances:	196
Number of references to this view:	0

Total accumulated area:

Number of IOs: 13

Number of LCs: 162

Black Box counter: 1

BlackBox

lpm_ram_dp_8_11_TRUE_UNUSED_REGISTERED_REGISTERED_REGISTERED_UN

REGISTERED_ON_LPM_RAM_DP: 2

Number of accumulated instances: 196

****

Device Utilization for EP20K300EQC240

****

Resource	Used	Avail	Utilization
IOs	13	152	8.55%
LCs	162	11520	1.41%
Memory Bits	0	147456	0.00%

Clock Frequency Report

Clock	: Frequency
clock	: 220.8 MHz
sigrdcounterclk	: 193.9 MHz
sigpisoclk	: 115.6 MHz
c9_counter4(0)	: 137.6 MHz
c9_counter4(1)	: 271.0 MHz
sigregclk	: 269.5 MHz
c9_NOT_counter4(3)	: 195.7 MHz

Critical Path Report

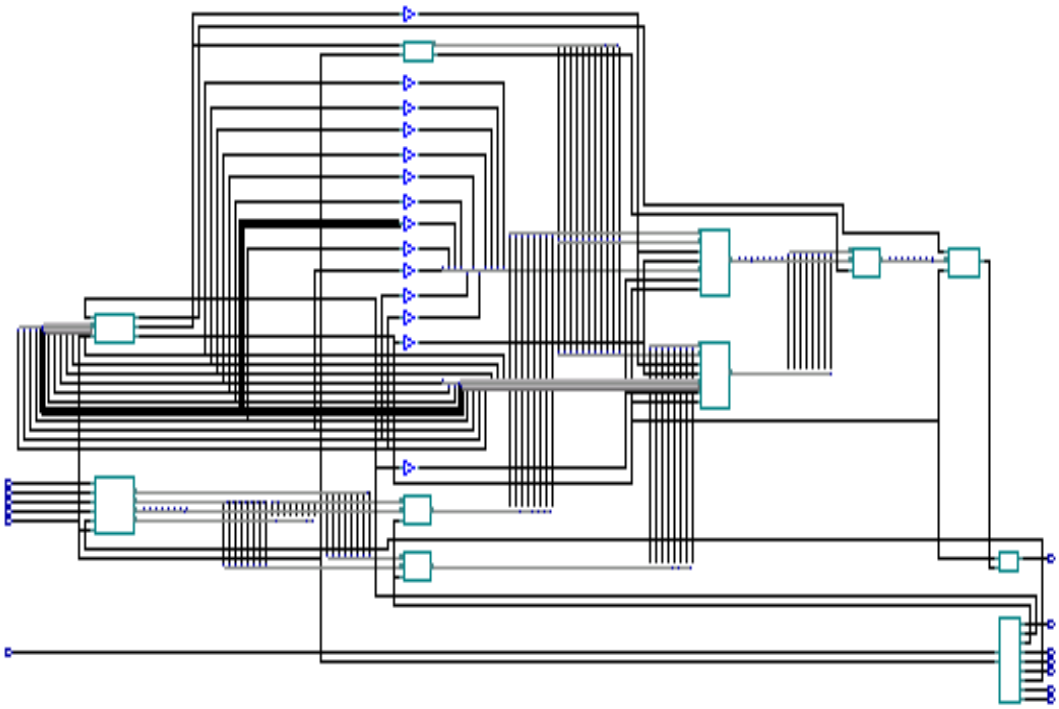
Critical path #1, (path slack = 14.1):

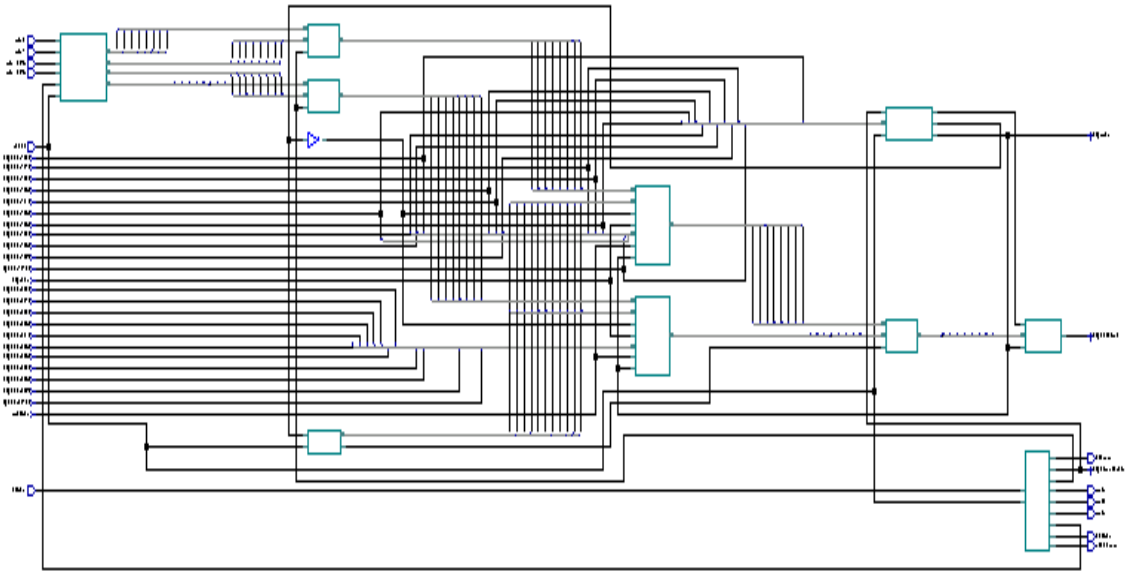
NAME	GATE	ARRIVAL	LOAD
reset/	0.00	0.00 up	1.22
reset_ibuf/combout	apex20_io_input_none_from_pin	5.14 5.14 up	3.50
ix658/combout	apex20_lcell_normal	2.33 7.47 up	1.22
sclock_obuf/padio	apex20_io_output_none_none	3.39 10.86 up	1.22
sclock/	0.00	10.86 up	0.00
data arrival time		10.86	
data required time (default specified)		25.00	

data required time	25.00
data arrival time	10.86
	---
slack	14.14

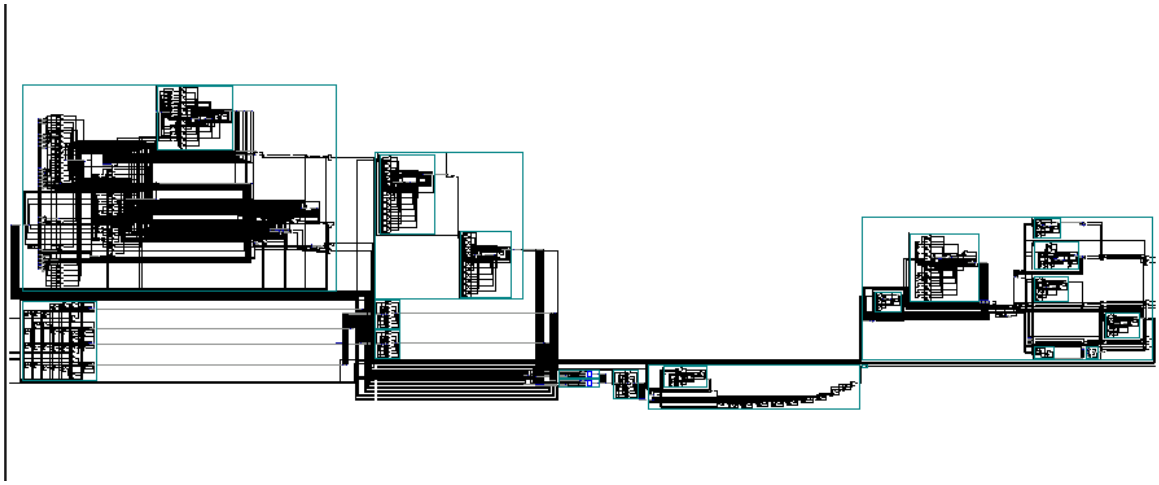
5.2.2 Schematic views:

The schematic views and hierarchical view of design with blocks are shown below.





Hierarchical view:



5.3. Post-synthesis simulation results

Post synthesis simulation results are also same as pre –synthesis simulation results (which are shown above) but with some delay. The post synthesis simulation is done by adding all gate delays to back annotated file (adding ***.sdf*** file).

Chapter-6

INTRODUCTION

Over the past decade, developments in image-sensor technology brought new image capture equipment to the market. Camcorders and Digital Cameras are the well known products of this development. At the same time due to improvements in wireless and portable electronics, there is increasing demand for miniaturized, low-power and cost efficient imaging systems. This trend has led to a shift in technology from Charge Coupled Device (CCD) based image sensors to Complementary Metal Oxide Semiconductor (CMOS) based imagers. This is mainly because CMOS-based image sensors offer the potential opportunity to integrate low-power signal processing circuitry on-chip and hence reduce component and packaging cost. There is also great demand for wide dynamic range, high fill-factor and high resolution image sensors in some applications such as spectroscopy and fingerprint sensors. These specific applications employ scanning and swiping methods to capture images and hence a linear image sensor is preferred to area format image sensor. Digital interface of the imager chip is essential to overcome system level issues such as signal integrity. To implement digital interface to the imager chip requires an on-chip analog to digital converter. This research presents a new linear image sensor architecture and circuit techniques that lead to low power, wide dynamic range, high fill-factor and high resolution linear image sensor with digital interface.

Image Sensor Terminology

The definition of most commonly used terms in solid state image sensors is given below **Charge-coupled device (CCD):** CCD is a charge transfer device that collects light in pixels and then uses clock pulses to shift the charge along a chain of pixels.

Correlated double sampling (CDS): CDS is the technique of taking two samples of a signal closely spaced in time and subtracting the first signal from the second to remove the low frequency correlated noise.

Dark current: The signals charge that the pixel collects in the absence of light divided by the integration time.

Dynamic range: It is ratio of the saturation signal to the root mean square (rms) noise floor of the sensor.

Fill factor: It is the ratio of light sensitive area to the pixels total area.

Fixed pattern noise (FPN): It is the noise due to mismatch in the properties – transistor thresholds, gain, parasitic capacitance, pixel geometry - of pixels.

Integration time: It is the time that the sensor is exposed to light to integrate the photo generated signal charge.

Micro lens: It is a lens etched directly on the chip's surface for each pixel to focus the light on to the light sensitive area of the pixel.

Photocurrent/photocharge: It is is current/charge generated due to the exposure of silicon to light.

Photo site: It is the portion of the silicon that functions as a light-sensitive area.

Pixel: It is discrete photosensitive cell that collects and holds a photo charge.

Quantum efficiency: It is the ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area.

Chapter-7

GENERAL DESCRIPTION OF ROIC

Even though CMOS Image Sensors appeared in 1967, CCDs have prevailed since their invention in 1970. However the major problem with CCDs is that they are manufactured in foundries using specialized and expensive processes that can only be used to make CCDs, and therefore cannot take advantage of economies of scale general purpose fab. Meanwhile, recent advances in the CMOS technology for microprocessors and Application Specific Integrated Circuits (ASICs) to the development of highly integrated image sensors with on chip signal processing algorithms, sensor array controls and image processing. Also, CMOS is by far the most common, lowest cost and highest yielding process in the world. Using the same process to manufacture CMOS image sensors cuts cost dramatically because of the fixed costs of the plant are spread over a much larger number of devices. As a result of this economy scale, the cost of fabricating a CMOS wafer is lower than the cost of fabricating a similar wafer using the more specialized CCD process

7.1 Block Diagram of ROIC

The conceptual block diagram of ROIC with 8×8 array of unit cells is shown in **Figure7.1**. For clarity, **Figure7.1** can be divided in three sections

- Unit cells which constitute array
- Post unit cell signal processing circuitry
- Digital circuitry for synchronizing the entire activity.

Array consists of 8 columns and 8 rows and surrounding this array is row and column select logic which controls row selection and analog multiplexer respectively. Placement of post unit cell circuitry only at column level reduces space and power utilization, which is one of the major goals in design of ROIC. As a row or line is selected the integrated and held voltage in 8 unit cells of that line drops to column amplifiers through their respective column buses.

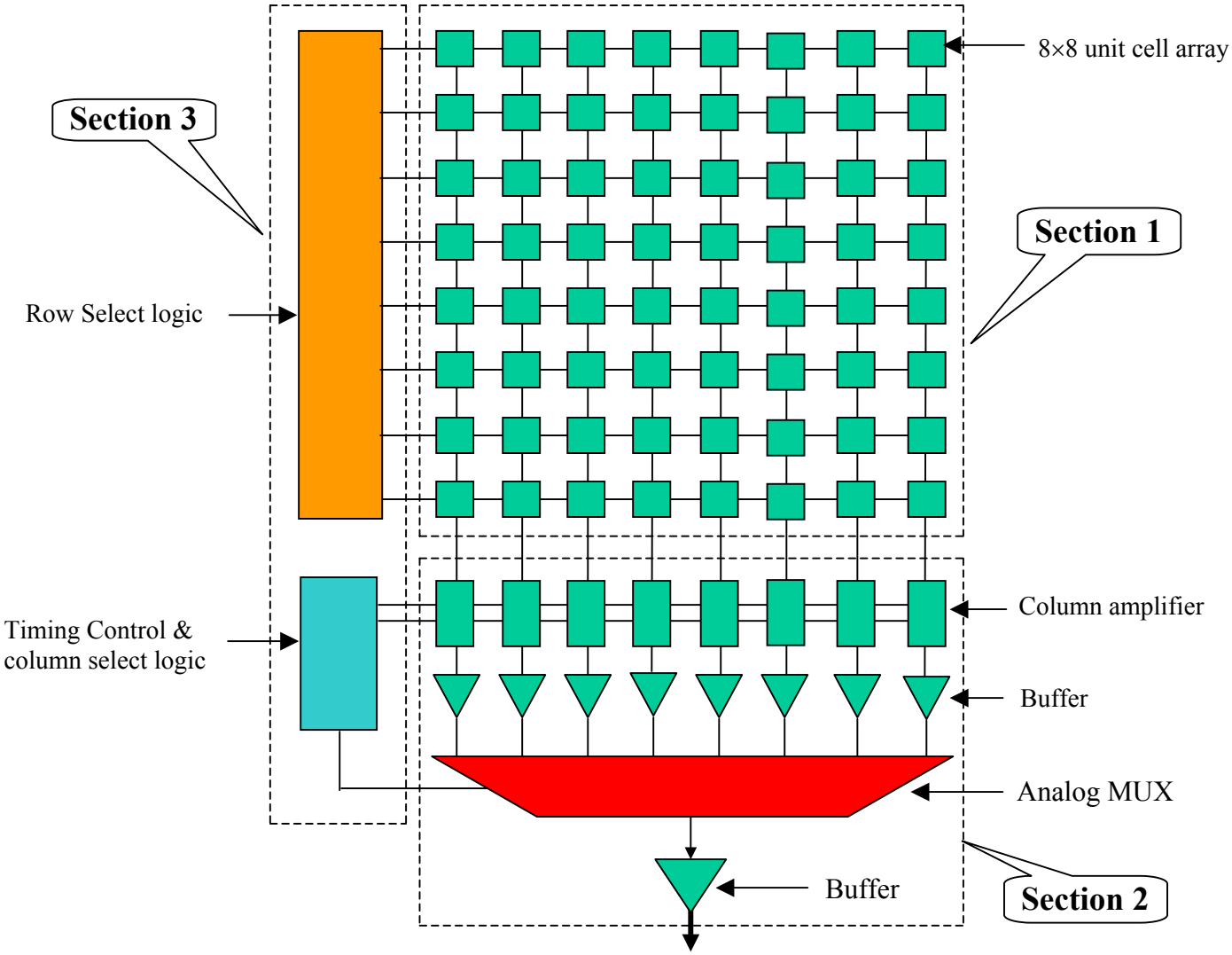


Figure 7.1: Block Diagram of ROIC

7.1.1 Unit cell

Unit cell is basically a trans-impedance amplifier, which converts the input photocurrent from sensor to voltage through an integrating capacitor. There are various architectures to construct unit cell. One of the prime parameter in deciding about architecture is area. Apart from area some of the other governing parameters for unit cell are:

- Stability of detector bias
- Low input referred noise
- Low input resistance (Related with injection efficiency)
- High linearity and
- High dynamic range.

It's apparent that design finalization of unit cell is governed by performance optimization for all of these parameters.

Key to the development of the ROIC has been the evolution in input preamplifier (unit cell) technology. This evolution has been driven by increased performance requirements and silicon processing technology improvements. There various architecture for unit cell like Capacitive Trans impedance Amplifier (CTIA), Current Mirroring Integration (CMI) and Direct Injection (DI). The one of various architectures, Direct Injection circuit for unit cell is shown in **Figure7.2.** This architecture has advantage of small area but Detector bias is unstable

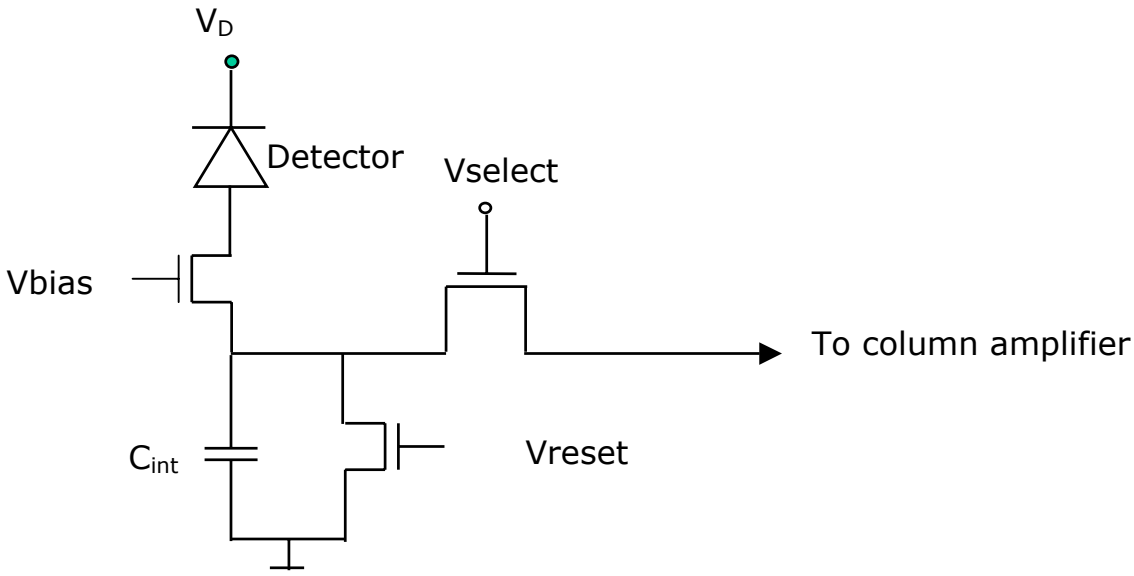


Figure 7.2: Direct Injection (DI) architecture for unit cell

7.1.2 Post unit cell signal processing circuitry:

This circuitry will consist of Column amplifier, Buffer, Analog multiplexer, Output buffer, Bias and reference generator. Column amplifier will basically be a offset compensated switched capacitor amplifier block with programmable gain, correlated double sampling (CDS) circuit and background subtraction capability. It will be followed by a buffer with the load of 10pf, driving the analog multiplexer, which in turned is connected to last analog buffer whose output load is resistor of 500K in parallel to capacitor of 20pF. Data is output in serial fashion.

The main sources of errors in the switched capacitor circuits are: Offset voltage of opamps, Clock feedthrough and charge injection of CMOS switches.

The offset voltage problem can be overcome by "auto zeroing" technique, which is very effective and easy to implement in the switch-cap design. In this technique, an opamp is connected in unity gain voltage follower mode, by shorting the inverting terminal to the output. Now the output will be at offset voltage. This offset is sampled on a capacitor and used to cancel the offset by connecting it in opposite polarity in next cycle.

Clock feedthrough is due to the coupling of the clock signal to the high impedance node of the switch by gate to source/drain capacitance. Although techniques are available to minimize feedthrough, this is a limiting factor of the accuracy of the switched capacitor circuits.

Charge injection is related with the fact that when CMOS switch gets OFF, it dumps its channel charge on both source and drain nodes as per the impedance present on these nodes. By carefully adjusting the sizes of NMOS and PMOS in switch this effect can be minimized.

7.1.3 Digital circuitry:

The basic aim of this circuitry is to synchronize the entire activity in ROIC. The digital control and timing circuit generates the timing clocks for the different switches. The different phases required for all the switches are generated by this block. Usually switches should be turned OFF and ON without overlap (break before make). This non-overlapping clock requirement is also met by special delay circuits. The logic circuit that is used to select rows and columns can be developed by using either a shift register or a decoder. The pixels are read out to the vertical column busses that connect the selected row of pixels to column parallel analog signal processing blocks. Here this has 8X8 array of pixels, so the clock speed for column selection is eight times faster than that of row selection clock.

The logic circuit that is used to select rows and columns, to readout pixels data can be developed by using either a *shift register* or a *decoder*. The pixels are read out to the vertical column busses that connect the selected row of pixels to column parallel analog signal processing blocks.

7.2 Integration Modes

There are tow types of integration modes for a pixel, *integration then read* and *integration while read* modes.

7.2.1 Integrate then Read Mode (ITR)

It is also called "Snapshot" mode and is one of the prime feature of ROIC. Here all unit cells of the array integrate simultaneously or in other words begin and end their integration at the same time. This is followed by readout of array, row by row. To achieve the snapshot mode, integration and holding capability is incorporated in every unit cell of ROIC. The integration process is controlled by the FSYNC clock, and this allows both Integrate-While-Read and Integrate-Then-Read modes of operation. **Figure7.3** shows a timing pattern for operation of the Integrate-Then-Read mode. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed immediately by a sequence of LSYNC pulses that produce a readout sequence. Note that in this case, the FSYNC clock remains high until the readout sequence has been completed. In this case, the integration time occurs after the readout time, resulting in a frame time that is approximately equal to the readout time plus the integration time. This results in a lower maximum frame rate and integration time duty cycle for a given window size.

$$T_{FRAME} = T_{READ} + T_{RESET} + T_{INT}$$

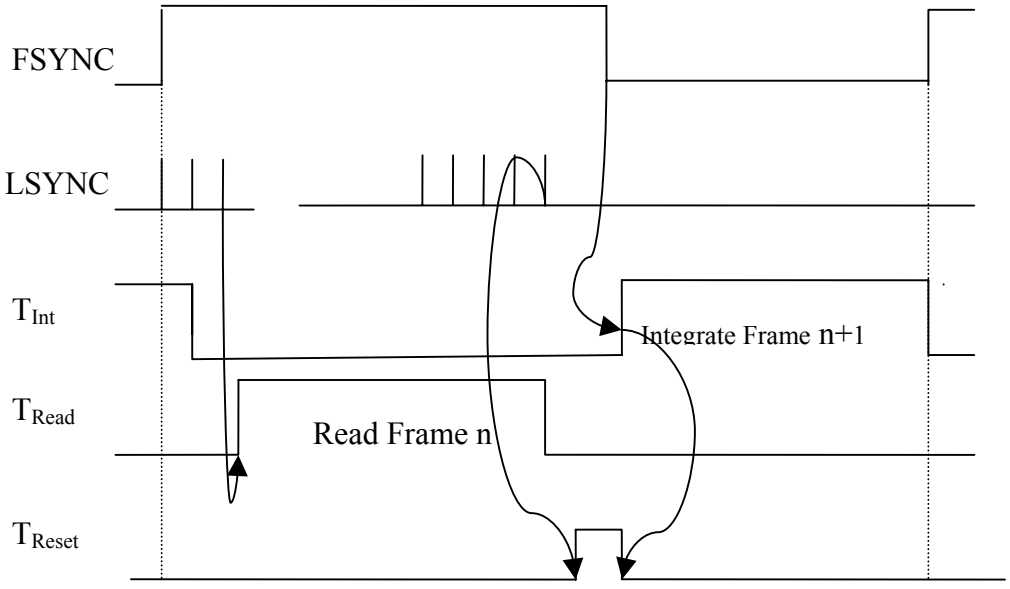


Figure 7.3: Timing diagram for Integration Then Read Mode

7.2.2 Integrate While Read Mode (IWR)

It can also be thought of as "Rolling Wave" mode. Here array is continuously integrating even during the readout. In this mode first row is addressed, readout and reset while the other 7 rows integrate. The second row is then addressed, readout and reset as the other 7 rows integrate. When this process has cycled through all 8 rows it simply restarts at the first row after some user defined delay time, if any. Although pixels in different rows do not begin and end their integration at the same time, the total integration time is the same per pixel. A timing pattern for the Integrated-While-Read operation is shown in **Figure7.4.** The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed by a series of LSYNC (LSYNC controls the synchronization of the readout of each individual line) pulses that produce the readout sequence. For this case the integration time occurs during the readout time, allowing for the greatest possible frame rate and integration time duty cycle (where integration time duty cycle = TInt / TFrame) for a given window size.

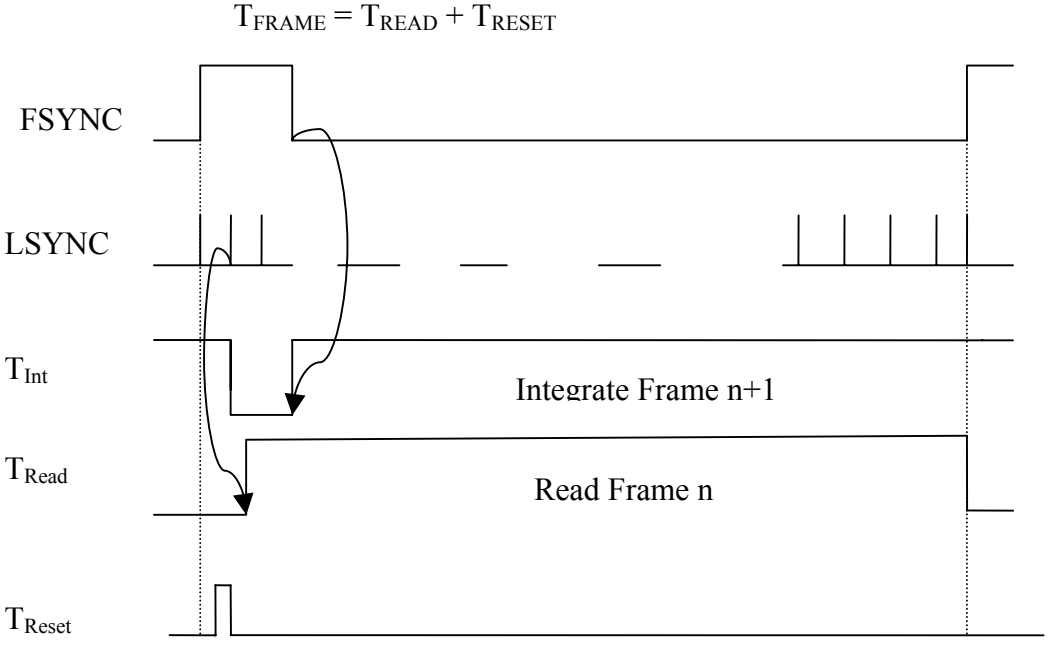


Figure 7.4: Integration while Read mode

Chapter-8

DESIGN

The block diagram of ROIC is divided into three sections, those are Unit cells which constitute array, Post unit cell signal processing circuitry and Digital circuitry for synchronizing the entire activity as explained above. In the post unit cell circuitry there is buffer after column level block. This buffer is driving the analog multiplexer with the load of 10pf.

The schematic diagram of the opamp to be used in column level ***offset compensated Switched Capacitor Amplifier*** as well as in ***buffer*** is shown in **Figure8.3**. A two stage operational amplifier (***opamp*** shown in figure) in unity gain configuration is used as the buffer. The opamp is designed for high gain, wide common mode input range and large output swing.

8.1 OPERATIONAL AMPLIFIER

8.1.1 Introduction

The operational amplifier is one of the most important circuits used in analogue and mixed signal design. Early opamps were constructed from discrete components (vacuum tubes and then transistors, and resistors), so their costs were prohibitively high. In the mid 1960s the first integrated circuit was produce. This unit was made up of relatively large number of transistors and resistors on same silicon chip. The one of the reasons for popularity of opamp is its versatility; equally important is the fact that the IC opamp has characteristics closely approaching to that of assumed ideal opamp.

Ideal operational amplifier

The symbol of opamp is shown in **Figure8.1**. It has two input terminals and output terminal in signal point of view. Terminals *Vin+, Vin-* are input terminal and *Vout* is output terminal. The power supplies to this opamp are VDD and VSS.

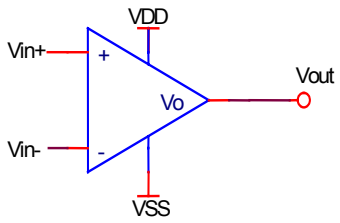


Figure 8.1: circuit symbol for the opamp

The opamp is designed to sense the difference between the voltages signals applied at its input terminals, the value at output is difference multiplied by gain.

Vout = A (Vin+ - Vin-) where **A** is gain of opamp.

The ideal opamp is not supposed to draw any input current, that is the signal current into terminal *Vin-* and signal current into terminal *Vin+* are both zero. In other words the *input impedance of an ideal opamp is supposed to infinite*.

The output voltage at output terminal and ground is always equal to difference of input signals multiplied by its gain; it is independent of current that may be drawn from *Vout* into load impedance. So the *output impedance of an ideal opamp is supposed to be zero*.

The opamp is only responds to the difference between input signals and hence it ignored the common to both inputs. We call this property as common mode rejection. For ideal opamp it is zero common mode gain or equivalently *infinite common mode rejection ratio*.

The ideal opamp has a gain that remains constant down to zero frequency and up to infinite frequency. That is ideal opamp will amplify signals of any frequency with equal gain so ideal opamp has *infinite band width*.

The Characteristics of ideal opamp are

- Infinite input impedance
- Zero output impedance
- Zero common mode Gain (infinite common mode rejection ratio)
- Infinite open loop gain
- Infinite bandwidth
- Infinite PSRR
- Zero offset

opamp with vastly different levels of complexity are used to describe to realize functions ranging from dc bias generation to high-speed amplification or filtering. We loosely define the Op amp as a "*high-gain differential amplifier"*, by high means a value that adequate for applications. The basic specifications to design op amp are open loop Gain, Gain Bandwidth, Output voltage swing, PSRR, Small signal Settling time, Large signal Slew Rate, CMRR, Phase Margin, Power dissipation, Noise, Common-mode input range, Silicon area.

8.1.2 Design Approach

The basic Design approach of Op-amp is shown in **Figure8.2**. The different stages of Design are Specifications, Design, simulations (Analysis) and modification if required.

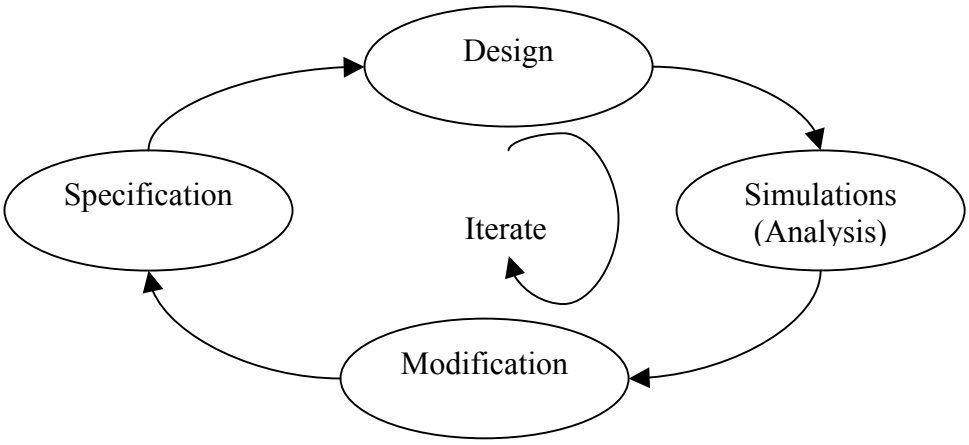


Figure 8.2: Design Approach of opamp

a. Specifications:

The Basic Specifications of opamp are

- Open loop Gain (Av)
- Gain Bandwidth (GBW)
- Output voltage swing
- Phase Margin (PM)
- Gain Margin (GM)
- Power Supply Rejection Ratio (PSRR)
- Small signal Settling time
- Slew Rate
- Common Mode Rejection Ratio (CMRR)
- Power dissipation
- Noise
- Common-mode input range

b. Design

The design process involves two distinct activities:

Architecture Design

- Find architecture already available and adapt it to present requirements
- Create a new architecture that can meet requirements

Component Design

- Design transistor sizes
- Design compensation network

If available architectures do not meet requirements, then an existing architecture must be modified, or a new one is designed. Once a satisfactory architecture has been obtained, then devices and the compensation network must be designed. The different types of popular architecture of opamp are Telescopic, Folded Cascode, Two Stage and Gain Boosting.

Design the opamp by using given specifications (sizing of Transistors) then select the compensation network to meet the required specifications. The different types of compensations are

1. *Miller compensation* -Use of a capacitor feeding back around a high-gain, inverting stage.
   - Miller capacitor only
   - Miller capacitor with a unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
   - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.

2. *Self compensating* - Load capacitor compensates the opamp.

3. *Feed forward* - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

c. Simulation and Analysis:

The Design begins with hand calculations based on first order equations for selected architecture (sizing of transistors). Compensation components are also sized in this step of the procedure. After each device is sized by hand, a circuit simulator is used to fine tune the design.

The different types of simulations are dc, ac and transient performance. We simulate the designed architecture with different types of simulations and understand the how the variation parameter influence the performance. This process is continued until require specifications are met and no more modifications are required.

8.1.3 Design of Two Stage OPAMP:

The basic architecture (Schematic) of Two-Stage opamp is show in **Figure8.3**.
In the design of the amplifier, the bulks were tied to the sources i,e. **Vsb=0**

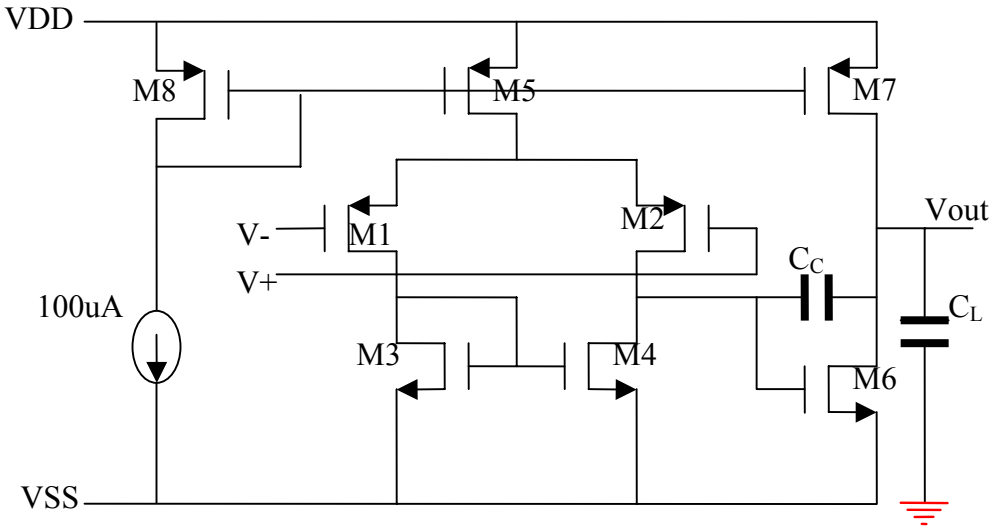


Figure8.3: Schematic Diagram of Two-Stage Op-Amp

In the schematic diagram of two stage opamp, M1–M5 forms the differential amplifier – note P-type devices have been used as input to differential due to improve in slew rate, Unity Gain Bandwidth and less flicker (1/f) noise. M5 is the current source for the differential amplifier and has been initially set in our case at 200uA, thus giving 100uA down

each arm of the differential amplifier. The current mirror formed by M3 and M4 combine the differential output voltage to give a single voltage output feeding into M6. M6 is a simple current source inverter (M7 is the current source load for this amplifier) with miller compensating capacitor Cc. The architecture uses miller compensation capacitor (Cc) as compensation network and class A as output stage. So it is also called **two stage miller class A amplifier.**

In the coming section the basic features of a two-stage opamp, equations required to meet specific design goals and most important of all the frequency response design drivers of opamp are described.

a. Basic Design Drivers & Calculations

The following equations are used to design this opamp structure. The following relations are used in these calculations of design drivers.

$g_{m1} = g_{m2}$,

$g_{ds2} + g_{ds4} = G_1 = 1/R_1$ where $R_1 = r_{02} \parallel r_{04}$ and

$g_{ds6} + g_{ds7} = G_2 = 1/R_2$ where $R_2 = r_{06} \parallel r_{07}$

Slew Rate (SR):

The slew rate is the non-linear ability of the op-amp to respond to a large stepped impulse on the input. Ideally a square waveform input should remain a square wave after amplification. The limitations of the opamp cause the waveform edges to become ramped. The slew rate is specified as a voltage attained after a preset time and is dependant on the tail current through M5 in the differential amplifier. The tail current is determined from equation Slew Rate (SR) $= \frac{I5}{C_C}$. If SR is not given then I_5 = 10* settling time * Cc.

Gain Bandwidth (GB):

The gain bandwidth is a function of the differential amplifier stage conductance (g_{m1}) and the miller compensation capacitor (Cc).

$$\text{Gain-Band Width (GB)} = \frac{g_{m1}}{2*\pi*C_C}$$

Gain (Av):

First Stage Gain (A_{V1}) = - g_{m1}* R1

Second Stage Gain (A_{V2}) = - g_{m6}* R1

Overall Gain (A_V) = A_{V1} * A_{V2}

Positive CMR (Vin max):

The positive input common mode range (Vin max) is the maximum voltage for which the transistor M5 is also in saturation region.

Positive CMR $Vin\ \max = VDD\ - Vsd\ 5 - Vgs\ 1$

$$Vin\ \max = VDD\ - \sqrt{\frac{I\,5}{\beta 5}} - Vov\ 1 + \left|Vt\ 1\right|$$

Negative CMR (Vin min):

The negative input common mode range (Vin min) is the minimum voltage for which the transistors M1 & M2 are always in saturation region

Negative CMR $Vin\ \min = VSS\ + Vgs\ 3 + Vds\ 1 - Vgs\ 1$

$$Vin\ \min = VSS\ + \sqrt{\frac{I1}{\beta 1}} - \left|Vt\ 1\right| + Vt\ 3$$ Where Vov = V_{GS}-V_T and $\beta = \mu Cox * \left(\frac{W}{L}\right)$

Capacitances calculation:

Input load capacitance (C1): This capacitor consists of the parasitic capacitors around M2, M4 & M6. In most cases the bulk will be connected to VSS or VDD, which will be AC ground, so in fact these capacitors will all add together that is

C1 = Cgd4+Cdb4+Cgd2+Cdb2+Cgs6

Output load capacitance (C2): This capacitor consists of the parasitic capacitors around M6, M7 and load capacitance of opamp (C_L). In most cases the bulk will be connected to VSS or VDD, which will be AC ground, so in fact these capacitors will all add together that is

C2 = Cgd7+Cdb7+Cdb6+C_L =~ C_L

Where C_L is the Load Capacitance and C_C is the Compensation Capacitance.

All these parasitic capacitors generate poles in the frequency response of the op-amp especially where the capacitor is connected to a high impedance point of the circuit, generated a large time constant (low frequency pole).

Output Pole (P2) = $\frac{-g_{m6}}{2*\pi*C_C}$ and Miller pole (P1) = $\frac{-G_1 G_2}{g_{m6}*2*\pi*C_C}$

RHP Zero (Z) = $\frac{g_{m6}}{2*\pi*C_C}$

Phase Margin (PM):

Phase Margin is calculated from ac simulation graph, it is the value at which gain of opamp is unity (i,e. at unity gain frequency). This can be formulated from poles and zeros of circuit.

$$PM = 180 - \tan^{1}\left(\frac{GB}{P1}\right) - \tan^{1}\left(\frac{GB}{P2}\right) - \tan^{1}\left(\frac{GB}{Z}\right)$$

In order for the opamp to be stable is to have a reasonable phase margin (typically ~ 60 degrees) at the point where the gain response has fallen to 0dB (feedback factor = 1).

The important formulae used in Design are shown in following table

$g_{m1} = g_{m2}$,

$g_{ds2} + g_{ds4} = G_1 = 1/R_1$ where $R_1 = r_{02} \parallel r_{04}$ and

$g_{ds6} + g_{ds7} = G_2 = 1/R_2$ where $R_2 = r_{06} \parallel r_{07}$

Slew Rate (SR) = $\frac{I5}{C_c}$

First Stage Gain (A_{V1}) = - g_{m1}* R_1, second Stage Gain (A_{V2}) = - g_{m6}* R_2

Overall Gain (Av) = A_{V1} * A_{V2}

Gain-Band Width (GB) = $\frac{g_{m1}}{C_c}$

Output Pole (P2) = $\frac{-g_{m6}}{C_c}$

RHP Zero (Z) = $\frac{g_{m6}}{C_c}$

ICMR Max = $Vin\ \max = VDD - \sqrt{\frac{I5}{\beta 5}} - Vov\,1 + Vt\,3(\min)$

ICMR Mini. = $Vin\ \min = VSS + \sqrt{\frac{I1}{\beta 1}} + |Vt\,1| + Vt\,3$

C1 = Cgd4+Cdb4+Cgd2+Cdb2+Cgs6, C2 = Cgd7+Cdb7+Cdb6+C ~= C_L

Where C_L is the Load Capacitance and C_C is the Compensation Capacitance,

Vov=V_{GS}-V_T and $\beta = \mu Cox * \left(\frac{W}{L}\right)$

b. Design Steps

This design procedure assumes that the gain at dc (*Av*), unity gain bandwidth (*GB*), Input Common mode range (*Vin* min and *Vin* max), load capacitance (*CL*), slew rate (*SR*), settling time (*Ts*), output voltage swing (*Vout* max and *Vout* min), and power dissipation (*Pdiss*) are given.

1. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

2. From the desired phase margin, choose the minimum value for *Cc*, i.e. for a 60° phase margin we use the following relationship. This assumes that Z>= 10*GB*. i,e. $C_C > 0.22C_{L.}$

3. Determine the minimum value for the "tail current" (*I*5) from the largest of the two values.

$$I5 = SR * C_C$$

If settling time is given then $I5 = 10 * \left[\frac{VDD + VSS}{2 * Ts}\right] * C_C$

4. We can calculate W/L of M5 is calculated from maximum input CMR (Vin Max),

$$\left(\frac{W}{L}\right)_5 = \frac{I5}{K_5'\left[VDD - Vin\ \max - Ov1 + |Vt1|\right]^2}$$

5. We can calculate W/L of M1 (M2) is calculated from Unity Gain Bandwidth (GB)

$g_{m1} = GB * C_C$ then $\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1}^{\ 2} * C_C}{K_1' * I5}$ where $I5 = 2I_1$

6. We can calculate W/L of M3 (M4) is calculated from minimum input CMR (Vin min),

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I5}{K_3'\left[Vin\ \min - VSS + |Vt1| - Vt3\right]^2} \quad \text{where } I5 = 2I_3$$

7. Find g_{m6} and W/L of M6 by the relationship relating to phase margin, load, and compensation capacitor in the balance condition.

$g_{m6} = 0.22 * g_{m1} * (C_L/C_C)$ then $\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_3 \frac{g_{m6}}{g_{m3}}$

8. We can calculate W/L 0f M5 from the relation $\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_5 \frac{\left(\frac{W}{L}\right)_6}{2*\left(\frac{W}{L}\right)_4}$

Where $K_P' = \mu Cox$ of Transistor Mp

From the above equation of M6 and M4 we can calculate I6.
Power dissipation P_{diss}= (I5+I6)* (VDD+VSS).

9. If the gain specification is not met, then the currents, I5 and I6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they have been satisfied. If the power dissipation is too high, then one can only reduce the currents I5 and I6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

10. Simulate the circuit to check to see that all specifications are met.

8.2 AUTOZEROING TECHNIQUE (AZ)

8.2.1 *Introduction*

In the block diagram of ROIC, shown in Figure 7.1, there is a column level switched capacitor amplifier block. The SC amplifier is implemented using opamp, explained in above section.

The opamp with MOS input transistors, the opamp input current at low frequencies can indeed be made extremely small; however, the input voltage of practical opamp is uaually significantly large, since it is affected by several non-ideal effects such as noise (most importantly 1/f noise and thermal noise) and input referred DC offset voltage. There are different techniques to reduce those non ideal effects of opamp. The two important basic techniques use to reduce dc offset and noises are ***Autozeroing (AZ)*** *and* ***Chopper Stabilization (CHS).*** The distinction between these two techniques is autozeroing technique is sampling technique where as chopper stabilization technique is modulation technique. The technique which is a particular case of autozeroing technique is correlated double sampling (CDS) is also used to reduce those non ideal effects, in this CDS technique noise and offset are sampled twice in each clock period.

8.2.2 Basic Principle:

The basic idea of AZ is sampling the unwanted quantity (noise and offset) and then subtracting it from instantaneous value of the contaminated signal either at the input or the output of the opamp. The cancellation ia also done at some intermediate node between input and the output of opamp.

The AZ process requires at least two phases, sampling phase (Ø1) and signal processing phase (Ø2). The two clock phases are non overlapping phases (two phases never have high value at any time). A sampling phase (Ø1) during which the offset voltage Vos and the noise V_N are sampled and stored and a signal processing phase (Ø2) during which the offset free stage is available for operation. In this AZ, during phase Ø1, the amplifier is disconnected from the signal path, it inputs are shorted to common-mode voltage. In the phase Ø2, the input terminals of amplifier are connected to signal for amplification.

The AZ technique and Chopper stabilization techniques are implemented with SC amplifier (with MOS switches). In the next section the different non ideal effects in switches are described. The MOS switch non idealities include a non zero on-resistance. However, the most important factors affecting residual offset are:

- Clock feed through
- Channel charge injection
- Sampled noise
- Leakage current

The switch (sample and hold circuit) using n-MOS is shown in **Figure8.4** below. When a switch is turned off, the charges in its conducting channel are released and removed through the MOS source and drain terminals (the fraction of charge that flows to substrate can generally be neglected). The partitioning of these charges between source and drain depends mainly on the ratio of the total capacitor C_h at the switch drain and at the source (C_p, total parasitic capacitance) and on the so called switching parameter determined mainly by transistor on resistance R_{on} and the slope of clock signal to the gate. The channel charge is split equally between source and drain only if either the capacitances C_p and C_h are equal, or the switching transition time is much less than the $R_{on}C$ time constant. In general for slow falling clock signals, the channel charge is divided unequally between source and drain, going mostly to the terminal showing lower impedance. In the case where the source or drain capacitance much larger than the other, most of the charge flows to the larger capacitance. The charge q_{inj} injected into the hold capacitor is that difficult to predict accurately.

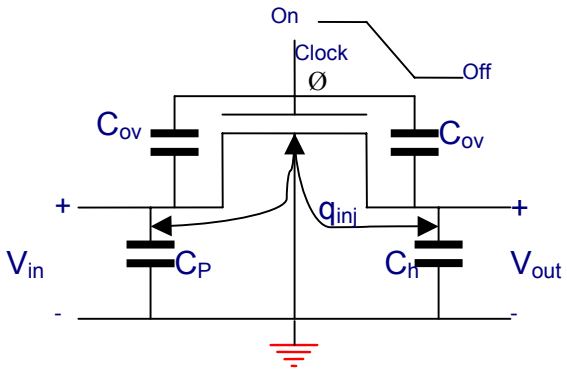


Figure 8.4: Basic sample and hold (S/H) circuit

There are, however circuit techniques which can reduce the effect of charge injection are,

1. Making capacitance C_p much larger than C_h (by adding extra capacitor) and choosing switching parameter smaller then one (slower clock transition) in order to attract most of the channel charge to C_p, reducing qinj almost to zero. This technique of course sets a limit on the maximum clock frequency.
2. Making C_p equal to C_h to force the channel charge to split equally between source and drain, and then compensating the injected charge by adding half-sized dummy switches.
3. Using a very short transition time to force the channel charge to split equally between source and drain and then compensating the injected charge by half-sized dummy witch. This half-sized technique depends on a proper layout in order to insure a good matching and first-order insensitivity to doping gradient.
4. Using two complementary switches in such a way that the charges released by one switch are absorbed by the complementary device building block its channel.

The last technique using two complementary switches is very simple and used to implant the switches in further offset free (AZ) techniques. This technique rather inefficient, since the matching between the channel charges of n-MOS and p-MOS devices are poor.

Each time the switch is opened, an additional charge due to the thermal noise of switch channel will be sampled on the hold capacitor Ch. The variance of the noise charge is equal to KTC_h, corresponding to sampled noise voltage variance equal *to* KT/C_h.

For very long hold time and/or for very high temperature operation, the leakage current I_{leak} associated with the drain to bulk junctions also has to be taken into account, since it will discharge the hold capacitor and thus introduces an additional error into the sample voltage.

The total error in the sample voltage across the hold capacitor due to clock feed through, charge injection, sampled noise and leakage current.

$$Verror = \alpha \frac{C_{OV}}{C_{OV} + C_h} Vswing + \frac{q_{inj}}{C_h} + \sqrt{\frac{KT}{C_h}} + \frac{I_{leah} T_h}{C_h}$$

Where, *Vswing* is the swing of clock signal, α is attenuation factor ($\alpha < 1$),

I_{leak} is the leakage current, *Cov* is overlapping capacitance.

In practical cases the second term is dominates, $Verror = \frac{q_{inj}}{C_h}$

8.2.3 Different offset cancellation techniques:

The different techniques to cancel the offset are Open-Loop cancellation, Closed-Loop cancellation, multistage offset storage principle, closed-loop cancellation using an auxiliary input port and continuous- Time AZ amplifiers. In the next section the first two techniques are described.

a. The Open-Loop Offset cancellation Technique:

The simplest way to implement offset cancellation is to sample the offset at the output of amplifier as shown in **Figure8.5.** This technique is some times called Output Offset Storage (OOS). Here the switches are implemented with CMOS transistors.

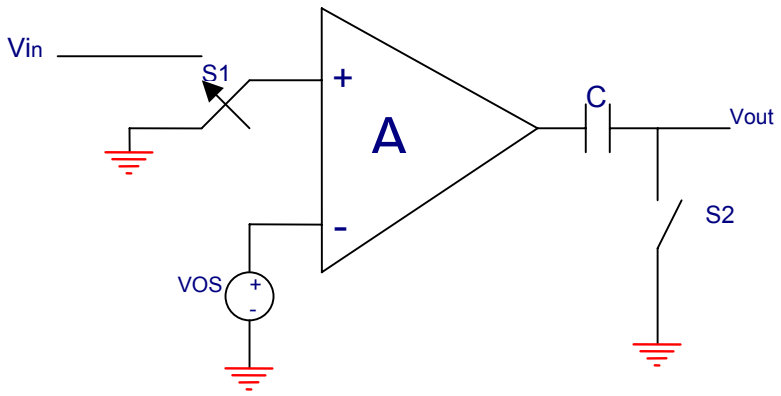


Figure 8.5: Open-Loop offset cancellation technique

During AZ phase, the input switch S1 and the output switch S2 are both connected to ground. Switch S2 is opened and offset voltage is multiplied by amplifier gain A remains stored in capacitor *C*. the stored output is altered by an error voltage q_{inj}/C cause by charge injection at the opening of switch S2. After the AZ phase, the input terminal of the amplifier is connected back to the signal by switch S1. The input referred residual offset is thus limited by the charge injection q_{inj}.

$$V_{os-res} = \frac{1}{A}\frac{q_{inj}}{C}.$$

This technique is obviously effective only if the amplifier does not saturate during the offset sampling phase. This requires that the output referred offset remain smaller than the minimum saturation voltage. This is possible only if the amplifier gain is relatively small (less than ten).

b. The Close-Loop Offset Cancellation Technique:

The Open-Loop offset cancellation principle is not well suited to high-gain amplifiers. It is usually preferable there to sense the amplifiers offset in a closed-loop configuration as shown in **Figure8.6.**

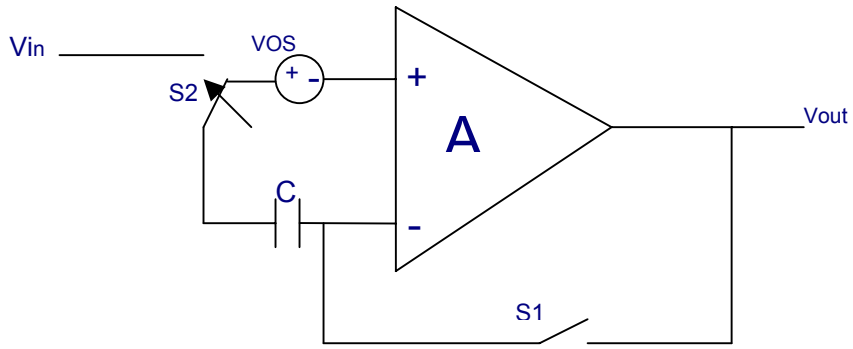


Figure 8.6: Closed-Loop offset cancellation technique

During the sampling phase the amplifier is disconnected from the signal path and connected in a unity-gain configuration. Assuming that the open-loop gain A of the amplifier is much larger than one, the voltage Vc obtained across the capacitor C after the amplifier has settled is almost equal to its offset voltage Vos.

$$Vc = \frac{A}{1+A} Vos \cong Vos$$

This voltage (plus and additional error q_{inj}/C caused by the charge injection occurring when switch S1 is opens) stored across the capacitor C. the charge will remain trapper on capacitor C since the input current of the amplifier is zero for a MOS input stage, and hence capacitor behaves like a floating voltage source equal to Vos. After sampling phase, offset compensated stage is available for amplification, so in this phase the switch S2 is connected again to the signal path. The residual offset can then be found

$$V_{os-res} = Vos - Vc \cong \frac{Vos}{A} + \frac{q_{inj}}{C} \cong \frac{Vos}{A}$$

8.2.4 Implementation of Close-Loop offset cancellation:

There are number of ways to implement the Close-Loop Offset cancellation Technique. In this section implementation of offset cancellation technique using ***non-inverting*** and ***inverting*** switch capacitor voltage amplifier circuits are explained.

In the implementation of Switch capacitor circuits, the following things are important

- Always use the non-overlapping clocks to OFF/ON the witch. (*Ø1, Ø2).*
- The clock frequency is kept roughly ten times greater than the signal frequency.
- The output signal (Vout) is relevant in only one clock set (either *Ø1 or Ø2)*
- In the other clock set the output signal (Vout) is goes to some fixed level.
- For higher the clock frequency, more fast opamp (less settling time) is needed.

a. Non-Inverting SC Voltage amplifier:

The schematic diagram of offset cancellation using non-inverting SC voltage amplifier is shown in **Figure8.7.** The two clocks (*Ø1, Ø2*) are used to Off/ON the switches are non-overlapping clocks (these two clocks never have high value at a time).

The gain of Switched Capacitor Amplifier is decided by ratio of ***C1/C2.***

$$Gain = \frac{C1}{C2}$$

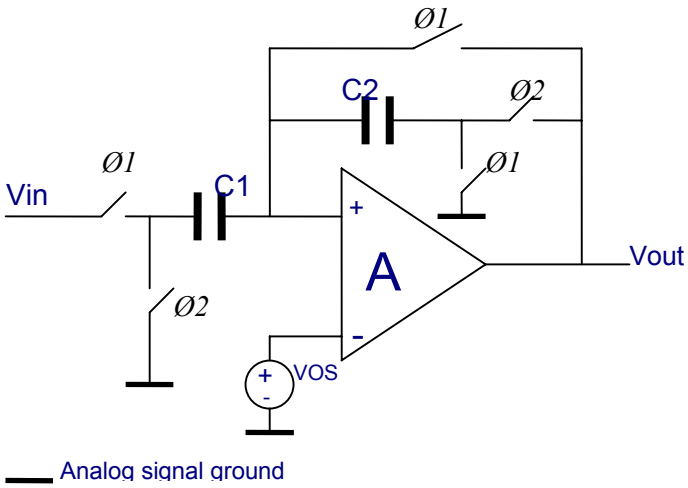


Figure 8.7: Offset- Compensation non-inverting Amplifier (AZ technique)

The switches in this schematic can implement using CMOS transistor, shown in **Figure8.8.** Here the fourth terminal (substrate) of n-MOS is connected to VSS and fourth terminal of p-MOS is connected to VDD.

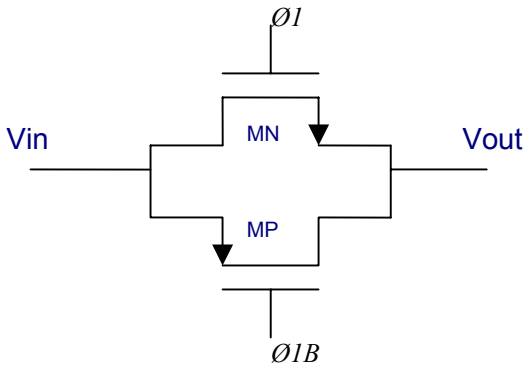
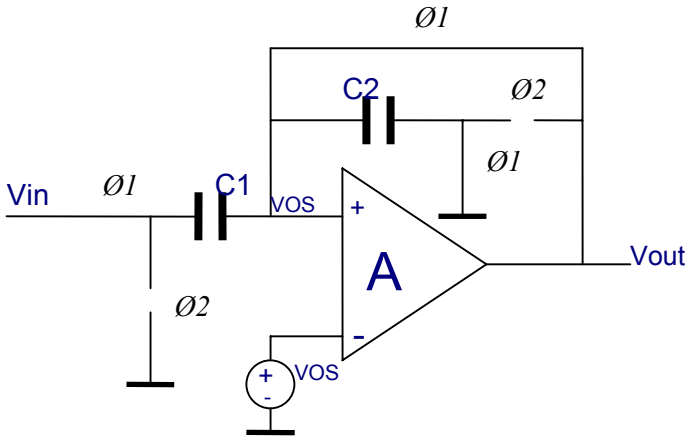
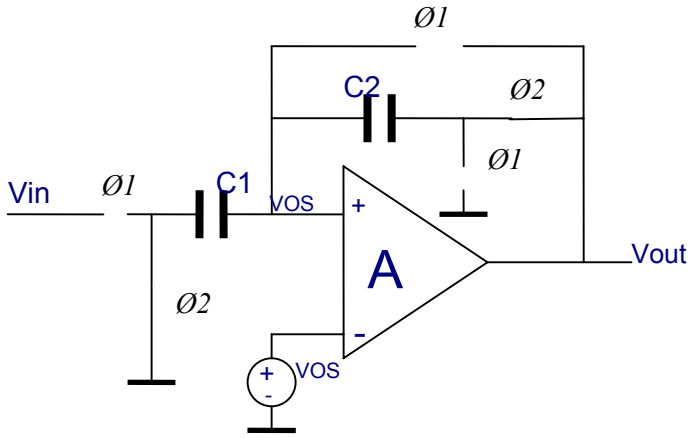


Figure 8.8: Switch implementation using CMOS

During the phase1 (*Ø1*), the circuit is configured as shown in figure below. So the capacitor C1 is charge to voltage *Vin-Vos* and capacitor C2 charge to voltage *Vos* and output is *Vos* since it is acting as buffer.



During the phase1 (*Ø2*), the circuit is configured as shown in figure below. If the input referred offset voltage is constant, the charge entering at the virtual ground node is *Vin*C1-C2* Vout.* So the output developed in this phase is independent of *Vos*. So the out follows the input signal in clock phase2. The implementation results are shown in results section



b. Inverting SC Voltage amplifier:

The schematic diagram of offset cancellation using inverting SC voltage amplifier is shown in **Figure8.9.** The two clocks (*Ø1, Ø2*) are used to Off/ON the switches are non-overlapping clocks (these two clocks never have high value at a time). In this circuit the clock phases at the input terminals are interchanged. So the clock phase2 is going to be high before the clock phase1.

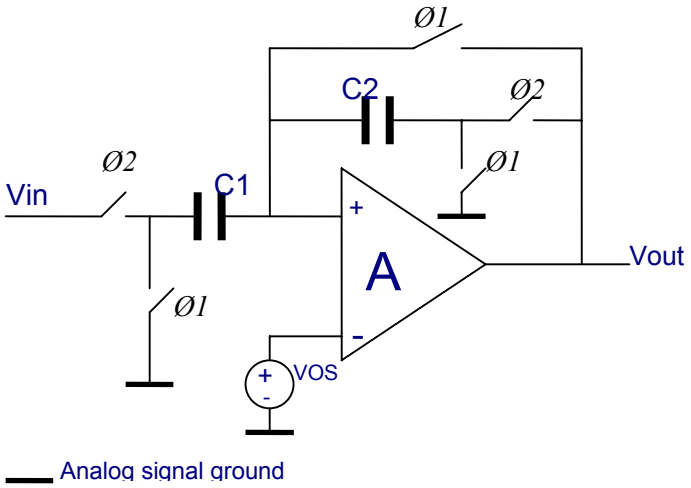
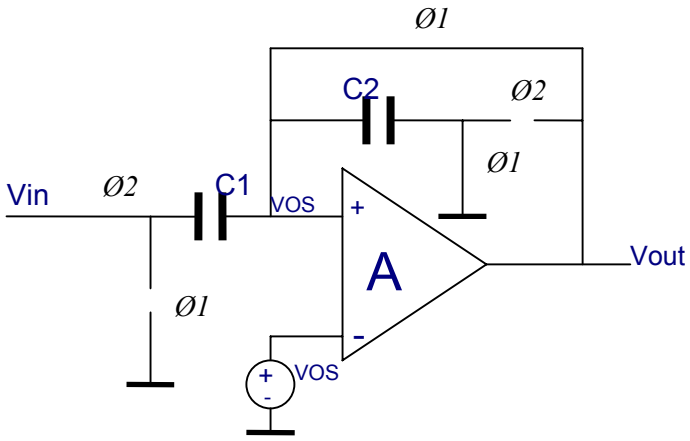
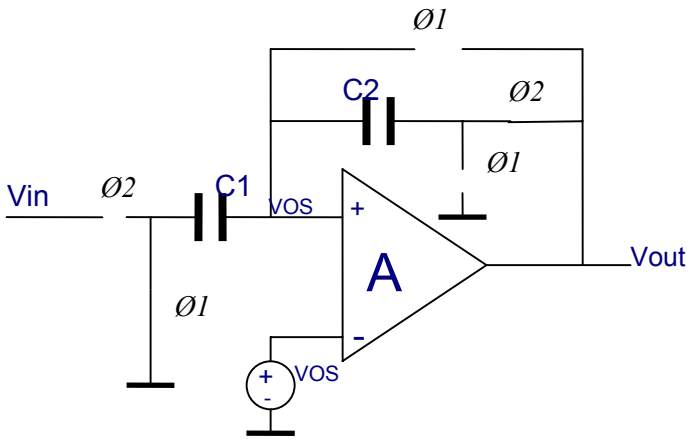


Figure 8.9: Offset- Compensation inverting Amplifier (AZ technique)

During the phase2 (*Ø2*), the circuit is configured as shown in figure below. So the capacitor C1 is charge to voltage *Vin-Vos* and capacitor C2 charge to voltage *Vos* and output is *Vos* since it is acting as buffer.



During the phase1 (*Ø1*), the circuit is configured as shown in figure below. In this phase the capacitors are always connected to virtual ground node. So if the input referred offset voltage is constant, the charge entering at the virtual ground node is *Vin*C1+C2* Vout.* So the output developed in this phase is independent of *Vos*. The implementation results are shown in results section



Chapter-9

RESULTS and DISCUSSION

To simulate the design modules we use *Hspice* as simulator and *Awan waves* as to analyze the module. The description of the *Hspice* and *Awan waves* is given below.

Hspice

The Star-Hspice optimizing analog circuit simulator is Avant!'s industrial-grade circuit analysis product for the simulation of electrical circuits in steady-state, transient, and frequency domains. Circuits are accurately simulated, analyzed, and optimized from DC to microwave frequencies greater than 100 GHz. Star-Hspice is ideal for cell design and process modeling and is the tool of choice for signal-integrity and transmission-line analysis.

Star-Hspice is compatible with most SPICE variations, and has the following additional features:

- Superior convergence
- Accurate modeling, including many foundry models
- Hierarchical node naming and reference
- Circuit optimization for models and cells, with incremental or simultaneous multiparameter optimizations in AC, DC, and transient simulations
- Interpreted Monte Carlo and worst-case design support
- Input, output, and behavioral algebraics for parameterizable cells
- Cell characterization tools for calibrating library models for higher-level logic simulators
- Geometric lossy coupled transmission lines for PCB, multi-chip, package, and IC technologies
- Discrete component, pin, package, and vendor IC libraries
- AvanWaves interactive waveform graphing and analysis from multiple.simulations

Awan Waves

AvanWaves provides a convenient graphical interface to display, analyze, and print the results of Star-Hspice simulations. This version of AvanWaves enables to:

- Load all files associated with a particular design in one step
- Open multiple designs simultaneously
- Update an existing design with information obtained from a new simulation run
- Superimpose results with two different data types within one graph, using up to two different Y-axes
- Build algebraic expressions and macros to modify and combine simulation results for display
- Graph (without limitations) simulation results or for displaying panels
- Interactively measure and label data on waveforms
- Save and restore all aspects of a particular design analysis as a configuration
- Look at individual parametric variations using the Sweep Filter
- Produce hard copy prints of the design analysis and results display
- Access online Help

Run Star-Hspice within the waveform analysis section

9.1 OPERATIONAL AMPLIFIER (BUFFER):

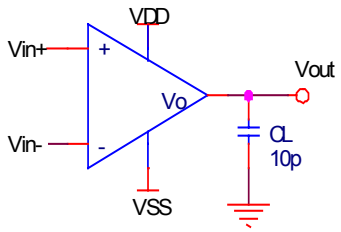
The different biasing parameters of all MOS transistors used in Design are shown in below Table

	W	L	Type	Id	Vth	gds
M1	68.75u	3u	PMOS	-100.0478u	-764.9653m	5.0627u
M2	68.75u	3u	PMOS	-100.0478u	-764.9653m	5.0627u
M3	26.90u	3u	NMOS	100.0478u	739.7856m	2.5361u
M4	26.90u	3u	NMOS	100.0478u	739.7856m	2.5361u
M5	146.45u	3u	PMOS	-200.0956u	-770.9977m	13.7792u
M6	125.35u	3u	NMOS	500.8225u	732.6583m	11.5032u
M7	335.65u	3u	PMOS	-500.8329u	-763.4170m	25.3227u
M8	73.80u	3u	PMOS	-100.0000u	-771.3659m	6.7377u

1. Input off set voltages (Vos):

To find input off-set voltage of opamp (shown in circuit setup), the input terminal voltage of circuit are fixed to average of power supplies, then we measure the output voltage. If the output voltage is not equal to average of power supplies (VDD and VSS) then we change the voltage of positive terminal according to output. The process is continuing until the output voltage is equal to average of power supplies, at that point we calculate the input offset voltage. It is the difference between average of power supplies and voltage at positive terminal.

Circuit setup



Spice commands

```
VD      VDD   0       DC      5V
V1      IN-   0       DC      2.5V
V2      IN+   0       DC      2.5V
.DC     V2    2.495   2.505   100U
.PRINT          DC      V(VO)
```

Input offset =245nV

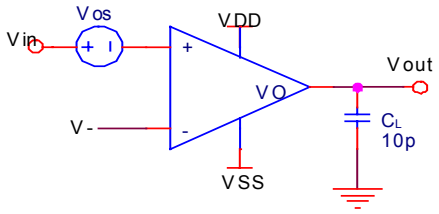
Output swing =0.4V to 4.41V

2. Gain and Phase Margin:

The gain and phase margin was measure using the configuration shown in Figure below.

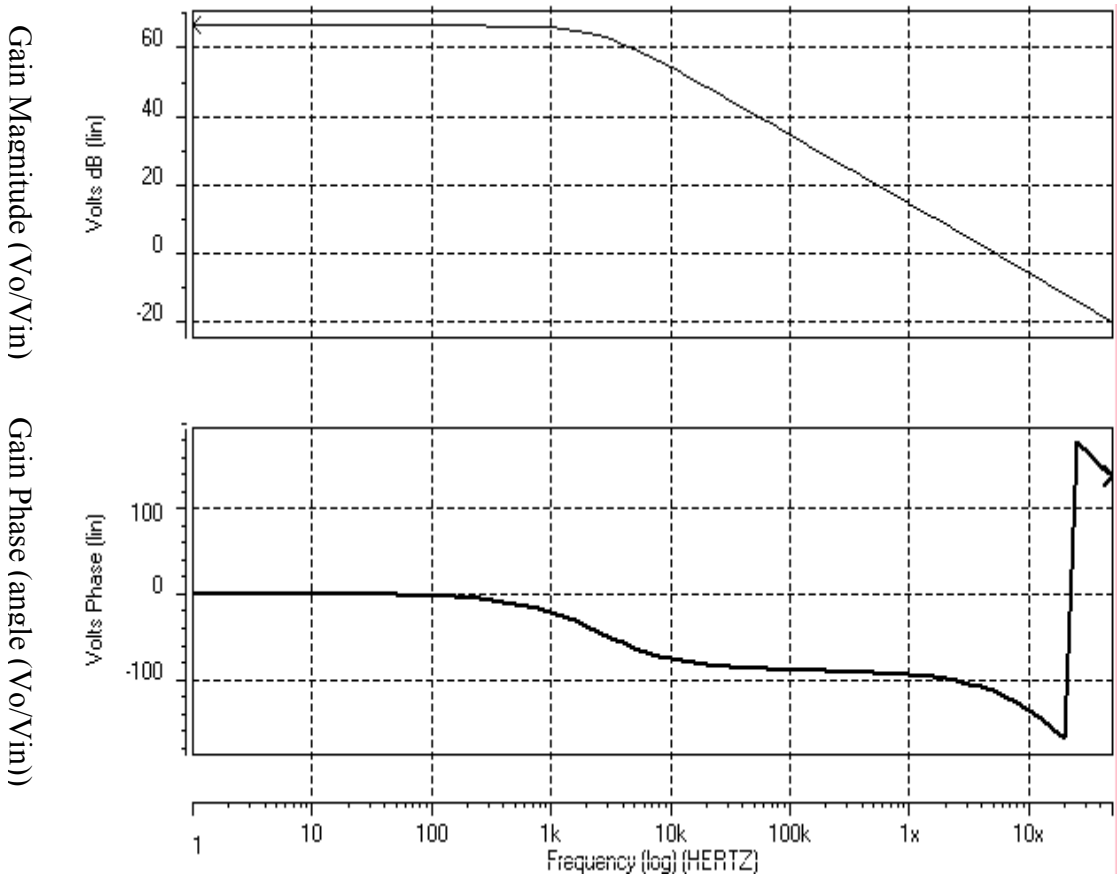
Circuit setup

Vin = DC 2.499999755v, AC=1v
V- = 2.5v, Vos=175nv



Spice commands

```
V1      IN-   0       DC      2.5V
V2      IN+   0       DC      2.499999755 V       AC 1.0V
.AC     DEC   10      1       10MEG
.PRINT AC     VDB(OUT)    VP(OUT)
```



Gain (Av) =66.5dB = 2113.5v/v

GB= 5.35MHz

Phase Margin=65^{o}

Phase cross over frequency = 25.1MHz

Gain Margin = 13.8 dB

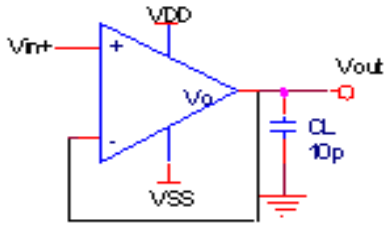
3. Input Common Mode Range (ICMR)

In hand calculations, the CMR appeared to be the most limiting constraint for the design, requiring a small value for I5 and large values for $(W/L)_5$ and $(W/L)_2$. The CMR was measured using the circuit in Figure by sweeping the input voltage from V_{SS} to V_{DD}.

In the unity gain configuration, however, the linear portion of the curve represents the CMR of the amplifier with the observation of current through M5 (I5).

Circuit setup

Vin+ =DC 5.0v



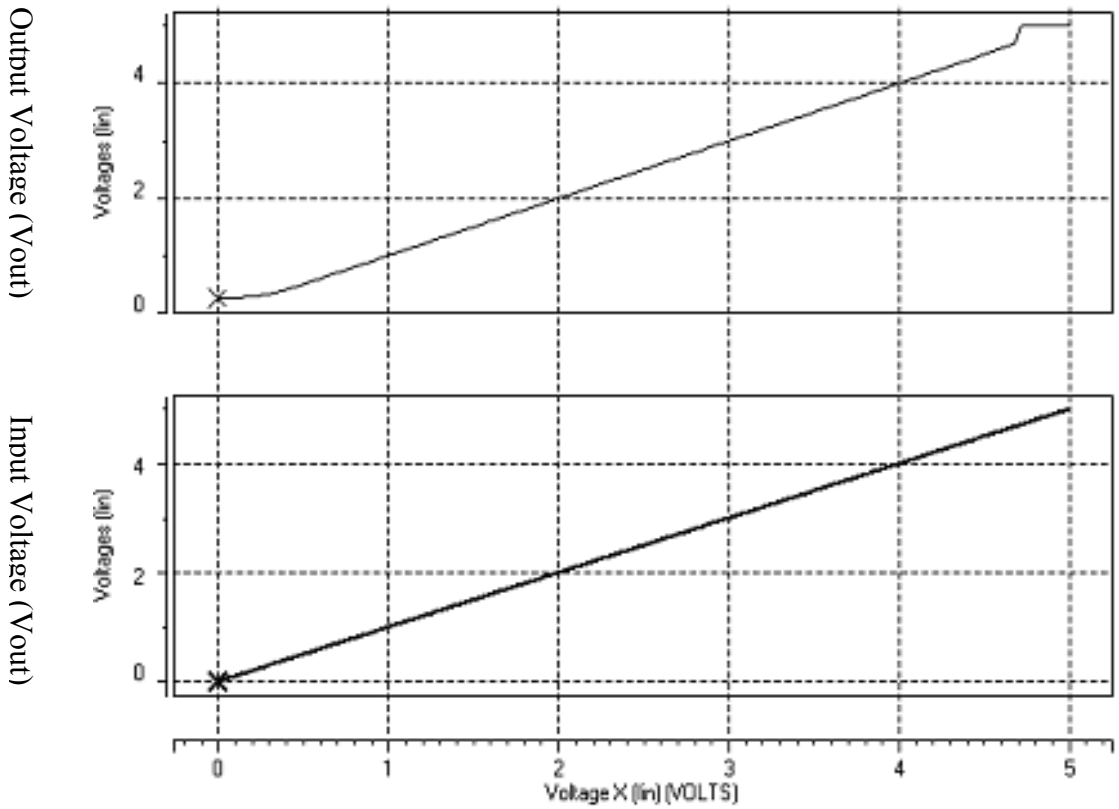
Spice commands

VF IN- VO 0V

V2 IN+ 0 DC 5.0V

.DC V2 0 5.0V 0.01V

.PRINT DC V(OUT) V(IN+)



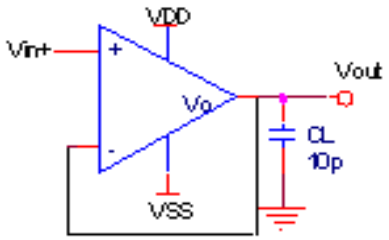
ICMR Max (Vin max) =3.30V

ICMR Mini (Vin min) =0.25V

4. Op-Amp as Buffer

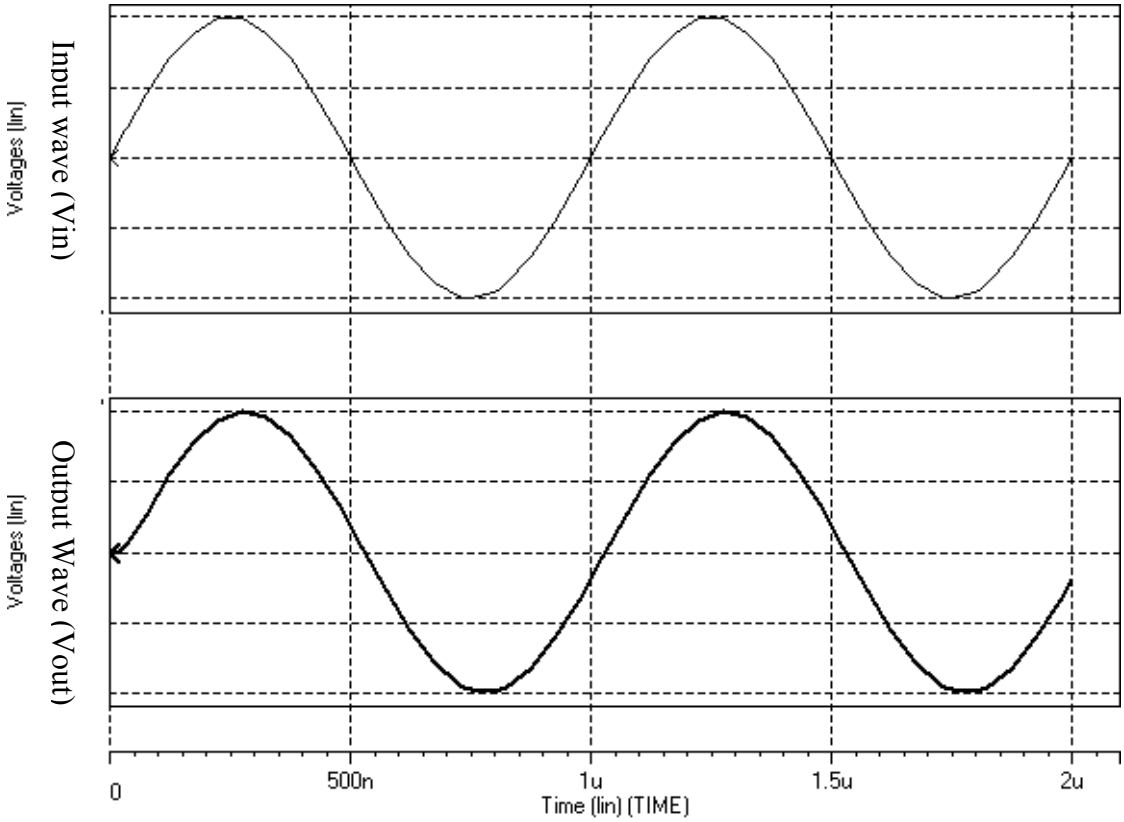
Op-Amp can be used as buffer by connecting output to negative terminal of input (unity gain configuration). We can verify Op-Amp as buffer by applying sinusoidal wave at input with 2v (peak-peak) riding at 2.5v.

Circuit setup



Spice commands

```
VF      IN-     VO      0V
VC      IN+     0       SIN(2.5 1.0 1MEG)
.TRAN           0.01U   2U
.PRINT          TRAN V(IN+) V(OUT)
```

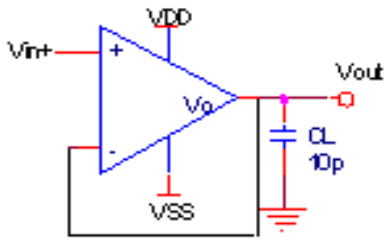


5. Settling Time (Ts) and Slew Rate (SR)

The settling time was the most demanding constraint in the design of the opamp. The initial design contained large (W/L) ratios and a small current in the differential pair in order to meet the CMR specification. This, however, led to a extremely poor settling time. If the ICMR is not main limiting constraint then we can get better settling time with the increase of current through differential amplifier. At this point, the capacitance at the output node was the limiting factor for the settling time. The slew rate is the rate of change of output voltage when a large signal pulse is applied at input. This also depend on I5 and compensation capacitor (C_C).

The settling time of opamp can be calculated by applying a small signal pulse of 0.5v riding at 2.5v. The slew rate of amplifier can be calculated by applying a large signal pulse of 3.5v riding at 0.5v. These were measured using the circuit shown in Figure

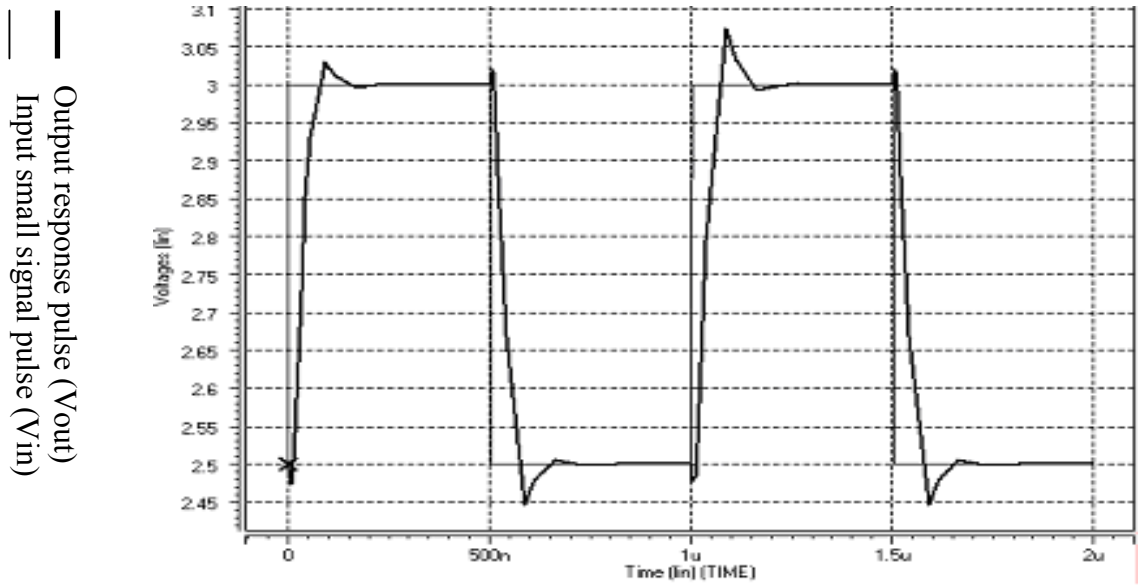
Circuit setup



Spice commands

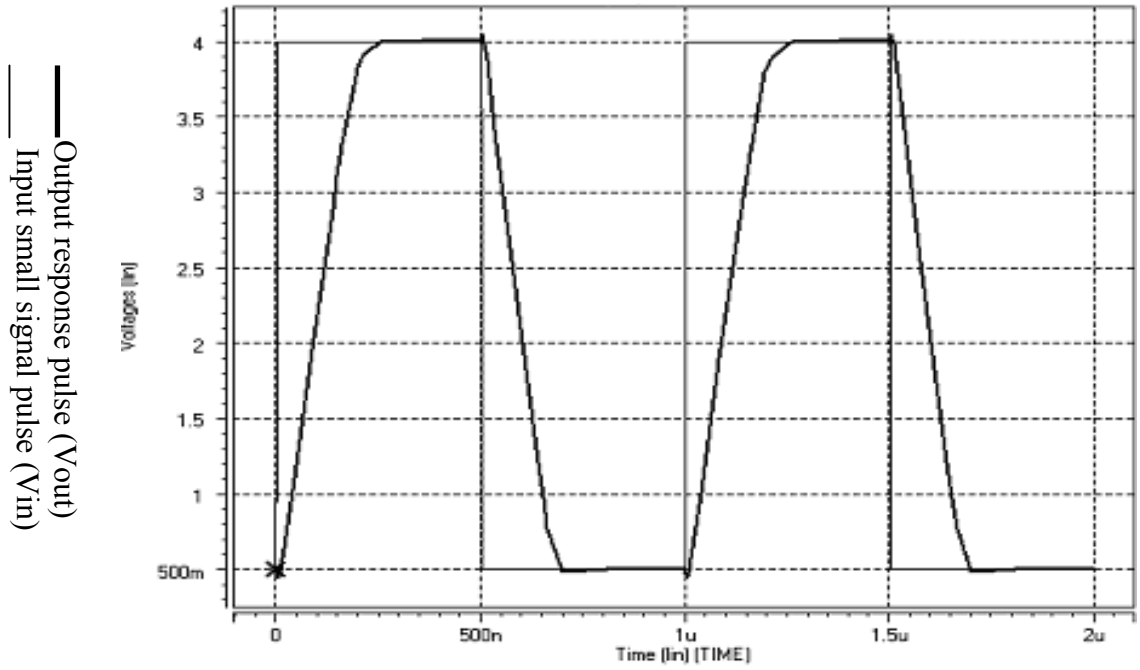
```
***settling time
VF      IN-     VO      0V
VC      IN+     0       PULSE(2.5V 3.0V 0 2NS 2NS 500NS 1US)
.TRAN           0.01U   2U
.PRINT          TRAN V(IN+) V(OUT)

***slew rate
VF      IN-     VO      0V
VC      IN+     0       PULSE(0.5V 4.0V 0 2NS 2NS 500NS 1US)
.TRAN           0.01U   2U
.PRINT          TRAN V(IN+) V(OUT)
```

Settling time



Settling Time (Ts) =150nS

Slew rate



Slew Rate (SR)

Positive SR =17.15V/uS

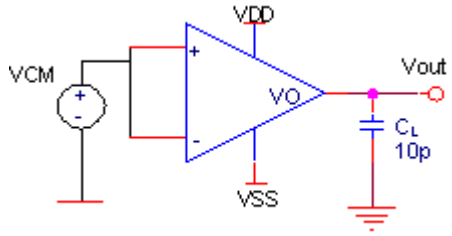
Negative SR =21.51V/uS

6. Common Mode Rejection Ratio (CMRR)

This is the ratio of differential gain to the common mode gain. The CMRR specification was not much of a constraint during the design of the amplifier, and basically required a commode-gain of less than 1 V/V. The CMRR was measured using the circuit in Figure by sweeping the input voltage from 0 to 2.5v.

Circuit setup

VCM=2.5v DC



Spice commands

V1 IN- VO 2.5V

V2 IN+ 0 2.5V

.DC V1 0 2.5V 0.01V

.TF V(VO) V1

Ac=886.5244m

Ad=2113.5

CMRR= Ad/Ac=2384 =67.55dB

7. Power Supply Rejection Ratio (PSRR)

The PSRR turned out to be an important constraint near the end of the design process. This is ratio of change in output voltage w.r.t input (vdd=0) to change in output w.r.t vdd (vin=0). i,e. PSRR=Av/Add.

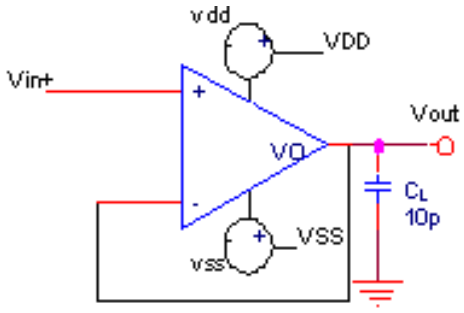
The PSRR was measured using the circuit of Figure, with vss active for PSRR- and vdd active for PSRR+. As was shown in circuit setup, the unity gain configuration produces an output that is approximately equal to 1/PSRR. The values of $PSRR^+$ and $PSRR^-$ are calculated in different runs where vdd and vss are small ac signal of 1v.

Circuit setup

$PSRR^+$=Vdd/Vout

$PSRR^-$=Vss/Vout

Vin+ = 2.5v



Spice commands

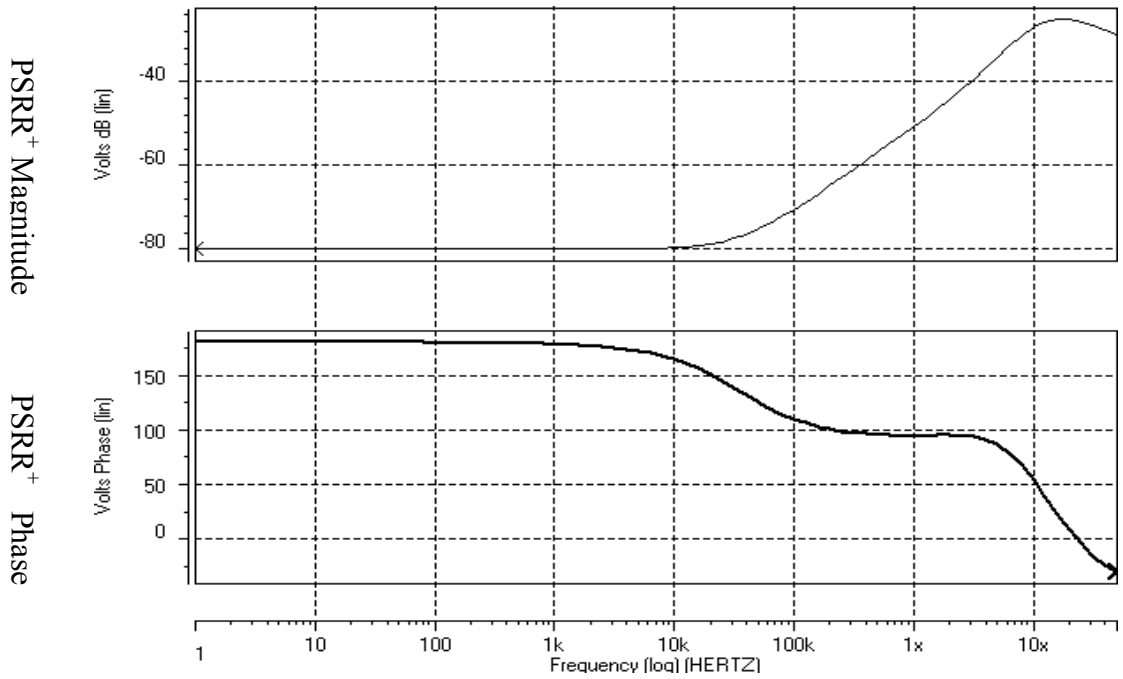
$PSRR^+$

```
VD     VDD    0      DC     5V      AC 1.0V
VS      VSS    0      0V
V2      IN+    0      DC     2.5V
 .AC    DEC    10     1      50MEG
.PRINT AC     VDB(OUT)    VP(OUT)
```

$PSRR^-$

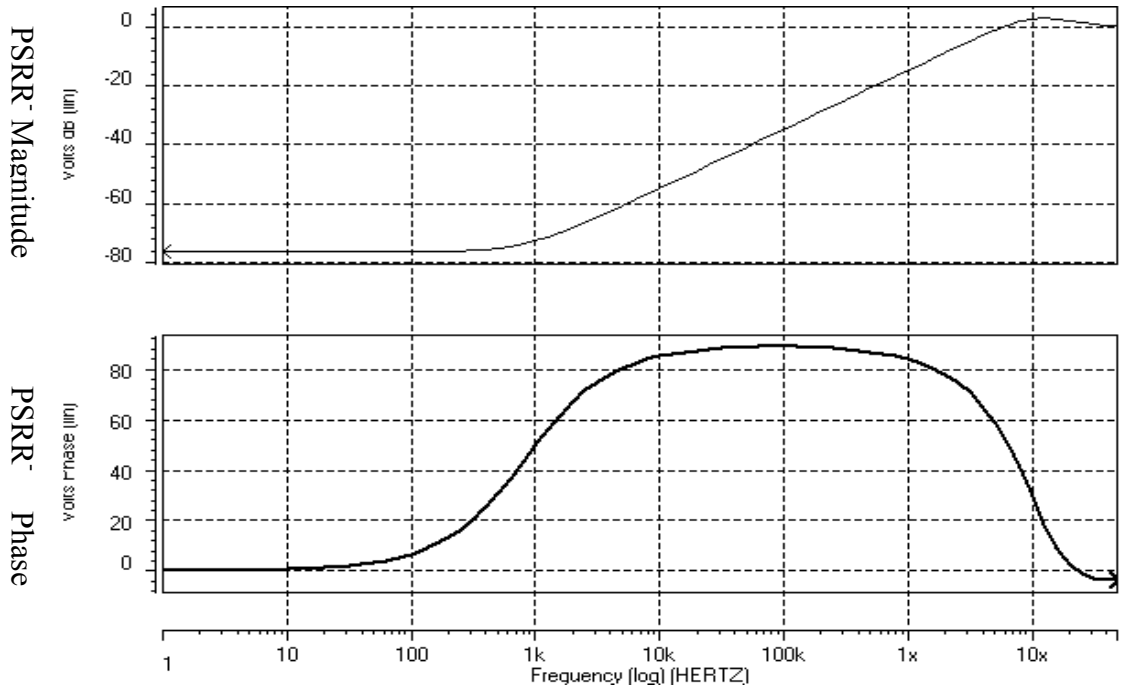
```
VD     VDD    0      DC     5V
VS      VSS    0      0V     AC 1.0V
V2      IN+    0      DC     2.5V
 .AC    DEC    10     1      50MEG
.PRINT AC     VDB(OUT)    VP(OUT)
```

PSRR$^+$



PSRR$^+$ = 79.99dB

PSRR$^-$



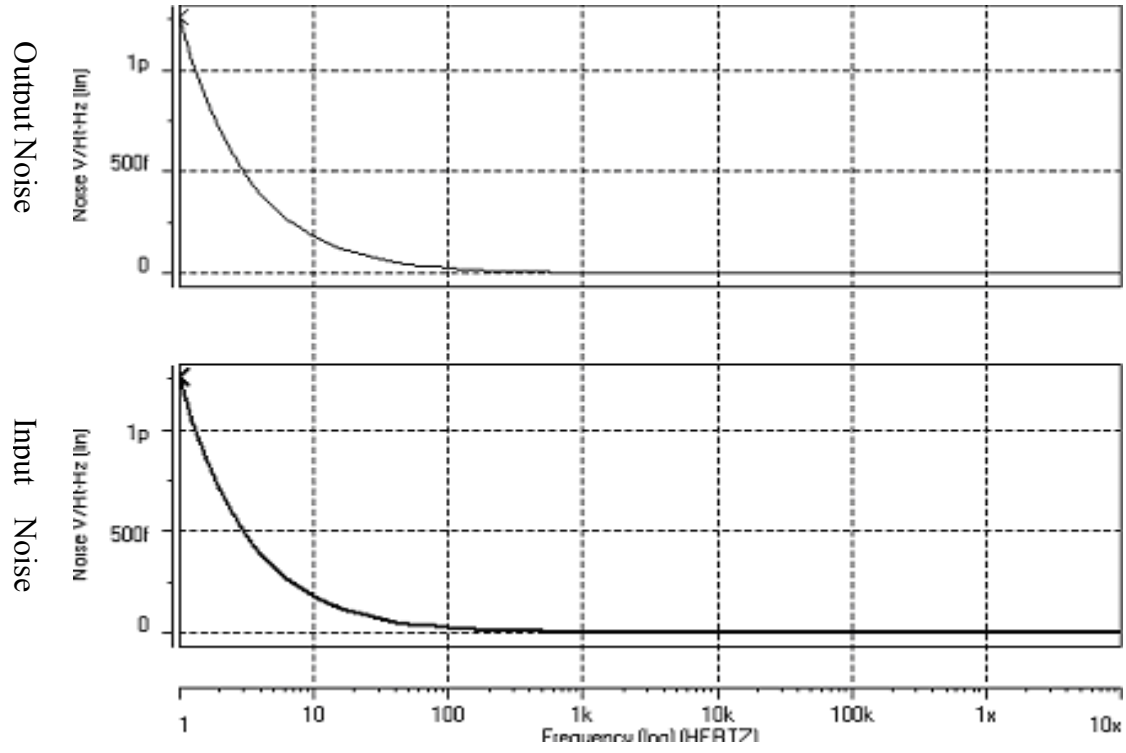
PSRR$^-$ = 76.2dB

8. Noise Analysis

Noise analysis can be done using the unity Gain configuration with application 2.5V DC and 1V AC at input. We can measure output noise in terms of V/(Sq Hz) then input noise can be calculated using Gain (output noise/Gain).

Spice commands

```
V1      IN-   0      DC    2.5V
V2      IN+   0      DC    2.5V AC 1.0V
.NOISE        V(OUT) V2    5
.AC     DEC   10     1     10MEG
.PRINT AC     VDB(OUT)     VP(OUT)
```



The output noise and input noises are calculated at different frequencies, shown in below table.

	@1Hz	@1KHz	@3.16MHz
Output Noise $\left(\frac{V}{\sqrt{Hz}}\right)$	1.1209u	62.5723n	11.68n
Input Noise $\left(\frac{V}{\sqrt{Hz}}\right)$	1.1209u	62.5757n	11.91n

The Final Specification of Op-Amp (met) are

S. No	Specification	Simulation Value
	DC Specifications	
1	Input Common Mode Range (ICMR)	
2	Input offset	0.25V to 3.30V 175nV
	AC Specifications	
3	Open Loop Gain	66.5dB
4	Phase Margin	65^{o}
5	Gain Margin	13.8dB
6	Phase cross over frequency	25.1MHz
7	Gain cross over frequency (UGB)	5.35 MHz
8	Output Swing	0.4V to 4.4V
9	Common Mode Rejection Ratio (CMRR)	67.55dB
	Response Time	
10	Settling Time (delta=0.1% of final value)	150nS
11	Slew Rate (SR)	
	Positive Slew Rate	17.14V/uS
	Negative Slew Rate	21.51V/uS
12	Power dissipation	4.0047mW
13	Noise $\left(\frac{V}{\sqrt{Hz}}\right)$	
	Output Noise @1Hz	1.1209u
	Input Noise@1Hz	1.1209u

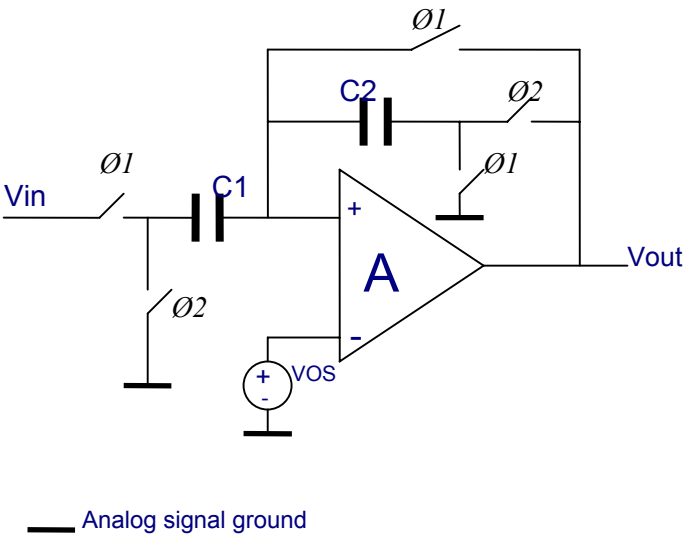
Note: For all above specifications were measured with load of $\mathbf{C_L}$ **=10pF**

9.2 AUTOZEROING TECHNIQUE:

This Autozeroing technique is mostly used to cancel or to reduce the offset and noise in the circuit, as explained in section 8.2. The results of offset cancellation implementation (Autozeroing Technique) using *non-inverting* and *inverting* SC voltage amplifier are shown in this section.

a. Non-inverting SC voltage Amplifier:

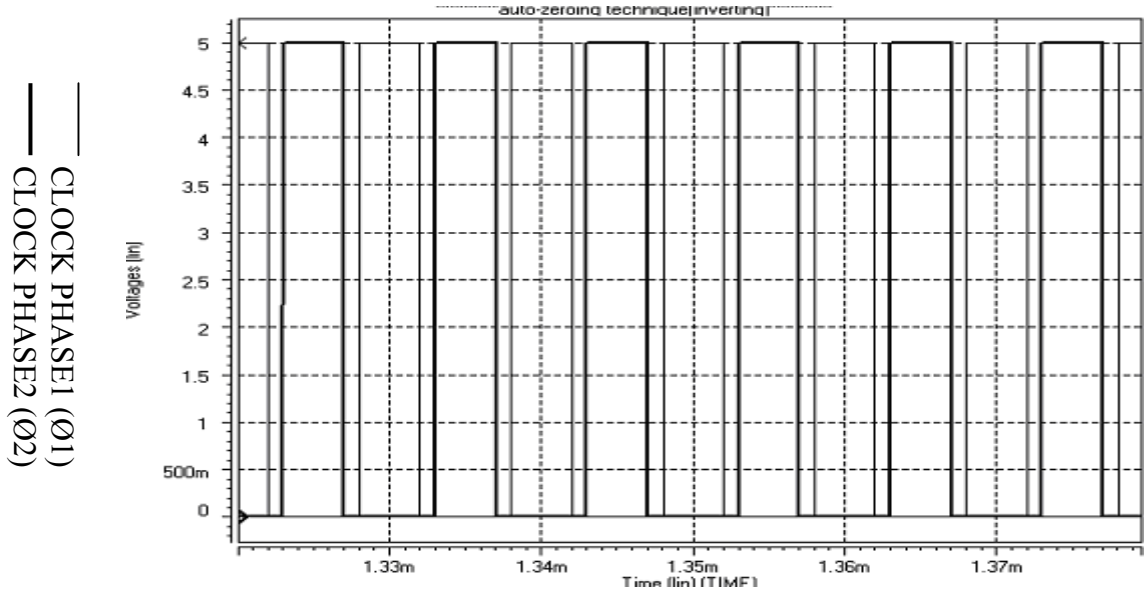
Circuitry:



In this implementation of autozeroing technique, the switches are controlled by the two non-overlapping clocks. The spice netlist for this circuitary is shown in *Appendix.* The switches are implemented using CMOS transistor and the non-over lapping clocks are generated using *PULSE* command in *SPICE* at the time of simulation, shown below.

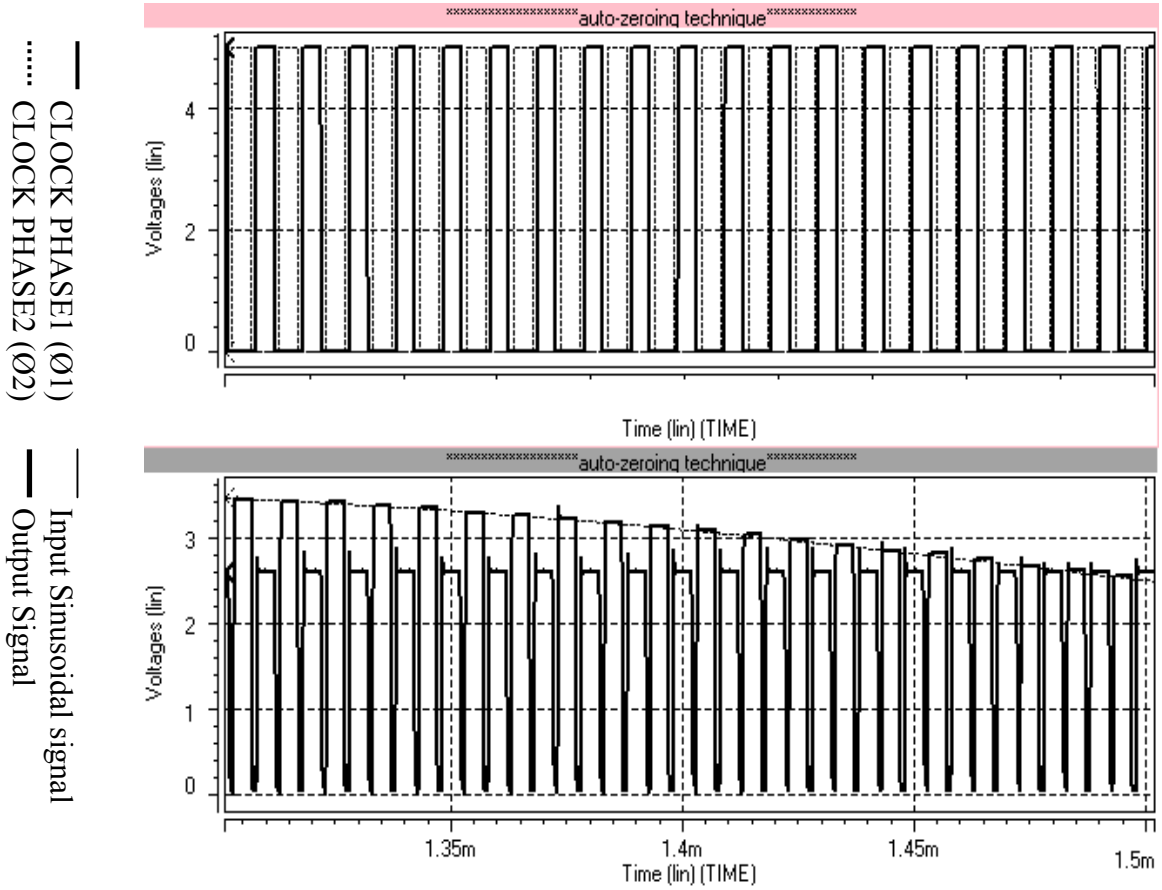
Spice commands:

```
**********CLOCK PHASE1 (Ø1) **********
VC1    CK1    0       PULSE(5V 0V 2US 0.02US 0.02US 6US 10US)
VC1B   CK1B   0       PULSE(0V 5V 2US 0.02US 0.02US 6US 10US)

**********CLOCK PHASE1 (Ø2) **********
VC2    CK2    0       PULSE(0V 5V 3US 0.02US 0.02US 4US 10US)
VC2B   CK2B   0       PULSE(5V 0V 3US 0.02US 0.02US 4US 10US)
```

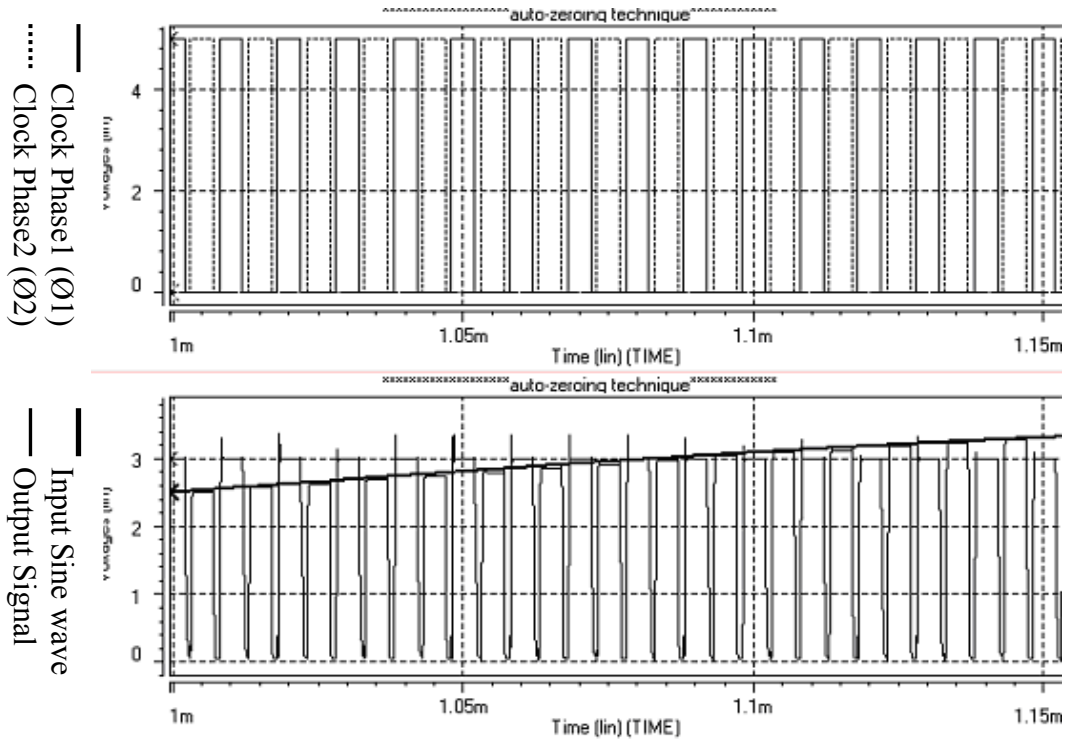


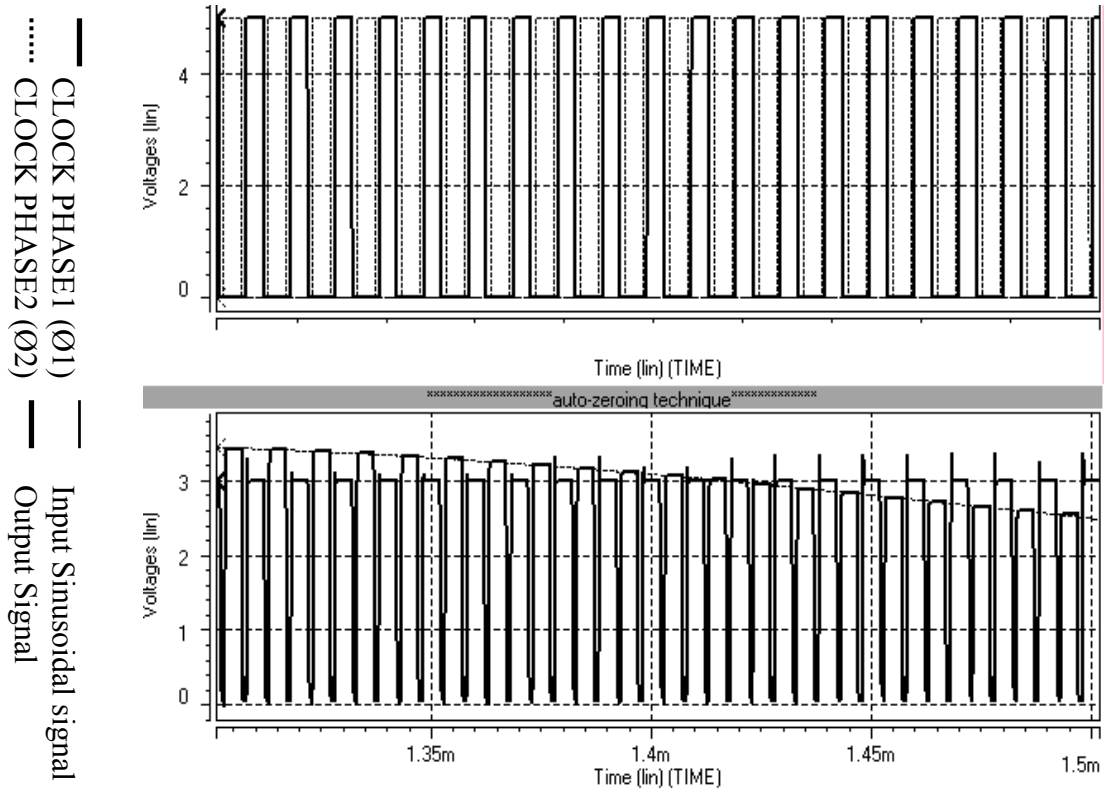
For this circuit, the input is sinusoidal of frequency of 1 KHz riding at 2.5v, clock frequency of 100 kHz are applied. This simulated with different values of Vos in two different simulation runs. Signal ground at 2.5v.

Vos=0.1v



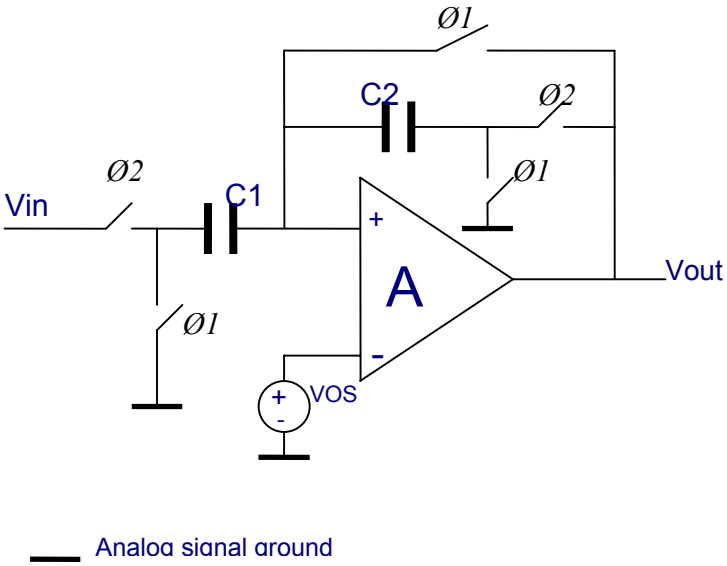
Vos= 0.5v


auto-zeroing technique
Clock Phase1 (Ø1)
Clock Phase2 (Ø2)
Voltages [lin]
Time (lin) (TIME)
1m
1.05m
1.1m
1.15m
auto-zeroing technique
Input Sine wave
Output Signal
Voltages [lin]
Time (lin) (TIME)


CLOCK PHASE1 (Ø1)
CLOCK PHASE2 (Ø2)
Voltages [lin]
Time (lin) (TIME)
auto-zeroing technique
Input Sinusoidal signal
Output Signal
Voltages [lin]
1.35m
1.4m
1.45m
1.5m
Time (lin) (TIME)

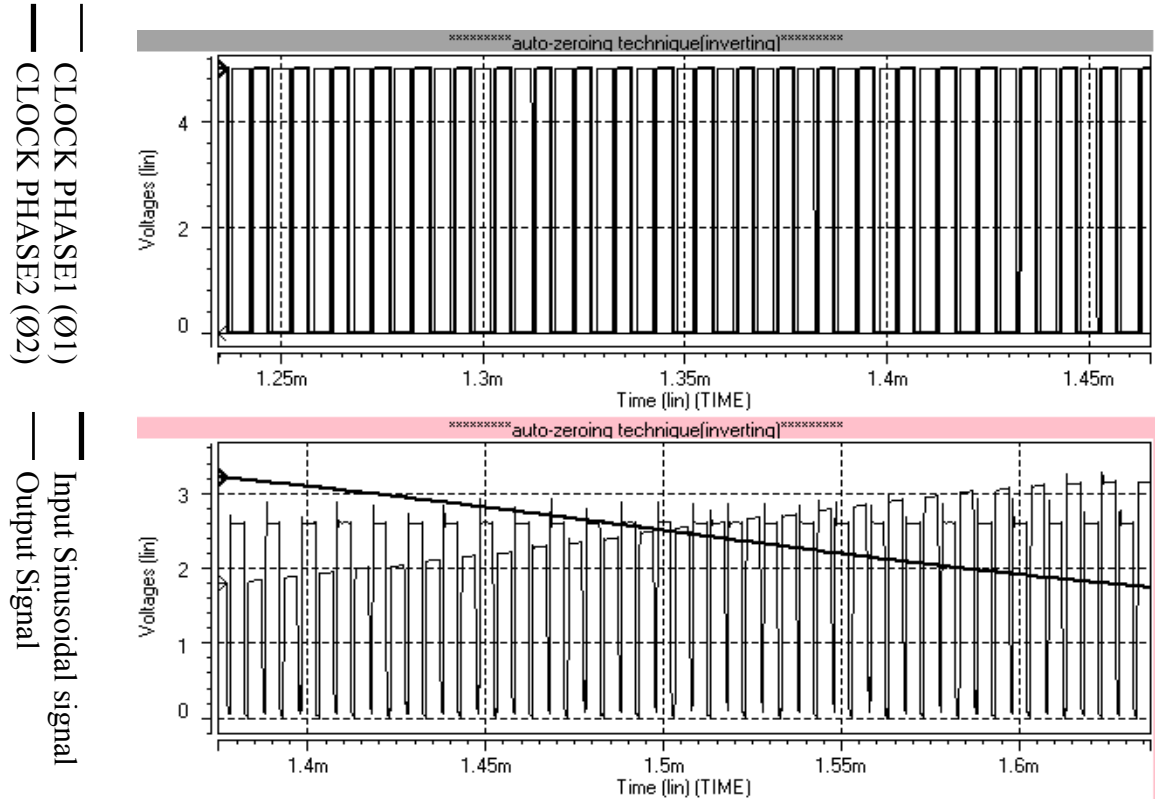
b. Inverting SC voltage amplifier:

Circuitry:

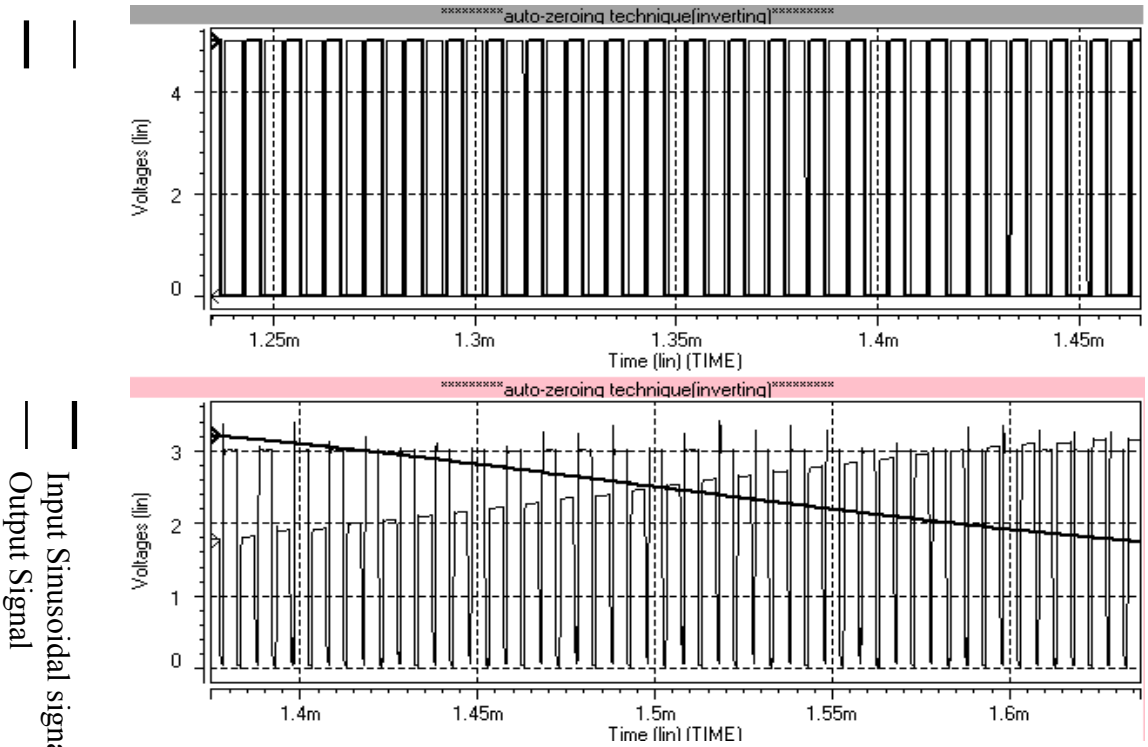


For this circuit, the input is sinusoidal of frequency of 1 KHz riding at 2.5v, clock frequency of 100 kHz are applied. This simulated with different values of Vos in two different simulation runs. Signal ground at 2.5v.

Vos=0.1V

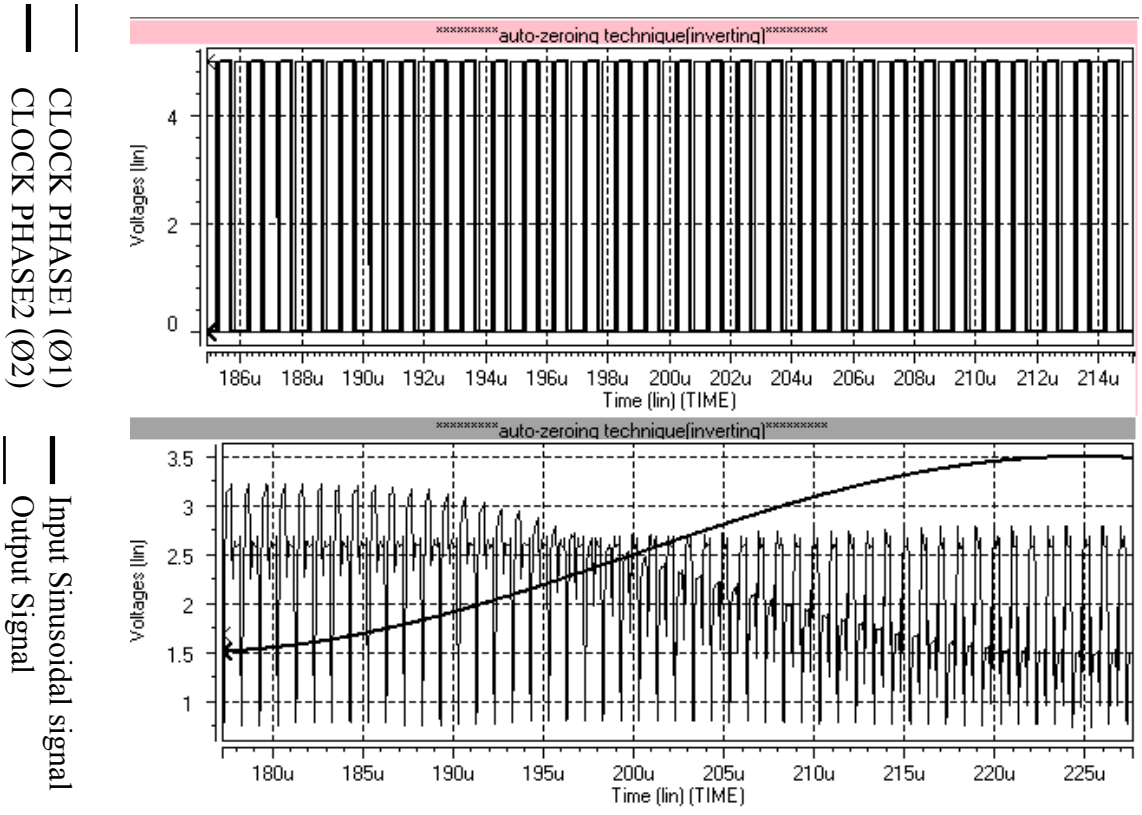


Vos = 0.5v



For this circuit, the input is sinusoidal of frequency of 10 KHz riding at 2.5v, clock frequency of 1MHz are applied. This simulated with Vos=2.6V and Analog Signal ground at 2.5v

Vos=2.6v



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APPENDIX
SPICE NETLIST

A. Two Stage Operational Amplifier (Buffer)

```
**********TWO STAGE OP-AMP**********

**********POWER SUPPLIES**********
VD      VDD    0       5V      *AC 1V
VS      VSS    0       0V      * AC 1V
*****************************************

*************************************************************
**********DIFFERENTIAL STAGE**********
M1      D1      IN-     D5      D5      PA      L=3U  W=68.75U
M2      D2      IN+     D5      D5      PA      L=3U  W=68.75U
M5      D5      D8      VDD     VDD     PA      L=3U  W=146.45U
M3      D1      D1      VSS     VSS     N       L=3U  W=26.90U
M4      D2      D1      VSS     VSS     N       L=3U  W=26.90U
*****************************************

**********GAIN STAGE**********
M6      OUT     D2      VSS     VSS     N       L=3U  W=125.35U
M7      OUT     D8      VDD     VDD     PA      L=3U  W=335.65U
*****************************************

**********BIASING**********
M8      D8      D8      VDD     VDD     PA      L=3U  W=73.80U
I       D8      VSS     100UA
*****************************************

********CAPACITANCES**********
CC      D2      OUT     10PF
CL      OUT     VSS     10PF
**********
*************************************************************

**********FORCES**********
VF      OUT     IN-     0
*V2     IN+     0       DC      2.5V    AC      1V      *2.499999755V
*V1     IN-     0       DC      2.5V
*VI     VC      0       DC      2.5V
VI      IN+     0       SIN(2.5V 1.0V 1MEG)
*VI     IN+     0       PULSE(0.5V 4.0V 0NS 2NS 2NS 500NS 1000NS)
*VI     IN+     0       PULSE(2.5V 3.0V 0NS 2NS 2NS 500NS 1000NS)
*****************************************
```

```
**********ANALYSYS**********
*.DC        VI          0        2.5V    0.01V
*.TF        V(OUT)   VI
*.PRINT    DC         V(OUT)    V(IN+)

.TRAN      0.01U      2U
.PRINT     TRAN       V(OUT)    V(IN+)

*.AC        DEC        10     1     10MEG
*.PRINT    AC        VDB(OUT)   VP(OUT)

*.NOISE   V(OUT)     V1     5
******************************************

******************************************
.OPTION       POST  NOMOD
.OP
.OPTION       NUMDGT=6
.OPTION       INGOLD=2
******************************************

********MODEL PARAMETERS*********
.PROTECT

.INCLUDE  /USR1/DTECH/PROCESS/CP8X/MODELS/POST_SI/HSPICE/TNTP13_5V

.UNPROTECT
****************************************
.END
************************************************************
```

B. Autozeroing Technique

B.1 Non-inverting amplifier

```
**********AUTO-ZEROING TECHNIQUE (Non-inverting) **********

*****************POWER SUPPLIES**************
VD     VDD  0       5V
VS     VSS  0       0V
*********************************************

*************************************************************
.SUBCKT     OPAMP       IN+    IN-     OUT   VDD   VSS
* CONNECTION            IN+     |       |      |      |
*                                IN-     |      |      |
*                                        OUT    |      |
*                                               INP    |
*                                                      VSS

********DIFFERENTIAL STAGE*******************
M1     D1     IN-    D5     D5     PA     L=3U  W=68.75U
M2     D2     IN+    D5     D5     PA     L=3U  W=68.75U
M5     D5     D8     VDD    VDD    PA     L=3U  W=146.45U
M3     D1     D1     VSS    VSS    N      L=3U  W=26.90U
M4     D2     D1     VSS    VSS    N      L=3U  W=26.90U
*********************************************
******************GAIN STAGE*****************
M6     OUT    D2     VSS    VSS    N      L=3U  W=125.35U
M7     OUT    D8     VDD    VDD    PA     L=3U  W=335.65U
*********************************************
******************BIASING********************
M8     D8     D8     VDD    VDD    PA     L=3U  W=73.80U
I      D8     VSS    100UA
*********************************************
***************CAPACITANCES*****************
CC     D2     OUT    10PF
*********************************************
.ENDS
*********************************************

*****************************************************
M1     IN     CK2    VB1    VSS    N      L=0.8U   W=50U
M2     VB1    CK2B   IN     VDD    P      L=0.8U   W=75U

M3     VB1    CK1    SG     VSS    N      L=0.8U   W=50U
M4     SG     CK1B   VB1    VB1    P      L=0.8U   W=75U

C1     VB1    IN-    10PF
```

```
M5     IN-    CK1   OUT   VSS   N      L=0.8U  W=50U
M6     OUT    CK1B  IN-   VDD   P      L=0.8U  W=75U

M7     VB2    CK1   SG    VSS   N      L=0.8U  W=50U
M8     SG     CK1B  VB2   VDD   P      L=0.8U  W=75U

M9     VB2    CK2   OUT   VSS   N      L=0.8U  W=50U
M10    OUT    CK2B  VB2   VDD   P      L=0.8U  W=75U

C2     IN-    VB2   10PF

X1     IN+    IN-   OUT   VDD   VSS    OPAMP
*************************************************

**********FORCES**********
VG     SG     0       DC     2.5V
VOS    IN+    SG      DC     0.1v
*VI    IN     SG      DC     1.0V
VI     IN     0       SIN(2.5V 1.0V 1K)

**********NON_OVERLAPPING CLOCKS********
VC1    CK1    0       PULSE(5V 0V 2US 0.02US 0.02US 6US 10US)
VC1B   CK1B   0       PULSE(0V 5V 2US 0.02US 0.02US 6US 10US)

VC2    CK2    0       PULSE(0V 5V 3US 0.02US 0.02US 4US 10US)
VC2B   CK2B   0       PULSE(5V 0V 3US 0.02US 0.02US 4US 10US)
*********************************************

**********ANALYSYS***************
.TRAN 10U 4000U
*.PRINT TRAN V(IN) V(OUT) V(IN-) V(VB1)
*****************************************
**********************
.OPTION       POST   NOMOD
.OP
.OPTION NUMDGT=6
**********************

**********MODEL PARAMETERS*********
.PROTECT
.INCLUDE  /USR1/DTECH/PROCESS/CP8X/MODELS/POST_SI/HSPICE/TNTP13_5V
.UNPROTECT
*****************************************************************
.END
```

B.2 inverting amplifier

```
**********AUTO-ZEROING TECHNIQUE (Non-inverting) **********

*****************POWER SUPPLIES**************
VD     VDD  0       5V
VS     VSS  0       0V
*********************************************

*************************************************************
.SUBCKT     OPAMP       IN+    IN-     OUT   VDD   VSS
* CONNECTION            IN+     |       |      |      |
*                                IN-     |      |      |
*                                        OUT    |      |
*                                               INP    |
*                                                      VSS

********DIFFERENTIAL STAGE*******************
M1     D1     IN-    D5     D5     PA     L=3U  W=68.75U
M2     D2     IN+    D5     D5     PA     L=3U  W=68.75U
M5     D5     D8     VDD    VDD    PA     L=3U  W=146.45U
M3     D1     D1     VSS    VSS    N      L=3U  W=26.90U
M4     D2     D1     VSS    VSS    N      L=3U  W=26.90U
*********************************************
******************GAIN STAGE*****************
M6     OUT    D2     VSS    VSS    N      L=3U  W=125.35U
M7     OUT    D8     VDD    VDD    PA     L=3U  W=335.65U
*********************************************
******************BIASING********************
M8     D8     D8     VDD    VDD    PA     L=3U  W=73.80U
I      D8     VSS    100UA
*********************************************
***************CAPACITANCES*****************
CC     D2     OUT    10PF
*********************************************
.ENDS
*********************************************

*****************************************************
M1     IN     CK1    VB1    VSS    N      L=0.8U   W=50U
M2     VB1    CK1B   IN     VDD    P      L=0.8U   W=75U

M3     VB1    CK2    SG     VSS    N      L=0.8U   W=50U
M4     SG     CK2B   VB1    VB1    P      L=0.8U   W=75U

C1     VB1    IN-    10PF
```

```
M5     IN-    CK1   OUT   VSS   N      L=0.8U  W=50U
M6     OUT    CK1B  IN-   VDD   P      L=0.8U  W=75U

M7     VB2    CK1   SG    VSS   N      L=0.8U  W=50U
M8     SG     CK1B  VB2   VDD   P      L=0.8U  W=75U

M9     VB2    CK2   OUT   VSS   N      L=0.8U  W=50U
M10    OUT    CK2B  VB2   VDD   P      L=0.8U  W=75U

C2     IN-    VB2   10PF

X1     IN+    IN-   OUT   VDD   VSS    OPAMP
*************************************************

**********FORCES**********
VG     SG     0       DC     2.5V
VOS    IN+    SG      DC     0.1v
*VI    IN     SG      DC     1.0V
VI     IN     0       SIN(2.5V 1.0V 1K)

**********NON_OVERLAPPING CLOCKS********
VC1    CK1    0       PULSE(5V 0V 2US 0.02US 0.02US 6US 10US)
VC1B   CK1B   0       PULSE(0V 5V 2US 0.02US 0.02US 6US 10US)

VC2    CK2    0       PULSE(0V 5V 3US 0.02US 0.02US 4US 10US)
VC2B   CK2B   0       PULSE(5V 0V 3US 0.02US 0.02US 4US 10US)
*********************************************

**********ANALYSYS***************
.TRAN 10U 4000U
*.PRINT TRAN V(IN) V(OUT) V(IN-) V(VB1)
*****************************************
**********************
.OPTION       POST   NOMOD
.OP
.OPTION NUMDGT=6
**********************

**********MODEL PARAMETERS*********
.PROTECT
.INCLUDE  /USR1/DTECH/PROCESS/CP8X/MODELS/POST_SI/HSPICE/TNTP13_5V
.UNPROTECT
*****************************************************************
.END
```