Prototype Hardware Model Development of HVDC Transmission System

By

MOHAMMED IRFAN I. SIDDIQUI

11MEEE16

DEPARTMENT OF ELECTRICAL ENGINEERING

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(ELECTRICAL POWER SYSTEMS)

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MOHAMMED IRFAN I. SIDDIQUI

11MEEE16

DEPARTMENT OF ELECTRICAL ENGINEERING

INSTITUTE OF TECHNOLOGY

NIRMA UNIVERSITY

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MAY 2013

Undertaking for Originality of the Work

I, **Mr. Mohammedirfan I. Siddiqui**, Roll.No.**11MEEE16**, give undertaking that the Major Project entitled **"Prototype Hardware Model Development of HVDC Transmission System"** submitted by **Mr. Mohammedirfan I. Siddiqui** submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Electrical Engineering (Electrical power Systems)**of Nirma University, Ahmedabad, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action

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Place:

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Endorsed by

Prof. C. B. Bhatt

Department of Electrical Engineering

Institute of Technology

Nirma University

Ahmedabad

Certificate

This is to certify that the Major Project Report entitled **"Prototype Hardware Model Development of HVDC Transmission System"** submitted by **Mr. Mohammed Irfan I. Siddiqui (Roll No-11MEEE16)** towards the partial fulfillment of the requirements for the award of degree in Master of Technology(Electrical Engineering) in the field of Electrical Power Systems of Nirma University is the record of work carried out by him under our supervision and guidance. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.
Date :

....

Project Guide:

Prof. C. B. Bhatt

Department of Electrical Engineering,

Institute of Technology,

Nirma University,

Ahmedabad.

Head of Department

Department of Electrical Engineering

Institute of Technology

Nirma University

Ahmedabad

Director

Institute of Technology

Nirma University

Ahmedabad

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Mohammed Irfan Siddiqui

11MEEE16

Abstract

The project entails simulating a model of a complete HVDC transmission line and prototype hardware model of HVDC transmission system. This involves the design of converter circuitry, gate firing units, gamma detection circuits, rectifier and inverter control systems and passive harmonic filtering circuits. The complete model converts AC power into DC power by controlled rectifier and then again converts this DC power into AC power by line commutated inverter, after transmitting DC power through the cable. This action is controlled automatically by the system. For prevention of large fluctuation in direct current due to variation in AC system voltage, maintaining direct voltage near rated value and prevention of commutation failure in inverter, three basic controls for rapid control of converters are implemented. Constant current control for both rectifier and inverter, CEA (constant extinction angle) control for inverter and CIA (constant ignition angle) control for rectifier. Conversion of power, Bi-directional power flow on HVDC link and behaviour of HVDC link during fault occurrence and fault clearance are main objective of this project. Simulation of complete HVDC transmission system for 2.2 kW, 415 V, 50 Hz System is done in Simulation software package. The gate firing using the Individual Phase Control (IPC) scheme and the Equidistant Pulse Control (EPC) scheme have been simulated to observe their relative advantages and disadvantages. By using ARDUINO DUE micro-controller, complete HVDC control system and gate firing units are implemented in hardware model. Thus, complete working model of prototype HVDC transmission system is developed using the basic concepts and appropriate circuitry.

Contents

List of Figures

Abbreviations

CC .... Constant Current
CEA .... Constant Extinction Angle
CIA .... Constant Ignition Angle
EPC .... Equidistant Phase control
FACTS .... Flexible AC Transmission System
HVAC .... High Voltage Alternating current
HVDC .... High Voltage Direct Current
IGBT .... Insulated Gate Bipolar Transistor
IPC .... Individual Phase Control
PI .... Proportional Integral
PLL .... Phase Locked Loop
PWM .... Pulse Width Modulation
VCO .... Voltage Controlled Oscillator
VDCOL .... Voltage dependent Current Order Limit

Nomenclature

I_d .... Direct Current through the HVDC Link
V_d .... DC Voltage
L_d .... Smoothing Reactor
L_c .... Source Inductance
V_{do} .... Average value of Direct Voltage
$T_1 - T_6$ .... Thyristors
P_{dr} .... Power delivered
P_{di} .... Power Received
α .... Ignition Delay Angle
μ .... Overlap Angle
δ .... Extinction Angle
β .... Ignition Advance Angle
γ .... Extinction Advance Angle

Chapter 1

Introduction

1.1 Introduction

EHV transmission links, superposed on a lower voltage AC network, or inter-connecting two such networks, or connecting distant generating plants to an AC network, are compared as to their principal components and the arrangements thereof, according to whether the line operates on AC or DC. Three phase lines cannot be operated, except for a very short time (less than 1 sec) with one or two conductors open, because such operation causes unbalance voltages in AC system and interference in parallel telephone lines. Therefore,three pole switching is always used to clear permanent faults, although such a fault may involve only one conductor. Long circuits ac links are usually sectionalized by means of intermediate switching stations for several reasons. On long EHV AC lines, shunt reactors are required for limiting the voltage, especially at the light loads. High-voltage transmission has advantages over ac transmission in special situations. The following are the type of applications for which HVDC transmission has been used.

1. Underwater cables longer than about 30 km. AC transmission is impractical for such distances because of the high capacitance of the requiring intermediate compensation stations.

2. Asynchronous link between two AC systems where AC ties would not be feasible because of system stability problems or a difference in nominal frequencies of the two systems.

3. Transmission of large amounts of power over long distances by overhead lines. HVDC transmission is a competitive alternative to ac transmission for distances in excess of about 600 km.

HVDC systems have the ability to rapidly control the transmitted power. Therefore, they have a significant impact on the stability of the associated AC power systems. An understanding of the characteristics of the HVDC systems is essential for the study of the stability of the power system. More importantly,proper design of the HVDC control is essential to ensure satisfactorily performance of the overall AC/DC system. HVDC system is thus,

1.2 Literature survey

Various references have been used for theoretical understandings as well as an aid to the simulation carried out.

1. As an introduction to the fundamental concepts of HVDC, Direct current transmission by Edwards Wilson Kimbark[1] acts as classical guide. It details the operation of converters in a lucid manner and helps build concepts from a basic level. It provides detailed explanations on the rectification and inversion modes of operation and the associated problems like commutation overlap. Emphasis is on thorough understanding and where applicable, all pertinent formulae have been derived from fundamental priciples. The control of the link is explained in great depth, focusing on the subtle nuances of HVDC control.

2. For a quickly covering all the major topics pertaining to line commutated HVDC lines with thyristor valves, Power System Stability by P.S.kundur[2] is an invaluable book. The book servers more like an encyclopedia than a textbook and

chapter 10 of the book on HVDC transmission is a handy reference. It allows us to understand the concepts within a few days if time is limited. It also provides a basic understanding of converter action, overlap, control of the link and the introduction to topics like harmonics and modelling of HVDC lines.

3. HVDC transmission Systems by K.R.Padiyar[6] is a true textbook on the subject. It is an up-to-date book on the subject. Coverage of material is thorough and no topic is left out. The Chapter on harmonics is particularly useful as the chapter is more thorough than [2] and less voluminous than [1]. The book also serves as a quick reference as facts are easily accessible and detailed references are provided for further reading.

4. The research paper The phase-Locked Oscillator- "A New Control System for controlled static converters",J.Ainsworth,IEEE Trans.on power Apparatus and Systems, Vol. PAS-87,No.3, March 1968, pp.859-865 [4]is a seminar paper and it has been absolutely essential for understanding phase locked loop based equidistant pulse firing schemes and gamma detection.

5. HVDC and FACTS controllers: Application of Static Converters in Power Systems by Vijay Sood[3] is another book that provides broad coverage. It also includes various advanced topics for the interested reader.

6. High Voltage Direct Current Transmission by J.Arrillaga[7] is also a good book. It describes the variety of reasons justifying the use of DC transmission as well as basic concepts and techniques involved in the AC-DC and DC-AC conversion process. It also includes the improvements in the ratings and reliabilites of thyristor valves and other semiconductor devices and more controllable solid state devices.

7. Power Electronics by P.C.Sen[7] is a nice book for the understanding of various triggering circuits of the Phase Controlled Converters. It provides basic ideas for designing of different triggering circuits of the converters.

8. Power Electronics by M.D.Singh and K.B.Khanchandani[5] is very essential book for understanding of operation and control of Rectifier and inverters.It gives the knowledge about working and designing of phase controlled rectifier, operation of phase controlled rectifier, working of line commutated inverter and how to set the parameters of phase controlled converter.

9. A seminar paper on PID Controllers by Zoran Vukic and Ognjen Kuljaca is absolutely essential for understanding of PI-Controller. It gives an explanation about basics of On-Off controllers, P-controller, PI-Controller an PID Controllers. It also explains about different topology of PI-Controller, PI-Controller parameters, topology identification and Experimental tuning of the PI-Controller parameters. Different methods for tuning of PI-Controller are used in this seminar paper.

1.3 Objective of Dissertation

A high-voltage direct current (HVDC) electric power transmission system uses direct current for the bulk transmission of electric power, in contrast with the more common alternating current systems. The main objective of the Dissertation is to develop prototype hardware model of HVDC transmission system. For this, simulated model of HVDC transmission system is to build in Simulation software package. For this purpose, thyristor based converters are chosen and firing scheme have been designed. Two major gate firing scheme are to be implemented with circuitry designed:Individual Phase Control scheme and Equidistant Phase Control scheme; along with this the current control, voltage control and power control are also to be implemented. Also, sending end voltage is to be converted into DC by controlled rectifier and again DC voltage is to be converted into AC voltage by line commutated inverter. Bi-directional power flow from rectifier to inverter and inverter to rectifier on HVDC link has been simulated and implemented. Behaviour of HVDC link during the fault occurrence and fault clearance is to be analyzed.

Chapter 2

Line Commutated Converters

A high voltage,direct current (HVDC) electrical power transmission system uses direct current for the bulk transmission of electrical power, in contrast with the more common alternating current systems. Earlier static systems used mercury arc rectifiers, which were unreliable and required high maintenance. The thyristor valve was first used in HVDC systems in the 1960s.

2.1 Rectifying and Inverting system

At the AC ends of the HVDC system, we have a step up transformer before the rectifier and a step down transformer after the inverter. The voltage is stepped up to about 500 kV for the HV system and converted to DC by rectification. The output of the three winding transformer is connected to bridge rectifier formed by a number of valves. At the inverter end, the HVDC is converted to HVAC. Rectification and inversion use essentially the same machinery. Many substations (converter stations) are set up in such a way that they can act as both rectifiers and inverters. The output of the inverter is then stepped down by a three winding transformer back again.

2.2 Types of DC Links

HVDC links may be broadly classified into the following categories:

1. Monopolar links
2. Bipolar links
3. Homopolar links

2.2.1 Monopolar link

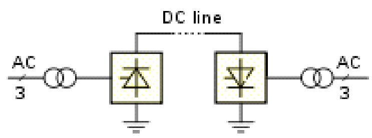


Figure 2.1: Monopolar link

It uses one conductor, usually of negative polarity. The return path is provided by ground or water. Cost consideration often lead to the use of such systems, particularly for cable transmission. This type of configuration may also be the first stage in the development of a bipolar system. Instead of ground return, a metallic return may be used in situations where the earth resistivity is too high or possible interference with underground/underwater metallic structure is objectional. The conductor forming the metallic return is at low voltage.

2.2.2 Bipolar link

It has two conductors, one positive and the other negative. Each terminal has two converters of equal rated voltage, connected in series on the DC side. The junctions between the converters is grounded.Normally, the currents in the two poles are equal, and there is no ground current. The two poles can operate independently. If one pole

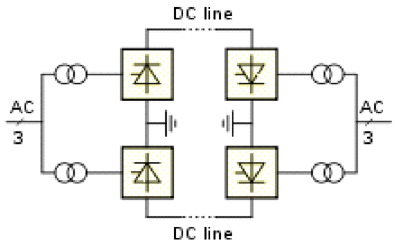


Figure 2.2: Bipoloar link

is isolated due to a fault on its conductor, the other pole can operate with ground and thus carry half the rated load or more by using the overload capabilities of its converters and line.

2.2.3 Homopolar link

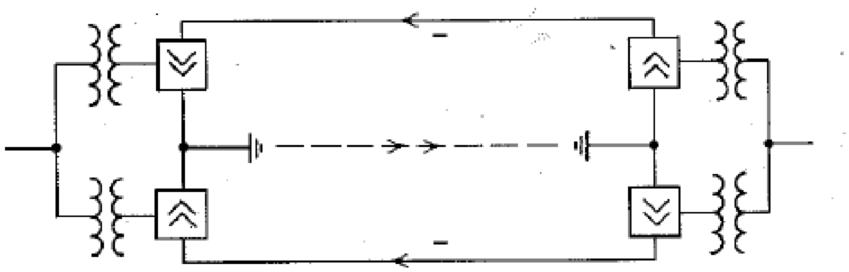


Figure 2.3: Homopolar link

It has two or more conductors, all having the same polarity. Usually a negative polarity is preferred because it causes less radio interference due to corona. The return path for such a system is through ground. When there is a fault on one conductor, the entire converter is available for feeding the remaining conductors which, having some overload capability, can carry more than the normal power. In contrast, for a bipolar scheme usually not feasible. Homopolar configuration offers an advantage in this regard in situations where continuous ground current is acceptable.

2.3 Converter theory and performance equation

The most commonly used converter circuit is the Graetz circuit shown below.

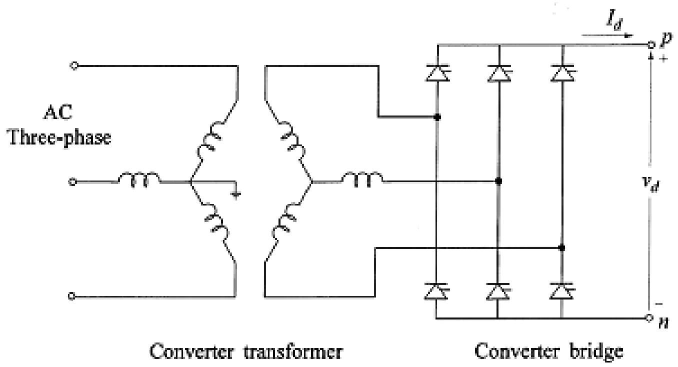


Figure 2.4: Graetz circuit

The line to neutral voltages or phase voltages are,

$$e_a = E_m cos(\omega t + 60^o) \tag{2.1}$$

$$e_b = E_m cos(\omega t - 60^o) \tag{2.2}$$

$$e_c = E_m cos(\omega t - 180^o) \tag{2.3}$$

Where as the line to line voltages are:

$$e_{ac} = e_a - e_c = \sqrt{3} E_m cos(\omega t + 30^o) \tag{2.4}$$

$$e_{ba} = e_b - e_a = \sqrt{3} E_m cos(\omega t - 90^o) \tag{2.5}$$

$$e_{cb} = e_c - e_b = \sqrt{3} E_m cos(\omega t + 150^o) \tag{2.6}$$

For the purposes of analysis we need to make the following assumptions:

1. We represent the AC system, including the converter transformer, by an ideal source of constant voltage and frequency in series with a lossless inductance.

This inductance represents primarily the transformer leakage inductance.

2. The direct current I_d is constant and ripple-free. This is justified since there's a large smoothing reactor L_d on the DC side.

3. The valves are considered ideal switches. This means they are assumed to have zero resistance when conducting and infinite resistance when not conducting.

Thus the general circuit is: We will now consider three situations:

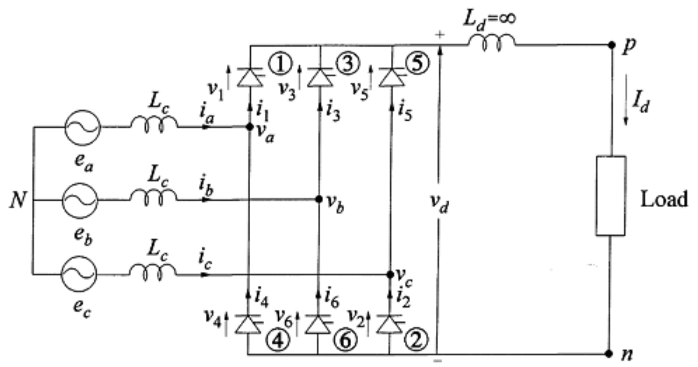


Figure 2.5: General circuit for modeling HVDC converters

1. When the value of inductance is negligible (there's no overlap) and no ignition delay ($\alpha = 0$) is set

2. No overlap but ignition delay is set

3. The effects of both overlap and ignition delay are considered.

Case 1: No overlap and no ignition delay The waveforms in this case are similar to that of an uncontrolled 3-phase rectifier. The firing sequence of the valves is T_1, T_2, T_3, T_4, T_5 and T_6. There is 60^o phase difference between the ignitions of any two valves, and 120^o between the ignition of two valves in the same row (upper or lower). Thus, each valve conducts for 120^o.

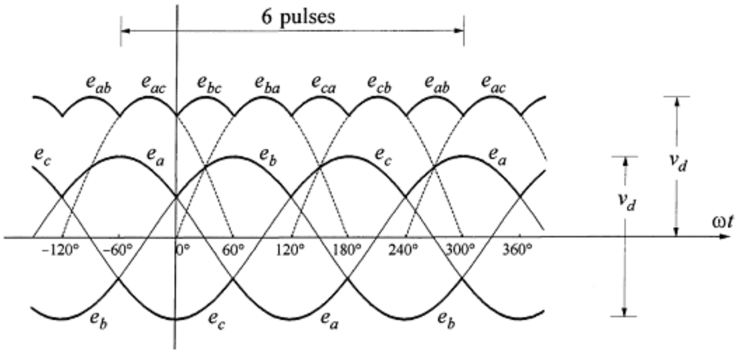


Figure 2.6: Line voltages and phase voltages

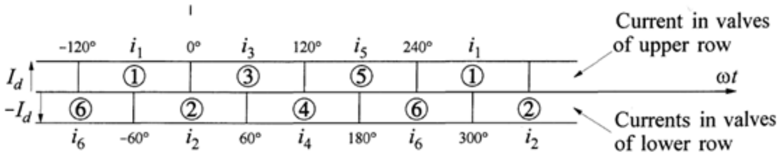


Figure 2.7: Valve currents and periods of conduction

Source line-to-neutral and line-to-line voltages

Let us understand the commutation process by considering the period between 0^o and 120^o. When ωt $= 0^o$, e_b becomes more positive than ea and hence valve 3 is fired. Now, the voltage across valve 1's cathode is e_b and anode is e_a. Since the cathode is more positive with respect to the anode, this valve is reverse biased and hence turned off. Similarly, at ωt $= 60^o$, e_a is more negative than e_c, and hence valve 4 ignites and valve 2 extinguishes. The valves in the upper row carry positive current and those in the lower row carry negative (or return) current. Thus the phase current i_a is equal to i_1 - i_4. This waveform is shown below The average direct voltage is calculated by considering any one 60^o pulse as follows:

$$V_{do} = \frac{3}{\pi} \int_{-60}^{0} e_{ac}\, d\theta \tag{2.7}$$

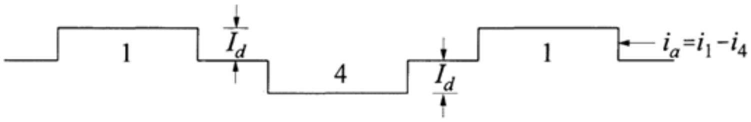


Figure 2.8: Phase current waveform

We express V_{do} in terms of the RMS line-to-line and line-to-neutral voltages,

$$V_{do} = (\frac{3\sqrt{6}}{\pi}) \int_{-60}^{0} e_{ac}\, d\theta = 2.34 E_{LN} \tag{2.8}$$

$$V_{do} = (\frac{3\sqrt{2}}{\pi}) \int_{-60}^{0} e_{ac}\, d\theta = 1.35 E_{LL} \tag{2.9}$$

Case 2: With ignition delay but no overlap In this case the ignition of the valves is delayed by an angle α. This angle, called the firing angle or ignition angle, is limited to 180^o. To explain this limitation, let us take the example of valve 3. When ωt is greater than 180^o, then e_b is less than e_a and hence valve 3 does not ignite. The average direct voltage is calculated over the 60^o interval obtained by increasing the limits of the integral in the previous case (Case 1) by α.

$$V_d = V_{do} \cos\alpha \tag{2.10}$$

Thus, by controlling the ignition angle the ignition angle the average voltage can be varied between the limits plus and minus V_{do}. Negative V_d corresponds to inversion. It can be shown by Fourier analysis that the angle by which the fundamental line current lags the line-to-neutral source voltage ϕ=α. Thus, $\cos\phi$ =$\cos\alpha$ The term $\cos\phi$ is called the displacement power factor. As α increases up to 180^o, real power decreases and reactive power increases, until at 180^o real power is zero and reactive power is maximum. After that till 180^o real power becomes more and more negative whereas reactive power remains positive but decreases. At ω = 180^o real power is

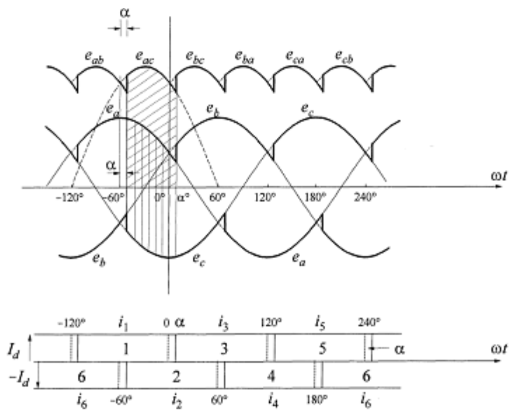


Figure 2.9: The effect of the delay in ignition on the waveforms

negative maximum and reactive power is zero.

Case 3: The effects of both overlap and ignition delay are now considered
Due to the source inductance L_c, the current cannot change instantly from one phase to another. A finite amount of time known as the commutation time is required. This is specified by the commutation angle μ. We'll consider the most common case where $0^0 < \mu < 60^0$ In such a situation either two or three valves conduct simultaneously. During commutation, the current in one valve reduces to zero whereas the current in the other valve increases to I_d. This is illustrated in the figure below The angle δ at

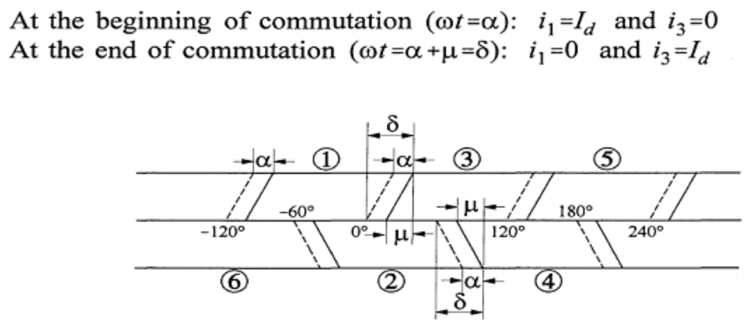


Figure 2.10: The effect of commutation overlap

which the commutation ends is called the extinction angle.

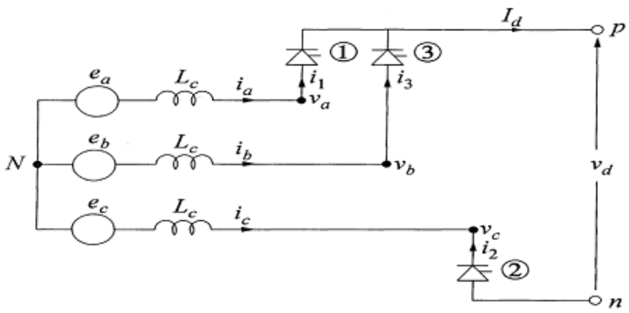


Figure 2.11: The circuit commutation from valve-1 to valve-3

$$e_b - e_a = L_c \frac{di_3}{dt} - L_c \frac{di_1}{dt} \tag{2.11}$$

The voltage e_b-e_a is the "commutating voltage". It's equal to the line voltage mentioned at earlier equation. Using those formulae we get:

$$\sqrt{3}E_m \sin(\omega t) = L_c \frac{di_3}{dt} - L_c \frac{di_1}{dt} \tag{2.12}$$

Since,$i1 = I_d - I_3$

$(\frac{di_1}{dt}) = -(\frac{di_3}{dt})$

Hence,$(e_b - e_a) = \sqrt{3}E_m \sin \omega t = 2L_c \frac{di_3}{dt}$

$$\frac{di_3}{dt} = \frac{\sqrt{3}E_m \sin \omega t}{2L_c} \tag{2.13}$$

$$i_3 = I_{s2}(\cos\alpha - \cos\omega t) \tag{2.14}$$

$$I_{s2} = \frac{\sqrt{3}E_m}{2\omega L_c} \tag{2.15}$$

Thus the current i_3 has a constant component and a sinusoidal component. This is to be expected since there is an effective line to line short-circuit via an inductance of $2L_c$. $i_1 = I_d$ - i_3. Also, the overlap is shortest when $\alpha = 90^o$, since for this ignition angle i_3 is associated with the segment of the sine wave which is linear. These concepts are illustrated below: During Commutation,

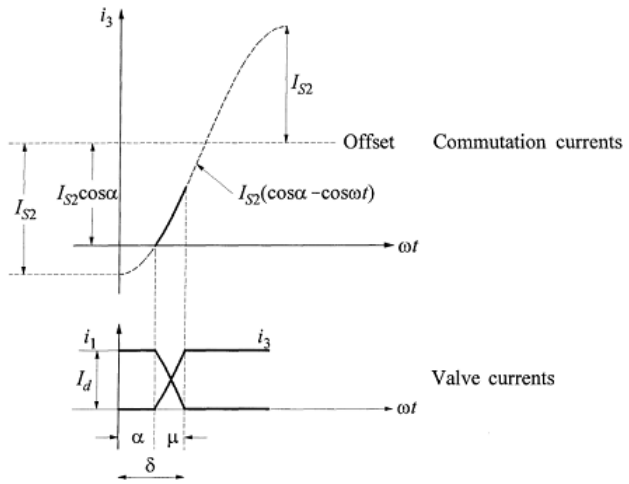


Figure 2.12: The effect of commutation overlap

$$v_a = v_b = e_b - L_c \frac{di_3}{dt} \tag{2.16}$$

As,We have derived earlier,

$$L_c \frac{di_3}{dt} = \frac{e_b - e_a}{2} \tag{2.17}$$

$$v_a = v_b = e_b - \frac{e_b - e_a}{2} = \frac{e_a + e_b}{2} \tag{2.18}$$

The corresponding average voltage drop can be calculated as shown:

$$\Delta V_d = \frac{V_{do}}{2}(\cos\alpha - \cos\delta) \tag{2.19}$$

This voltage drop ΔVd can be expressed as $RcId$ where Rc is called the "equivalent commutating resistance", it accounts for the voltage drop due to resistance; however its not a real resistance and it doesn't consume any power.

Equivalent circuit of a rectifier

At the end of commutation $\omega\mathrm{t} = \delta$ and $i_3 = I_d$, hence,

$$I_d = \frac{\sqrt{3}E_m}{2\omega L_c}(\cos\alpha - \cos\delta) \tag{2.20}$$

Hence,

$$\frac{\sqrt{3}E_m}{2}(\cos\alpha - \cos\delta) = I_d\omega L_c \tag{2.21}$$

Substituting ΔV_d value in equation(1.20),

Thus,for rectifier we have, $V_d = V_{do}\cos\alpha - R_c I_d$,

Where, $R_c = \frac{3}{\pi}(\omega L_c) = \frac{3}{\pi}X_c$

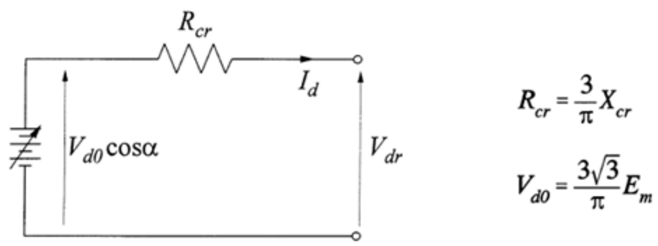


Figure 2.13: Equivalent circuit of rectifier

Equivalent circuit of an inverter

$$V_d = V_{do}\cos\alpha - \Delta V_d \tag{2.22}$$

The voltage from the converter becomes negative when $\alpha > 90$. This is called the inversion mode. In this mode, the direct voltage of the inverter opposes the current from the rectifier, as in a DC motor, and is called a counter-voltage or back voltage. The direct voltage from the rectifier forces the current through the inverter valves against this voltage. While for the description of the rectifier we use the following angles:

α = ignition delay angle

μ = overlap angle

δ = ignition delay angle $=\alpha + \mu$

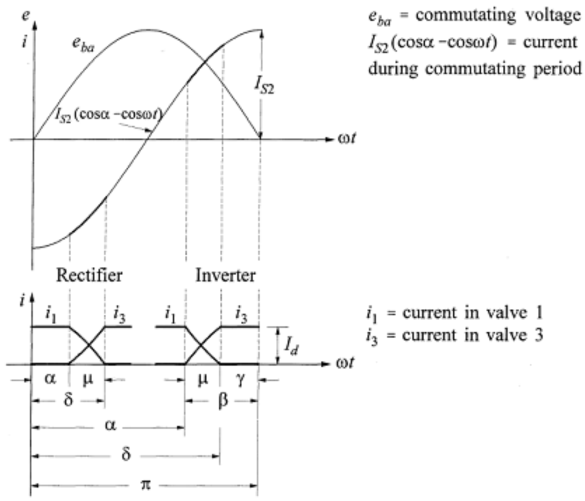
The inverter the angles used are:

$\beta = \pi - \alpha$ = Ignition advance angle

$\gamma = \pi - \delta$ = Extinction advance angle

$\mu = \delta - \alpha = \beta - \gamma$ = Overlap

Substituting equations,



$$V_d = \frac{V_{do}}{2}(\cos\alpha - \cos\delta) \tag{2.23}$$

Now since, $\cos\alpha = -\cos\beta$ and $\cos\delta = -\cos\gamma$ from equations,we get following equations involving γ and β,

$$I_d = I_{s2}(\cos\gamma - \cos\beta) \tag{2.24}$$

$$V_d = \frac{V_{do}}{2}(\cos\gamma - \cos\beta) \tag{2.25}$$

$$V_d = V_{do}\cos\beta + R_c I_d \tag{2.26}$$

Equation(1.26) may also be written as,

$$V_d = V_{do} \cos \gamma - R_c I_d \tag{2.27}$$

From equation(1.25) and equation(1.26) we get following circuits,

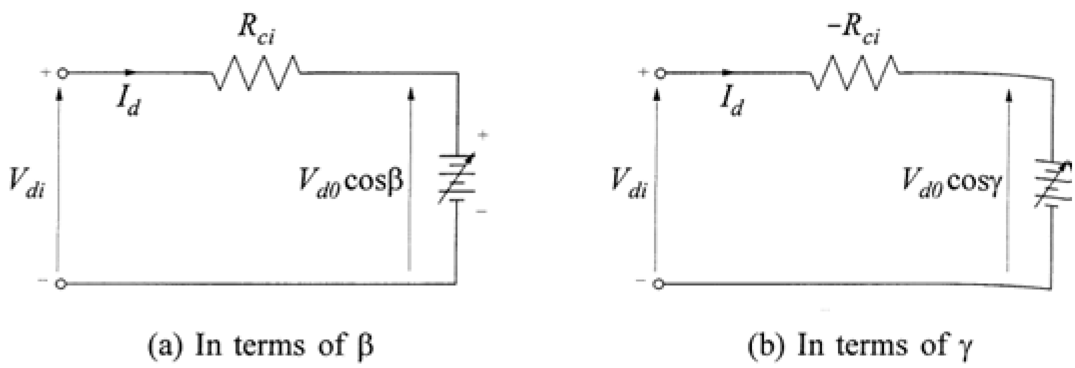


Figure 2.14: The Equivalent circuit of inverter

Chapter 3

Control of Line Commutated Converters

The following is the general circuit for a mono-polar HVDC link. This can be rep-

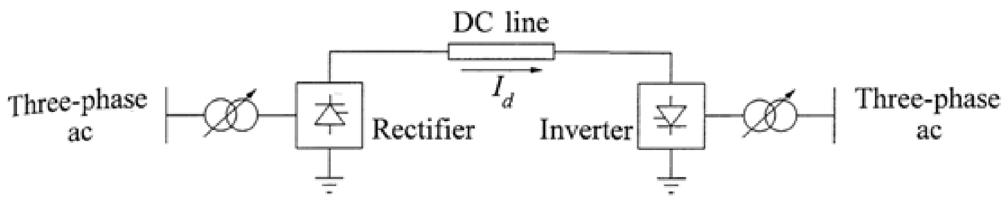


Figure 3.1: Mono-pole HVDC link

resented by its equivalent circuit, using the equivalent circuits of the inverter and rectifier. As can be seen the current can only flow in one direction through the converters. In order to transfer power to the second power system the current must flow against the DC voltage as in the case of a DC motor; this is why inversion of the voltage across the second converter is required. The voltage profile across the line is shown below: The Direct current flowing from the rectifier to the inverter is

$$I_d = \frac{V_{dor}\cos\alpha - V_{doi}\cos\gamma}{R_{cr} + R_L - R_{ci}} \tag{3.1}$$

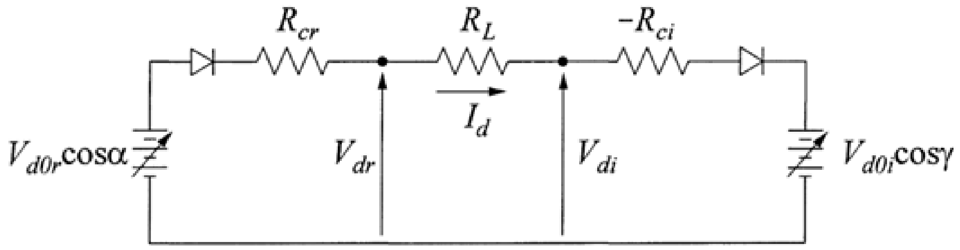


Figure 3.2: Equivalent circuit of Mono-pole HVDC link

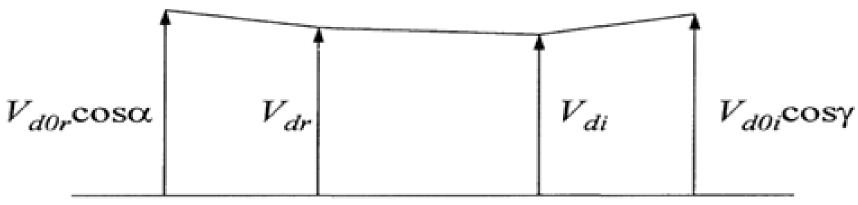


Figure 3.3: Voltage characteristic of Mono-pole HVDC link

The power at the rectifier terminal is,

$$P_{dr} = V_{dr} I_d \tag{3.2}$$

and at the inverter terminal is,

$$P_{di} = V_{di} I_d = P_{dr} - R_L I_d^2 \tag{3.3}$$

Basic Requirements of controls

There are two basic ways to control an HVDC link, one is by varying the firing angle (which controls the voltage rapidly within milliseconds) and the other is by tap changing which takes 5 to 6 seconds. Initially the firing angle scheme is used to rapidly control the voltage and then tap changing at the converters is used to bring α and γ to their normal values. The following are some of the factors that need to be kept in mind while designing the control system of the link:

1. We need to prevent the variation of DC current due to variation in AC system voltage. A small change in the values of V_{dor} and V_{doi} can lead to large variations in the value of I_d for which rapid converter control of α and γ is required.

2. We need to maintain the direct voltage profile across the line close to the rated voltage level since then the DC current will be lower leading to lower line losses.

3. We need to maintain the power factors at the sending and receiving end at a value which is as high as possible. This is because a high power factor leads to high rated power for the given current and voltage ratings of the transformer and valve, reduced stresses in the valves, lower losses in the AC system, lower voltage drops at the AC terminals as loading increases and lower cost of reactive power supply to converters.

4. We need to prevent commutation failure in inverters. Commutation failure in inverters lead to one thyristor valve conducting for a longer duration, and hence this causes dead short circuits since both the upper and lower valves on one leg of the bridge conduct for some time.

While designing the control strategy, it's important to keep in mind that there's a minimum α limit of 5^o. This is to ensure adequate voltage across the valve before firing. The rectifier normally operates at a value of α within the range of $15^o$to 20^o so as to leave some room for increasing rectifier voltage to control DC power flow. In the case of an inverter it is necessary to maintain certain minimum extinction angle to avoid commutation failure and allow sufficient margin for de-ionization before commutating voltage reverses. Sufficient commutation margin above the minimum γ limit must be maintained; the value of γ with acceptable margin is 15^o for 50 Hz systems and 18^o for 60 Hz systems.

Ideal Characteristics

Under normal conditions the inverter is operated in the Constant Extinction Angle (CEA) mode and the rectifier is operated in the Constant Current (CC) mode. The control of the current is handled by the rectifier and that of the voltage by the inverter. Although the voltage of the inverter in the CEA mode is ideally constant, in reality it is given by the equation

$$V_d = V_{doi} \cos \gamma + (R_L - R_{ci}) I_d \tag{3.4}$$

Thus, the inverter characteristic is a horizontal line has a small negative slope. With only proportional control the rectifier characteristic has a large negative slope whereas with proportional and integral control the characteristic is nearly a straight vertical line.

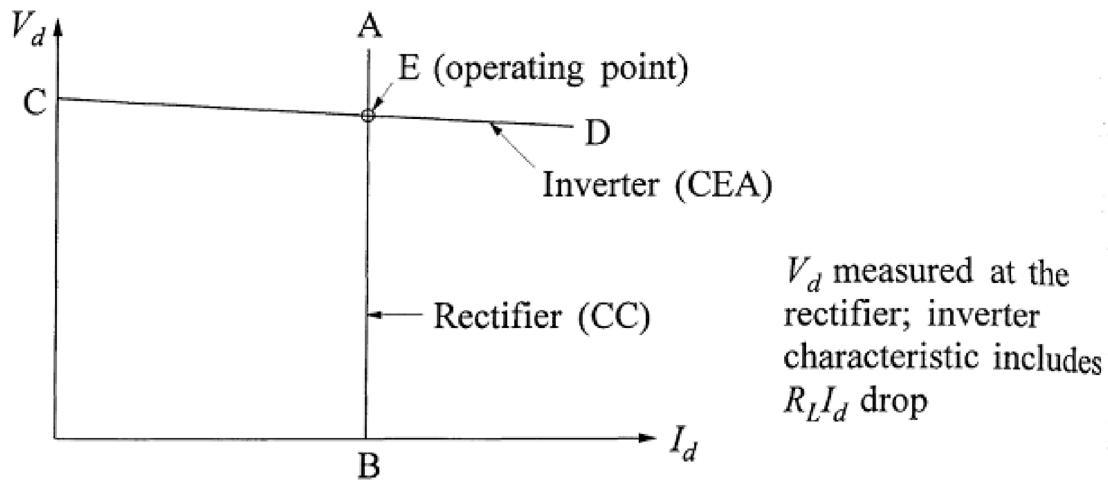


Figure 3.4: Ideal characteristics of converters

Actual Characteristics

The rectifier maintains constant current by changing α. However, the α value is limited to a value α_{min} as explained earlier. Thus, beyond this value of α the voltage becomes constant as α is fixed. This is called the Constant Ignition Angle (CIA) control mode. In this mode the rectifier maintains the voltage constant and the current varies. As shown in the figure below, the system initially operates at the point E where the rectifier and inverter characteristics meet. At this point the value of I_d and V_d is such that they satisfy both the rectifier and inverter equations and power can be transferred. Supposing there is a reduction in voltage on the rectifier side due to a fault (FA B), this leads to a situation where the inverter characteristic doesn't intersect with the rectifier one and the system runs down since no operating point can be obtained. To prevent this situation from arising, the inverter is also equipped with a current controller whose current setting is lower than that of the rectifier. Thus, beyond a certain value of current the inverter works in the constant current mode. The difference between the rectifier current order and the inverter current order is I_m which is called the current margin. Hence, in the case of a fault the operating point shifts to E, wherein the inverter now maintains constant current and rectifier maintains constant voltage.

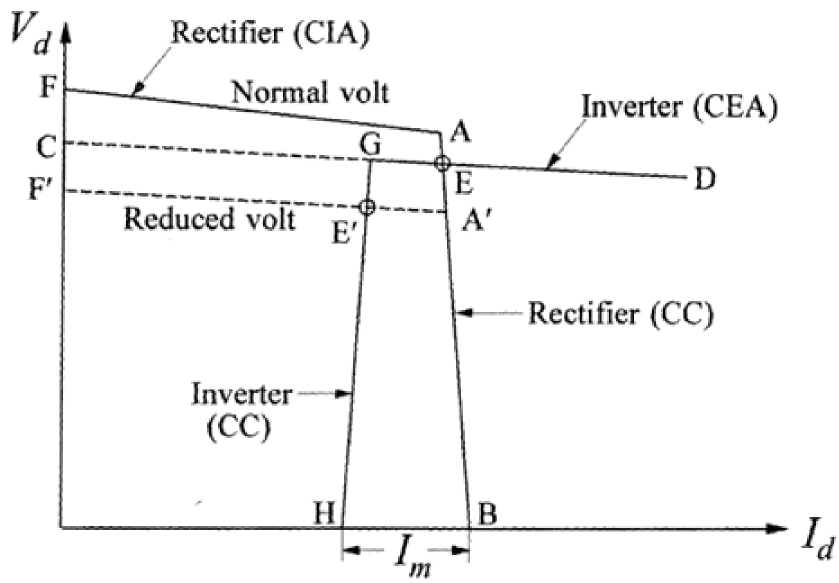


Figure 3.5: Actual characteristics of converters

Current Limits

While establishing the current order we need to consider the following current limits:

1. **Maximum Current Limits**

   The maximum short-time current is usually limited to 1.2 to 1.3 times normal full-load current, to avoid thermal damage to valves.

2. **Minimum Current Limits**

   This is required because at low values of current, the current waveform can become discontinuous. This leads to high voltage due to Ldi/dt in the transformer windings and DC reactor. Moreover, the overlap is small and hence the two jumps in direct voltage at the beginning and end of commutation merge to form one jump twice as large, resulting in an increased stress on the valves.

3. **Voltage Dependent Current Order Limit(VDCOL)**

   The voltage drop (by more than 30 percent of rated voltage) at one converter leads to increased leads to increased reactive power demand of the remote converter. Furthermore, at reduced voltages, there are also risks of commutation failure and voltage instability. These problems can be prevented by the VDCOL, whose characteristics may be a function of the ac commutating voltage or the DC voltage. The figure below shows the characteristics as a function of the alternating voltage: The figure below shows the characteristics as a function of the direct voltage. The V-I characteristics shown below demonstrate that the inverter characteristics match the rectifier characteristics in order to maintain the current margin. For VDCOL operation the measured direct voltage is

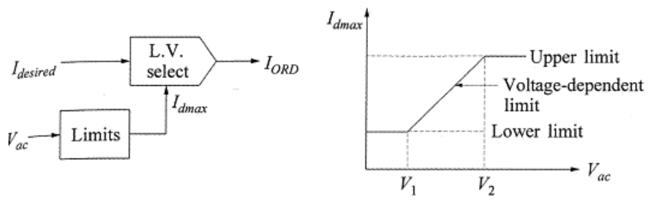


Figure 3.6: VDCOL characteristics of converters

passed through a first order time lag element. When the voltage is going down, fast action is required; hence the time-lag is small. On the other hand, when voltage is recovering, a small time lag may lead to oscillations and instability. Therefore, in this case a larger time-lag is required.

Chapter 4

Analysis of Simulation Results

4.1 Basic circuit of Rectifier and Inverter

The first simulation consists of line commutated converters operating without ignition and extinction angle control. The firing angle alpha(α) is 20^o for rectifier and 170^o for inverter. The fig. shows the controlled rectifier for 415 V, 50 Hz supply. The firing angle alpha is set at α=20^o for rectifier and α=160^o for inverter.

The firing sequence of thyristor is T_1=-100^o,T_2=-40^o,T_3=20^o,T_4=80^o,T_5=140^o and T_6=200^o. The per phase resistance of 3-phase induction motor is 12 Ω/phase.

The firing sequence of thyristor for inverter is T_4=130^o,T_5=70^o,T_6=10^o,T_1=50^o, T_2=110^o and T_6=200^o. Rectifier side the current flows from the negative end to the positive end and hence power is transmitted. The current through the valves can flow in only one direction. Thus, to deliver power to the inverter, we need to invert the voltage so that current flows from the positive end to the negative end against induced voltage. The direct voltage of the inverter opposes the current,as in a dc motor, and is called a counter voltage or back voltage. The applied 700 V DC volt forces current through the inverter valves against this back voltage.

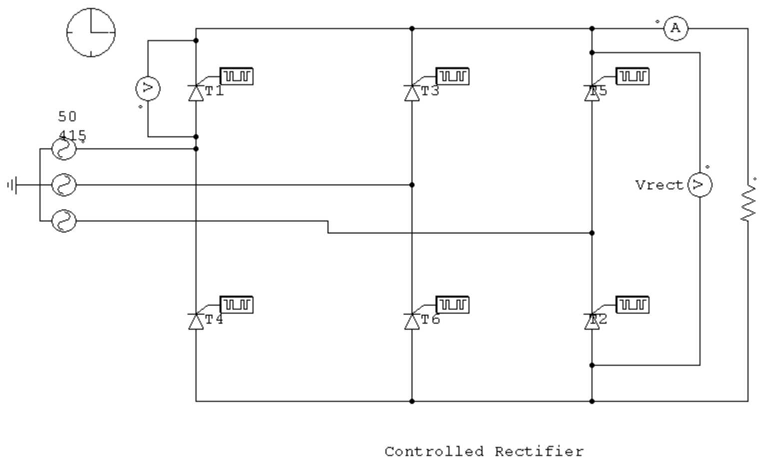


Figure 4.1: controlled rectifier

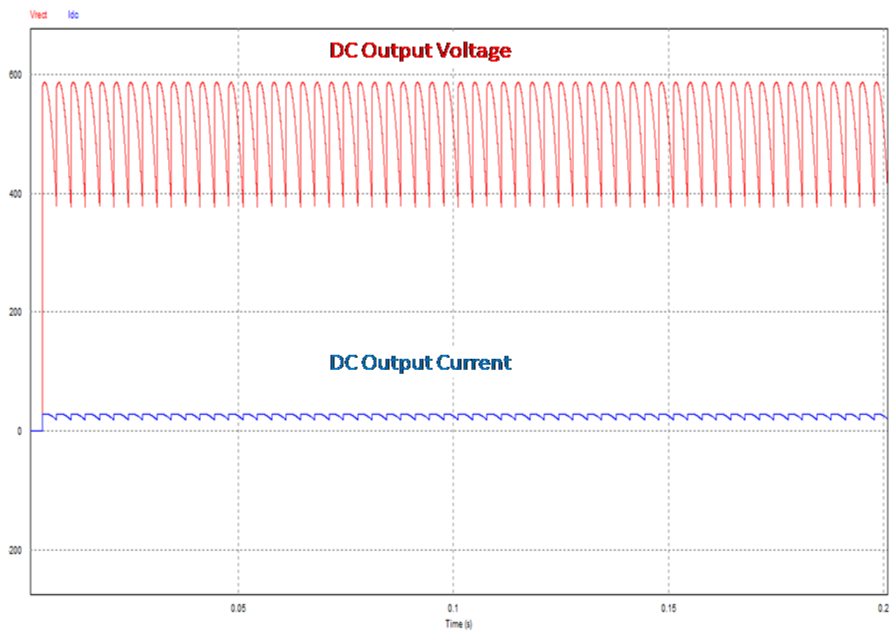


Figure 4.2: Waveform of controlled rectifier

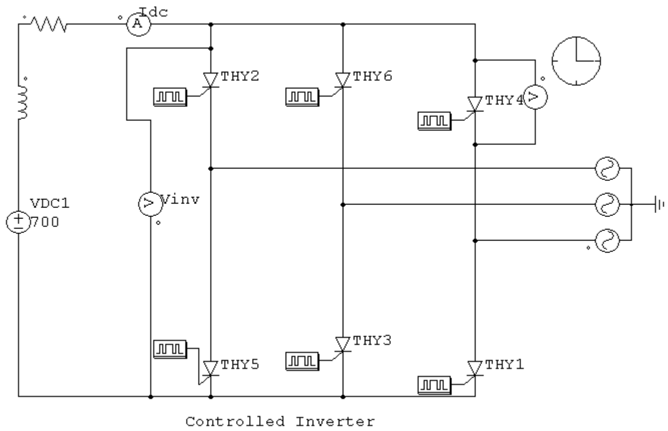


Figure 4.3: Line Commutated Inverter

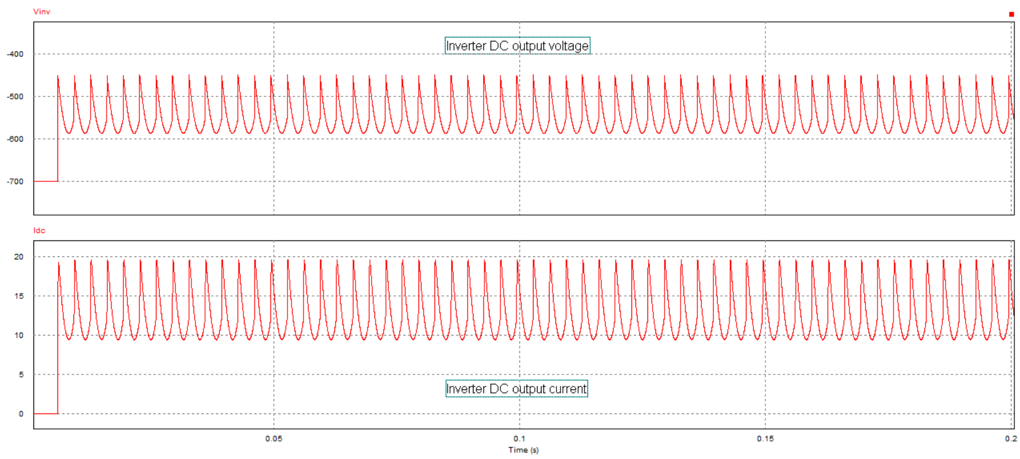


Figure 4.4: Waveform of line Commutated Inverter

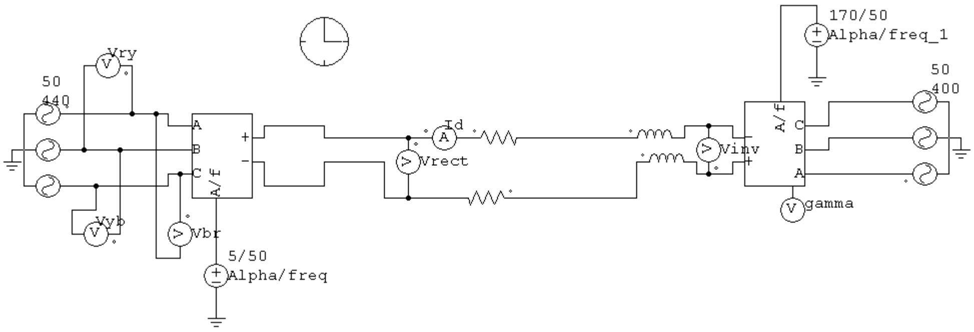


Figure 4.5: Main circuit of HVDC link

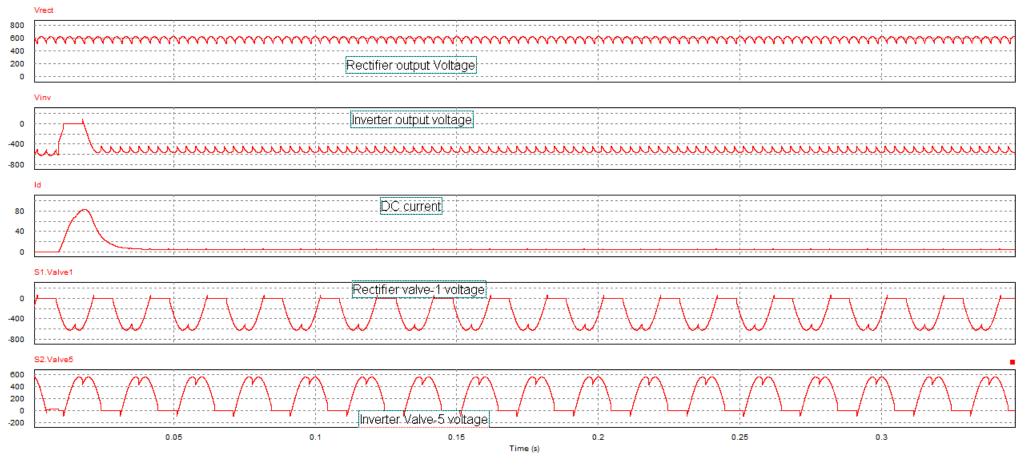


Figure 4.6: waveforms of DC voltage,DC current and thyristor voltage

4.2 IPC scheme for 6-pulse converter based on HVDC link

4.2.1 Main-circuit

In this system, we are simulating a complete HVDC link. A 50 Hz, 440 V system is connected to a 50 Hz, 400 V AC system via the HVDC link (in this experiment,it is cable). The DC line consists of smoothing inductance of 23 mH and resistance of 6 Ω (equally divided between the upper and lower link). We can set the alpha

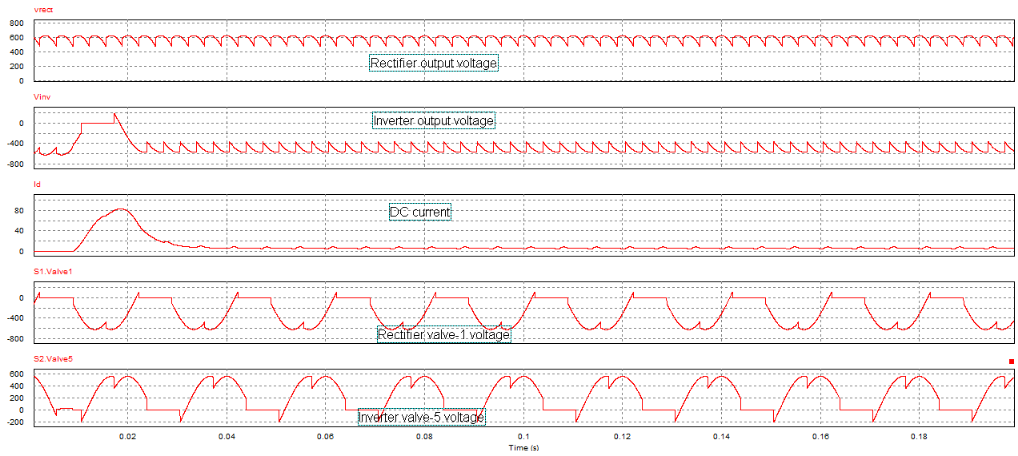


Figure 4.7: Waveform of DC voltage,DC current and thyristor voltage

values of the two converter blocks through a DC voltage signal equal to the value 'alpha/frequency'. This has been demonstrated in the link, with the rectifier working at an alpha of 5^o and the inverter at an alpha of 170^o. The Gate firing unit employed here utilizes constant alpha firing method. As will be explained, (with the detailed circuitry inside the sub-circuit representing the converter) the zero-crossing of the respective valve voltages is detected by using a zero-crossing detector and a phase shift circuit is used to provide the requisite phase shift corresponding to α. Fig-4.6 and Fig-4.7 show the rectifier output voltage, the inverter output voltage, the DC current, the voltage across valve 1 of the rectifier and the voltage across valve 5 of the inverter respectively. Slight ripple is observed in the rectifier and inverter output voltages and the waveform of the current. However, the system performs the basic function of rectifying AC to DC, transmitting DC and inverting it back to AC. The valve voltage waveforms are as expected and regular gating pulses are observed.

The two waveforms (shown above) show the difference in waveforms when the α value is modified. The first set of waveforms, show the rectifier and inverter operating at 5^o and 170^o respectively. The next set of waveforms (fig-4.7) shows the operation at 10^o and 160^o respectively. This shows the ability of the system to modify α. In this system, the α value of each individual phase is controlled individually. Hence it's called Individual Phase Control.

4.2.2 Sub-circuit of Line commutated Inverter

As shown in the circuit above (fig-4.12), each converter sub-circuit consists of a 3-phase voltage source being fed to a Graetz bridge circuit with 6 thyristor valves. The phase voltages are sensed by voltage sensors and they act as input to a zero-crossing detector which calculates the line voltages and detects the zero-crossing of the appropriate commutation voltage for each valve. The zero-crossing of the commutation voltages mark the beginning of the range over which the valves can be turned on. The six output signals of the zero-crossing detector are fed to six circuits which apply the required phase shift before sending the pulses to the thyristor gating circuits.

Explanation

As shown in fig-4.8, a definite voltage (value V=100 volt) is connected to the input of the re-settable integrator and the integrator's time constant is set appropriately (100/360). When a pulse is applied to the integrator from the zero-crossing detector, the integrator produces a ramp waveform which is compared to the reference (alpha/frequency). The integrator time constant, value of the constant voltage and the reference are chosen such that the integrator value becomes greater than the reference value after the required phase shift corresponding to alpha. At that instant a pulse is generated which is given to the IGBT switch. Turning this on generates a voltage output; this output is grounded after a fixed time delay. Thus a fixed pulse is created whose width depends on the time delay. This delay is set using the analog circuit shown in the figure above. When the input to the gate of the IGBT becomes positive, the capacitor starts charging. Initially, the voltage drops entirely across the resistor and hence the voltage at the negative terminal of the capacitor is greater than the fixed voltage at the positive terminal (0.001 not shown in the figure). When the capacitor is fully charged, the voltage across the resistor is zero, i.e. less than 0.001. Thus the comparator output becomes positive and turns on the second IGBT switch

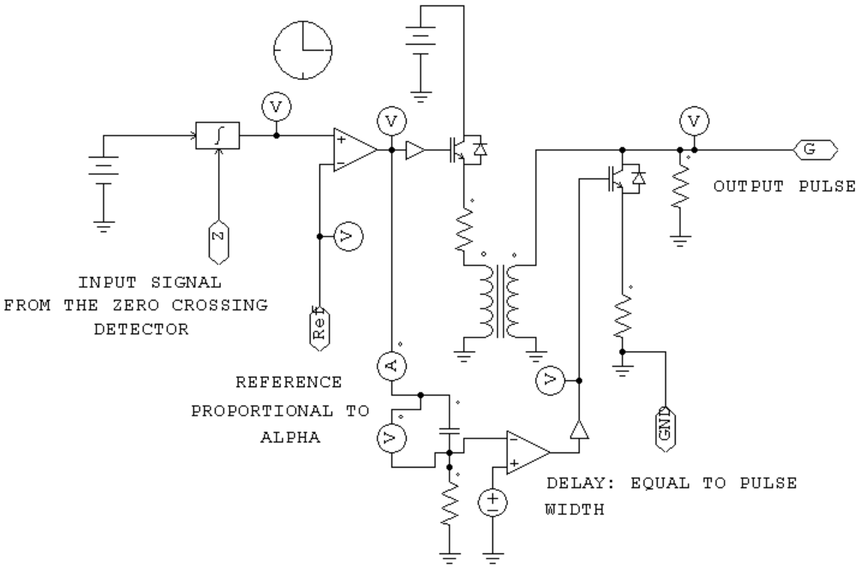


Figure 4.8: Phase shift circuit of converter

which grounds the output of the transformer thus bringing the gating pulse voltage to zero. Thus the resistor and capacitor set the time delay.

4.2.3 Rectifier control system

The control block accepts the actual line current and the current reference as the input, obtains the error, sends it to a PI controller to generate the alpha value and then passes it via a limiter to limit the alpha value. The final alpha value is divided by the frequency to generate the 'alpha/frequency' value which is sent to the converter. The PI controller is tuned as explained below.

4.2.4 Tuning of PI controller

Here, Ziegler-Nichols close loop method is use for the tuning of the PI controller but the general approach is as follow.

1. Initially have no integral gain(T_i large).

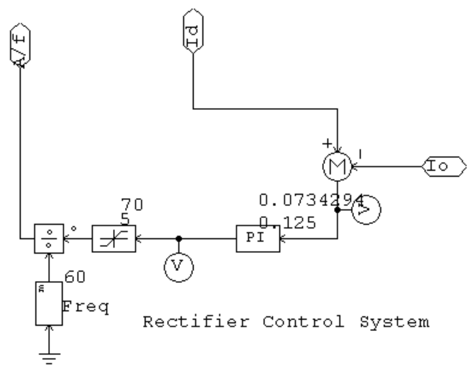


Figure 4.9: Rectifier Current control of converter

2. Increase K_p until get satisfactory response.

3. Start to add in integral (decreasing T_i) until the steady state error is removed in satisfactory time (may need to reduce K_p if the combination becomes oscillatory)

The value of 'P' that causes continuous oscillation is called critical (ultimate) gain, K_{cu}. The peak to peak period i.e. the time between successive peaks in the continuously oscillating process output, is called critical period, Pu. Then for PI controller, the values to be used are: Gain=0.45 K_{cu}, Time Constant= Pu/1.2 (CIGRE HVDC BENCHMARK)

4.2.5 Power control of HVDC system

The preset power is divided by the voltage V_d to get the current reference. Also, the threshold voltage (V_{th} - voltage below which the VDCL acts) is set. The input parameters are V_d, V_{th}, I_{ref} and I_{min}. After the voltage gets in the operating range (below V_{th}), the current reference is proportional to the slope of the falling voltage and the reference falls till minimum current limit is attained (I_{min}). The rectifier control block accepts the current order from the power control block and the real current in order to take corrective action based on the error. The corrective action involves

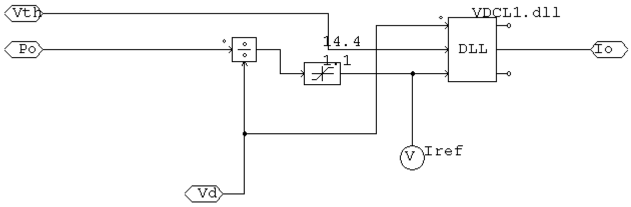


Figure 4.10: Power control of converter

changing the alpha value (it uses a PI controller) while the inverter control system operates based on the detected value of the gamma in order to prevent commutation failure.

4.2.6 Inverter control system

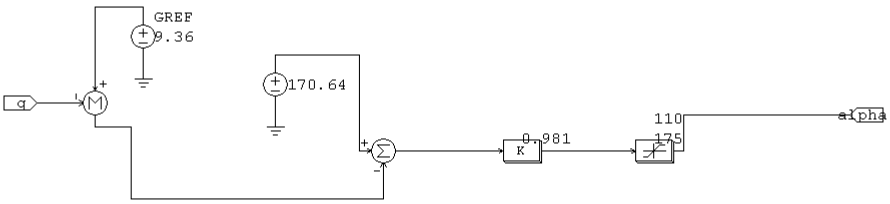


Figure 4.11: CEA control of inverter

The CEA (constant extinction angle) control takes the gamma value as input from the converter compares it with the reference and generates the gamma error. This is subtracted from 170.64^o to get the alpha value which is passed through the proportional controller to get the alpha output. This alpha value is the output of the block; the output of the block is then divided by the frequency to get the 'alpha/frequency' value which is sent to the converter.

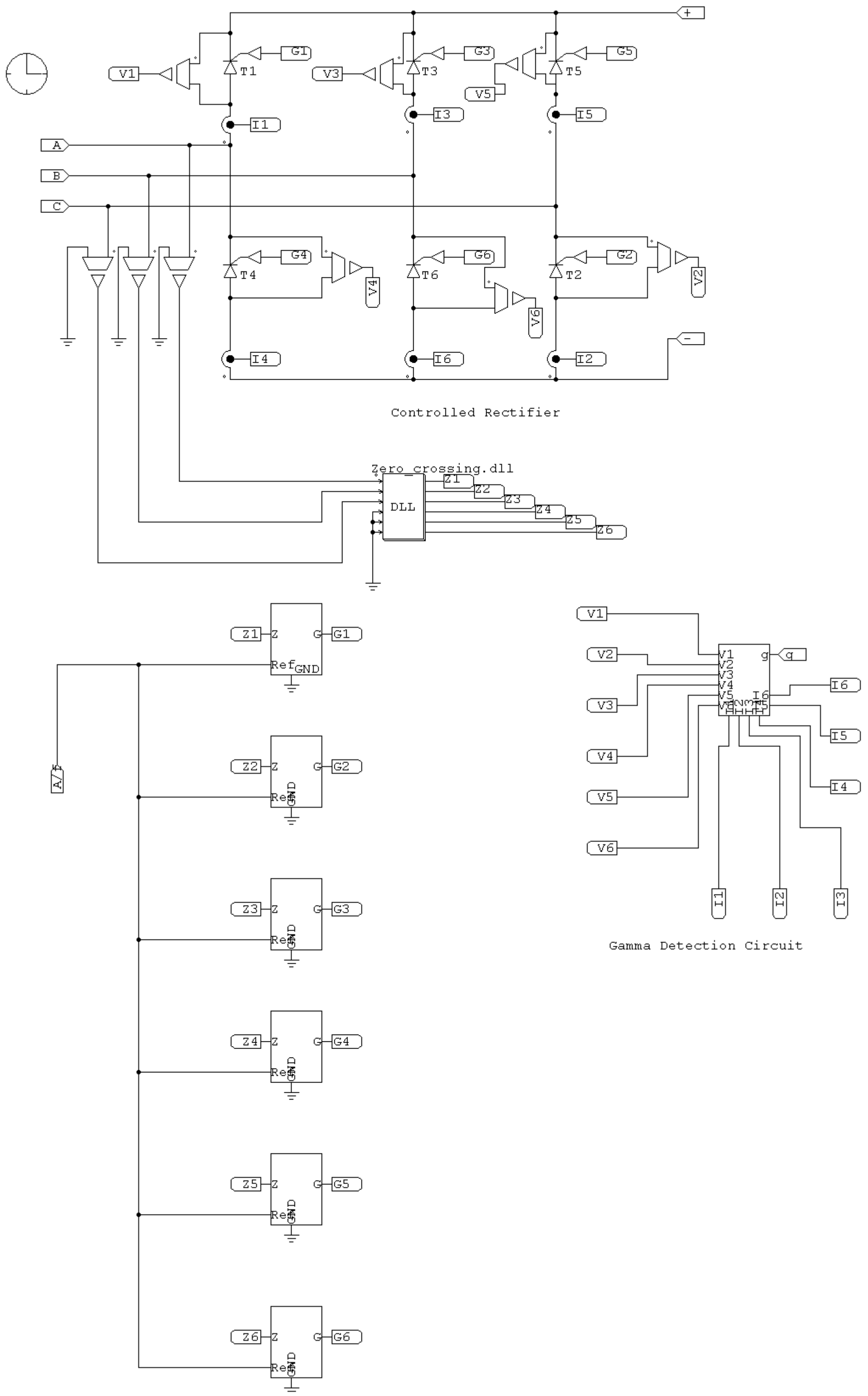


Figure 4.12: Inverter system of converter

4.2.7 Circuit for Inverter system

As seen from the circuit above the voltage across the six valves and the current through them are sensed and given to the gamma detection circuit. This circuit detects the current zero and calculates the duration during which the voltage is greater than zero (transiently) to determine the gamma value (the gamma value is the duration of the voltage spike across the valves expressed in degrees). The gamma value for all the valves is calculated and the minimum value is output from the circuit.

4.2.8 Sub-circuit of gamma detection

As seen above, for each valve, when the current becomes less than 0.09 (considered current zero) a pulse is generated by one of the comparators, whereas the output of the other comparator becomes positive when the voltage becomes positive for the respective valve voltage. Only when both the input are positive, does the output of the AND gate become positive. The width of this pulse is calculated by the pulse width counter and it is divided by the time period (1/50 = 1/frequency) and multiplied by 360 to get the gamma value in degrees. This is sent to the minimum gamma detector which outputs the minimum value of gamma.

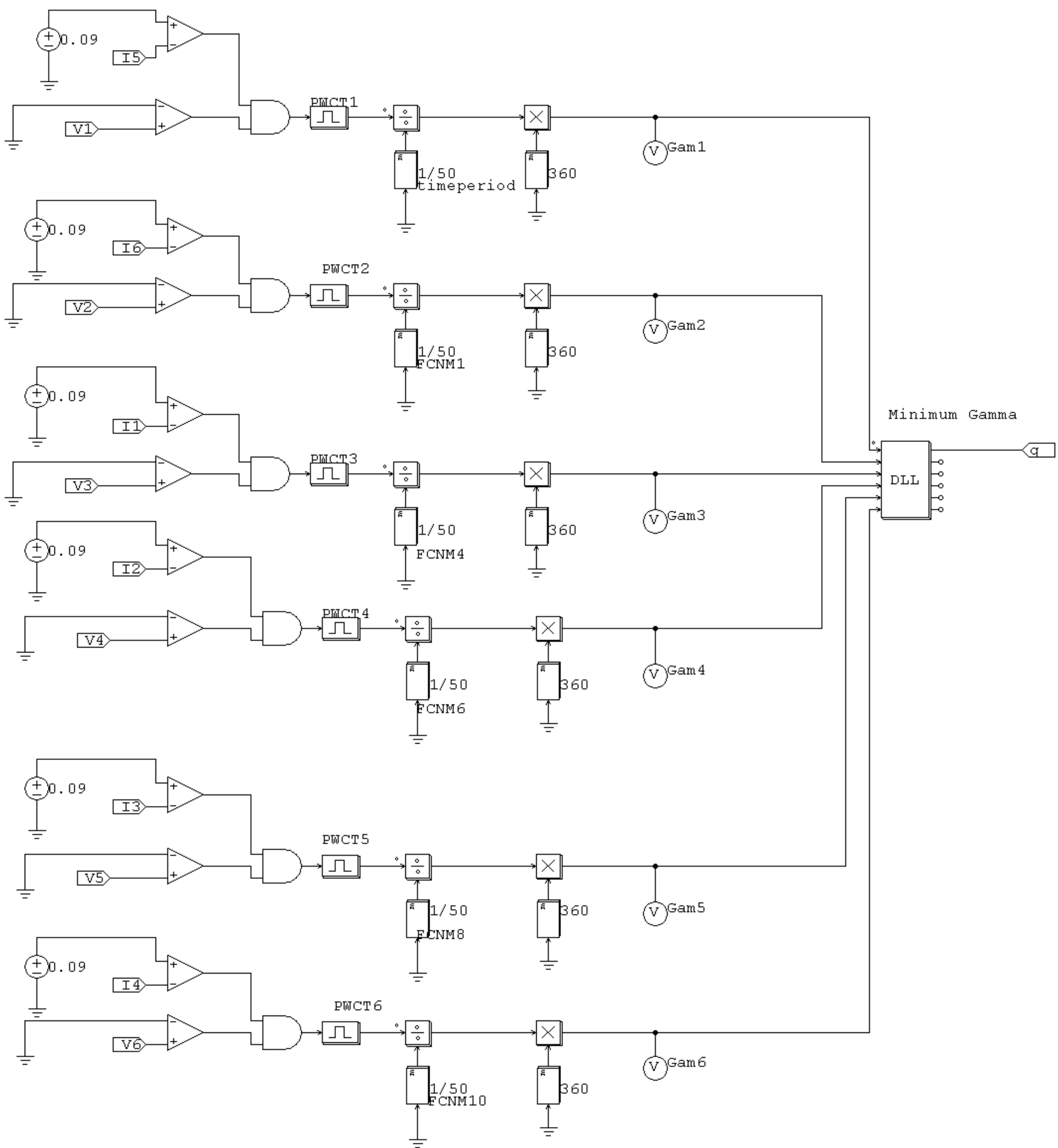


Figure 4.13: Circuit for gamma detection

Chapter 5

Simulation of EPC Scheme

This section explains the working of the equidistant pulse firing scheme with the help of a simulation. Although this firing scheme results in higher negative damping contribution to torsional oscillations and reduces power transfer during AC faults as compared to the individual phase control (IPC) scheme, this scheme has the inherent advantage of working satisfactorily with a weak AC system since it does not aggravate the non-characteristic harmonics. Thus, in most cases IPC scheme leads to harmonic instability since the firing of the thyristor valves is dependent on the supply voltage zero crossing feedback. Thus is eliminated in this case since the firing pulses produced by this scheme are equidistant and independent of the supply frequency.

For this EPC scheme, 440 V system is opted for and simulated in Simulation software package. Rectifier side supply is 440 V and inverter side supply is 415 V. Six pulse converter is used for rectifier as well as inverter topology. It is called converter because it can be used for rectification operation as well as inverter operation. The converter-1 is supplied with 440 V. The value of source inductance is 5 mH. Voltage across thyristor is sensed by voltage sensor and current flowing through thyristor is sensed by current sensor.

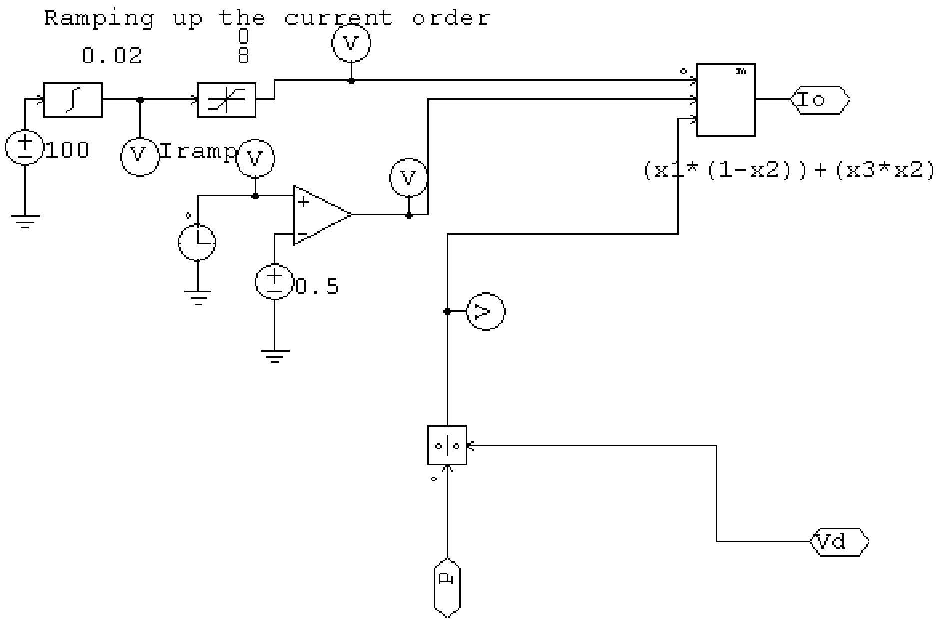


Figure 5.1: Power Control

5.1 Master control or power control

This block takes the average value of direct line voltage V_d and the power order as input. It divides the power order by the voltage value to get the current order. However, while starting the link the current order is ramped up to the value of 7 A first before the actual current order is used. This feature is implemented as shown above. The output of an integrator is fed via a limiter (with a maximum of 7 A) to the function block. The second input is the output of a comparator. This input becomes equal to 1 after 0.5s. The third input is the actual current order. The formula implemented is $(x_1 * (1 - x_2)) + (x_3 * x_2)$.Thus, during the first 0.5s, x_2 is 0, hence the output current order is equal to x_1, i.e. the current is ramped up to 7 A and held constant for 0.5s. After that, x_2 is 1, making the output current order equal to x_3, i.e. the actual current order.

5.2 CC,CIA and CEA control of Converter

The converter-1 (rectifier) maintains the current through the link using the following control system which changes the time period of the oscillator within a fixed range according to the error generated. The error is equal to the difference between the real current I_d and the current order I_o (taken from the master control block). The converter-1 maintains the Constant Ignition Angle (CIA) by keeping the $\alpha = 5^o$. For this, $t = -0.0183333$ is set which gives constant α. The positive voltage appearing across each thyristor before firing is used to charge the supply circuit providing the firing pulse energy to the thyristor. Therefore, firing cannot occur earlier than about 5^o.

The Constant Extinction Angle (CEA) control of the converter-2 (inverter) is meant for maintaining constant voltage and preventing commutation failure. This is achieved by maintaining the gamma value as required. Thus,the converter-2 (inverter) works within a fixed range of alpha values and maintains a constant voltage. Since the converter-2 (inverter) maintains a constant receiving end voltage, the current is maintained by the converter-1 (rectifier). In the figure-5.2, All three controls are shown together in converter-1 control because it should have all three characteristics for Bi-directional power flow. Initially, the voltage across the converter is positive and the pulses that are generated are equidistant by 60^o. Now in order to bring the converter in the inversion mode, the first pulse of the sequence must be shifted by 100^o instead of 60^o. This is achieved by the first circuit comprising of two AND gates and an OR gate. When the converter voltage is positive, and as long as the other two conditions are satisfied, the output of the OR gate is 1 (NOTE: if we only had the condition that inverter voltage should be positive, then even if the converter voltage became negative transiently, the logical circuit would fail). The output of the OR gate is ANDed with the outputs of the two comparators. This operation is 1 if the G_1 is zero and G_6 is one. Thus, during the interval between the G_6 gating pulse and G_1, the output of the logical circuit is one and hence during this interval the time

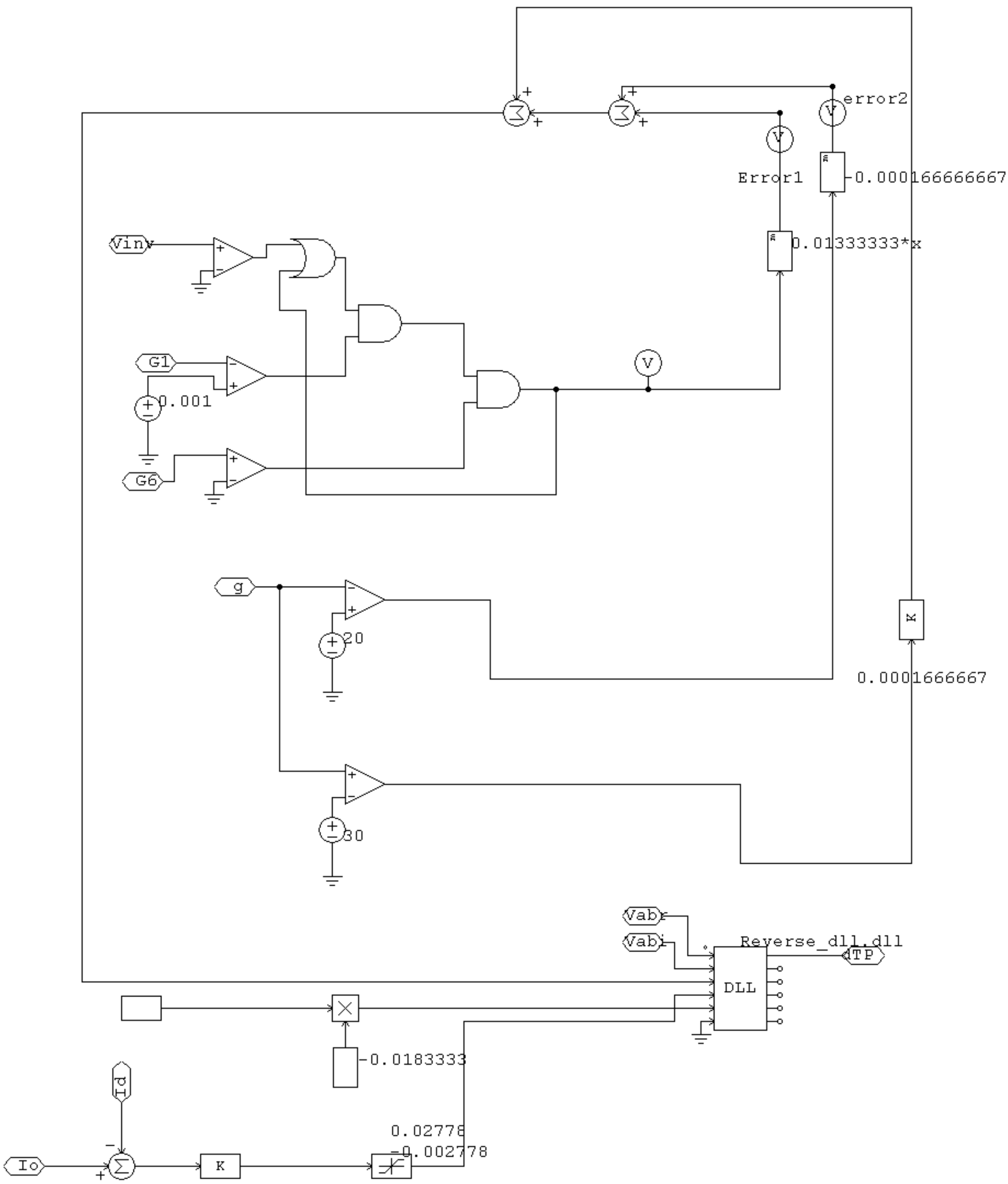


Figure 5.2: CC,CIA and CEA control of Converter-1

period is increased by the fraction 0.01333333s. This causes the requisite 100^o pulse width required between G_6 and G_1 of the next cycle of pulses.

During normal operation we need to maintain the value of gamma in order to prevent commutation failure and also to make sure that the equidistant firing pulses generated do not start triggering the valves in the rectification range. Thus the gamma value is maintained less than 30^o and greater than 20^o. If the gamma value falls below 20^o then the phase difference between the pulses is kept 59.5^o by reducing the time period by 0.000166666667s. Also when the gamma value becomes greater than 30^o, the time period is increased by the same amount. This maintains gamma and makes certain that the inverter works as specified. The various error signals for the various conditions are summed and we get a value for dTP which is the required change in time period of the oscillator (i.e. change in frequency) which would be fed to the PLL circuit.

```
#include <math.h>
__declspec(dllexport) void simuser (t, delt, in, out)
// Note that all the variables must be defined as "double
double t, delt;
double *in, *out;
{// Place your code here............begin
//  Define "sum" as "static" in order to retain its value
    double Vabr, Vabi, Vir;
    Vabr = in[0];
    Vabi = in[1];
    Vir  = Vabi-Vabr;
    if ( (Vir>35) && (Vir<50) )
    {
        out[0] = in[2];  // CEA control for rectifier
    }
    else if ( Vir>60 )
    {
    out[0] = in[3];    // CIA control of rectifier
    }
    else
    {
    out[0] = in[4];   // CC control of rectifier
    }
}
```

Figure 5.3: CC,CIA and CEA control of Converter-1

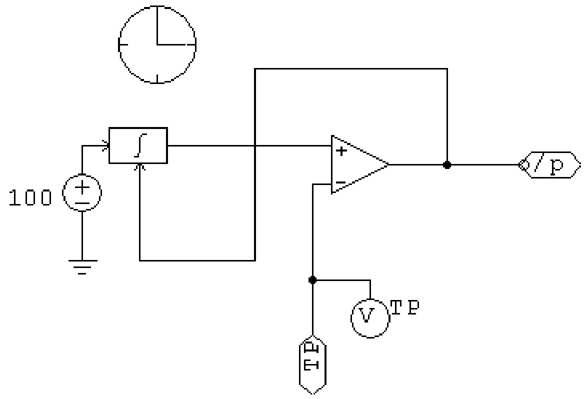


Figure 5.4: CC control of Converter-2

For converter-2 (inverter), same DLL code is used but only difference is in constant current characteristic because in power reversal mode, converter-2 has to be worked in rectifier mode. So there should be some margin between rectifier current order and inverter current order. It is 10 to 15% of rated current. It is shown as above.

5.3 Phase Locked Loop

The following figure tries to explain the basic operation of the PLL based EPC scheme that has been implemented: Herein an error signal is generated based on the deviation of the controlled variable, which might be either current in the case of the rectifier or

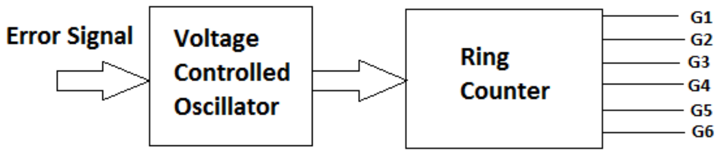


Figure 5.5: Phase Locked Loop

gamma value in the case of the inverter, from the reference value. This error signal is converted to a voltage signal and fed to a voltage controlled oscillator (VCO). Under normal conditions the VCO runs at a constant frequency which is six times the fundamental frequency (for a six pulse bridge). These pulses are supplied to a ring counter. For each pulse, the ring counter fires a different valve of the bridge in a cyclic manner. Thus all the gating pulses are equidistant under steady state conditions with a 60^o phase difference between them. This frequency increases or decreases based on the error signal and the VCO speeds up or slows down until it once again locks onto the correct value of alpha and the frequency becomes six times the fundamental yet again. The error, in terms of time period is used by the circuit shown below to generate the firing pulses. The change in time period is added to the default time period corresponding to 50 Hz, and the frequency so obtained is fed through a limiter which limits frequency between 10 and 100 Hz. The frequency signal is multiplied by 6 (since its a 6 pulse bridge converter) and once again converted to time period which is used by the VCO circuit. The VCO generates a train of clock pulses at 6 times the input frequency and these are fed to the ring counter block along with the time period. The ring counter generates one gating pulse for each clock pulse; hence 6 equidistant pulses are generated in a cyclic manner.

5.4 Voltage Controlled Oscillator

The integrator creates a ramp with a constant slope. This ramp keeps rising till its equal to a value proportional to the time period. At this point an output pulse is

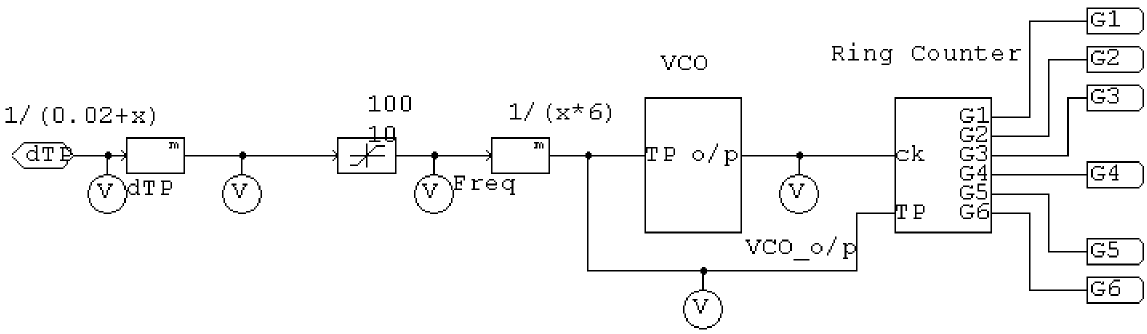


Figure 5.6: Circuit for generation of firing pulses

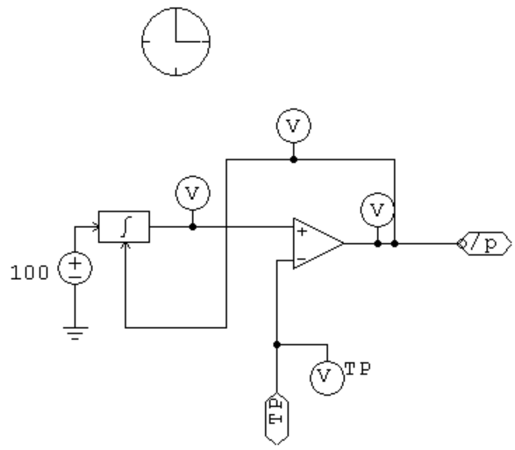


Figure 5.7: Voltage controlled oscillator

generated which is used to reset the ramp for the next interval. Therefore, a train of pulses is generated with intervals equal to the time period corresponding to the required frequency.

5.5 Ring Counter

The circuit connected to the left side of the counter is used to set the first flip flop to 1. After that, the binary value of 1 is shifted from one flip flop to another one after the other whenever a clock pulse is received. Accordingly, after each clock pulse a

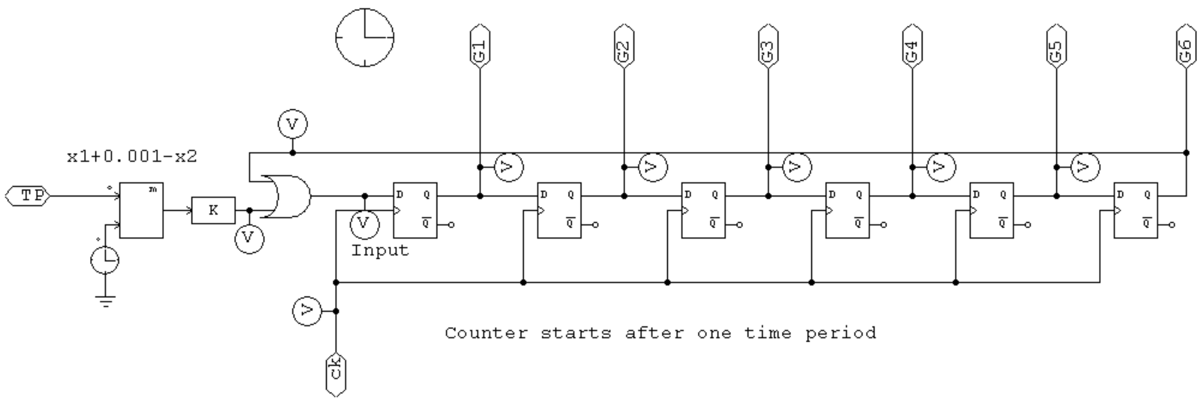


Figure 5.8: Ring Counter

different flip flop outputs 1; this leads to a set of equidistant clock pulses coming one after the other.

5.6 Full Circuit

As it can be seen in the figure, the HVDC system simulated consists of an AC system on each side. The AC system is modeled as a 3-phase source with source inductance of 5 mH. The value of the source inductance is high showing that it is not a strong AC system. The converters acting as rectifier and inverter supply a line with resistance equal to 20Ω/km (and total smoothing inductance of 0.46 H. The rectifier and inverter are controlled by current control (CC) and constant extinction angle (CEA) respectively. The rectifier controls the current through the system whereas the inverter maintains the receiving end voltage. The current order is set by the power control block depending on the rectifier side voltage and the power order. A 3-phase induction motor of 3 HP is connected to the inverter output. So induction motor should draw the power from inverter output not from source. For this, wattmeter is connected to the inverter output, source side and input to the induction motor.

Now,power is to be reversed means first power was flowing from converter-1 (rectifier) to converter-2 (inverter). Now it should be from converter-2 (rectifier) to

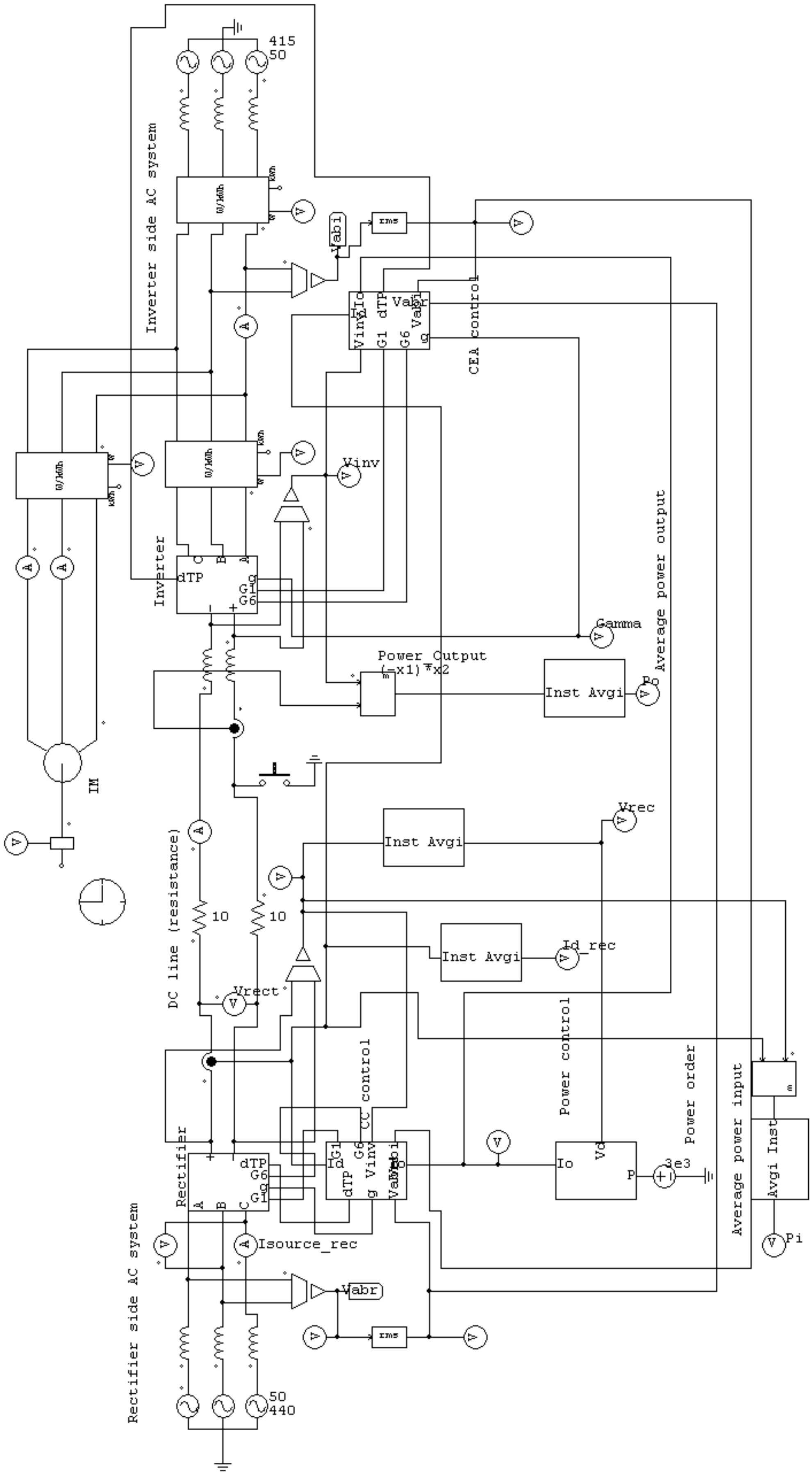


Figure 5.9: Full Circuit of EPC scheme

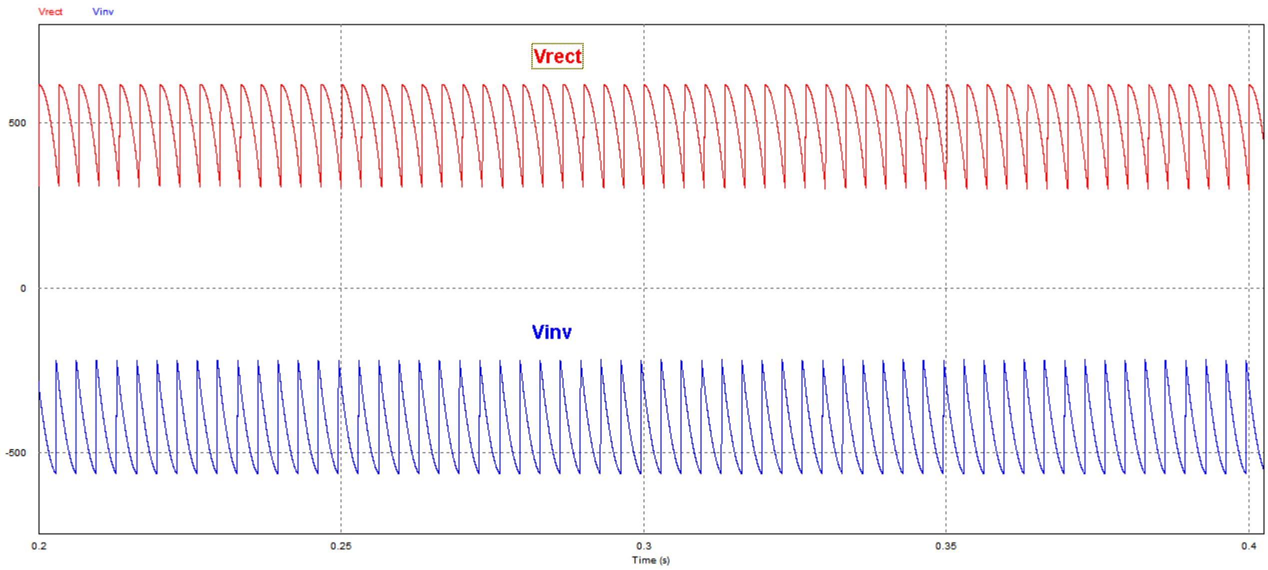


Figure 5.10: Waveform of rectifier and inverter voltage

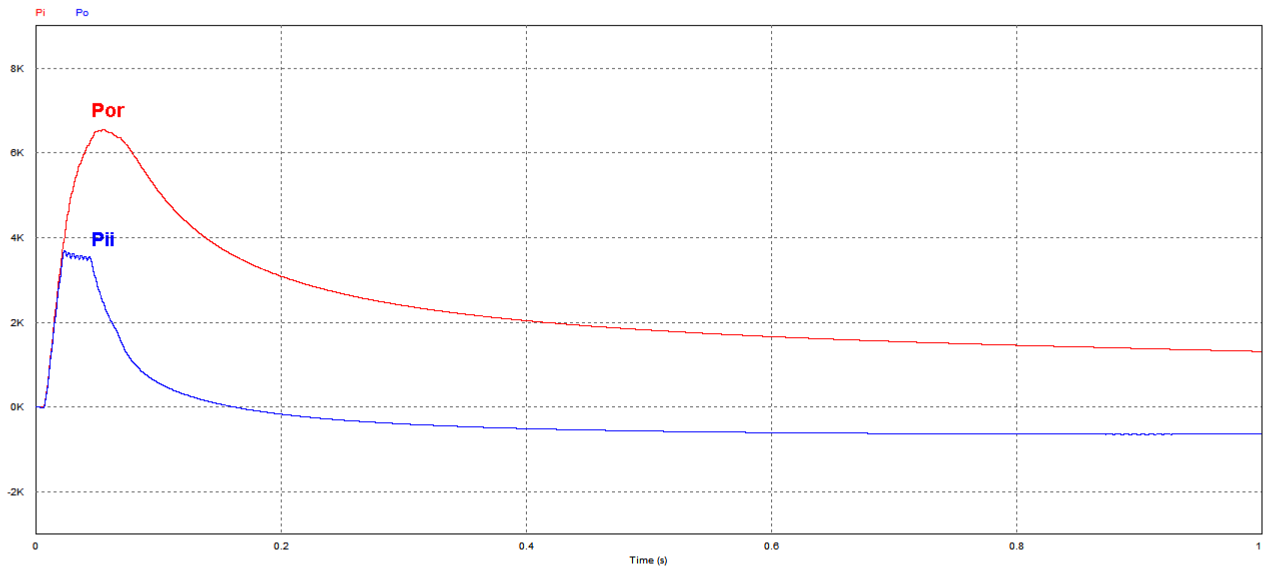


Figure 5.11: Power delivered by rectifier and inverter

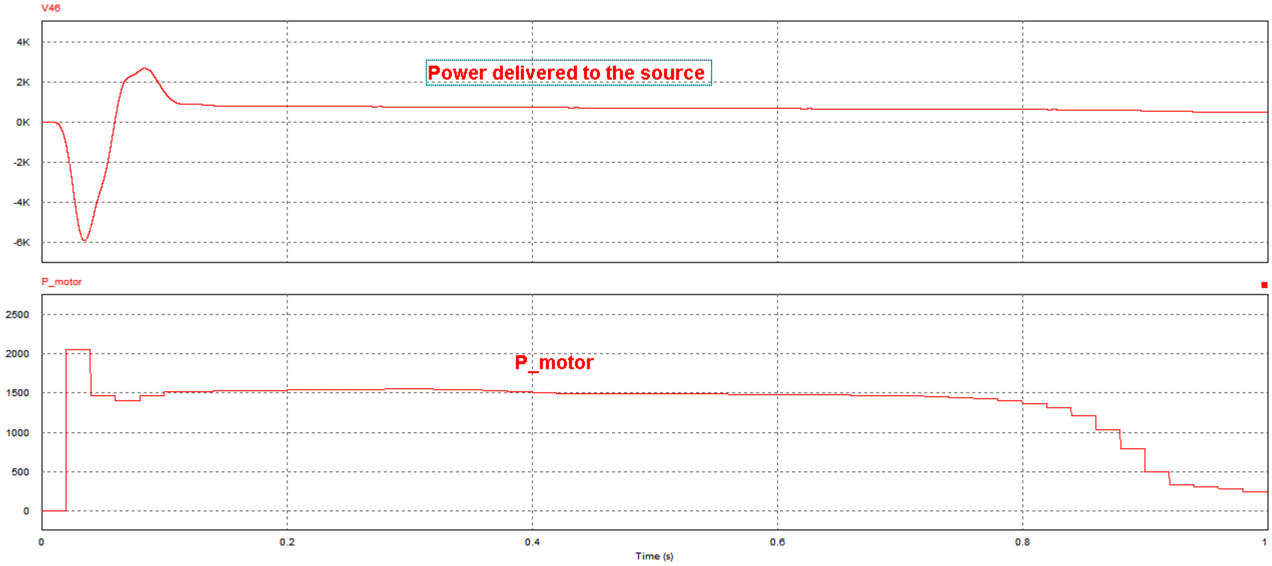


Figure 5.12: Waveform of power

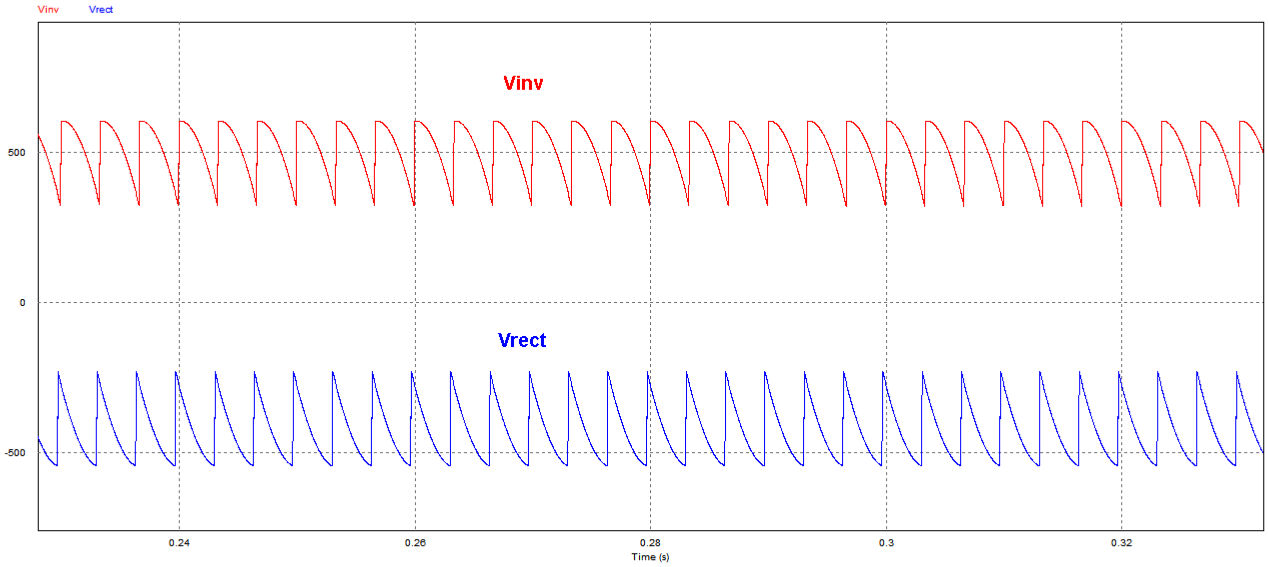


Figure 5.13: Waveform of rectifier and inverter voltage in Reverse power flow

converter-1 (inverter). For this, inverter should take over the CC and CIA characteristic of rectifier and similar way, rectifier should take over the CC and CEA characteristic of inverter. In this case, inverter current order margin should be more than the rectifier current order margin. Waveforms for rectifier and inverter is as follow. Inverter voltage has became positive and rectifier voltage become negative. When voltage and current both are positive, power flows from source to load and when voltage is negative and current is positive, power flows from load to source.

5.7 Simulation of HVDC link for 230V System

In this EPC scheme, 230V is opted for rectifier as well as inverter. Same controls are implemented here which are used in 440V system.The power transfer is reduced to 2KW from 5KW by changing the value of resistance and inductance of the line and system voltage.

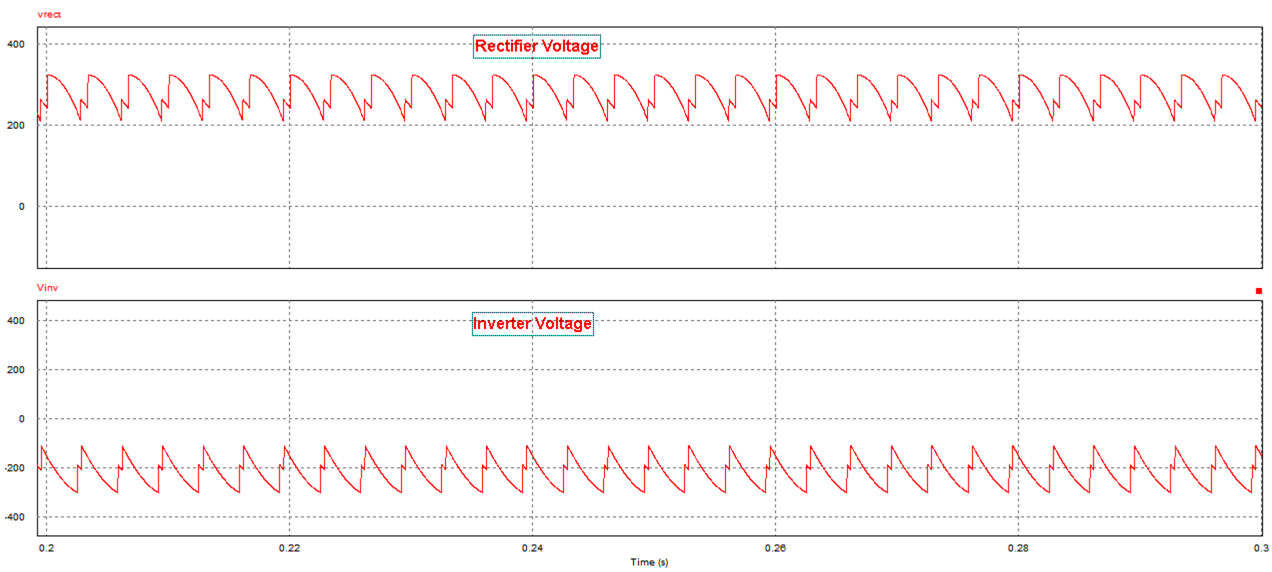


Figure 5.14: Waveform of rectifier and inverter voltage

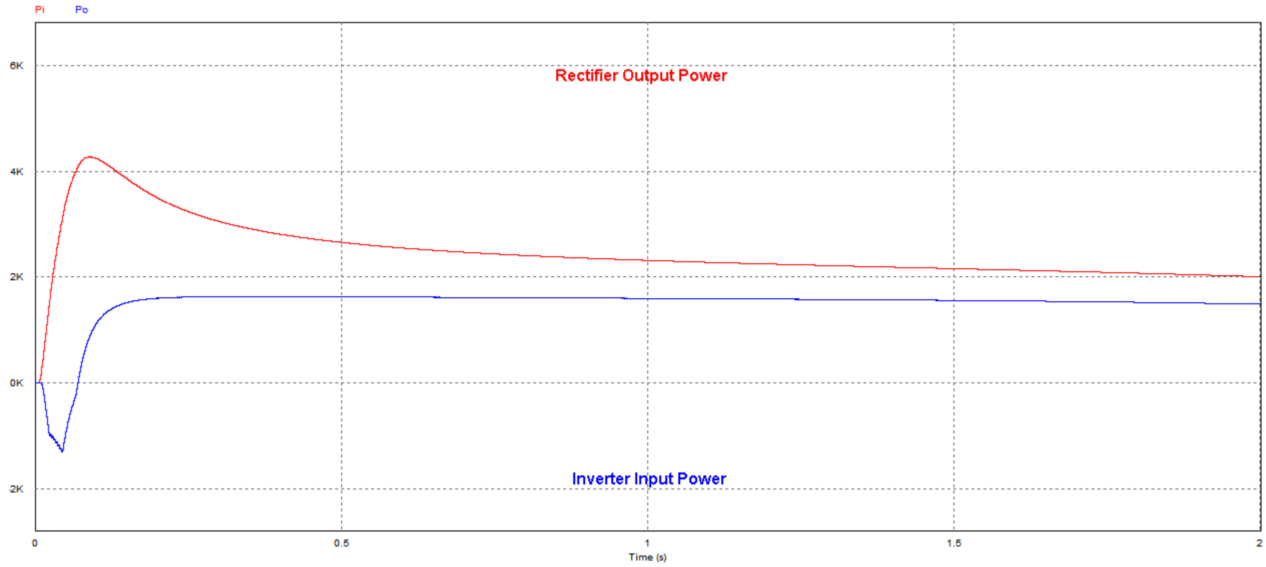


Figure 5.15: Waveform of rectifier and inverter power

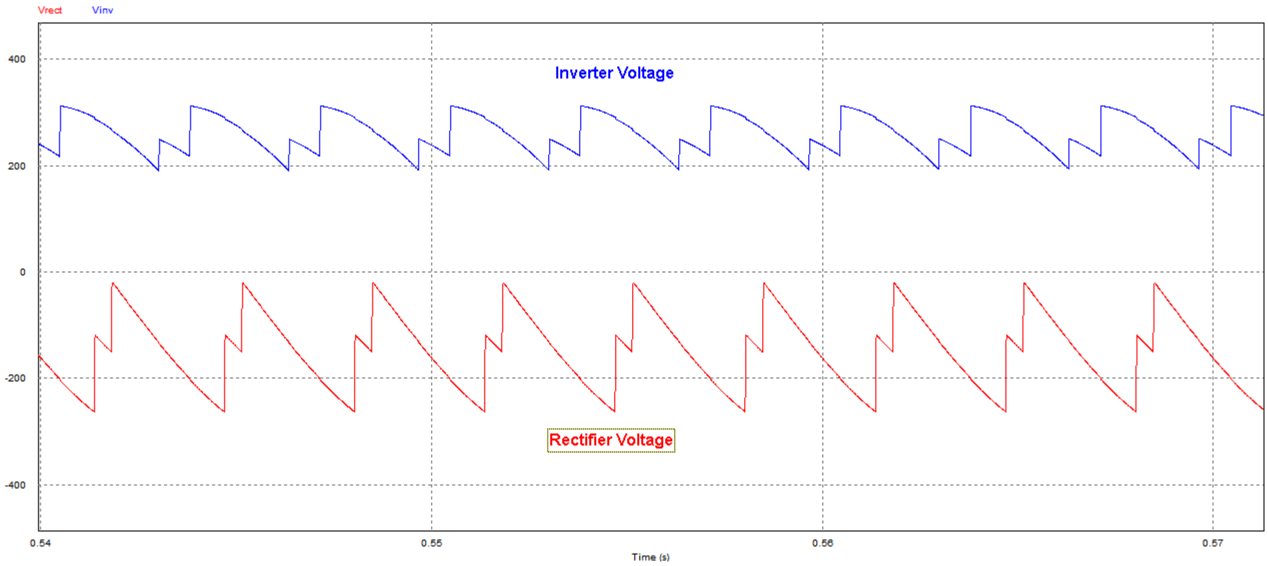


Figure 5.16: Waveform of rectifier and inverter voltage in inversion mode

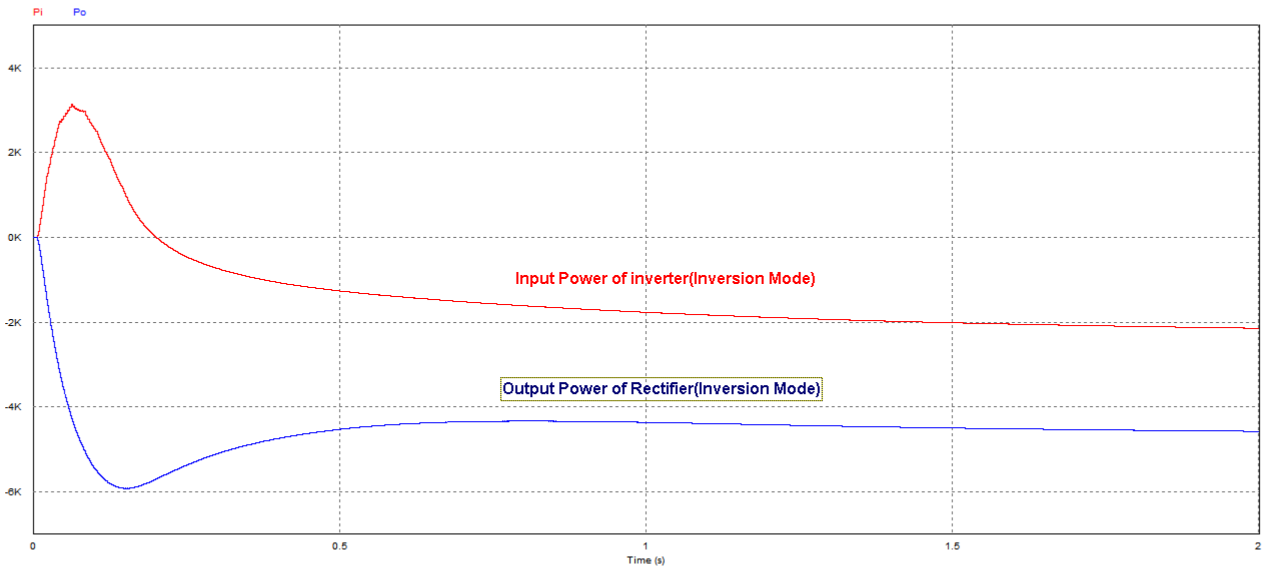


Figure 5.17: Waveform of rectifier and inverter power in inversion mode

Chapter 6

Hardware Model of Rectifier and Inverter

6.1 ARDUINO DUE

The ARDUINO DUE is a micro-controller board based on the Atmel SAM3X8E ARM Cortex-M3 CPU. It is the First ARDUINO board based on a 32-bit ARM core micro-controller. It has 54 digital input/output pins (of which 14 can be used as PWM outputs), 16 analog inputs, 4 UARTs (hardware serial ports),2 DAC (Digital to Analog), 84MHz crystal oscillator, a USB connection, a power jack, an ICSP header and a reset button. It contains everything needed for micro-controller, simply connect it to a computer with USB cable or power it with a AC to DC adapter or battery to get started. Operating voltage of ARDUINO is 3.3 V and voltage limit is 6-20 V. DC current per i/o pin is 300mA. Flash memory is 512 KB of which 8 KB used by bootloader. A program to generate current order in ARDUINO is as shown in fig-6.1. In this program, millis command is used to calculate the time in millisecond. Integrator time constant is 6 and input is 100 so output will be (100/6). Millis calculates time in millisecond but we need it in second so have to divide by 1000 so it will be 0.016. DC line Voltage is sensed by voltage divider and it is given to the analog pin A_o. AnalogRead command reads the value of analog pin, returning a range from 0 to 1023, that represents the voltage being passed into the pin. AnalogWrite command writes an analog value to a pin can be any value between 0 and 4096.

```
unsigned long start;
float x1,x2,x3,Io,power=3000,voltage;
void setup()
{
  Serial.begin(9600);
}
void loop()
{
  start=millis();
  x1=0.016*start;              //Integrator function
  if(start>=500)               //500 millisecond
  {
  x2=1;
  }
  else
  {
  x2=0;
  }
  voltage=analogRead(A1);
  x3=power/voltage;
  Io = x1*(1-x2)+(x3*x2);
  analogWrite(A2,Io);
}
```

Figure 6.1: Program for current order

6.2 Scaling of Voltage and Current Signal

Potential divider is used to sense DC voltage. This quantity is scaled down by potential divider using resistive network. One high value resistor (1.5KΩ) and one low value resistor (25Ω) is used. Voltage is sensed across the 25Ω resistor. For smoothing the output, 200 micro farad capacitance is used.

In case of AC quantity, one can not give directly it to micro-controller because

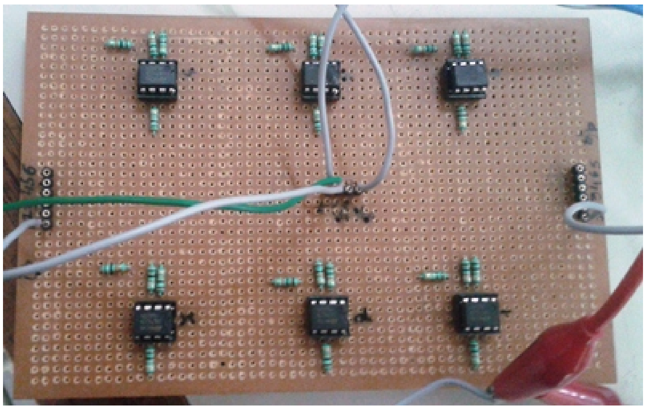


Figure 6.2: Setup of level shifter circuit

micro-controller accepts only DC signal. First, transformer will step down the voltage at 12V then by using potential divider, it is dropped at 3.3V. The negative side of the signal is shifted above the zero axis by using level shifter and one can get whole positive signal(+3.3V). A diagram of the level shifter is as shown in fig-6.2

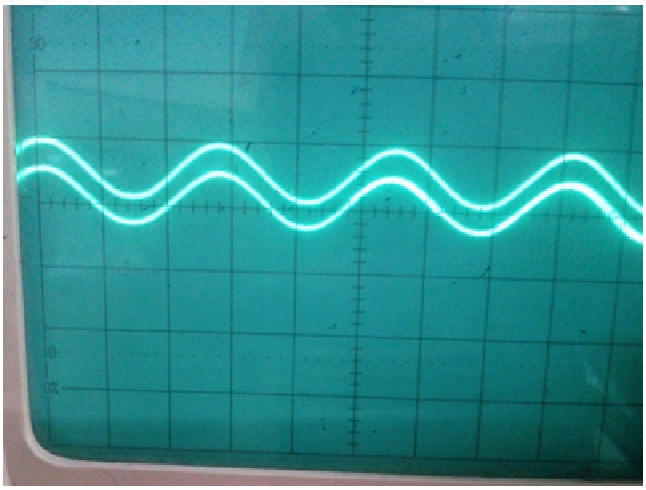


Figure 6.3: output of level shifter

6.3 Power Supply

Power supply is prepared for an optocoupler TLP250 IC. This IC is used to isolate power circuit from control circuit. This IC is driven at 12 V V_{cc} in this project. One 12-0-12 transformer is used. The output of the transformer is given to the diode bridge rectifier for conversion of AC into DC. This DC is filter by using two 100 micro farad capacitors.

6.4 Triggering Circuit of Thyristor

A thyristor can be triggered by the application of a positive gate voltage and positive gate current, supplied from a gate drive circuit. A trigger circuit used in this scheme is R-triggering circuit. In this circuit, R_s is the source resistance. Presence of R_2 is optional. However, if gate pulse is greater than maximum gate voltage, it helps to clip gate voltage not to exceed maximum gate voltage level. A single pulse or train of pulses are also used to trigger a thyristor. This design considerations(with DC values of gate voltage current) are also valid for a pulse width up to 100 microseconds.(All resistance value are in ohm).

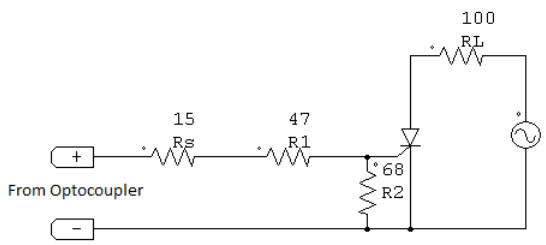


Figure 6.4: Triggering circuit of thyristor

6.5 Results of Single Phase Controlled Rectifier

The waveform of single phase controlled rectifier is shown in fig-6.5. It is the full rectification. In one cycle, there are two half wave. For smoothing the output , 1000 microfarad capacitor is used

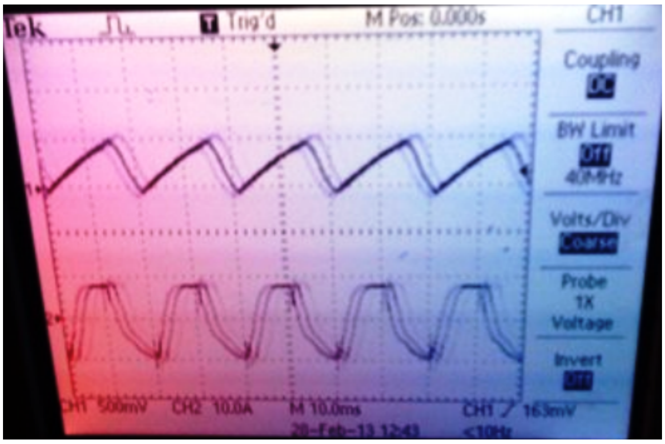


Figure 6.5: Output voltage waveform of single phase controlled rectifier

6.6 Three Phase Controlled Rectifier

After getting successful results of single phase controlled rectifier, three phase controlled rectifier is implemented for HVDC system. Power circuit of controlled rectifier for 3-phase system is shown in fig-6.6

6.6.1 Thyristor Gate Pulses

It is necessary to check the zero crossing of AC voltage for triggering the thyristor. zero-crossing detector is prepared by using operational amplifier(LM741). The circuit of zero-crossing detector is as shown in fig-6.7

The output of zero-crossing detector is square wave which is given to the microcontroller. Negative pulse of square wave is removed by using diode. A programming

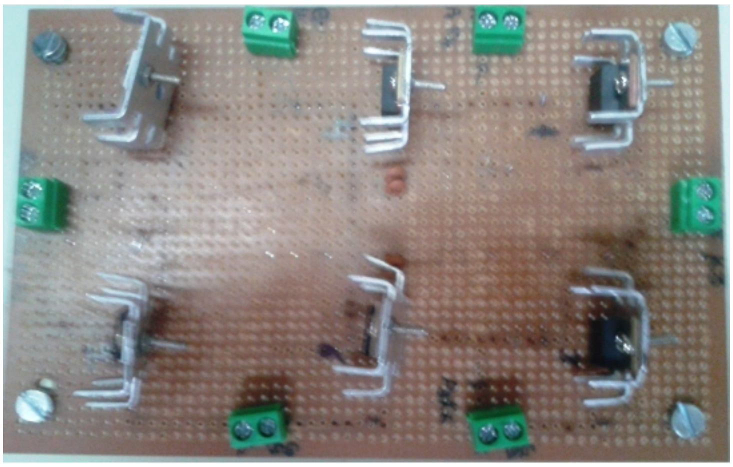


Figure 6.6: Six pulse bridge controlled rectifier

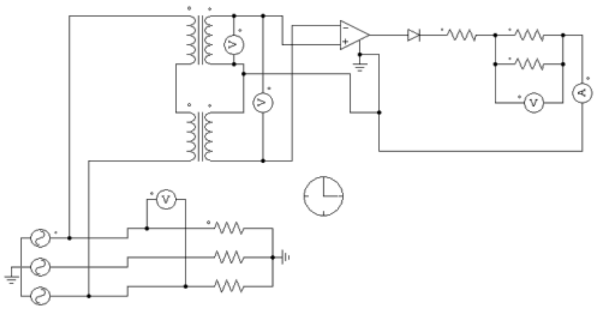


Figure 6.7: Test circuit of zero crossing detector

of whole control circuitry is done in ARDUINO DUE Micro-controller. The square pulse of zero-crossing detector is given to the PWM pin of ARDUINO DUE controller. ARDUINO will use pin no-2 as external interrupt and at the rising edge of the pulse, it will generate one interrupt. After doing mathematical calculation, ARDUINO will generate six gate pulses which are 60^o apart with each other. Six gate pulses which are synchronized with the output of the zero-crossing detector are given to the six triggering circuits of controlled rectifier.

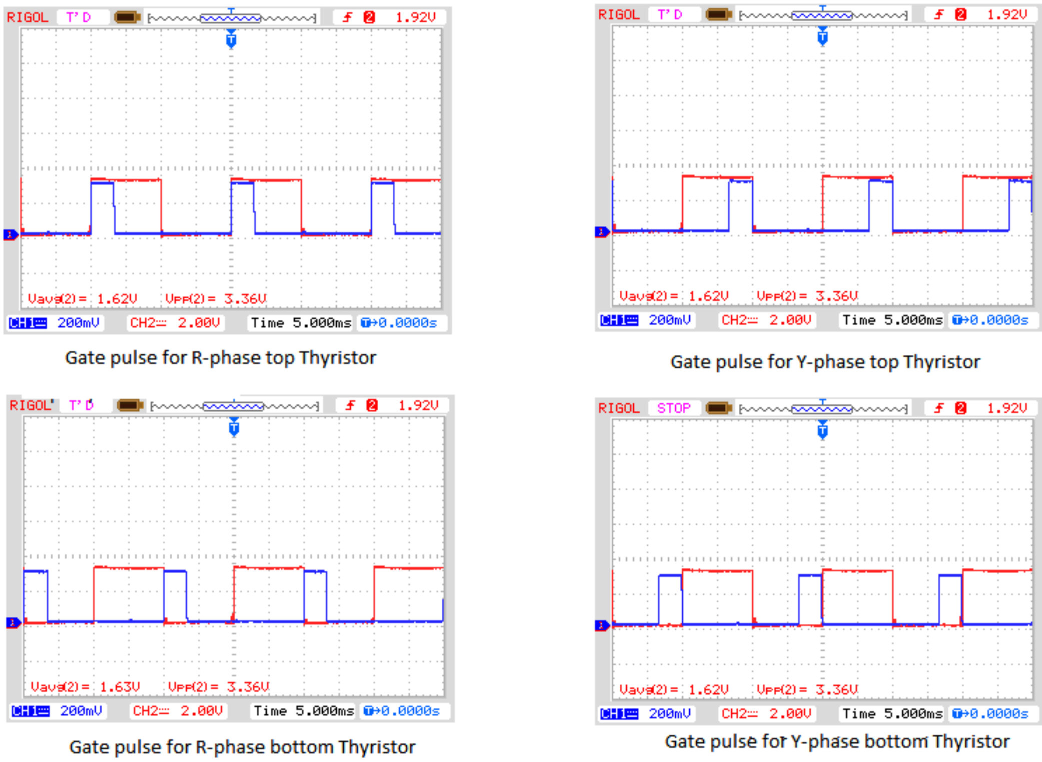


Figure 6.8: Gate pulse to Thyristor-1,4,3 and 6

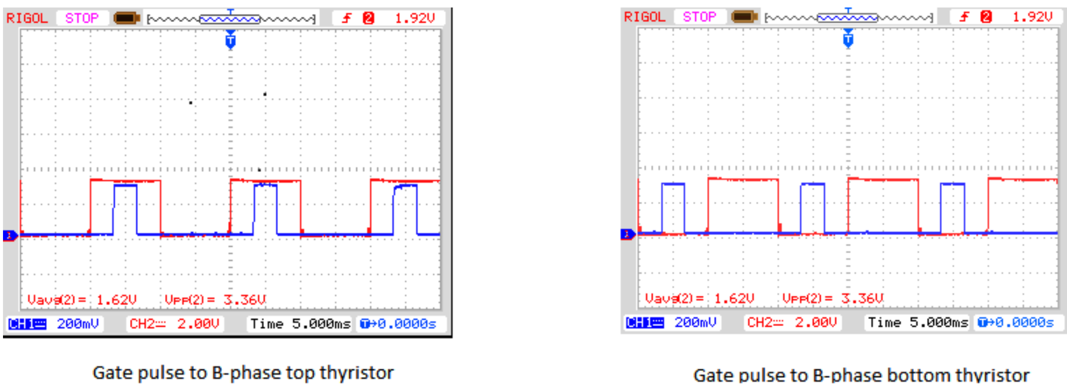


Figure 6.9: Gate pulse to Thyristor-2 and 5

6.7 Test Setup of Controlled Rectifier

The entire test setup is shown in fig-6.8 Six pulses are given to the six TLP250 which is an optocoupler IC. It will provide isolation between control circuit and power circuit. For driven the TLP250, 12 V DC suppy is given to the pin-8 and pin-5 from power supply. The output of optocoupler is given to the R-triggering circuit. This triggering circuit will generate sufficient latching current to drive the thyristor because it is a current driven device. Requirement of latching current for thyristor (25TTS12) is 200 mA to turn on it. so, this much current is injected to gate circuit of thyristor. Continuous current capacity of TLP250 is 50 mA. However, each TLP250 is used for 17 percent duty cycle. so, current rating of TLP250 can be marginally increased.

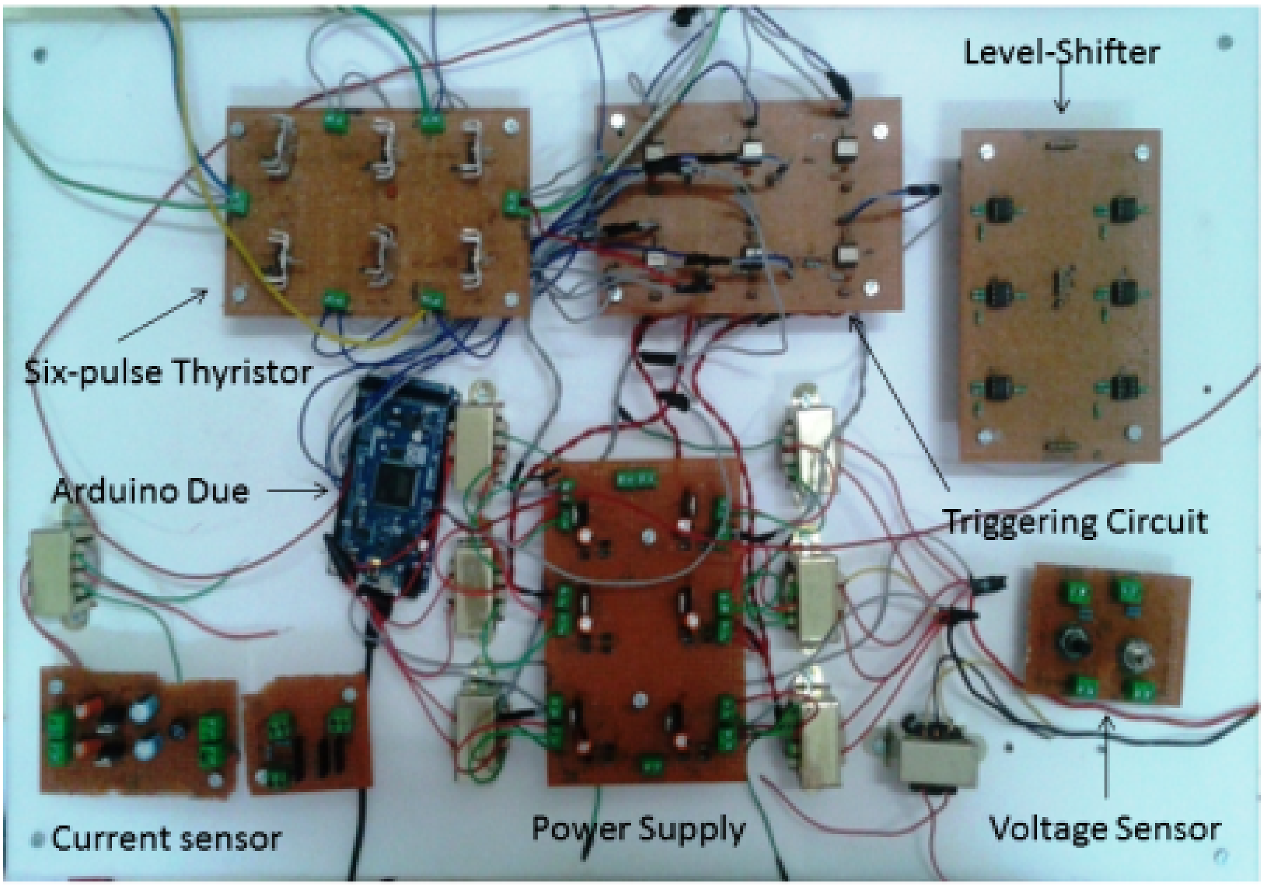


Figure 6.10: Test setup of controlled rectifier

6.8 Line Commutated Inverter

DC output of controlled rectifier is supplied to the line commutated inverter. Same power circuit is used for inverter but only difference of firing angle. Rectifier is operated as an inverter if firing angle is above 90^o. In case of inverter, voltage across each thyristor and current through each thyristor is sensed by voltage sensor and current sensor respectively. Gamma(γ) of inverter is determined from voltage and current of thyristor. Generally, gamma is maintained at constant angle due to commutation problem. There is also problem of reactive power if gamma is not maintained at constant value. Same triggering circuit is also used for inverter. Firing angle of thyristor is controlled by ARDUINO DUE micro-controller. Line commutated inverter has same principle as Induction generator. It supplies active power to the source and consume reactive power from source. In inverter operation, output voltage of inverter is negative and current is positive so power is negative that is why active power flows from load to source.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

HVDC consists of rectifier and line commutated inverter. Behavior and control of converters plays a very major role in entire HVDC system. The simulation approach for the IPC scheme using CC Controller, CIA Controller and CEA Controller shows desired results with required parameters. After having these outcomes, the same system has been simulated in EPC mode. The arrangement yields much better output and for the same, system parameters have also been well defined. Prototype combined model of rectifier and inverter have been prepared and tested.

7.2 Future Work

It needs to be checked in real practice that after defining all the crucial things, does the system behave in a correct manner or not? In the subsequent stage of the work, following aspects to be covered with micro-controller coding which has been already prepared. Following points proposed the future work to be carried out in this project to improve the performance of HVDC system.

1. Integration of individual models of rectifier and inverter.

2. Three phase load is to be driven by this prototype hardware model to validate the results.
3. Performance of HVDC link during fault occurrence.
4. Performance of HVDC link after implementing filters to mitigate harmonics at AC side.

Appendix A

Program to generate six pulses from Arduino due

EPC control scheme is programmed in arduino. For generating the current reference, voltage is sensed by voltage sensor. It is given to the Analog pin A0. Once power order is fixed, Power is divided by voltage to get the current reference. When line is stop, there is no voltage across the line so current reference is generated by using integrator and limitor for 2 seconds. Current is sensed by current sensor and it is given to the analog pin A1. An error is generated by reference current and measured current. This error is reduced by proportional controller and it is compared with the time according to 50 Hz system. This time is converted into frequency and then it is multiplied by six to generate six pulses. Then, Timer is started and this time is compared with time generated by six times frequency. As this condition become true, Interrupt is generated on pin-2 and six pulses are generated on six digital pins.

```
volatile boolean l;
volatile long f,t;
//TC1 ch 0
void TC3_Handler()
{
 TC_GetStatus(TC1, 0);
}
void myfunction(){
  c=1;
}
int pin2=2,pin3=3,pin4=4,pin5=5,pin6=6,pin7=7;
long X,Z,Time;
float x2,Io,power=2000.0,voltage=277.0,elapse,VCO,F,Id,x4;
double error,Fo,dTP,TP,Kp,b,x1,x3;
void setup(){//
  Serial.begin(115200);
  startTimer(TC1, 0, TC3_IRQn, 4); //TC1 channel 0, the IRQ for that channel and the desired frequency
  pinMode(pin2, OUTPUT);
  pinMode(pin3, OUTPUT);
  pinMode(pin4, OUTPUT);
  pinMode(pin5, OUTPUT);
  pinMode(pin6, OUTPUT);
  pinMode(pin7, OUTPUT);
  c=0;
    }
```

Figure A.1: Part-1

```
void startTimer(Tc *tc, uint32_t channel, IRQn_Type irq, uint32_t frequency) {
    pmc_set_writeprotect(false);
    pmc_enable_periph_clk((uint32_t)irq);
    TC_Configure(tc, channel, TC_CMR_WAVE | TC_CMR_WAVSEL_UP_RC | TC_CMR_TCCLKS_TIMER_CLOCK4);
    uint32_t rc = VARIANT_MCK/2/frequency; //128 because we selected TIMER_CLOCK4 above
    TC_SetRA(tc, channel, rc/2); //50% high, 50% low it can be used for PWM operation
    TC_SetRC(tc, channel, rc);  // setting match value to trigger the in this program it depends on frequency
    TC_Start(tc, channel);
    tc->TC_CHANNEL[channel].TC_IER=TC_IER_CPCS;
    tc->TC_CHANNEL[channel].TC_IDR=~TC_IER_CPCS;
    NVIC_EnableIRQ(irq);
}
void stopTimer(Tc *tc, uint32_t channel, IRQn_Type irq, uint32_t frequency) {
    pmc_set_writeprotect(false);
    pmc_enable_periph_clk((uint32_t)irq);
    TC_Configure(tc, channel, TC_CMR_WAVE | TC_CMR_WAVSEL_UP_RC | TC_CMR_TCCLKS_TIMER_CLOCK5);
    uint32_t rc = VARIANT_MCK/2/frequency; //128 because we selected TIMER_CLOCK4 above
    TC_SetRA(tc, channel, rc/2); //50% high, 50% low it can be used for PWM operation
    TC_SetRC(tc, channel, rc);  // setting match value to trigger the in this program it depends on frequency
    TC_Stop(tc, channel);
    tc->TC_CHANNEL[channel].TC_IER=TC_IER_CPCS;
    tc->TC_CHANNEL[channel].TC_IDR=~TC_IER_CPCS;
    NVIC_EnableIRQ(irq);
}
void loop(){
 Time =micros();
 x4=10.0*(Time/1000000.0);
 x1=constrain(x4,0,5);
```

Figure A.2: Part-2

```
if(Time>=1000000)
 { x2=1;
 } else
 { x2=0;
 }
 //voltage=map(analogRead(A0),0,4096,0,275);
 x3=power/voltage;
 Io= x1*(1-x2) + (x3*x2);
 //Id=map(analogRead(A1),0,4096,0,7);
 float Id=7.0;
 error=Io-Id;
 Kp=0.00001*error;
 b=constrain(Kp,-0.002773,0.02773);
 F=1.0/(0.02+b);
 Fo=constrain(F,10.0,100.0);
 dTP=1.0/(6*Fo) ;
 startTimer(TC1, 0, TC3_IRQn, 4);
 bailOut:
 t=REG_TC1_CV0;
 double Y = (t/84000000.0);
if(Y<=dTP){
goto bailOut; }
attachInterrupt(pin2, myfunction , FALLING);
```

Figure A.3: Part-3

```
if(c==1){
digitalWrite(pin3,HIGH);
delayMicroseconds(3300);
 digitalWrite(pin3,LOW);
 digitalWrite(pin4,HIGH);
delayMicroseconds(3300);
digitalWrite(pin4,LOW);
  digitalWrite(pin5,HIGH);
delayMicroseconds(3300);
digitalWrite(pin5,LOW);
digitalWrite(pin6,HIGH);
delayMicroseconds(3300);
digitalWrite(pin6,LOW);
 digitalWrite(pin7,HIGH);
delayMicroseconds(3300);
digitalWrite(pin7,LOW);
 digitalWrite(pin8,HIGH);
delayMicroseconds(3300);
digitalWrite(pin8,LOW);
  stopTimer(TC1, 0, TC3_IRQn, 4);
  startTimer(TC1, 0, TC3_IRQn, 4);
  c=0; }
detachInterrupt(pin2);
}
```

Figure A.4: Part-4

Appendix B

Components used in Project

- Arduino due
- SCR 25TTS12
- Optocoupler TLP250
- Voltage Regulator IC 7812 and 7912
- Diode-D1N4007
- Isolation Transformer (18-0-18)
- Current sensor LA 25-NP

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