Major Project Report
on

"Power Analysis of I/O Cells"

Submitted as a Partial Fulfillment for Semester III-IV

Master of Technology
in
ELECTRONICS & COMMUNICATION ENGG.
(VLSI Design)

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CERTIFICATE

This is to certify that the M. Tech Dissertation Report entitle **"POWER ANALYSIS OF I/O CELLS"** submitted by **Divyesh Vora (Roll no. 05MEC018)** towards the partial fulfillment of the requirements for the Sem III-IV in **Master of Technology (Electronics and Communication)** in the Field of **VLSI Design**, **Nirma University of Science and Technology, Ahmedabad** at **S.T.Microelectronics, Noida** is the record of the work carried out under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this Dissertation-project work to the best of our knowledge have not been submitted to any other University or Institute for award of any degree or diploma.

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ABSTRACT

Two bottle-necks for today's IC designers are speed and power. Moreover, there is trade of between the two. In today's world of mobile devices low power is one of the major requirements. In this thesis are carried out, some of the power analysis on I/Os, which are one of the major components responsible for the power consumption. Entire power characterization is divided into to parts, static and dynamic power.

Leakage power or static power is the power dissipated by the cell when it is not switching, that is, when it is inactive or static. The largest percentage of static power results from source-to-drain sub threshold leakage. This leakage is caused by reduced threshold voltages that prevent the cell from completely turning off. Static power is also dissipated when current leaks between the diffusion layers and the substrate.

Internal power is any power dissipated within the boundary of a cell. During switching, a circuit dissipates internal power by the charging or discharging of any existing capacitances internal to the cell. The definition of internal power includes power dissipated by a momentary short circuit between the P and N transistors of a cell, called short circuit power. For circuits with fast transition times, short circuit power can be small. However, for circuits with slow transition times, short circuit power can account for 30 percent of the total power dissipated by the gate. Short circuit power is also affected by the dimensions of the transistors and the load capacitance at the gates output.

In this thesis work, different component of currents responsible for leakage and internal power are analyzed for different temperature, voltage, slope and load conditions. Also, the analysis of different I/O cells for Leakage Power and Internal Energy are carried out for different parametric variations.

COMPANY PROFILE

Company Name	**STMicroelectronics Pvt. Ltd.**
Address	Plot No.1, Knowledge Park-III, Institutional Area, Greater Noida-201301. Uttar Pradesh (INDIA)
Contact Number	0120-4003200, 4006300,3916000
Website	http://www.st.com
Branches (India)	Greater Noida, Bangalore
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Head Office (Worldwide)	Geneva, Switzerland
CEO	Mr.Carlo Bozotti
Site Director	Mr.Vivek Sharma

ST Microelectronics is a global independent semiconductor company and is a leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications. ST is one of the world's largest semiconductor companies. In 2004, ST's net revenues were US$8,760 million and net earnings were US$601 million.

ST is the world's leading supplier of application-specific analog ICs overall with number one rankings in various segments within this field. ST is also the leader in MPEG-2 decoder ICs. Additionally, ST is ranked at number two for discrete products, and in the memory market, ST is ranked third in NOR Flash ICs. In application segments overall: ST is number one for ICs in set-top boxes; at number two in smart cards, at number three in automotive; and at number four in wireless.

Origin

The ST group was formed in June 1987 as a result of the merger between SGS Microelectronics of Italy and Thomson Semiconductors of France. In May 1998, the company changed its name from SGS-THOMSON Microelectronics to ST Microelectronics.

The Company has significantly broadened and upgraded its range of products and technologies and has strengthened its manufacturing and distribution capabilities in Europe, North America, and Asia Pacific region. This capacity expansion is an ongoing process with the upgrading of existing facilities and the creation of new 8-inch, sub-micron fabs around the world. ST currently has five 8-inch fabs in operation in: Rousset (France); Agrate Brianza, R2 (Italy); Crolles (France); Phoenix (Arizona); Catania (Italy); and Singapore. Furthermore, a new 12inch manufacturing facility is currently under construction in Catania and the company is now ramping up production from a 12-inch pilot line called Crolles2 in partnership with Philips and Freescale Semiconductor. The Crolles operation is also host to the joint development program between the three companies to develop leading-edge CMOS process technology down to the 32nm node, in conjunction with TSMC for process alignment.

ST Noida Evolution

1987...	Liaison office set up in Delhi
1989...	Decision to start design center, 40 engineers recruited and sent to Europe and Singapore for training
1992...	Start of design operation in Delhi in semi custom and MIS Development centre
1993...	Expansion with start of Central R&D Library Development and System Software Application Lab
1995...	Move to own premises at Noida, expansion to about 170 engineers
1997...	Foundation of new building
1998...	Noida becomes part of Region 5 with headquarter in Geneva

1999...	2nd building becomes operational. 450 engineers
2000…	Site is ISO 9001 certified, 670 engineers
2004…	Third Design center facility in Noida, over 1500 employees
2005…	Further expansion to over 1700 engineers
2006…	Gtr. Noida new Design Building started to build

Market Position

ST is one of the world's largest semiconductor companies, with net revenues of US$8.88 billion in 2005 and market leadership that is spread across many fields. For example, according to the latest industry data, ST is the world's fifth largest semiconductor company and has leading positions in sales of Analog Products, Application Specific Integrated Circuits ("ASICs") and Application Specific Standard Products ("ASSPs"). ST is also number one in camera modules, number two in discrete and analog, and number three in, NOR Flash, as well as in the application segments of Automotive, Industrial, and Wireless. ST is also a leading supplier of semiconductors for set-top boxes, smart cards, and power management devices. Furthermore, ST was the 3rd biggest semiconductor supplier in China in 2005.

Computer systems, multimedia products, telephone networks, consumer goods, industrial control systems, automobiles and medical equipment can all be found with ST products inside. Applications can even be found in outer space.

Work Environment

FTM

Role: To provide quality Library Solutions and service to divisions in the company's drive in time to market, IP Reuse and Super Integration.

CIO (CMOS I/Os)

Role: Design and Development of compatible CMOS I/Os library for chip solutions.

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CHAPTER:1 FUNDAMENTALS OF I/Os

1.1. What are I/O's?

I/O is the specially designed element, which interface to core signal to off chip environment.

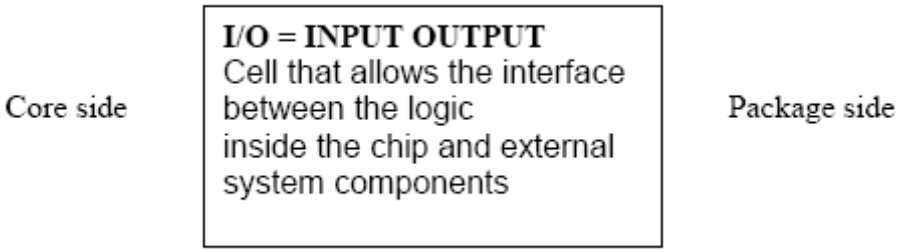


Figure 1: Block Diagram of Chip

1.2. Why do I/O's need special attention? Why are they important?

Any input signal which comes from off chip device has to be checked by the I/O for any discrepancy in its behavior other than the defined for the core and if it finds any characteristic of the signal which can damage the core, it either modifies the signal or simply rejects it. It also checks the signal going from core to the outside world. So I/Os are responsible for proper functioning of the entire chip. Thus, however efficient the core design may be; it is the I/Os, which determine the efficiency of the chip.

It is necessary for the designer to analyze the designed I/O under the practical conditions to verify the deriving strength of the chip, delay in signal, power etc as they all are heavily dependent on the I/O irrespective of whether the core is compliant with the specifications or not. Because, even if there is a minor difference in the performance of the I/O; than the desired one can damage the whole circuit or even can cause problems to the off chip circuit. It is the responsibility of the I/O to limit the outgoing signaling in all respect like amplitude, frequency, delay etc, under the specified one, for proper functioning.

1.3. Types of I/Os & Specific Functions

3 different types of an I/O

- Input
- Output
- Bi-directional

Specific functions:

- Pull-up, pull-down
- Hysteresis
- Analog
- Supplies

1.3.1. Input

These types of I/Os, receive signal from off the chip circuit and feed the core. But before feeding the core, it brings the signal into the operating limit of the core so as to make sure that chip works proper.

Input buffers are available with two possible drives towards the core.

- Normal drive, which is equivalent to an X4 drive in the standard digital library. These cells are characterized with internal loads up to 80 standard loads i.e. 0.72pF.
- High drive which is equivalent to an X16 drive in the standard digital library. They are characterized with loads up to 316 standard loads i.e.2.84pF

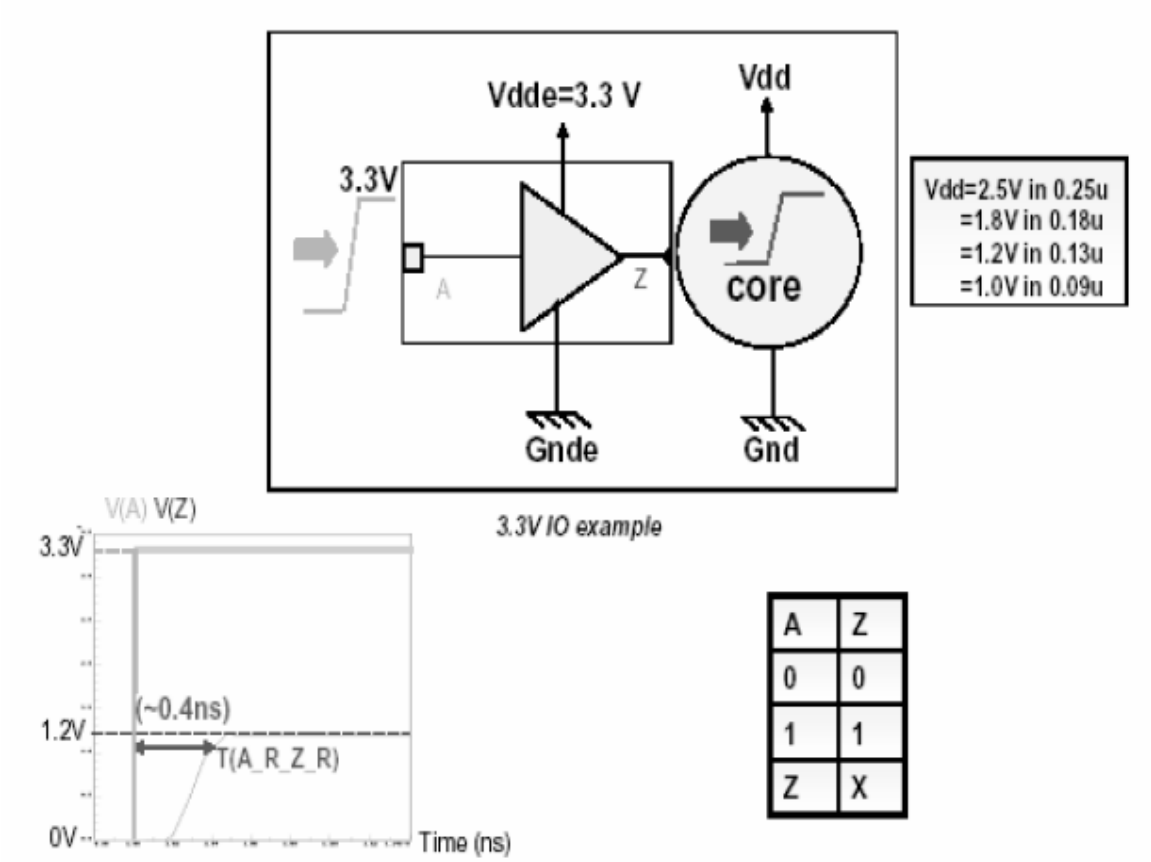


Figure 2: Block diagram of Input Section

1.3.2. Output

The IO amplifies and adapts the signal from the core to the outside load. These buffers are used to drive large capacitive loads which arise from long interconnect lines such as clock distribution networks, high capacitance fan out and high off chip loads .The drive capability of such a buffer should be such as to achieve the requisite rise and fall times into a given capacitive load.

Normally the drive capability of I/O buffers is as high as 8 mA. By driving Capability, it means that the output buffer can source or sink the specified amount of current in the worst case.

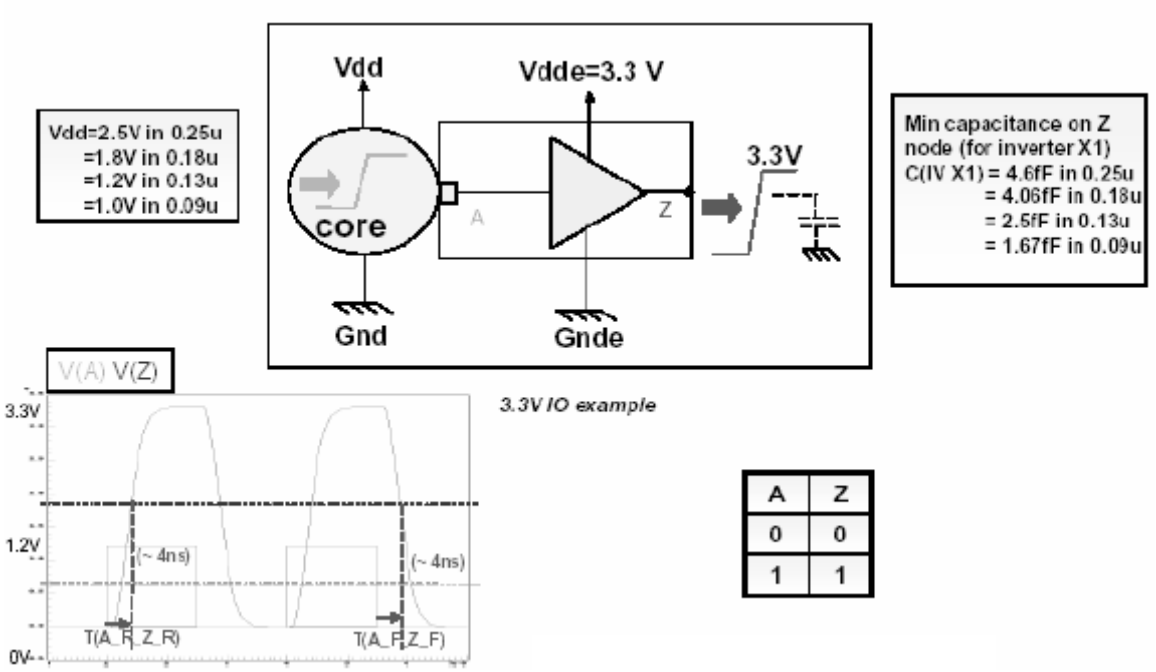
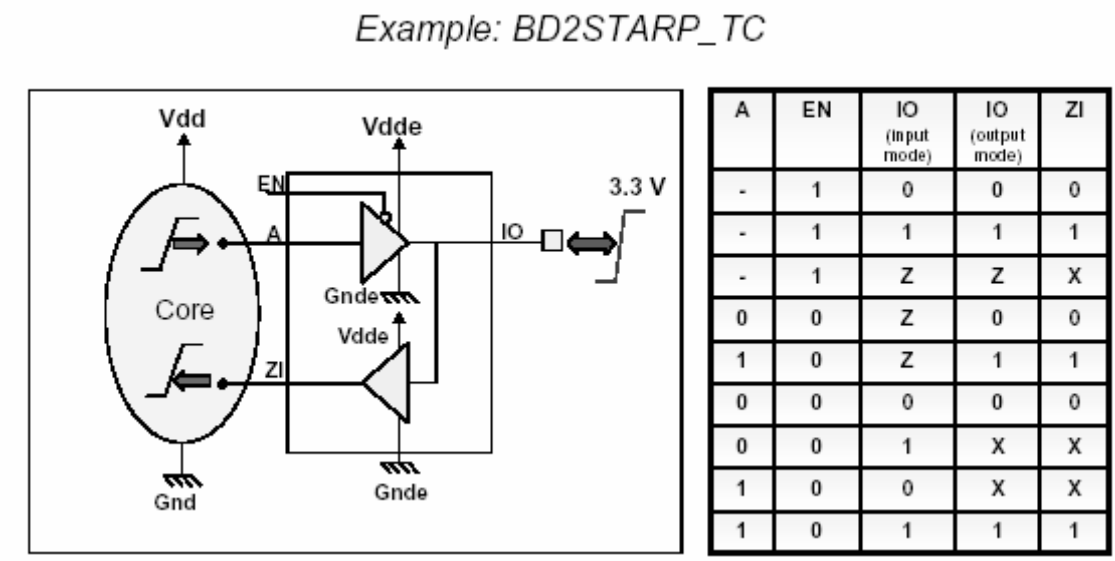


Figure 3: Block diagram of Output Section

1.3.3. Bi-directional

The IO can either be programmed in input or output mode BiDir, Tri-state. Normal bidirectional buffers are tri-state output buffers associated with an input buffer. All the characteristics for both the input and output section must be satisfied by the bidirectional buffer. Also, there are some bidirectional buffers which have tri-state both input and output section to interface external and internal buses



A	EN	IO (input mode)	IO (output mode)	ZI
-	1	0	0	0
-	1	1	1	1
-	1	Z	Z	X
0	0	Z	0	0
1	0	Z	1	1
0	0	0	0	0
0	0	1	X	X
1	0	0	X	X
1	0	1	1	1

Figure 4: Block diagram of InOut Section

1.4. Basic Building Blocks of I/Os

1.4.1. Input Section

Since this section is directly connected to the core so it has to make sure that the signal is within the operating limit of the core. As we have different output stages for different needs, similarly in input stage section, we have a variety of different functionality blocks to fulfill our requirement.

1.4.1.1. Input with Pull-up and Pull-down

Often the input is put to a particular logic level instead of letting it float. Either logic low or logic high is connected to the input pin when it is not used.

This is achieved by pull up or pull down circuits. They may have switch to connect the input to pull up or pull down circuit. The switch versions are useful for example when IDDQ testing is required since in this case all I/Os can be put in a zero DC power consumption state. If no signal is present on the bus, a resistive load pulls up or pulls down the bus.

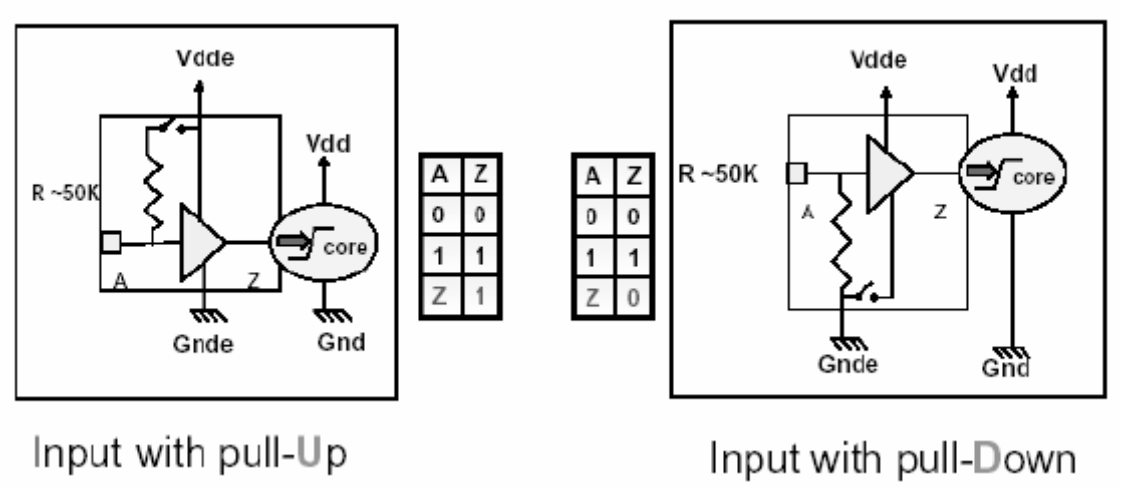


Figure 5: Pull-up and Pull-down Sections

1.4.1.2. Input with Hysteresis: Schmitt trigger

Hysteresis is often required in input buffers to decouple the noisy external signal from the core circuitry of the chip. Generally the circuit is biased at VDD/2 and therefore if due to introduction of noise in the input signal, the signal oscillates around VDD/2, the output of the circuit oscillates between logic level 1 and logic level 0. To avoid these unwanted oscillations, basic principle of different switching thresholds for input signals from low to high and high to low transitions is employed.

Transistors with different threshold voltages are used and further controlled by body effect. The difference in switching level for low to high and high to low avoids the conduction of p and n transistors simultaneously or in the narrow range of input voltage. Whenever two or more transistors are connected in series, the potential difference between source and substrate increase as we move away from the transistor whose substrate and source is tied together .This results in increase in the width of depletion layer which in turn increase the channel substrate junction potential. This increases the gate-channel voltage drop. The overall effect is increase in the threshold voltage. This whole phenomenon is known as *Body effect***.**

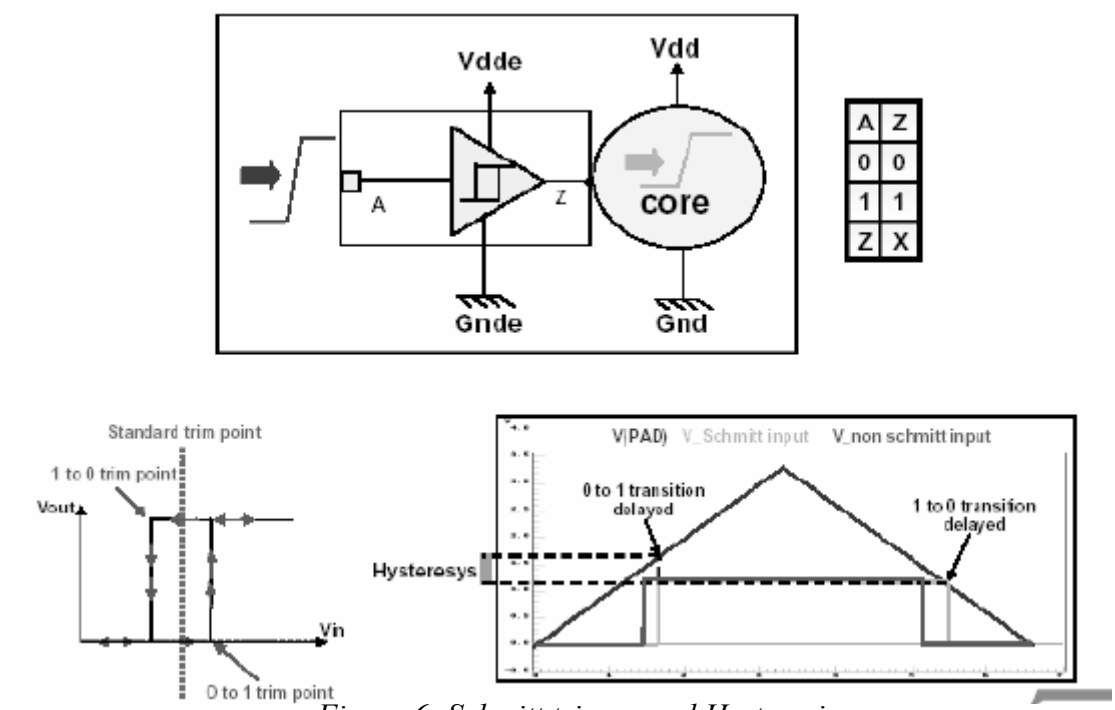


Figure 6: Schmitt trigger and Hysteresis

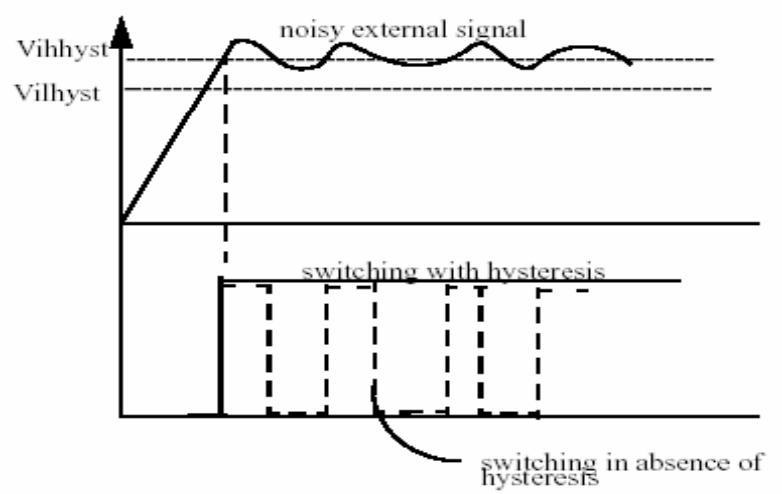


Figure 7: Switching in absence of hysteresis

1.4.1.3. CMOS and TTL Buffer

An external signal may be either CMOS or TTL. Normally the design of input buffers consists of cascaded CMOS inverter chain sufficient to drive the internal load. A CMOS to CMOS buffer is very simple, having to inverters cascaded together. Gate lengths of first stage inverter are greater than the

normal gate lengths to prevent early avalanche breakdown with high input gate voltages. Many times TTL or ECL chip is used, for increasing the speed or to perform some specific function, with CMOS. So a circuit is required to convert TTL logic to CMOS logic at the input section. This circuit has inverter which has been scaled down to switch between the TTL logic thresholds.

1.4.2. Output Section

Output buffers are used to drive large capacitive loads which arise from long global interconnect lines such as clock distribution networks, high capacitance fan out and high off chip loads. An output buffer must have sufficient drive capability to achieve adequate rise and fall times into a given capacitive load. To achieve the specified functionality of the output buffer, different types of output stages are used at the output section.

1.4.2.1. Push Pull Stage

A push pull stage consists of p and n transistors at the output pad for sourcing and sinking respectively, where each of transistors is controlled through a different chain of tapered inverters fed after buffering. This has two advantages:

- No direct gate contacts of the two output driver transistor.
- Static and short circuit power dissipation can be avoided by bifurcating the inverter chain in a way such that while sourcing current at the output pad, NMOS driver is made off before PMOS is on and vice versa.

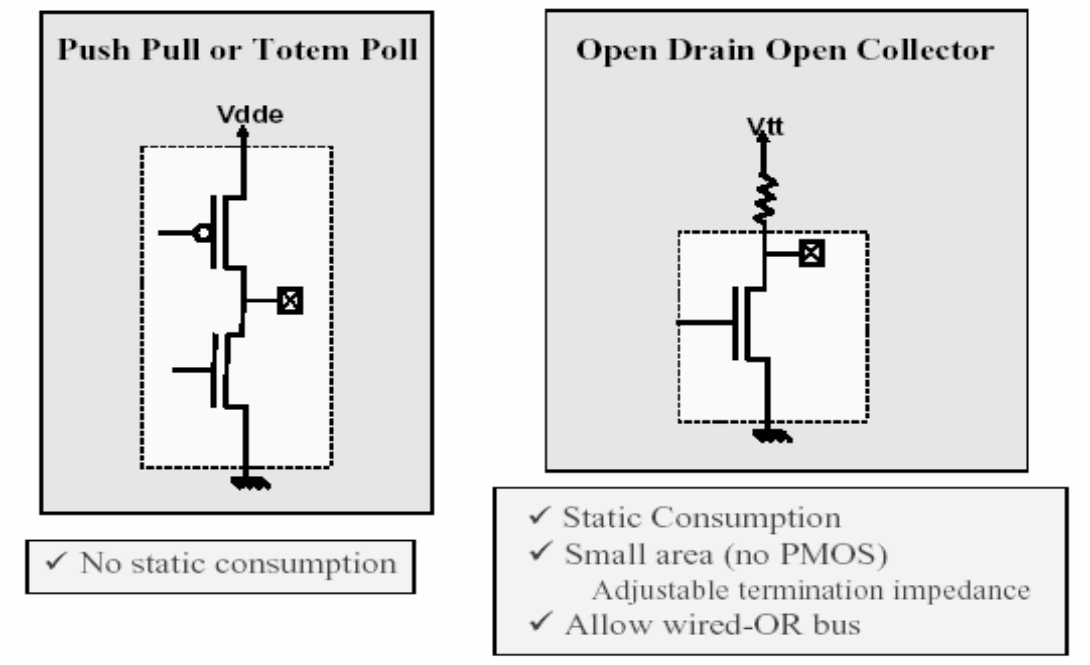


Figure 8: Different pull-up circuits

1.4.2.2. Open Drain Output Stage

This has an advantage over the push pull, and that is, it has just one driver stage. Such configuration avoids gate source-drain capacitance, thus making it faster than push pull. But this configuration can either sink or source current at a time, which limits its usage. The output state of the pad can also be driven to tristate and can be connected to buses where high impedance state is required for data transfer.

1.4.2.3. Push Up/down Stage

Often the tristated output is put to a particular logic level instead of letting the bus float. Either logic low or high can be made at the output using the pull up or pull down transistors. Normally the NMOS transistor is used for pull down and PMOS transistor for pull up. But the strength of the transistor is so chosen that when a logic level appears at the output from core, it must overcome the pulling up or pulling down action.

1.4.3. Predriver

This block is used at the output section of the chip and is connected between the core and slew rate control block .A predriver consists of multiplexer, to select the test mode or basic operating mode, series of inverters to generate two signals NIN and PIN at the output for slew rate control. The signal at NIN rises faster than PIN while signal at PIN falls faster than NIN.

1.4.4. Slew Rate Control

A fast transition of the signal at the output pad tends to introduce frequencies in UHF range into the off chip load being fed. Most of the time, it is undesirable and thus appears as noise. The source of this noise is the inductive voltage which is due to the inductance of the introduced by the package pins. To reduce this noise, we generally control the switching which reduces the rate of change of current at the output. Slew rate control circuits thus artificially limit the rate of current switching thereby limiting the UHF interference.

Sometimes slew rate gets affected due to change in PVT and even the slew rate controller cannot do anything as they are hardcode while fabrication. So to compensate for the change in slew rate in changing PVT conditions, codes are fed through a compensation block which generates the code according to the conditions. Compensation block has only an enable pin and the output pins. This block senses the change and generates a common code for all the slew rate controlling devices.

Now a problem arises, generally we have same slew rate for all the I/Os inside a chip but in some special cases we can require different slew rate for different I/Os and as there is one or at the most two compensation blocks inside the chip, the generated code is same for all the I/Os and hence there would not be any difference in their slew rate as required. So to overcome this problem, some modification is done at the cell level. The normal functioning code is noted down for all the slew rate controllers and some circuit is added at that level to

generate the required code from the common code generated by the compensation block for each controller.

1.4.5. Electrostatic Discharge

Protection is very important to save the chip from unwanted voltages which gets developed at the pin due to some source coming in contact with the pin. This large accumulated charge can destroy the transistor, so a mechanism is needed which can effectively and quickly discharge this unwanted accumulated charge.

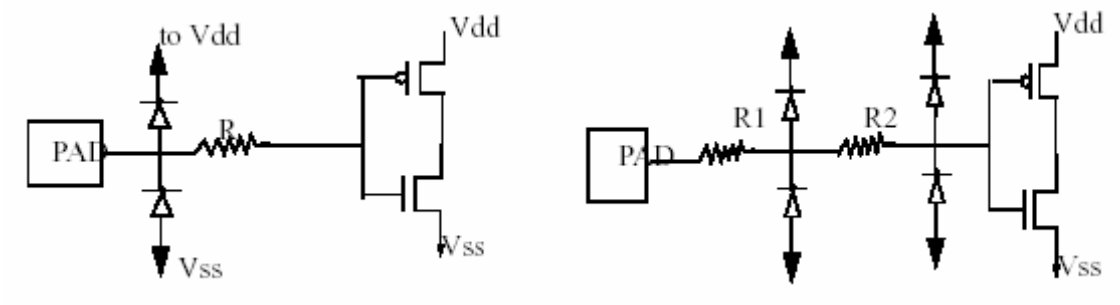


Figure 9: ESD Protection

An input buffer couples the external off chip signal to the core elements of the chip. Since the external signal can have voltage ranges much beyond the normal CMOS operating voltages, an input ESD protection is required for these buffers. Non-destructive breakdown of diodes is utilized to clamp the voltage between VDD and VSS. The resistor tends to decrease the current reaching gate. But this block introduces RC delay; hence the design has to be optimized if used in high speed circuits.

1.4.6. Power Supplies

Power supply is required to bias the circuit and, as the circuit consists of both the I/O and the core, therefore we have different power supply for these two. The primary goal of having different rails is *to minimize the effect of the noisy output buffers*. The power supply for core should be clean i.e. it should not contain any noise. I/O section is connected to the outside world where the signal

is more prone to get diluted with noise; therefore the separation for the two power supply is must in those chips where even a slight amount of noise can degrade the performance of core to a greater extent.

In some chips, where the noise has little or no effect on the performance of the core, both I/Os and core can have the same power supply. These pads are basically a sandwich of various metal layers used in the design. The pads consist of pins and metal connection on all sides to provide the power connection to both the Core (Internal Library elements) and the I/O elements. The power and ground bus widths may be calculated using the worst case power dissipation estimate.

1.4.7. Latch Up

It is a parasitic effect and results in shorting of the VDD and VSS lines, usually resulting in chip, self destruction or at least system failure with the requirement to power down. In a chip due to presence of both the NMOS and PMOS transistor on the same substrate, the combination results in a circuit which is composed of an NPN transistor, a PNP transistor and two resistors connected between the power and the ground rails. This whole thing results in action similar to a PNPN thyristor which has latching property i.e. as the circuit behaves like a positive feedback amplifier so after a certain value of applied voltage, called the trigger point, the circuit snaps and draws a large current while maintaining a low voltage across the output. This is, in effect, a short circuit which can destroy the MOS transistors.

Latchup can be triggered by transient currents or voltages that may occur internally to a chip during power up or externally due to voltages or current beyond operating ranges. During normal circuit operation in internal circuitry this may occur due to supply voltage transients, but this unlikely. However, these conditions may occur at the I/O circuits employed on a CMOS chip, where the internal circuit voltages meet the external world and large currents can flow.

Prevention

Latchup may be prevented in two basic ways:

1. **Latchup resistant CMOS processes**

In this method, the substrate is doped with varying degree of doping, bottom is highly doped whereas the upper portion is lightly doped compared to bottom. This reduces the parasitic resistances offered by the nwell and the substrate and hence reduces the gain of the circuit. This shifts the triggering voltage to higher value than VDD and prevents the Latchup

2. **Layout Techniques**

In this method, the p+ substrate of NMOS transistor is *surrounded by the nwell of the PMOS transistor,* which acts as dummy collectors and spoils the gain of the parasitic transistor by collecting minority carriers and preventing them from being injected into the respective bases.

1.5. Nomenclature of Buffers

A standardized naming convention is adopted for all the types of buffer, so that even at just looking at the name of a buffer, viewer can have sufficient information about the buffer.

Abbreviations used for different types of buffers:

IBUF	CMOS input buffer.
TLCHT	TTL input buffer.
SCHMIT	Input buffer with hysteresis.
B	Push pull output buffer.
BT	Tri-state output buffer.
BI	Bidirectional buffer.

Suffix used to indicate the characteristics of buffers:

2,4,8	For different driving capability in mA.
C	CMOS buffer.
T	TTL buffer.
R	Slew rate control.
AR	Active slew rate control.
H	High drive input stage.
U	Active pull up (Input buffer).
D	Active pull down (Input buffer).
Q	Switch on pull up/down.
P	Test pin.
OD	Open Drain (Output buffer).
_FT	5v Tolerant.
S	Schmitt trigger on input.
ZI	Tristate input stage.

CHAPTER 2 CHARACTERIZATION FLOW

2.1. Characterization Flow

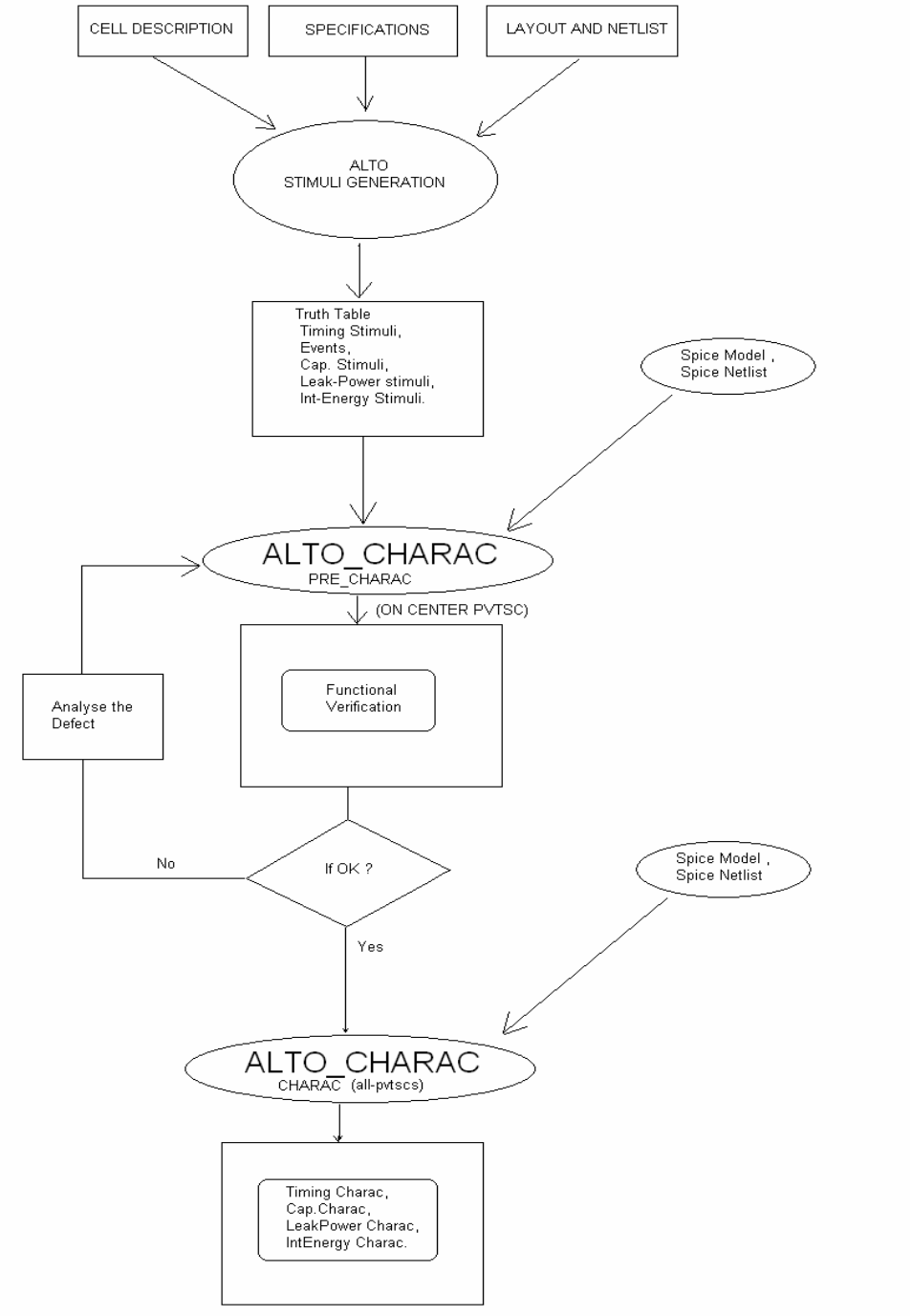


Figure 10: Characterization Flow

2.2. Inputs

2.2.1. Cell Description

The cell functional specification is a netlist of structural primitives. The primitives are based on a subset of the IEEE.STD_LOGIC package.

The cell specification is also written using a simple Lisp-like syntax. The usual parameters are:

- the name of the cell,
- the list of inputs,
- list of outputs,
- a short phrase describing the cell,
- netlist.

The basic template for cell description will always be the following:

```
(cell ’name
        :text "description of the cell"
        :lin ’(input1 ... inputN)
        :lout ’(output1 ... outputN)
        :netlist
        ’(list of assignments))
```

2.2.2. Specifications

The library specification is now in a simple ASCII format. The file is lib.spec, at the root directory.

The configuration of the tools that are part of the library development is too complex for a production flow. We decided to have a common specification file for all the tools, with a simple format.

The library specification file will contain the following informations:

- global definition (name, version temperature)
- default units (usually nS, pF, V)
- supplies definition
- pattern description (which values to apply on input pins)
- threshold definition (slope, cload and time)
- capacitance and slope range definition
- PVT definition
- operating point (used for precharacterization)
- description of a characterization methodology

2.2.3. Netlist

Netlist reflects the physical organization of the cell. It is a set of assignments. Each assignment line computes the value of an output or an internal signal from the values of the inputs.
For example:

(z (andgate a b))

The internal signals need not be declared before being used. The order of the lines is very important. An internal signal cannot be used in the right-hand side of an assignment before it was first assigned a value.

2.3. Stimuli Generator

The Alto Specification gives a complete functional model of a cell. From this, search algorithms generates test patterns which can be used to test cell models and for timing characterization. There are three kinds of test patterns:

- functional
- propagation delay
- timing constraint

For combinational cells, a functional test simply covers all 2^n input combinations. A propagation delay test covers all single input changes that result in an output change. Combinational cells have no timing constraints.

For sequential cells, a functional test covers all single input changes for all combinations of input and state variables. A timing test is much shorter, covering only those single input changes for combinations of input and state variables that result in an output change. Timing constraint sequences include setup, hold, pulse width, and other constraints.

Test sequences can become extremely long when a cell has many inputs. It can become necessary to limit the length when memory or time limits are exceeded. Good judgment is necessary here, as any omission could lead to an undetected fault in a cell model. Murphy's Law applies here.

2.3.1. Functional Stimuli File Format

The stimuli file is in ASCII format, organized as lines and columns.At the head of the file, pin directions are declared in comment lines.

The first non-comment line contains pin names. Input pins are The rest of the lines in the stimulus file are test steps. The only characters {0 1 X L H W Z U} separated by spaces or tabs.

2.3.2. Timing Stimuli File Format

The format for the timing stimuli file is similar to the functional stimuli file syntax. After the usual logical values, there are some extra columns. Any line in the file that does not have these extras is not a timing event. These extra columns specify the arcs (input Conditions).

2.3.3. Intenergy Stimuli File Format

The format for the timing stimuli file and intenergy stimuli is the same. Moreover the intenergy and timing stimuli are strictly identical for combinational cells. You have extra event definition for all stable arcs for sequential cells.

2.3.4. Leakpower Stimuli File Format

The format for the leakpower stimuli file is similar to the functional stimuli file syntax. After the usual logical values, there are some extra columns. Any line in the file that does not have these extras will not produce leakpower measurement. The algorithm to get the leakpower stimuli is identical to functional algorithm. Only extra information on state is added at each line.

2.4. AltoCharac

Altocharac uses by default the Eldo electrical simulator to measure input capacitance, input threshold, crosstalk sensibility, propagation delay, rise time, delay and slope degradation with frequency, leakage power, internal energy and timing constraints (setup, hold, recovery, removal, pulse width). The other simulators supported are HSIM and Eldomach.

Alto in the initialization step generates reference files for timing, capacitance, constraints and power characterization. These reference files have a generalized structure so that the tool can read the reference stimulus from these reference files.

These reference files contain s the information regarding the Load capacitance, voltages , temperature and process to be used for different pvtsc conditions.

2.4.1. Inputs

The simulator needs to have a model of the cell. SPI is the cell netlist extracted from the layout. The transistor and diode device models are also needed.

Alto models give the logical function, voltage levels of the cell.Stimuli (logical sequences) that identify and exercise the timing events can come from Alto or be edited manually.

The characterization setup defines what operating conditions space to explore and what derating strategy to use.

2.4.2. Outputs

The timing information produced by characterization is stored as tables of raw data in an ASCII table format called RDB.

In a second step this database can be read to produce all Unidata views having characterization information (lutiming, lurfall, tdef, drc, intenergy, leakpower, cap, ...).

CHAPTER 3 LIBRARY SPECIFICATIONS

3.1. Introduction

The configuration of the tools that are part of the library development is too complex for a production flow. So there is a common specification file for all the tools, with a simple format. The library specification file will contain the following information:

- Global definition (name, version temperature)
- Default units (usually nS, pF, V)
- Supplies definition
- Pattern description (which values to apply on input pins)
- Threshold definition (slope, cload and time)
- Capacitance and slope range definition
- PVT definition
- Operating point (used for precharacterization)
- Description of a characterization methodology

Following is the specifications example that a lib.spec (Specification file) will contain. Specification is not complete and will vary according the tools used and the library to be characterized.

3.2. Keywords

```
##-----------------------------------
## GLOBAL DEFINITION
##-----------------------------------
        NAME
        TEMP_MIN
        TEMP_MAX
```

```
##-----------------------------------
## UNIT
##-----------------------------------
        TIME_UNIT
        LOAD_UNIT
        VOLTAGE_UNIT
        POWER_UNIT
        ENERGY_UNIT

##-----------------------------------
## SUPPLIES
##-----------------------------------
        SUPPLIES
        GROUNDS
        SUPPLY_RANGE
        VDD
        GND

##-----------------------------------
## PATTERN
##-----------------------------------
        INPUT_VALUES

##-----------------------------------
## TIME THRESHOLD
##-----------------------------------
        DEFAULT_TIME_THRESHOLD
        TIME_THRESHOLD TTL
        TIME_THRESHOLD CMOS

##-----------------------------------
## CAP THRESHOLD
##-----------------------------------
        DEFAULT_CAP_THRESHOLD
        CAP_THRESHOLD DEFAULT

##-----------------------------------
## SLOPE THRESHOLD
##-----------------------------------
        DEFAULT_SLOPE_THRESHOLD
        SLOPE_THRESHOLD DEFAULT
```

```
##----------------------------------
## SWING
##----------------------------------
        DEFAULT_SWING
        SWING DEFAULT

##----------------------------------
## MISCELLANEOUS
##----------------------------------
        GLITCH_TOLERANCE
        DEFAULT_ELECTROMIGRATION
        CURRENTDECREASEFACTOR
        CELL_NAMES
        SPLIT_NUMBER


##----------------------------------
## OPOINT definition
##----------------------------------
BEGIN OPOINT FUNCTIONAL
        PROCESS
        VOLTAGE
        TEMPERATURE
        SLOPE
        CLOAD
END

##----------------------------------
## PVT definition
##----------------------------------
BEGIN PVT nominal
        CENTER
        CENTER_LEAKAGE
        PROCESS
        VOLTAGE
        TEMPERATURE
        CENTER_SLOPE
        CENTER_CLOAD
        SELECT
        ELECTROMIGRATION
        NETLIST
END
```

3.3. Description

Description for the terms used in the above paragraph is shown below.

TIME_UNIT = 1e-9
LOAD_UNIT=1e-2;
VOLTAGE_UNIT = 1;
POWER_UNIT=1e-12; # pW
ENERGY_UNIT = 1e-12; # pJ
	This gives the default unit for time, capacitance, voltage. All the data read or generated by Alto is displayed using the default unit specified here.

CLOAD ciocap = 0.01 0.04 0.1 0.4; CLOAD ciocap2= 0.02 0.08 0.2 0.8; DEFAULT_CLOAD = ciocap;	Define two ranges of capacitances, one names CIOCAP and the other CIOCAP2. It doesn't matter if the name is uppercase or lowercase. We give the default cload for the library.
SLOPE default = 0.1 0.2 0.3 0.4; DEFAULT_SLOPE = default;	Definition of a range of input slopes, and definition of the default slope range for the library.
TIME_THRESHOLD cmos = 40% 60%; TIME_THRESHOLD ttl = 1.4; DEFAULT_TIME_THRESHOLD = cmos	The definition of the thresholds used for the measurement of propagation delays. The values can be either relative (e.g. 40%, 60%) to the value of the supply of a given pin, or absolute (e.g. 1.4). If there are two values, the first is for the rising event, the second is for falling
CAP_THRESHOLD cap = 10% 90%; DEFAULT_CAP_THRESHOLD = cap;	Definition of the thresholds used for measuring input capacitances, usually relative to the supply on the pin
SLOPE_THRESHOLD default = 10% 90%; DEFAULT_SLOPE_THRESHOLD = default;	Definition of the thresholds used for measuring the output slopes.
SWING default = 0% 100% DEFAULT_SWING = default;	This defines the swing values for a pin. A swing of 0-100% means that the output voltage for a pin is between 0 and VDD. This is needed for some low swing IO cells, where the pad voltage is between 1.4V and 1.7V.
MODEL typ = model/hcmos7_mm9.typ; MODELworst=model/hcmos7_mm9.max	Definition of the process names and the associated file names of the SPICE models.
SUPPLIES = VDD VDD3; GROUNDS = GND;	Definition of the names of the supplies and the grounds of the library. At least one ground name is required; to use GND as a supply, a dummy ground name must be provided.

BEGIN OPOINT p1 PROCESS = typ; VOLTAGE = [VDD 2.5] [VDD3 3.3]; TEMPERATURE = 25; SLOPE = [default median]; CLOAD = [ciocap median] [ciocaph smallest]; END	This is the definition of an operating point. The operating point defines the conditions for one experiment, like a precharacterization. We give the process name, of which we can deduce the model files. Then the values to all the supplies of the library, Then we have the temperature. Then, we need to assign a value to the input slopes and output capacitances. For each SLOPE and CLOAD range, we tell Alto how to choose the value. INDEX <n> tells to choose the nth value of the range. MEDIAN, AVERAGE, SMALLEST, BIGGEST are supported. A number assigns directly a numeric value.
BEGIN PVT nominal CENTER = typ [VDD 2.0] [VDD3 3.3] 25 CENTER_LEAKAGE = typ [VDD 2.4] [VDD3 3.3] 20; CENTER_SLOPE = median; CENTER_CLOAD = average; ELECTROMIGRATION = 2.0; PROCESS = worst typ best; VOLTAGE = [VDD 1.5 1.8 2.0 3.3] [VDD3 3.3 3.3 3.3 3.3]; TEMPERATURE = -40 25 125; END	This is the important part of a lib.spec file. The definition of the space that will be explored during the characterization. CENTER defines the center of the space: this is the point taken as the origin for the deratings in P, V, T. It defines the range of P, V and T for the deratings. The electromigration limit is optional and default value is taken in DEFAULT_ELECTROMIGRATION.
GLITCH_TOLERANCE = 0.1 ;	This defines the tolerance taken in account during the changed of an output value. Alto takes in account the switch of an output pin only if the expected value is in the expected bounds for the pin ((usually 0 < value < VDD < value) and the percentage between the expected value and the real value exceeds GLITCH_TOLERANCE %

Table 1: Library Specifications

CHAPTER:4 BASIC POWER EXTRACTION METHODOLOGIES

4.1. Introduction

Basically there are two types of power in any circuit. They are static power and dynamic power.

Static power is the power dissipated because of the leakage in the circuit. It has nothing to do with transition. It depends only on the current state. So, in our further analysis we will call it as leakpower.

The dynamic power is the power dissipated because of switching. It depends on the switching states and stitching frequencies. But, instead of dynamic power the component more important for us is the power consumed over the specified time duration. It is nothing but the energy. So, we will call it as intenergy, i.e. internal energy.

4.2. Leakage Power

Leakage power or static power is the power dissipated by the cell when it is not switching, that is, when it is inactive or static. The largest percentage of static power results from source-to-drain sub threshold leakage. This leakage is caused by reduced threshold voltages that prevent the cell from completely turning off. Static power is also dissipated when current leaks between the diffusion layers and the substrate.

No extra circuits are needed for leakage power measurements and the standard network is used as shown below.

For each combination of inputs, we measure the current flowing through every supply and every pin of the cell. The result is given in POWER_UNIT.

$$W = \sum_{allpins} Vi \times Ii + \sum_{all\,\sup plies} Vj \times Ij$$

The result file is leakpower.rdb, which is an RDB file (pure ASCII, fields separated by tabs, easy to process with the set of RDB utilities or with tools like awk, perl, etc).

The Alto Leakage power experiment simulates all input pins configurations, which means that, in some cases, can create short circuits on inout pins. This leads to higher than normal leakage power values.

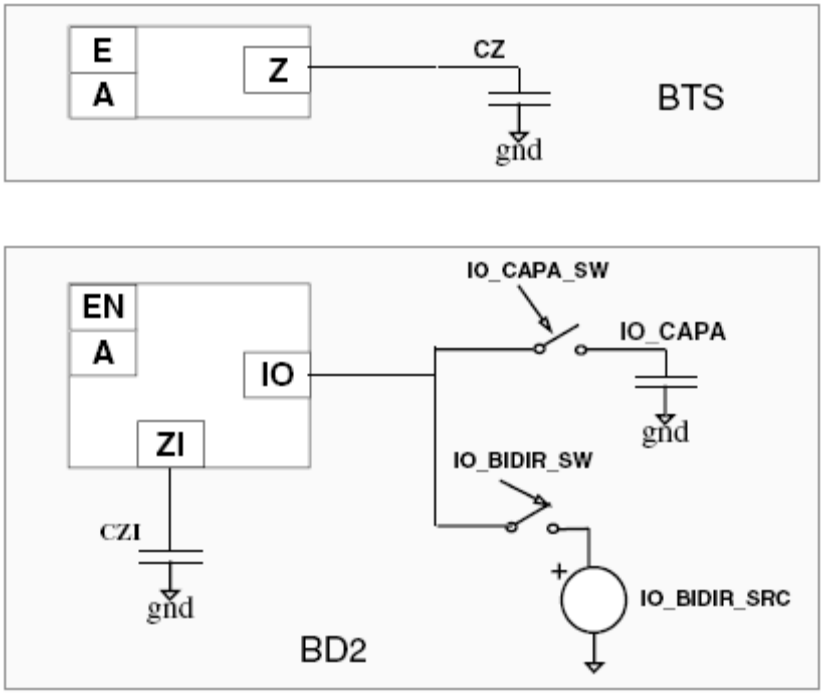


Figure 11: Arrangement for leakage measurement

Since the measurement of leakage power involves very small currents, it is wise to change the options according to the spice simulator used (for Eldo: put at least EPS=1e-8, use the BE integration method). Moreover, as the consumption must be stabilized, the step used for Leakage power measurement is specially defined by LEAKAGE_MIN_STEP parameter in lib.spec (default value: 0.01 seconds) and should be upper than STEP value.

4.2.1. Leakage power Measurement Algorithm

Alto includes an algorithm that checks if the consumption is stabilized. If consumption if not stabilized, Alto re-write the .cir file with a step 10 times bigger and re-launch the simulation, to let the cell reach a stable state for all states extracts. The criteria to decide if the consumption is stabilized is explained below, and use lib.spec parameter LEAKAGE_MIN_SLOPE (default value: 0.01)

In case we use multi_power flow, we provide a leakage_power value for each power_rail. We give the contribution in term of leakage of each power_rail. The sum of all new leakage_power value (one per power_rail) should give the same value than before (ie in standard flow). It also implies that contribution of each input has to be taken only once. The contribution of each input pin is taken only for the power_rail it is related to.

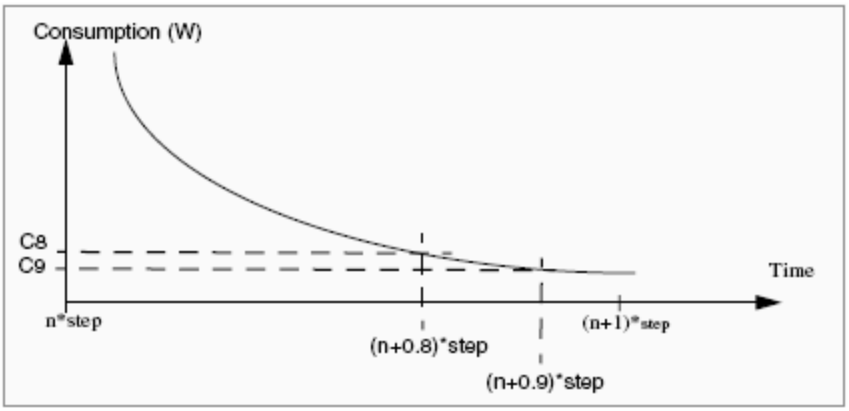


Figure 12: Timing slot for leakage measurement

On the graph above, “n” is the number of the stimuli line taken from leakpower.stim file. First line starts with n=0. At the beginning, the STEP is initialized to LEAKAGE_MIN_STEP.

After simulation, if the consumption detected as “not stable”, a new simulation is done with a STEP 10 times bigger. The loop finishes if the simulation is stable or if STEP = 10 seconds. In this last case, the status of the simulation is set to WARNING instead of OK.

By definition, consumption is considered as stable if, for each event:

$$LEAKGE\_MIN\_SLOPE > abs(\frac{C9 - C8}{STEP}) \times 100$$

Example for BD2SCARDQP_60OHM_2V5_LIN cell, with default parameters (LEAKAGE_MIN_STEP=0.01, LEAKAGE_MIN_SLOPE=0.01):

First extract to compute C8 on first state (n=0):

```
* LAB1 = "A0_EN0_TA0_TEN0_TM0_TUD1_IO0 () END 9.0e-4 9.0e-4 vdd"
.EXTRACT  LABEL="LAB1"
+ +YVAL(V(vdd), 800.0U) * -1 * YVAL(I(Vvdd), 800.0U)
+ +YVAL(V(A), 800.0U) * -1 * YVAL(I(VA), 800.0U)
+ +YVAL(V(EN), 800.0U) * -1 * YVAL(I(VEN), 800.0U)
+ +YVAL(V(TA), 800.0U) * -1 * YVAL(I(VTA), 800.0U)
+ +YVAL(V(TEN), 800.0U) * -1 * YVAL(I(VTEN), 800.0U)
+ +YVAL(V(TM), 800.0U) * -1 * YVAL(I(VTM), 800.0U)
+ +YVAL(V(TUD), 800.0U) * -1 * YVAL(I(VTUD), 800.0U)
```

Second extract to compute C9 on first state (n=0):

```
* LAB2 = "A0_EN0_TA0_TEN0_TM0_TUD1_IO0 () PREV 9.0e-4 8.0e-4 vdd"
.EXTRACT  LABEL="LAB2"
+ +YVAL(V(vdd), 900.0U) * -1 * YVAL(I(Vvdd), 900.0U)
+ +YVAL(V(A), 900.0U) * -1 * YVAL(I(VA), 900.0U)
+ +YVAL(V(EN), 900.0U) * -1 * YVAL(I(VEN), 900.0U)
+ +YVAL(V(TA), 900.0U) * -1 * YVAL(I(VTA), 900.0U)
+ +YVAL(V(TEN), 900.0U) * -1 * YVAL(I(VTEN), 900.0U)
+ +YVAL(V(TM), 900.0U) * -1 * YVAL(I(VTM), 900.0U)
+ +YVAL(V(TUD), 900.0U) * -1 * YVAL(I(VTUD), 900.0U)
```

-

In this simulation, we obtained LAB1=8.8882E-09 and LAB2=8.8882E-09, so the consumption is stable for this event. Unfortunately, for another event of the same simulation, we obtained 100*|C9-C8|/STEP > 0.01, which leads Alto to multiply STEP by 10 and re-launch the simulation.

4.3. Internal Energy

Internal Energy or Internal power is any power dissipated within the boundary of a cell. During switching, a circuit dissipates internal power by the charging or discharging of any existing capacitances internal to the cell. The definition of internal power includes power dissipated by a momentary short circuit between the P and N transistors of a cell, called short circuit power. See figure below (Inverter example):

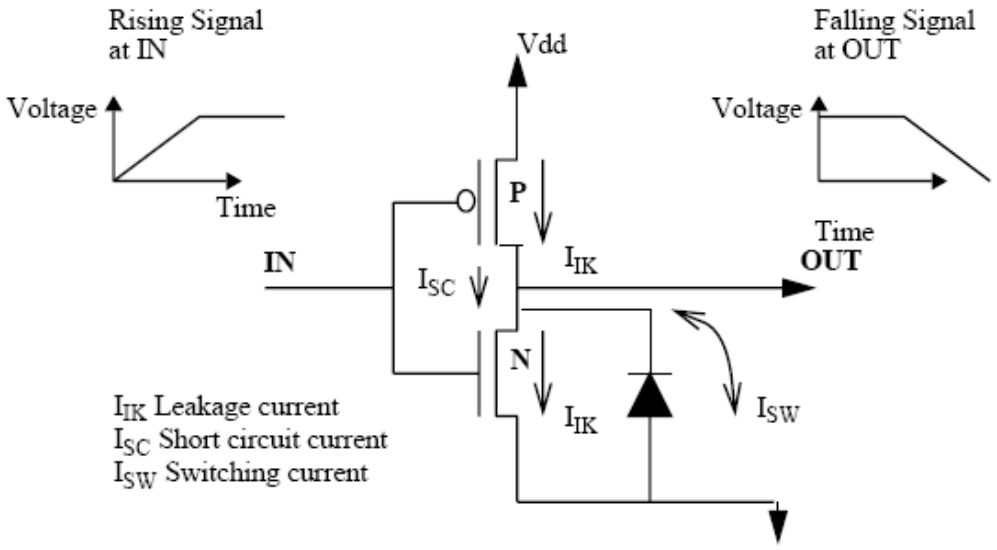


Figure 13: Various current components in an inverter

A rising signal is applied at IN. As the signal transitions from low to high, the N type transistor turns on and the P type transistor turns off. However, for a short time during signal transition, both the P and N type transistors can be on simultaneously. During this time, current Isc flows from VDD to GND, causing the dissipation of short circuit power (Psc).

For circuits with fast transition times, short circuit power can be small. However, for circuits with slow transition times, short circuit power can account for 30 percent of the total power dissipated by the gate. Short circuit power is also affected by the dimensions of the transistors and the load capacitance at the gates output.

The circuits added for Internal Energy simulation are identical to delay simulation.

Internal Energy analysis can be done on a simple RC switch circuit.

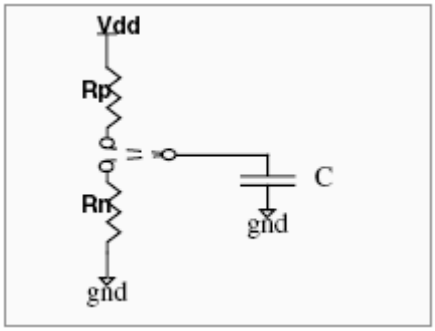


Figure 14: RC switch circuit

The switch connects the cap to Vdd or Gnd, as in CMOS inverters. The voltage on C rises to Vdd or falls to Gnd depending on which transistor is on.

The P transistor is just modeled as an ideal resistor Rp and a switch. Initially, assume the switch connects C to Gnd through Rn. At time 0, it immediately moves to connect C to Vdd through Rp.

For power analysis, this is the simplest CMOS model we can imagine! After t=0, current into C (i_C) equals the current through Rp (i_{Rp}). i_C's initial value is Vdd/Rp, and it decays exponentially to 0.

That is,

$$ic = (Vdd / Rp) \times e^{(-t)/(Rp \bullet C)}$$

The energy used to load the capacitance flowing from Vdd (Udd) during this rising half cycle is,

$$Uri\sin g = \int_0^\infty (Vdd \bullet ic)dt$$

$$Uri\sin g = \int_0^\infty (Vdd \bullet (Vdd / Rp) \bullet e^{(-t)/(Rp \bullet C)})dt$$

$$Uri\sin g = (Vdd \bullet Vdd / Rp) \bullet (-Rp \bullet C) \bullet \int_0^\infty (e^{(-t)/(Rp \bullet C)})dt$$

$$Uri\sin g = (-C \bullet Vdd \bullet Vdd) \bullet (0-1)$$

$$Uri\sin g = C \bullet Vdd^2$$

The energy used to discharge the capacitance flowing from Vdd during the falling half cycle is,

$$Ufalling = 0$$

The total energy per cycle is thus,

$$Utotal = C \bullet Vdd^2$$

To summarize, during the rising half cycle, half the energy is dissipated in the resistance Rp and half is stored in the capacitance. During the falling half cycle, the energy stored in the capacitor is dissipated in Rn, the N transitor. Of course, capacitors store electrical energy, but only resistance can consume.

4.3.1. Internal Energy Measurement Algorithm

Alto measurements extract from simulation, the power provided by power supplies and the power stored/released in each output pins (switch). The energy stored or released by capacitance is automatically calculated by alto.

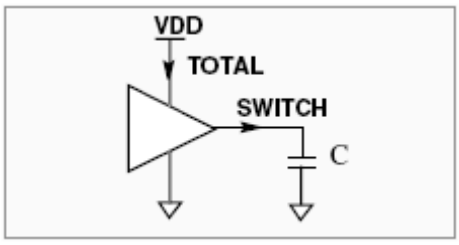


Figure 15: Buffer with C load

Internal Energy on a cycle is calculated by

$$Ecycle = E\_rising + E\_falling = Etotal\_rising + Etotal\_falling - CV^2.$$

The interval of integration for the consumption is given by the lib.spec parameter: INTENERGY_INTEGRAL_DURATION.

Alto provides two methods to fill the Internal Energy database according to the parameter INTENERGY_METHOD in lib.spec:

4.3.1.1. Method: 1

Here, Internal Energy is the energy provided by Vdd.

$$Erising = Etotal\_rising - CV^2$$
$$Efalling = Etotal\_falling - 0$$

The avantages of this method are:

1. ¨The Internal Energy views (and then, synopsys technology file) are no more dependent of the cload.
2. ¨Negative numbers for falling edges are removed.

4.3.1.2. Method: 2

Here, Internal Energy is the energy dissaped by the cell.

$$Erising = Etotal\_rising - CV^2/2$$
$$Efalling = Etotal\_falling - CV^2/2$$

This is the default method used for power characterization.

You can notice that the Internal Energy values defined in Internal Energy view is equal to TOTAL - CV2. So on a full cycle both methods are fully equivalent. The TOTAL value include the leakage consumption.

Deep sub-micron CMOS technologies shows that the internal energy taken directly from input pins are no more negligable compared to energy taken on power supplies.

4.4. Leakage for Internal Energy

No extra circuits are needed for leakage power measurements and the standard network is used.

Because the leakage consumption can be very high for high speed technology, in power characterization this consumption is extracted in a single simulation for each Internal Energy event.

The extraction methodology of leakage consumption is identical to Leakage power measurement except the leak-for-int is calculated by:

$$\text{Leak-for-int} = \text{Leakpower} \bullet \text{INTENERGY\_INTEGRAL\_DURATION}$$

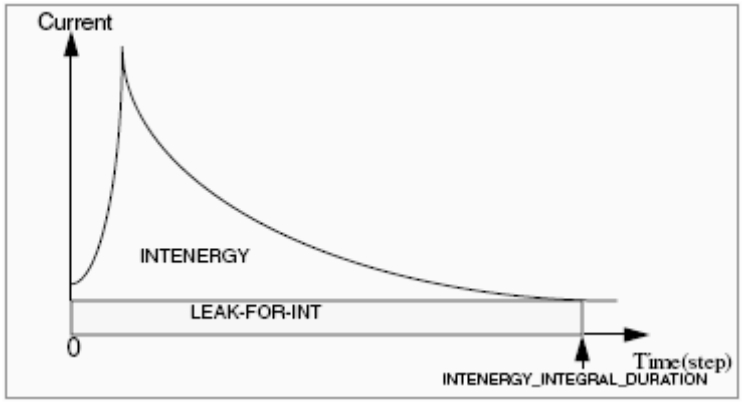


Figure 16: Leakage during internal energy measurement

Example for an inverter

EVENT	COND	LEAK-FOR-INT	PVTSC
10S	10S	9N	8S
A_R_Z_F		3.36305e-4	pvtsc12
A_F_Z_R		1.8861e-5	pvtsc12

4.5. Standard components added for all measurements

To do measurements, alto adds some components to the spice netlist. The following list of components is added to all type of measurement.

4.5.1. Global nets: supplies and grounds

Spice simulator needs to declare all power supplies as global variables, and it needs to have a voltage source for each of them. The steps Alto follows to provide these are:

1. List the names of the supplies used by the library. The list of supplies used is described at the library level. Even if the cell doesn't use all of them.

   ```
   SUPPLIES = VDD VDD3;
   ```

2. Check whether the supply is ground (if so, it's voltage is 0). The library has a set of ground supplies:

   ```
   GROUNDS = GND;
   ```

   To give a small voltage value to GND, you need to declare GND in the SUPLIES and a dummy ground name in GROUNDS.

3. If it's not ground, get the voltages from the TEC/ALTO/volt_ref.rdb. With the pvtsc extracted from *pvt_<pvtname>.ref* or *opoint<opoint_name>.ref*, alto reads the *volt_ref.rdb* file to extract all the voltage values.

All these steps result in spice commands similar to the following,

```
.GLOBAL VDD VDD3
.GLOBAL GND
VVDD VDD 0 2.5
VVDD3 VDD3 0 3.0
VGND GND 0 0
```

4.5.2. Temperature

With the pvtsc extracted from pvt_<pvtname>.ref or opoint<opoint_name>.ref, alto reads the pt_ref.rdb file to extract temperature.

```
.TEMP 25.0
```

4.5.3. Include files: models, netlist and specific netlist

According to the lib.spec parameters DK_MODEL DK_LIB_PATH and MODEL alto add include cards to insert spice models.

```
.INCLUDE <filename>
        or
.LIB transistor.lib PMOS
```

4.5.4. Internal wave definition

For internal needs, especially for power measurements, some DEFWAVE are inserted.

```
.DEFWAVE WVDD=-I(VVDD)*V(VDD)
.DEFWAVE WZ=-I(CZ)*V(Z)
```

4.5.5. Capacitance

Capacitance for each output pins are automatically added but for all inout pins a switch is also added to connect or disconnect the capacitance to the pin according to the sense used.

The switch is closed when the input value applied to the inout pin is equal to Z/L/H (output mode) to disconnect the capacitance.

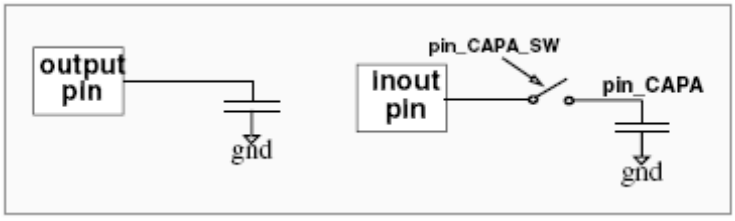


Figure 17: Capacitance added at pin

4.5.6. PWL for input pins

The default behavior is the following one: for all inputs pins which can take only 0 or 1 values a piece wise linear card is added:

```
#IN A
#OUT Z
A Z
0 1
1 0

VA A 0 PWL(
0.0ps 0.0
100000.0ps 0.0
100025.0ps 2.5
200000.0ps 2.5
+ )
```

4.5.7. Inout drive

To drive an inout pin (input mode), a switch connects (or disconnects) the voltage source to the pin. The switch is closed when the pin has to be drive (equal to 0 or 1). Default slope of this switch is 10 ps. If your cell has a very small slope, it can be necessary to decrease the switch slope.

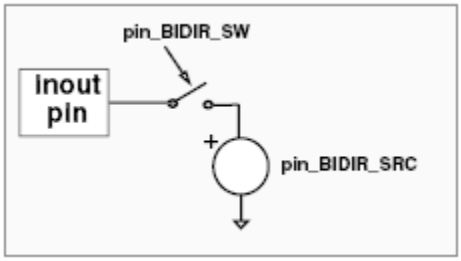


Figure 18: External source for InOut pin

CHAPTER:5 VARIOUS CURRENT COMPONENTS

5.1. Introduction

Five main parameters having major impact on leakage power and internal energy are process, voltage, temperature, slope and load. Also, fragmenting the current components responsible for leakage power and internal energy we have gate leakage, channel leakage, substrate leakage, switching and short-circuit currents. We will analyze the effect to each of the following parameter on the relevant component.

5.2. Effect of Voltage Variation

First of all let us start with the effect of change in voltage i.e. power supply on gate, channel and substrate leakage and on switching and shortcircuit currents.

5.2.1. Gate Leakage

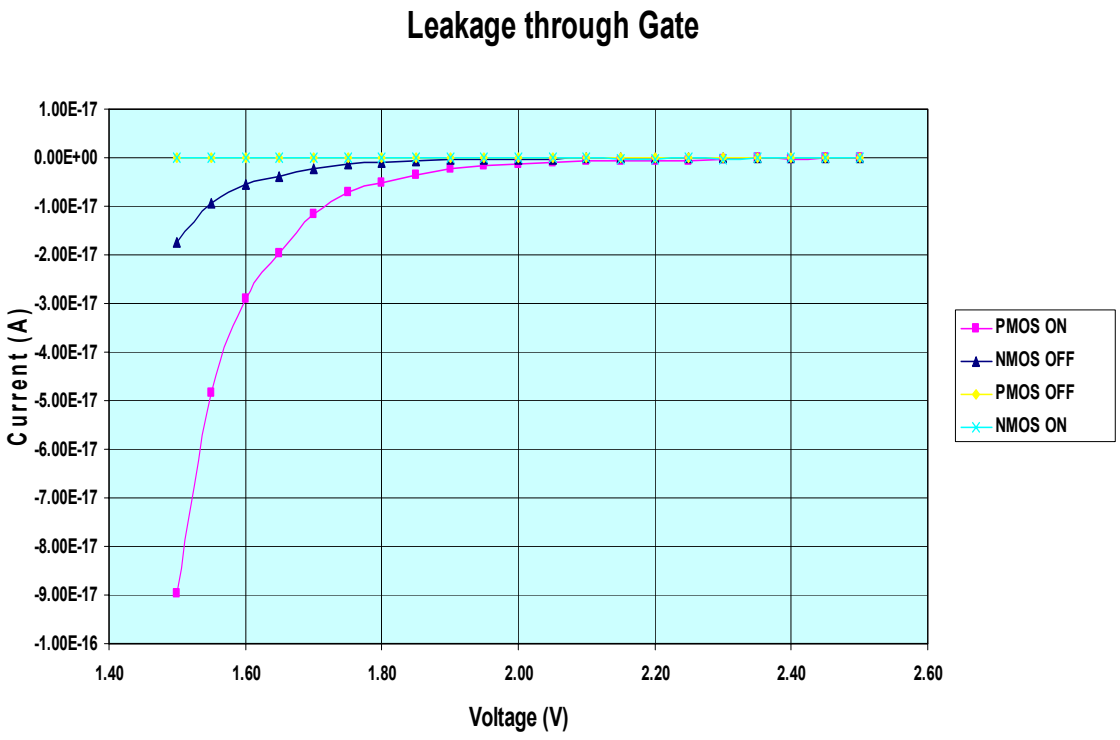


Figure 19: Gate Leakage for Voltage Variation

Gate Leakage occurs in any of these two states: Steady State or Transition State

Steady State: This can be either ON or OFF region.

• *OFF region:* In the steady-state OFF region, both gate and source are at ground while the drain is at high (V_{DD}) voltage. Since no channel is formed in this condition, the only active component is I_{gd}. The direction of the current flow is from diffusion to gate.

• *ON region:* In this region, both gate and drain of the device are held at high with the source being grounded. There exists a well-formed channel with three separate components of the gate tunneling current I_{gs}, I_{gcs} and I_{gcd}. The component from gate to drain overlap (*Igd*) has been extinguished due to the almost zero electric field in that region of the oxide. The overall current flow is from gate to source and channel, opposite to the flow in the OFF state.

Transient State: This state becomes important when the device switches from ON to OFF or OFF to ON. This change is not an instantaneous process; both the intrinsic gate capacitance and the gate tunneling capacitance will inhibit it.

As we can observe from the figure above that with increase in voltage, gate leakage decreases exponentially. Also, gate leakage is more prominent in the transistor which is on; because at that time Vgs is approximately equal to Vdd

5.2.2. Base Leakage

Leakage through base or substrate is linearly proportional to the voltage. As voltage increases leakage through base also increases.

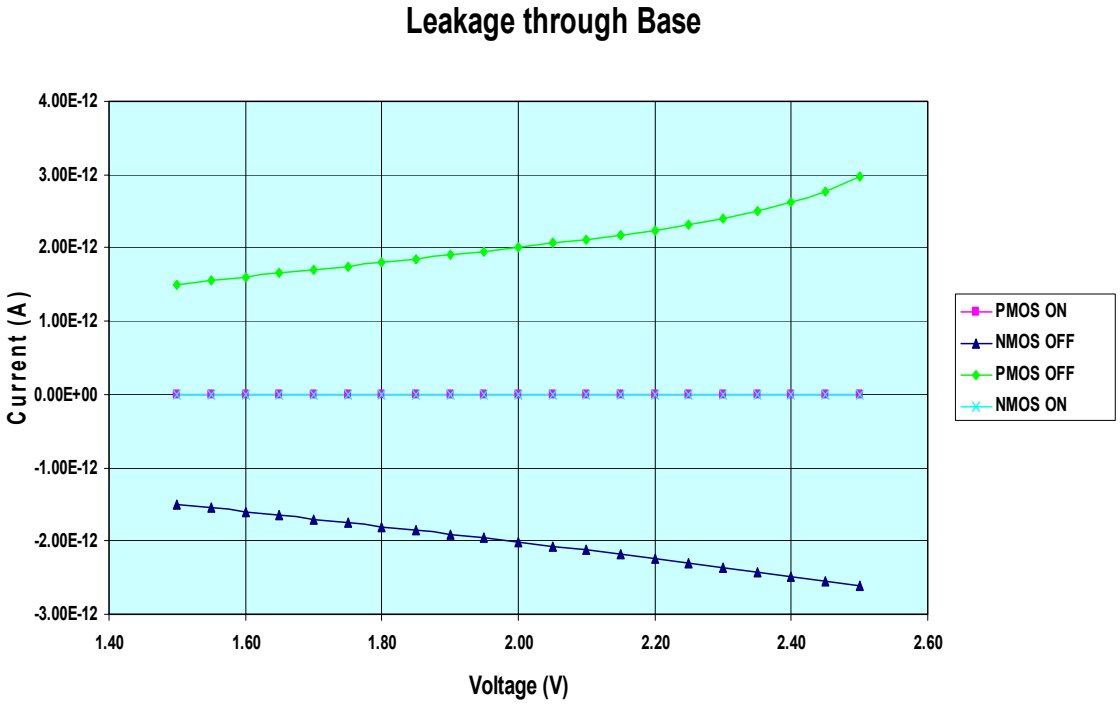


Figure 20: Base Leakage for Voltage Variation

5.2.3. Channel Leakage

As the channel length is reduced, these depletion regions occupy more space in the channel region. The depletion regions near the source and drain edges are shared with the channel. This effect produces a reduction in the threshold voltage with decreasing channel length and increasing drain to source voltage, the so-called short-channel and DIBL effects.

The DIBL and short-channel effects imply that shorter effective gate lengths than the nominal value will increase exponentially the I_{LEAK} current, while larger values of the channel length will tend to lower I_{LEAK} values.

Leakage through channel appears to be linearly proportional to the voltage, but is exponential according to the following equation.

$$I_{sub} = A \bullet (e^{a \cdot V_{OD} / V_T} - 1)$$

But because of multiplication factor of V_{OD} it seems to be linear in the lower range of voltage variation.

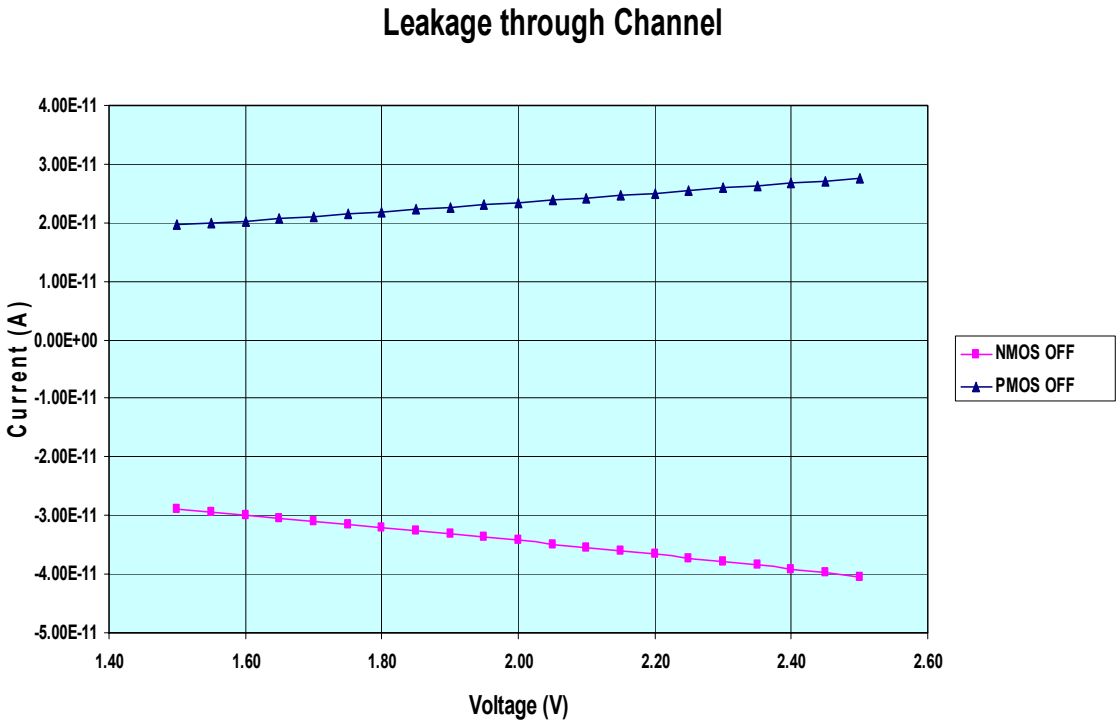


Figure 21: Channel Leakage for Voltage Variation

5.2.4. Switching Current

As voltage increases switching current also increases linearly. This can be verified with the charging current equation of the capacitor. Switching current is the component of current during transition state responsible for the charging the capacitance. Equation for charging current of capacitor is

$$I_C = \frac{V_{dd}}{R_p} e^{-t/R_p C}$$

From the above equation we can observe that Ic is directly dependent on supply voltage Vdd, which is very well seen in the plot of voltage Vs current.

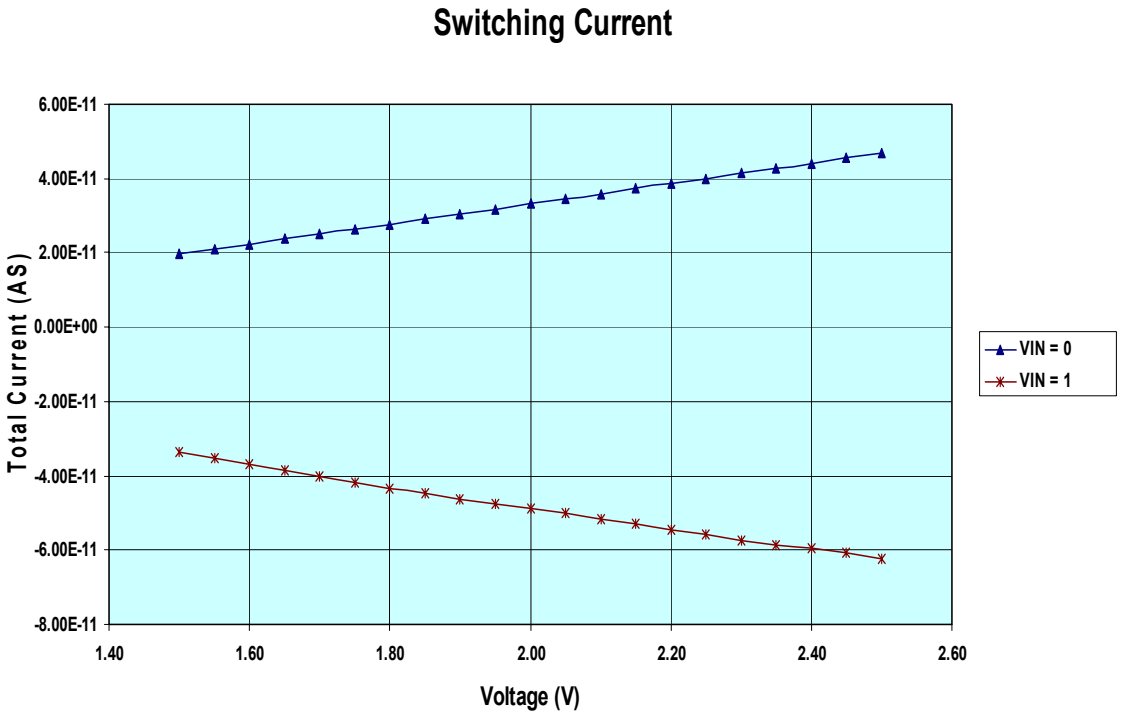


Figure 22: Switching Current for Voltage Variation

5.2.5. Short Circuit Current

In a static CMOS logic gate, the short-circuit current; I_{SC} is observed when both NMOS and PMOS devices form a DC path between power rails. The power associated with this current is referred to as short-circuit power. Since this power is delivered by the voltage supply (V_{DD}), the total short-circuit power (total energy per transition) can be written as

$$P_{SC} = V_{DD} \int_{T} I_{SC}(\tau)\, d\tau$$

where, T is the switching period.

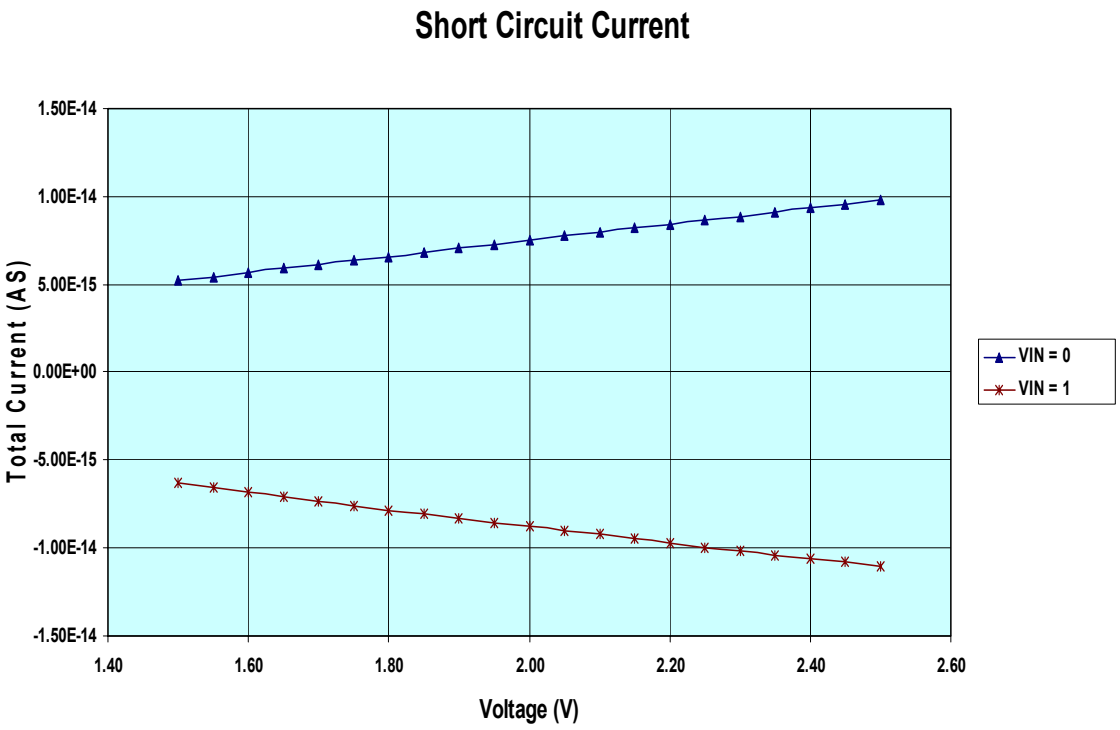


Figure 23: Short Circuit Current for Voltage Variation

Simulation results for the inverter in figure above shows that the Short circuit current varies almost linearly with the voltage.

5.3. Effect of Temperature Variation

5.3.1. Gate Leakage

The gate tunneling current is almost insensitive to temperature variation since the electric field across the oxide does not strongly depend on temperature.

But from figure we can see that ON transistor is under major influence than OFF transistor.

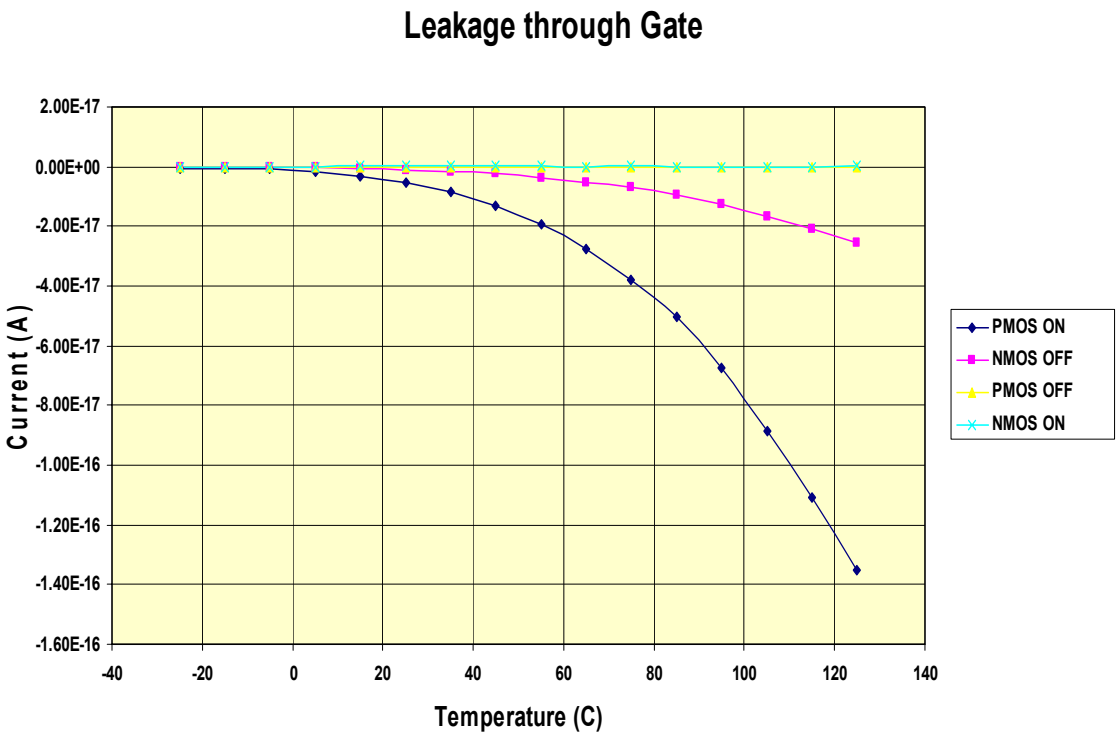


Figure 24: Gate Leakage for Temperature Variation

5.3.2. Base Leakage

The junction BTBT current increases with temperature due to the narrowing of bandgap at higher temperatures. The bandgap ($E_g(T)$) at a temperature T is given by

$$E_g(T) = E_g(0) - \frac{\alpha_T T^2}{(T + \beta_T)}$$

where $E_g(0)$ is the limiting value of the bandgap at 0K and is equal to 1.17 eV for Si. α_T and β_T are parameters with values $4{:}73 \times 10^{-4}$ and 636, respectively, for silicon. Due to the bandgap narrowing, BTBT increases with temperature.

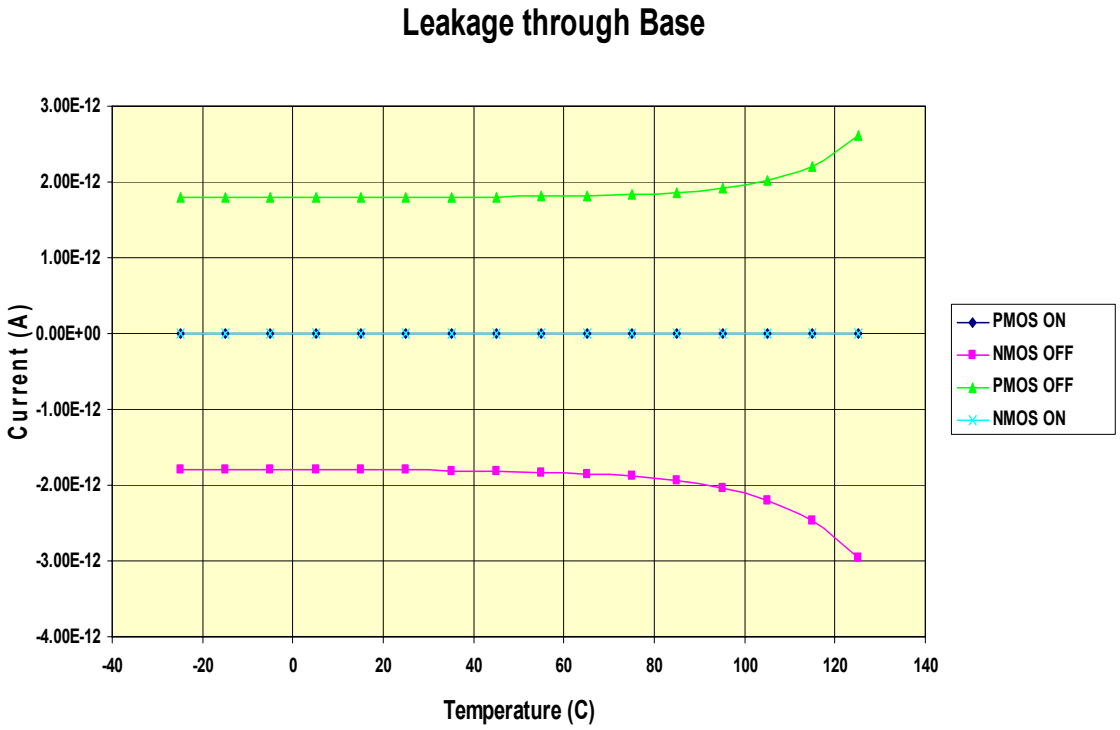


Figure 25: Base Leakage for Temperature Variation

5.3.3. Channel Leakage

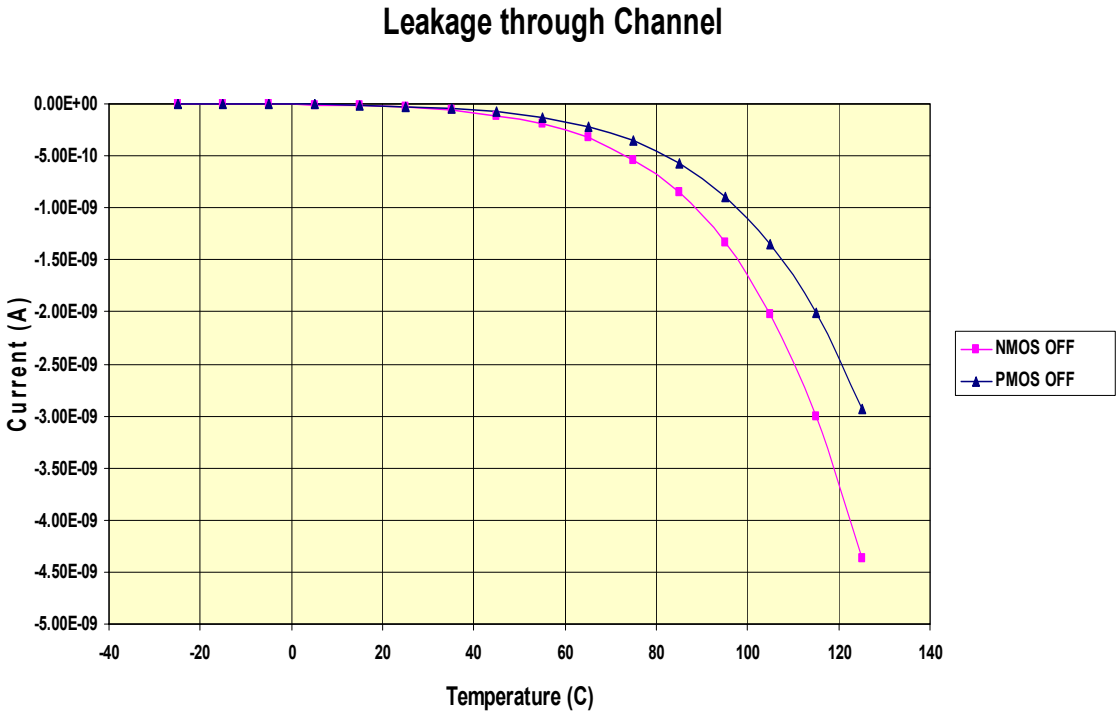


Figure 26: Channel Leakage for Temperature Variation

Subthreshold current increases exponentially with temperature due to reduction in threshold voltage (V_{th}), and increase in thermal voltage (V_T). This can be very well observed in the above figure. Also one can see for same device dimension PMOS is less leaky than NMOS.

5.3.4. Switching Current

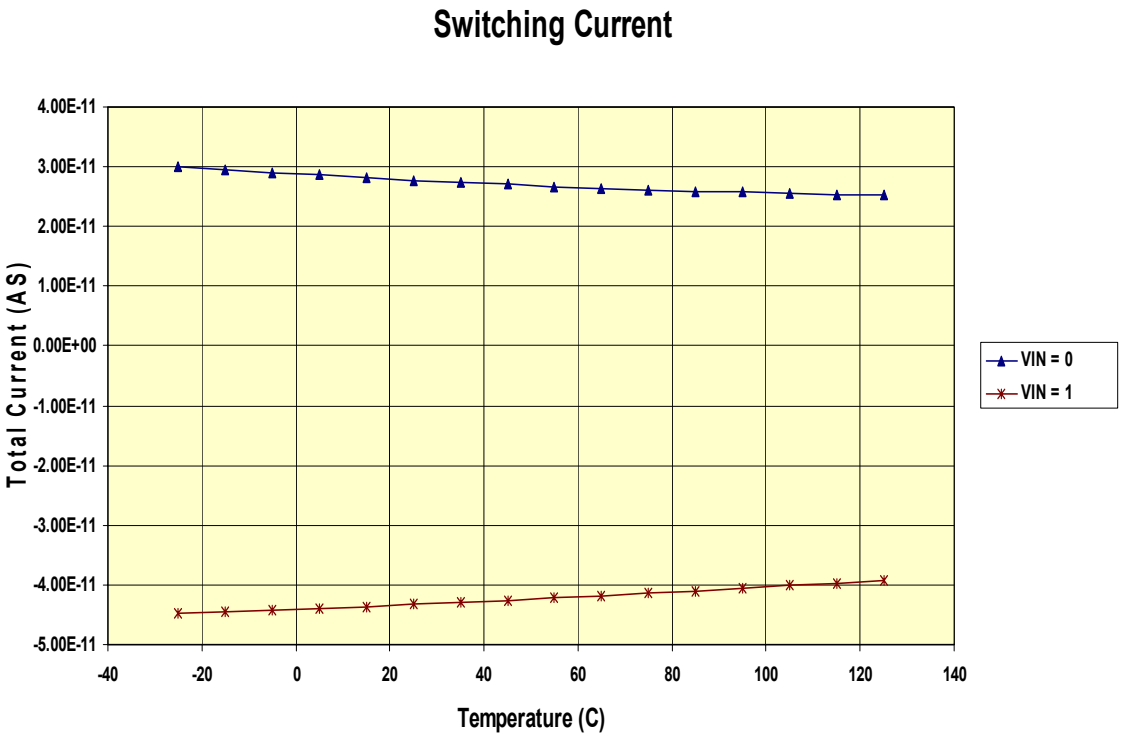


Figure 27: Switching Current for Temperature Variation

Switching current decreases with respect to the temperature. As temperature increases, value of capacitance decreases; as a result switching current also decreases.

5.3.5. Short Circuit Current

Effect of temperature variation is no that dominating in case of short circuit current that can be seen from the graph below. It is almost constant with respect to temperature variation in the given range.

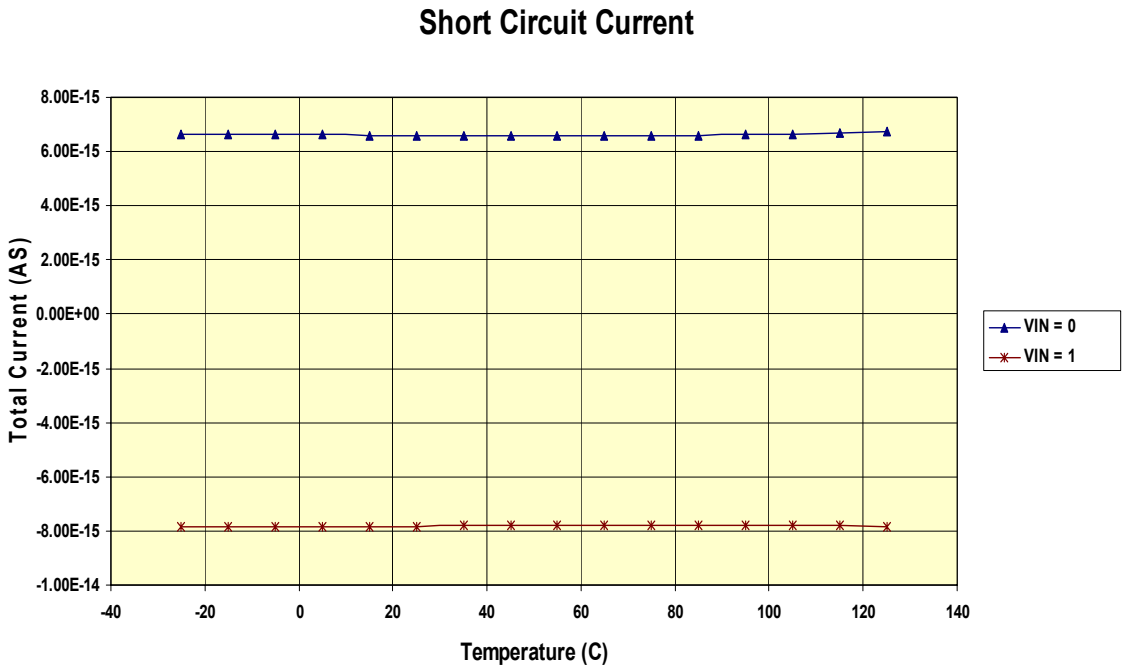


Figure 28: Short Circuit Current for Temperature Variation

5.4. Effect of Slope Variation

5.4.1. Switching Current

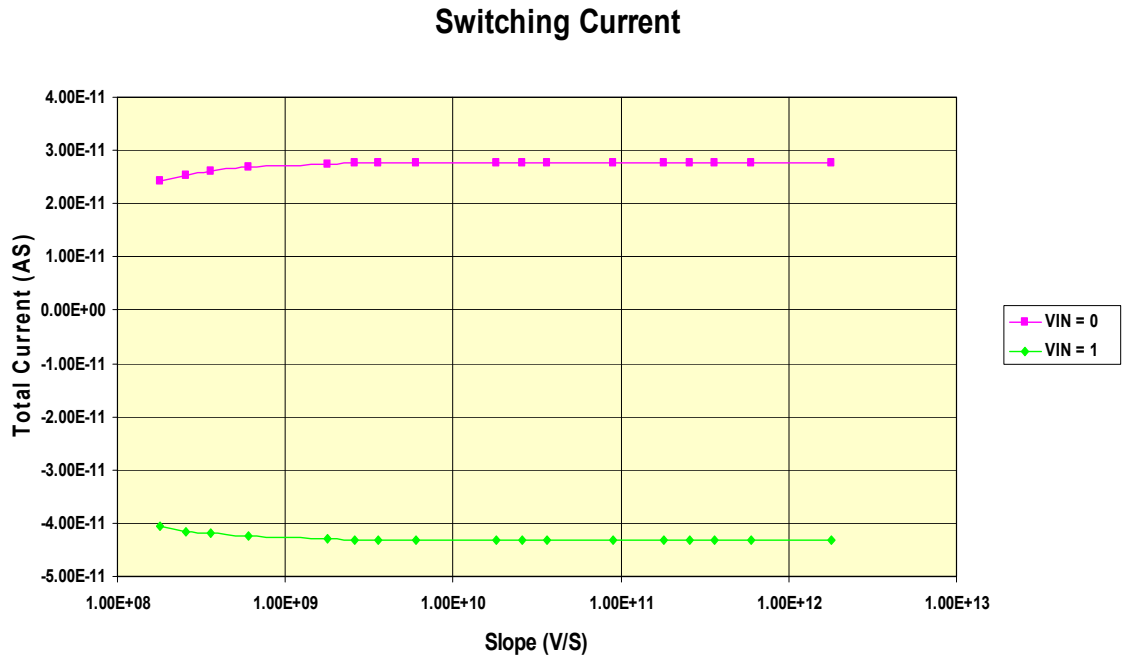


Figure 29: Switching Current for Slope Variation

At lower slope one can see that switching is lower but after that it is almost constant and slope variation do not have major influence on the switching current.

5.4.2. Short Circuit Current

Shortcircuit current decreases linearly with increase in transition time. Because as slope increase transistors get more time for conduction and hence more current will flow from Vdd to Gnd.

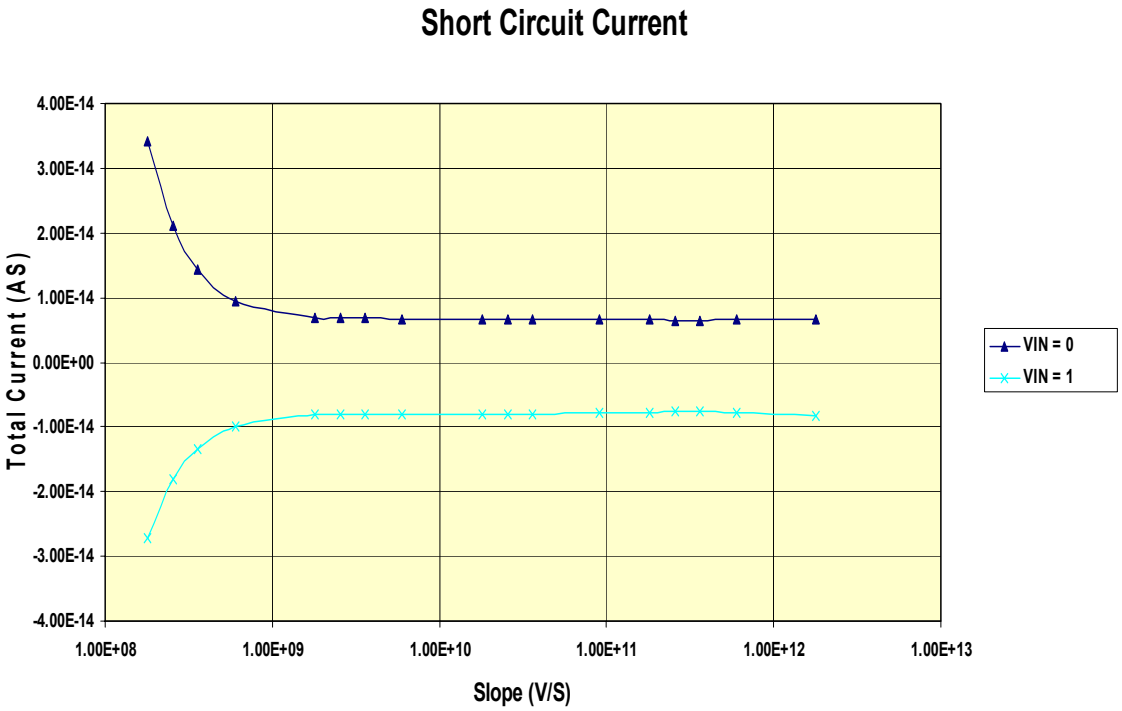


Figure 30: Short Circuit Current for Slope Variation

5.4.3. Output Voltage

The NMOS transistor is off, and the PMOS transistor is in the linear region. Part of the charge from the input which was injected through gate to drain coupling capacitance causes an overshoot at the early part of the output voltage. During the overshoot the PMOS device operates in a reversed linear

mode. Thus the PMOS device initially helps to discharge the load capacitance toward the supply voltage.

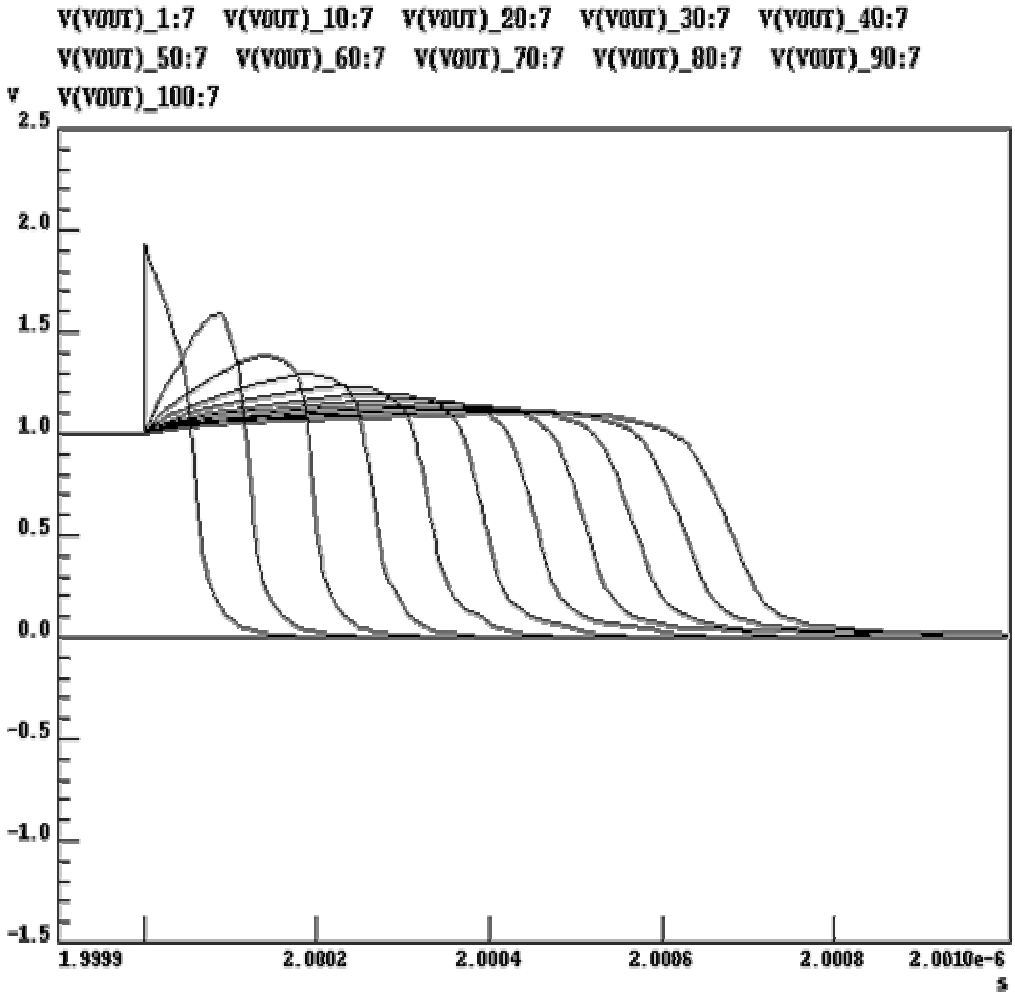


Figure 31: Output Voltage for Slope Variation

5.5. Effect of Load Variation

5.5.1. Switching Current

As load capacitance increases switching current increases exponentially. Because larger the capacitance more the time constant and large the amount of current required for charging it.

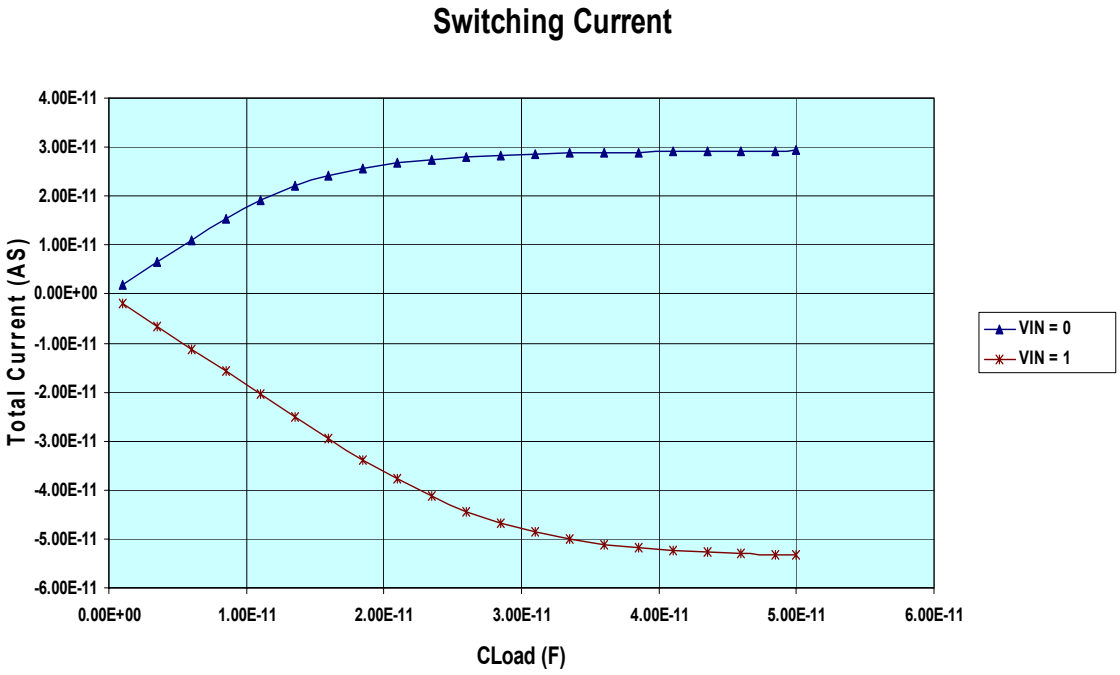


Figure 32: Switching Current for Load Variation

5.5.2. Short Circuit Current

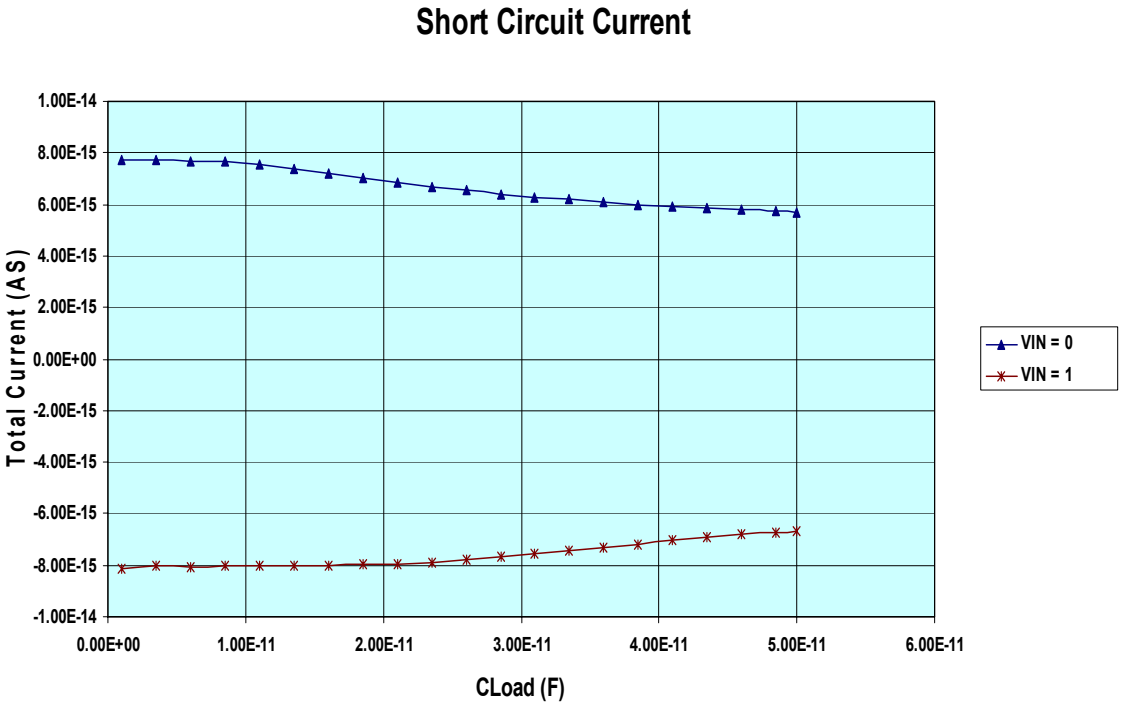


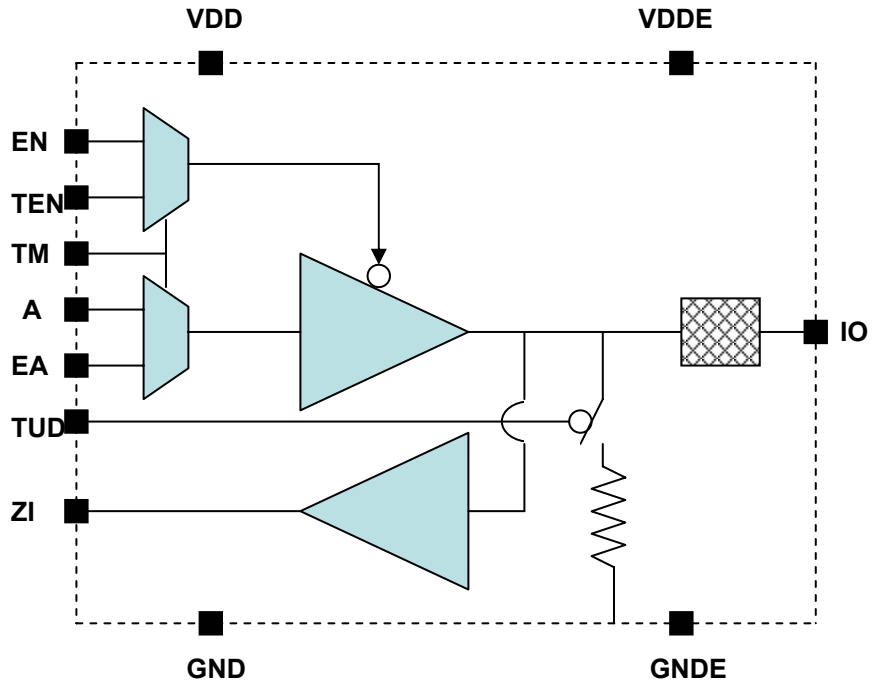
Figure 33: Short Circuit Current for Load Variation

As load capacitance increases short circuit current decrease because time constant will increase and the effective time for which both transistor will be on decreases because of the large time constant.

CHAPTER:6 LEAKAGE POWER ANALYSIS

6.1. Bidirectional Pad Buffer

It is a CMOS Schmitt Trigger Bidirectional Pad Buffer with 2mA drive capability, with Slew-rate Control and Switchable Pull-Down.



Block Diagram

Figure 34: Block diagram of Bidirectional Pad Buffer

6.1.1. Specifications

Technology: 90nm
Process: Worst Normal Best
IO Supply: 0.9 to 1.26 V (Vdd)
Core Supply: 2.25 to 2.75 V (Vdde)
Temperature: -40 to 150 ^{O}C
O/P Swing: 0-Vdde

6.1.2. Functional Table

A	EN	TA	TEN	TM	TUD	IO	ZI	IO
L	L	-	-	0	1	Z	0	0
H	L	-	-	0	1	Z	1	1
-	H	-	-	0	1	Z	X	Z
-	H	-	-	0	1	L	0	L
-	H	-	-	0	1	H	1	H
-	H	-	-	0	0	Z	0	0
-	-	L	L	1	1	Z	0	0
-	-	H	L	1	1	Z	1	1
-	-	-	H	1	1	Z	X	Z
-	-	-	H	1	1	L	0	L
-	-	-	H	1	1	H	1	H
-	-	-	H	1	0	Z	0	0

Table 2: Functional table of Bidirectional Pad Buffer

6.1.3. Simulation Results

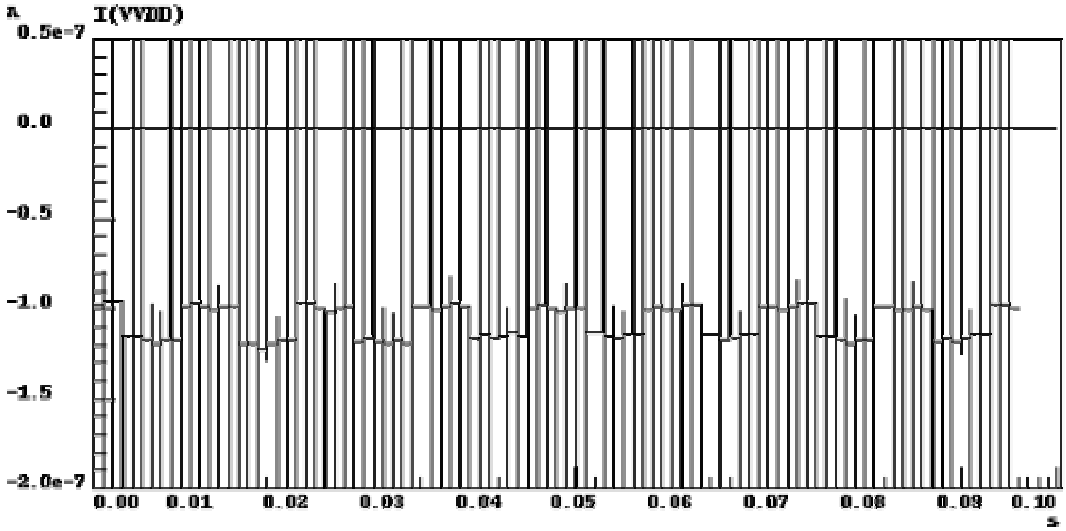
Pin	State A EN TA TEN TM TUD IO	Leakage (A)
A	X X 1 X 1 1 X	1.6095e-09
	1 X X X 0 1 X	1.6087e-09
	X X 0 X 1 1 X	5.7530e-12
EN	X X X 1 1 1 X	1.6095e-09
	X 1 X X 0 1 X	1.6087e-09
	X X X 0 1 1 X	5.7530e-12
TA	X X 1 X 1 1 X	7.6518e-10
	1 X X X 0 1 X	6.5811e-10
	0 X X X 0 1 X	6.5760e-10
TEN	X X X 1 1 1 X	7.6518e-10
	X 1 X X 0 1 X	6.5811e-10
	X 0 X X 0 1 X	6.5760e-10

Pin	State A EN TA TEN TM TUD IO	Leakage (A)
TM	X X X X 1 X X	8.2502e-10
TUD	X X X X X 1 X	1.0449E-09
Vdde	X 1 X X 0 1 1	1.2402e-08
	X 1 X X 0 1 0	1.7202e-08
	X 1 X X 0 1 Z	1.7284e-08
	1 0 X X 0 1 1	1.3327e-08
	1 0 X X 0 1 0	**8.3509e-02**
	1 0 X X 0 1 Z	1.9127e-08
	0 0 X X 0 1 1	1.5072e-08
	0 0 X X 0 1 0	1.7460e-08
	0 0 X X 0 1 Z	1.7680e-08
IO	0 0 X X 0 1 1	**7.5340e-02**

Table 3: Simulation results of Bidirectional Pad Buffer for Leakage

6.1.4. Waveforms

Current through Core Supply Vdd



Current through I/O Supply Vdde

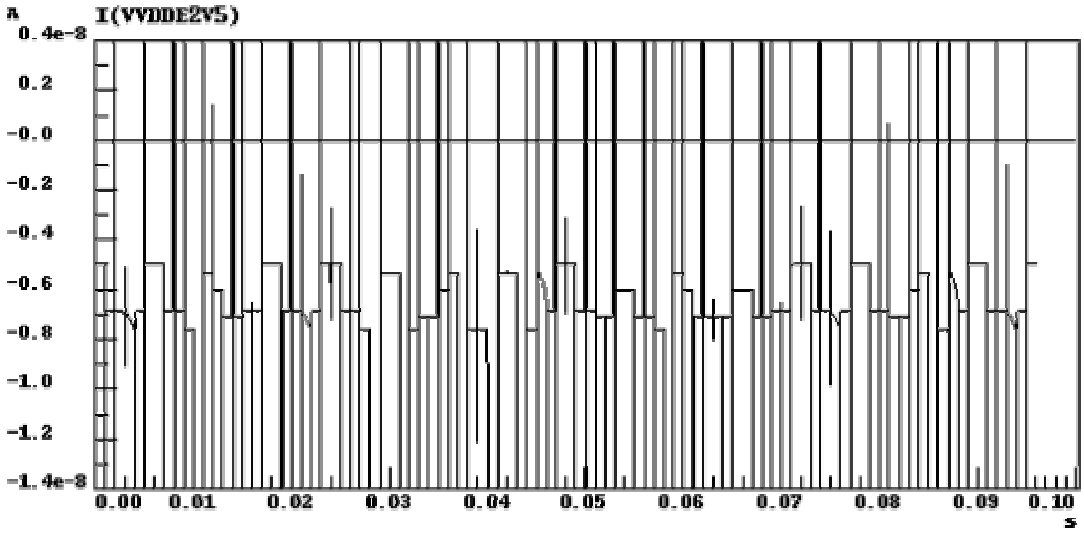


Figure 35: Current waveforms for Bidirectional Pad Buffer

6.1.5. Inference

- Vectors at the inputs have large impact on the leakage.
- When Pin is at Gnd leakage through that Pin Supply is zero. i.e. keeping all the inputs pins at Gnd reduce leakage through pins.
- But, leakage through Vdd is maximum when all pins are at Gnd.
- So, appropriate state should be found where overall leakage is minimum. For Vdd, minimum when 000011000 and maximum when 110001111.
- Similarly, leakage through Vdde is maximum when IO is tristate.
- It can be minimized by pulling IO to Vdde when in standby by TUD. But, now there will be a leakage through TUD Supply and pulling network.
- Pull-up or Pull-down network will increase area at the cost of power.
- For Vdde, minimum when 101111ZXZ and maximum when opposite logic at output.
- Overall leakage is minimum when all 000011000 and maximum during opposite logic at output.

6.2. Differential Output Driver

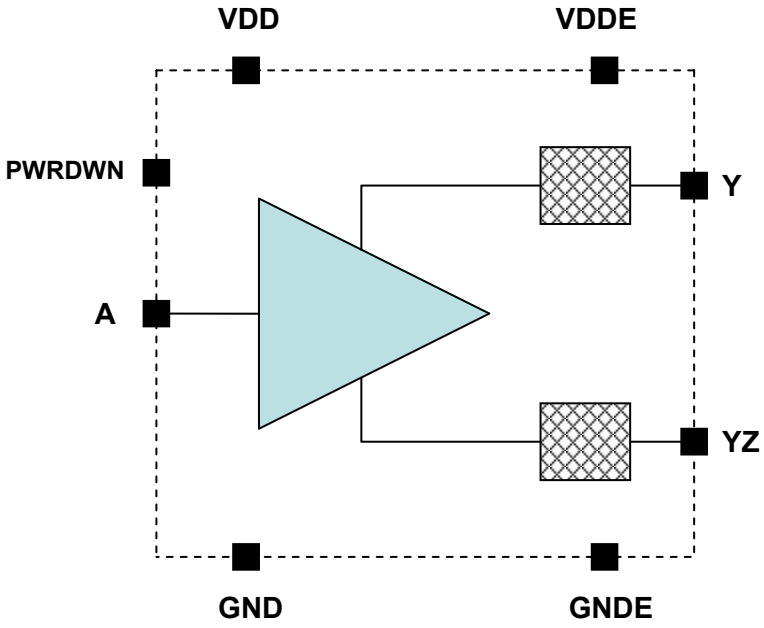


Figure 36: Block diagram of Differential Output Driver

6.2.1. Specifications

Technology: 65nm
Process: Worst Normal Best
IO Supply: 0.9 to 1.3 V (Vdd)
Core Supply: 1.65 to 1.95 V (Vdde)
Temperature: -40 to 150 ^{O}C
O/P Swing: 0.4 to 0.6 Vdde

6.2.2. Functional Table

A	PWRDWN	Y	YZ
L	1	0	1
H	1	1	0
-	0	Z	Z

Table 4: Functional table for Differential Output Driver

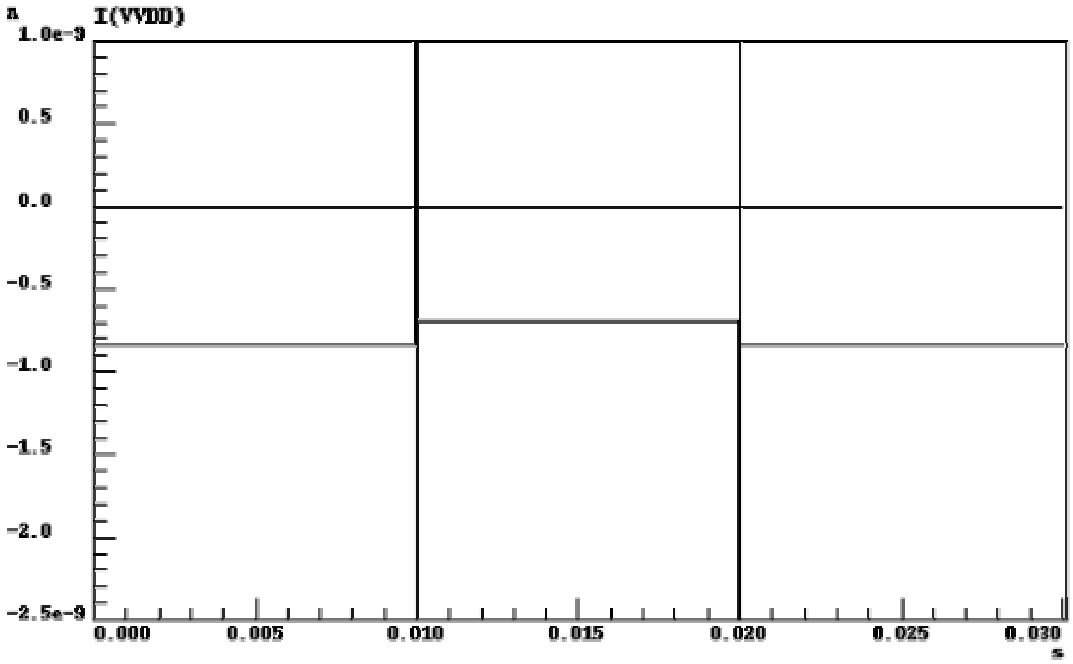
6.2.3. Simulation Results

Condition	Leakage Vdd (A)		Leakage Vdde (A)
	A=1	A=0	
Best, Vdd 1.3 V, Vdde 1.95 V, T 105 ^{O}C	1.4428e-08	1.5043e-08	1.2063e-2
Best, Vdd 1.1 V, Vdde 1.95 V, T -40 ^{O}C	8.4638e-11	1.3066e-10	1.4546e-2
Best, Vdd 1.1 V, Vdde 1.95 V, T 105 ^{O}C	9.2358e-09	9.8388e-09	1.2063e-2
Best, Vdd 1.1 V, Vdde 1.95 V, T 150 ^{O}C	4.3184e-08	4.7500e-08	1.1703e-2
Nom, Vdd 1.0 V, Vdde 1.80 V, T 025 ^{O}C	3.7607e-11	4.8017e-11	7.2977e-3
Worst, Vdd 1.1 V, Vdde 1.65 V, T 105 ^{O}C	3.2550e-10	3.9277e-10	3.6612e-3
Worst, Vdd 0.9 V, Vdde 1.65 V, T 105 ^{O}C	2.1182e-10	2.6063e-10	3.6612e-3
Worst, Vdd 0.9 V, Vdde 1.65 V, T 150 ^{O}C	1.4134e-09	1.7557e-09	3.7407e-3

Condition	Leakage A (A)		Leakage PWRDWN (A)
	A=1	A=0	
Best, Vdd 1.3 V, Vdde 1.95 V, T 105 ^{O}C	6.6318e-11	0	6.6458e-11
Best, Vdd 1.1 V, Vdde 1.95 V, T -40 ^{O}C	2.5085e-11	0	2.5134e-11
Best, Vdd 1.1 V, Vdde 1.95 V, T 105 ^{O}C	2.5999e-11	0	2.6050e-11
Best, Vdd 1.1 V, Vdde 1.95 V, T 150 ^{O}C	2.6329e-11	0	2.6381e-11
Nom, Vdd 1.0 V, Vdde 1.80 V, T 025 ^{O}C	5.3926e-12	0	5.4028e-12
Worst, Vdd 1.1 V, Vdde 1.65 V, T 105 ^{O}C	3.3234e-12	0	3.3302e-12
Worst, Vdd 0.9 V, Vdde 1.65 V, T 105 ^{O}C	1.1138e-12	0	1.1159e-12
Worst, Vdd 0.9 V, Vdde 1.65 V, T 150 ^{O}C	1.1365e-12	0	1.1386e-12

Table 5: Simulation results of Differential Output Driver for Leakage

6.2.4. Waveforms



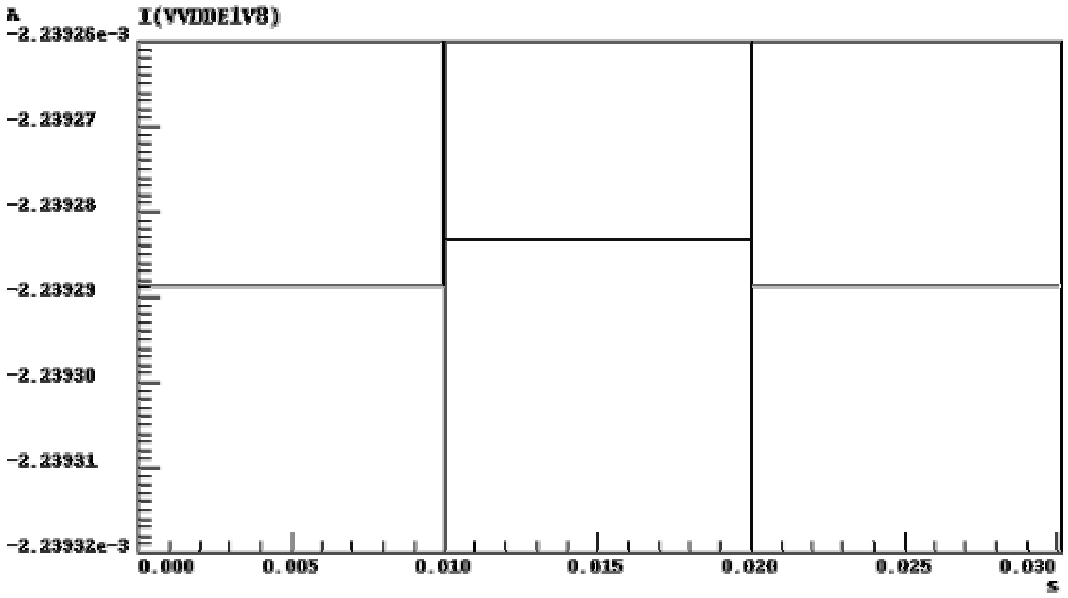


Figure 37: Current waveforms for Differential Output Driver

6.2.5. Inference

- A resistance exists between differential pins Y and YZ.
- Logic is always opposite on this differential pins.
- So a continuous path exists between Vdde and Gnde through resistance.
- Leakage can be decreased by increasing this resistance but this will decrease the speed as swing will increase.

6.3. Bias Cell

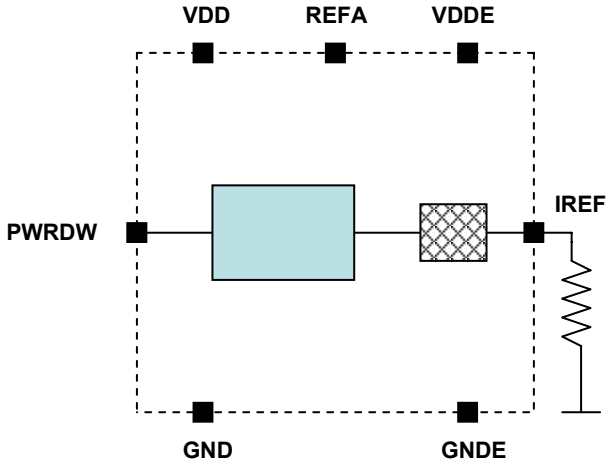


Figure 38: Block Diagram of Bias Cell

6.3.1. Specifications

Technology: 65nm

Process: Worst Normal Best

IO Supply: 0.9 to 1.3 V (Vdd)

Core Supply: 1.65 to 1.95 V (Vdde)

Temperature: -40 to 150 ^{O}C

O/P Swing: 0.4 to 0.6 Vdde

6.3.2. Functional Table

PWRDWN	REFA	IREF
1	Valid Vref	Vdde/2
0	Vdde	0

Table 6: Functional table for Bias Cell

6.3.3. Simulation Results

Condition	Leakage		
	PWRDWN (A)	Vdd (A)	Vdde (A)
Best, Vdd 1.3 V, Vdde 1.95 V, T 105 OC	6.9578e-11	3.6215e-09	3.1027e-04
Best, Vdd 1.1 V, Vdde 1.95 V, T -40 OC	2.6295e-11	1.6160e-11	3.2583e-04
Best, Vdd 1.1 V, Vdde 1.95 V, T 105 OC	2.8397e-11	2.4239e-09	3.1027e-04
Best, Vdd 1.1 V, Vdde 1.95 V, T 150 OC	5.0097e-11	1.2327e-08	2.9720e-04
Nom, Vdd 1.0 V, Vdde 1.80 V, T 025 OC	6.3930e-12	8.5672e-12	1.8440e-04
Worst, Vdd 1.1 V, Vdde 1.65 V, T 105 OC	4.5453e-12	1.0335e-10	1.3231e-04
Worst, Vdd 0.9 V, Vdde 1.65 V, T 105 OC	1.9324e-12	7.0593e-11	1.3231e-04
Worst, Vdd 0.9 V, Vdde 1.65 V, T 150 OC	2.1211e-12	4.8480e-10	3.2583e-04

Table 7: Simulation results of Bias Cell for Leakage

6.3.4. Waveforms

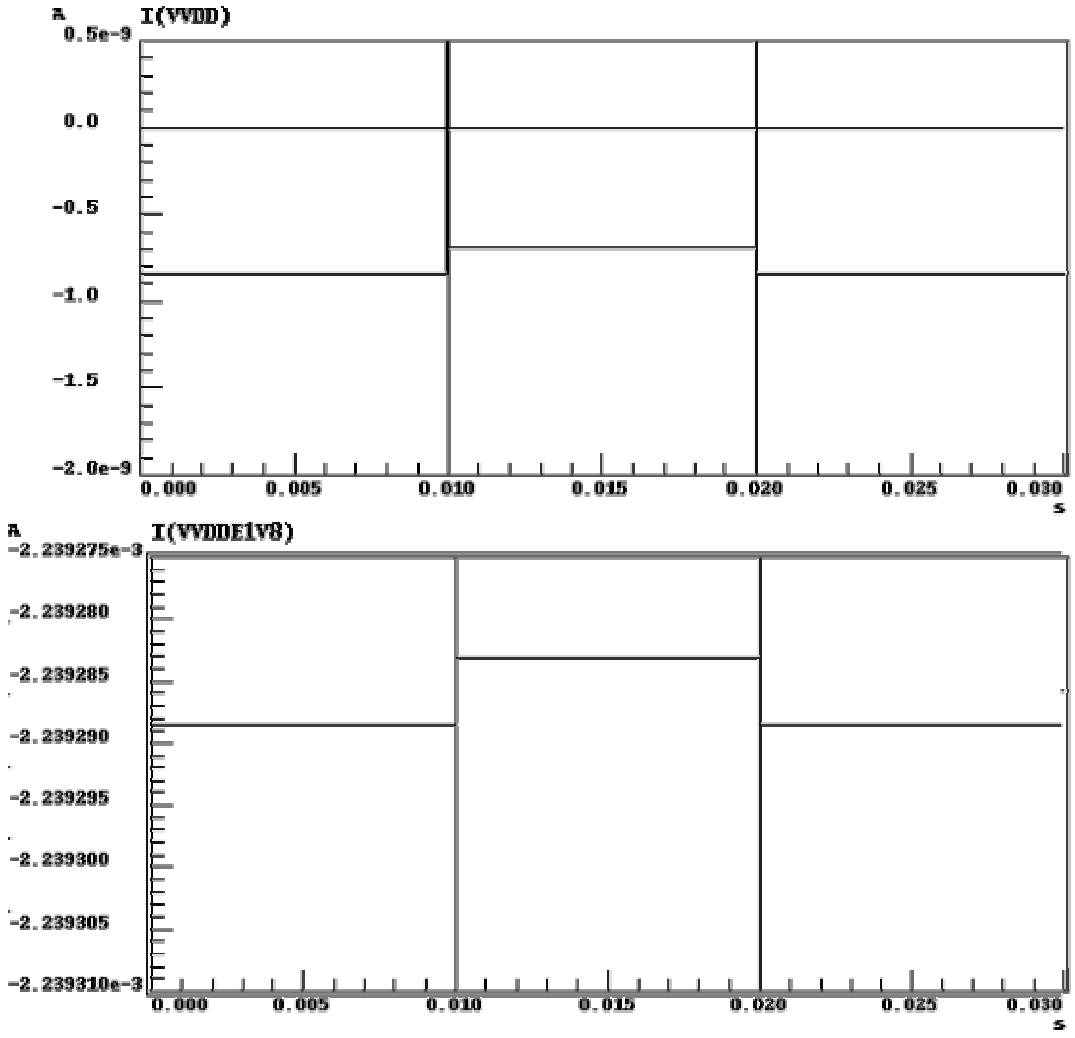


Figure 39: Current waveforms for Bias Cell

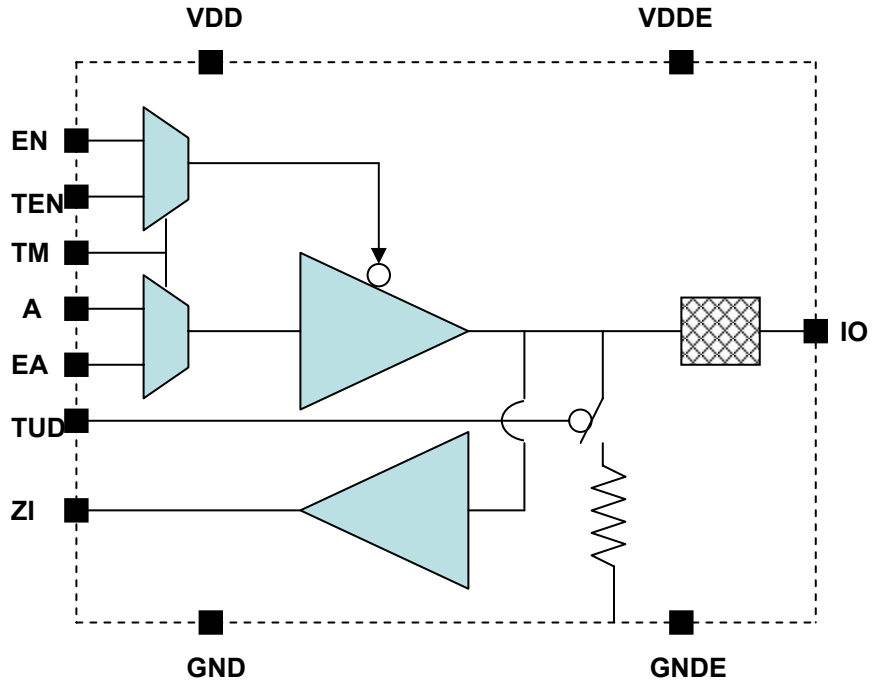
6.3.5. Inference

- Effect of leakage will be more a matter of concern in the bias cell, as it will be also ON.

CHAPTER:7 INTERNAL ENERGY ANALYSIS

7.1. Bidirectional Pad Buffer

It is a CMOS Schmitt Trigger Bidirectional Pad Buffer with 2mA drive capability, with Slew-rate Control and Switchable Pull-Down.



Block Diagram

Figure 40: Block diagram of Bidirectional Pad Buffer

7.1.1. Specifications

Technology: 90nm
Process: Worst Normal Best
IO Supply: 0.9 to 1.26 V (Vdd)
Core Supply: 2.25 to 2.75 V (Vdde)
Temperature: -40 to 150 ^{O}C
O/P Swing: 0-Vdde
Slope: 0.004 - 0.9713 pS/V
Cload: 1 – 50 pF

7.1.2. Functional Table

A	EN	TA	TEN	TM	TUD	IO	ZI	IO
L	L	-	-	0	1	Z	0	0
H	L	-	-	0	1	Z	1	1
-	H	-	-	0	1	Z	X	Z
-	H	-	-	0	1	L	0	L
-	H	-	-	0	1	H	1	H
-	H	-	-	0	0	Z	0	0
-	-	L	L	1	1	Z	0	0
-	-	H	L	1	1	Z	1	1
-	-	-	H	1	1	Z	X	Z
-	-	-	H	1	1	L	0	L
-	-	-	H	1	1	H	1	H
-	-	-	H	1	0	Z	0	0

Table 8: Functional table of Bidirectional Pad Buffer

7.1.3. Simulation Results

Process – Best
Temperature – 125 ^{o}C
Voltage – 1.08 V
Supply – Vdde
Arc – A_R_IO_R

CLoad (pF)	1.0	2.0	4.0	8.0	12.5	25.0	37.5	50.0
Slope (pS/V)	(pW)							
0.004	10.836	10.9305	11.1905	11.6815	12.3503	14.760	17.1387	19.3875
0.076	10.833	10.9185	11.1795	11.6675	12.3913	14.350	17.2087	20.1675
0.3011	10.830	10.9225	11.1385	11.6895	12.3823	14.490	17.3287	19.1575
0.9482	10.824	10.9235	11.1585	11.6795	12.3963	14.870	18.0387	20.0175
0.9713	10.834	10.9235	11.1745	11.6535	12.4703	14.640	17.0287	19.9675

Process – Best
Temperature – 125 ^{o}C
Voltage – 1.08 V
Supply – Vdde
Arc – A_F_IO_F

CLoad (pF)	1.0	2.0	4.0	8.0	12.5	25.0	37.5	50.0
Slope (pS/V)	(pW)							
0.004	8.46732	8.51632	8.62712	8.81962	9.03672	9.57632	10.0795	10.5655
0.076	8.46702	8.51722	8.62762	8.82162	9.03172	9.56542	10.0735	10.5645
0.3011	8.46722	8.51552	8.62662	8.81912	9.03622	9.57772	10.0705	10.5795
0.9482	8.46322	8.51002	8.62222	8.81802	9.02502	9.56142	10.0685	10.5805
0.9713	8.46392	8.51502	8.62072	8.81652	9.02962	9.56962	10.0735	10.5615

Table 9: Simulation results for Bidirectional Pad Buffer for Internal Energy

7.1.4. Waveforms

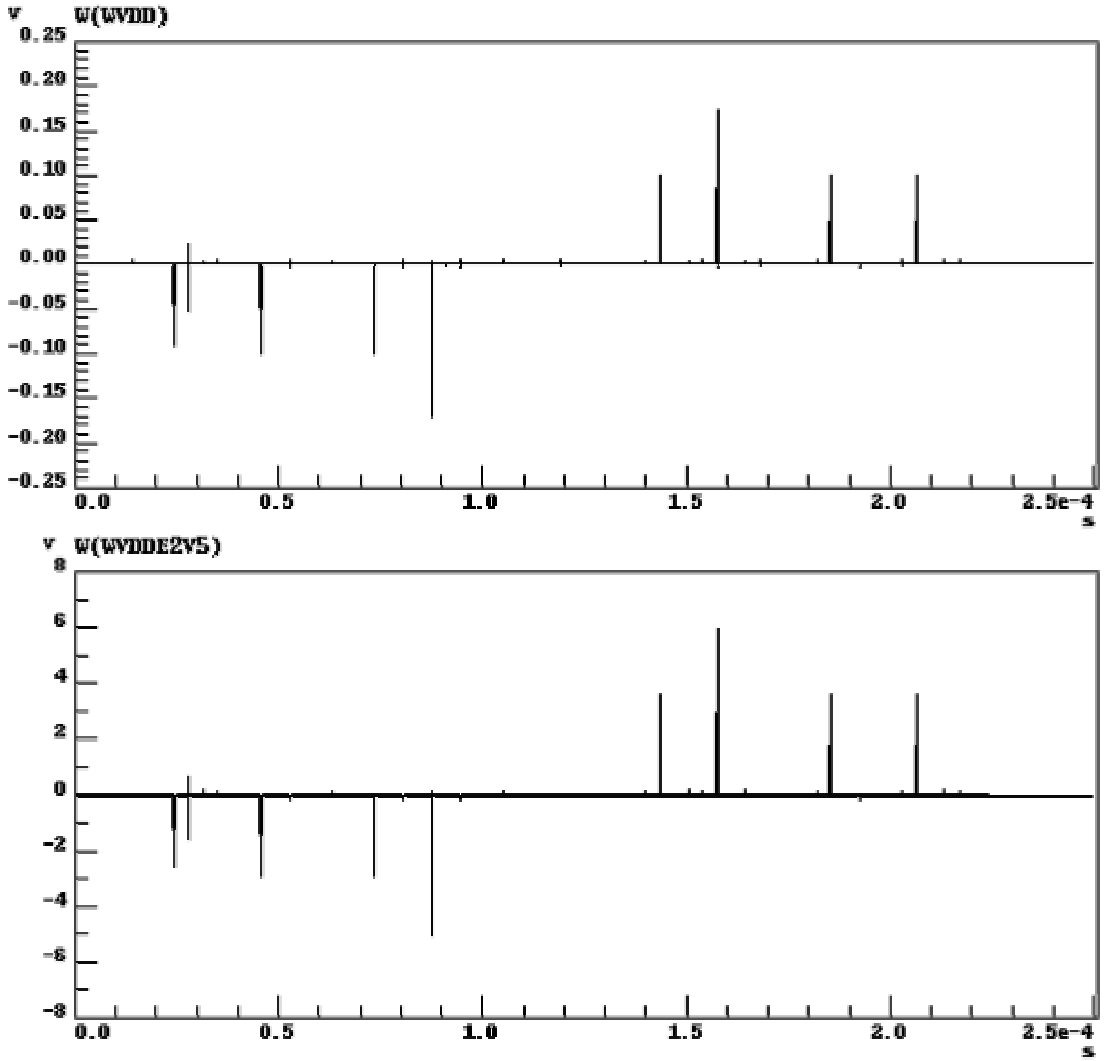


Figure 41: Energy waveforms for Bidirectional Pad Buffer

7.1.5. Inference

- Out of two supplies I/O supply plays a major role in power loss as it is in interaction with environment outside the chip where voltage is higher.
- Other than Temperature and Voltage two other parameter affecting the internal power consumption are Slope and Load.
- As slope increase short circuit current increases, resulting in the increase in internal power.
- As load increase shortcircuit current decrease some what but switching current increase, resulting in the increase in internal power.
- Load is having major impact than slope.
- Also, one can see that internal energy consumption over a cycle is positive.
- For fixed internal power consumption, one can see that there is a trade-off between driving capability and operating frequency.

7.2. Differential Output Driver

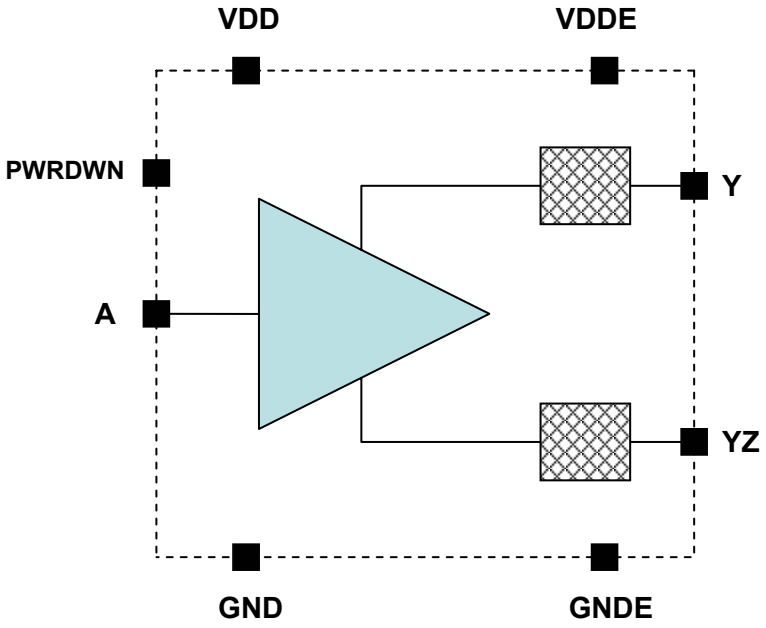


Figure 42: Block diagram of Differential Output Driver

7.2.1. Specifications

Technology: 65nm

Process: Worst Normal Best

IO Supply: 0.9 to 1.3 V (Vdd)

Core Supply: 1.65 to 1.95 V (Vdde)

Temperature: -40 to 150 ^{O}C

O/P Swing: 0.4 to 0.6 Vdde

Slope: 0.004 - 0.9713 pS/V

Cload: 1 – 50 pF

7.2.2. Functional Table

A	PWRDWN	Y	YZ
L	1	0	1
H	1	1	0
-	0	Z	Z

Table 10: Functional table for Differential Output Driver

7.2.3. Simulation Results

Process – Normal
Temperature – 25 ^{o}C
Voltage – 1.2 V
Supply – Vdde
Arc – A_R_IO_R

CLoad (pF)	1	2	3	5	10
Slope (pS/V)	(pW)				
0.005	1.645	1.645	1.645	1.655	1.665
0.12	1.645	1.645	1.645	1.655	1.665
0.24	1.645	1.645	1.645	1.655	1.665
0.47	1.645	1.645	1.645	1.655	1.665

Process – Normal
Temperature – 25 ^{o}C
Voltage – 1.2 V
Supply – Vdde
Arc – A_F_IO_F

CLoad (pF)	**1**	**2**	**3**	**5**	**10**
Slope (pS/V)	**(pW)**				
0.005	1.625	1.625	1.625	1.625	1.635
0.12	1.625	1.625	1.625	1.625	1.625
0.24	1.625	1.625	1.625	1.625	1.635
0.47	1.635	1.625	1.625	1.635	1.635

Table 11: Simulation results of Differential Output Driver for Internal Energy

7.2.4. Waveforms

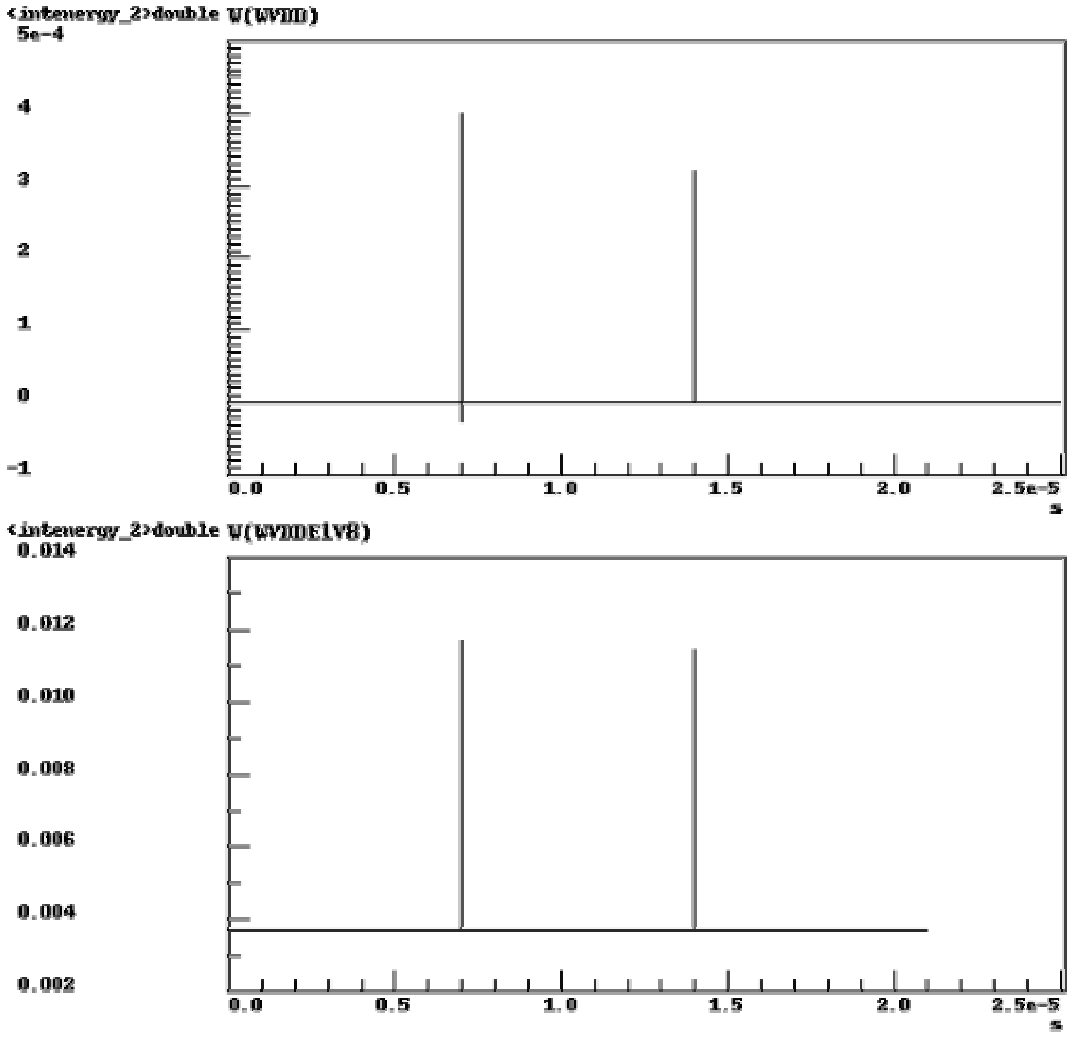


Figure 43: Energy waveforms for Differential Output Driver

7.2.5. Inference

- Logic is always opposite on this differential pins
- Because of this, there will be one capacitor at each output terminal. One capacitor is charging and other is discharging during a transition. So, the internal power consumption will be almost double.

CONCLUSION

With increase in voltage, gate leakage decreases exponentially, base leakage increase, channel leakage increases exponentially, total switching current and total short-circuit current have almost linear variation.

With increase in temperature, gate and channel leakage increases exponentially, base leakage remains constant until threshold is reached then it increases, total switching current decrease while total short-circuit current remains almost constant.

With increase in slope, total switching current remains almost constant while total short-circuit current remains follows inverse function.

With increase in load, total switching current increases exponentially while total short-circuit current decreases.

With these simulations, we conclude that for given temperature and voltage conditions, leakage for a given cell mainly depends on the sub-threshold current, which is merely constant. Varying factor of the leakage is gate current which depends on the applied input. Selecting proper input configuration can minimize the standby leakage to a good extent.

As internal energy depends on the transitions, it increases with increase in slope due to increased time for short circuit current that flows from Vdd to Ground and with load due to larger driving current required for charging the Load. Other than this Voltage and temperature also plays an important role in internal energy consumption as we have discussed.

FUTURE WORK

Work can be carried out further on the following issues.

Leakage Power

- Effect of Process Parameters such as oxide thickness, type of oxide, doping concentration, etc.
- Comparison of their impact with the impact of Temperature and Voltage.

Internal Energy

- Effect of Process Parameters such as oxide thickness, type of oxide, doping concentration, etc.
- Comparison of their impact with the impact of Temperature, Voltage, Slope and Load.

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