"DESIGN & SIMULATION OF WIDE SWING FOLDED CASCODE OTA USING 0.35 µm CMOS TECHNOLOGY"

A Major Project Report

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For the Degree of

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IN

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(VLSI DESIGN)

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CERTIFICATE

This is to certify that the major Project Report entitled **"Design & Simulation of Wide Swing Folded Cascode OTA using 0.35 um CMOS Technology"** submitted by **Mr. Kehul A. Shah (Roll No. 06 MEC 007),** towards the partial fulfillment of the requirements for Semester III-IV of **Master of Technology (Electronics & Communication Engineering)** in the field of **VLSI Design** of **Nirma University of Science & Technology** is the record of work carried out by him under our supervision and guidance. The work submitted has in my opinion reached a level required for being accepted for examination. The results embodied in this dissertation-Project work to the best of our knowledge have not been submitted to any other University or Institute for award of any degree or diploma.

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ABSTRACT

We are witnessing the dominance of microelectronics (VLSI) in every sphere of "Electronics and Communications" forming the backbone of modern electronics industry in Mobile communications, Computers, state-of-art processors etc. Designing high performance analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages.

The main bottleneck in an analog circuit is the operational – amplifier. At large supply voltages, there is a trade – off among **Speed, Power and Gain**. The main characteristics under consideration are **High gain, high PSRR; Low offset voltage, high output swing.** Performance of any circuit depends upon these characteristics. At reduced supply voltages, output swing becomes an important parameter. Due to the consistent efforts the Op-amp architectures have evolved **Telescopic amplifier** involving **less power consumption, low noise,** but **Telescopic amplifier has the inherent disadvantage of low output Swing.** Cascode circuits are widely used in circuit design at places where high gain and high output impedances are required.

"Folded Cascode Operational Tranconductance Amplifier" topology is done in order to optimize MOS transistor sizing. Cascode circuits are widely used in circuit design at places where **High gain and High output impedances** are required. Amongst all the topologies of OTA, Folded Cascode OTA is chosen as it allows shorting of input and output terminals with **negligible swing limitations**. The design of folded cascode OTA, which works for RF application.

"Wide-swing Folded Cascode OTA" which extends the input CMR beyond the power supply rails by combining both the NMOS and PMOS input pairs differential amplifiers.

Filters are the indispensable parts of any communication systems. There are various methods to design a filter depending upon the specifications and the application. Filter design using OTA is the most common method.

Programmable high-frequency active filters can be achieved by incorporating the operational Transconductance Amplifier-Capacitor filters (OTA-C). OTA-C filters also have simple structures, and can operate up to several hundreds of MHz. Also the OTA-C filters become very **Power hungry at GHz** range. OTA-C filter has been designed by replacing all the passive components in a passive network with an active device**. "Wide Swing Folded cascode OTA"** is selected as it suits best. **Programmable high-frequency active filters** can be achieved by incorporating the operational Transconductance Amplifier-Capacitor filters (OTA-C).

All Simulation results are performed using **SPICE software and BSIM3V3 model for CMOS 0.35µm process**.

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Chapter: 1

INTRODUCTION TO OTA

1.1 The Operational Transconductance Amplifier

The schematic symbol and equivalent circuit model for an Operational Transconductance Amplifier (OTA) are shown in Figure 1.1(a), (b) respectively.

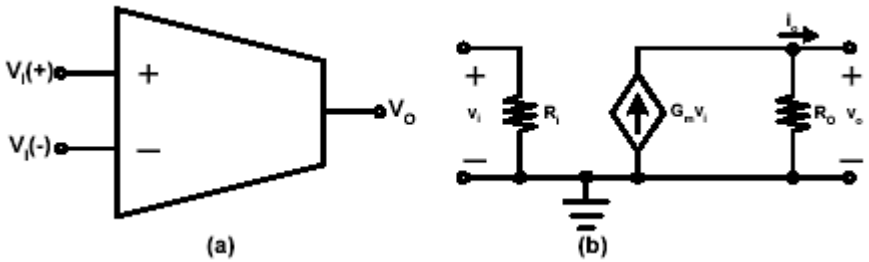


Fig: 1.1 OTA Symbol and Equivalent ckt

The OTA converts an input voltage to an output current relative to a transconductance gain parameter Gm=io/vi. Ideally the input and output resistances are infinite (Ri=Ro=α.) such that $i_i=i_{R0}=0$ and the output current is absorbed solely by the load. The conventional OTA is classified as a class An amplifier and is capable of generating maximum output currents equal to the bias current applied. The equivalent circuit model indicates the transconductance amplifier generates an output current (io) proportional to an input voltage (*vi*) based on the transconductance gain *Gm*. The open circuit voltage gain of the conventional OTA model in Figure 1.1 (b) is given by A=GmRo.

1.2 OTA Vs OP-AMP

- OTA is essentially an OP-AMP without an output buffer.
- An Operational Amplifier has an output buffer so that it is able to drive resistive loads.
- An OTA without output buffer can drive only capacitive loads
- OTA is an amplifier where all nodes except I/O are low Impedance nodes.
- Hence the Two stage OP-AMP configuration minus buffer is not an OTA
- As the name suggest, OTA is not Voltage gain, but is is Transconductance

1.3 CONVENTIONAL TRANSCONDUCTANCE AMPLIFIER

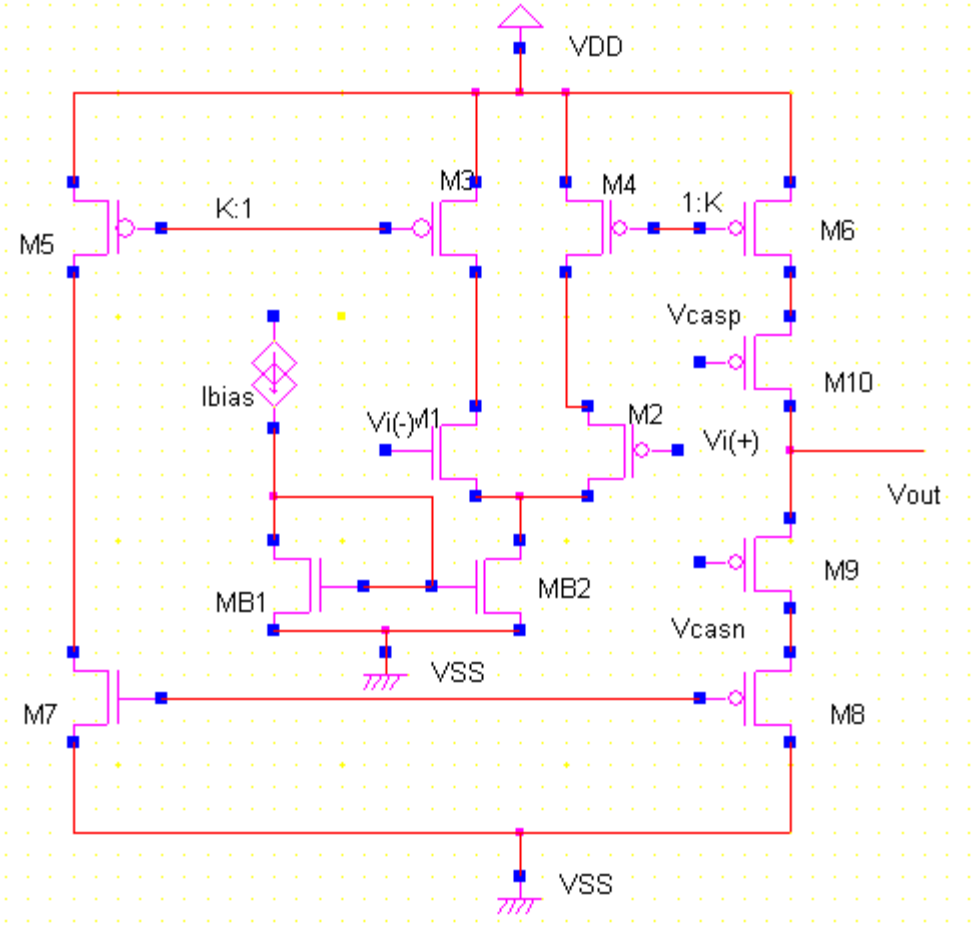


Fig: 1.2 CONVENTIONAL ONE-STAGE TRANSCONDUCTANCE AMPLIFIER

The OTA (Fig: 1.2) employs a differential input pair and three current mirrors. The differential input pair is comprised of transistors M1, 2. The differential pair is biased by MB1, 2. Mirrors formed by M3, 5 and M4, 6 reflect currents generated in the differential pair to the output shell. The current generated by the mirror of M3, 5 is then reflected to the output via the mirror formed by M7, 8. The mirror gain factor, *K*, indicates the gain in mirrors formed by M3, 5 and M4, 6 with the following relations: $\beta_5=K\beta_3$, $\beta_6=K\beta_4$ where $\beta=KP/2(W/L)$. In the following analysis, it will be shown that an increase in *K* will increase the slew rate and gain bandwidth of the conventional OTA at the cost of increased area/static power dissipation and a decrease in phase margin. Cascoding transistors M9, 10 are biased by V_{casn}/V_{casp} and provide increased gain via increased (cascoded) output resistance.

1.3.1 Operation

The conventional OTA (Figure 1.2) uses a differential pair in conjunction with three current mirrors to convert an input voltage into an output current. Common mode signals (Vi (+)=Vi (-)) are, ideally, rejected. For a common mode input voltage, the currents are constant and will be: $i_{d1}=i_{d2}=I_{BIAS}/2$ and $i_{out}=0$. A differential input signal will generate an output current proportional to the applied differential voltage based on the transconductance of the differential pair. Although the output stage is a push-pull structure, the conventional OTA is only capable of producing an output current with a maximum amplitude equal to the bias current in the output shell ($K^* I_{BIAS}$). For this reason, the conventional OTA is a referenced as a class A structure capable of producing maximum signal currents equal to that of the bias current applied. Slew rate (SR) is directly proportional to the maximum output current and is defined as the maximum rate of change of the output voltage. For a single stage amplifier, the slew rate is the output current divided by the total load capacitance. The conventional OTA therefore suffers the consequence that high speed requires large bias currents which translates to large static power dissipation. Wireless and battery powered systems require high slew rate and gain bandwidth values with low static power dissipation. These requirements are difficult to achieve with class A structures such as the conventional OTA.

1.4 Characterization Parameters

Several common characterization methods are used to classify the functionality of OTA structures. These measurement techniques will be used to analyze design structure via theoretical calculation, simulation, and experimentation. Here is a brief explanation of commonly considered parameters.

1. Input offset voltage:

An ideal operational amplifier will give an output of 0 V if both of its inputs are shorted together. A real op amp will have a non-zero voltage output even if its inputs are shorted together. This is the effect of its input offset voltage, which is the slight voltage present across its inputs brought about by its non-zero input offset current. In essence, the input voltage offset is also the voltage that needs to be applied across the inputs of an op amp to make its output zero.

2. Open loop gain:

This is the ratio of the op amp's output voltage to its differential input voltage without any external feedback.

3. Common Mode Rejection:

This is the ability of an operational amplifier to cancel out or reject any signals that are common to both inputs, and amplify any signals that are differential between them. Common mode rejection is the logarithmic expression of CMRR.

CMR=201ogCMRR.

CMRR is simply the magnitude of the ratio of the differential gain to the common-mode gain.

4. Gain-Bandwidth product:

For single pole amplifiers this is the product of the op amp's open-loop voltage gain and the frequency at which it was measured.

5. Slew Rate:

This is the maximum rate of change of the op amp's output voltage when the input signals are large.

6. Settling Time:

This is the length of time for the output voltage of an operational amplifier to approach, and remain within, a certain tolerance of its final value. This is usually specified for a fast full-scale input step.

7. Phase Margin:

An op amp will tend to oscillate at a frequency wherein the loop phase shift exceeds -180°, if this frequency is below the closed loop bandwidth. The closed-loop bandwidth of a voltage-feedback op amp circuit is equal to the op amp's bandwidth at unity gain, divided by the circuit's closed loop gain.

The phase margin of an op amp circuit is the amount of additional phase shift at the closed loop bandwidth required to make the circuit unstable (i.e., phase shift + phase margin = -180°). As phase margin approaches zero, the loop phase shift approaches -180° and the op amp circuit approaches instability. Typically, values of phase margin much less than 45° can cause problems such as "peaking" in frequency response, and overshoot or "ringing" in step response. In order to maintain conservative phase margin, the pole generated by capacitive loading should be at least a decade above the circuit's closed loop bandwidth.

8. Output voltage swing:

This is the maximum output voltage that the op amp can deliver without saturation or clipping for a given load and operating supply voltage.

9. Input Common Mode Range (ICMR):

This is the maximum voltage (negative or positive) that can be applied at both inputs of an operational amplifier at the same time, with respect to the ground.

10. Total Power dissipation:

The total DC power supplied to the op amp minus the power delivered by the op amp to its load.

11. Power Supply Rejection Ratio:

PSRR is a measure of an op amp's ability to prevent its output from being affected by noise or ripples at the power supply. It is computed as the ratio of the change in the op amp's output voltage to the change in the power supply voltage (caused by the power supply change). It is often expressed in dB.

12. Input Bias Current:

The average of the currents into the two input terminals with the output at zero volts.

13. Input Offset Current:

The difference between the currents into the two input terminals with the output held at zero.

14. Differential Input Impedance:

The resistance between the inverting and the non-inverting inputs. This value is typically very high.

15. Common-mode Input Impedance:

The impedance between the ground and the input terminals, with the input terminals tied together. This is a large value, of the order of several tens of megohms or more.

16. **Output Impedance:** The output resistance is typically less than 100 Ohms.

17. Average Temperature Coefficient of Input Offset Current:

The ratio of the change in input offset current to the change in free-air or ambient temperature. This is an average value for the specified range.

18. Output offset voltage:

The output-offset voltage is the voltage at the output terminal with respect to ground when both the input terminals are grounded.

19. Output Short-Circuit Current:

The current that flows in the output terminal when the output load resistance external to the amplifier is zero ohms (a short to the common terminal).

Chapter: 2

DIFFERENT TOPOLOGY

2.1 General Idea

The evolution of very large scale integration (VLSI) technology has developed to the point where millions of transistors can be integrated on a single die or " chip" . Integrated circuits once filled the role of subsystem components, partitioned at analog-digital boundaries, they now integrate complete systems on a chip by combining both analog and digital functions.
Complementary Metal-oxide semiconductor (CMOS) technology has been the mainstay in mixed –signal implementations because it provides density and power savings on the digital side, and a good mix of Components for analog design.

In a few years from now CMOS technology will overpower the whole Electronics Industry. Designing High Performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. **The main bottleneck in an analog circuit is the operational – amplifier. At large supply voltages, there is a trade – off among** Speed, Power and Gain**. The main characteristics under consideration are** High gain, high PSRR; Low offset voltage, high output swing. **Performance of any circuit depends upon these characteristics**.

2.2 CMOS OPERATIONAL –AMPLIFIER

It is one of the most versatile and important building blocks in analog circuit design. Based upon the value of their output resistance they are being classified into two categories

1.UNBUFFERED-OPERATIONAL-AMPLIFIER: These are Operational Transconductance Amplifiers (OTA), which have high output resistance.

2. BUFFERED-OPERATIONAL –AMLIFIER*:* These are Voltage Operational Amplifiers, which have low output résistance. Operational - amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer – function is practically independent of the gain of the opamp. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement negative feed –back concept.

2.3 DESIGN OF CMOS OP-AMPS

CMOS op-amps are very similar in architecture to their bipolar counterparts. It has different stages, which are explained below

DIFFERENTIAL TRANSCONDUCTANCE STAGE

(1) It forms input to op-amp.
(2) This stage sometimes provides the differential to single stage conversion.

(3) Normally a good portion of overall gain is provided by this stage, which improves Noise and offset performance.

HIGH GAIN STAGE

(1) It is the second stage of op-amp, which is typically an inverter.
(2) If the differential input stage doesn't perform the differential – to- single –ended conversion then it is accomplished by the second stage inverter.

BUFFER STAGE

(1) If the op-amp must drive a low resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large Signal swing.

BIAS CIRCUITS

(1) Bias circuits are provided to establish the proper operating point for each transistor in quiescent stage

When selecting an optimal Architecture for the operational –amplifier, Several fundamental Issues and tradeoffs are needed to be considered based upon the specific requirements.

2.4 SINGLE STAGE vs. MULTI STAGE

1. Single stage circuits are inherently faster than Multi stage designs due to the presence of fewer poles .
2. Single stage circuits consume less power because of fewer current legs.
3. But it is very difficult for a single stage circuit to meet the requirements for gain and dynamic range under very low supply voltage like that of 3 V or low.

2.5 OTHER TOPOLOGIES

There are several available op-amp architectures. A few popular topologies are discussed below:

2.5.1 TWO STAGE AMPLIFIER

With all the transistors in the output stage of this amplifier placed in the saturation regime, it has a differential output swing of $2V_{sup} - 4V_{ds,sat}$ where V_{sup} = supply voltage V_{ds}, sat is Minimum V_{ds} required to saturate a transistor for a typical V_{ds}, sat of 200mV, the differential swing is about $2V_{sup} - 0.8V$ which is superior to that of most other topologies. It' s non-dominant poles arising from it' s output nodes, is located at (g_{m6}/C_L),

Where g_{m6} = transconductance of transistor M5 or M6 and C_L = load capacitance

Since this pole is determined by an explicit load capacitance, it typically occurs at a relatively low frequency.

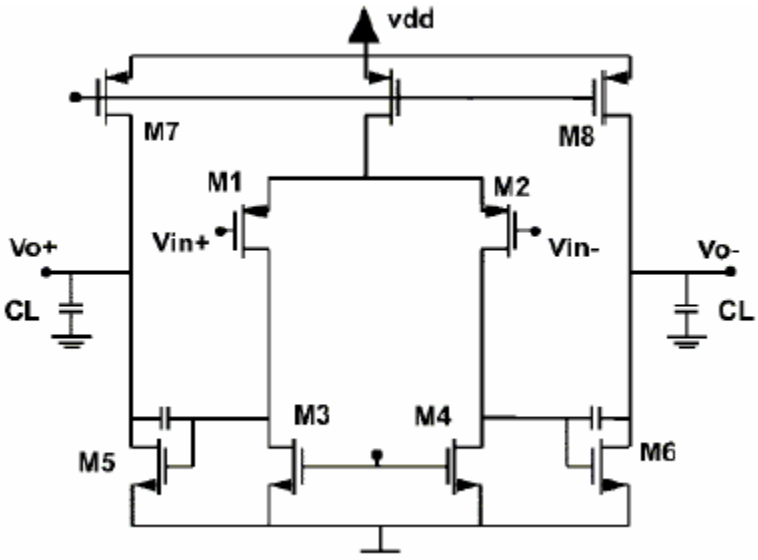


Fig 2.1 Two – Stage amplifier

ADVANTAGES:

1. It has high output voltage swing.

DISADVANTAGES:

1. It has a compromised frequency response.
2. This topology has high power consumption because of two stages in it's design.
3. It has a poor negative Power Supply Rejection at higher frequencies.

This op-amp particularly has applications in Telecommunications area. After initial success, it was noted that this op-amp suffers from a poor PSRR (Power Supply Rejection Ratio)

2.5.2 FOLDED CASCODE AMPLIFIER

Although only V_{ds}, sat is needed to saturate the bottom-most load transistors and the top – most current source transistors in order to allow for process variation, a small safety margin V_{margin} is often added to V_{ds} to ensure saturation. Accounting for these, and the V_{ds}, sat the differential output swing is $2V_{sup}$–8Vds,sat–$4V_{margin}$. With a voltage margin of 100mV, this is estimated to be $2V_{sup}$ – 2V. Although the currents in the output stage can be much smaller than that flowing through the input devices, in practice, the output stage current is picked to be the same or almost the same as the current in the input stage.

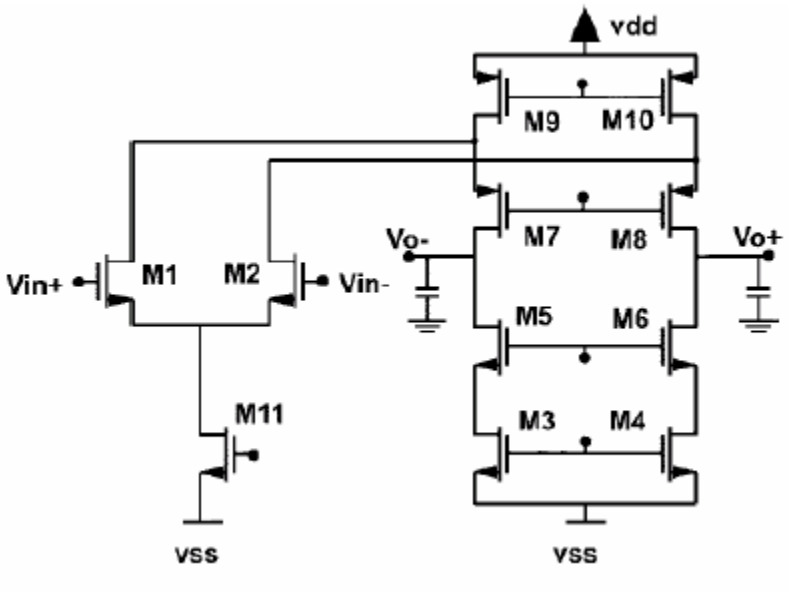


Fig 2.2 Folded Cascode amplifier

ADVANTAGES:

1. This design has corresponding superior frequency response than two – stage operational - amplifiers.
2. It has better high frequency Power Supply Rejection Ratio (PSRR).

The power consumption of this design is approximately the same as that of the two-stage design

DISADVANTAGES:

1. Folded cascode has two extra current legs, and thus for a given settling requirment, they will double the power dissipation.
2. The folded cascode stage also has more devices, which contribute significant input referred thermal noise to the signal.

2.5.3 TELESCOPIC CASCODE AMPLIFIER

Although Telescopic operational - amplifier has smaller swing, which means reduced dynamic range, this is offset somewhat by the lower noise factor. The above reason implies that the Telescopic op-amp is a better candidate for low power, low noise single stage Operational Transconductance Amplifier. The single stage architecture normally suggests low power consumption. Disadvantage of a Telescopic op-amp is severely limited output swing. It is smaller than that of Folded Cascode because the tail transistor directly cuts into output swing from both sides of the operational - amplifier.

The Telescopic operational - amplifier shown in fig 2.3(a), all transistors are biased in saturation region. Transistors M1 - M2, M7 – M8, and tail current source M9 must have at least V_{ds}, sat to offer good common – mode rejection, frequency response and gain. The maximum differential output swing of a telescopic op-amp is $2V_{sup}$ -$10V_{ds,sat}$ - $6V_{margin}$. Under identical conditions, the output swing of this design is limited to $2V_{sup}$- 2.6V. At large supply voltages, the telescopic architecture becomes the natural choice for systems requiring moderate gain for the op-amp. Reducing supply voltages, on the other hand, forces reconsideration in favor of the Folded Cascode, or in the extreme case, the two-stage design.

Although a Telescopic op-amp without the tail current source fig 2.3(b) improves the differential swing by 2Vds,sat + $2V_{margin}$ (600 mV), the common – mode rejection and power-supply rejection of such a circuit is greatly compromised. Moreover, the performance parameters (such as unity gain frequency) of the op-amp with no tail or with

a tail transistor in the linear region is sensitive to input common- mode and supply voltage variation, Which is undesirable in most analog cases.

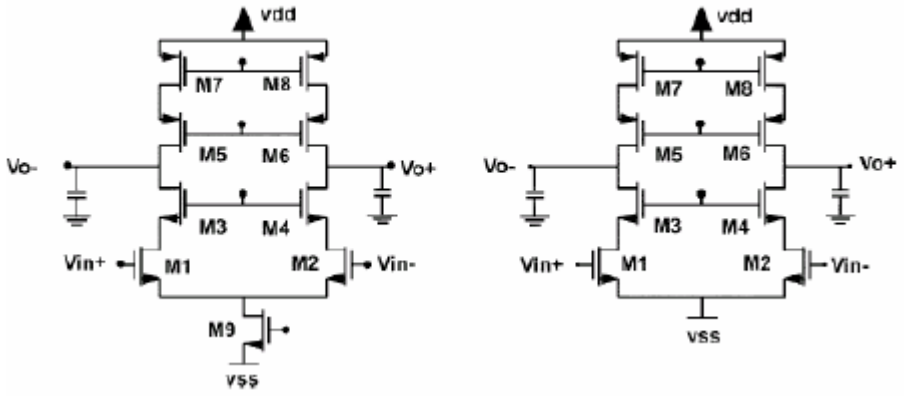


Fig 2.3 (a) Telescopic amplifier **Fig 2.3 (b) No-tail telescopic amplifier**

Other op-amps that have traditionally been employed in high performance applications include the class AB op-amp. This amplifier, however requirements a minimum supply voltage of $2V_t + 4V_{ds,sat} + 2V_{margin}$,

Where V_t = threshold voltage and

For $V_t = 0.8V$, V_{sup} must be greater than 2.6V.

This requirement renders this architecture unsuitable in future Low Voltage Applications. Other drawbacks are degraded frequency response and large opamp noise. The design under consideration combines the low power, high-speed advantage of the Telescopic architecture with the high Swing capability of the Folded Cascode and the Two Stage Design. It achieves its high performance while maintaining High Common mode and supply rejection and Ensuring constant performance parameters

2. 6 COMPARISON OF DIFFERENT CONFIGURATIONS

The table presents a comparison of basic op-amp parameters for different configurations described above.

Configuration	Gain	Output Swing	Speed	Power	Noise
Telescopic Cascode	Medium	Low	Highest	Low	Low
Folded Cascode	Medium	Medium	High	Medium	Medium
Two Stage	High	Highest	Low	Highest	Low
Regulated Cascode	High	Medium	Medium	Highest	Medium

TABLE 2.1: Comparison of various op-amp parameters for different op-amp configurations

2.7 Analog Design Octagons and Low Voltage Issue

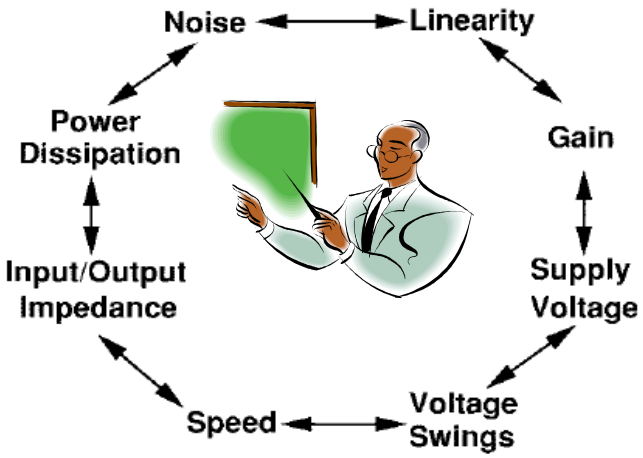


Fig: 2.4 Analog Design Octagon

It is clear that there are numerous performance metrics used for analog circuits, what makes the design process even more challenging is the nonlinear relation between them. For example, when trying to lower the power supply voltage the voltage swing is reduced. If the voltage swing is reduced the SNR is decreased and so on. Thus, determining the relations between the performance metrics is crucial in analog circuit design.

Low Voltage Issues

The whole history of integrated circuits has followed a trend of descending supply voltage. For a long time standard was 5 volts. The migration to a 3.3-volt supply in the mid-'90s started a trend in which almost every new process generation has a lower nominal supply voltage than its predecessor.

Today the 0.25-μmgeneration uses a 2.0-V supply and, according to Semiconductor Industry Association's roadmap, it will be scaled down to 0.9 V by 2010. Table 2.2 shows process parameters for different technology generations. The data, including the effective channel length, supply voltage, oxide thickness, threshold voltage, and threshold voltage matching parameter, is collected from real processes.

L_{min} (μm)	V_{DD} (V)	T_{ox} (A^o)	V_{th} (V)
1.0	**5.0**	**250**	**0.95**
0.8	**5.0**	**200**	**0.85**
0.5	**3.3**	**135**	**0.73**
0.35	**3.3**	**100**	**0.59**
0.18	**1.8**	**50**	**0.42**
0.12	**1.2**	**42**	**0.32**
0.10	**1.2**	**36**	**0.31**
0.07	**0.9**	**30**	**0.30**

Table 2.2 Process Parameter for Different Technology

There are two main drivers for voltage scaling: technology and power. The shrinking technology feature size leads to lower break down voltages and thus supply voltage scaling is mandatory. Due to the ever-increasing integration level, which aims toward a system-on-a-chip (SoC), the power dissipation of a single chip tends to rise, which leads to severe heat problems and increased cooling system costs.

On the other hand, the rapidly growing market for portable battery-operated devices, such as laptops, PDAs, and cellular phones, demands high signal processing capacity together with low power dissipation.

$$p = \frac{1}{2} V_{DD}{}^2 C_L f_{Clk} \alpha$$

----------(2.1)

Where $\mathbf{V_{DD}}$ is the supply voltage, $\mathbf{C_L}$ the load capacitance, $\mathbf{f_{clk}}$ the clock frequency, and α the switching probability. It is obvious that the most effective way to reduce power consumption is to lower the supply voltage. Although it affects the circuit speed, every new technology generation comes with enhanced device characteristics and the possibility of increasing parallelism in the logic, which together more than compensate for the speed loss.

Chapter 3

TELESCOPIC OTA DESIGN

3.1 INTRODUCTION

The gain that can be achieved by a single stage is around 40 dB. Thus, in order to achieve 80 dB or so it is necessary to use a cascade of two stages. However, two stages bring about two poles one close to the other and this requires compensation network, besides increasing the global complexity, reduces the design flexibility. A cascode with cascode load permits us to achieve high gain (around 80 dB) without the disadvantage of having two poles one close to each other. Therefore, the use of cascode based OTA is an interesting solution alternative to the two stages OTA

The simplest version of a single stage OTA is the telescopic architecture, shown in Fig 3.1, the input differential pair injects the signal currents into common gate stages. Then, the circuit achieves the differential to single ended conversion with a cascode current mirror .The transistors are placed one on the top of the other to create a sort of Telescopic composition The small signal resistance at the output node is quite high: it is the parallel connection of two cascode configurations. Such a high resistance benefits the small signal gain without limiting the circuit functionality when we require an OTA function**.**

By inspection of the circuit one finds the low-frequency small signal differential gain is proportional to the square of the product of a transistor transconductance and an output resistance.

$$A_0 = g_{m1}\frac{r_{ds8}g_{m6}r_{ds6}g_{m4}r_{ds4}r_{ds2}}{r_{ds2}r_{s8}r_{ds6}+r_{ds2}g_{m4}r_{ds4}}$$

----------(3.1)

Thus, as expected, the telescopic cascode achieves a gain similar to the one of the two stages architecture. Moreover, by inspection of the circuit, all the nodes, excluding the output, shows a pretty low small signal resistance.

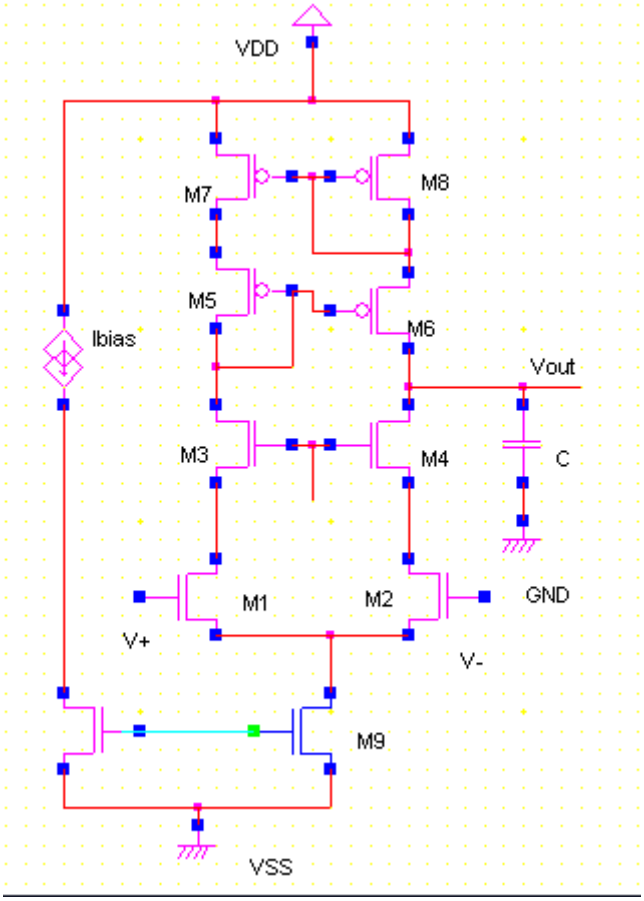


Fig: 3.1 Telescopic OTA

The Telescopic configuration uses only one bias current. It flows through the differential input stage, the common base stage and the differential to single ended converter. Therefore, for a given bias voltage, the power is used at the best .By contrast, we have disadvantages: they concern the limited allowed output dynamic range and the request to have an input common mode voltage pretty close to ground (or Vss).

The Triode limit of M6 establishes the maximum allowed output voltage. By inspection of the circuit it is given by

$$V_{out,\max} = V_{DD} - V_{GS7} - V_{GS5} + V_{GS6} - V_{SAT,P} = V_{DD} - V_{TH,P} - 2V_{SAT,P}$$

----------(3.2)

For typical situations it is 1 V or more below the positive supply voltage.

The lower boundary of the output voltage depends the triode limit of M4 that, in turn depends on $V_{B1.}$

$$V_{out,\min} = V_{B1} - V_{GS4} + V_{SAT,4} = V_{B1} - V_{TH,N}$$

----------(3.3)

Normally the designer broadens the output swing by keeping low VB1. However, the value of VB1 affects the minimum level of the input common mode voltage.

$$V_{in,cm} \le V_{B1} - V_{GS4} - V_{SAT,2} + V_{GS2} = V_{B1-2V_{SAT,N}}$$

----------(3.4)

In turn, the input common mode voltage should allow M9 to be in the saturation region.

$$V_{in,cm} > V_{SAT,9} + V_{GS2}$$

----------(3.5)

Therefore, we can achieve an optimum negative swing ($3V_{sat,n}$ above ground) Keeping the input common mode voltage as low as $V_{sat,9} + V_{GS2}$ approximately equal to $V_{TH,n} + 2V_{sat}$). Assuming a symmetrical output swing around $V_{out,\ max}$ and $V_{out,\ min}$ the output common mode voltage becomes,

$$V_{out,cm} = V_{DD} + V_{B1} - V_{TH,N} - V_{TH,P} - 2V_{SAT,N}$$

----------(3.6)

That for a typical design is a bit higher than V_{B1} . Thus, the output common mode voltage is different (higher) than the input common mode voltage. This, in some applications is a limit: for instance, it is not possible to connect the Telescopic cascode in the unity gain configuration. An interesting feature of this configuration is that it needs only two wires for the Biasing.

3.2 DIFFERENTIAL STAGE

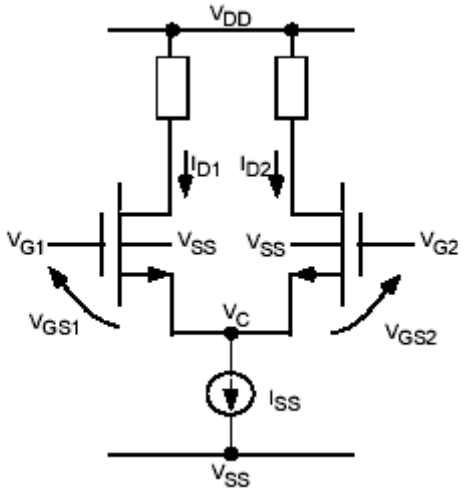


Fig: 3.2 Differential Input pair

A differential pair is widely used as the input stage of the op-amplifier. Fig 3.2 shows its CMOS configuration. It is made of two transistors with their source in common, fed by current source. The transistors may either be n-channel (as shown in Figure) or p-channel, and they are matched to each other. If the two transistors are in saturation region, we can write

$$I_1 = \frac{\mu C_{ox}}{2}\left\{\frac{W}{L}\right\}_1 (V_{gs1} - V_{th})^2$$

$$I_1 = \frac{\mu C_{ox}}{2}\left\{\frac{W}{L}\right\}_2 (V_{gs1} - V_{th})^2$$

----------(3.7)

where (W/L)1 and (W/L)2 are exactly equal, the transistors being matched. Moreover, in the above equations the output conductance has been neglected.

The input signals can be expressed as:

$$V_{GS1} = V_{GS0} + \frac{V_{in}}{2}$$

$$V_{GS1} = V_{GS0} - \frac{V_{in}}{2}$$

----------(3.8)

Where VGS0 is the common mode component and Vin is a differential signal. Since the bias current can be expressed as:

$$I_{ss} = \mu C_{ox} \left\{ \frac{W}{L} \right\}_{9,10} (V_{gs1} - V_{Th})^2$$

----------(3.9)

Therefore, in the differential stage, like in the case of the inverter with active load, the transconductance gain increases with the square root of the bias current.

3.3 High Compliance Current Mirror

The current mismatch inherent to the modified cascode configurations and the additional circuit complexity can be avoided by using the high compliance scheme, shown in Fig.3.3 By comparing the given circuit with the usual cascode current mirror.

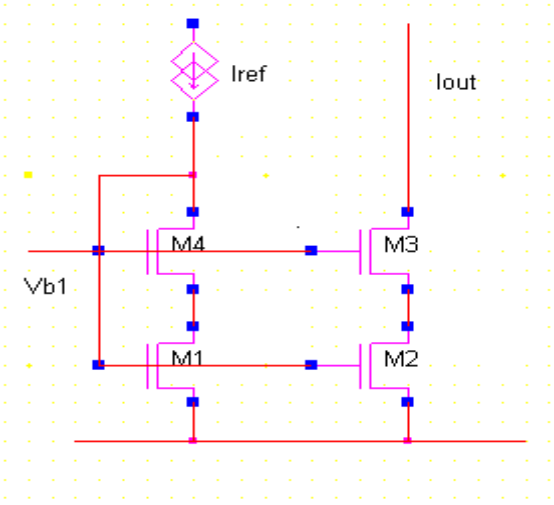


Fig: 3.3 High Compliance current Mirror

There is diode connection of transistor M1 incorporates transistor M4.Therefore, the drain-to –source voltage of M1 is no longer equal to its gate to-source voltage. Instead the value of V_{DS1} and that of V_{DS2} are controlled by the gate of transistors M4 and M3 respectively. The matching between these two elements ensures identical voltage at the drains of M1 and M2, thus leading to a systematic current matching.

The gates of M3 and M4 should be biased by a voltage that keeps both M1 and M2 in saturation and which, at the same time, should avoid M4 going into triode region. Therefore,

$$V_{bias} - V_{TH,4} - V_{SAT,4} > V_{SAT,1}$$

$$V_{bias} - V_{ds1} - V_{TH,4} < V_{TH,1} + V_{SAT,1} - V_{ds,1}$$

----------(3.10)

that requires keeping V_{bias} between one threshold plus two saturations and two thresholds plus one saturation. This condition can be achieved because V_{Th} is normally higher than V_{sat}. The designed value of V_{bias} causes V_{GS1} to split between V_{DS1} and V_{DS2}.

3.4 DESIGN PROCEDURE

DESIGN STEPS

STEP1: The first step of the design gives the estimation of the bias current. Assuming the GBW established by the dominant node, we have

$$2\pi f_T = \frac{2I_{ss}}{(V_{GS} - V_{TH})C_L}$$

----------(3.11)

Where Iss is the tail current.

STEP 2: Design Tail transistor M9 and calculate W and L of this transistor by using the transistor in saturation .The equation used is

$$I_{ss} = \mu C_{ox} \left\{ \frac{W}{L} \right\}_{9,10} (V_{gs1} - V_{Th})^2$$

----------(3.12)

STEP 3: Calculate the bias VB2 of transistor M9 using the equation

$$V_{B2} = V_{GS9} - V_{TH}$$

----------(3.13)

STEP 4: Design the differential pair of the circuit, by assuming both of them to be working in saturation mode. Their aspect ratios could be calculated using bias current Iss. The equation used is

$$I_{SS} = \mu C_{ox} \left\{ \frac{W}{L} \right\}_1 (V_{gs} - V_{TH})^2$$

---------(3.14)

STEP 5: Calculate the common mode voltage that allows M_9 to be in saturation

$$V_{in,cm} >= V_{SAT,9} + V_{GS1}$$

----------(3.15)

STEP 6: Design the High Compliance Current mirror and calculate the Bias voltage that is applied to both the gates by the following equation.

$$V_{B1} - V_2 - V_{TH,n} = V_{SAT,3}$$

----------(3.16)

Where V_{B1} is the bias voltage that is applied to High Compliance current mirror, V2 is the voltage at node 2 and $V_{Th,n}$ is the threshold voltage. The aspect ratios of transistors M3 and M4 can be calculated by assuming both the transistors in saturation and both are matching. The current equation is

$$I_{SS} = \mu C_{ox} \left\{ \frac{W}{L} \right\}_{3,4} (V_{gs} - V_{TH})^2$$

---------(3.17)

Where

$$V_{GS} = V_{B1} - V_{SAT,2} - V_{TH,N}$$

----------(3.18)

STEP 7: Design the Cascode Current Mirror stage where there are four PMOS transistors, which are identical, and the current passing through them is same as the drain and gate are tied to each other. They all are in saturation mode.

The current flowing is same that was in High Compliance Current Mirror stage. The aspect ratios can be calculated by the following current equation

$$I_{SS} = \mu C_{ox} \left\{ \frac{W}{L} \right\}_{5,6,7,8} (V_{gs} - V_{TH})^2$$

----------(3.19)

Where

$$V_{GS} = V_{DD} - 3V_{Th,P}$$

----------(3.20)

3.5 Specifications

Specifications	Value
A_V (dB)	90
F_T (MHz)	250
C_L (pf)	0.1
V_{DD}, V_{SS}	+2V, -2V
Phase Margin	50deg
Channel Length	0.35

Table 3.1 Specifications for Telescopic OTA

Based on above specification and design procedure calculated Aspect Ratio for transistors are as under

Transistor	W/L in μm
M1, M2	226/0.35
M3, M4	292/0.35
M5, M6, M7, M8	352/0.35
M9, M10	177/0.35

TABLE 3.2 CALCULATED ASPECT RATIO FOR TELESCOPIC OTA

The designed **Telescopic OTA** was biased at 2V power supply voltage using **CMOS technology of 0.35 µm of AMS with the BSIM3V3 (Level 49 Parameter) MOSFET model.**

3.6 Simulation Results of Telescopic OTA

3.6.1 AC Analysis

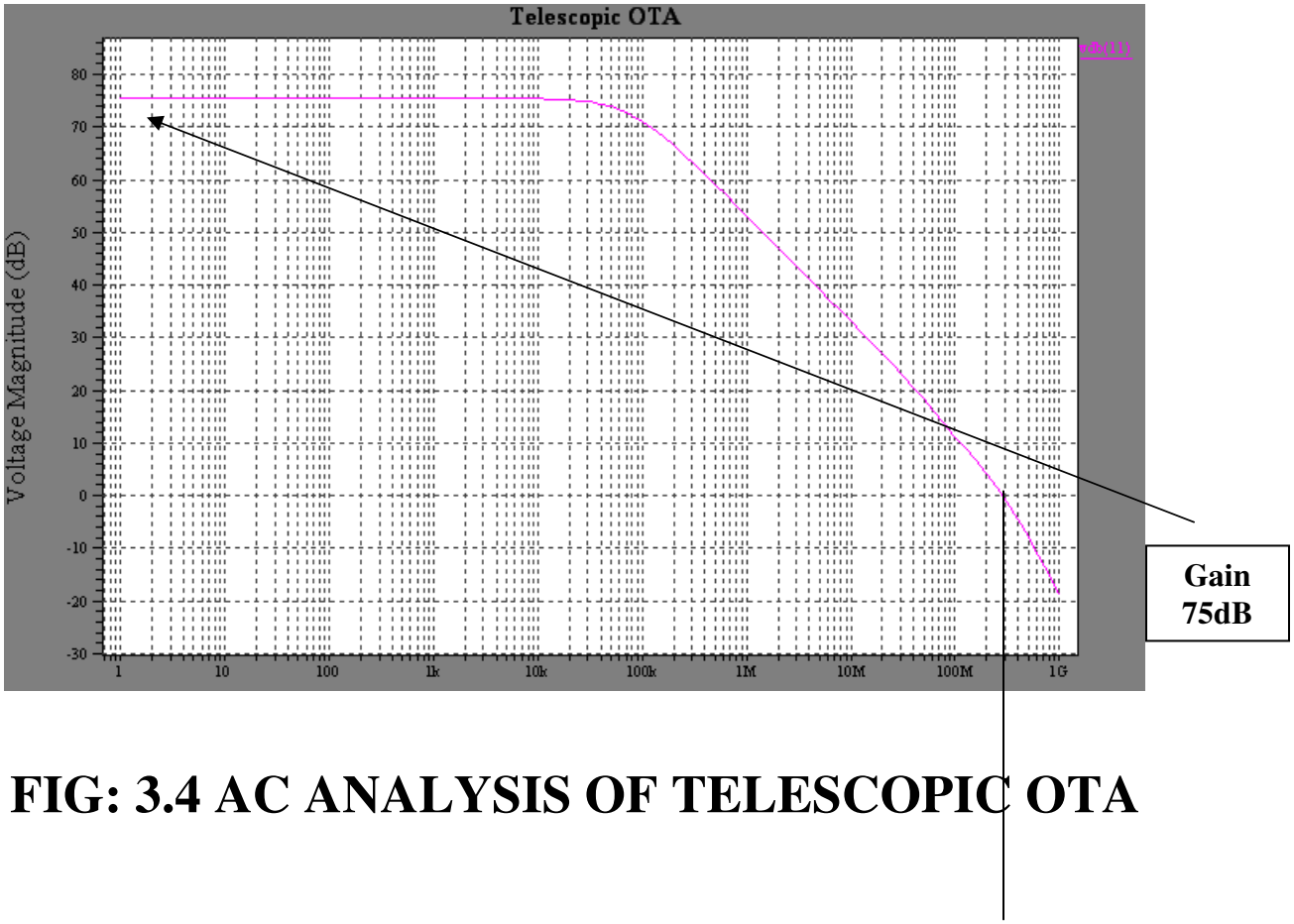


FIG: 3.4 AC ANALYSIS OF TELESCOPIC OTA

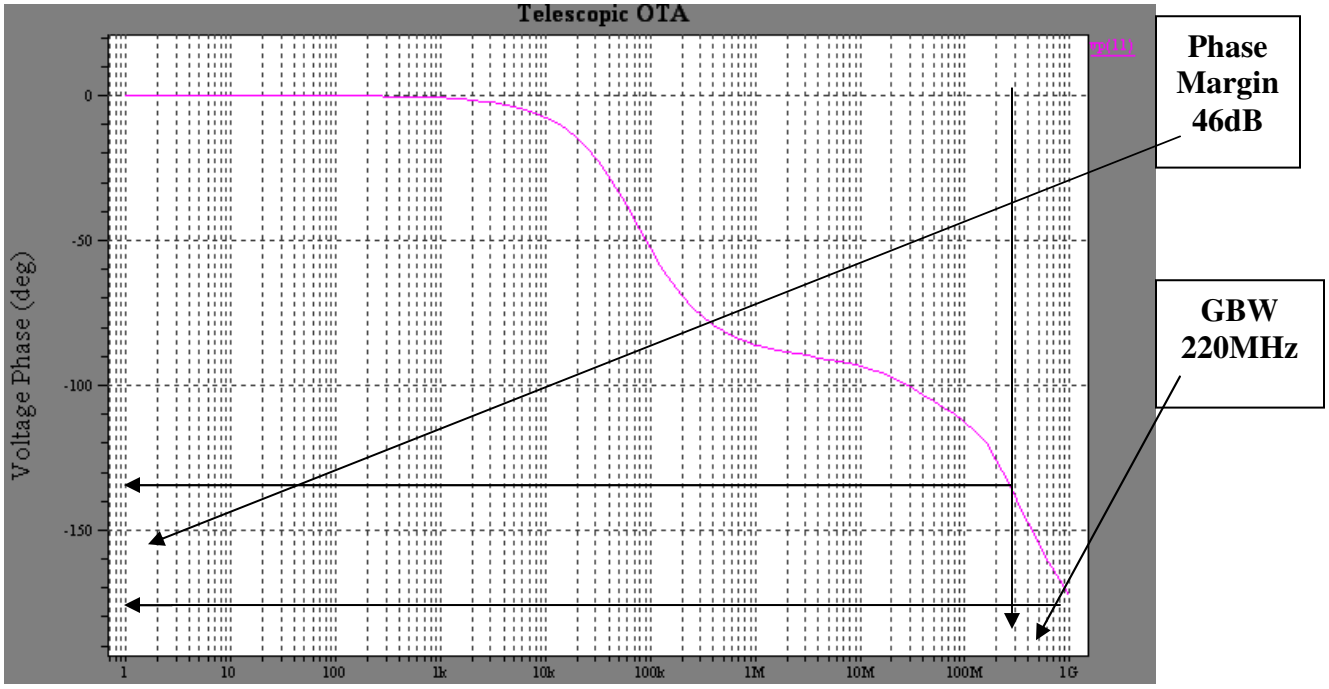


FIG:3.5 PHASE MARGIN AND GAIN BANDWIDTH PRODUCT

3.6.2 Input/Output Swing and Offset Measurement

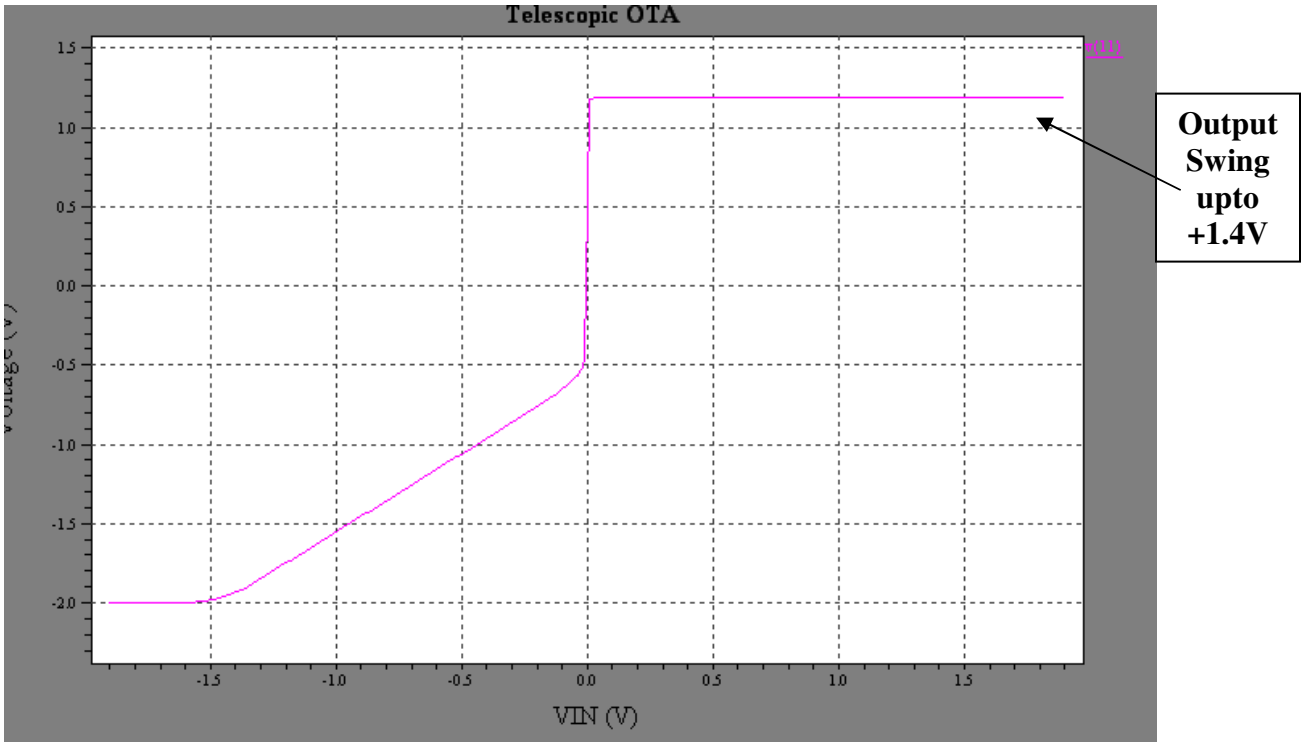


Fig: 3.6 Input/Output Swing and Offset Measurement of Telescopic OTA

3.6.3 Slew Rate

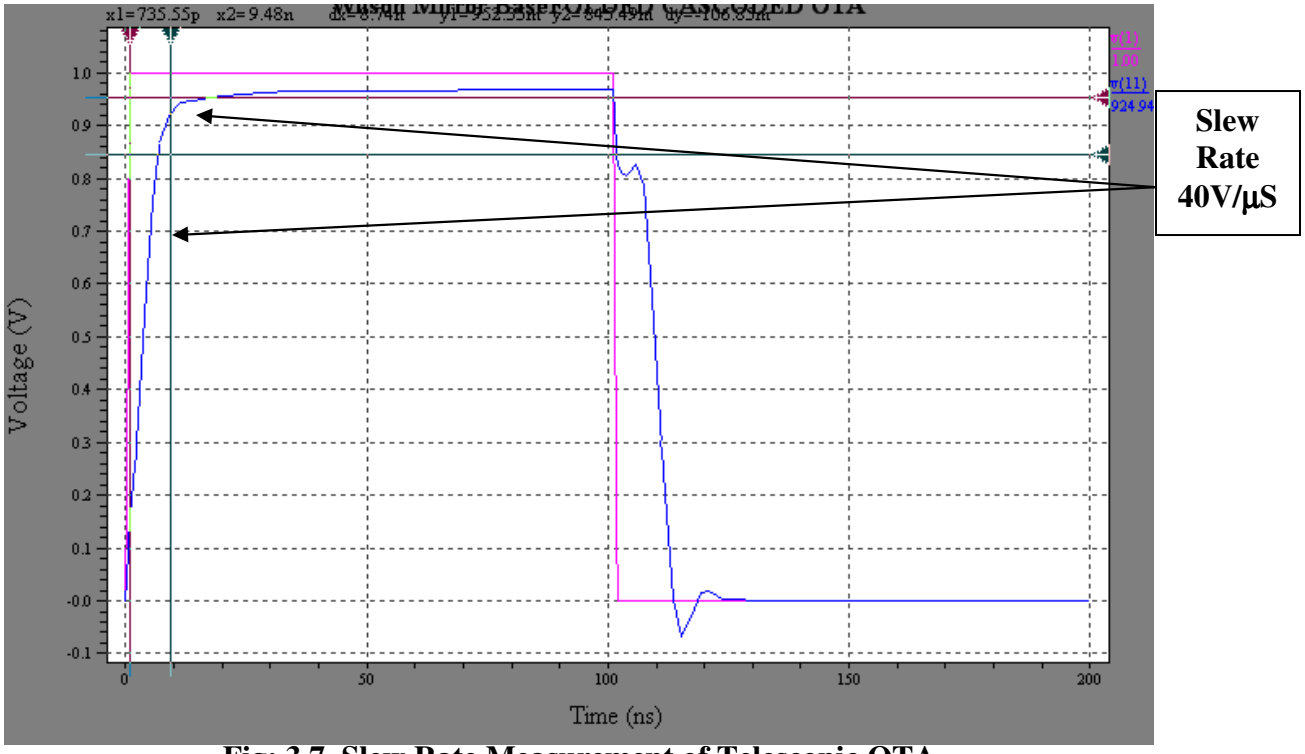


Fig: 3.7 Slew Rate Measurement of Telescopic OTA

3.6.4 Common Mode Gain for CMRR Measurement

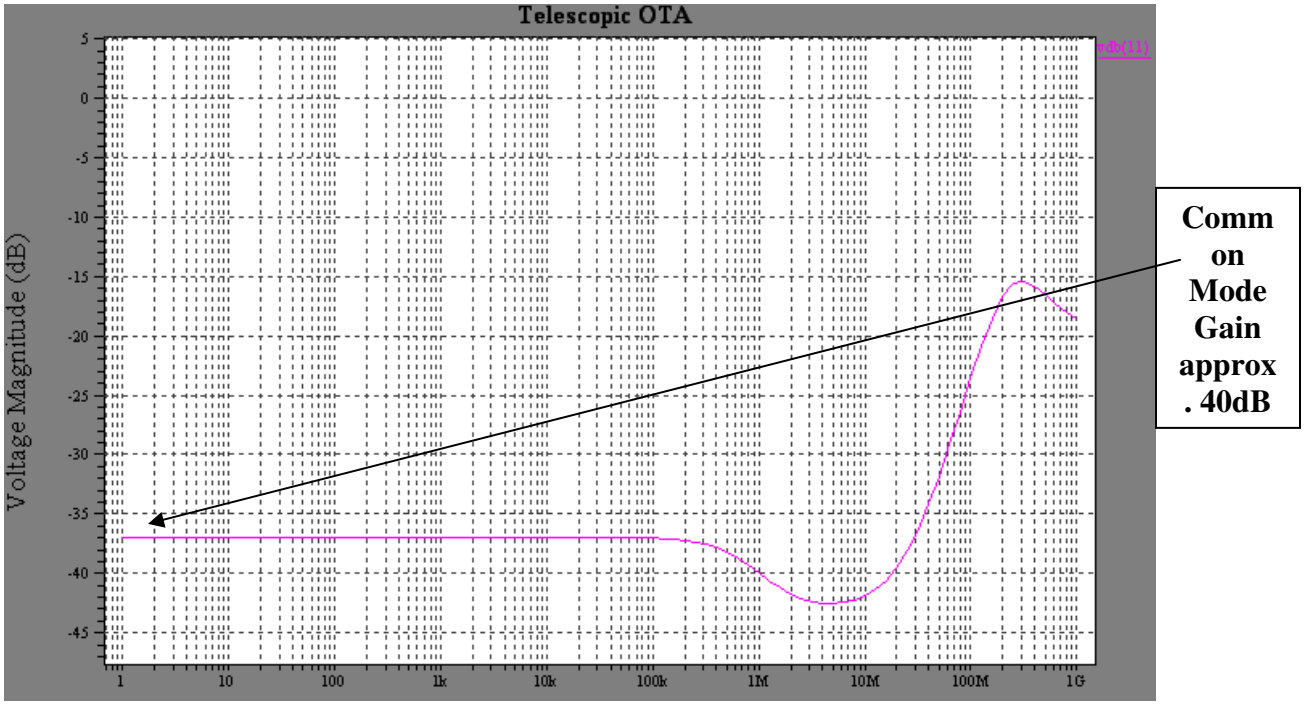


Fig: 3.8 Common Mode Gain for CMRR Measurement

3.6.5 Input Noise Spectral Density

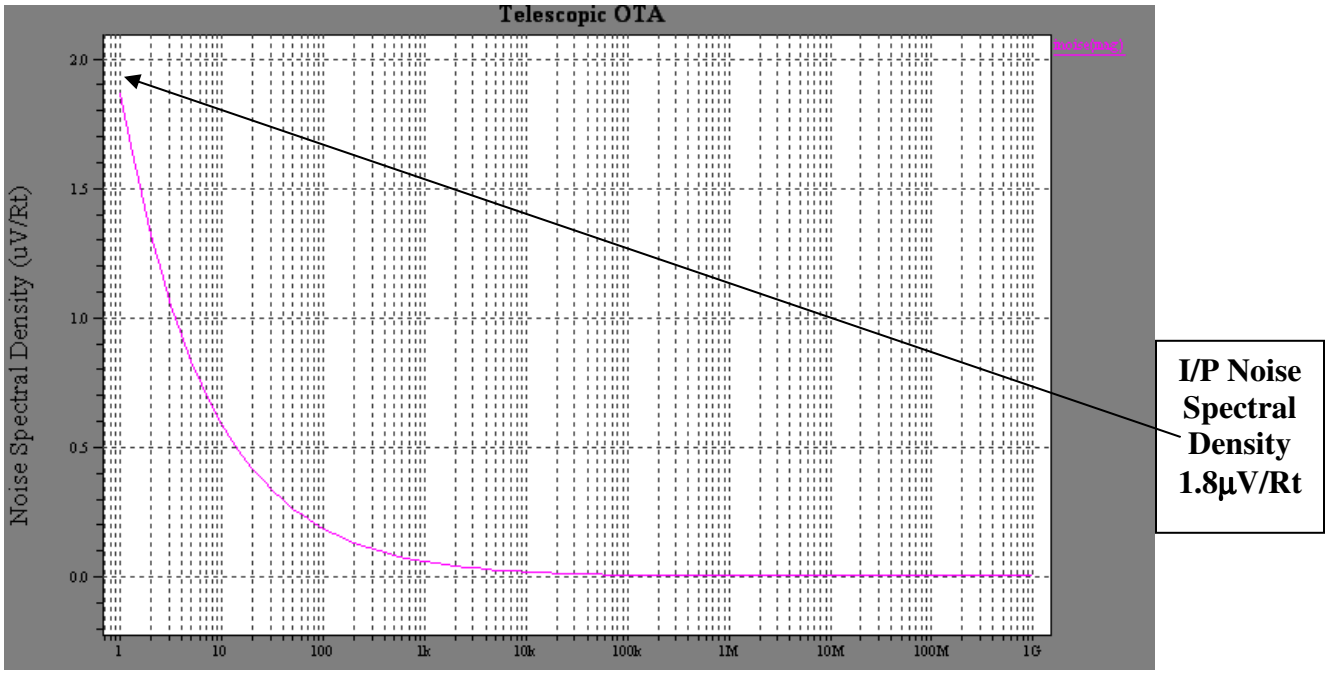


Fig: 3.9 Input Noise Spectral Density

3.6.6 Output Noise Spectral Density

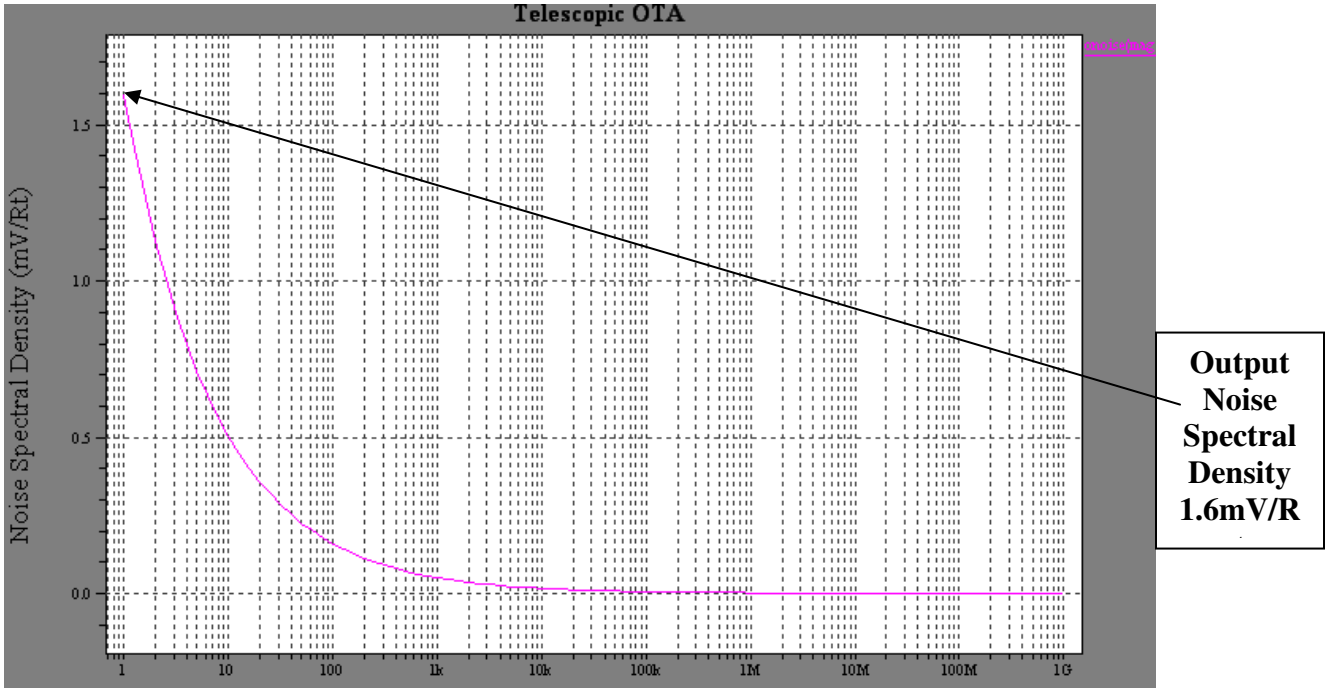


FIG: 3.10 OUTPUT NOISE SPECTRAL DENSITY

3.7 Summary of Simulation Results for Telescopic OTA

Specifications	Simulations Results
Gain	75dB
GBW	220MHz
Phase Margin	47dB
CMRR	120dB
PSSR	70dB

Offset Voltage	**1mV**
I/O Swing	**1.9V/1.4V**
Slew Rate	**40V/μS**
Input Noise spectral Density	**1.8μV/Rt**
Output Noise Spectral Density	**1.6mV/Rt**

3.3 Simulation Result summary of Telescopic OTA

3.8 Schematic of Telescopic OTA

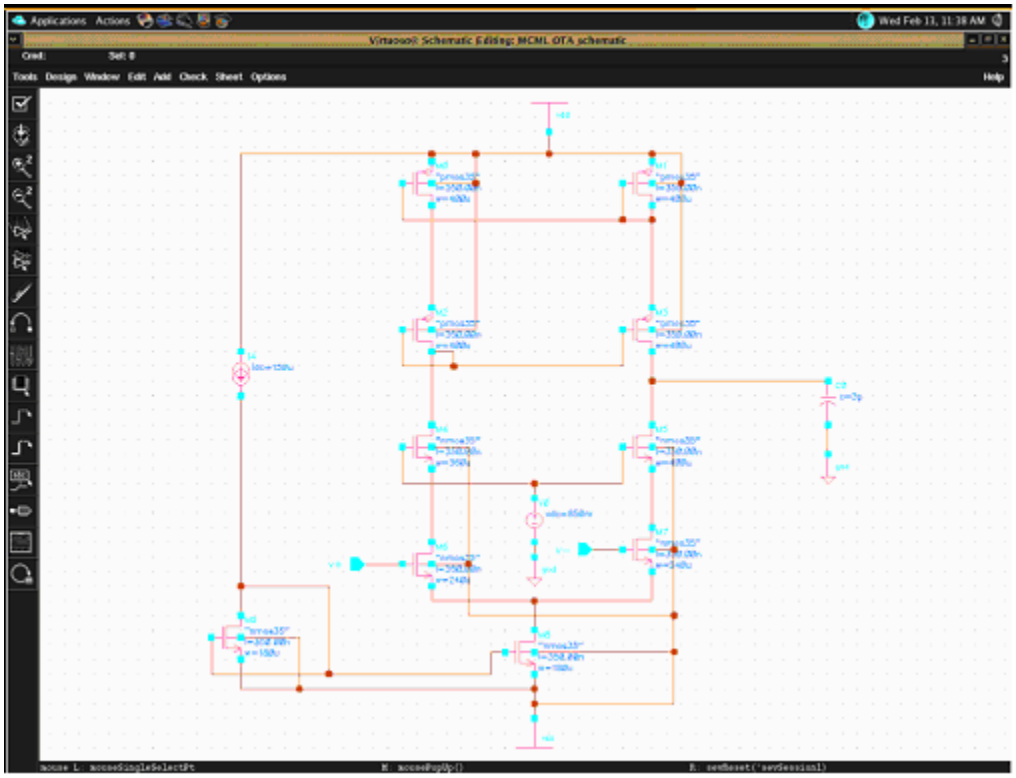
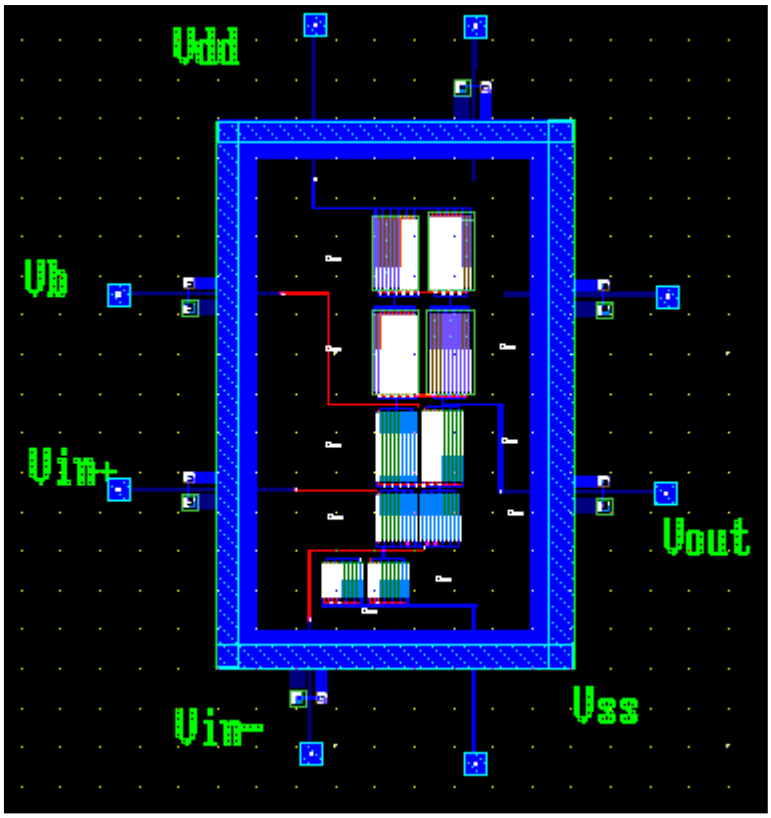


Fig:3.11 Schematic of Telescopic OTA

3.9 Physical Design of Telescopic OTA



3.12 Physical Design of Telescopic OTA

Chapter 4

Wide Swing Folded Cascoded OTA

4.1 Why Folded Cascode configurations?

The gain that can be achieved by a single stage is around 40 dB. Thus, in order to achieve 80 dB or so it is necessary to use a cascade of two stages. However, two stages bring about two poles one close to the other and this requires compensation network, besides increasing the complexity, reduces the design flexibility. A cascade with cascode load permits us to achieve high gain without the disadvantage of having two poles one close to each other.

Therefore the use of cascode based OTA is an interesting solution alternative to the two stages OTA. Thus two options have been left, one is "Telescopic configuration" and the other one is "folded cascode" configuration. The primary advantage of folded structure lies in the choice of voltage levels because it does not "stack" the cascode transistor on the top of the input device. Further Telescopic OTA suffers with limited output swing and hence the dynamic range. It is smaller than that of Folded Cascode because the tail transistor directly cuts into output swing from both side of op-amp.

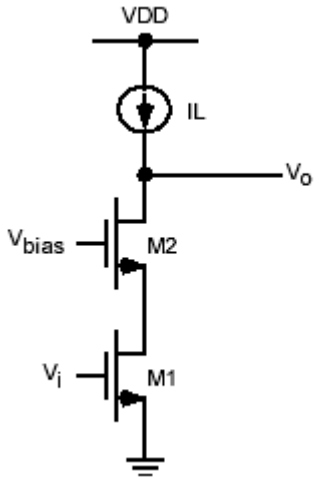


Fig: 4.1 Telescopic Cascode

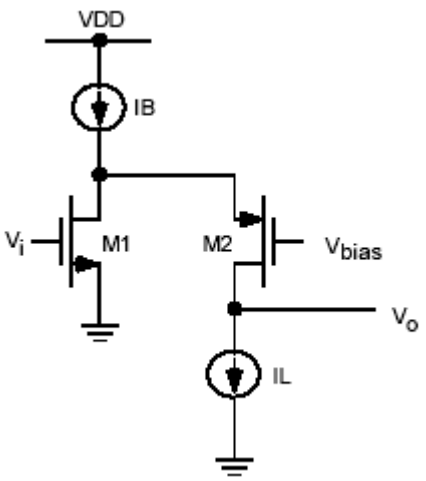


Fig: 4.2 Folded Cascode

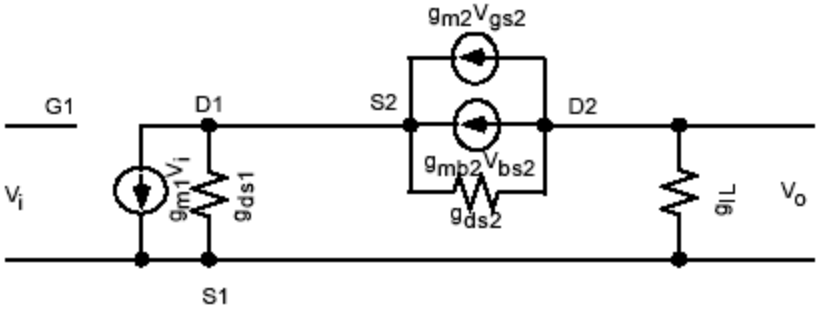


Fig: 4.3 Equivalent circuit of Telescopic Cascode

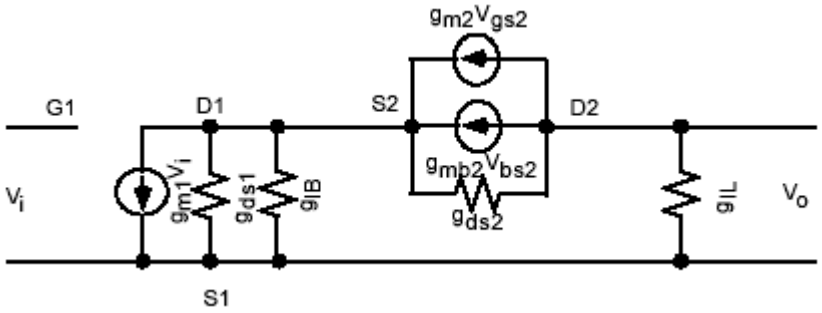


Fig: 4.4 Equivalent circuit of Folded Cascode

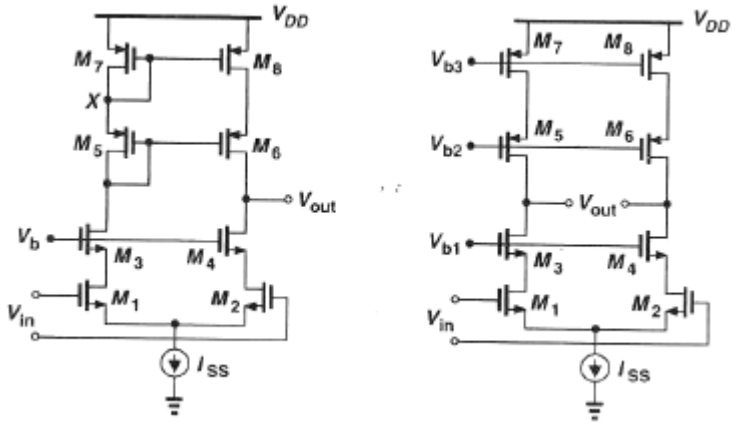


Fig:4.5 Single Ended and Double Ended Telescopic OTA

So, Telescopic OTA suffers with limited output swing, and there is a difficulty in shorting the input and output.

The output swing of telescopic op-amp (fig. 4.5) is given by

$$2V_{DD} - \left(V_{od1} + V_{od3} + V_{css} + V_{od5} + V_{od7}\right)$$

----------(4.1)

which is higher than that of folded cascode op-amp by overdrive voltage of tail current source.Another drawback of telescopic op-amp is difficulty in shorting input and outputs, e.g., to implement a unity gain buffer

The unity gain feedback topology shown in fig. 4.6 is considered. For M2 and M4 to be in saturation

$$V_{out} \le V_x + V_{TH2}$$
$$V_{out} >= V_b - V_{TH4}$$
$$V_x = v_b - v_{GS4}, V_b - V_{TH4} \le V_{out} \le V_b - V_{GS4} + V_{TH2}$$

----------(4.2)

As depicted in fig. 4.6, this voltage range is simply equal to V_{max} - V_{min} = V_{TH4} - (V_{GS4} - V_{TH2}), maximized by minimizing the overdrive of M4 but always less than V_{TH2}.

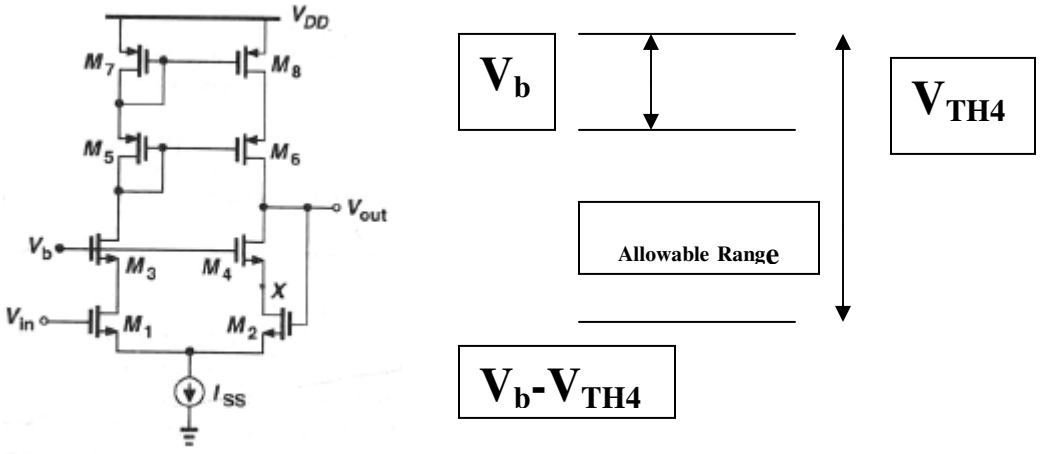


Fig: 4.6 Telescopic OTA with input and output shorted

Since the op-amp attempts to force V_{out} to be equal to V_{in}, for $V_{in} < V_b - V_{TH4}$, we have $V_{out} + V_{in}$ and M4 is in triode region while other transistors are saturated. Under this condition, the open-loop gain of op-amp is reduced. As Vin and hence V_{out} exceed $V_b - V_{TH4}$, M4 enters saturation and the open-loop gain reaches a maximum.

For $V_b - V_{TH4} < V_{in} < V_b - (V_{GS4} - V_{TH2})$, both M2 and M4 are saturated and for $V_{in} > V_b - (V_{GS4} - V_{TH2})$, M2, M1 enter the triode region, degrading the gain.

Further folded cascode op-amp has the capability of handling input common-mode levels close to one of the supply rails.

4.2 Basic Folded Cascode OTA

The folded-cascode OTA is shown in Fig.4.7. The name "folded-cascode" comes from folding down p-channel cascode active loads of a diff-pair and changing the MOSFETs to n-channels. This OTA, like all OTAs, has good PSRR compared to the two-stage op-amp since the OTA is compensated with the load capacitance.

To understand the operation of the folded-cascode OTA, consider Fig. 4.7 without the diff-amp (M1-M2*)* in the circuit. Without the diff-amp present in the circuit, 10μA flows in all MOSFETs. MOSFETs M3 and M4 provide the DC bias voltages to M5-M8. Note that the cascoded MOSFETs (M5-M12) are not biased for wide-swing operation. A wide-swing biasing circuit could replace M3-M4*,* and M9-M12 could be replaced with a wide-swing current mirror. Biasing for wide-swing operation increases the output voltage swing. When the diff-amp is added back into the circuit, it steals 5μA from M7-MI2, reducing their drain currents to 5μA.

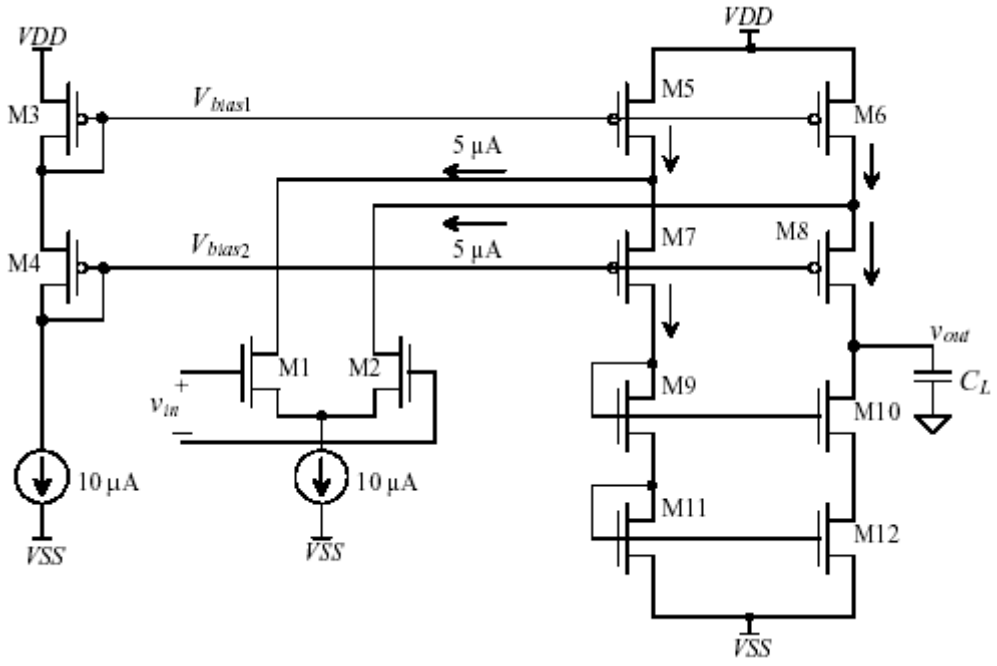


Fig: 4.7 Folded Cascode OTA

Applying an AC input voltage; V_{in} causes the diff-amp differential drain current to become $\mathbf{g_m v_{in}}$ *(*g_m is the transconductance of the diff-amp). This AC differential drain current is mirrored in the cascoded MOSFETs M7 through M12. The output voltage of the OTA is then

$$V_{out} = g_m V_{in} R_o$$

-------(4.3)

Where

$$R_o = \textbf{(R looking into drain of Ml0) ll (R looking into drain of M8)}$$

----------(4.4)

$$= r_{010}\left(1 + g_{m10} r_{012}\right) \parallel r_{08}\left(1 + g_{m8} r_{06}\right)$$

-------(4.5)

The gain of the folded-cascode OTA is given by

$$\frac{V_{out}}{V_{in}} = g_m R_o$$

------ (4.6)

The dominant pole of the OTA is located at $1/2\pi RoC_{L.}$ Parasitic poles exist at the sources of M7/M8 and M9/M1O. These parasitic poles should be larger than the unity gain frequency, which is given by

$$f_u = \frac{g_m}{2\pi C_L}$$

----------(4.7)

4.3 Design of Folded Cascade OTA

The folded cascode OTA is shown in Fig. 4.8. The name "folded cascode" comes from folding down n-channel cascode active loads of a diff-pair and changing the MOSFETs to p-channels. This OTA, like all OTAs, has good PSRR compared to the operational amplifier.

To understand the operation of the folded cascode OTA, differential stage consisting of PMOS transistors M9 and M10 intend to charge Wilson mirror. MOSFETs M11 and M12 provide the DC bias voltages to M5-M6-M7-M8 transistors

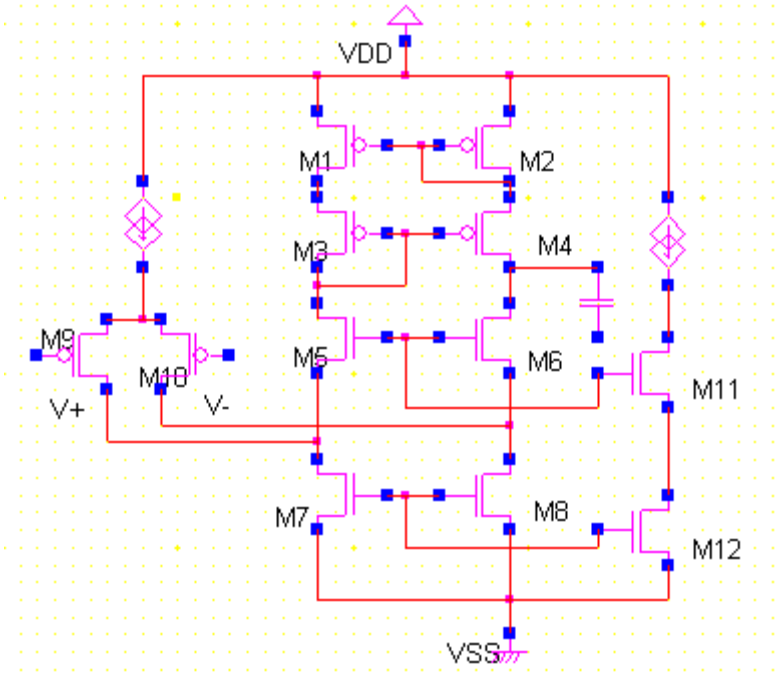


Fig: 4.8 Folded Cascode OTA

The output Voltage of the OTA is given by:

$$V_{out} = G_m V_{in} R_o$$

----------(4.8)

Where

R_0 = (R looking into drain of M6) ‖ (R looking into drain of M4)

$$= [r_{06}(1 + g_{m06} r_{08})] \parallel [r_{04}(1 + g_{m04} r_{02})]$$

----------(4.9)

The "Unity gain frequency**"** of the OTA is given by the expression:

$$f_u = \frac{2\pi g_{m9}}{C_L}$$

----------(4.10)

Gm is computed as

$$G_m = 2\pi(GBW)C_L$$

----------(4.11)

The open-loop voltage gain is given by:

$$A_V = \frac{g_{m9} g_{m4} g_{m6}}{I_D{}^2 (g_{m4} \lambda_N{}^2 + g_{m6} \lambda_P{}^2)}$$

----------(4.12)

Where g_{m9}, g_{m4} and g_{m6} are respectively the transconductances of transistors M9, M4 and M6. I_D is the bias current flowing in MOSFETs M4, M6, and M9. C_L is the capacitance at the output node.λ_N and λ_P are the parameters related to channel length modulation respectively for NMOS and PMOS devices.

Taking the complimentarily between the transistors M4 and M6 into account:

$$g_{m4} = g_{m6}$$

----------(4.13)

The gain expression becomes:

$$A_V = \frac{g_{m9} g_{m4}}{I_D{}^2 (\lambda_N{}^2 + \lambda_P{}^2)}$$

----------(4.14)

A top-down synthesis methodology for CMOS OTA architectures illustrated by a design plan (Fig. 4.8). Specifications, for example: gain and transition frequency in order to determine the unknowns that are MOS devices sizes. The universal gm/I_D as a function of I_D /(W/L) characteristic of the NMOS and PMOS transistors of the of the NMOS and PMOS transistors of the CMOS technology under consideration (0.35µm) is exploited in order to apply the above design steps and compute the design parameters from top-down synthesis flow using specifications

$$w_u \rightarrow \frac{g_{m9}}{I_D} \leftrightarrow \frac{I_D}{\left(\frac{W}{L}\right)_9}$$

$$A_v \rightarrow \frac{g_{m4}}{I_D} \leftrightarrow \frac{I_D}{\left(\frac{W}{L}\right)_4}$$

----------(4.15)

4.4 G_m/I_D Method

The present trend toward portable equipment as well as the increasing circuit density and size of integrated systems tend to make low power consumption a primary concern. In CMOS analog circuits the minimum power consumption is achieved when MOS transistors operate in the weak inversion region. However, the best compromise in terms of consumption and speed is achieved in moderate inversion.

MOS transistors are either in strong inversion or in weak inversion. Mainstream methods assume generally strong inversion and use the transistor gate voltage overdrive (GVO) as the key parameter, where GVO = $V_G - V_T$, V_G being the gate voltage and V_T, the threshold voltage. Micropower design techniques, on the other hand, exploit known weak inversion models. It provides an alternative taking full advantage of the moderate inversion region to obtain a reasonable speed- power compromise. The method exploits the transconductance over dc drain current ratio (g_m/I_D) relationship versus the normalized current I_D /(W / L).

we consider the relationship between the ratio of the Tran conductance g_m over dc drain current I_D and the normalized drain current as I_D /(W / L) a fundamental design tool. The choice of g_m / I_D is based on its relevance for the three following reasons.

1) **It is strongly related to the performances of analog**

2) It gives an indication of the device-operating region.

3) It provides a tool for calculating the transistors dimensions

The g_m / I_D ratio is a measure of the efficiency to translate current (hence power) into transconductance; i.e., the greater the g_m / I_D value, the greater the transconductance we obtain at a constant current value. Therefore, the g_m / I_D ratio is sometimes interpreted as a measure of the "transconductance generation efficiency"

The relation of the g_m / I_D ratio is equal to the derivative of the logarithmic of I_D with respect to V, as shown below

$$\frac{G_m}{I_D} = \delta \ln \frac{\left(\frac{I_D}{\frac{W}{L}} \right)}{\delta V_G}$$

----------(4.16)

This derivative is maximum in the weak inversion region where the I_D dependence versus V_G is exponential while it is quadratic in strong inversion, becoming almost linear deeply in strong inversion because of the velocity saturation. The maximum is equal to $1 / (n U_T)$ where *n* is the sub threshold slope factor and U_T the thermal voltage. The g_m / I_D ratio decreases as the operating point moves toward strong inversion. Therefore, the g_m / I_D ratio is also an indicator of the mode of operation of the transistor.

The "universal" quality of the g_m / I_D versus I_D /(W/L) curve can be extensively exploited during the design phase, when the transistor aspect ratios (W/L) are unknown. Once a pair of values among g_m / I_D, has been derived, the W/L of the transistor can be determined.

$$\frac{g_m}{I_D} = 0 \qquad \textbf{in deep sub threshold operation}$$

$$= \frac{1}{n_{wi} U_T} \qquad \textbf{in weak Inversion}$$

$$= \left[\frac{2\mu C_{ox}}{n_{si} I} \right]^{1/2} \qquad \textbf{in strong inversion}$$

----------(4.17)

n_{wi} **subthresold slop factor**

U_T **Thermal Potential**

μ **Mobility**

C_{ox} **Gate Capacitance**

N_{si} **Body Factor**

I **Scaled drain current equal to I_D /(W/L)**

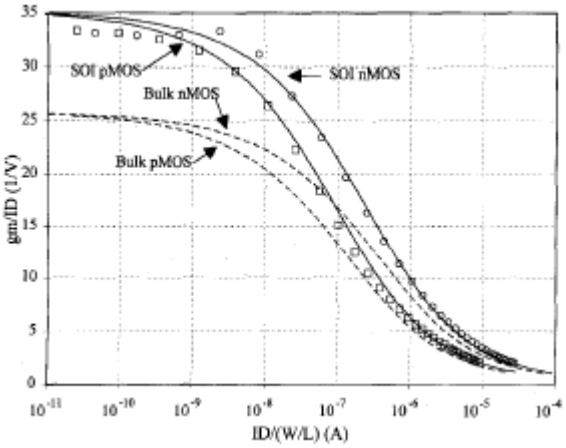


Fig. 4.9. g_m / I_D versus I_D /(W / L) curve

4.5 Specifications

Specifications	Value
A_V (dB)	90
F_T (MHz)	250
C_L (pf)	0.1
V_{DD}, V_{SS}	+2V, -2V
Phase Margin	60deg
Channel Length	0.35

Table 4.1 Specifications for Telescopic OTA

Based on above specification and design procedure Calculated Design Parameter and Aspect Ratio for transistors are as under.

Design Parameter

PARAMETER	VALUE
$G_{m9,\ 10}$ / I_D (v^{-1})	7.92
I_D /(W/L) $_{9,10}$ (μA)	0.86
G_{m4}/ I_D (v^{-1})	5.84
I_D /(W/L) 4(μA)	1.65

TABLE 4.2 CALCULATED DESIGN PARAMETER FOR FOLDED CASCODE OTA

Aspect Ratio

Transistor	W/L in μm
M1, M2, M3, M4	18/0.35
M5, M6, M7, M8, M11, M12	6/0.35
M9, M10	35/0.35

TABLE 4.3 CALCULATED ASPECT RATIO FOR FOLDED CASCODE OTA

The designed **Folded Cascode OTA** was biased at 2V power supply voltage using **CMOS technology of 0.35 μm with the BSIM3V3 (Level 49 Parameter) MOSFET model.**

4.6 Simulation Results of Folded Cascode OTA

4.6.1 AC Analysis

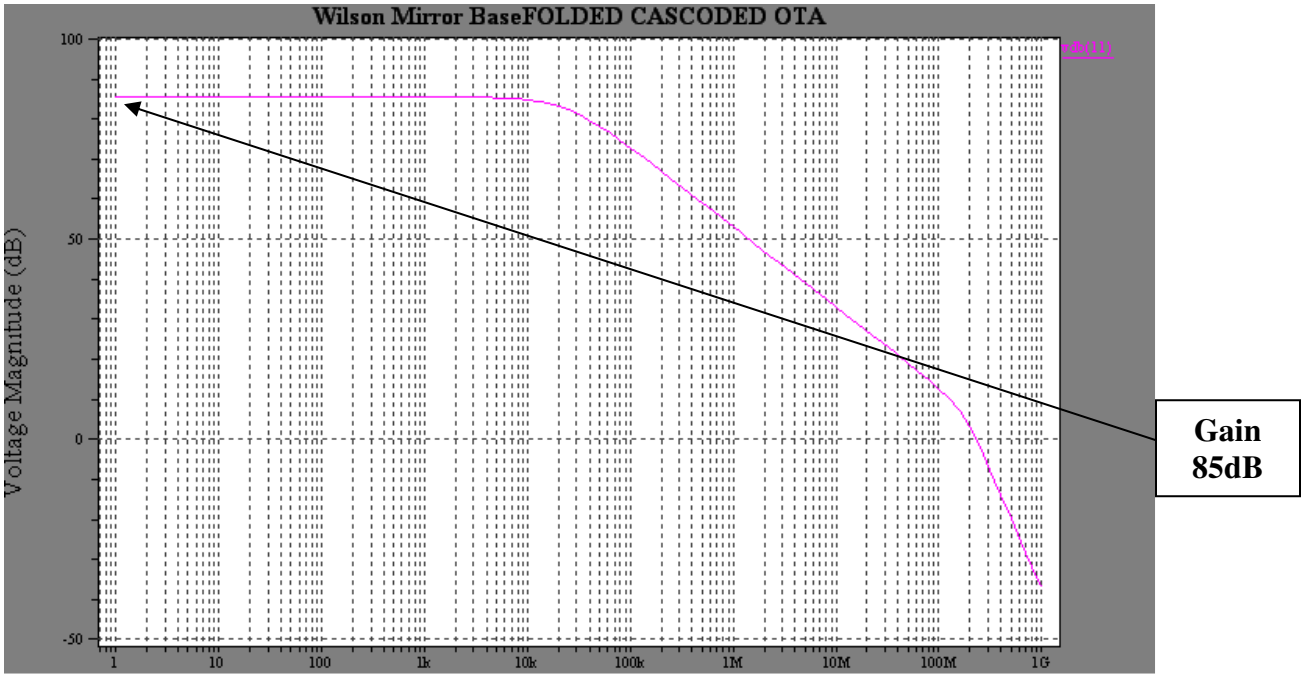


Fig: 4.10 AC Analysis of Folded Cascode OTA

4.6.2 Gain bandwidth and Phase Margin

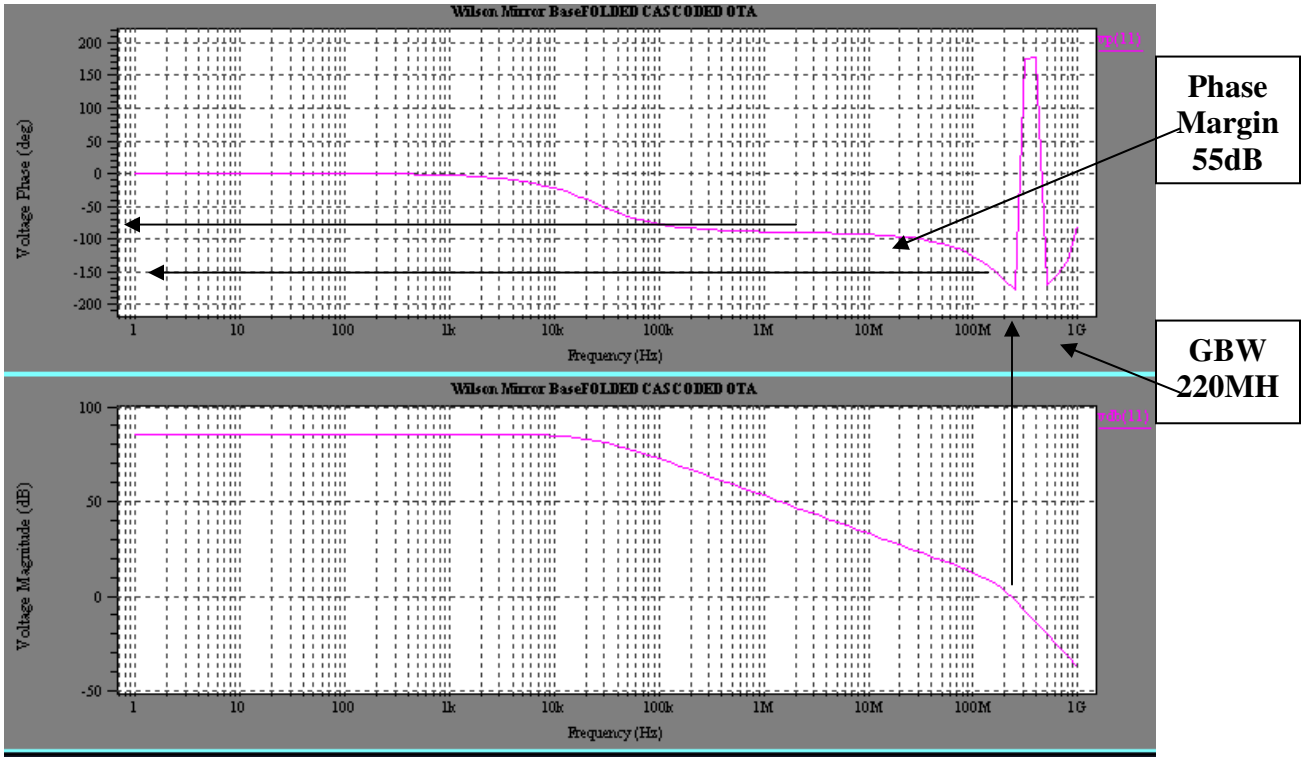


Fig: 4.11 Gain Bandwidth and Phase Margin of Folded Cascode OTA

4.6.3 Input-output Swing

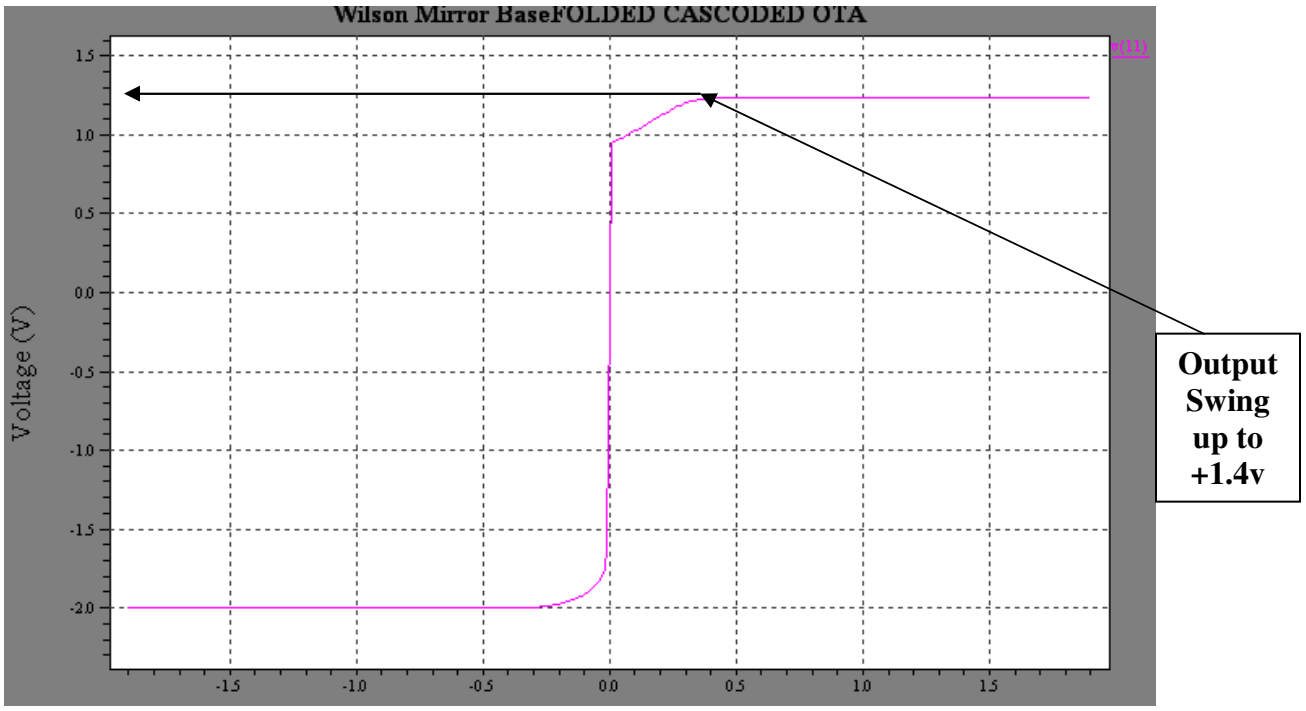


Fig: 4.12 Input-Output Swing of Folded Cascode OTA

4.6.4 Slew Rate

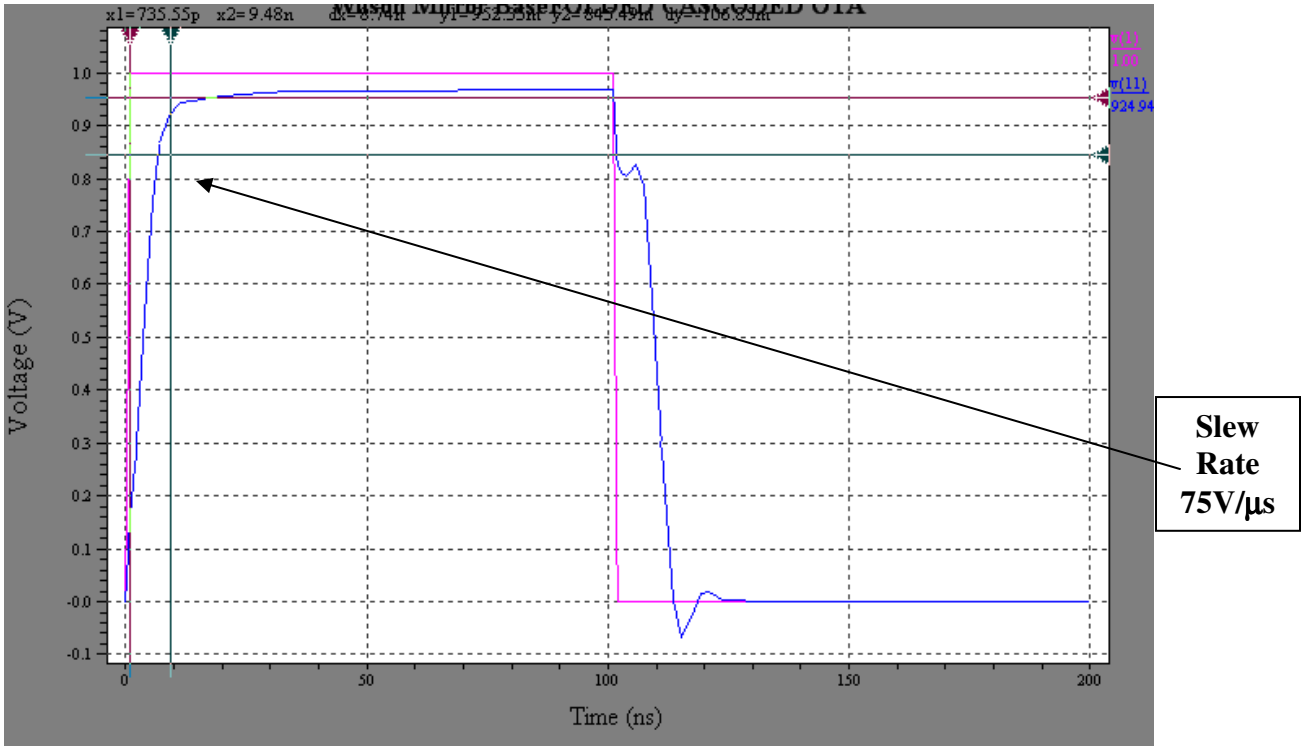


Fig: 4. 13 Slew Rate of Folded Cascode OTA

4.6.5Common Mode Gain

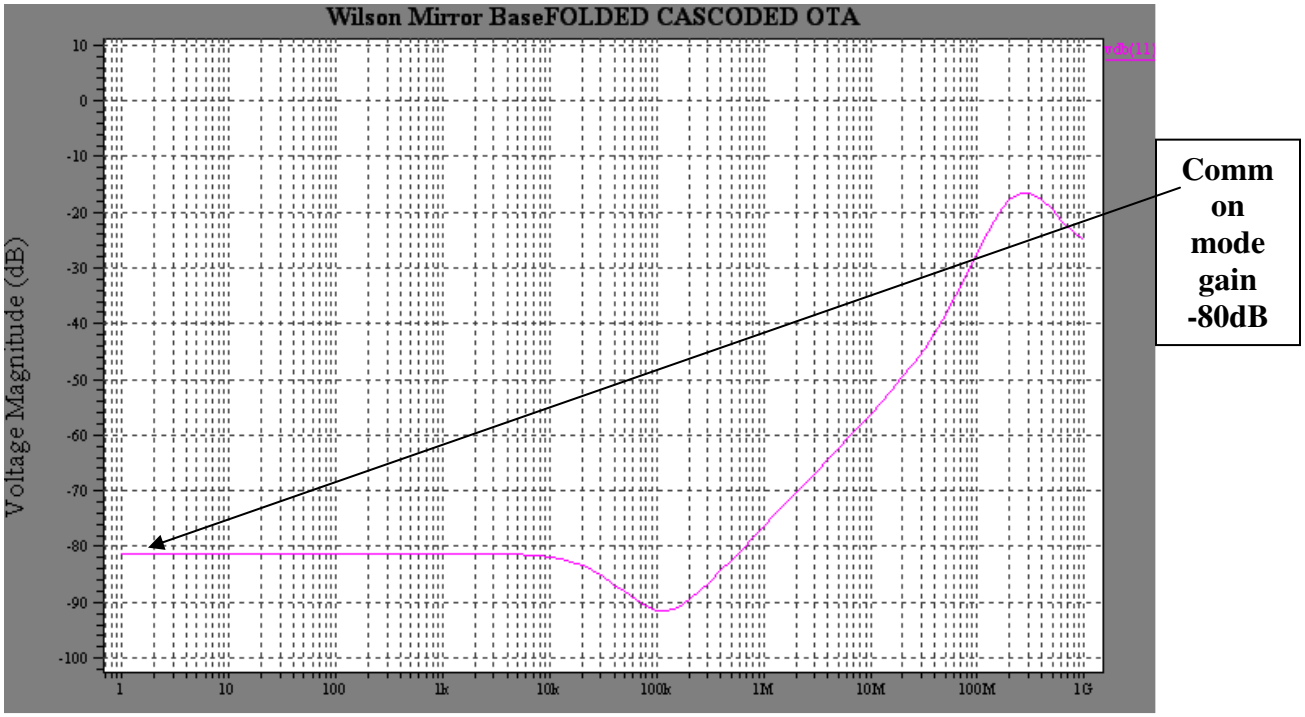


Fig: 4.14 Common Mode Gain of Folded Cascode OTA

4.6.6 PSSR Measurement with VDD=0V

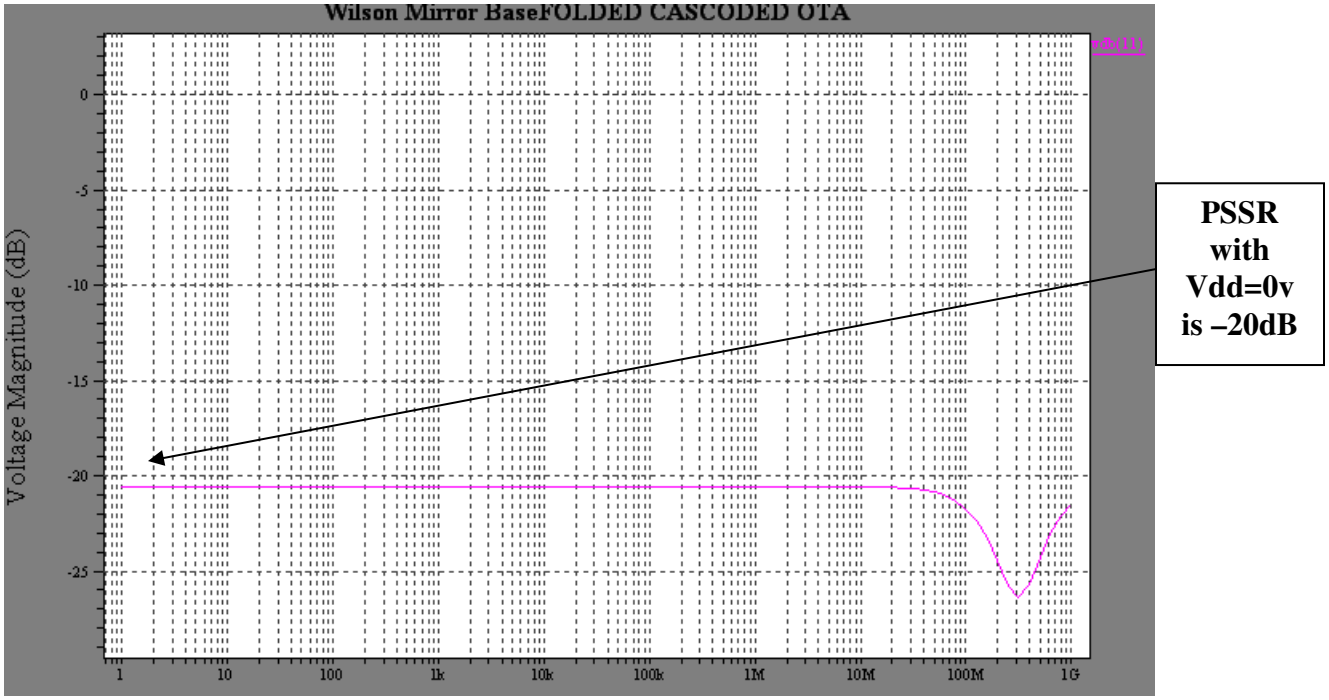


Fig: 4.15 PSSR Measurenmt with Vdd=0V for Folded Cascode OTA

4.6.7 PSSR Measurment with Vin=0V

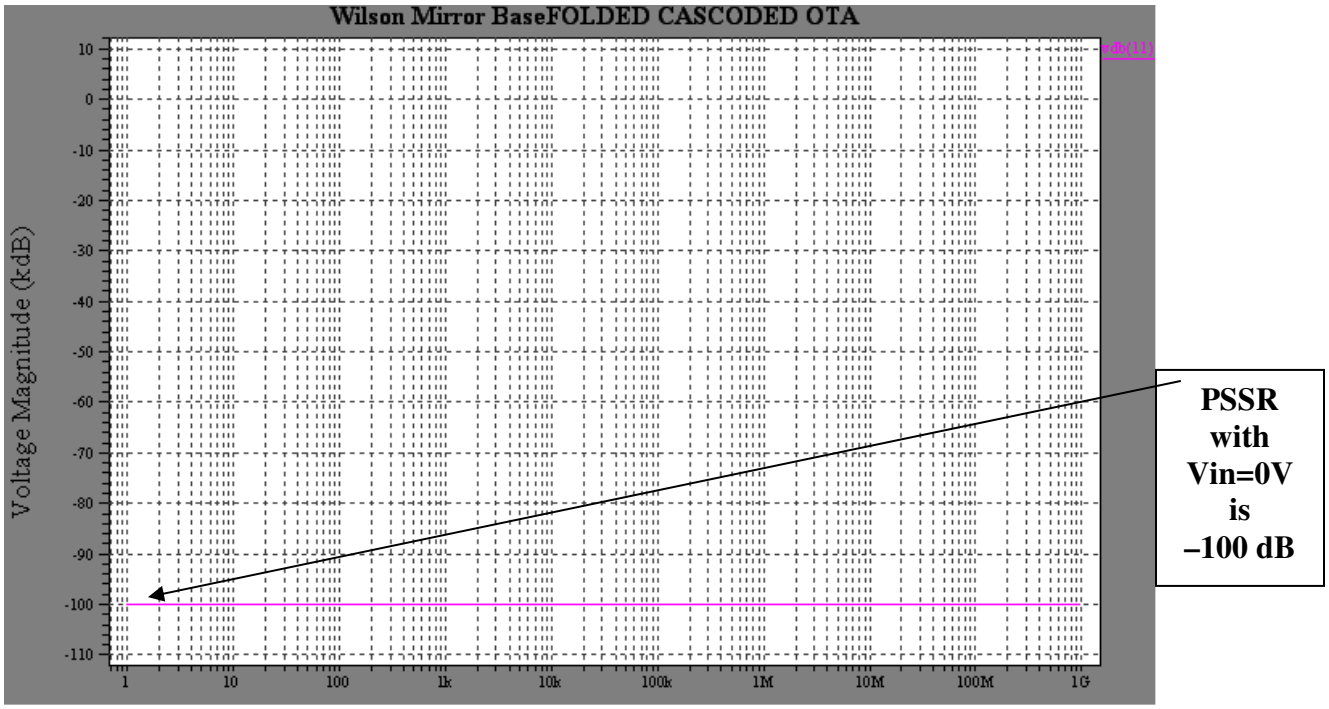


Fig: 4.16 PSSR Measurment with Vin=0v for folded Cascode OTA

4.6.8 Noise Spectral Density

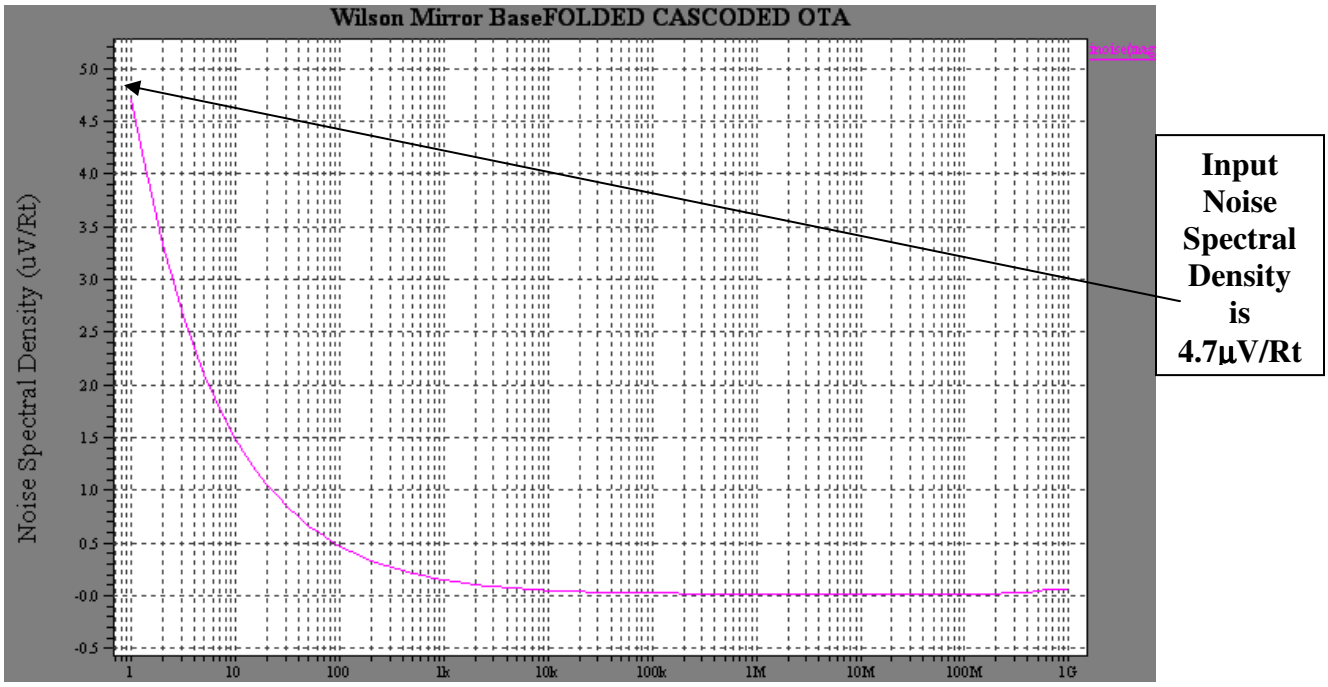


Fig: 4.17 Input Noise Spectral Density for Folded Cascode OTA

4.6.9 Output Noise Spectral Density

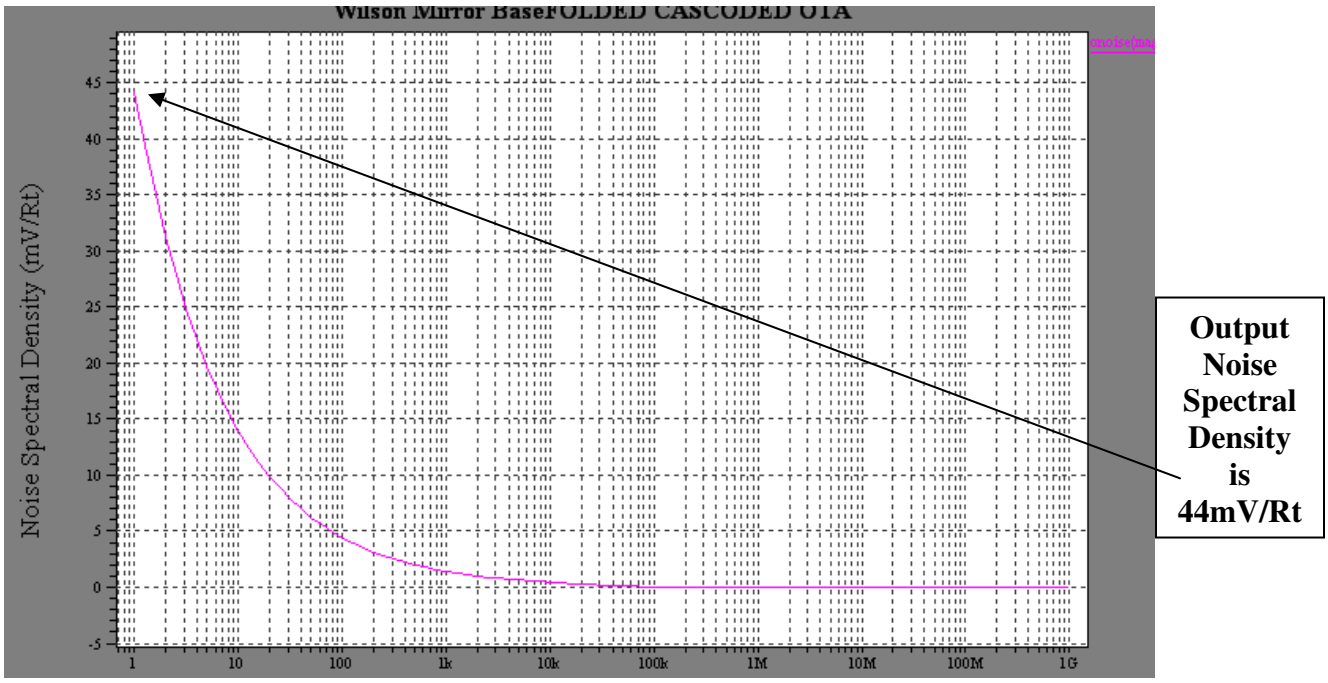


Fig: 4.18 Output Noise Spectral Density for Folded Cascode OTA

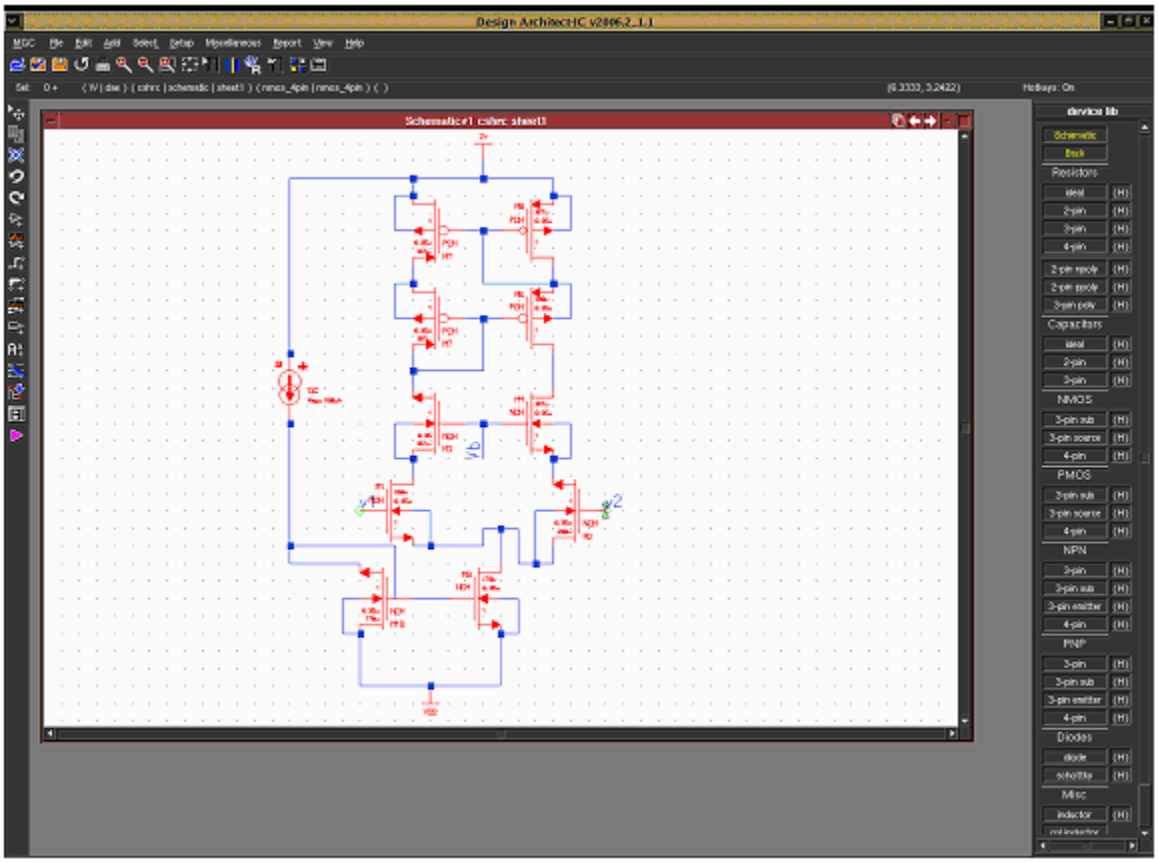
4.7 Summary of Simulation Results for Folded Cascode OTA

Specifications	Simulations Results
Gain	85dB
GBW	220MHz
Phase Margin	55dB
CMRR	160dB
PSSR	80dB

Offset Voltage	**1mV**
I/O Swing	**1.9V/1.4V**
Slew Rate	**75V/μS**
Input Noise spectral Density	**4.7μV/Rt**
Output Noise Spectral Density	**44mV/Rt**

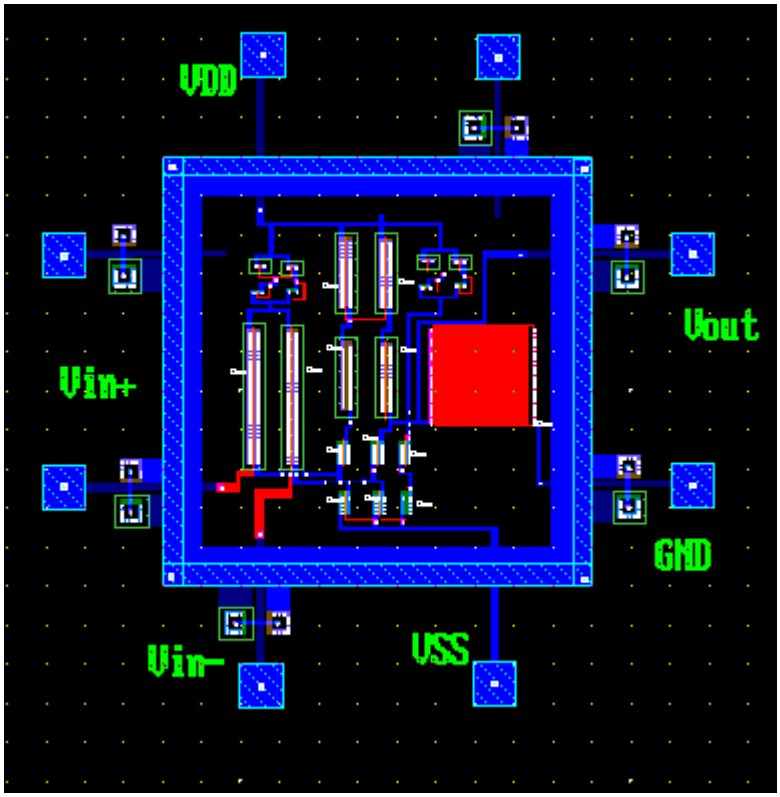
4.4 Simulation Result Summary of folded Cascode OTA

4.8 Schematic of Folded Cascode OTA



4.19 Schematic of Folded Cascode OTA

4.9 Physical Design of Folded Cascode OTA



4.20 Physical Design of Folded Cascode OTA

4.10 Biasing and Wide Swing OTA Circuit

The bias voltages can be generated using the circuit of Fig.5.6. This circuit is basically two wide-swing current mirrors. MB1 and MB2 are sized one-fourth the size of the other MOSFETs. This biasing scheme causes 10μA to flow in MOSFETs MN3, MN4, MP6, MP8 **(Fig: 4.21)**, and all MOSFETs in the biasing circuit **(Fig: 4.19 or 4.20).**

MOSFETs MNl, MN2, and MP5, MP7, MN5-MN8 have 5μA of drain current. Note that this biasing scheme gives the maximum voltage swing on the output of the OTA (i.e., the drains of MP7 and MN7).

Wide Swing means that I/P CMR is close to Supply Voltage.

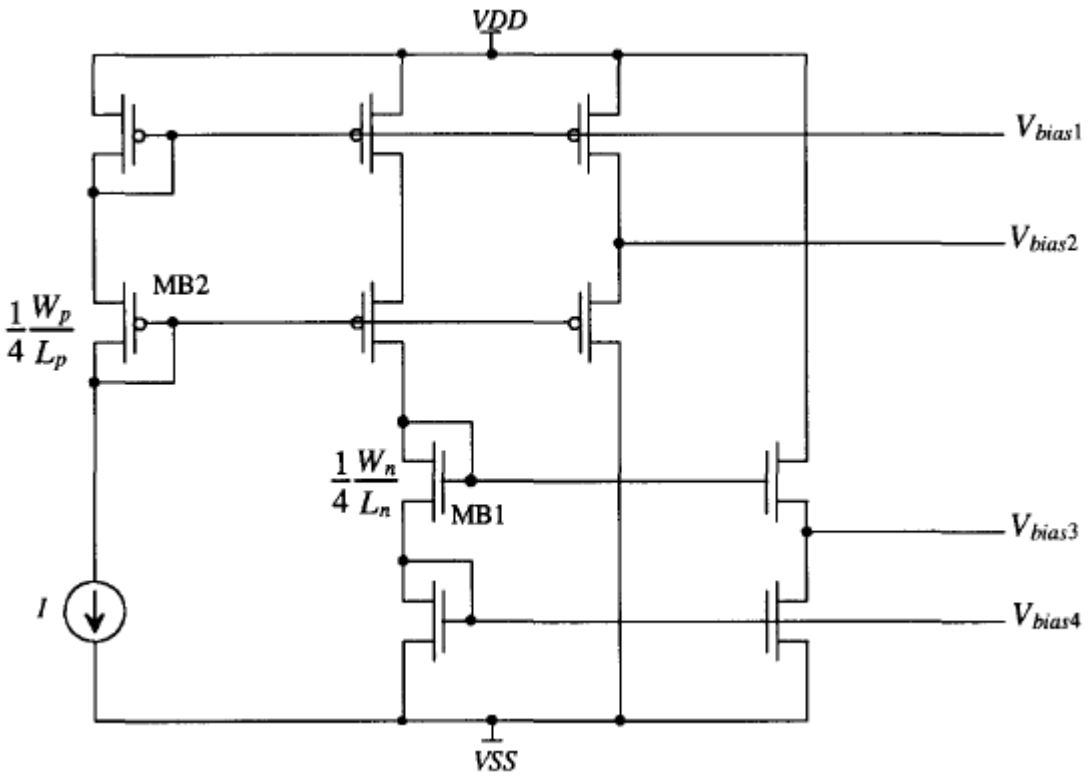


Fig: 4.21 Biasing Circuit

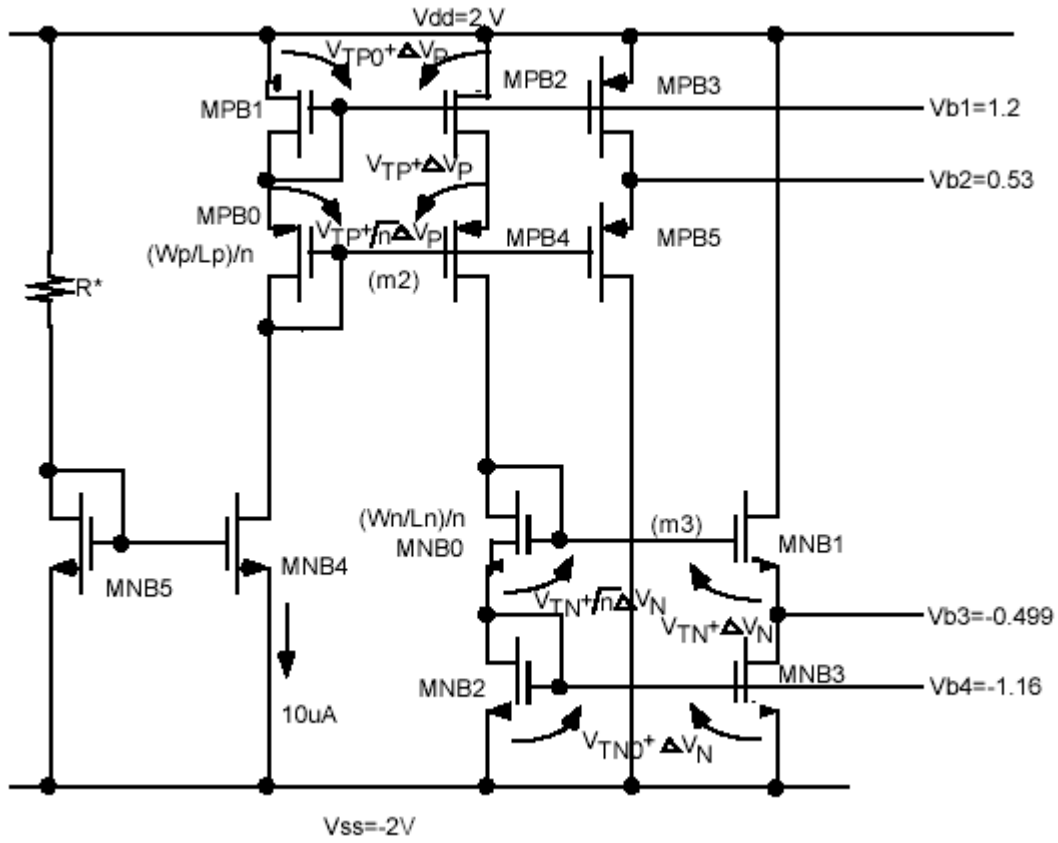


Fig: 4.22 Modified Bias Circuit

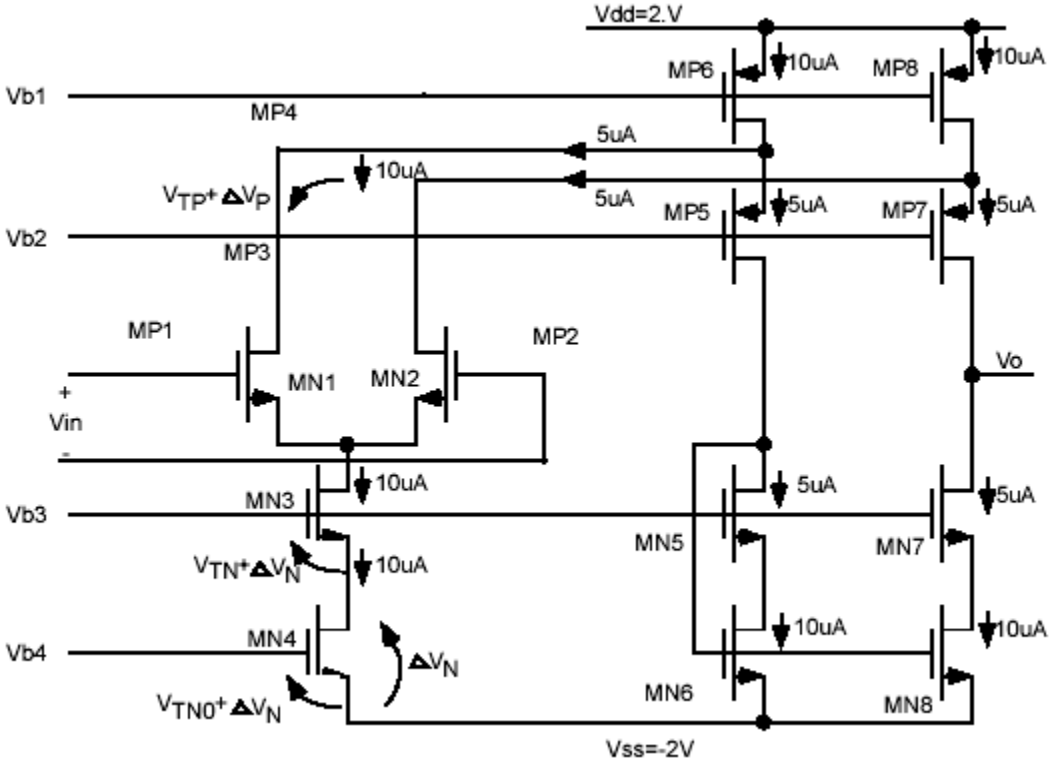


Fig: 4.23 Wide Swing OTA (NMOS Differential Pair-Poor Negative CMR) Circuit

4.11Simulation Result for Wide Swing OTA (NMOS Differential Pair-Poor Negative CMR)

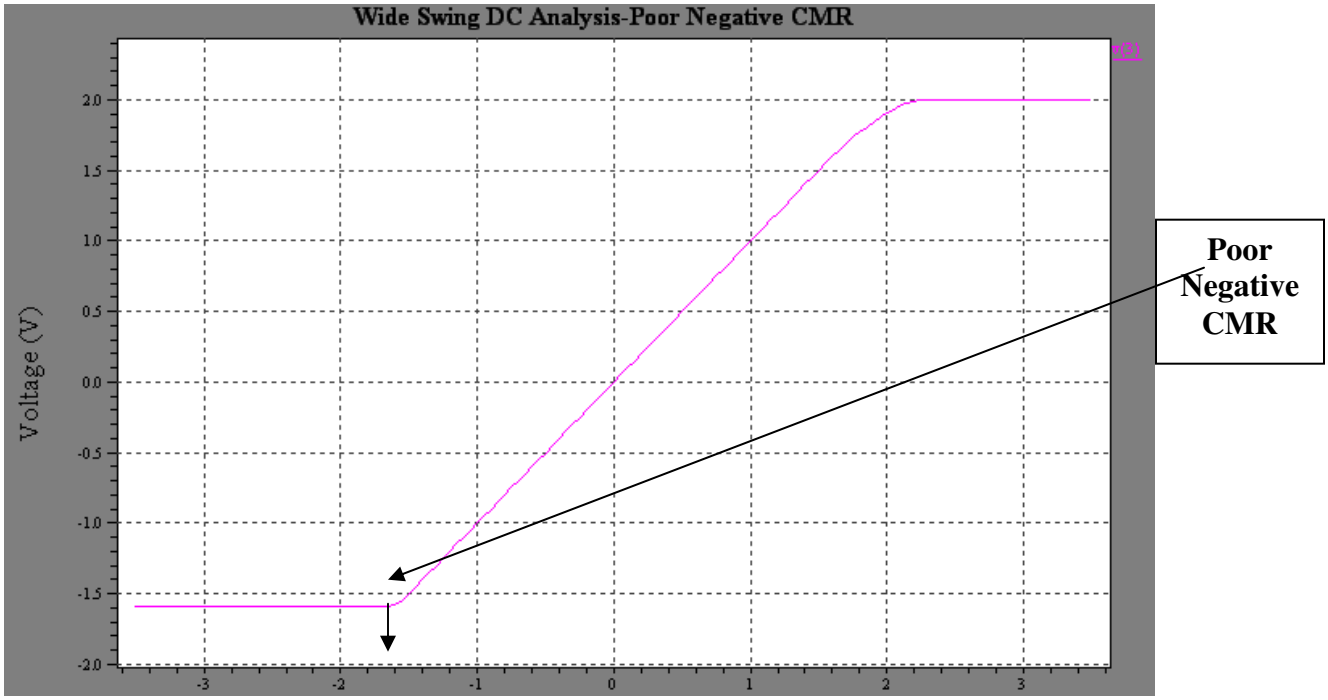
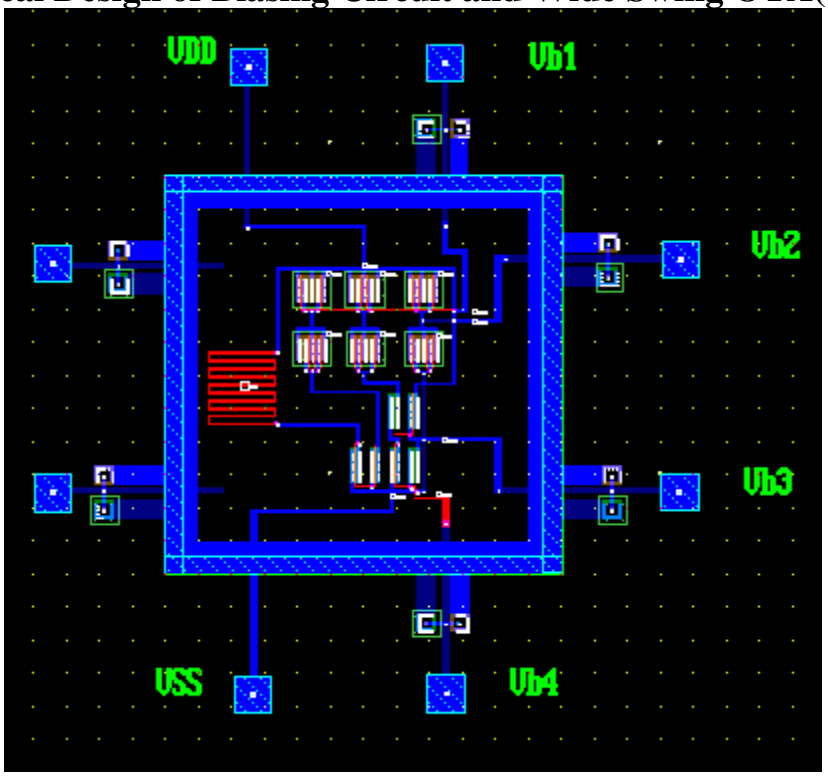


Fig: 4.24Wide Swing OTA (NMOS Differential Pair-Poor Negative CMR) Result

"The problem with Differential amplifier with NMOS input pair is that the positive CMR extends beyond VDD, while the negative CMR is limited by the minimum voltage across the differential input."

4.12 Physical Design of Biasing Circuit and Wide Swing OTA(-CMR)



Biasing Circuit

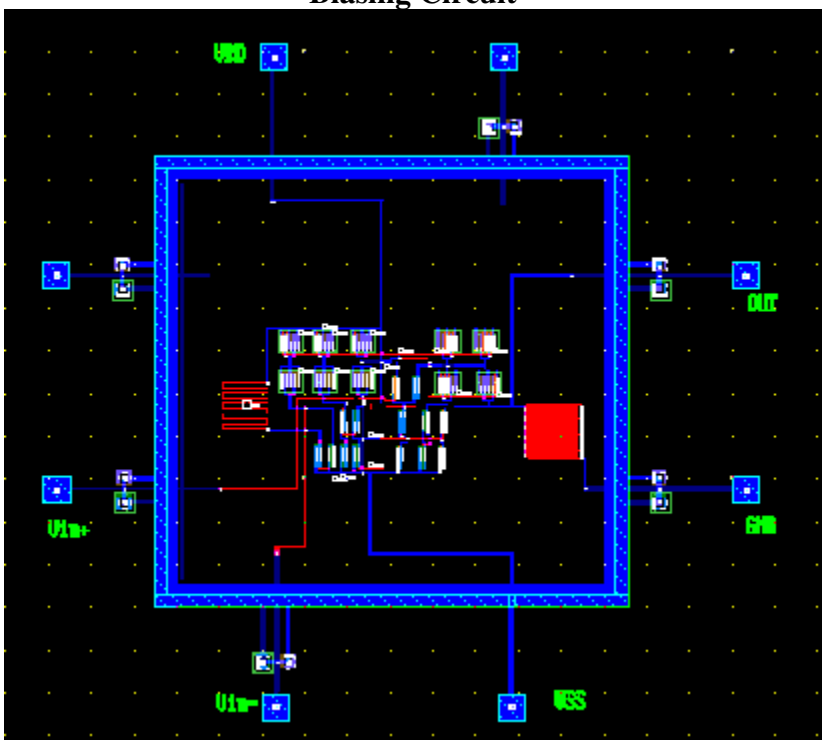


Fig:4.25 Physical Design of Biasing Circuit and Wide Swing OTA(-CMR)

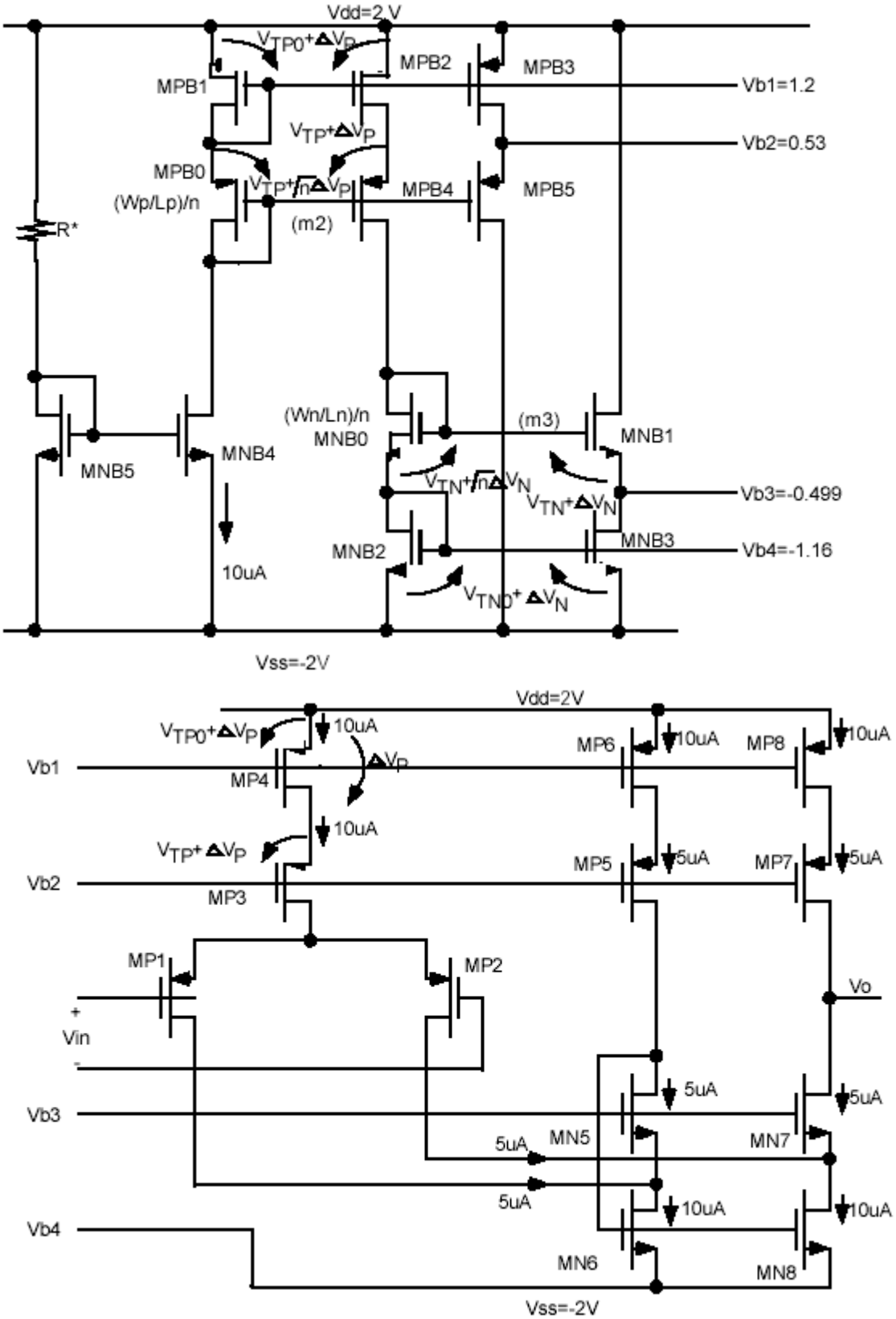


Fig: 4.26 Biasing and Wide Swing OTA (PMOS Differential Pair-Poor Positive CMR) Circuit

4.13 Simulation result for Wide Swing OTA (PMOS Differential Pair-Poor Positive CMR)

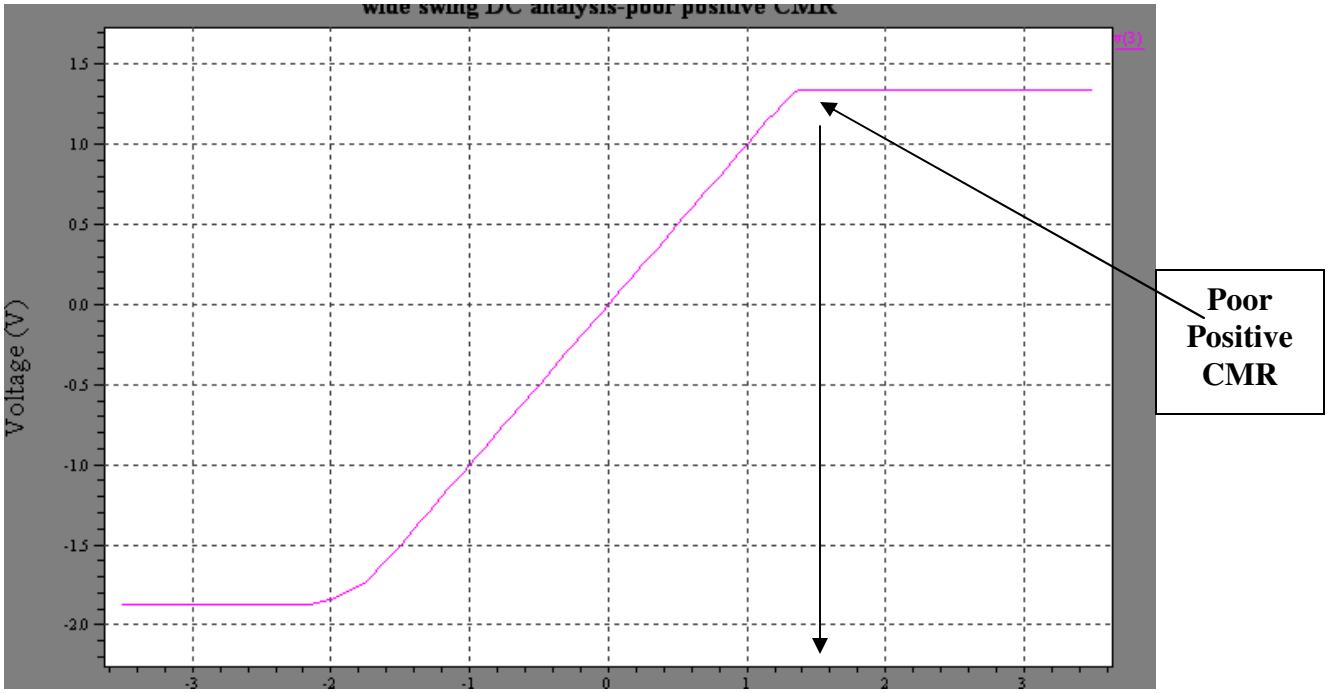


Fig: 4.27 Wide Swing OTA (PMOS Differential Pair-Poor Positive CMR) Result

"The problem with Differential amplifier with PMOS input pair is that the positive CMR is limited by the minimum voltage across the differential input, while the negative CMR extend beyond VSS."

4.14 Physical Design of Wide Swing OTA(+CMR)

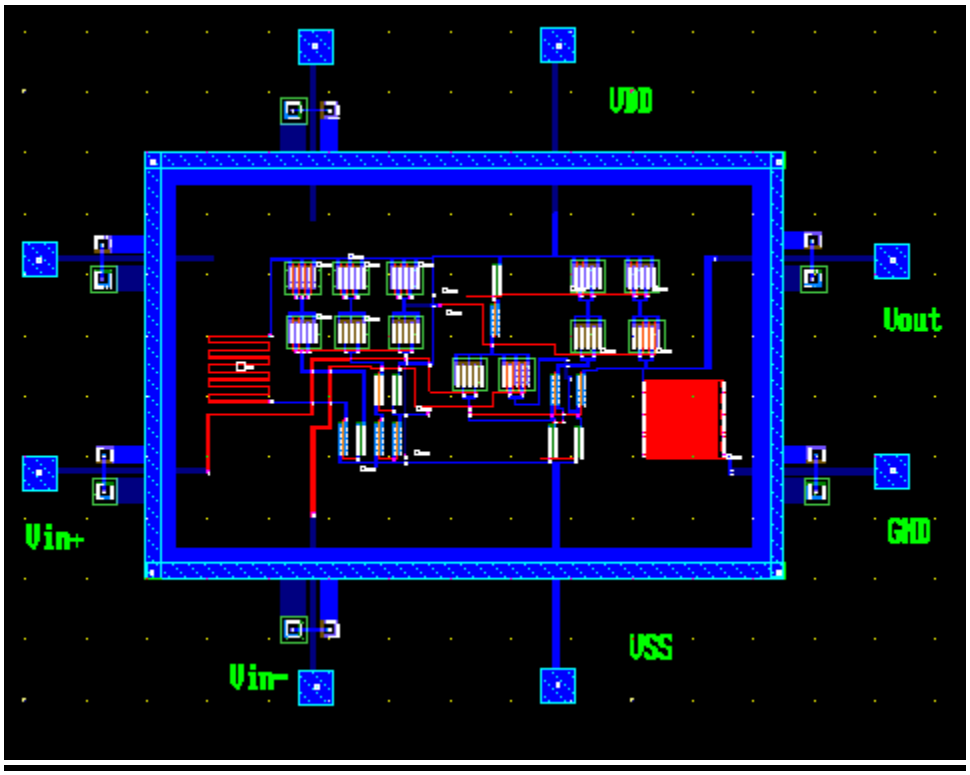
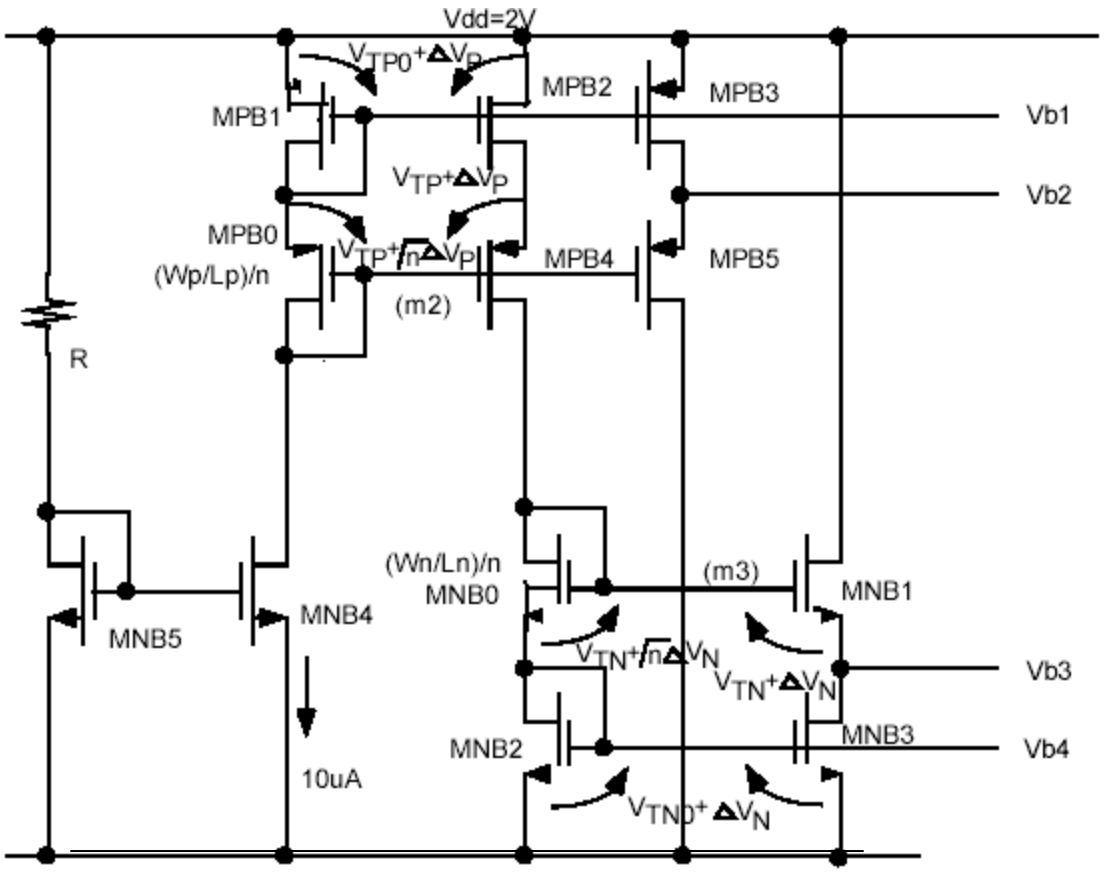


Fig: 4.28Physical Design of Wode Swing OTA(+CMR)

4.15 Wide Swing Folded Cascoded OTA

Figure 4.26 shows a "Wide-swing Folded Cascoded OTA" which extends the input CMR beyond the power supply rails by combining both the NMOS and PMOS input pairs differential amplifiers. The circuit utilized folded-cascode load to increase the output impedance. Figure 4.25 shows the biasing circuit, which generates the four biasing voltages for the wide-swing folded-cascode OTA.



4.29 Biasing Circuit for Wide Swing OTA

The wide-swing characteristic is simulated by applying input ranging from –3.5v to 3.5v with power rails of –2V and 2V.The wide swing characteristic is important when designing filter circuit with high Q in cascaded filter implementation, where the output of one stage is the input of the next stage. The high Q stage could easily drive the output voltage beyond the power rails.

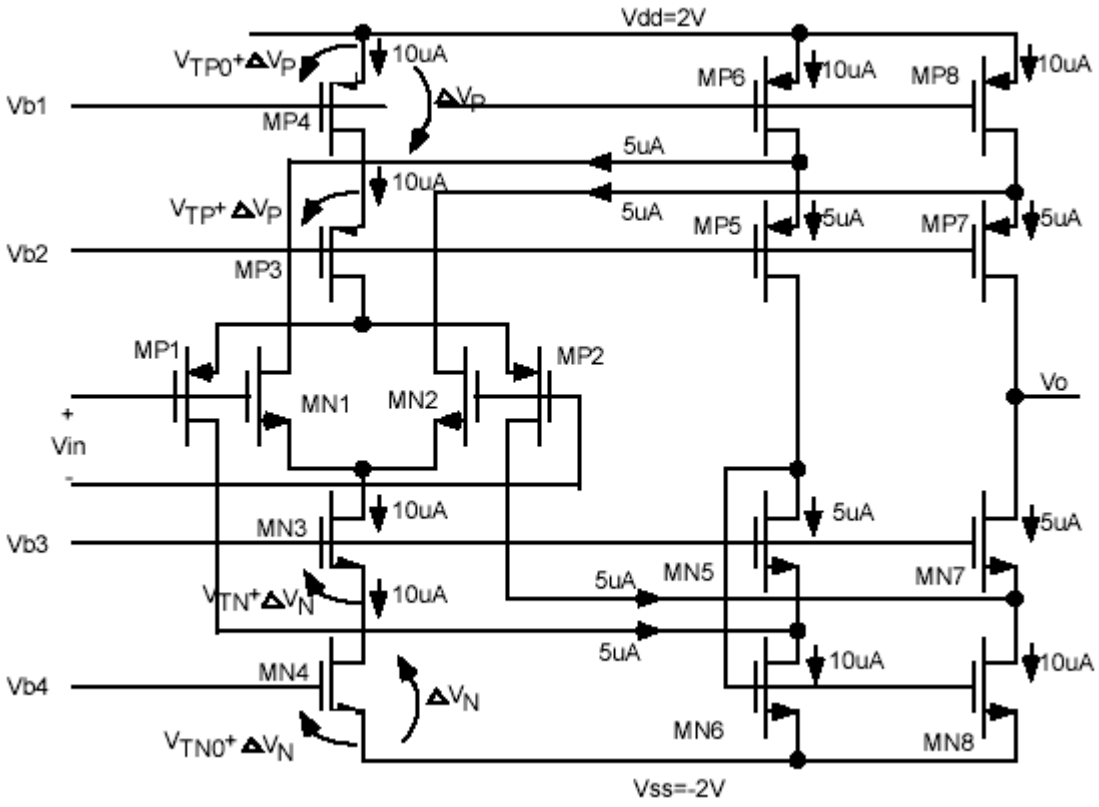


Fig: 4.30 Wide Swing Folded cascaded OTA

The goal of the biasing circuit shown in Figure 4.25 is to generate the biasing voltages needed by the OTA circuit shown in Figure 4.26 so that the gate to source voltages of the four transistors MN3, MN4, MP3, MP4 are as shown to generate the same current. That is,

$$I_D(N3) = I_D(N4) = -I_D(P3) = -I_D(P4)$$

----------(4.18)

$$V_{TH} + \Delta V_N = V_{TN0} + \Delta V_N = -(V_{TP} + \Delta V_P) = -(V_{TP0} + \Delta V_P)$$

----------(4.19)

$$\Delta V_N = -\Delta V_P \text{ and } V_{TN0} = -V_{TP0}$$

----------(4.20)

Transistor MN3 and MP3 both have non-zero bulk to source voltage. Hence their threshold voltages increase. These values are computed as follows:

$$V_{BS}(P3) = V_B(P3) - V_S(P3) = V_{DD} - (V_{DD} + \Delta V_P) = -\Delta V_P$$

$$V_{TN} = V_{TN0} + \gamma\sqrt{\phi - V_{BS}} - \sqrt{\phi} = V_{TN0} + \gamma\sqrt{\phi + \Delta V_N} - \sqrt{\phi} = 1 + \sqrt{0.6 + 0.34} - \sqrt{0.6} = 1.195$$

$$V_{BS}(P3) = V_B(P3) - V_S(P3) = V_{DD} - (V_{DD} + \Delta V_P) = -\Delta V_P$$

$$V_{TP} = V_{TP0} + \gamma\sqrt{\phi + V_{BS}} - \sqrt{\phi} = V_{TP0} + \gamma\sqrt{\phi - \Delta V_P} - \sqrt{\phi} = -1 + \sqrt{0.6 + 0.34} - \sqrt{0.6} = -1.19$$

The Value of Biasing Voltage can Calculated from OTA circuit

$$\begin{aligned} V_{B4} &= V_{TN} + V_{SS} + \Delta V_N = -1.16 \\ V_{B3} &= V_{TN} + 2(\Delta V_N) + V_{SS} = -0.625 \\ V_{B2} &= V_{TP} + 2(\Delta V_P) + V_{DD} = 0.82 \\ V_{B1} &= V_{TP} + (\Delta V_P) + V_{DD} = 1.36 \end{aligned}$$

----------(4.21)

The biasing circuit must determine the value of the divisor n to achieve the desired biasing voltages. $\mathbf{V_{b4}}$ and $\mathbf{V_{b1}}$ are satisfied by selecting the same transistor size as that of the OTA circuit. For $\mathbf{V_{b3}}$ and $\mathbf{V_{b2}}$, the value of n must be determined to achieve the biasing voltages. The voltage on the biasing circuit side is determined and equated to the corresponding required OTA bias voltage. This is illustrated as follows:

$$V_{b3} = V_{TN0} + \Delta V_N + V_{SS} + V_{TN} + \sqrt{n} + \Delta V_N - (V_{TN} + \Delta V_N) = V_{TN0} + V_{SS} + \sqrt{n}\Delta V_N$$

Equating with corresponding equation, we get

$$V_{TN0} + V_{SS} + \sqrt{n}\Delta V_N = V_{TN0} + V_{SS} + 2\sqrt{n}\Delta V_N$$

$$(\sqrt{n} - 2)\Delta V_N = V_{TN} - V_{TN0}$$

$$n = \left\{ \frac{V_{TN} - V_{TN0}}{\Delta V_N} + 2 \right\}^2 = \left\{ \frac{1.195 - 1}{0.34} + 2 \right\}^2 = 6.62 \cong 7$$

Similarly V_{b2} on both side are equated to obtain n

$$V_{DD} + v_{TP0} + \sqrt{n}\Delta V_P = V_{DD} + V_{TP} + 2(\Delta V_P)$$
$$(\sqrt{n} - 2)\Delta V_P = V_{TP} - V_{TP0}$$

$$n = \left\{ \frac{V_{TP} - V_{TP0}}{\Delta V_P} + 2 \right\}^2 = \left\{ \frac{-1.195 - (-1)}{-0.34} + 2 \right\}^2 = 6.62 \cong 7$$

4.16 Gain Calculation of Wide Swing Folded Cascoded OTA

$$\lambda = \lambda_N = \lambda_P = 0.02$$

$$R_{DS}(P7) = R_{DS}(N7) = \frac{1}{\lambda I_{DSQ7}} = \frac{1}{(0.02)(5E-6)} = 10E6$$

$$R_{DS}(P8) = R_{DS}(N8) = \frac{1}{\lambda I_{DSQ8}} = \frac{1}{(0.02)(105E-6)} = 5E6$$

$$g_m(N1) = g_m(N7) = \sqrt{2\beta I_{DSQ}} = \sqrt{2K_N \frac{W_N}{L_N} I_{DSQ}} = \sqrt{2(40E-6)\frac{10.6(5E-6)}{0.35}} = 40.38E-6$$

$$g_m(P1) = g_m(P7) = \sqrt{2\beta I_{DSQ}} = \sqrt{2K_P \frac{W_P}{L_P} I_{DSQ}} = \sqrt{2(15E-6)\frac{32.4(5E-6)}{0.35}} = 43.23E-6$$

$$R_{ON} = g_m(N7)R_{DS}(N7)R_{DS}(N8) = (37.947E-6)(10E6)(5E6) = 2.1245E6$$

$$R_{OP} = g_m(p7)R_{DS}(P7)R_{DS}(P8) = (4.249E)(10E6)(5E6) = 1.895E6$$

$$R_0 = \left[\frac{R_{ON}R_{OP}}{R_{ON}+R_{OP}}\right] = 1.19E9$$

$$g_m = g_m(N1) + g_m(P1) = (40.38E-6) + (42.23E-6)$$

----------(4.22)

$$A_V = g_m R_o = (83.61E-6)(1.19E9) = 9.9E4$$

----------(4.23)

4.17 Simulation Result for Wide Swing Folded cascode OTA

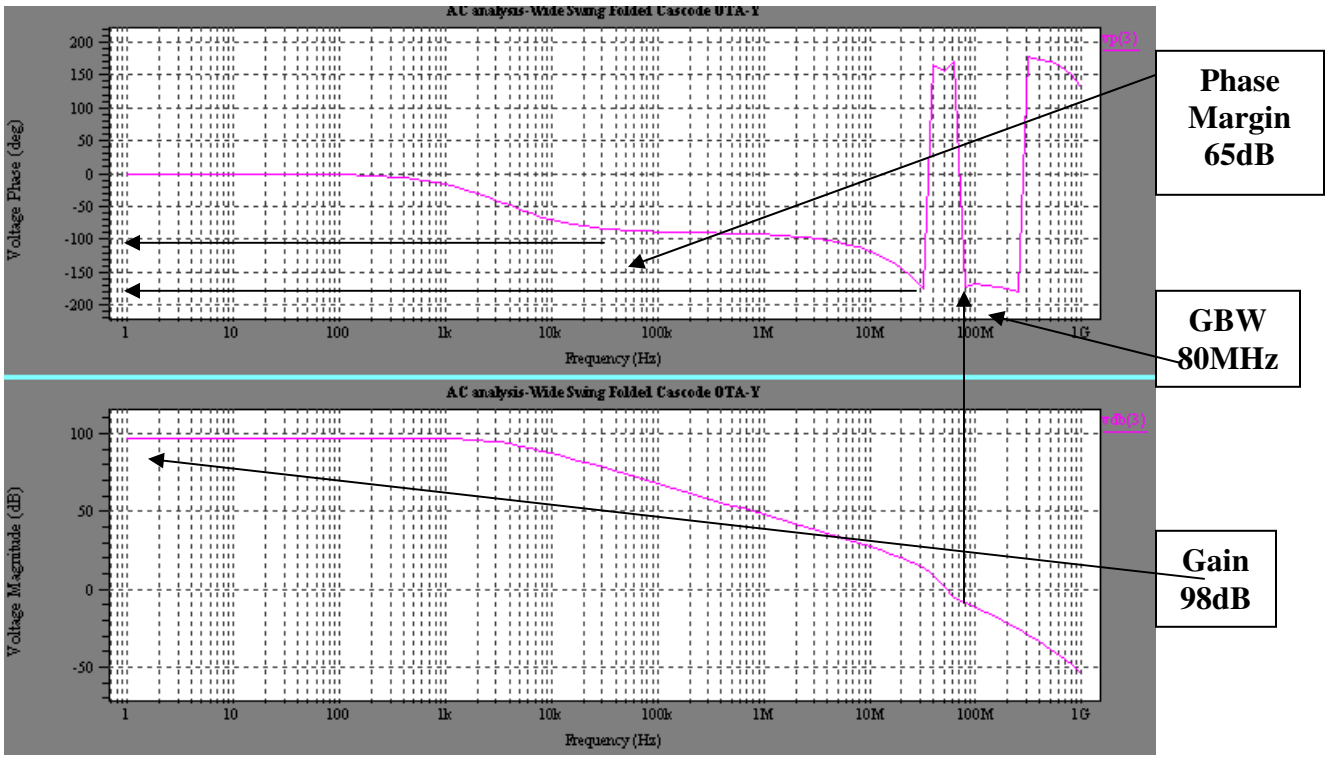


Fig:4.31 Simulation Result for Wide Swing Folded Cascode OTA

(Gain, GBW and Phase Margin)

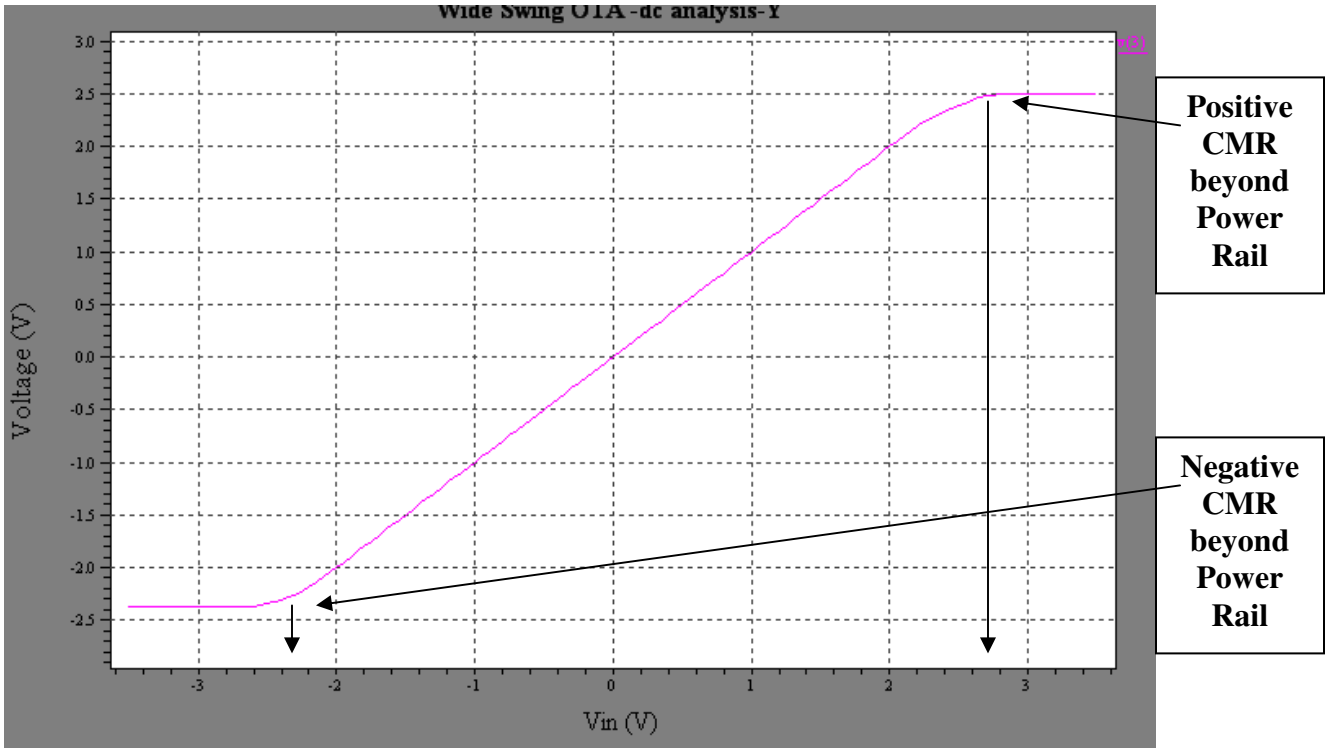


Fig: 4.32 DC Analysis for Wide Swing Folded Cascode OTA

"Wide Swing Folded Cascoded OTA" is Simulated and the result shown below are very closed to the theoretical value.

$$\frac{V(3)}{V_{in}} = 9.3E4 = A_V$$

$$G_m = \frac{A_V}{R_o} = 85.44\mu$$

Internal node voltages of Wide Swing Folded Cascode OTA are shown below:

Node	Voltage
3	-1.156
M1	1.488
M2	-1.05
M3	1.44
N1	2.08
N2	2.08
N3	-1.65
N4	1.15
N5	-2.12
N6	-2.12
N7	-2.19
N8	1.51
N9	2.15
In+	0.00
In-	0.00
Vb1	1.17
Vb2	0.71
Vb3	-0.67
Vb4	-1.15
Vdd	+2V
Vss	-2V

Table 4.5-Measured Node Voltage

The Calculated Biasing voltage value and Measured biasing voltages are compared in the following table:

Biasing Voltage	Calculated Biasing voltage	Measured biasing voltages
Vb1	1.16V	1.17V
Vb2	0.82V	0.71V
Vb3	-0.62V	-0.67V
Vb4	-1.16V	-1.15V

Table 4.6 Calculated and Measured Biasing Voltage

4.18 Physical Design of Wide Swing Folded Cascode OTA

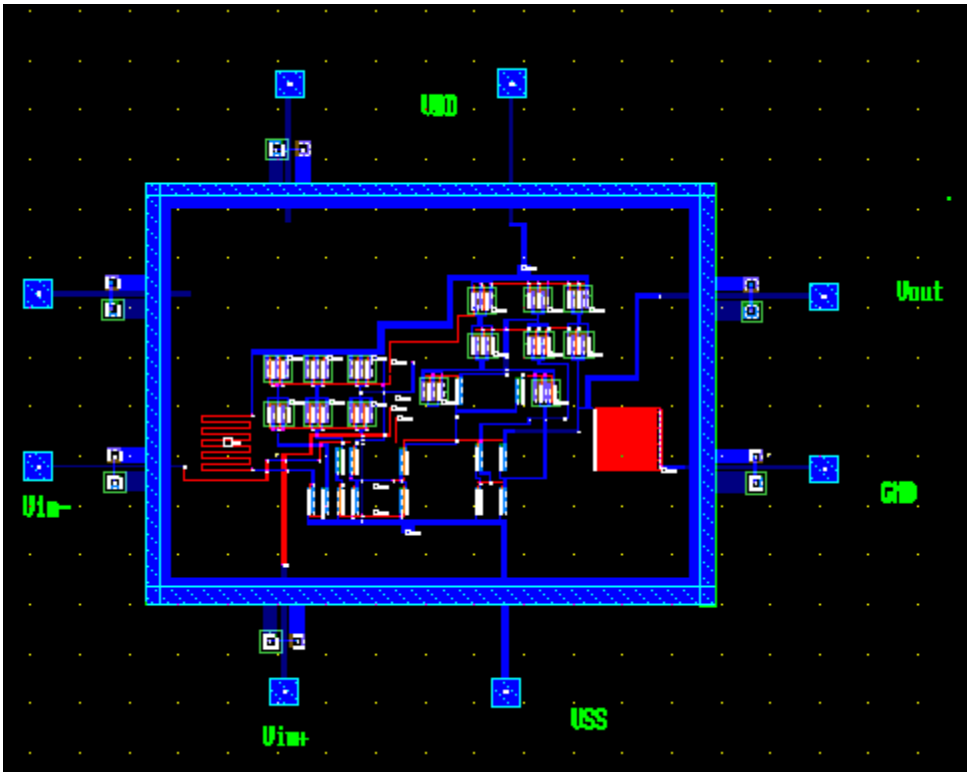


Fig:4.33 Physical Design of Wide Swing Folded Cascode OTA

Chapter 5

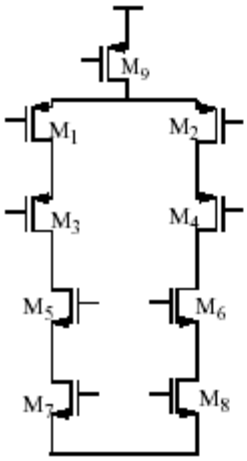
Noise in Telescopic and Folded Cascode OTA

Noise limits the minimum signal level that a circuit can process with acceptable quality. Today's analog designers constantly deal with the problem of noise because it trades with power dissipation, speed and linearity. Real circuits are never immune from small," random" fluctuations in voltage and current levels. In T-Spice, the influence of noise in a circuit can be simulated and reported in conjunction with AC analysis. The purpose of noise analysis is to compute the effect of the noise associated with various circuit devices on an output voltage or voltage as a function of frequency.

Noise analysis is performed in conjunction with AC analysis; if the .ac command is missing, then the. Noise command is ignored. With the .ac command present, the. Noise command causes Noise models take the form of frequency dependent mean-square currents generate by adding a current source to the circuit for each modeled noise source. Noise sources at different points in the circuit are uncorrelated. Noise models are available for resistors and semiconductor devices (diodes, BJTs, JFETs, MOSFETs and MESFETs). Semiconductor device models may contain noise model parameters, which affect the size of noise sources. External model devices may also contain noise sources. Noise analysis results can be reported with the. Print noise command.

5.1 Noise Contribution

Operational Transconductance Amplifier can be designed using either a telescopic or folded cascode topology, shown in Figure 5.1 The topology with lower power consumption and lower noise should be chosen for this design. There are four current legs between Vdd and ground in the folded cascode topology while there are only two current legs in the telescopic amplifier. This implies that the telescopic amplifier consumes less static power.



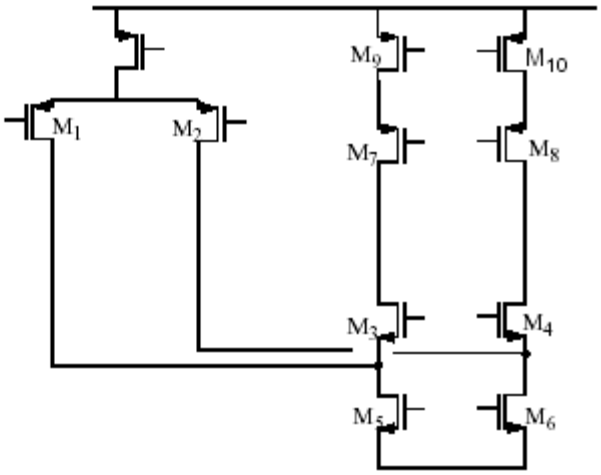


Fig:5.1(a) Telescopic **Fig: 5.1(b) Folded Cascode**

From a noise perspective, the folded-cascode amplifier has six noise contributing devices—M_1, M_2, M_5, M_6, M_9, M_{10}. It can be shown that the cascode devices (M_3, M_4, M_7, M_8) contribute negligible noise to the amplifiers. In the telescopic amplifier, only four transistors—M_1, M_2, M_7, M_8 contribute significant noise. Because the telescopic amplifier has fewer current legs and fewer noise-contributing device.

Flicker noise is also an important design consideration. Caused by the charge and discharge of oxide traps at the silicon-silicon dioxide surface, the flicker noise from PMOS devices is about three times lower than NMOS devices because of speed of the PMOS carriers. The input devices of both the telescopic and folded-cascode amplifier are thus chosen to be PMOS to lower flicker noise.

The telescopic topology has fewer noise contributing devices, so it is a better candidate for low noise single stage OTA. The total output noise in the circuit is dominated by the input devices (M1, M2-Fig: 3.1) and the active loads at the top of the cascade (M7,M8-Fig:3.1). The noise contribution from cascade devices is negligible .The principle noise sources in the MOSFET are thermal noise and flicker noise generated in the channel. The relations between the flicker noise and the MOSFET geometry and bias conditions depend on the fabrication process. In most cases, the flicker noise, when referred to the input, is independent of the bias voltage and current and is inversely proportional to the product of the act.

5.2 TYPES OF NOISE

Two different types of noise corrupt analog signals processed by integrated circuits: Device Noise and " Environmental" Noise. The latter refers to random disturbances that a circuit experiences through the supply or ground lines or through the substrate.

5.2.1 THERMAL NOISE

RESISTOR THERMAL NOISE-The random motion of electrons in a conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. Thus, the spectrum of thermal noise is proportional to the absolute temperature.

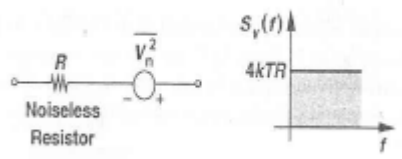


Fig:5.2 Thermal noise of a resistor

As shown in Fig.5.2, the thermal noise of a resistor *R* can be modeled by a series voltage source, with the one-sided spectral density

$$S_V(f) = 4KTR \text{ ----------(5.1)}$$

For $f \geq 0$

Where k=1.38*10 ^{23} – J/K is the Boltzmann constant. The above equation suggests that hermal noise is white .In reality; $S_V(f)$ is flat for up to roughly 100 THz, dropping at higher frequencies.

5.2.2 FLICKER NOISE

The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since the silicon crystal reaches an end at this interface, many dangling" bonds appear, giving rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing " flicker" noise in the drain current. In addition to trapping, several other mechanisms are believed to generate flicker noise.

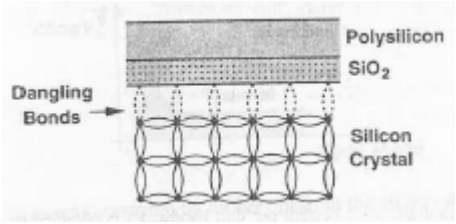


Fig5.3 Dangling bonds at the oxide silicon surface

Unlike thermal noise, the average power of flicker noise cannot be predicted easily. Depending on the " cleanness" of the oxide-silicon interface, Flicker noise may assume considerably different values and as such varies from one CMOS technology to another. The flicker noise is more easily modeled as a voltage source in series with the gate and roughly given by

$$V_n^2 = \frac{k}{C_{ox}WLf} \text{ ----------(4.2)}$$

Where ***K*** is a process –dependent constant on the order of 10^{25} - V^2 F.

The trap-and-release phenomenon associated with the dangling bonds occurs at low frequencies more often. For this reason, flicker noise is also called 1/*f* noise.

The inverse dependence of equation (4.2) on **WL** suggests that to decrease 1/*f* noise, the device area must be increased. It is therefore not surprising to see devices having areas of several thousand square microns in low-noise applications. It is also believed that PMOS devices exhibit less 1/*f* noise than NMOS transistors because the former carry the holes in a " buried channel", i.e., at some distance from the oxide-silicon interface. Nonetheless, this difference between PMOS and NMOS transistors is not consistently observed.

Chapter 6

Filter Design using OTA

6.1 Introduction

Filter design using OTA (Operational Transconductance Amplifier) is the most common method. Biquad, Butterworth, Chebyshev, Bessel and Elliptic filters can be designed easily and efficiently using OTAs. An OTA is a voltage controlled current source (VCCS), more specifically the term “operational” comes from the fact that it takes the difference of two voltages as the input for the current conversion. In addition to the voltage control characteristics, the OTA based circuits show high frequency applications where conventional opamp based circuits become bandwidth limited.

High-speed filters are increasingly based on an Operational Transconductance Amplifiers (OTAs) Capacitor (gm-C) approach, because of their simple circuitry and improved frequency response. However, the nonidealities of the transconductor limit overall filter performance. The performance of OTA-C filters depends on: (I) the OTA circuit, which is the main noise and distortion contributor in the filter, and (II) the OTA-C filter structure.

Programmable high-frequency active filters can be achieved by incorporating the operational Transconductance Amplifier-Capacitor filters (OTA-C). OTA-C filters also have simple structures, and can operate up to several hundreds of MHz.The OTA has been implemented widely in CMOS and bipolar and also in BiCMOS and GaAs technologies. The typical values of transconductances are in the range of tens to hundreds of μS in CMOS and up to mS in bipolar technology. Although OTA-C filters operate at relatively high frequencies (MHz range), the linear signal range of the used transconductance limits the dynamic range. Also the OTA-C filters become very power hungry at GHz range. The Operational Transcondutance Amplifier-Capacitor (OTA-C) technique is a popular technique for implementing high-speed continuous time filters and is widely used in many industrial applications.

To achieve any required cutoff frequency in passive filter, we require different values of resistors & inductors as calculated from mathematical expression. To solve this problem, we can use OTAs. We achieve the required resistance and inductance values by varying its gm.

Passive components are generally the basic building blocks of filters, which work normally on high frequencies; but at audio frequencies inductor causes problem. Inductor size increases ,at audio frequency and become bulky & expensive. At low frequencies inductor requires more number of turns, which adds series resistances and degrades inductor's performance because of its low quality factor (Q), which results in high power dissipation. Using OTA the above mentioned problems are solved.

6.2 OTA FUNDAMENTALS

An ideal operational transconductance amplifier is a voltage-controlled current source, with infinite input and output impedances and constant transconductance.

The OTA has two attractive features:

(1) Changing the external dc bias current or voltage can control its tranconductance, and

(2) It can work at high frequencies.

Fig.6.1 (a) shows a general model of the transconductor cell and Fig. 6.1(b) shows the simple NMOS transistor as the simplest transconductor cell.

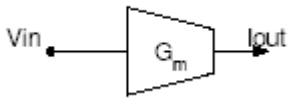


Fig: 6.1(a) Transconductor cell

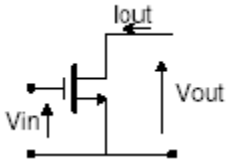


Fig: 6.1(b) Simple MOS cell

The current-voltage relation given by equation (6.1) governs a MOS transistor in the saturation region, neglecting λ effects. The model's output current Iout = i_D, is the total

$$i_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

---------(6.1)

Drain current, which includes the DC and the ac small signal current. The input voltage Vin $= V_{GS}$, also includes the DC voltage (VGS) and the ac component (*vgs*). The remaining terms are μ: the carrier mobility, Cox: the oxide capacitance per unit area of the channel, Vt: the threshold voltage, W and L are the width and length of the channel. The derivative leads to a first order relation between current and voltage, as shown in below equations

$$i_D = g_m V_{gs}$$

$$g_m = f(I_D)$$

----------(6.2)

The term gm is called the transconductance and hence the name transconductor amplifier. The transconductance can be adjusted by the width to length ratio, W/L, of the gate and is proportional to the square root of the bias current I_D. The unit of transconductance is Siemens (S).

The performance of filters designed by the use of passive components degrades at audio frequencies and the required resistances and inductances values calculated from the mathematical expression are very difficult to meet from the market. To find a solution to this problem we have performed Passive Filters into Active Filters using Operational Transconductance Amplifier (OTA). By controlling the Voltage Gain of OTA, one can change its transconductance, which is very useful in the designing the first order and second order active filters.

OTA is a differential voltage controlled current source (VCCS) where the output current is controlled by an applied input voltage signal. To achieve any required cutoff frequency in passive filter, we require different values of resistors & inductors as calculated from mathematical expression. We achieve the required resistance and inductance values by varying its gm. Passive components are generally the basic building blocks of filters, which work normally on high frequencies; but at audio frequencies inductor causes problem. Inductor size increases, at audio frequency and become bulky & expensive. At low frequencies inductor requires more number of turns, which adds series resistances and degrades inductor's performance because of its low quality factor (Q), which results in high power dissipation. Using OTA the above mentioned problems are solved.

The OTA is a transconductance device in which the input voltage controls the output current. The transconductance g_m makes the OTA as voltage controlled current source; where as the op-amps are voltage controlled voltage source. An ideal OTA is defined by $I_0 = g_m(V^+ - V^-)$. Where input & output impedances are infinite. The transconductace g_m is directly proportional to control bias current I_b.

- **Characteristics of Ideal OTA can be summarized as follows**
- **Input impedance (Z_{in}) = ∝**
- **Output Impedance (Z_o) = ∝**
- **Inverting input current I_o^- = I_0^+ Non-Inverting input current**
- **Bandwidth = ∝**

The Figures 6.2 & 6.3 shows the basic schematic and equivalent circuit of OTA.

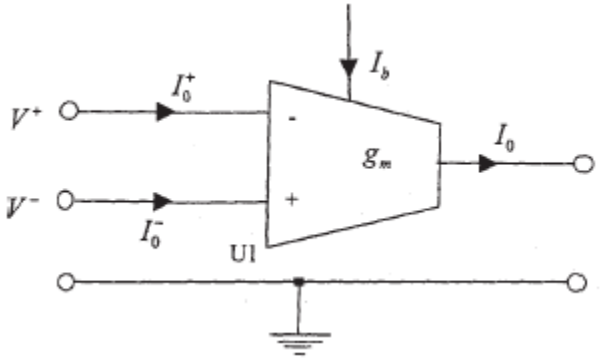


Fig: 6.2 Circuit Symbol of OTA

Fig: 6.3 Small Signal Equivalent Circuit

6.3 BASIC BUILDING BLOCKS USING OTA

The OTA can be used for various applications like simple resistor implementation, an amplifier, a voltage variable resistor, an integrator etc.

6.3.1 Voltage Variable Resistor

A grounded voltage-variable resistor can be easily obtained using the ideal OTA as shown in Fig. 6.4. Since $I_0 = -I_i$

$$Z_i = \frac{V_i}{I_i} = \frac{V_i}{-I_0} = \frac{V_i}{g_m V_i} = \frac{1}{g_m}$$

----------(6.3)

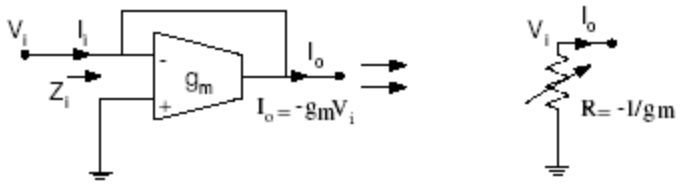


FIG: 6.4 VOLTAGE VARIABLE RESISTOR

Using two such arrangements cross-connected in parallel, a floating VVR can be obtained. On the other hand, if in Fig.6.4 the input terminals are interchanged, the input resistance will be 1/ gm. Thus, using OTAs, both positive and negative resistors become available without actually having to build them on the chip. These, coupled with capacitors, lead to the creation of active-C filters.

6.3.2 Voltage Summation

Voltage summation can be obtained using OTAs, which in effect translate voltages to currents. These are easily summed as shown in Fig. 6.5 for two voltages V_1 and V_2. it is clear that from (6.4), (6.5) and (6.6), V_o a function of V_1 and V_2 . By adjusting the values of the transconductances, a voltage summer can be obtained. By changing the grounded input of one of the input OTAs, voltage subtraction can be achieved. These operations are useful for the realization of transfer functions.

$$I_{01} + I_{02} + I_0 = 0$$

----------(6.4)

$$g_{m1}V_1 + g_{m2}V_2 - g_{m0}V_0 = 0$$

----------(6.5)

$$V_o = \frac{g_{m1}}{g_{m0}}V_1 + \frac{g_{m2}}{g_{m0}}V_2$$

----------(6.6)

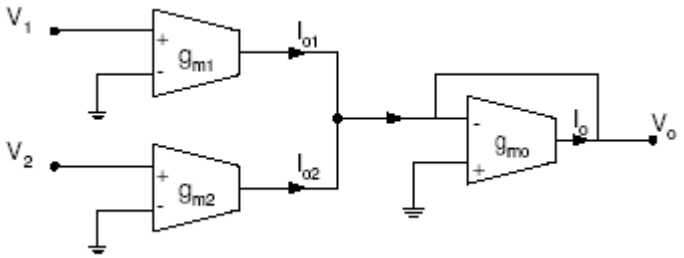


Fig: 6.5 Voltage summation

6.3.3 Voltage Amplifier / Integrator

Inverting and non-inverting voltage amplification and also integration can be achieved using an OTA. Fig. 6.6 shows the simple OTA with a load. If Z_L is a passive resistor R_L, then the structure behaves like a voltage amplifier and depending on the polarity of the input the voltage amplifier could be a positive or negative one. Any desired gain can be achieved by a proper choice of g_m and R_L. It should be noted that the output voltage V_o is obtained from a source with output impedance equal to R_L.

If the load is a capacitor C, the structure behaves like a first order integrator. Zero output impedance can be achieved only if a buffer or voltage follower follows such circuits.

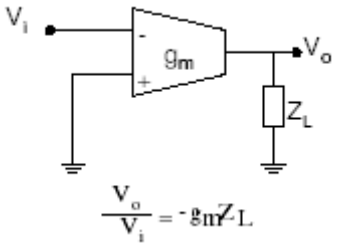


Fig: 6.6 OTA with load

6.3.4 Integrator

The operation of integration can be achieved using the OTA as is shown in Fig. 6.7. Clearly, It follows that both inverting and noninverting integration is easily achieved.

$$V_0 = \frac{I_0}{sC} = \frac{g_m}{sC}(V_1 - V_2)$$

----------(6.7)

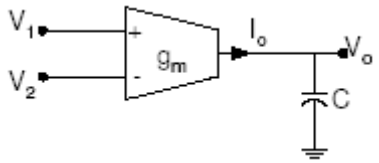


Fig: 6.7 First Order Integrator

6.4 OTA-C FILTERS FROM PASSIVE FILTERS

First order low pass filter

1. Passive Filter

Consider a first order low pass filter as shown in fig. 6.8 below.

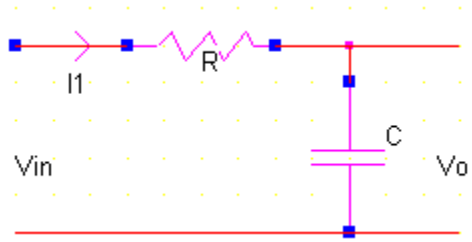


Fig: 6.8 First Order Low Pass Filter (Passive Filter)

$$V_{in} = I_1\left\{R + \frac{1}{SC}\right\}$$

----------(6.8)

$$V_0 = \frac{I_1}{SC}$$

----------(6.9)

$$\frac{V_o}{V_{in}} = \frac{\frac{1}{CR}}{\frac{1}{CR} + S}$$

---------(6.10)

Realization Using OTAs

From fig.6.9 we get

$$I_1 = g_m(V_{in} - V_0)$$

----------(6.11)

From equation (6.11) and equation (6.9), the transfer function for considered filter is

$$T_{(s)} = \frac{\frac{g_m}{C}}{\frac{g_m}{C} + S}$$

----------(6.12)

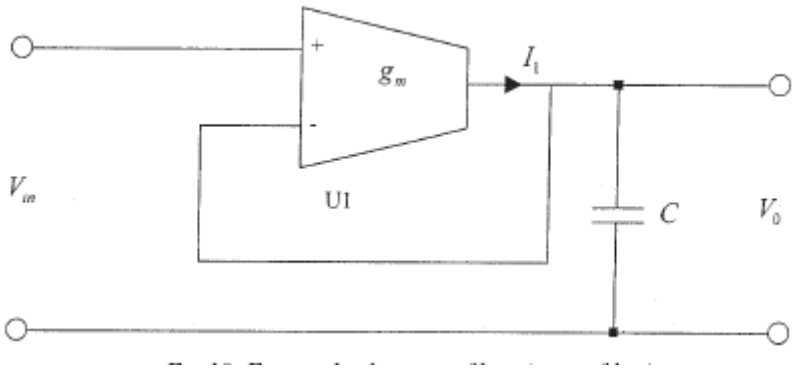


Fig: 6.9 first order Low Pass Filter (Active Filter)

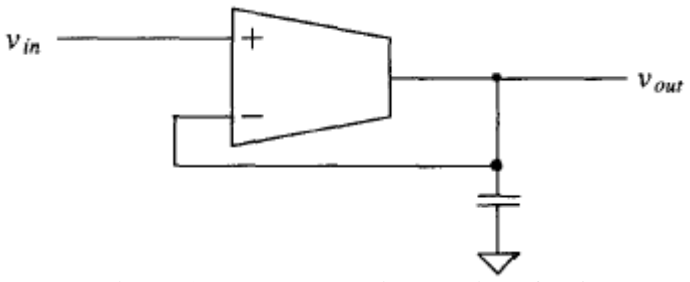


Fig: 6.10 Low Pass Filter using OTA

The Current out of OTA is given by:

$$I_{out} = g_m(V_{in} - v_{out})$$

----------(6.13)

The output voltage is given by:

$$V_{out} = \frac{g_m}{j\omega C}(V_{in} - V_{out})$$

----------(6.14)

The transfer function of the circuit is given by:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\omega C\dfrac{1}{g_m}}$$

----------(6.15)

The circuit of Fig.6.10 performs the function as a simple low-pass single-time constant filter with a capacitor value of C and a resistor value of 1/ $\mathbf{g_m}$. The major advantage of this circuit is that the source, V_{in} sees the input impedance of the OTA, which is practically infinite. A high-pass OTA circuit is shown in Fig. 6.11. The transfer function of the circuit is given by

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{j\omega C}{g_m}}{\dfrac{j\omega C}{g_m} + 1}$$

----------(6.16)

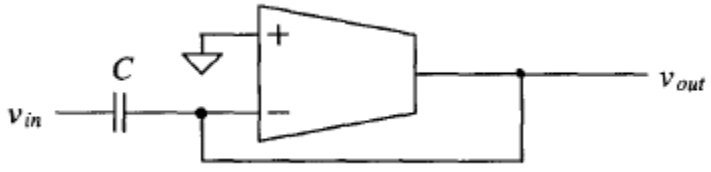


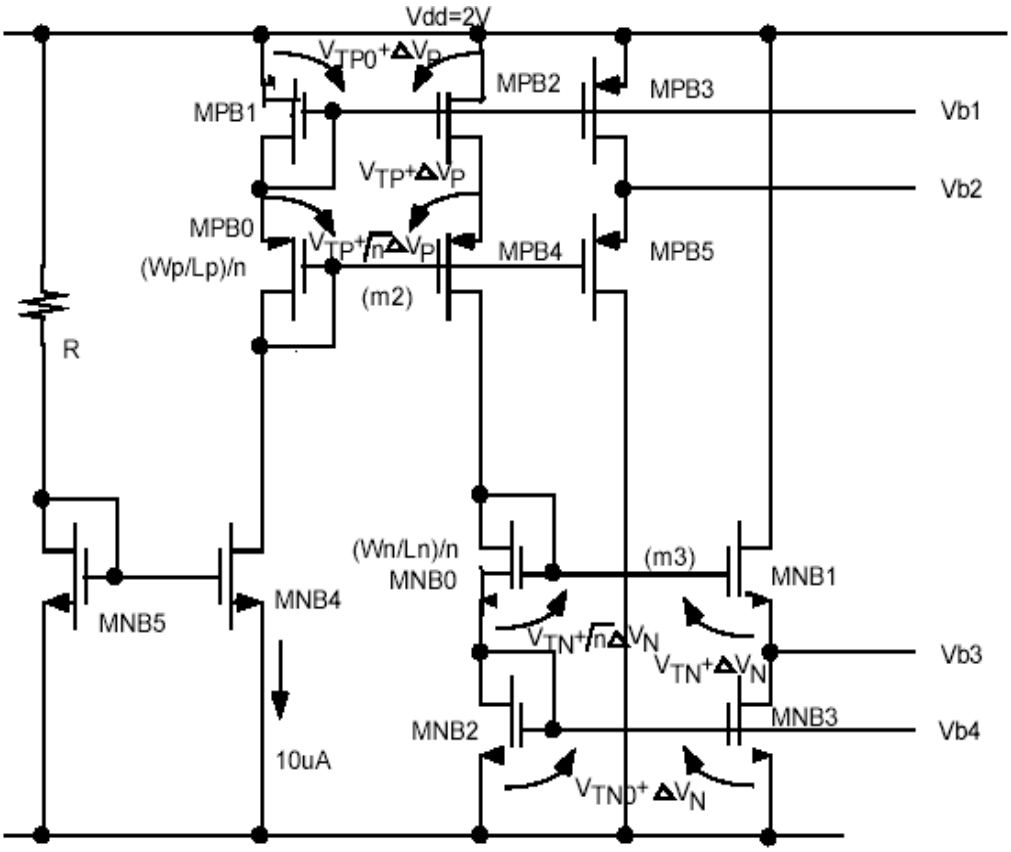
Fig: 6.11 High Pass Filter using OTA

6.5 Wide Swing Folded Cascoded OTA

Two practical concerns when designing an OTA for filter applications are the input signal amplitude and the parasitic input/output capacitances. Large signals cause the OTA gain to become nonlinear. The external capacitance should be large compared to the input/output parasitic of the OTA. This limits the maximum frequency of a filter built with an OTA and causes amplitude or phase errors. The errors can usually be tuned out with proper selection of $\mathbf{I_{bias}}$

Figure 6.13 shows a "Wide-swing Folded Cascoded OTA" which extends the input CMR beyond the power supply rails by combining both the NMOS and PMOS input pairs differential amplifiers. The circuit utilized folded-cascode load to increase the output impedance. Figure 6.12 shows the biasing circuit which generates the four biasing voltages for the wide-swing folded-cascode OTA.

The wide-swing characteristic is simulated by applying input ranging from –3.5v to 3.5v with a power rail of –2V and 2V.The wide swing characteristic is important when designing filter circuit with high Q in cascaded filter implementation, where the output of one stage is the input of the next stage. The high Q stage could easily drive the output voltage beyond the power rails.



6.12 Biasing Circuit for Wide Swing OTA

Biasing Voltage Calculations

The goal of the biasing circuit shown in Figure 6.12 is to generate the biasing voltages needed by the OTA circuit shown in Figure 6.13 so that the gate to source voltages of the four transistors MN3, MN4, MP3, MP4 are as shown.to generate the same current. That is,

Transistor MN3 and MP3 both have non-zero bulk to source voltage. Hence their threshold voltages increase. These values are computed as follows:

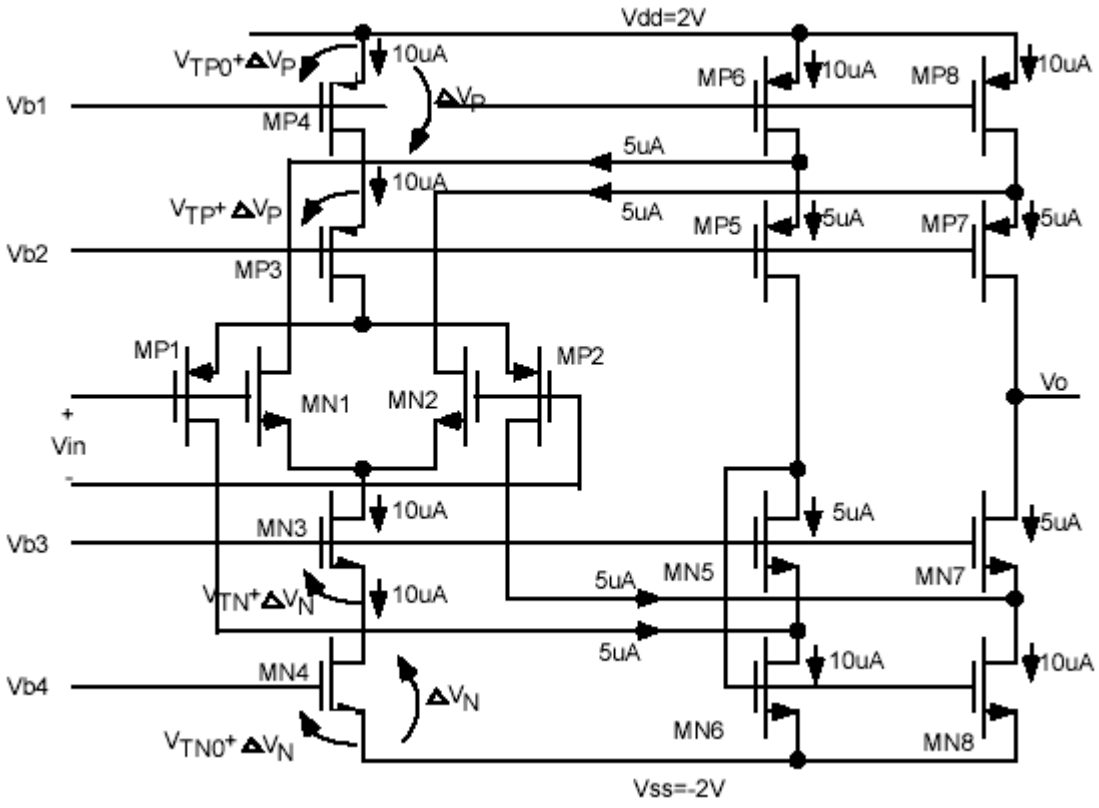


Fig: 6.13 Wide Swing Folded cascaded OTA

$$I_D(N3) = I_D(N4) = -I_D(P3) = -I_D(P4)$$

----------(6.17)

$$V_{TH} + \Delta V_N = V_{TN0} + \Delta V_N = -(V_{TP} + \Delta V_P) = -(V_{TP0} + \Delta V_P)$$

----------(6.18)

$$\Delta V_N = -\Delta V_P \text{ and } V_{TN0} = -V_{TP0}$$

----------(6.19)

Transistor MN3 and MP3 both have non-zero bulk to source voltage. Hence their threshold voltages increase. These values are computed as follows:

$$V_{BS}(P3) = V_B(P3) - V_S(P3) = V_{DD} - (V_{DD} + \Delta V_P) = -\Delta V_P$$

$$V_{TN} = V_{TN0} + \gamma\sqrt{\phi - V_{BS}} - \sqrt{\phi} = V_{TN0} + \gamma\sqrt{\phi + \Delta V_N} - \sqrt{\phi} = 1 + \sqrt{0.6 + 0.34} - \sqrt{0.6} = 1.195$$

$$V_{BS}(P3) = V_B(P3) - V_S(P3) = V_{DD} - (V_{DD} + \Delta V_P) = -\Delta V_P$$

$$V_{TP} = V_{TP0} + \gamma\sqrt{\phi + V_{BS}} - \sqrt{\phi} = V_{TP0} + \gamma\sqrt{\phi - \Delta V_P} - \sqrt{\phi} = -1 + \sqrt{0.6 + 0.34} - \sqrt{0.6} = -1.19$$

The Value of Biasing Voltage can Calculated from OTA circuit

$$\begin{aligned} V_{B4} &= V_{TN} + V_{SS} + \Delta V_N = -1.16 \\ V_{B3} &= V_{TN} + 2(\Delta V_N) + V_{SS} = -0.625 \\ V_{B2} &= V_{TP} + 2(\Delta V_P) + V_{DD} = 0.82 \\ V_{B1} &= V_{TP} + (\Delta V_P) + V_{DD} = 1.36 \end{aligned}$$

----------(6.20)

The biasing circuit must determine the value of the divisor n to achieve the desired biasing voltages. $\mathbf{V_{b4}}$ and $\mathbf{V_{b1}}$ are satisfied by selecting the same transistor size as that of the OTA circuit. For $\mathbf{V_{b3}}$ and $\mathbf{V_{b2}}$, the value of n must be determined to achieve the biasing voltages. The voltage on the biasing circuit side is determined and equated to the corresponding required OTA bias voltage. This is illustrated as follows:

$$V_{b3} = V_{TN0} + \Delta V_N + V_{SS} + V_{TN} + \sqrt{n} + \Delta V_N - (V_{TN} + \Delta V_N) = V_{TN0} + V_{SS} + \sqrt{n}\Delta V_N$$

Equating with corresponding equation, we get

$$V_{TN0} + V_{SS} + \sqrt{n}\Delta V_N = V_{TN0} + V_{SS} + 2\sqrt{n}\Delta V_N$$

$$(\sqrt{n} - 2)\Delta V_N = V_{TN} - V_{TN0}$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{j\omega C}{g_m}}{\frac{j\omega C}{g_m}+1} \quad n = \left\{\frac{V_{TN} - V_{TN0}}{\Delta V_N} + 2\right\}^2 = \left\{\frac{1.195-1}{0.34} + 2\right\}^2 = 6.62 \cong 7$$

Similarly V_{b2} on both side are equated to obtain n

$$V_{DD} + v_{TP0} + \sqrt{n}\Delta V_P = V_{DD} + V_{TP} + 2(\Delta V_P)$$
$$(\sqrt{n} - 2)\Delta V_P = V_{TP} - V_{TP0}$$

$$n = \left\{\frac{V_{TP} - V_{TP0}}{\Delta V_P} + 2\right\}^2 = \left\{\frac{-1.195-(-1)}{-0.34} + 2\right\}^2 = 6.62 \cong 7$$

Gain Calculation of Wide Swing Folded Cascoded OTA

$$\lambda = \lambda_N = \lambda_P = 0.02$$

$$R_{DS}(P7) = R_{DS}(N7) = \frac{1}{\lambda I_{DSQ7}} = \frac{1}{(0.02)(5E-6)} = 10E6$$

$$R_{DS}(P8) = R_{DS}(N8) = \frac{1}{\lambda I_{DSQ8}} = \frac{1}{(0.02)(105E-6)} = 5E6$$

$$g_m(N1) = g_m(N7) = \sqrt{2\beta I_{DSQ}} = \sqrt{2K_N \frac{W_N}{L_N} I_{DSQ}} = \sqrt{2(40E-6)\frac{10.6(5E-6)}{0.35}} = 40.38E-6$$

$$g_m(P1) = g_m(P7) = \sqrt{2\beta I_{DSQ}} = \sqrt{2K_P \frac{W_P}{L_P} I_{DSQ}} = \sqrt{2(15E-6)\frac{32.4(5E-6)}{0.35}} = 43.23E-6$$

$$R_{ON} = g_m(N7)R_{DS}(N7)R_{DS}(N8) = (37.947E-6)(10E6)(5E6) = 2.1245E6$$

$$R_{OP} = g_m(p7)R_{DS}(P7)R_{DS}(P8) = (4.249E)(10E6)(5E6) = 1.895E6$$

$$R_0 = \left[\frac{R_{ON}R_{OP}}{R_{ON}+R_{OP}}\right] = 1.19E9$$

$$g_m = g_m(N1) + g_m(P1) = (40.38E-6) + (42.23E-6)$$

----------(6.21)

$$A_V = g_m R_o = (83.61E-6)(1.19E9) = 9.9E4$$

----------(6.22)

6.6 Biquad filter Implementation using Wide Swing Folded Cascode

Figure 6.14shows a Biquad Filter (2nd order) implementation using wide swing folded cascode OTA which is useful as a low-pass, high-pass, band-pass, or band-reject filter. The Input conditions and filter type are given in Table 6.1.

If we assume that the transconductances of each stage are equal and **f_0= 100K**, then the **Natural frequency of the filter** is given by

$$\omega_0 = \frac{g_m}{\sqrt{C_1 C_2}} \qquad \text{----------(6.23)}$$

While the *Q* of the filter is

$$Q = \sqrt{\frac{C_2}{C_1}} \qquad \text{----------(6.24)}$$

Design Data

Q	**1.6**
C1	**84.78pf**
C2	**216.71pf**

Table 6.1 Design Data for 2nd biquad filter using wide Swing folded Cascode OTA

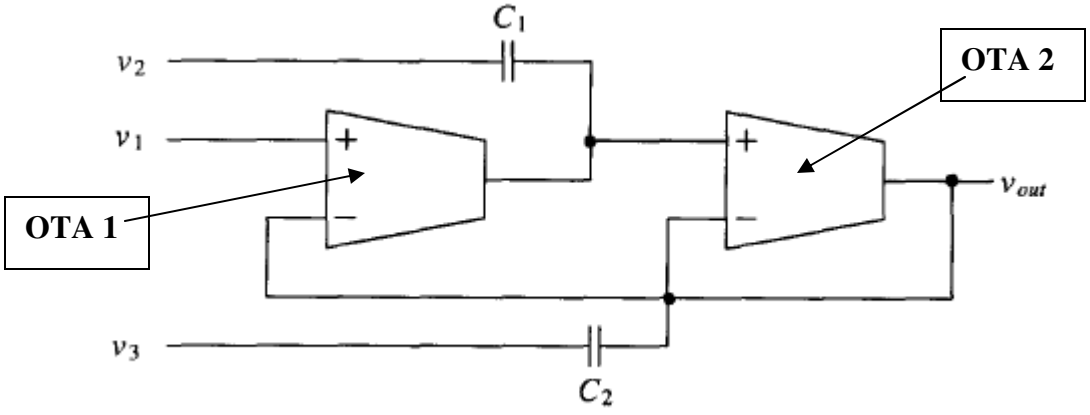


Fig: 6.14 Biquad Filter (2nd Order) Implementation using OTAs Schematic

Filter Type	Input Condition	Transfer Equation
Low Pass Filter	**$V_{in} = V_1$, with V_2 and V_3 grounded**	$\frac{g_m^{\ 2}}{S^2C_1C_2 + SC_1g_m + g_m^{\ 2}}$
High Pass Filter	**$V_{in} = V3$, with V_2 and V_1 grounded**	$\frac{S^2C_1C_2}{S^2C_1C_2 + SC_1g_m + g_m^{\ 2}}$
Band Pass Filter	**$V_{in} = V2$, with V_1 and V_3 grounded**	$\frac{SC_1g_m}{S^2C_1C_2 + SC_1g_m + g_m^{\ 2}}$
Band Stop Filter	**$V_{in} = V_1 = V_3$, with V_2 grounded**	$\frac{S^2C_1C_2 + g_m^{\ 2}}{S^2C_1C_2 + SC_1g_m + g_m^{\ 2}}$

Table 6.2: Design Equations For Biquad Filter (2^{nd} Order)

6.9 Simulation Results for 2nd biquad filter using wide Swing folded Cascode OTA

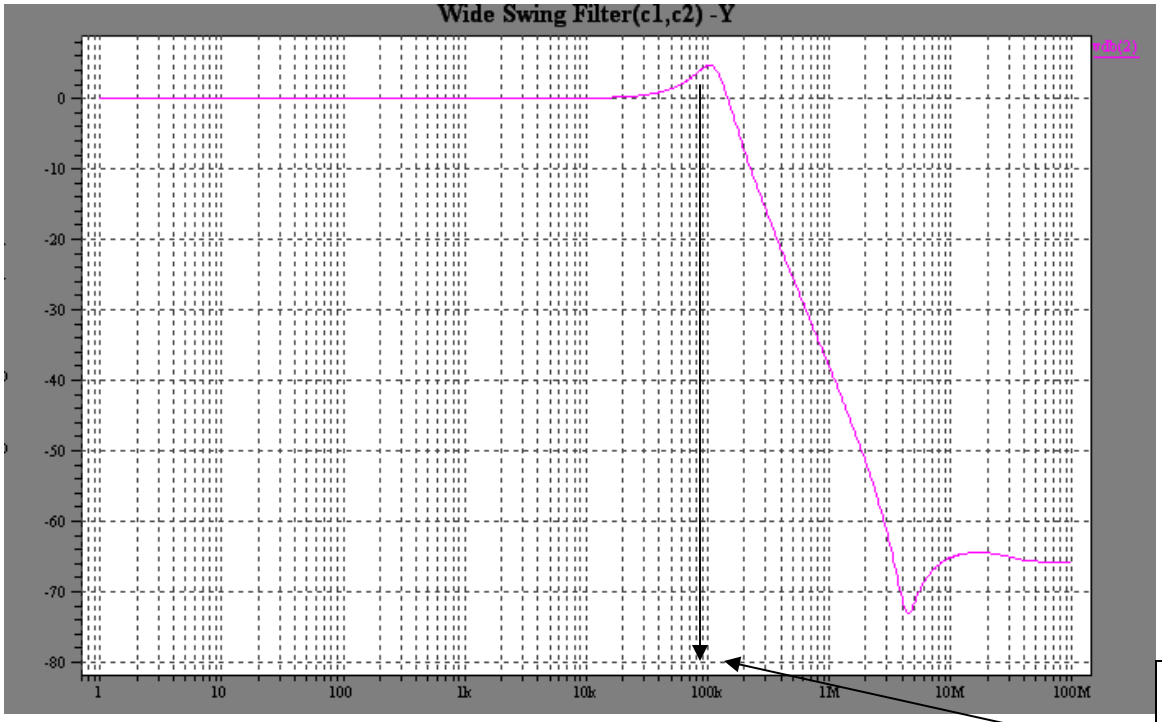


Fig:6.15 Low Pass Filter ($V_{in} = V_1$, with V_2 and V_3 grounded)

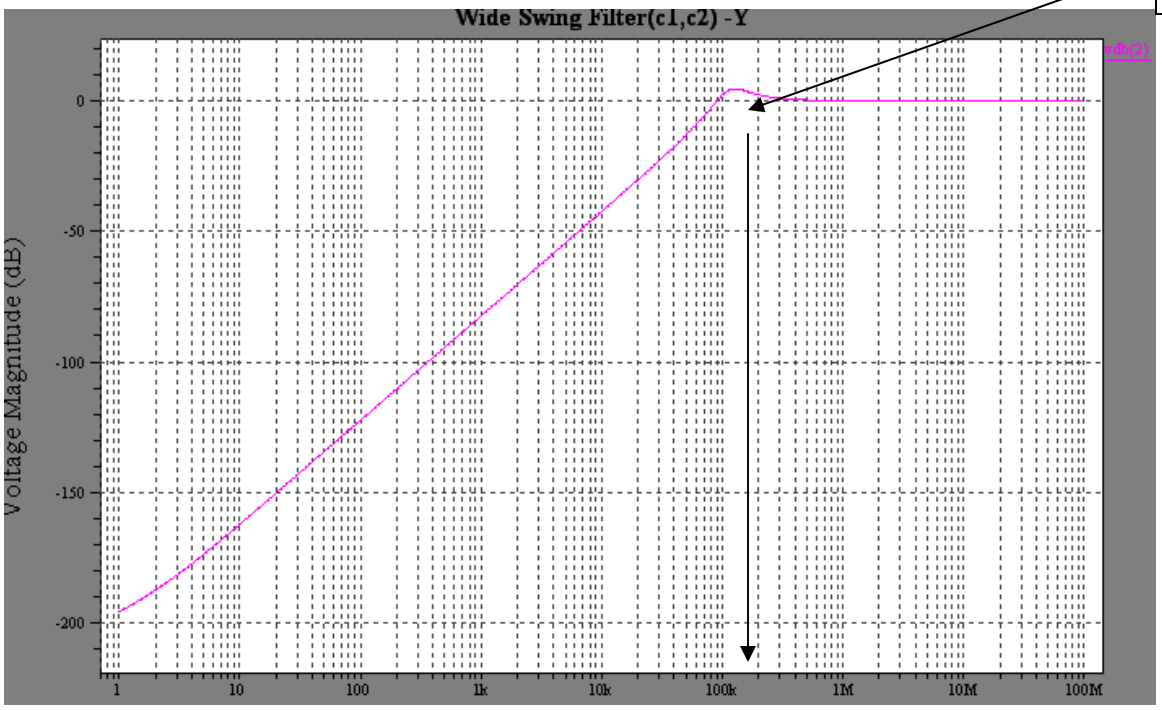


Fig: 6.16 High Pass Filter ($V_{in} = V_3$, with V_2 and V_1 grounded)

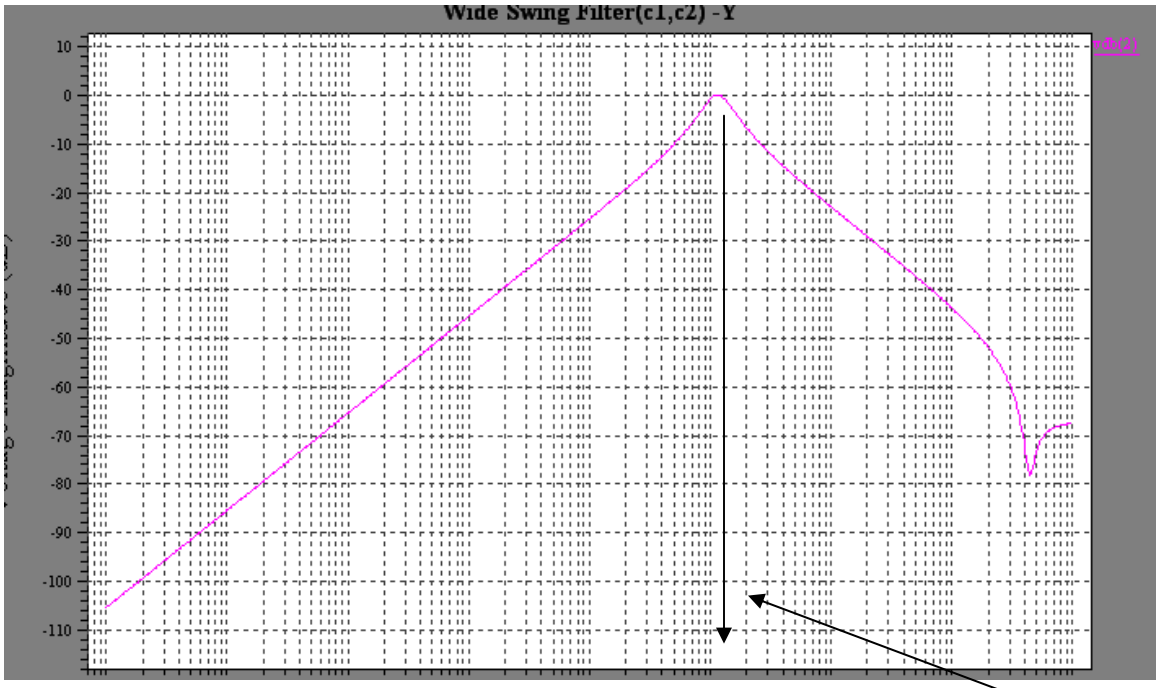
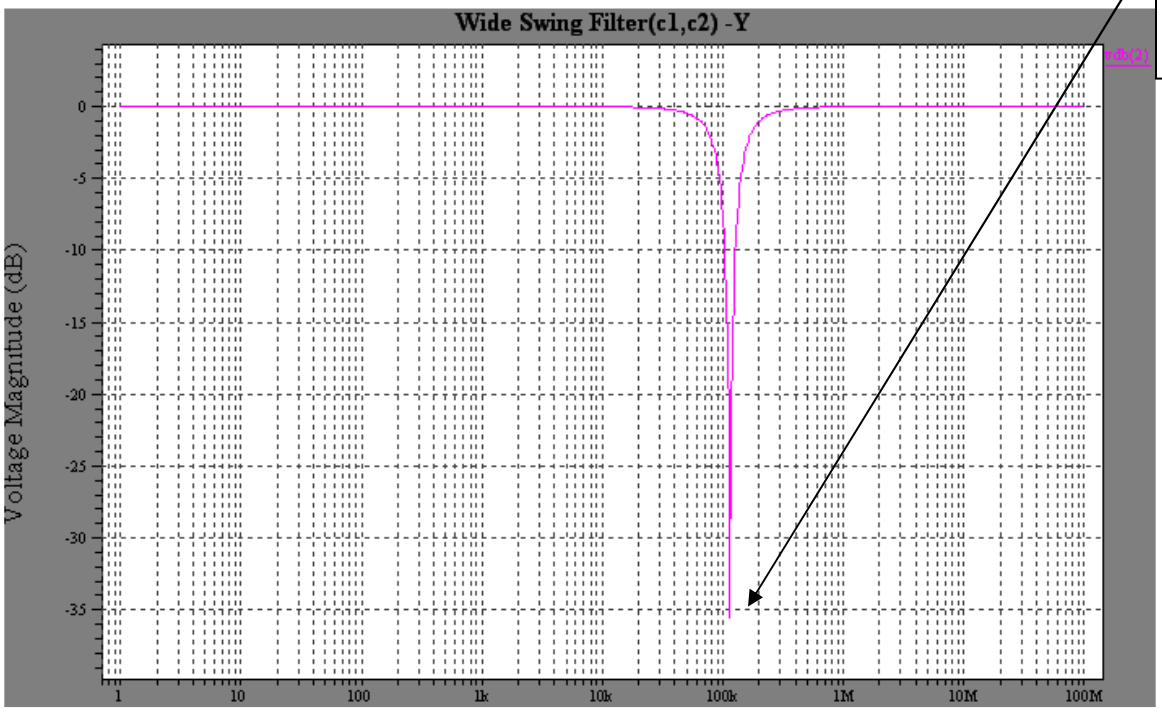


Fig: 6.17 Band Pass Filter ($V_{in} = V_2$, with V_3 and V_1 grounded)



Cut-off Frequency 100K

Fig: 6.18 Band Pass Filter ($V_{in} = V_3 = V_1$ with V_2 grounded)

6.10 Physical Design of 2nd order Biquad Filter

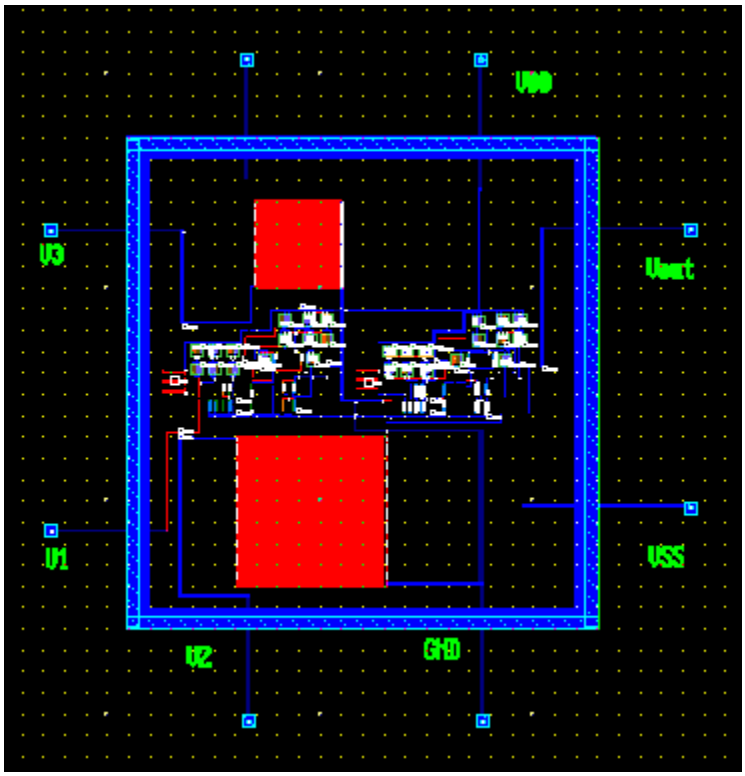


Fig:6.19 Physical Design of 2nd order Biquad Filter

Chapter 7

Conclusion and future Scope

7.1 Conclusions

Designing high performance analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages. The main characteristics under consideration are **High gain, high PSRR; Low offset voltage, high output swing.** Performance of any circuit depends upon these characteristics.

At reduced supply voltages, Telescopic amplifier involving **less power consumption, low noise,** but Telescopic amplifier has the inherent disadvantage of **low output Swing**. Cascode circuits are widely used in circuit design at places where **High gain and High output impedances** are required. Amongst all the topologies of OTA, Folded Cascode OTA is chosen as it allows shorting of input and output terminals with negligible swing limitations."Wide-swing Folded Cascode OTA" which extends the **input CMR beyond the power supply rails** by combining both the NMOS and PMOS input pairs differential amplifiers.

"Filter design using OTA" is the most common method. Programmable high-frequency active filters can be achieved by incorporating the operational Transconductance Amplifier-Capacitor filters (OTA-C). OTA-C filters also have simple structures, and can **operate up to several hundreds of MHz**. OTA-C filter has been designed by replacing all the **passive components in a passive network with an active device**. "Wide Swing Folded cascode OTA" is selected as it suits best because its CMR beyond the power supply rails.

7.2 Future Scope

Many Applications required very low power consumption. Portable apparatuses are powered by small batteries with limited power capacity. **So Designing**

“ Low Power OTA (Wang’s OTA)”

When the bias current in a MOS transistor become very low, the region of operation is no longer in Saturation but it enter in to “Subthresold Region”. Small current determine limited Bandwidth and also lead to small Slew Rate. **So Designing**

“Micro-Power OTA” using any one of the following two method”

- **Dynamic Biasing of the Current Tail and**
- **Dynamic Voltage Biasing in Push-Pull Stage**

Appendix A

BSIM3V3 Level 49 Parameter

MODEL PARAMETER

.MODEL NM1 NMOS LEVEL=49

*Common Extrinsic model parameters

+acm=2 rd=0 rs=0 rsh=8.2e01 rdc=0.0 rsc=0.0 lint=8.3e-09 wint=2.7e-08 ldif=0.0 hdif=6.0e-07 wmlt=1.0 lmlt=1.0 xj=3.0e-07
+js=2.0e-05 jsw=0.0 is=0.0 n=1.0 nds=1000. vnds=-1.0 cj=9.3e-04 cjsw=2.8e-10 fc=0.0 mj=3.1e-01 mjsw=1.9e-01 tt=0.0
+pb=6.9e-01 php=9.4e-01

*Threshold voltage related model parameters

+nch=2.3e+17 vth0=4.6e-01 voff=-5.7e-02 dvt0=2.2e+01 dvt1=1.0 dvt2=3.4e-03 keta=-6.2e-04 k1=6.0e-01 k2=2.9e-03 k3=-1.7
+k3b=6.3e-01 pscbe1=2.7e+08 pscbe2=9.6e-06 dvt0w=0.0 dvt1w=0.0 dvt2w=0.0

*parasitic resistance and capacitance related model parameters

+rdsw=6.0e+02 cdsc=0.0 cdscb=0.0 cdscd=8.4e-05 prwb=0.0 prwg=0.0 cit=1.0e-03
* Flags
+mobmod=1.0 capmod=2.0

*mobility related model parameters

+ua=1.0e-12 ub=1.7e-18 uc=5.7e-11 u0=4.0e+02
*sub-threshold related parameters

+dsub=5.0e-01 eta0=3.0e-02 etab=-4.0e-02 nfactor=1.1e-01

*temperature effect parameters

+at=3.3e+04 ute=-1.8 kt1=-3.3e-01 kt2=2.2e-02 kt1l=0.0 ua1=0.0 ub1=0.0 uc1=0.0 prt=0.0

*Overlap Capacitance related and dynamic model parameters

+cgdo=2.1e-10 cgso=2.1e-10 cgbo=1.1e-10 cgdl=0.0 cgsl=0.0 ckappa=6.0e-01 cf=0.0
elm=5.0 xpart=1.0 clc=1.0e-15 cle=6.0e-01

*Saturation related parameters

+em=4.1e+07 pclm=6.8e-01 pdiblc1=1.1e-01 pdiblc2=1.4e-03 drout=5.0e-01 a0=2.2
a1=0.0 a2=1.0 pvag=0.0 vsat=1.2e+05
+ags=2.5e-01 b0=-1.8e-08 b1=0.0 delta=1.0e-02 pdiblcb=2.6e-01

*process and parameters extraction related model parameters

+tox=7.7e-09 ngate=0.0 nlx=1.9e-07 xl=5.0e-08 xw=0.0

*substrate current related model parameters

+alpha0=0.0 beta0=3.0e+01

*Geometry modulation related model parameters

+ll=0.0 lw=0.0 lwl=0.0 lln=1.0 lwn=1.0 wl=0.0 ww=0.0 wwl=0.0 wln=1.0 wwn=1.0
w0=1.2e-07 dlc=8.3e-09 dwc=2.7e-08 dwb=0.0
+dwg=0.0

*Noise effect related model parameters

+af=1.4 kf=2.8e-27 ef=1.0 noia=1.0e+20 noib=5.0e+04 noic=-1.4e-12 nlev=0.0

*End Model

.MODEL PM1 PMOS LEVEL=49

*Common Extrinsic model parameters

+acm=2 rd=0 rs=0 rsh=6.0e01 rdc=0.0 rsc=0.0 lint=9.9e-08 wint=3.9e-08 ldif=0.0 hdif=8.0e-07 wmlt=1.0 lmlt=1.0 xj=3.0e-07
+js=2.0e-05 jsw=0.0 is=0.0 n=1.0 nds=1000. vnds=-1.0 cj=6.0e-04 cjsw=3.3e-10 fc=0.0 mj=4.4e-01 mjsw=2.4e-01 tt=0.0
+pb=8.4e-01 php=9.4e-01

*Threshold voltage related model parameters

+nch=5.9e+16 vth0=-7.8e-01 voff=-1.1e-01 dvt0=2.0 dvt1=5.0e-01 dvt2=-4.0e-02 keta=-7.7e-03 k1=6.0e-01 k2=-1.6e-02 k3=-1.5e+01
+k3b=-1.4 pscbe1=5.0e+08 pscbe2=1.0e-10 dvt0w=0.0 dvt1w=0.0 dvt2w=0.0

*parasitic resistance and capacitance related model parameters

+rdsw=3.8e+03 cdsc=0.0 cdscb=0.0 cdscd=2.2e-04 prwb=0.0 prwg=0.0 cit=3.2e-04
* Flags
+mobmod=1.0 capmod=2.0

*mobility related model parameters

+ua=6.8e-11 ub=1.0e-18 uc=-1.2e-10 u0=1.1e+02

*sub-threshold related parameters

+dsub=4.4e-01 eta0=4.8e-02 etab=-3.5e-05 nfactor=2.2e-01

*temperature effect parameters

+at=3.3e+04 ute=-1.4 kt1=-5.7e-01 kt2=2.2e-02 kt1l=0.0 ua1=0.0 ub1=0.0 uc1=0.0 prt=0.0

*Overlap Capacitance related and dynamic model parameters

+cgdo=3.4e-10 cgso=3.4e-10 cgbo=1.3e-10 cgdl=0.0 cgsl=0.0 ckappa=6.0e-01 cf=0.0 elm=5.0 xpart=1.0 clc=1.0e-15 cle=6.0e-01

*Saturation related parameters

+em=4.1e+07 pclm=1.5e-01 pdiblc1=5.9e-03 pdiblc2=3.4e-04 drout=7.9e-02 a0=7.5e-01
a1=0.0 a2=1.0 pvag=0.0 vsat=9.5e+04
+ags=1.7e-01 b0=3.4e-07 b1=0.0 delta=1.0e-02 pdiblcb=-3.0e-01

*process and parameters extraction related model parameters

+tox=1.3e-08 ngate=0.0 nlx=2.8e-07 xl=0.0 xw=0.0

*substrate current related model parameters

+alpha0=0.0 beta0=3.0e+01

*Geometry modulation related model parameters

+ll=0.0 lw=0.0 lwl=0.0 lln=1.0 lwn=1.0 wl=0.0 ww=0.0 wwl=0.0 wln=1.0 wwn=1.0
w0=7.3e-07 dlc=9.9e-08 dwc=3.9e-08 dwb=0.0
+dwg=0.0

*Noise effect related model parameters

+af=1.8 kf=1.1e-26 ef=1.0 noia=1.0e+20 noib=5.0e+04 noic=-1.4e-12 nlev=0.0

***End Model**

Appendix B

T-spice code for Telescopic OTA

*TELESCOPIC OTA DESIGN

***MODEL PARAMETER**

. MODEL NM1 NMOS LEVEL=49

Use Appendix A Level 49 Parameter

***End Model**

. MODEL PM1 PMOS LEVEL=49

***Use Appendix A Level 49 Parameter**

***End Model**

```
M1 12 1 8 8          NM1 L=0.35U W=240U
M2 13 2 8 8          NM1 L=0.35U W=240U
*M2 13 11 8 8        NM1 L=0.35U W=240U(slew rate)
M3 4 3 12 12         NM1 L=0.35U W=360U
M4 11 3 13 13        NM1 L=0.35U W=360U
```

***Wilson mirror use M5 M6 M7 M8**

```
M5 4 4 5 5           PM1 L=0.35U W=400U
M6 11 4 6 6          PM1 L=0.35U W=400U
M7 5 6 9 9           PM1 L=0.8U W=360U
M8 6 6 9 9           PM1 L=0.8U W=360U

M9 8 7 10 10         NM1 L=0.35U W=180U
M10 7 7 10 10        NM1 L=0.35U W=180U

CL 11 0 0.1pf
IBIAS 9 7 150u
VB 3 0 850mV

VDD 9 0 2V
VSS 10 0 -2V
```

***Different Analysis (AC, DC, Slew Rate, CMRR, PSSR, Noise etc.) is to be done based on above code**

Appendix C

T-spice code for Folded Cascode OTA

***FOLDED CASCODE OTA DESIGN**

***MODEL PARAMETER**

. MODEL NM1 NMOS LEVEL=49

Use Appendix A Level 49 Parameter

***End Model**

. MODEL PM1 PMOS LEVEL=49

*** Use Appendix A Level 49 Parameter**

***End Model**

```
M1 14 10 9 9        PM1 L=0.35U W=18U
M2 10 10 9 9        PM1 L=0.35U W=18U
M3 8 8 14 14        PM1 L=0.35U W=18U
M4 11 8 10 10       PM1 L=0.35U W=18U
M5 8 7 4 4          NM1 L=0.35U W=6U
M6 11 7 5 5         NM1 L=0.35U W=6U
M7 4 6 15 15        NM1 L=0.35U W=6U
M8 5 6 15 15        NM1 L=0.35U W=6U
M9 4 1 3 3          PM1 L=0.35U W=35U
M10 5 2 3 3         PM1 L=0.35U W=35U
*M10 5 11 3 3       PM1 L=0.35U W=35U(for slew rate )
M11 7 7 6 6         NM1 L=0.35U W=6U
M12 6 6 15 15       NM1 L=0.35U W=6U

CL 11 0 0.1pf
IBIAS1 9 3 10u
IBIAS2 9 7 10u

VDD 9 0 2V
VSS 15 0 -2v
```

***Different Analysis (AC, DC, Slew Rate, CMRR, PSSR, Noise etc.) is to be done based on above code**

Appendix D

T-spice code for Wide Swing Folded Cascode OTA (Poor Negative CMR)

```
*WIDE SWINGFOLDED CASCODE OTA DESIGN

*MODEL PARAMETER

. MODEL NM1 NMOS LEVEL=49

*Use Appendix A Level 49 Parameter

*End Model

. MODEL PM1 PMOS LEVEL=49

* Use Appendix A Level 49 Parameter

*End Model
* Wide-swing OTA
* Simulation using subckt
* NMOS input stage => poor negative CMR
* OTA inputs

Vin 1 0 DC 0V
Xwsota 1 3 3 WSOTA
.SUBCKT WSOTA in+ in- out

* Power supplies
VDD vdd 0 DC 2V
VSS vss 0 DC -2V

* Wmin=Lmin=0.35  for linear analog circuit
. PARAM Wn=10.8U, Ln=0.35U
. PARAM Wp=32.4U, Lp=0.35U
. PARAM Wn7=3.6U, Ln7=0.35U
. PARAM Wp7=5.4U, Lp7=0.35U
. PARAM IB=10UA
```

*** Biasing Circuit to generates vb1, vb2, vb3, vb4**

MPB1 vb1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB2 m1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB3 vb2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB4 m3 m2 m1 vdd PMOS1 W=Wp L=Lp
MPB5 vss m2 vb2 vb2 PMOS1 W=Wp L=Lp
MPB0 m2 m2 vb1 vb1 PMOS1 W=Wp7 L=Lp7
MNB0 m3 m3 vb4 vss NMOS1 W=Wn7 L=Ln7
MNB1 vdd m3 vb3 vss NMOS1 W=Wn L=Ln
MNB2 vb4 vb4 vss vss NMOS1 W=Wn L=Ln
MNB3 vb3 vb4 vss vss NMOS1 W=Wn L=Ln
ISS m2 vss IB

*** Wide Swing OTA Implementation**
MN1 n1 in+ n3 vss NMOS1 W=Wn L=Ln
MN2 n2 in- n3 vss NMOS1 W=Wn L=Ln
MN3 n3 vb3 n7 vss NMOS1 W=Wn L=Ln
MN4 n7 vb4 vss vss NMOS1 W=Wn L=Ln
MN5 n4 vb3 n5 vss NMOS1 W=Wn L=Ln
MN7 out vb3 n6 vss NMOS1 W=Wn L=Ln
MN6 n5 n4 vss vss NMOS1 W=Wn L=Ln
MN8 n6 n4 vss vss NMOS1 W=Wn L=Ln
MP6 n1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP8 n2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP5 n4 vb2 n1 vdd PMOS1 W=Wp L=Lp
MP7 out vb2 n2 vdd PMOS1 W=Wp L=Lp
.ENDS

*** Analysis**

. DC Vin -3.5V 3.5V .05V
***. PROBE**
. Print v (3)
. End

Appendix E

T-spice code for Wide Swing Folded Cascode OTA (Poor Positive CMR)

```
*WIDE SWING FOLDED CASCODE OTA DESIGN

*MODEL PARAMETER

. MODEL NM1 NMOS LEVEL=49

*Use Appendix A Level 49 Parameter

*End Model

. MODEL PM1 PMOS LEVEL=49

* Use Appendix A Level 49 Parameter

* Wide-swing OTA
* Simulation using subckt
* PMOS input stage=>poor positive input CMR
* OTA inputs

Vin 1 0 DC 0V
Xwsota 1 3 3 WSOTA

*Xwsota 1 0 3 WSOTA
*VS 3 0 DC 0V

.SUBCKT WSOTA in+ in- out

* Power supplies
VDD vdd 0 DC 2V
VSS vss 0 DC -2V

* Wmin=Lmin=0.35  for linear analog circuit
. PARAM Wn=10.8U, Ln=0.35U
. PARAM Wp=32.4U, Lp=0.35U
. PARAM Wn7=3.6U, Ln7=0.35U
. PARAM Wp7=5.4U, Lp7=0.35U
. PARAM IB=10UA
```

*** Biasing Circuit to generates vb1, vb2, vb3, vb4**

MPB1 vb1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB2 m1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB3 vb2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB4 m3 m2 m1 vdd PMOS1 W=Wp L=Lp
MPB5 vss m2 vb2 vb2 PMOS1 W=Wp L=Lp
MPB0 m2 m2 vb1 vb1 PMOS1 W=Wp7 L=Lp7
MNB0 m3 m3 vb4 vss NMOS1 W=Wn7 L=Ln7
MNB1 vdd m3 vb3 vss NMOS1 W=Wn L=Ln
MNB2 vb4 vb4 vss vss NMOS1 W=Wn L=Ln
MNB3 vb3 vb4 vss vss NMOS1 W=Wn L=Ln
ISS m2 vss IB

*** Wide Swing OTA Implementation**

MN5 n4 vb3 n5 vss NMOS1 W=Wn L=Ln
MN7 out vb3 n6 vss NMOS1 W=Wn L=Ln
MN6 n5 n4 vss vss NMOS1 W=Wn L=Ln
MN8 n6 n4 vss vss NMOS1 W=Wn L=Ln
MP6 n1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP8 n2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP5 n4 vb2 n1 vdd PMOS1 W=Wp L=Lp
MP7 out vb2 n2 vdd PMOS1 W=Wp L=Lp
MP1 n5 in+ n8 vdd PMOS1 W=Wp L=Lp
MP2 n6 in- n8 vdd PMOS1 W=Wp L=Lp
MP4 n9 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP3 n8 vb2 n9 vdd PMOS1 W=Wp L=Lp
.ENDS

*** Analysis**
. DC Vin -3.5V 3.5V .05V
***. PROBE**
. Print v (3)
. END

Appendix F

T-spice code for Wide Swing Folded Cascode OTA (Both NMOS-PMOS Differential Pair)

* Wide Swing Folded Cascode OTA Design

```
*MODEL PARAMETER

. MODEL NM1 NMOS LEVEL=49

*Use Appendix A Level 49 Parameter

*End Model

. MODEL PM1 PMOS LEVEL=49

* Use Appendix A Level 49 Parameter

*wsotatf.cir(AC Analysis)
* Wide-swing OTA
* Simulation showing all components
* Wmin=Lmin=0.35 for linear analog circuit

. PARAM Wn=10.8U, Ln=0.35U
. PARAM Wp=32.4U, Lp=0.35U
. PARAM Wn7=3.6U, Ln7=0.35U
.PARAM Wp7=5.4U, Lp7=0.35U

* Power supplies

VDD vdd 0 DC 2V
VSS vss 0 DC -2V

* Biasing Circuit to generates vb1, vb2, vb3, vb4

MPB1 vb1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB2 m1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB3 vb2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB4 m3 m2 m1 vdd PMOS1 W=Wp L=Lp
MPB5 vss m2 vb2 vdd PMOS1 W=Wp L=Lp
MPB0 m2 m2 vb1 vdd PMOS1 W=Wp7 L=Lp7
```

MNB0 m3 m3 vb4 vss NMOS1 W=Wn7 L=Ln7
MNB1 vdd m3 vb3 vss NMOS1 W=Wn L=Ln
MNB2 vb4 vb4 vss vss NMOS1 W=Wn L=Ln
MNB3 vb3 vb4 vss vss NMOS1 W=Wn L=Ln
ISS m2 vss 10uA

*** Wide Swing OTA Implementation**

MN1 n1 in+ n3 vss NMOS1 W=Wn L=Ln
MN2 n2 in- n3 vss NMOS1 W=Wn L=Ln
MN5 n4 vb3 n5 vss NMOS1 W=Wn L=Ln
MN7 3 vb3 n6 vss NMOS1 W=Wn L=Ln
MN6 n5 n4 vss vss NMOS1 W=Wn L=Ln
MN8 n6 n4 vss vss NMOS1 W=Wn L=Ln
MN3 n3 vb3 n7 vss NMOS1 W=Wn L=Ln
MN4 n7 vb4 vss vss NMOS1 W=Wn L=Ln
MP6 n1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP8 n2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP5 n4 vb2 n1 vdd PMOS1 W=Wp L=Lp
MP7 3 vb2 n2 vdd PMOS1 W=Wp L=Lp}
MP1 n5 in+ n8 vdd PMOS1 W=Wp L=Lp
MP2 n6 in- n8 vdd PMOS1 W=Wp L=Lp
MP4 n9 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP3 n8 vb2 n9 vdd PMOS1 W=Wp L=Lp

***AC Analysis**
*** OTA inputs**
***Vin in+ 0 DC 0V AC 1V**
***Vb in- 0 DC 0V**
***.AC DEC 10 1Hz 1000MegHz**
***. PRINT VDB (3) VP (3)**
***.OP**
***.END**

*** DC transfer Analysis**
***.DC Vin -3.5V 3.5V .05V**
***. Print dc V (3)**
***.END**

Appendix G

T-spice code for 2nd Order Biquad Filter using Wide Swing Folded Cascode OTA

* 2nd Order Biquad Filter using Wide Swing Folded Cascode OTA

```
*MODEL PARAMETER

. MODEL NM1 NMOS LEVEL=49

*Use Appendix A Level 49 Parameter

*End Model

. MODEL PM1 PMOS LEVEL=49

* Use Appendix A Level 49 Parameter

*Biquad 2nd order filter. fo=100K

Vin 1 0 DC 0V AC 1V
*LP
Xs2flt 1 0 0 2 S2FLT
*HP
*Xs2flt 0 0 1 2 S2FLT
*BP
*Xs2flt 0 1 0 2 S2FLT
*BR
*Xs2flt 1 0 1 2 S2FLT

. SUBCKT S2FLT v1 v2 v3 v0

. PARAM C=135.98pF
. PARAM Q=1.61803
Xota1 v1 v0 n2 WSOTA
Xota2 n2 v0 v0 WSOTA

C1 n2 v2 C/Q IC=0V
C2 v0 v3 Q*C IC=0V
. ENDS
. SUBCKT WSOTA in+ in- out

* Power supplies
VDD vdd 0 DC 2V
```

```
VSS vss 0 DC -2V
* Wmin=Lmin=0.35 for linear analog circuit

. PARAM Wn=10.8U, Ln=0.35U
. PARAM Wp=32.4U, Lp=0.35U
. PARAM Wn7=3.6U, Ln7=0.35U
. PARAM Wp7=5.4U, Lp7=0.35U
. PARAM IB=10UA

* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB2 m1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB3 vb2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MPB4 m3 m2 m1 vdd PMOS1 W=Wp L=Lp
MPB5 vss m2 vb2 vb2 PMOS1 W=Wp L=Lp
MPB0 m2 m2 vb1 vb1 PMOS1 W=Wp7 L=Lp7
MNB0 m3 m3 vb4 vss NMOS1 W=Wn7 L=Ln7
MNB1 vdd m3 vb3 vss NMOS1 W=Wn L=Ln
MNB2 vb4 vb4 vss vss NMOS1 W=Wn L=Ln
MNB3 vb3 vb4 vss vss NMOS1 W=Wn L=Ln
ISS m2 vss IB

* Wide Swing OTA Implementation
MN1 n1 in+ n3 vss NMOS1 W=Wn L=Ln
MN2 n2 in- n3 vss NMOS1 W=Wn L=Ln
MN5 n4 vb3 n5 vss NMOS1 W=Wn L=Ln
MN7 out vb3 n6 vss NMOS1 W=Wn L=Ln
MN6 n5 n4 vss vss NMOS1 W=Wn L=Ln
MN8 n6 n4 vss vss NMOS1 W=Wn L=Ln
MN3 n3 vb3 n7 vss NMOS1 W=Wn L=Ln
MN4 n7 vb4 vss vss NMOS1 W=Wn L=Ln
MP6 n1 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP8 n2 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP5 n4 vb2 n1 vdd PMOS1 W=Wp L=Lp
MP7 out vb2 n2 vdd PMOS1 W=Wp L=Lp
MP1 n5 in+ n8 vdd PMOS1 W=Wp L=Lp
MP2 n6 in- n8 vdd PMOS1 W=Wp L=Lp
MP4 n9 vb1 vdd vdd PMOS1 W=Wp L=Lp
MP3 n8 vb2 n9 vdd PMOS1 W=Wp L=Lp

. ENDS
* AC Analysis
. AC DEC 100 1Hz 100MegHz
. Print Vdb (2)
. END
```

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Appendix H

Published Paper

During this work the following two papers were accepted.

1.Kehul Shah, N. M. Devashrayee "Folded Cascode OTA for Wide Band Application" National Conference on advance Communication, to be held on 29th - 30th March 2008 at Dharmsinh Desai University, Nadiad, Gujarat.

2. Kehul Shah, N. M. Devashrayee "Wide Swing Folded Cascode OTA" National Conference on advance Communication, to be held on 8th - 9th April 2008 at C.U. Shah College of Engineering, Wadhawan, Gujarat.

3. Kehul Shah, N. M. Devashrayee "Universal Filter Design using Wide Swing Folded Cascode OTA" A State Level Paper Contest "Networking:Technology and Applications-2008", to be held on 20th April 2008 at "Institution of Electronics and Telecommunications engineers" and "The Institution of Engineers (India)"I.E.T.E Vadodara Center, Vadodara Gujarat.

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