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Analysis and Characterization of Various Current Mirror Topologies in 90 nm Technology

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***Abstract*— Although large electronic systems can be constructed almost entirely with digital techniques, many systems still have analog components and current mirror is the core structure for almost all analog and mixed mode circuits. It determines the performance of analog structures, which largely depends on their characteristics. In this paper, we have analyzed various topologies of current mirror using 90 nm technology in Mentor Graphics and compared them based on different parameters like power dissipation, minimum output voltage, bandwidth, transfer characteristics etc.**

***Keywords*— Current Mirror, Excess gate voltage, Minimum output voltage, MOSFET, Output impedance, Power dissipation, Transfer characteristics**

I. Introduction

A two terminal circuit whose output current is independent of the output terminal voltage and depends only on the input current is called current mirror. Generally, it is used to generate a replica of given reference current. If necessary, it can also amplify or attenuate the reference current. A current mirror can be thought as a current controlled current source. Ideally, the output impedance of a current source/sink should be infinite and capable of generating or drawing a constant current over a wide range of voltages. However, finite value of output resistance and a limited output voltage required to keep device in saturation will ultimately limit the performance of the current mirror. Current mirror is used for biasing, loading, current amplification etc. Current mirrors are employed in many applications such as operational amplifiers, analog to digital and digital to analog converters.

Fig. 1 shows the symbols of current mirror circuits in which arrow is used to designate the direction of the current flow on the input side. The ratio 1: K represents the current gain of the mirror circuit. [4]

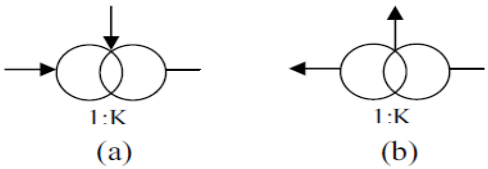

Fig. 1 Current Mirror Symbols (a) NMOS Current Mirror (b) PMOS Current Mirror

Current mirrors mimic the performance of an ideal current source. Therefore their designs must fulfill the following requirements. [3]

- Input impedance should be zero.
- Output impedance should be infinite.
- Output current should be constant over wide swing of voltage
- Accurate copy of input current.

The paper is organized as follows: Various current mirror topologies are described in section II. The simulation results are discussed in section III. The paper is concluded in section IV.

II. Topologies Of Current Mirror

A. Basic Current Mirror

Fig. 2 shows the basic current mirror. A current flows through M1 corresponding to V_{GS1}. Since V_{GS1} = V_{GS2}, ideally the same current, or a multiple of the current in M1, flows through M2. If the MOSFETs are of the same size, the same drain current flows in each MOSFET, provided M2 stays in the saturation region[1]. The current through M1 can be given by,

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{THN})^2$$

The output current, assuming M2 in saturation is given by

$$I_{D2} = I_O = \frac{\beta_2}{2}(V_{GS2} - V_{THN})^2$$

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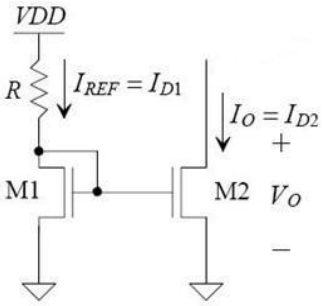

Fig. 2 Basic Current Mirror

Since $V_{GS1}=V_{GS2}$, the ratio of the drain currents is

$$\frac{I_{D2}}{I_{D1}} = \frac{\beta_2}{\beta_1} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}}$$

The desired output current can be obtained by adjusting W/L ratios of two devices.[1]

Here it is required that M2 remains in saturation. Therefore the minimum output voltage across the current mirror is given by $V_{min}=V_{DS(SAT)}=V_{GS}-V_{THN}$. The output resistance of current mirror is equal to output resistance of M2.

$$r_o = \frac{1}{\lambda I_o}$$

The simulation results are shown in fig. 8a and 8b. Fig. 8a shows AC analysis. Transfer characteristic is shown in fig. 8b. Transfer characteristic is not exactly linear. It is of curved shape because of small scale effects. Output resistance of basic current mirror is very low. But it possesses larger bandwidth compared to other topologies.

B. Double Cascode Current Mirror

Double cascode configuration is used to increase the output resistance of a current source or sink. Fig. 3 shows schematic diagram for this configuration. If we define ΔV as excess gate-source voltage, the gate voltage of M4 is $2(\Delta V+V_{THN})$ and source voltage is $\Delta V+V_{THN}$. The minimum voltage across the current sink is limited by the requirement that M4 remains in the saturation region. $V_{DS4} \geq V_{GS4} - V_{THN}$ or $V_{D4} \geq 2\Delta V+V_{THN}$ [1]. This minimum voltage across the cascode current mirror is significantly larger than the minimum voltage across the basic current mirror.

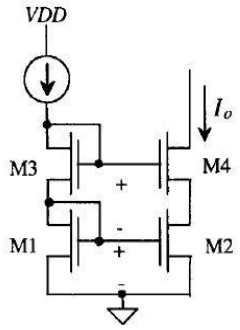

Fig. 3 Double Cascode Current Mirror

Fig. 4 shows the small signal model for double cascode current mirror. The output resistance of the double cascode current source is given by

$$R_o = r_{o4}(1+g_{m4}r_{o2})+r_{o2} \cong g_{m4}r_o^2$$

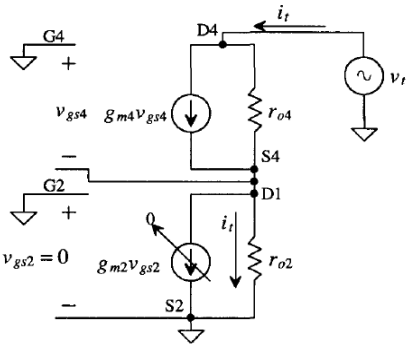

Fig. 4 Small-signal model of Double Cascode Current Mirror

C. Triple Cascode Current Mirror

Output impedance can be further increased by adding one more stage to double cascode configuration.[1] Triple cascode configuration is shown in fig. 5.

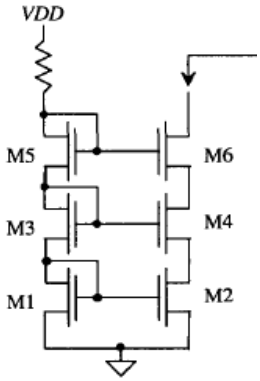

Fig. 5 Triple Cascode Current Mirror

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The minimum output voltage for triple cascode configuration is given by $3\Delta V+2V_{THN}$.[2] Output impedance can be found by applying small signal model at output side and is given by,

$$R_o \cong g_{m6} g_{m4} r_o^3$$

Where g_{m4} and g_{m6} is trans-conductance of M4 and M6 respectively and r_o is output impedance of each MOSFET.

D. Regulated Cascode Current Mirror

This configuration uses negative feedback concept to stabilizes the output current I_o. This configuration is shown in fig. 6.

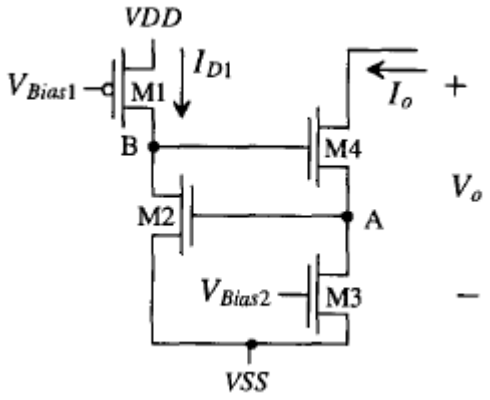

Fig. 6 Regulated Cascode Current Mirror

MOSFETs M2 and M4 provides negative feedback while, M1 and M3 form current mirror.[1]Here, the voltages V_{Bias1} and V_{Bias2} are applied in such a way that only constant current can pass through M1 and M3 respectively. If output current increases due to some reason, voltage at node-A rises since only constant current can pass through M3. So it increases current through M2, but because of V_{Bias1}, current cannot increase for M1. This results in decrease in voltage at node-B. Thus, excess current from M4 is absorbed by M2 and it balances the output current I_o.

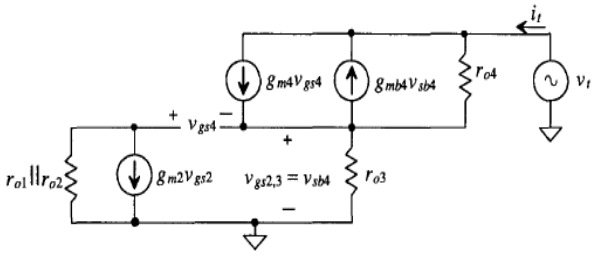

Fig. 7 Small-signal model for Regulated Cascode Current Mirror

The minimum output voltage for regulated cascade is given by $V_{DS3(sat)}$. The small-signal model is shown in fig. 7. The output impedance can be given by,

$$R_{out} \approx g_{m2} g_{m4} (r_{o1} \| r_{o2}) r_{o3} r_{o4} \approx \frac{g_m^2 r_o^3}{2}$$

Where g_m is trans-conductance for particular MOSFET and r_o is output impedance.

III. Simulations Results

All the above proposed topologies were simulated using 90 nm technology. Simulation results were taken with the help of "Pyxis Schematic" tool provided by Mentor graphics.

For analog design it is extremely important to keep output resistance as high as possible. It is also important to reduce the effect of channel length and mobility modulation. These effects are reduced by increasing the channel length of devices. We have taken the channel length equals to 100 nm for all the MOSFETs used in each topology due to above reasons. Their widths may vary according to need and topology.

For our simulation values of different parameters are as follows: V_{THN} = 0.228 V, V_{THP} = -0.2038 V, V_{GS} = 0.35 V, V_{DD} = 0.9 V, V_{SS} = -0.9 V, I_0 = 10 µA, λ = 0.84 V^{-1}.

A. Basic Current Mirror

This topology does not provide high output impedance. But it provides very high bandwidth as shown in fig. 8a. It is also seen that output current is not perfectly following the input current form fig. 8b. Transfer characteristic is nonlinear in nature.

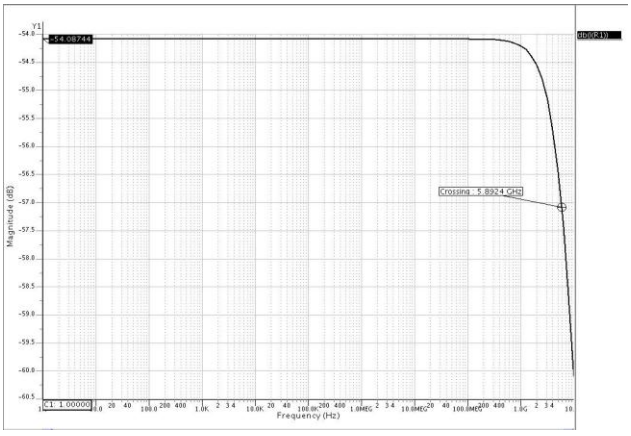

Fig. 8a AC Characteristic of Basic Current Mirror

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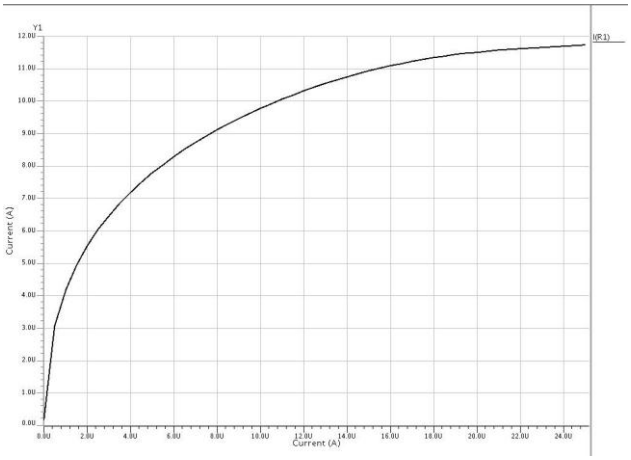

Fig. 8b Transfer characteristic of Basic Current Mirror

B. Double Cascode Current Mirror

This topology provides high output resistance than basic configuration but it requires comparably high minimum output voltage. It provides less bandwidth than basic configuration as shown in fig. 9a. Output current is effectively following the input current which can be seen from fig. 9b. Still transfer characteristic is quite non-linear.

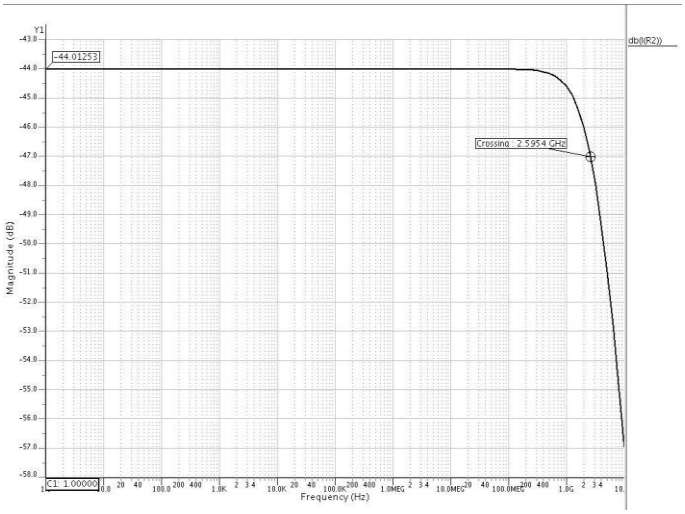

Fig. 9a AC Characteristics of Double Cascode Current Mirror

C. Triple Cascode Current Mirror

This topology provides same results as double cascade. The minimum output voltage required to keep output device in saturation is higher than double cascade current mirror. Bandwidth is increased by some amount as shown in fig. 10a. Transfer characteristic is shown in fig. 10b.

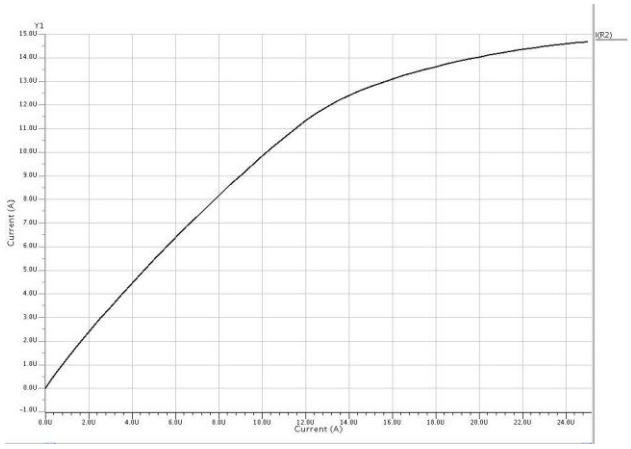

Fig. 9b Transfer characteristic of Double Cascode Current Mirror

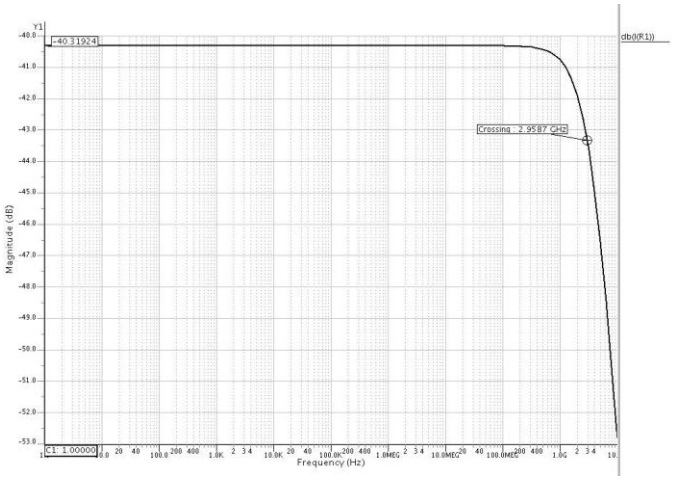

Fig. 10a AC Characteristics of Triple Cascode Current Mirror

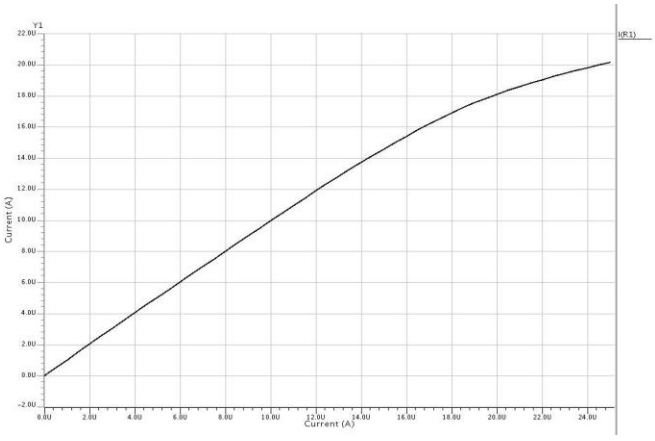

Fig. 10b Transfer characteristic of Triple Cascode Current Mirror

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TABLE I
COMPARISON AMONG VARIOUS PARAMETERS

Topology	Minimum output Voltage	Bandwidth	Power Dissipation	Output Resistance
Basic Current Mirror	0.122 V	5.89 GHz	34.84 µW	119 KΩ
Double Cascode Current Mirror	0.472 V	2.59 GHz	32.84 µW	2.32 MΩ
Triple Cascode Current Mirror	0.822 V	2.95 GHz	31.70 µW	45.26 MΩ
Regulated Cascode Current Mirror	0.122 V	659 MHz	102.68 µW	22.63 MΩ

D. Regulated Cascode Current Mirror

Negative feedback provides optimization between output resistance and minimum output voltage. It provides less bandwidth compared to double and triple cascade configurations and is shown in fig. 11a. The transfer characteristics is linear for small input current, but for larger value of current it becomes non-linear as shown in fig. 11b.

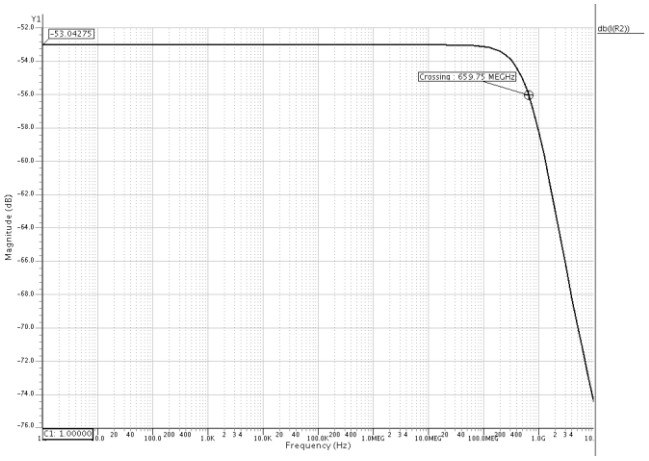

Fig. 11a AC Characteristics of Regulated Cascode Current Mirror

IV. CONCLUSION

The design of current mirrors is one of the most challenging aspects in the analog and mixed signal design. In this paper we have analysed various current mirror parameters like minimum output voltage, output impedance, bandwidth etc. for different topologies in 90 nm technology.

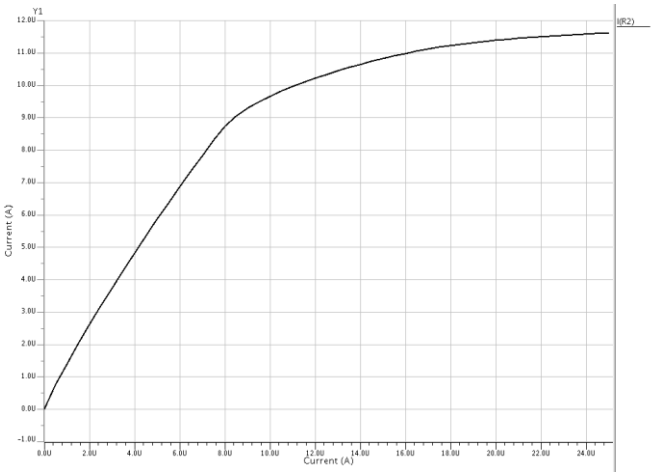

Fig. 11b Transfer characteristic of Triple Cascode Current Mirror

Different current mirror topologies have their own advantages and disadvantages. Minimum output voltage and output impedance are the two most important parameters for any current mirror topology. Output impedance can be increased by stacking more and more number of stages in basic current mirror. The consequence is the increase in minimum output voltage. Hence there is a trade-off between output impedance and minimum output voltage required.

From table 1 it is clear that basic current mirror provides very high bandwidth and possesses lowest minimum output voltage, but has very low output impedance. Double cascode and triple cascode current mirror possess very high output impedance, but they require higher minimum output voltage compared to basic current mirror topology.

Regulated cascode current mirror topology comprises negative feedback technique to provide stable output current. It possesses optimum values for almost all parameters compared to other topologies.

In 90 nm technology, due to small-scale effects found in MOSFETs, current mirrors behave non-linearly. This non-linearity decreases from basic current mirror topology to higher topologies. Operating bandwidth of current mirror is very high for 90 nm technology.

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