Designing Wideband Voltage Controlled Oscillators for Software-Defined Radio

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Abstract- **The demand for mobile communication systems with global coverage, interfacing with various standards and protocols, high data rates and improved link quality for a variety of applications has dramatically increased in recent years. The Software-Defined Radio (SDR) is the recent proposal to achieve these. In SDR, new concepts and methods, which can optimally exploit the limited resources, are necessary. One very important requirement of SDR is designing wideband RF hardware covering octave bands. For example, the local oscillator of the mixer should be a wideband voltage controlled oscillator (VCO). The paper presents theoretical concepts for designing VCOs. It also provides simulation of the design. Using this conceptual design and simulation, the actual VCO hardware was designed and fabricated, and the results including very good phase noise performance are presented.**

Keywords- **Software-defined Radio, Voltage Controlled Oscilator, Phase Noise**

I. INTRODUCTION

The need of the mobile telephony is continuous coverage throughout the world and ease of interfacing with different systems and standards. To manage such changes, mobile devices must have reconfigurable hardware and reprogrammable software. Such radios, known as Software-Defined Radios (SDR) can be implemented efficiently using software radio architectures in which the radio reconfigures itself based on the system it will be interfacing with and the functionalities it will be supporting [1, 2].

Implementation of the software-defined radio would require either the conversion of RF into baseband at the antenna or the design of a completely flexible radio frequency (RF) front-end for handling a wide range of frequencies [4]. The smart antenna system in SDR combats the multipath effects and co-channel interference [3]. Digitizing the signal with an analog to digital converter (ADC) in the IF range eliminates the last stage in the conventional model in which problems like carrier offset and imaging are encountered.

One of the challenges in SDR design is: for the reconfigurable RF front end, the architectures and circuits should be designed for a broad range of requirements in carrier frequency, channel bandwidth and noise performance. Meeting the performance parameters over a broad range of frequency is not trivial. The following work includes theory, design, simulation, fabrication and test & optimization of voltage controlled oscillator for wideband LO in SDR.

II. VCO DESIGN THEORY

Although numerous researchers in the past have published oscillator configurations based on some form of small signal analysis, these approaches require a combination of theoretical and empirical calculations and do not always lend themselves to the desired result as tuning of the final device is inevitable. Our approach involves simulation resulting in considerable savings in design time as well as tuning time, yielding results very close to the desired performance. The transistor selection is of primary importance. For a frequency range of a few hundred megahertz to several thousand megahertz, VCOs are commonly built around Bipolar Junction Transistors (BJTs) due to their inherent low noise. Contrary to popular belief, f_{max} is not the most definitive quantity in the selection of the device. Here, f_{max} is defined as the frequency at which the unilateral gain falls to unity, and the device ceases to oscillate. With a high f_{max} the device is susceptible to oscillations outside the desired frequency range, and extraneous coupling between the device leads may arise. Needless to say, if cost is to be kept low, devices with very high f_{max} are prohibitive. f_{max} should definitely be within the desired range of operation, but power dissipation is also an important criteria in the selection of the device. Power dissipation is important, as VCO active devices operate at high power levels. Also, care should be taken to control the oscillation totally through the external circuitry with no possible spurious oscillations inside the device. A preliminary simulation/construction of a non-oscillating circuit is necessary in order to prove that the device is free of unwanted spurious oscillations. The line of BJTs selected offers an ideal choice as they can typically be used up to 8 GHz and lend themselves to all forms of external positive feedback, while producing an average negative resistance of 50 to 400 ohms.

Most of the available literature on oscillators describes the operation of oscillators using small signal S-parameters. The main reason for this is that small signal S-parameters are readily measurable and all transistor manufacturers supply them for their devices. The small signal design technique offers valuable insight into the conditions that govern oscillator starting, while giving a rough prediction

of the possible frequency range of operation. The disadvantage, though, is that those estimates are valid only for the first few cycles after the device is turned on. A proper way to describe the oscillation process is through a thorough derivation of the feedback network of the device, with an application of the Barkhausen criteria. The Barkhausen criteria states that the product of the forward gain path and the feedback path for the complete oscillator network should be equal to unity, while the feedback loop should add the output wave form to the input of the combined network with no phase shift (i.e. positive feedback). During that condition the mechanism that keeps the device in oscillation is the continuous balancing of these two quantities. For example, as the oscillation amplitude of the device increases, its gain decreases to satisfy the previous criteria.

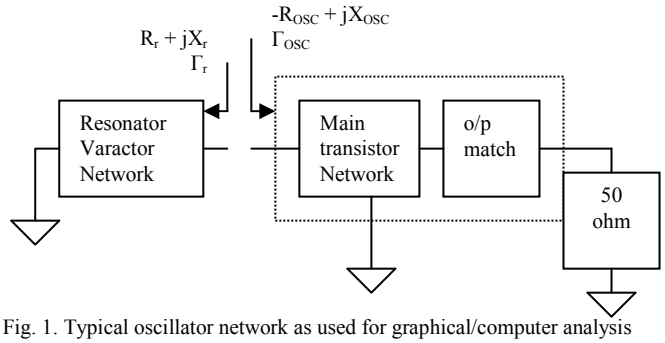

Fig. 1. Typical oscillator network as used for graphical/computer analysis

The derivation of the equations for the feedback loop and the forward gain of the device can be very complex in certain cases, and special care should be taken in identifying the two loops. Rohde [5] offers a very good description of that process. In addition to the above, a rather simplistic method of describing the oscillation criteria has been used here. This process is not favored for its insight in the operation of the device, but rather for its ease of application. Here, the considerations for the input resistance of the device attempt to explain why the amplitude of the signal starts increasing while building up from the internal noise level. Looking at Figure 1, it can be seen that this happens because the resistance of the combined active device is greater than the resistance of the load, namely:

$$\left|-R_{OSC}\right| > R_r \text{ and } X_{OSC} = -X_r \qquad (1)$$

As the oscillation amplitude keeps increasing, the DC operating point of the device shifts continuously; thereby changing the transconductance g_m of the device and, of course, its input and output impedance. This situation produces a frequency shift, a change in output harmonics and/or a change in output power levels, and the oscillator operation predictions in general. The increase in amplitude will cease when the real parts of the respective impedance and the active device become equal, or:

$$\left|-R_{OSC}\right| = R_r \text{ and } X_{OSC} = -X_r$$

$$\text{Alternatively when } \Gamma_r \cdot \Gamma_{osc} = 1 \qquad (2)$$

Where Γ_r and Γ_{osc} are the reflection coefficients produced by $R_r + jX_r$ and $R_{OSC} + jX_{OSC}$ respectively. When steady state occurs, the device reaches saturation levels. R_{OSC} is a very important quantity and is accurately described by the nonlinear I-V relationship of the transistor. If we look at a common base transistor, we can see that due to the nonlinear current source the value of R_{OSC} varies non-linearly about a given I-V operation point. Since that resistance is related to the internal current source, we can imagine the total current as the sum of all the individual currents at all harmonic frequencies. This can be simply stated as:

$$I_{total} = I_{dc} + I_1 + I_2 + I_3 + \ldots\ldots = \sum_{n=0}^{\infty} I_n \qquad (3)$$

Where I_{dc} is the DC current through the device when it dose not oscillate. And I_1, I_2, I_3 are the currents of the first, second, and third harmonics, respectively, which come into play when the device starts oscillating. The total current mentioned above is related to the internal current generator of the transistor, and we can thus express the total transconductance characteristic of the device as:

$$G_{mtotal} = g_{m0} + g_{m1} + g_{m2} + g_{m3} + \ldots = \sum_{n=0}^{\infty} g_{mn} \qquad (4)$$

In the above, g_{m0} is the value of transconductance at DC while g_{m1}, g_{m2} etc are the values at the first, second and third harmonics respectively. It is important to keep in mind that g_{m1} the trans conductance attributed to the first harmonic is approximately equal to $0.7g_{m0}$ and is the most important of the harmonics in equation 4. As the oscillations increases in amplitude the value of g_{m1} decreases in order to keep the device meeting the oscillation criteria, and have G_{mtotal} equal to a constant value for a specific DC input current. The latter explains why the magnitude of R_{osc} is more negative while the system commences oscillation and settles down to a more positive number when the system reaches equilibrium. Also the fact that the g_m terms are a decaying series verifies the fact that the system cannot oscillate to infinity.

There are several options available for the main transistor network [6]. A common base or common emitter configuration is used, with the feedback element in series of parallel from.

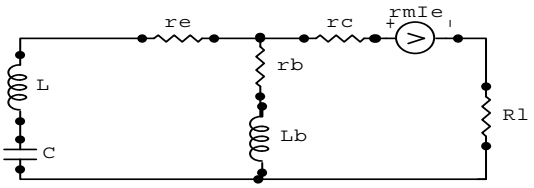

Fig. 2. Small signal model for the common-base configuration

The configuration selected for our design is the common base as shown in figure 2, because it lends itself more easily into oscillation and presents an inherent isolation from output (collector) to input (emitter). The L and C are the part of tank circuit connected at the emitter. The R_l is the load resistor at the collector. The L_b is an external inductor connected at the base for the ease of oscillation as explained later. In this CB configuration, we can assume that the

internal AC base resistance r_b is much less than r_c the internal AC collector resistance, an assumption which is true because r_b is less than 20 ohms while r_c, may well be in the ten megaohm range. Assuming this, we can safely claim that there is a factor α such that $r_m = \alpha \cdot r_c$. Here α is called the short circuit current multiplication factor, a quantity greater than or equal to unity, and r_m is the transfer resistance of the BJT current generator. The importance of α in the determination of the oscillation conditions is easily seen if we attempt to find the input impedance of the previous circuit. It can be easily proven that the input impedance is :

$$R_{in} = (V_{eb}/I_e)|_{Ic=0} = r_e + r_b\, r_c(1-\alpha)/ (r_b + r_c) = r_e + r_b(1-\alpha) \qquad (5)$$

From 4 and 5 we can see that it is possible for a common base configuration to develop a negative input resistance (since α>1) if r_b (or r_b in series with some impendence) becomes sufficiently large. The latter can be easily satisfied by the addition of an external element like the inductance L_b (Figure 2). In order to examine the stability of such a network let us assume that the admittance matrix of the combined device and base stub is Y consisting of parameters Y_{11}, Y_{12}, Y_{21} and Y_{22}. If the output port is terminated with a frequency-varying network Y_{load}, the input admittance is given by equation 7. Similarly if the input port is terminated by a frequency-varying network Y_{source}, then the output admittance will be given by 8.

$$Y_{in} = y_{11} - y_{12}\, y_{21}/(y_{load} + y_{22}) \qquad (7)$$

$$Y_{out} = y_{22} - y_{12}\, y_{21}/(y_{source} + y_{11}) \qquad (8)$$

In view of equations 7 and 8, the stability of the device can be ascertained in two ways: the Linville stability factor (equation 9) or the condition in equation 10 which states than the Z (or Y) matrix of the complete network should be equal to 0.0

$$c = \frac{|y21y12|}{2\mathrm{Re}\{y11\}\mathrm{Re}\{y22\} - \mathrm{Re}\{y21y12\}} \qquad (9)$$

Where c > 1 for instability

Or [V] = [Z]·[I} where the determinant of [Z] is equal to 0.0 for the onset of oscillation. We shall use the second method which gives us a little more insight into the operation of the circuit. We add the output impedance R_l, the inductance L_b and the varactor/inductor combination to the network. We get a network similar to the one in Figure 2.

The following loop equation can then be derived.

$$\begin{pmatrix} 0 \\ 0 \end{pmatrix} = \begin{pmatrix} j(wL - 1/wC) + r_e + r_b + L_b & r_b + L_b \\ r_m + r_b + L_b & r_c + R_l + r_b + L_b \end{pmatrix} \begin{pmatrix} I_e \\ I_c \end{pmatrix} \qquad (10)$$

The determinant of the above matrix must reduce to 0, so the above equation becomes:

$j(wL-1/wC)(r_c+R_l+r_b+L_b)+r_e(r_c+R_l) +(r_e+R_l+(1-\alpha)r_c)(r_b+L_b)=0$

By setting the reactive part to 0.0 we can show that the resonant frequency is $f_0=(1/2\pi)\sqrt{(1/LC)}$ (11)

Similarly, by setting the real part to 0 we can show that:

$$\alpha \geq \left[1 + R_l / r_c\right]\left[1 + r_e /(r_b + L_b)\right] \qquad (12)$$

If α > 1 in 12 by properly choosing R_l(i.e. the output matching network) and L_b(the length of the microstrip inductor), we can ascertain that the circuit will oscillate. Furthermore, by properly selecting the value of the capacitance/ inductance at the emitter, we can tune the circuit over a range.

III. CIRCUIT SIMULATION

A proper method for simulation of oscillating circuits is the nonlinear approach, which can be achieved by using Genesys from Agilent Technologies. The approach describes the active device with a nonlinear large signal S-parameter model, and simulates the network using well-defined goals for oscillation ranges, fundamental and output harmonic power levels. The linearized approach described in the following section (5) involves a simplistic method for the design of the unit. It offers a prediction of the output oscillation range but it has no insight into any of the circuit performance parameters associated with the nonlinear parts of the models.

The first step in the simulation is to determine the optimum base reactance at the desired frequency range of operation (Figure 2). This reactance is selected to make certain that the transistor will oscillate at one frequency in the region of interest (preferably midband). The value of that inductance can be arrived at by a simulation of the transistor in CB configuration with the base stub present and including the parasitic, DC block capacitors and biasing networks. The best choice for a stub length is one that achieves maximum amplitude for S_{11} and S_{22}. In general, the longer the stub, the lower the frequency and vice versa. The optimization tool may be ideal for arriving at the correct value of the base inductance. Care should be taken to see that in the process of maximizing S_{11} and S_{22}, S_{21} is kept relatively constant, as that quantity will now roughly govern the linearity of the output power. To establish the conditions of oscillation, the following have to be met:

$$\Gamma_r \cdot S_{11} = 1 \text{ and } \Gamma_l \cdot S_{22} = 1 \qquad (13)$$

We can continue the optimization by matching the output of the transistor, S_{22}, to the 50 ohm load. This is usually achieved by maximizing S_{11} while the output is conjugately matched. A typical output-matching network is a combination series/open stub. During the optimization process, the lengths of the series and open stubs are left to vary freely while a goal of matching a 50 ohm load has been selected. Of course, this particular matching network is not the sole solution, just a simple choice out of many (some very complex) that the designer can use for effective matching to the load. Once the output has been matched, the input of the one port network, which now looks similar to the combined network in Figure 1, is plotted. If the matching at the output was performed properly, the value of its reflection coefficient should still be much greater than one. The output can either be plotted as $1/S11_{osc}$ on the Smith chart in order to match any loops in the locus or in a tabulated form in order to match amplitude and phase to the reflection coefficient of the resonator. Loops in the locus of the active device at this point may indicate a possibility for injection locking or spurious oscillations.

The resonator section is usually composed of a network of varactors, with a short-circuited stub to ground which serves as a matching network to the input of the transistor combination. Both section of the circuit as per figure 1 were simulated simultaneously. A tabulated form of the results is shown in Table 1 clearly showing the oscillation condition for 500-1000 MHz VCO.

TABLE 1. Various parameters as varactor is tuned

F(GHz)	Mag. $S11_r$	Mag. $S11_{osc}$	$<S11_r$	$<S11_{osc}$
0.57	0.915	1.118	178.8	-179
0.74	0.925	1.993	150.7	-153
0.93	0.93	1.175	156	-156
Note that $\|S11_r\| > 1/\|S11_{osc}\|$ and $<S11_r = -<S11_{osc}$				

IV. HARDWARE DESIGN AND TEST

The typical circuit diagram of the design is shown in figure 3. The printed circuit board using FR4 material was designed and then components were populated as shown in figure 4. The transistor used is NEC's NE85633 with cut off frequency of 7 GHz and noise figure of 1.4 dB. The actual VCO hardware was then tested. The device exhibits excellent phase noise characteristics: typically at 650 MHz; -96 dBc/Hz at 10 kHz from the carrier and -75 dBc/Hz at 1 kHz as shown in figure 5. The output power variation and the tuning voltage across the range for a 500-1000 MHz VCO is +/- 2.5 dB. The VSWR is measured to be 1.85:1 across the band or better. The tuning sensitivity is 50-70 MHz/V and the absolute maximum tuning voltage is 25 volts. Typical frequency pulling is 17 MHz peak to peak and frequency pushing 3 MHz per volt.

TABLE 1. Performance parameters of the VCO designed

Parameter	Tested Value
Frequency range	500-1000 MHz
Phase Noise	-96 dBc/Hz at 10 kHz offset
Amplitude	+13 dBm +/- 2.5 dB
Output VSWR	1.85:1
Tuning sensitivity	50-70 MHz/V
Frequency pulling	17 MHz
Frequency pushing	3 MHz/Volt

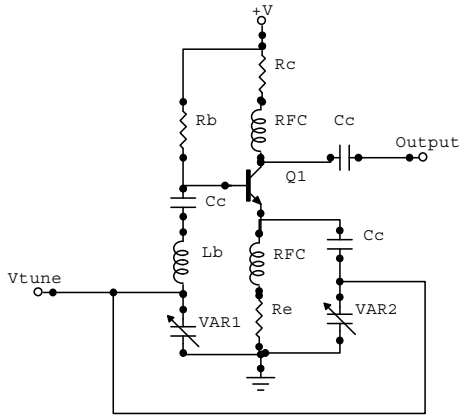

Fig 3: Circuit diagram of the VCO

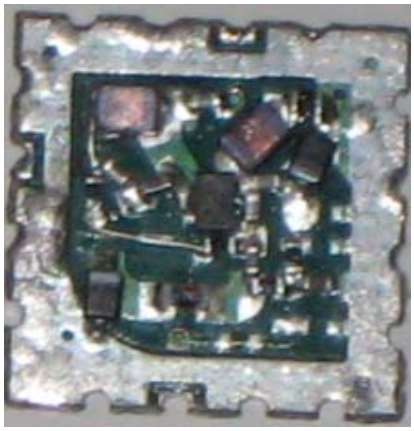

Fig 4: Hardware realization of the VCO

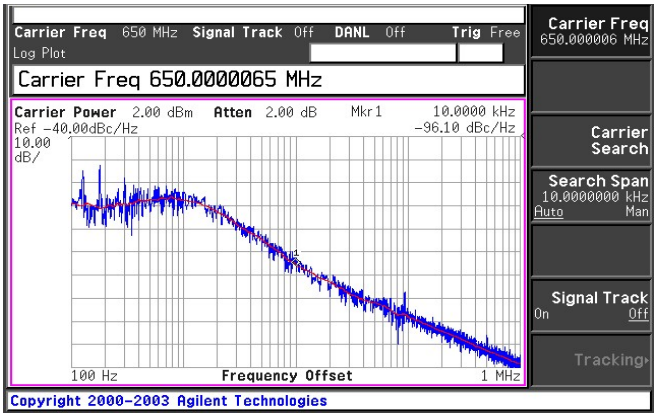

Fig 5: Typical phase noise plot at 650 MHz

V. CONCLUSION

A concise description of a method for the design of a VCO has been presented, and the results of applying this method to a wideband VCO model have been demonstrated. The actual hardware was built covering 500 to 1000 MHz and the prototype test results are very good. This particular design and other designs based on this find very good applications in the wideband front RF end of the software-defined radio.

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