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(Research Article)

VCO and PLL Frequency Synthesizer Discrete Designs for 0.3 – 2.4 GHz Local Oscillator of a Radio Operating Over Wide Frequencies

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Abstract

The transceivers used in the software defined radio require designing wideband RF hardware covering octave bands. The local oscillator of the mixer should be a wideband frequency synthesizer. Building on the theory of oscillations in the voltage controlled oscillator, the paper presents the concept of negative resistance in the transistor circuit with some inductance at the base. It also provides simulation of this concept. The functioning of the phase-locked loop and how it can be used to synthesize various frequencies in local oscillator is discussed with emphasis on design tradeoffs. Applying the theory and simulation, four different VCO circuits were designed and fabricated for the range covering 300 to 2400 MHz. These VCOs were later used in the design of wideband PLL frequency synthesizer. The results including very good phase noise performance are presented. This approach can be used to design wideband synthesizers used in software defined radio of the base stations in mobile communication.

Keywords: Local Oscillator, Phase Noise, Phase-locked Loop, Software-defined Radio, Voltage Controlled Oscillator

1. Motivation

For mobile telephony, the idea of global roaming requires that the radio transceivers support coverage across all geographical regions and interfacing with all systems and standards. The example of first feature is the multimode phones that can be switched between standards like CDMA and Global System Mobile (GSM), while the example of the second feature is to interface mobile phone with IEEE 802.11 or Bluetooth networks. Also, the wireless industry must upgrade their systems to comply with the rapid changes in the technology as well as the human needs. Such radios can be implemented efficiently using Software-Defined Radio (SDR). Joe Mitola in 1991 introduced the term software-defined radio as the class of reconfigurable radios [1,2] - a radio that defines in software its modulation, error correction, and encryption processes, exhibits some control over the RF hardware, and can be reprogrammed is a software-defined radio as shown in figure 1.

SDR requires either the digitization at the antenna, or the design of a reconfigurable radio frequency (RF) front end for the wide frequency range. The smart antenna system that incorporates direction of arrival of the RF wave finding algorithms and reconfiguration of the directional property of the antenna i.e. beam forming to combat the co-channel interference and multipath [4]. The wideband RF chain converts RF to a digital IF and passes on to analog to digital converter (ADC), or as mentioned earlier, RF can be directly down converted to baseband right after the antenna. With the help of the concept of under-sampling, the digital IF signals give spectral replicas that can be placed at the baseband frequency, allowing frequency translation and digitization to be carried out simultaneously. The channel select function is done digitally and sample rate conversion is done to interface the ADC to the processing hardware.

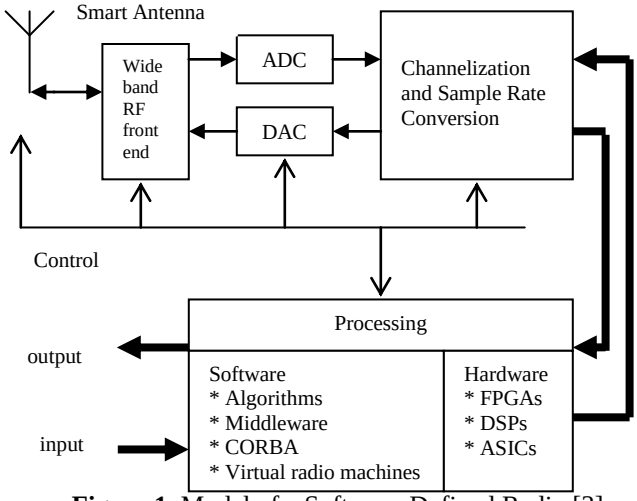

Figure 1. Model of a Software-Defined Radio [3]

The signal processing is performed in software using DSP microprocessors, field programmable gate arrays (FPGAs), or application specific integrated circuits (ASICs). The algorithm used to modulate and demodulate the signal may

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use software methodologies, such as middleware, e.g., common object request broker architecture (CORBA) [5], or virtual radio machines, which are similar in function to JAVA virtual machines.

The noteworthy commercial application of SDR is from Alcatel-Lucent as advertised in their press note [6]. The flexibility of their radio network solutions, as demonstrated with the LTE software module that has been introduced for their 3G NodeBs, is part of a more comprehensive strategy to offer a converged RAN approach. Leveraging years of Bell Labs research in SDR and experience with software-only upgrades, Alcatel-Lucent provides unprecedented flexibility to operators in their network evolution or renovation. Beyond the ability to upgrade 3G base stations to support LTE, their solutions allow different technologies to coexist in a single base station and flexible software based spectrum reframing.

One of the challenges in SDR hardware design is: for the reconfigurable RF front end of the software-defined radio, architectures and circuits should be designed for a broad range carrier frequency, channel bandwidth and noise performance. Meeting the performance parameters over a broad range of frequency is not trivial. The developmental work in the following sections of this paper includes theoretical analysis, hardware design, and testing of RF circuits like Voltage-controlled Oscillators (VCO) and PLL frequency synthesizers used in the local oscillator (LO) section of the wideband transceivers of SDR.

2. Design Theory of Voltage Controlled Oscillator

The VCO design theory is thoroughly presented by the authors of this paper in [7]. The negative resistance theory of the oscillation claims that if the overall resistance of the circuit is negative, the reactive elements of the circuit selects one particular frequency component out of all frequency components present in the thermal noise of a resistor of the circuit; and this frequency component is amplified by the active element of the circuit until the oscillations are sustained. The selection of a transistor as an active element is of primary importance. For a frequency range of a few hundred megahertz to several thousand megahertz, VCOs are commonly built around Bipolar Junction Transistors (BJTs) due to their inherent low noise. Contrary to popular belief, fmax is not the most definitive quantity in the selection of the device. Here, fmax is defined as the frequency at which the unilateral gain falls to unity, and the device ceases to oscillate. With a high fmax the device is susceptible to oscillations outside the desired frequency range, and extraneous coupling between the device leads may arise. Needless to say, if cost is to be kept low, devices with very high fmax are prohibitive. fmax should definitely be within the desired range of operation, but power dissipation is also an important criteria in the selection of the device. Power dissipation is important, as VCO active devices operate at high power levels. Also, care should be taken to control the oscillation totally through the external circuitry with no possible spurious oscillations inside the device. A preliminary simulation/construction of a non-oscillating circuit is necessary in order to prove that the device is free of unwanted spurious oscillations.

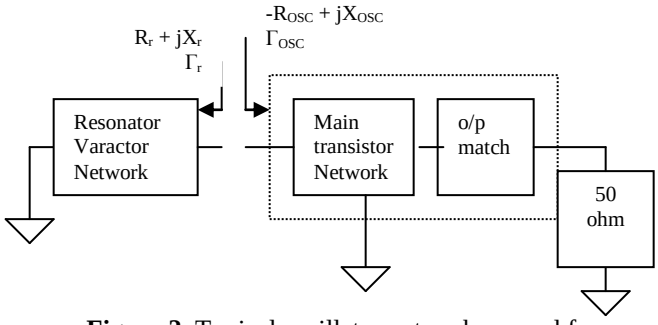

Figure 2. Typical oscillator network as used for graphical/computer analysis

The derivation of the equations for the feedback loop and the forward gain of the device can be very complex in certain cases, and special care should be taken in identifying the two loops. Rohde [8] offers a very good description of that process. In addition to the above, a rather simplistic method of describing the oscillation criteria has been used here. Here, the considerations for the input resistance of the device attempt to explain why the amplitude of the signal starts increasing while building up from the internal noise level. Looking at Figure 2 of a typical oscillator network, it can be seen that this happens when the resistance of the combined active device is greater than the resistance of the load, namely:

$$\left| -R_{OSC} \right| > R_r \text{ and } X_{OSC} = -X_r \qquad (1)$$

As the oscillation amplitude keeps increasing, the DC operating point of the device shifts continuously; thereby changing the transconductance gm of the device and, of course, its input and output impedance. The increase in amplitude will cease when the real parts of the respective impedance and the active device become equal, i.e.

$$\left| -R_{OSC} \right| = R_r \text{ and } X_{OSC} = -X_r \text{ Alternatively, } \Gamma_r \cdot \Gamma_{osc} = 1 \qquad (2)$$

Where Γ_r and Γ_{osc} are the reflection coefficients produced by $R_r + jX_r$ and $R_{OSC} + jX_{OSC}$ respectively. When steady state occurs, the device reaches saturation levels.

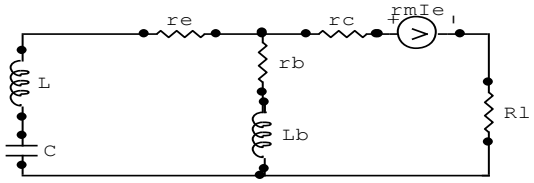

Figure 3. Small signal model for the CB configuration

There are several options available for the main transistor network [9]. The configuration selected for our design is the

common base as shown in figure 3, because it lends itself more easily into oscillation by having 0 degree phase shift and presents an inherent isolation from output (collector) to input (emitter). The L and C are the part of tank circuit connected at the emitter. The Rl is the load resistor at the collector. The Lb is an external inductor connected at the base for the ease of oscillation as explained later. In this CB configuration, we can assume that the internal AC base resistance rb is much less than rc the internal AC collector resistance, an assumption which is true because rb is less than 20 ohms while rc, may well be in the ten megaohm range. Assuming this, we can safely claim that there is a factor α such that rm=α·rc. Here α is called the short circuit current multiplication factor, a quantity greater than or equal to unity, and rm is the transfer resistance of the BJT current generator. The importance of α in the determination of the oscillation conditions is easily seen if we attempt to find the input impedance of the previous circuit. It can be easily proven that the input impedance is:

$$R_{in}= (V_{eb}/I_e)|_{Ic=0} = r_e + r_b\, r_c(1-\alpha)/ (r_b + r_c) \approx r_e + r_b(1-\alpha) \quad (3)$$

We can see that it is possible for a common base configuration to develop a negative input resistance (since α>1) if rb (or rb in series with some impendence) becomes sufficiently large. The latter can be easily satisfied by the addition of an external element like the inductance Lb (Figure 3). In order to examine the stability of such a network let us assume that the admittance matrix of the combined device and base stub is Y consisting of parameters Y11, Y12, Y21 and Y22. If the output port is terminated with a frequency-varying network Yload, the input admittance is given by equation 4. Similarly if the input port is terminated by a frequency-varying network Ysource, then the output admittance will be given by 5.

$$Y_{in} = y_{11} - y_{12}\, y_{21}/(y_{load} + y_{22}) \quad (4)$$
$$Y_{out} = y_{22} - y_{12}\, y_{21}/(y_{source} + y_{11}) \quad (5)$$

In view of equations 4 and 5, the instability of the device can be ascertained by the Linville stability factor;

$$c = \frac{|y_{21}y_{12}|}{2\mathrm{Re}\{y_{11}\}\mathrm{Re}\{y_{22}\} - \mathrm{Re}\{y_{21}y_{12}\}} \quad (6)$$

where c > 1 for instability; or the condition in equation 7 which states than the Z (or Y) matrix of the complete network should be equal to 0. We shall use the second method which gives us a little more insight into the operation of the circuit. We add the output impedance Rl, the inductance Lb and the varactor/inductor combination to the network. We get a network as shown in Figure 3. The following loop equation in matrix form can then be derived.

$$\begin{pmatrix} 0 \\ 0 \end{pmatrix} = \begin{pmatrix} j(wL - 1/wC) + r_e + r_b + L_b & r_b + L_b \\ r_m + r_b + L_b & r_c + R_l + r_b + L_b \end{pmatrix} \begin{pmatrix} I_e \\ I_c \end{pmatrix} \quad (7)$$

The determinant of the above matrix must reduce to 0 for the oscillations to build, so the above equation becomes:
$j(wL-1/wC)(r_c+R_l+r_b+L_b)+r_e(r_c+R_l)+(r_e+R_l+(1-\alpha)r_c)(r_b+L_b)=0$
By setting the reactive part to 0, the resonant frequency is:

$$\omega_0 = 2\pi f_0 = 1/\sqrt{LC} \quad (8)$$

Similarly, by setting the real part to 0 we can show that:

$$\alpha = \left[1 + R_l / r_c\right]\cdot\left[1 + r_e /(r_b + L_b)\right] \quad (9)$$

If α > 1 in equation 9 by properly choosing Rl (i.e. the output matching network) and Lb, we can ascertain that the circuit will oscillate. Furthermore, by properly selecting the value of the capacitance and inductance at the emitter, we can tune the circuit over a range.

3. Design Theory of Phase-locked Loop Frequency Synthesizer

3.1 Basic PLL Operation and Terminology The Phase-Locked Loop (PLL) as shown in figure 4 is very well analyzed by [10]. It starts with a stable crystal reference frequency (XTAL). The R counter divides this frequency to a lower one, which is called the comparison frequency (Fcomp). The phase-frequency detector outputs a current that has an average value proportional to the phase error between the comparison frequency and the output frequency, after it is divided by the N divider. The constant of proportionality, Kφ turns out to be the magnitude of the current that the charge pump can source or sink. If this average DC current from the phase detector is multiplied with the impedance of the loop filter, Z(s), then the input voltage to the VCO can be found. The typical third order (three capacitor) loop filter is also shown in the figure 4 that basically converts the current pulses from the output of the phase detector into average voltage. If the tuning voltage range of the VCO is more than that can be supplied by the charge pump output, then the active loop filter using OPAMP and resistor-capacitor network is used to expand the voltage range. The VCO is a voltage to frequency converter with a constant of Kvco. This tuning voltage adjusts the output phase of the VCO, such that its phase, when divided by N, is equal to the phase of the comparison frequency. Since phase is the integral of frequency, this implies that the frequencies will also be matched, and the output frequency is:

$$Fout = N \bullet Fcomp \quad (10)$$

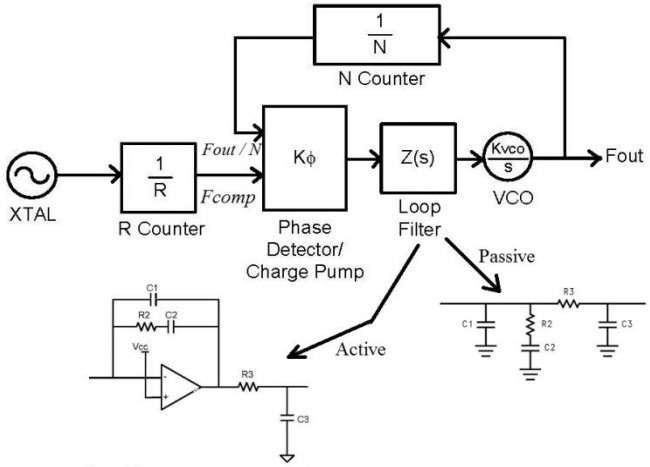

Figure 4. Block Diagram of a Phase Locked Loop [10]

For a given application, R is typically fixed, and by programming N counter, the local oscillator frequency can be changed to tune different channels of the wideband transceivers. If N and R are integers, then the PLL can only generate frequencies that are a multiple of Fcomp. For this reason, many people think that Fcomp and the channel spacing are the same. Although this is often the case, this is not necessarily true. For a fractional N PLL, N is not restricted to an integer, and therefore the comparison frequency can be chosen to be much larger than the channel spacing. In general, keep the comparison frequency as high as possible for optimum performance. The transfer function from the output of the R counter to the output of the VCO determines a lot of the critical performance characteristics of the PLL. The closed loop bandwidth of this system is referred to as the loop bandwidth (Fc), which is an important parameter for both the design of the loop filter and the performance of the PLL. Another parameter, phase margin (φ), refers to 180 degrees minus the phase of the open loop phase transfer function from the output of the R counter to the output of the VCO. The phase margin is evaluated at the frequency that is equal to the loop bandwidth. This parameter has less of an impact on performance than the loop bandwidth, but still does have a significant impact and is a measure of the stability of the system. It gives a limit by which the phase response of the overall loop can change before the loop goes into oscillation, ideally to be designed to be 50 degrees.

The spurs are the undesired spurious outputs that appear at a spacing of Fcomp from the carrier. In the locked condition, the charge pump is off for the majority of the time. When the charge pump is off, leakage causes the VCO tuning voltage to drop. This can cause an undesired AC signal on the tuning line which FM modulates the VCO output causing spurs. Reference spurs that are too large can interfere with other channels and cause other problems and are usually kept below some desired level. Loop bandwidth (explained in the next section) controls the level of reference spurs. Lower the loop bandwidth, higher the rejection of the reference spurs [11].

The lock time is defined as the time that it takes for the PLL to change from one frequency to another for a given frequency step size to within a given tolerance. Eg. 500 uS to within 500 Hz for a frequency jump of 50 MHz (changing from 865 to 915 MHz for example). The rule of thumb is: lock time = 3/(loop bandwidth). Higher the loop bandwidth, faster the loop locks to the new frequency [11].

3.2 PLL Noise Sources The instantaneous frequency of the oscillator is not constant; it varies slightly about the nominal frequency creating an uncertainty in the frequency at any given point in time. This frequency change can be viewed as a change in time of the waveform edge from the ideal nominal frequency edge. This change in time of the edge is called jitter. The phase noise is the frequency domain representation of rapid, short-term, random fluctuations in the phase of a waveform, caused by time domain instabilities i.e. jitter. It is expressed as a graph of power vs. frequency. The noise sources in the PLL loop are the active devices: Crystal, dividers, charge pump and VCO. This noise is shaped by the closed loop response of the system.

The way to convert the standard PLL diagram of figure 4 into figure 5 is to understand that the phase detector is simply taking the difference of two phases. Because of this the noise sources are viewed as noise on the phase of the signal or "phase noise". Once the diagram is drawn, this represents a classical control loop from the control theory:

$$G = K\varphi \cdot (Kvco/s) \cdot Z(s) \quad (11)$$

$$H = 1/N \quad (12)$$

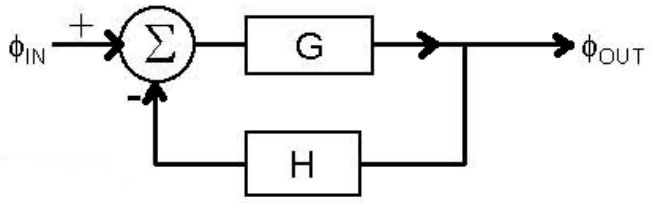

Figure 5. Derivation of Noise Transfer Function

Note that H is constant and G is a decreasing function with respect to $s = j\omega$. For the basic system with feedback, it can be shown that the transfer function is G/(1+GH). This is called the closed loop gain. Table 1 summarizes the transfer functions for various noise sources in the loop. The loop bandwidth is the frequency at which GH is unity. It can be thought of as a corner frequency. It will be shown later that it has a large influence on the reference spurs and lock time. Note that for noise frequencies that are less than the loop bandwidth, the crystal, counters, and charge pump dominate. In most cases, the charge pump is the most dominant of these three sources. For frequencies that are much higher than the

loop bandwidth, all these noise sources are greatly attenuated and the VCO noise becomes the dominant source. The crystal noise is divided by R, which implies a higher R counter divides this noise more. Also, the charge pump noise is divided by the charge pump gain, which implies the best phase noise occurs when the highest charge pump current is used (in the case of PLLs with selectable charge pump currents).

Table 1. Transfer Functions for Loop Noise Sources[10]

Noise Sources	Transfer Function	Low Frequency (GH >> 1)	High Frequency (GH << 1)
Crystal	(1/R)·G/(1+GH)	(1/R)·N	(1/R)·G
R Counter	G/(1+GH)	N	G
N Counter	G/(1+GH)	N	G
Charge Pump	(1/ *K*φ)·G/(1+GH)	N/*K*φ	G
VCO	1/(1+GH)	1/GH	1

The factor G/(1+GH), which is the loop gain, is common to all noise sources except the VCO. This function is a constant (equal to N) for smaller frequency values (less than the loop bandwidth) and is a decreasing function for higher frequency values (greater than the loop bandwidth). The fact that all these transfer functions contain a factor of N imply that if the N divider value is increased, the phase noise increases by a factor of 20*log(N). The one important thing to remember that increasing the comparison frequency increases the charge pump noise by a factor of 10*log(Fcomp). Outside the loop bandwidth, all these noise sources are attenuated because G is a decreasing function. The transfer function of the VCO is highpass, so VCO noise is high pass filtered, whereas all other noise sources are multiplied by N and low pass filtered because of the low pass nature of the loop.

4. Hardware Designs of 1200 – 1800 MHz and 1800 – 2400 MHz VCOs

Based on the theory presented in the previous sections of this paper, we have simulated, designed, fabricated and tested two VCOs.

4.1 Simulation using Genesys A proper method for simulation of oscillating circuit is the nonlinear approach, which can be achieved by using Genesys from Agilent Technologies. Our goal was to simulate for two VCOs: the first one in 1200-1800 MHz range, and second in 1800-2400 MHz range.

As per the theory presented in previous section, for any circuit to oscillate, the following have to be met:

$$\Gamma_r \cdot S_{11}=1 \text{ and } \Gamma_l \cdot S_{22}=1 \qquad (13)$$

But to start oscillation and to build up the voltage, value of Γr·S11 and Γl·S22 should be greater than unity. Also, the reflection coefficient at output side of the main transistor circuit should be as high as possible. Another condition for oscillation is: total impedance of the circuit should be nonpositive so that oscillations do not cease. Through Genesys, the circuit is to be made which have maximum reflection coefficient at output side and maximum negative impedance of the main transistor circuit. And to make the oscillations controlled by external tuning voltage, the variable capacitor (varactor diode) is to be used through which the oscillation frequency can be varied from, for example, 1200 MHz to 1800 MHz. First of all, to fulfill the conditions, only RF part as shown in figure 6 i.e. main transistor part without DC biasing is simulated and the range of the variable capacitor is found.

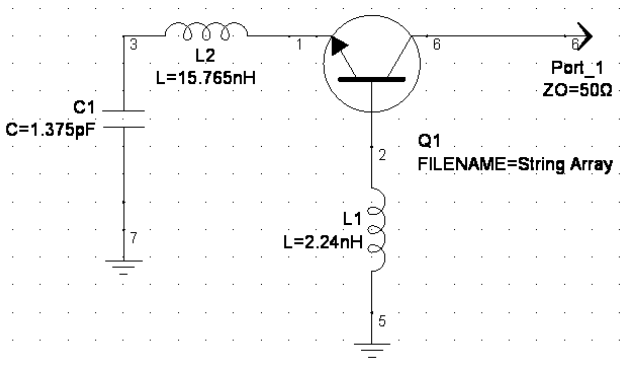

Figure 6. Circuit for the simulation

Now, to get oscillations at different frequencies, the capacitor C1 is kept variable and from optimization method for different values of capacitor, two basic conditions to start oscillations i.e. maximized S11 (reflection from output port) and negative resistance of the circuit are fulfilled. The results of this simulation for the 1200-1800 MHz VCO are summerized in table 2.

Table 2. Various parameters as C_1 is tuned

Frequency of Oscillation, MHz	Capacitance value, pF	S11 (dB)	Real (Z)
1200	5.76	4	-168.3
1300	3.98	7	-111.36
1500	2.90	13.5	-88.58
1600	2.20	22	-60.1
1700	1.763	7.2	-53.4
1800	1.375	3	-43.1

To simulate the PLL synthesizer operation, Texas Instrument's WEBENCH EasyPLL simulation tool is used. It takes VCO and loop parameters as inputs and gives designs of the loop filter and simulates the phase noise, loop lock time etc parameters. Active loop filters are used for the both VCOs as the tuning voltage requirement is higher than the PLL IC supply voltage.

4.2 Hardware Design and Test The discussions in the VCO design section reveals that the inductive reactance at the base of the transistor in the common base configuration helps achieving negative resistance required for the oscillation. Therefore, a circuit configuration of figure 7 was designed for

the 1200 to 1800 MHz VCO circuit. The RFC is high inductance decoupling RF from the DC supply at collector side and also at emitter side decoupling emitter resistor. The inductance at base L_b is required for the oscillation. The capacitors C_c are for coupling RF and blocking the DC. The transistor is biased at 12 mA of collector current to give approximately 5 dBm output. The transistor used is NEC's NE85633 with cut off frequency of 7 GHz and noise figure of 1.4 dB. The varactors selected BB535 and BB515 are from Infineon Technologies and have very low series resistance (less than 0.58 ohms), so that its effect on phase noise of the oscillator is minimized. The specifications are listed in table 3. Two varactors are used to give wider range, one at the base and the other at the emitter resulting into almost 600 MHz of range. To get 1800 to 2400 MHz range, the base inductor L_b value is decreased and one of the varactor with lower capacitance is used. The printed circuit board using FR4 material was designed and then components were populated as shown in figure 8.

The actual VCO was integrated into a phase-locked loop using Texas Instruments PLL IC LMX2434. We used the evaluation boards of LMX2434 and populated our VCOs and active loop filters on it [12]. The PLL is a dual PLL with RF and IF sections, so we locked VCO2 with RF and VCO1 with IF section. To incorporate 15 volts of tuning range, an active loop filters were designed using the simulation tool Webench EasyPLL from Texas Instruments [13]. The photograph of the complete hardware covering VCOs, PLL and active loop filters is shown in figure 9. The hardware was tested and gives frequency versus the tuning voltage performance as shown in figure 10. It exhibits excellent phase noise characteristics: at 2300 MHz; -95 dBc/Hz at 10 kHz from the carrier and -75 dBc/Hz at 1 kHz. Various phase noise plots taken on the spectrum analyzer are shown in figure 11. The output power variation across the range for a 1200-1800 MHz VCO is +/- 2.5 dB. The tuning sensitivity is 50-70 MHz/V and the absolute maximum tuning voltage is 15 Volts. The approximate frequency pulling (change in frequency when output is mismatched) is 17 MHz and frequency pushing (change in frequency when bias is changed) is 3 MHz per Volt. Similar are the results for the second VCO (1800 to 2400 MHz) as tabulated in table 4. Comparing our design with a commercially available design from Analog Devices [14], our design has improved performance as highlighted in table 5.

Table 3. Varactor specifications

Varactor	Capacitance ratio (C @ V_R=1V)/ (C @ V_R=14V)	Series Resistance
BB515	18 pf / 4 pf = 4.5	0.5
BB535	18.7 pf / 3 pf = 6.2	0.58
BB833	9.5 pf / 1 pf = 9.5	1.8

Table 4. Performance parameters of the VCO designed

Parameter	VCO #1	VCO #2
Frequency range	1200-1800 MHz	1800-2400 MHz
Phase Noise	-95 dBc/Hz at 10 kHz offset	-95 dBc/Hz at 10 kHz offset
Amplitude	+5 dBm +/- 2.5 dB	+5 dBm +/- 2.5 dB
Tuning sensitivity	50-70 MHz/V	50-70 MHz/V
Frequency pulling	17 MHz	25 MHz
Frequency pushing	3 MHz/Volt	6 MHz/Volt
PLL Loop BW	800 Hz	800 Hz
DC current	12 mA @ 5 V	12 mA @ 5 V

Table 5. Phase Noise Performance Comparison

Phase Noise of 2300 MHz signal @ 1 MHz offset	Analog Devices Part # ADRF6702 -125 dBc/Hz	Our Design -140 dBc/Hz 15 dB better
Phase Noise of 950 MHz signal @ 1 MHz offset	Analog Devices Part # ADRF6701 -135 dBc/Hz	Our Design -140 dBc/Hz 5 dB better

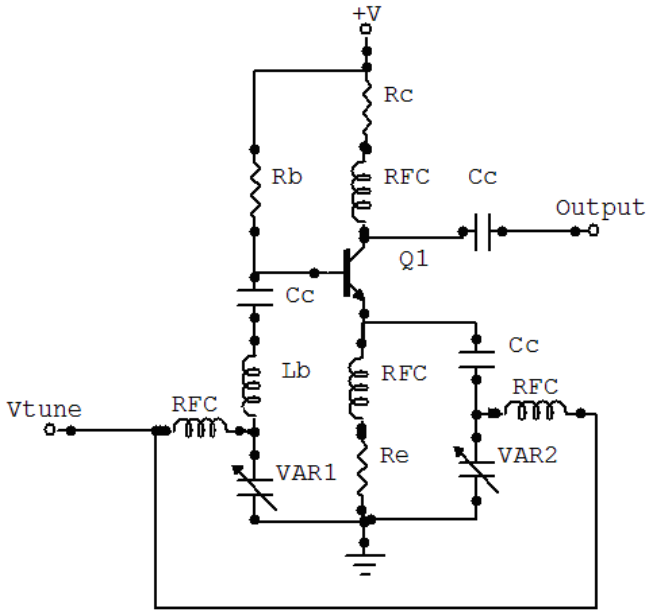

Figure 7. Circuit diagram of the VCO

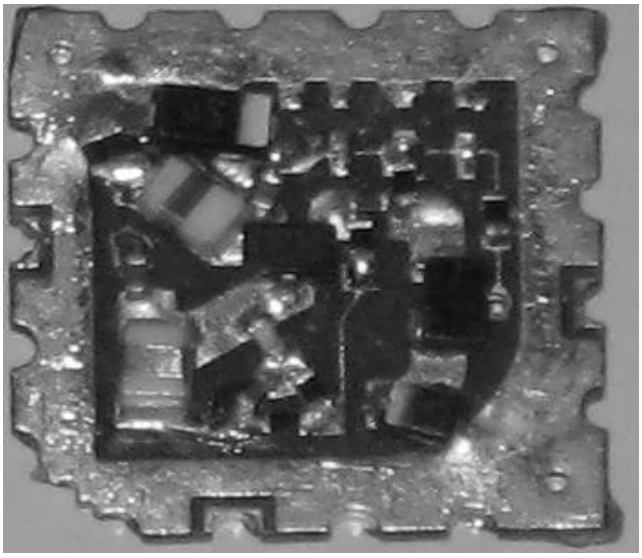

Figure 8. Hardware realization of the 1200-1800 MHz VCO

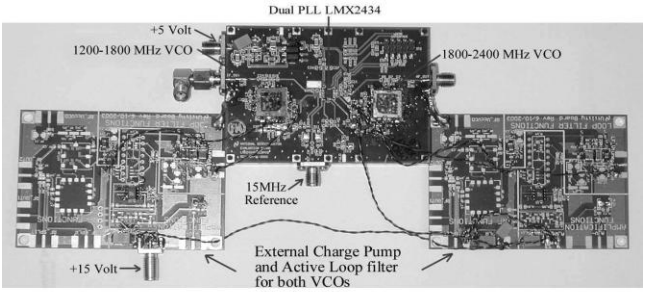

Figure 9. Hardware realization of the 1200-2400 MHz PLL Frequency Synthesizer

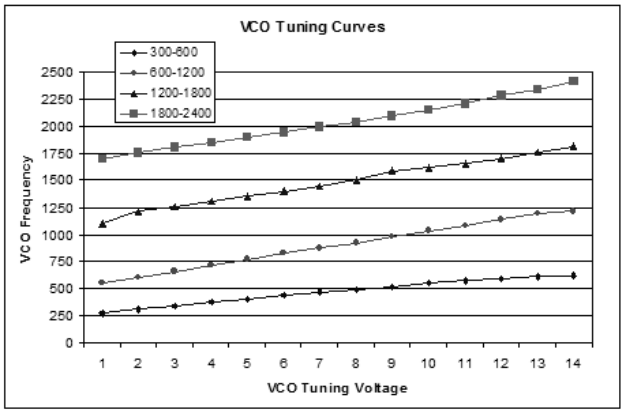

Figure 10. VCO tuning curves

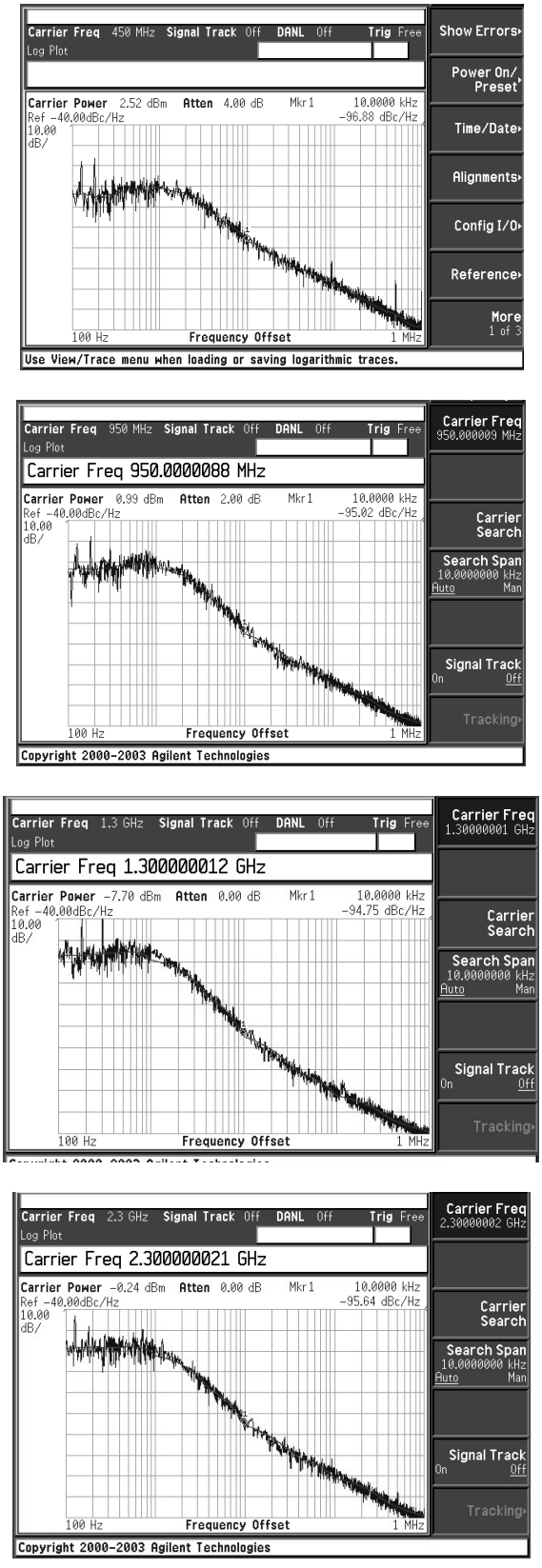

Figure 11. Typical phase noise plots at 450, 950, 1300 MHz and 2300 MHz

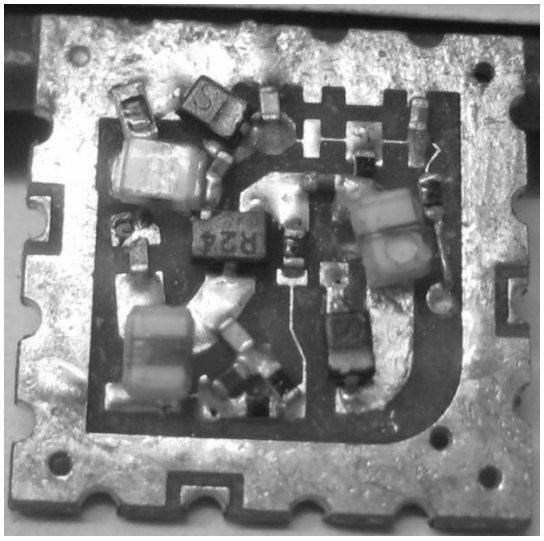

Figure 12. Hardware of the 600-1200 MHz VCO

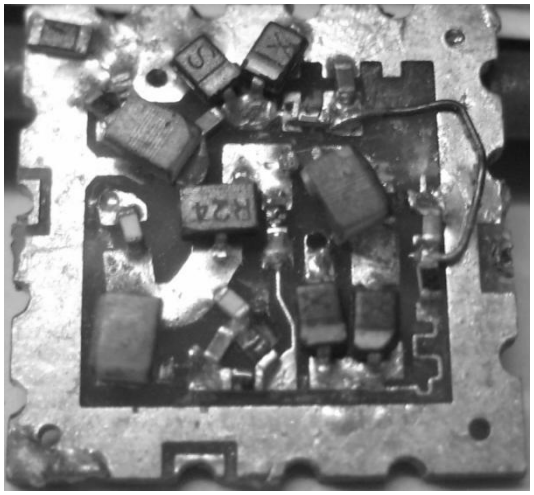

Figure 13. Hardware of the 300-600 MHz VCO

5. Hardware Designs of 300 – 600 MHz and 600 – 1200 MHz VCOs

After applying the VCO design theory to fabricate VCOs covering 1200-2400 MHz range, to validate the design we have designed two more VCOs to extend the overall frequency range of our VCOs: one covers 300 to 600 MHz and the other covers 600 to 1200 MHz. The key is to change the base inductor Lb, the varactors, and the configuration in which varactors are used. The value of inductor Lb for these VCOs is higher than that required for the previous section's VCOs. Also, to get the range of 300 to 600 MHz, two varactors (BB535 and BB833 from Infineon) are used in parallel at emitter and two varactors (both are BB835 from Infineon) are used in series at the base. For the 600 to 1200 MHz range, a varactor BB535 at emitter and BB535 at base is used. The values of base inductor Lb are appropriately selected to get range in both cases. The tuning curves are shown in figure 10 and typical phase noise plots in figure 11. The snapshots of these two designs are shown in figure 12 and 13. Our design performs 5 dB better compared to Analog Devices part # ADRF6701 [15] as shown in table 5.

6. Conclusion

The need of the time is the radio that can be used over a wide frequency range, and globally in all standards, interfaces and applications. One of the requirements of such SDR radio is designing RF front end including local oscillators operating over wide frequency range. A concise reviews of the voltage controlled oscillator design and phase-locked loop design have been presented, and the results of applying theory to implement wideband VCO models and PLL frequency synthesizer have been demonstrated. The actual PLL frequency synthesizer using these VCOs was built covering 1200 to 1800 MHz and 1800 to 2400 MHz. This particular design and other designs based on this e. g. 300 to 600 MHz and 600 to 1200 MHz VCOs that basically covers 0.3 GHz to 2.4 GHz frequency range find very good applications in the wideband RF front end of the SDR base stations.

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