Wideband Local Oscillator Design for Wideband Transceivers

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Abstract- **The wideband transceivers like the software defined radio require designing wideband RF hardware covering octave bands. The local oscillator of the mixer should be a wideband frequency synthesizer. Building on the theory of oscillations in the voltage controlled oscillator, the paper reviews the concept of negative resistance in the transistor circuit with some base inductance. It also provides simulation of this concept. To apply the theory and simulation, the actual VCO hardware was designed and fabricated for the range covering 1200 to 2400 MHz. These VCOs were used in the design of wideband PLL frequency synthesizer. The results including very good phase noise performance are presented. This approach can be used to design wideband synthesizers in other RF range.**

Keywords- **Software-defined Radio, Voltage Controlled Oscillator, Phase Noise, Frequency Synthesizer**

I. INTRODUCTION

The requirements of the mobile telephony are continuous coverage throughout the world and ease of interfacing with different systems and standards. To meet these requirements, the mobile devices must have reconfigurable hardware and reprogrammable software. Such radios, known as Software-Defined Radios (SDR) can be implemented efficiently using software radio architectures in which the radio reconfigures itself based on the system it will be interfacing with and the functionalities it will be supporting [1, 2].

The smart antenna system in SDR combats the multipath effects and co-channel interference [3]. Then, it would require either the conversion of RF into baseband at the antenna or the design of a completely flexible radio RF front-end for handling a wide range of frequencies [4]. Digitizing the signal with an analog to digital converter (ADC) in the IF range eliminates the last stage in the conventional model in which problems like carrier offset and imaging are encountered.

For the reconfigurable RF front end of the SDR wideband transcievers, the architectures and circuits should be designed for a almost octave band carrier frequency with better noise performance. The following work includes theory, design, simulation, fabrication and test & optimization of voltage controlled oscillator based PLL synthesizer for the frequency range 1200 to 2400 MHz that can be used perfectly as a wideband local oscillator in SDR.

II. VCO AND PLL DESIGN

The VCO design theory was developed by the authors of this paper in their previous work [5]. The design theory of that research paper is now extended in the range of 1200 MHz to 2400 MHz to design VCOs covering this range. To establish a design platform, the same theory is presented here briefly.

A proper way to describe the oscillation process is through a thorough derivation of the feedback network of the device, with an application of the Barkhausen criteria. The Barkhausen criteria states that the product of the forward gain path and the feedback path for the complete oscillator network should be equal to unity, while the feedback loop should add the output wave form to the input of the combined network with no phase shift (i.e. positive feedback). Rohde [6] offers a very good description of that process.

A rather simplistic method of describing the oscillation criteria has been used here. This process is not favored for its insight in the operation of the device, but rather for its ease of application. There are several options available for the main transistor network [7]. A common base configuration is used, with the feedback element in series or parallel from.

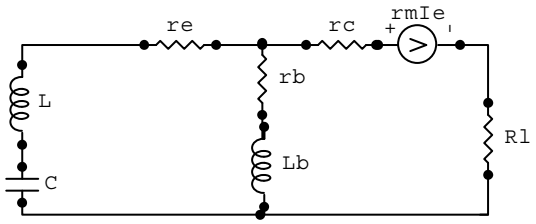


Fig. 1. Small signal model for the common-base configuration [5]

The configuration selected for our design is the common base as in figure 1, because it lends itself more easily into oscillation and presents an inherent isolation from output (collector) to input (emitter). The L and C are the part of tank circuit connected at the emitter. The R_l is the load resistor at the collector. The L_b is an external inductor connected at the base for the ease of oscillation as explained later. In this CB configuration, we can assume that the internal AC base resistance r_b is much less than r_c the internal AC collector resistance, an assumption which is true because r_b is less than 20 ohms while r_c, may well be in the ten megaohm range. Assuming this, we can safely claim that there is a factor α such that $r_m = \alpha \cdot r_c$. Here α is called the short circuit current multiplication factor, a quantity greater than or equal to unity, and r_m is the transfer resistance of the BJT

current generator. It can be proven that the input impedance is :

$$R_{in} = r_e + r_b r_c(1-\alpha)/(r_b + r_c) = r_e + r_b(1-\alpha) \quad (1)$$

From 1 we can see that it is possible for a common base configuration to develop a negative input resistance (since $\alpha>1$) if r_b (or r_b in series with some impendence) becomes sufficiently large. The latter can be easily satisfied by the addition of an external element like the inductance L_b (Figure 1). The frequency of oscillation f_0 is proved to be:

$$f_0=(1/2\pi)\sqrt{(1/LC)} \quad (2)$$

If $\alpha > 1$ in equation 1 by properly choosing R_l (i.e. the output matching network) and L_b (the inductance of the lumped inductor or microstrip inductor), we can ascertain that the circuit will oscillate. Furthermore, by properly selecting the value of the capacitance/ inductance at the emitter, we can tune the circuit over a range.

The phase locked Loop (PLL) is then used to lock the VCO. The typical PLL block diagram as in figure 2 shows a crystal oscillator frequency divided by R to become the comparison frequency F_{COMP}, usually equal to the channel bandwidth of the transceiver. The phase detector produces output proportional to the phase difference of its input signals. The loop filter usually is a resistor-capacitor network that converts the current pulses coming out of the phase detector into a slow varying voltage signal that controls the output frequency of the VCO.

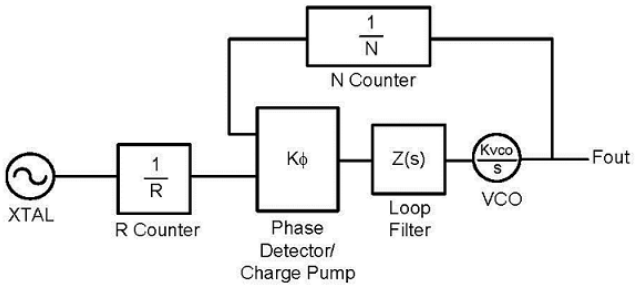


Fig 2: Phase Lock Loop Block Diagram [8]

The output frequency F_{OUT} is N times the F_{COMP}. By programming N counter, the local oscillator frequency can be changed to tune different channels of the wideband transceivers. The system function from the R counter output to the F_{OUT} is known as a loop and the loop bandwidth is an important parameter for both the design of the loop filter and the PLL performance. Higher the loop bandwidth, faster the loop locks to the programmed frequency, however, more amplitude of the reference spurs leak into the VCO output frequency. The reference frequency F_{COMP} and its harmonics actually modulate the VCO output and appears as spurs around the center frequency F_{OUT}. Another performance parameter is the phase noise that is related to the power of the noise of the PLL.The smaller the N counter value, the better the phase noise of the VCO output frequency as the N counter actually multiplies the noise. The PLL design related practical information is given in detail in [8].

III. CIRCUIT SIMULATION

A proper method for simulation of oscillating circuit is the nonlinear approach, which can be achieved by using Genesys from Agilent Technologies. Our goal was to simulate for two VCOs: the first one in 1200-1800 MHz range, and second in 1800-2400 MHz range.

According to the theory presented in previous section, for any circuit to oscillate, the following have to be met:

$$\Gamma_r \cdot S_{11}=1 \text{ and } \Gamma_l \cdot S_{22}=1 \quad (3)$$

But to start oscillation and to build up the voltage, value of $\Gamma_r \cdot S_{11}$ and $\Gamma_l \cdot S_{22}$ should be greater than unity. If we talk about second equation, reflection coefficient at output side of the main transistor circuit should be as high as possible. Another condition for oscillation is: total impedance of the circuit should be nonpositive so that oscillations do not cease. Through Genesys, the circuit is to be made which have maximum reflection coefficient at output side and maximum negative impedance of the main transistor circuit. And to make the oscillations controlled by external tuning voltage, the variable capacitor (varactor diode) is to be used through which the oscillation frequency can be varied from, for example, 1200 MHz to 1800 MHz. First of all, to fulfill the conditions, only RF part as shown in figure 3 i.e. main transistor part without DC biasing is simulated and the range of the variable capacitor is found.

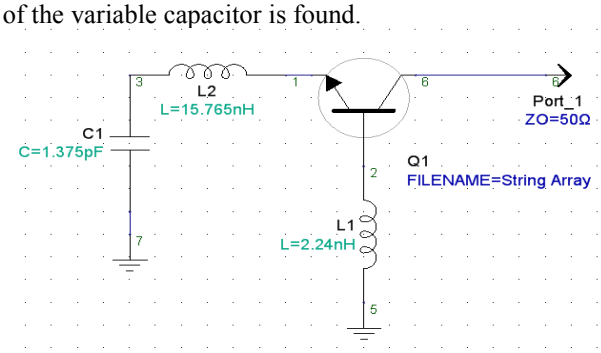


Fig 3: Circuit for the simulation

Now, to get oscillations at different frequencies, the capacitor C_1 is kept variable and from optimization method for different values of capacitor, two basic conditions to start oscillations i.e. maximized S_{11} (reflection from output port) and negative resistance of the circuit are fulfilled. The results of this simulation for the 1200-1800 MHz VCO are summerized in table 1.

To simulate the PLL synthesizer operation, National Semiconductor WEBENCH EasyPLL simulation tool [9] is used. It takes VCO and loop parameters as inputs and gives designs of the loop filter and simulates the phase noise, loop lock time etc parameters. Active loop filters are used for the both VCOs as the tuning voltage requirement is higher than the PLL IC supply voltage.

IV. HARDWARE DESIGN AND TEST

Based upon the design theory of section I we conclude that inductive reactance at the base of the transistor

in the common base configuration helps achieving negative resistance required for the oscillation. Therefore, a circuit configuration of figure 4 was designed for the VCO circuit. The RFC is high inductance decoupling RF from the DC supply at collector side and also at emitter side decoupling emitter resistor. The inductance at base is required for the oscillation. The capacitors C_c are for coupling RF and blocking DC. Two varactors are used to give wider range, one at the base and the other at the emitter resulting into almost 600 MHz of range. The transistor is biased at 12 mA of collector current to give approximately 5 dBm output. The printed circuit board using FR4 material was designed and then components were populated as shown in figure 5. The same circuit board was used to populate two different VCOs. The transistor used is NEC's NE85633 with cut off frequency of 7 GHz and noise figure of 1.4 dB. The varactors selected are from Siemens sample kit and have very low series resistance (less than 0.5 ohms), so that its effect on phase noise of the oscillator is minimized.

TABLE 1. Various parameters as C_1 is tuned

Frequency of oscillation, MHz	Capacitance Value, pF	S11(dB)	real(Z)
1200	5.76	4	-168.3
1300	3.98	7	-111.36
1500	2.90	13.5	-88.58
1600	2.20	22	-60.1
1700	1.763	7.2	-53.4
1800	1.375	3	-43.1

The actual VCO hardware was then tested by designing a PLL frequency synthesizer using National Semiconductor's LMX2434. We used the evaluation boards of LMX2434 and populated our VCOs and active loop filters on it. The PLL is a dual PLL with RF and IF sections, so we locked VCO2 with RF and VCO1 with IF section. To incorporate 15 volts of tuning range, an active loop filters were designed using the simulation tool Webench EasyPLL from National Semiconductor [9]. The photograph of the complete hardware covering VCOs, PLL and active loop filters is shown in figure 6. The hardware was tested and gives frequency Vs tuning voltage performance as shown in figure 7. It exhibits excellent phase noise characteristics: At 2300 MHz; -95 dBc/Hz at 10 kHz from the carrier and -75 dBc/Hz at 1 kHz (figure 8). The output power variation and the tuning voltage across the range for a 1200-1800 MHz VCO is +/- 2.5 dB. The VSWR is 1.80:1 across the band or better. The tuning sensitivity is 50-70 MHz/V and the absolute maximum tuning voltage is 15 Volts. Typical frequency pulling is 17 MHz peak to peak and frequency pushing 3 MHz per Volt. Similar are the results for the second VCO (table 2).

Comparing our design with commercially available synthesizer from Analog Devices [10], our design has significantly improved performance as highlighted in table 3.

V. CONCLUSION

A concise review of the voltage controlled oscillator design has been presented, and the results of applying to wideband VCO models have been demonstrated. The actual PLL frequency synthesizer using these VCOs was built covering 1200 to 1800 MHz and 1800 to 2400 MHz. This particular design and other designs based on this find very good applications in the wideband front RF end of the software-defined radio, which requires reconfigurable wideband local oscillators. This particular design may find application in the basestation transceiver as it has a good phase noise and wider tuning voltage required. For handheld application where low voltage and compact size are required, the integrated approach should be followed.

TABLE 2. Performance parameters of the VCO designed

Parameter	VCO #1	VCO #2
Frequency range	1200-1800 MHz	1800-2400 MHz
Phase Noise	-95 dBc/Hz at 10 kHz offset	-95 dBc/Hz at 10 kHz offset
Amplitude	+5 dBm +/- 2.5 dB	+5 dBm +/- 2.5 dB
Output VSWR	1.80:1	1.80:1
Tuning sensitivity	50-70 MHz/V	50-70 MHz/V
Frequency pulling	17 MHz	25 MHz
Frequency pushing	3 MHz/Volt	6 MHz/Volt
PLL Loop BW	800 Hz	800 Hz
DC current	12 mA @ 5 V	12 mA @ 5 V

TABLE 3. Phase Noise Performance Comparison

	Analog Devices Part # ADRF6702	Our Design
Phase Noise @ 1 MHz offset	-125 dBc/Hz	-140 dBc/Hz **Improvement of 15 dB**

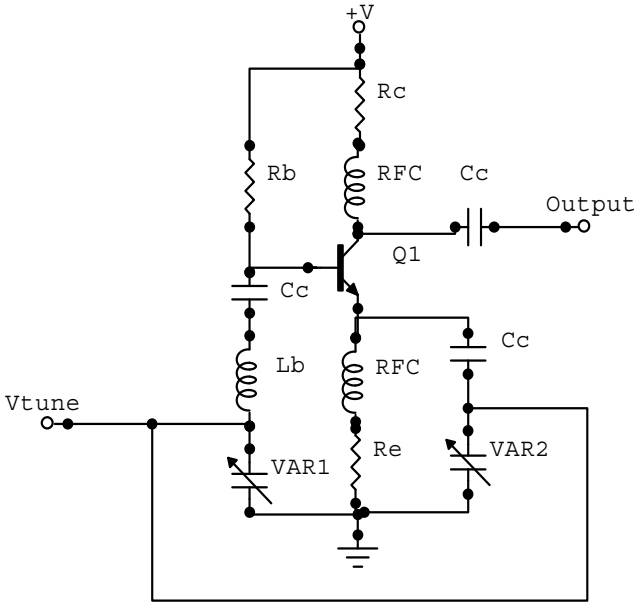


Fig 4: Circuit diagram of the VCO

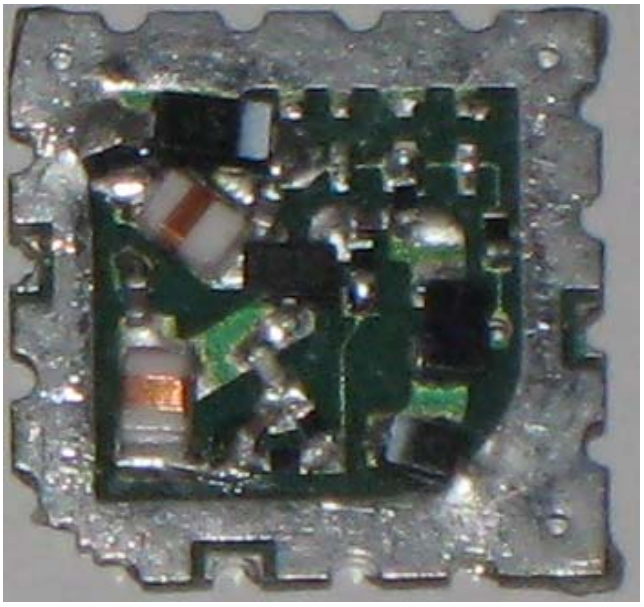


Fig 5: Hardware realization of the 1200-1800 MHz VCO

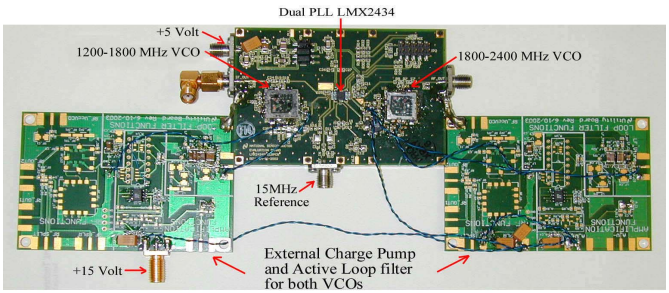


Fig 6: Hardware realization of the complete circuit

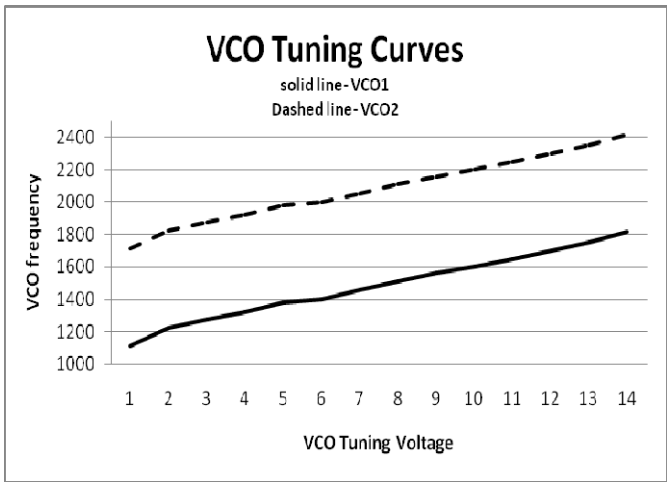
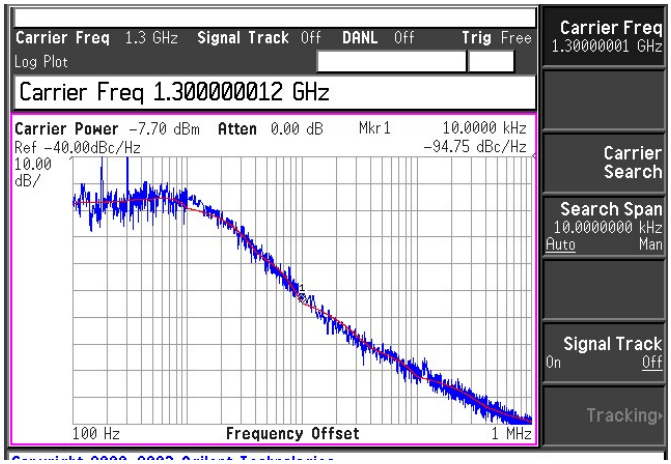


Fig 7: VCO tuning curves



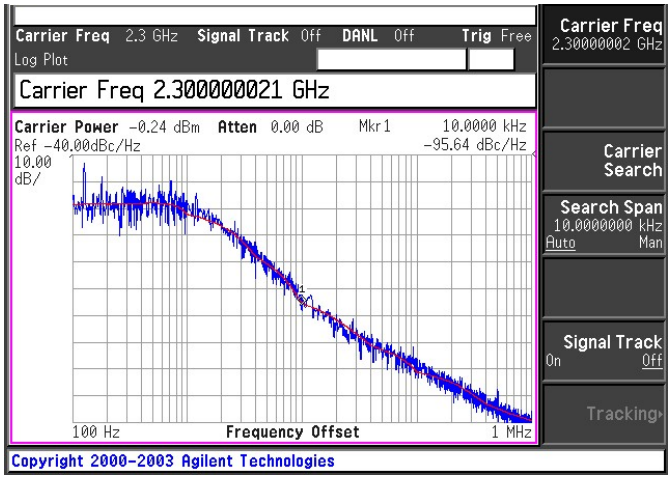


Fig 8: Typical phase noise plot at 1300 MHz and 2300 MHz

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