Journal of VLSI Design Tools and Technology
ISSN: 2249–474X
www.stmjournals.com

Design and Analysis of Source Current Effect on Preamplifier-Positive Feedback-based CMOS Comparator Using 90 nm Technology

Vijay Savani*[*], *NM Devashrayee
Institute of Technology, Nirma University, India

Abstract

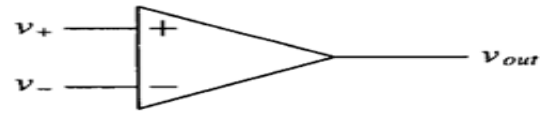
One of the most important and essential components of the data converter circuit is the comparator and this paper presents the implementation and characterization of the basic and simplest CMOS comparator in 90 nm technology. Once the technology scales down, the design and implementation becomes an essential issue at sub-micron and deep-sub-micron technology. The behavior of the threshold voltage in the CMOS is not a linear quantity when the parameters of the CMOS are scaled down. The paper shows implementation and characterization of the basic comparator in 90 nm technology. The simulation has been carried out for the different values of the current biasing to show how it effects the power dissipation and the delay. The implementation has been carried out using Mentor Graphics IC Studio tool and simulation is being carried out using Eldo tool.

Keywords: CMOS, deep-sub-micron technology, threshold voltage, comparator

[*]***Author for Correspondence*** E-mail: vijay.savani@nirmauni.ac.in

INTRODUCTION OF A COMPARATOR

Digitization of everything is the current scenario and the data converter works as a bridge between analog word and the digital word. The comparator is the basic block in the data converter circuit; this device compares two voltages or currents and switches its output to indicate which is larger and generates output accordingly. The comparator is the most important part in the Flash ADC or portable systems in today's life. As the scaling of CMOS technology continues, the supply voltage gets lower and it inherently limits the maximum input voltage swing [1–6]. The circuit symbol of a comparator is shown in Figure 1.



$v_+ > v_-$ then $v_{out} = VDD =$ logic 1
$v_+ < v_-$ then $v_{out} = VSS =$ logic 0

Fig. 1: *Symbol of a Comparator.*

The schematic symbol and basic operation of a comparator are shown in Figure 1. The comparator can be thought of as a decision-making circuit. If the V+ input of the comparator is at a greater potential than the V− input, the output of the comparator is a logic 1, whereas if the V+ input is at a potential less than the V− input, the output of the comparator is a logic 0. Although the basic op-amp can be used as a comparator in some less demanding low-frequency or speed applications, but here a separate comparator circuit is considered.

BASIC BLOCKS OF A COMPARATOR

A block diagram of a high-performance basic comparator is shown in Figure 2. The basic comparator consists of three stages:

1. The input preamplifier
2. Positive feedback or decision stage
3. Output buffer

The preamp stage (or stages) amplifies the input signal to improve the comparator sensitivity (i.e.,

increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise coming from the positive feedback stage. The positive feedback stage is used to determine which of the input signals is larger. The output buffer amplifies this information and outputs a digital signal. Designing a comparator can begin with considering input common-mode range, power dissipation, propagation delay, and comparator gain.

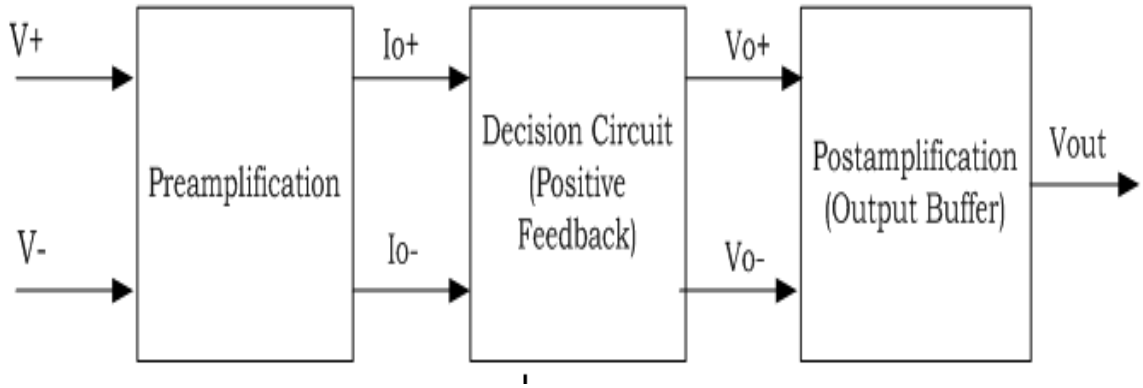


Fig. 2: *Block Diagram of a Basic Comparator* [2].

Preamplifier Stage

A basic comparator preamplification circuit is shown in Figure 3. This circuit is a differential amplifier with active loads. The sizes of M1 and M2 are set by considering the diff-amp transconductance and the input capacitance[7–9].

The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of Ml and M2. To further increase the gain of the first stage, widths of MOSFETs M3 and M4 relative to the widths of M31 and M41 can be changed. Using the sizes given in the schematic, we can relate the input voltages to the output currents by

$$io+ = \frac{gm}{2}(V+ - V-) + \frac{Iss}{2} = Iss - io-$$

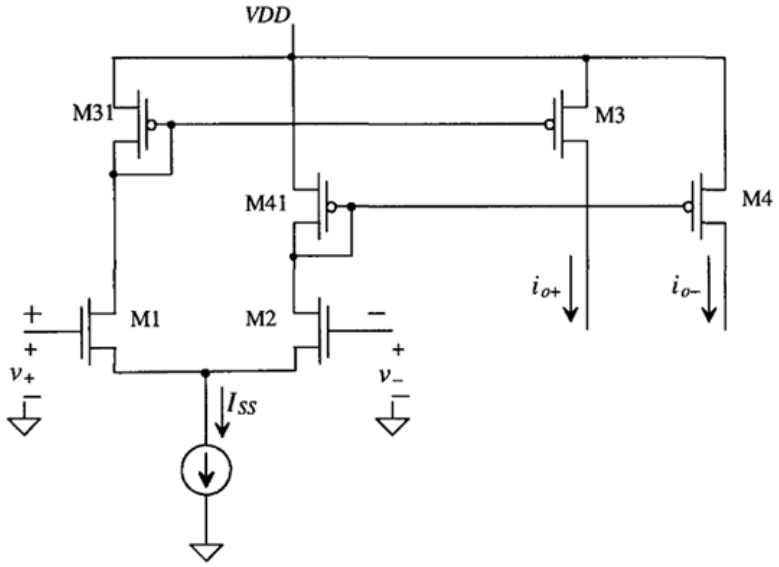


Fig. 3: *Pre-amplification Stage of a Basic Comparator* [2].

Positive Feedback or Decision Stage

The decision circuit is the heart of a basic comparator and should be capable of discriminating mV level signals. The circuit should be able to reject noise signal. The basic comparator decision circuit is shown in Figure 4. The circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element.

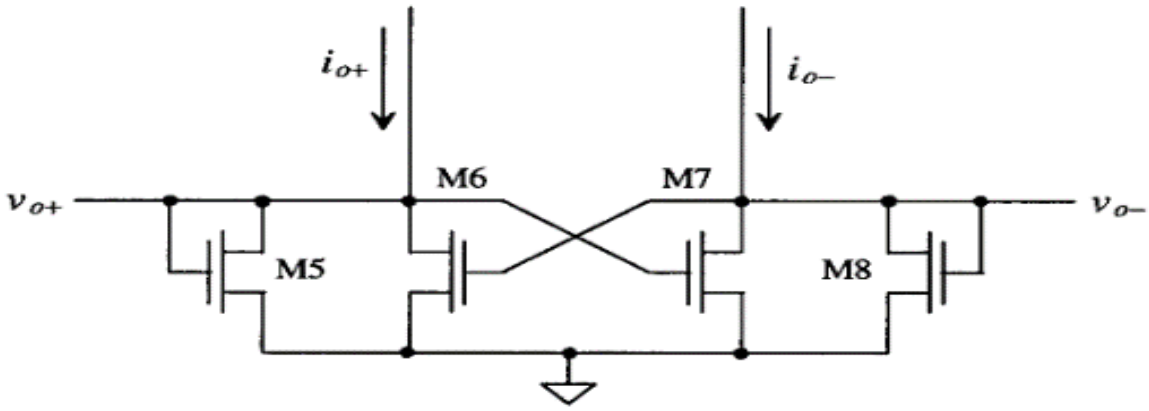


Fig. 4: *Positive Feedback Decision Circuit* [2].

If Io+ is much larger than Io− then M5 and M7 are ON and M6 and M8 are OFF. In the circuit, β5 = β8 and β6 = β7 (Here β is gain of relative transistor). Under these circumstances, Vo− is approximately 0 V and Vo+ is high.

$$V_{o+} = \sqrt{\frac{2io+}{\beta_A}} + V_{THN}$$

If Io− increases and Io+ decreases, then switching takes place when the drain-source voltage of M7 is equal to V_{THN} of M6. At this point, M6 starts to take current away from M5. This decreases the drain-source voltage of M5 and thus starts to turn M7 OFF. If we assume that the maximum value of Vo+ or Vo− is equal to 2 V_{THN}, then M6 and M7 operate, under steady-state conditions, in either cutoff or the triode regions. Under these circumstances, the voltage across M7 reaches VTHN, and thus M7 enters the saturation region, when the current through M7 is

$$io- = \frac{\beta_B}{2}(vo + -V_{THN})^2 = \frac{\beta_B}{\beta_A}\, io +$$

This is the point at which switching takes place; that means, M7 shuts off and M6 turns on. If $\beta_A = \beta_B$ then switching takes place when the currents, Io+ and Io− are equal. Unequal βS causes the comparator to exhibit hysteresis. A similar analysis for increasing Io+ and decreasing Io− yields a switching point of

$$io+ = \frac{\beta_B}{\beta_A}\, io -$$

The combined circuit of basic amplifier, pre-amplifier and decision-circuit stage is shown in Figure 5.

Output Buffer

The final component in the basic comparator design is the output buffer or post amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5 V). The output buffer should accept a differential input signal and not have slew-rate limitations.

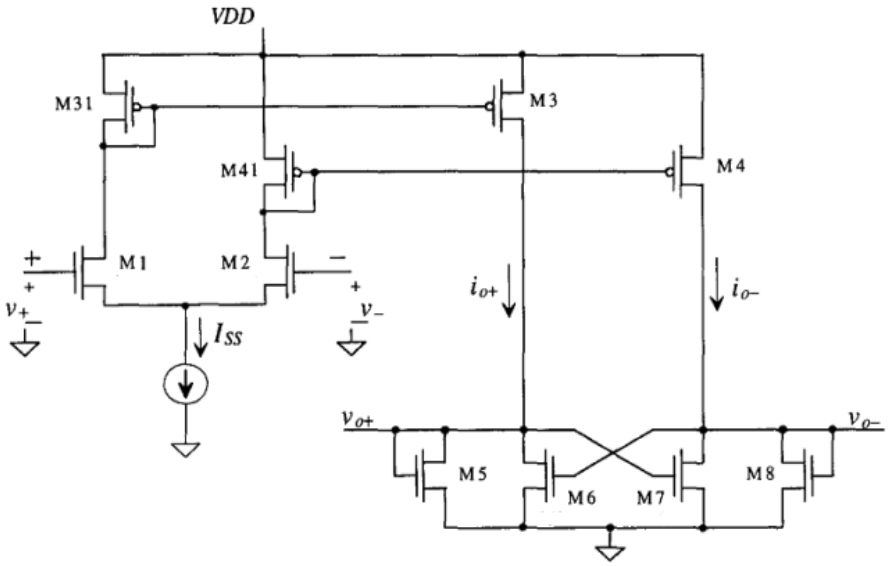


Fig. 5: *Combined Circuit of Basic Amplifier, Preamplifier and Decision-Circuit Stage* [2].

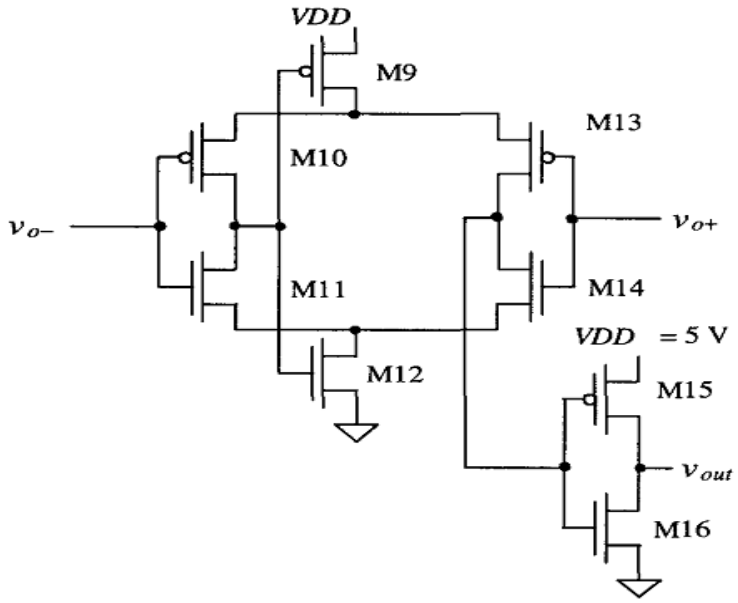


Fig. 6: *A Self-Biasing Differential Amplifier Used as the Comparator Output Buffer* [2].

The circuit used as an output buffer in the proposed basic comparator design is shown in Figure 6. This circuit is a self-biasing differential amplifier. An inverter was added on the output of the amplifier as an additional gain stage and to isolate any load capacitance from the self-biasing differential amplifier. In the basic comparator decision circuit, there is overlap between Vo− and Vo+. So output of the decision circuit cannot be connected directly to the output buffer circuit. There must be shift in output voltage of decision circuit to remove overlap [10–15]. To shift the output of the decision circuit, the circuit of Figure 7 is used. The MOSFET M17 is added in series with the decision circuit to increase the average voltage out of the decision circuit. The size of the MOSFET is somewhat arbitrary.

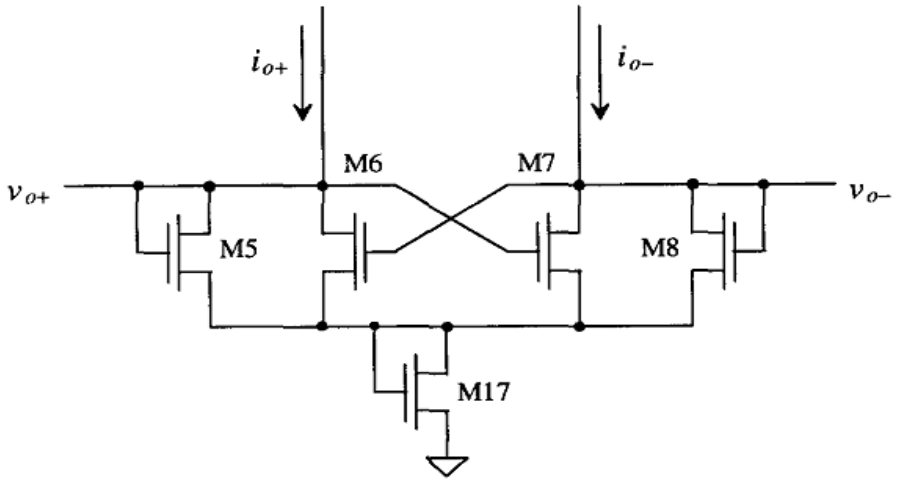


Fig. 7: Use of a Large MOSFET M17 to Level Shift the Output of the Decision Circuit [1].

BASIC CIRCUIT OF A COMPARATOR

Figure 8 shows the complete circuit of a basic comparator consisting of all the three stages discussed above.

Nowadays, it requires the use of very-low devices in the circuits and systems.

Low power A/D converters, sense amplifier and data converter, which are used for many applications, use comparators as their basic elements. Comparators are also used in data transmission circuits and switching power regulator circuits [12–15].

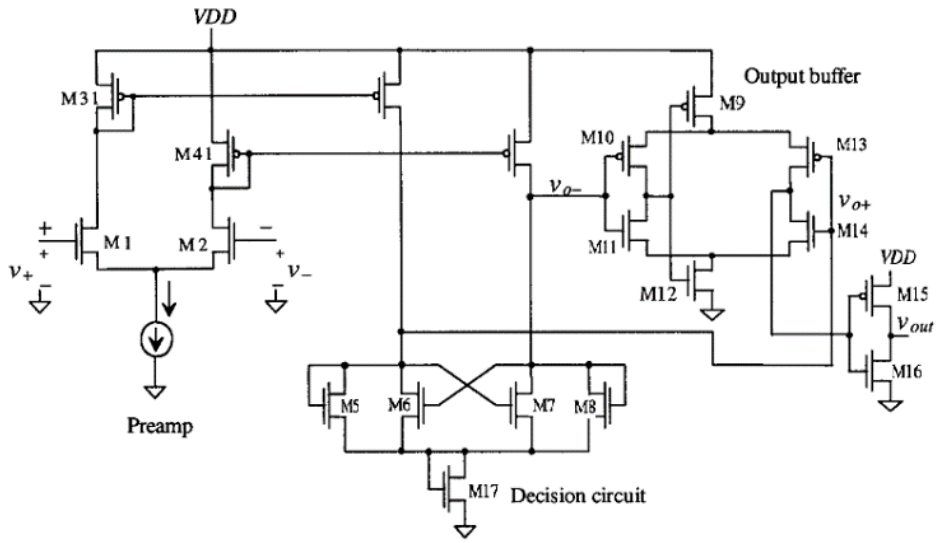


Fig. 8: Schematic Basic Comparator [2].

Characterization of a Basic Comparator in 90 nm Technology

The circuit in Figure 9 shows schematic layout of a basic comparator using 90 nm technology in Mentor Graphics tool. The channel length of all the transistors is kept 100 nm. The channel width

of all the NMOS transistors is kept 120 nm, while for PMOS transistors it is kept 2.5 times that of NMOS transistors, which is 300 nm.

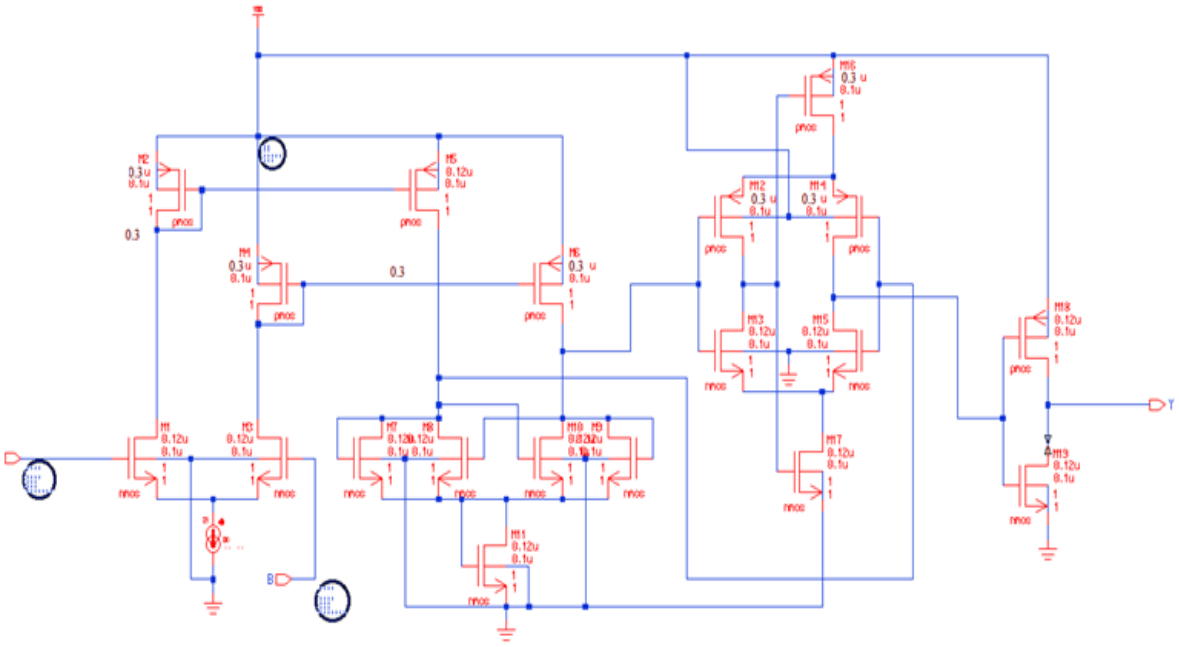


Fig. 9: *Schematic of Basic Comparator in 90 nm Technology.*

Transient Analysis

Transient responses for different input conditions and different parameters are shown in the Figure 10(a), 10(b) and 10(c).

Lengths of NMOS and PMOS transistors are set as 100 nm. Widths of NMOS transistors are set as 120 nm, while for PMOS transistors, widths are set as 300 nm. Figure 10(a) shows Transient response when inputs are digital patterns "0011" and "0101" having time period 100 ns

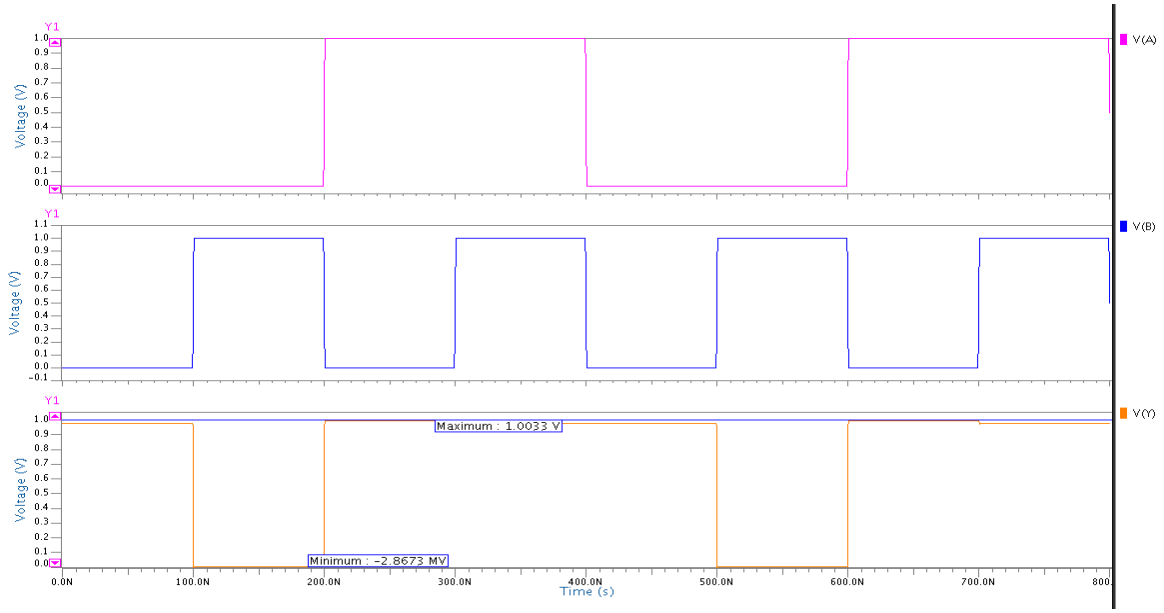


Fig. 10(a): *Transient Response when Inputs Are Digital Patterns "0011" and "0101" Having Time Period 100 ns.*

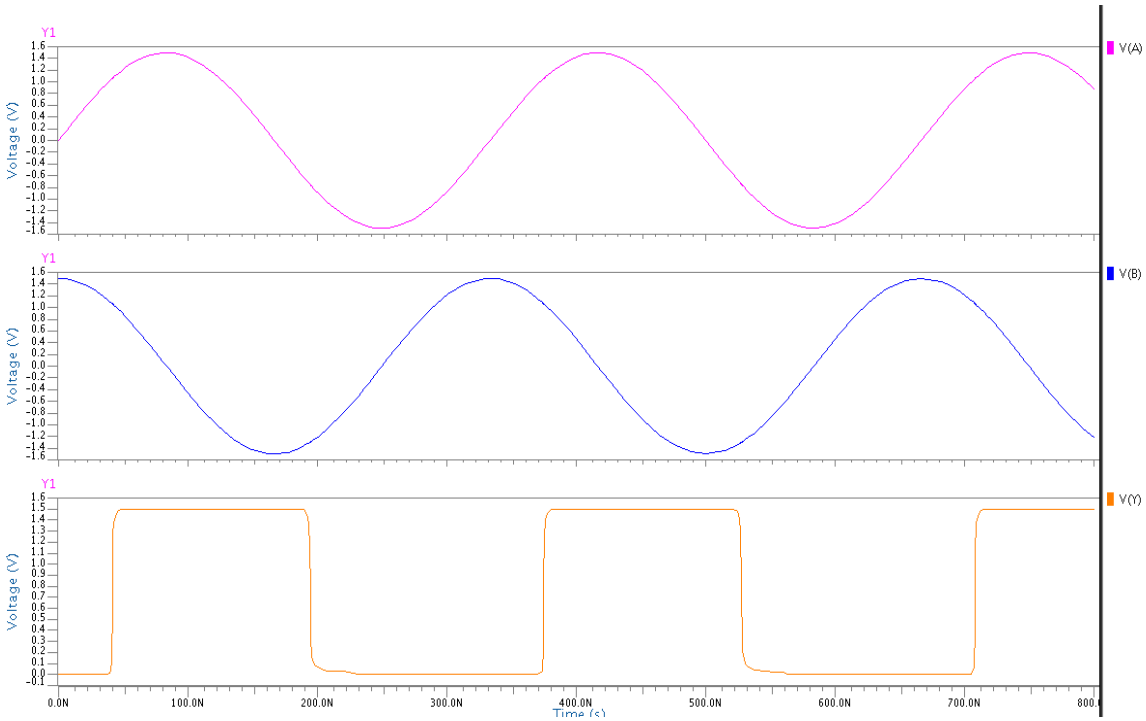


Fig. 10(b): *Transient Response when Inputs Are Sine Waves with Phase Difference 90°.*

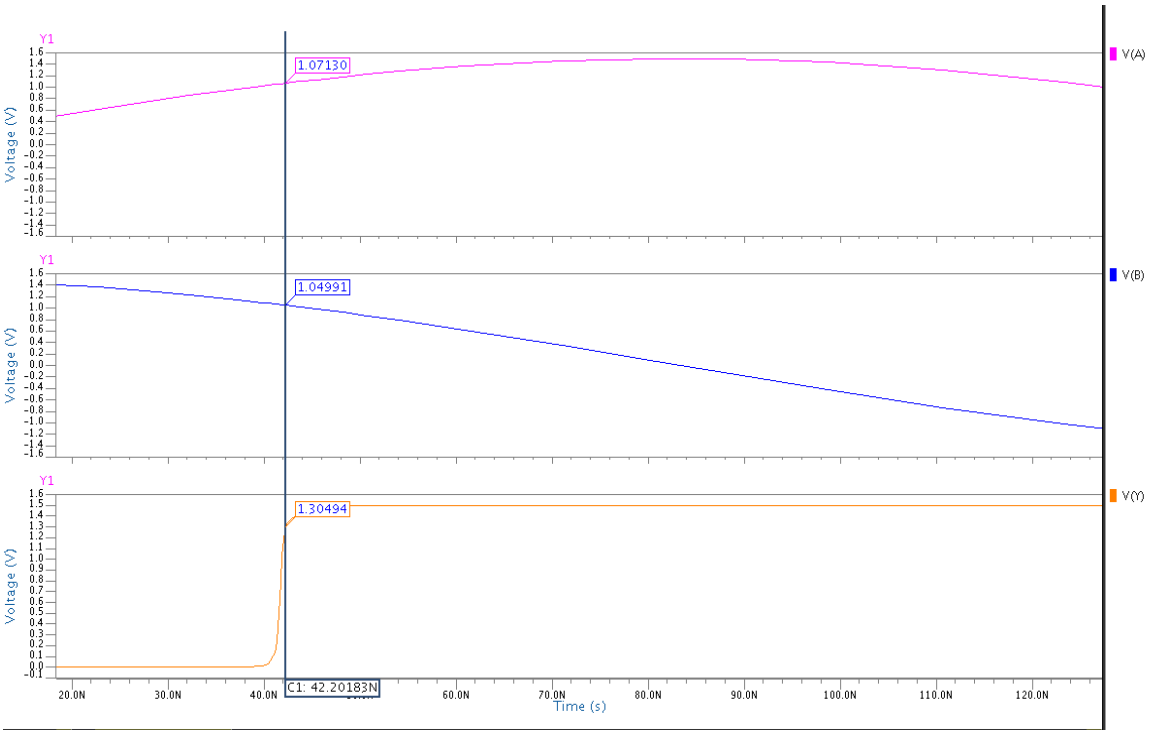


Fig. 10(c): *Zoomed View of the Rising Edge.*

Figure 11 is used to measure the parameters of the output of comparator. Figures 12(a), 12(b) and 12(c) are used to measure the offset voltage with different values of Iss(60, 40, 20 µA,) respectively.

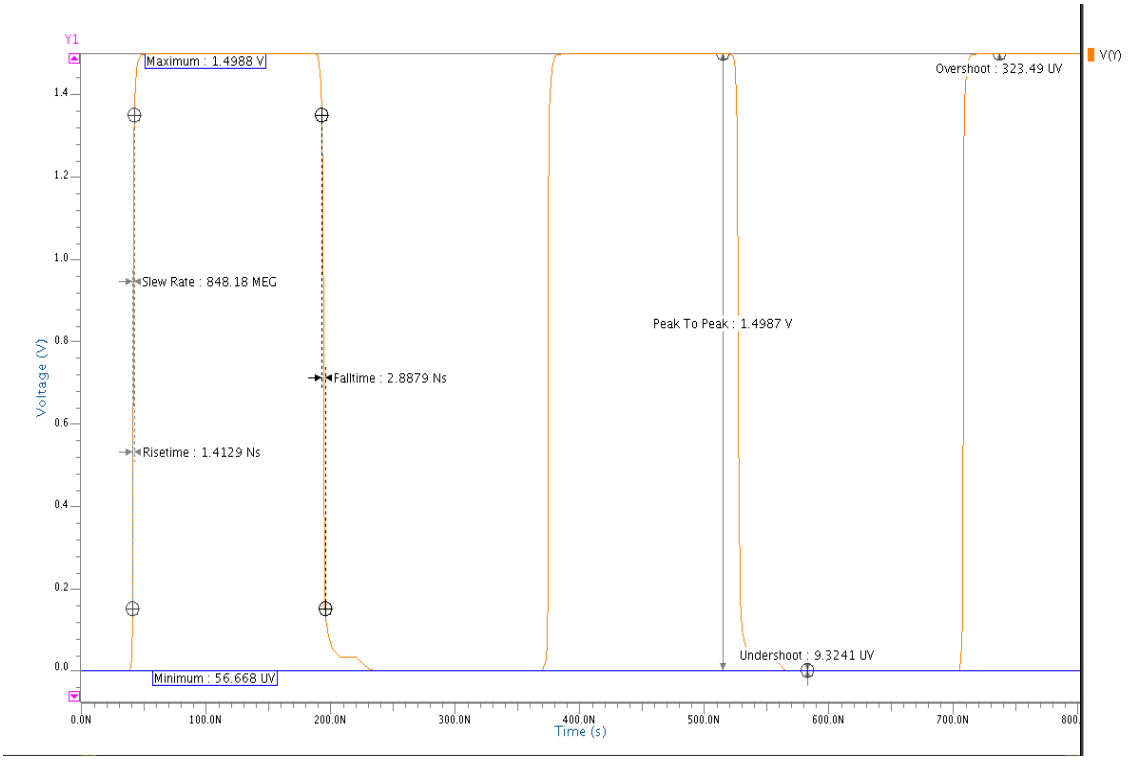


Fig. 11: *Measurement of Parameters of the Output of a Comparator.*

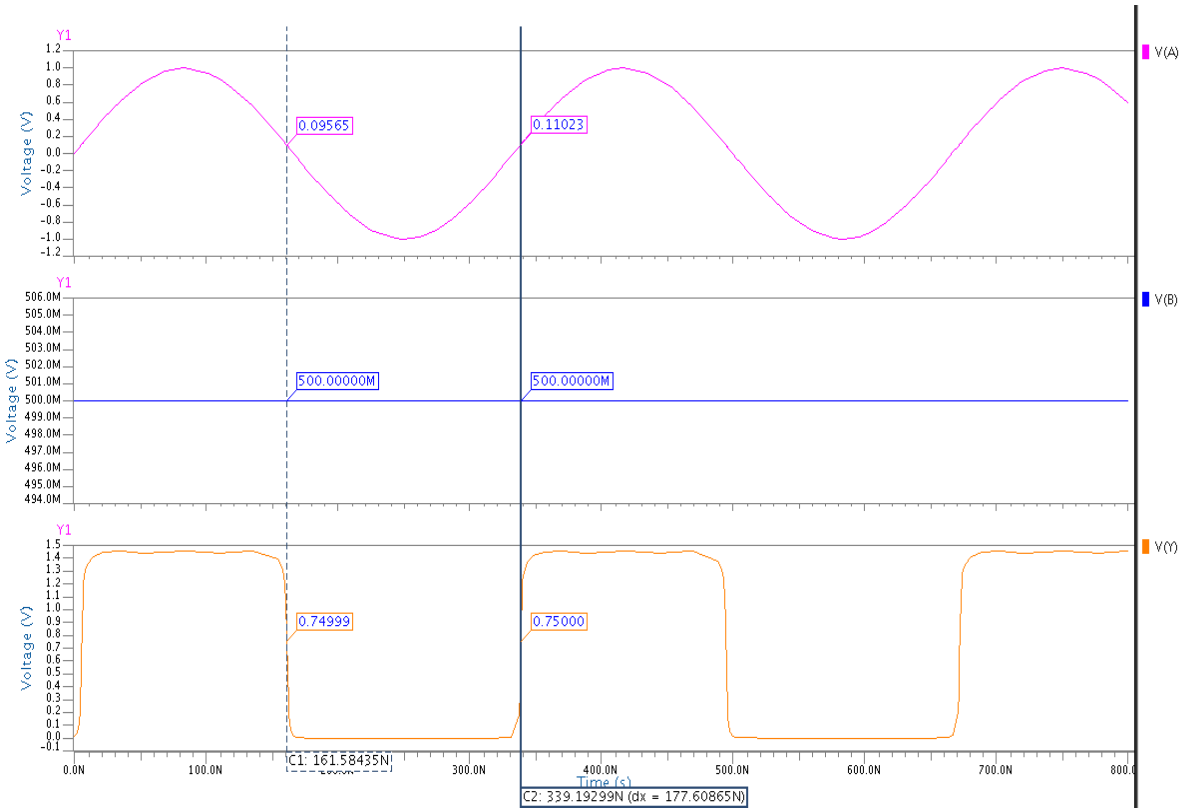


Fig. 12(a): *Offset Voltage Measurement for Iss = 60 µA.*

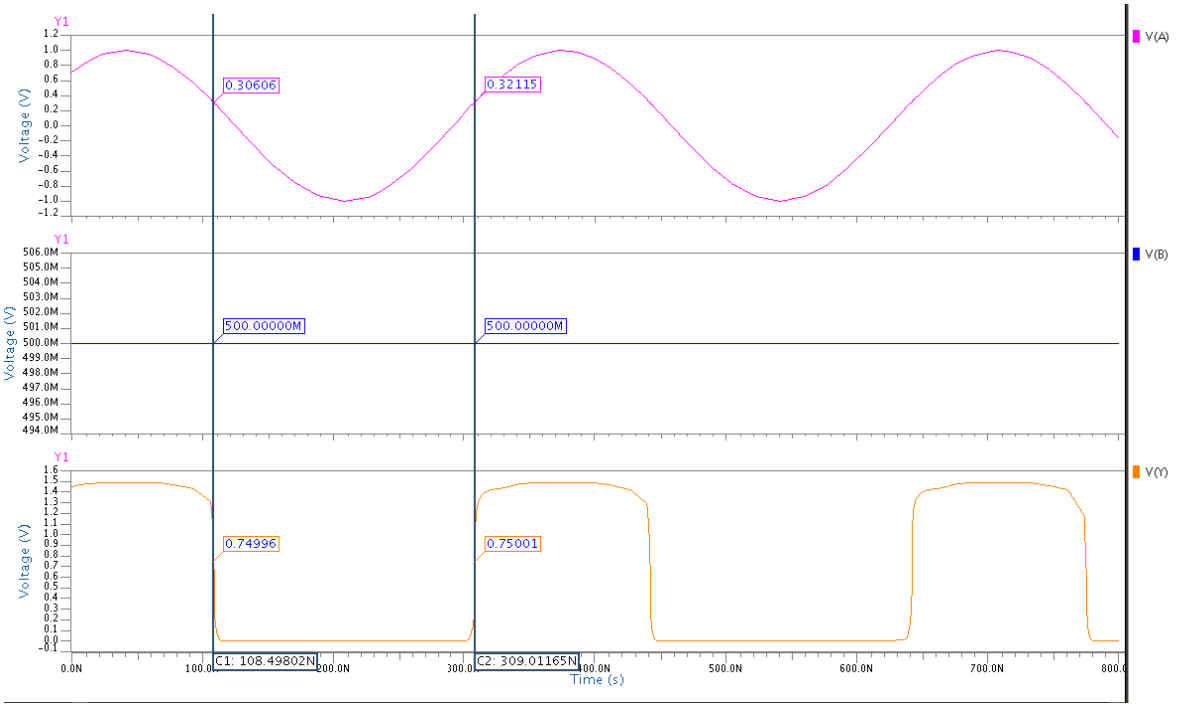


Fig. 12(b): *Offset Voltage Measurement for Iss = 40 µA.*

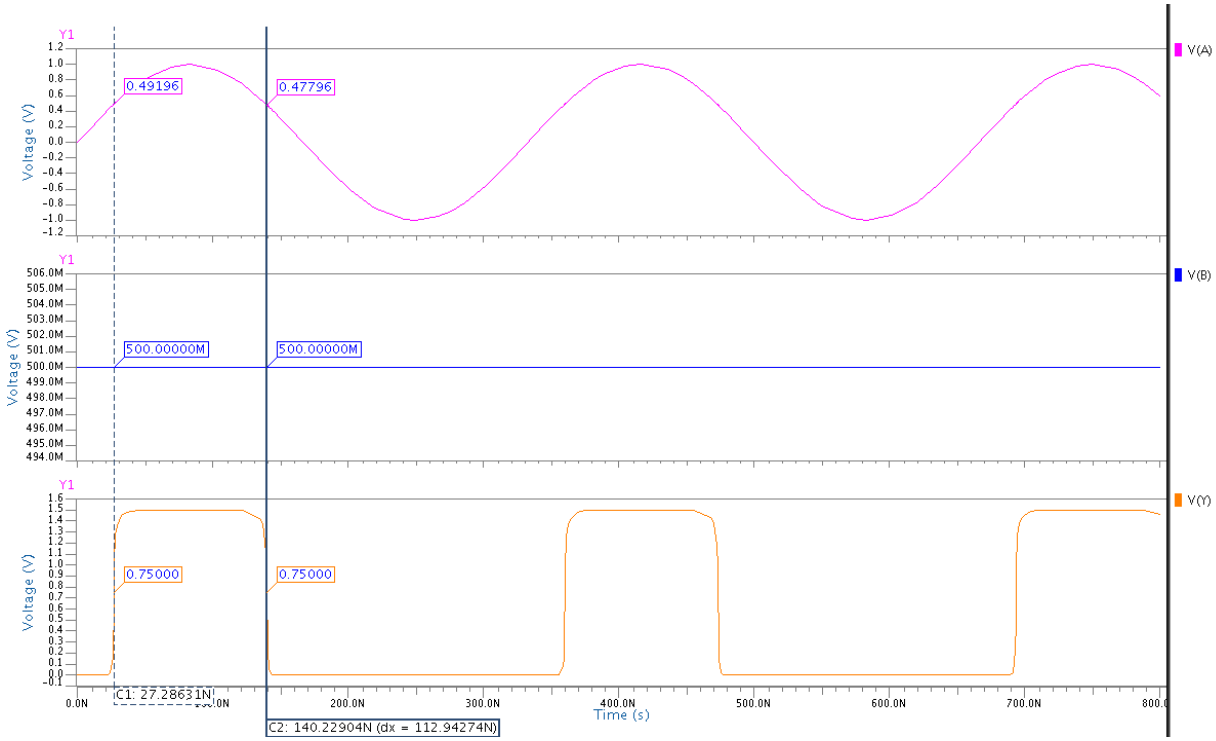


Fig. 12(c): *Offset Voltage Measurement for Iss = 20 µA.*

DC Analysis and Temperature Sweep

Figures 13(a, b) and 14 show the DC analysis and temperature sweep analysis respectively.

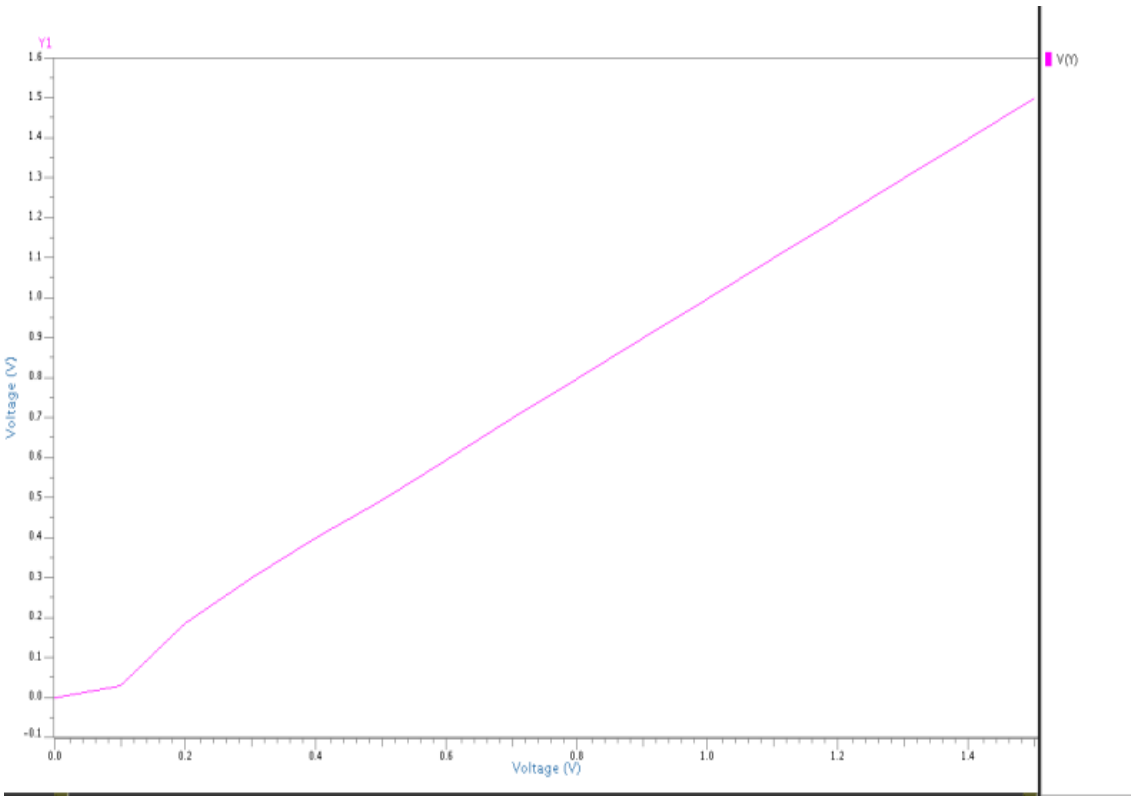


Fig. 13(a): *DC Analysis Source Voltage (Vdd sweep from 0 to 1.5 V).*

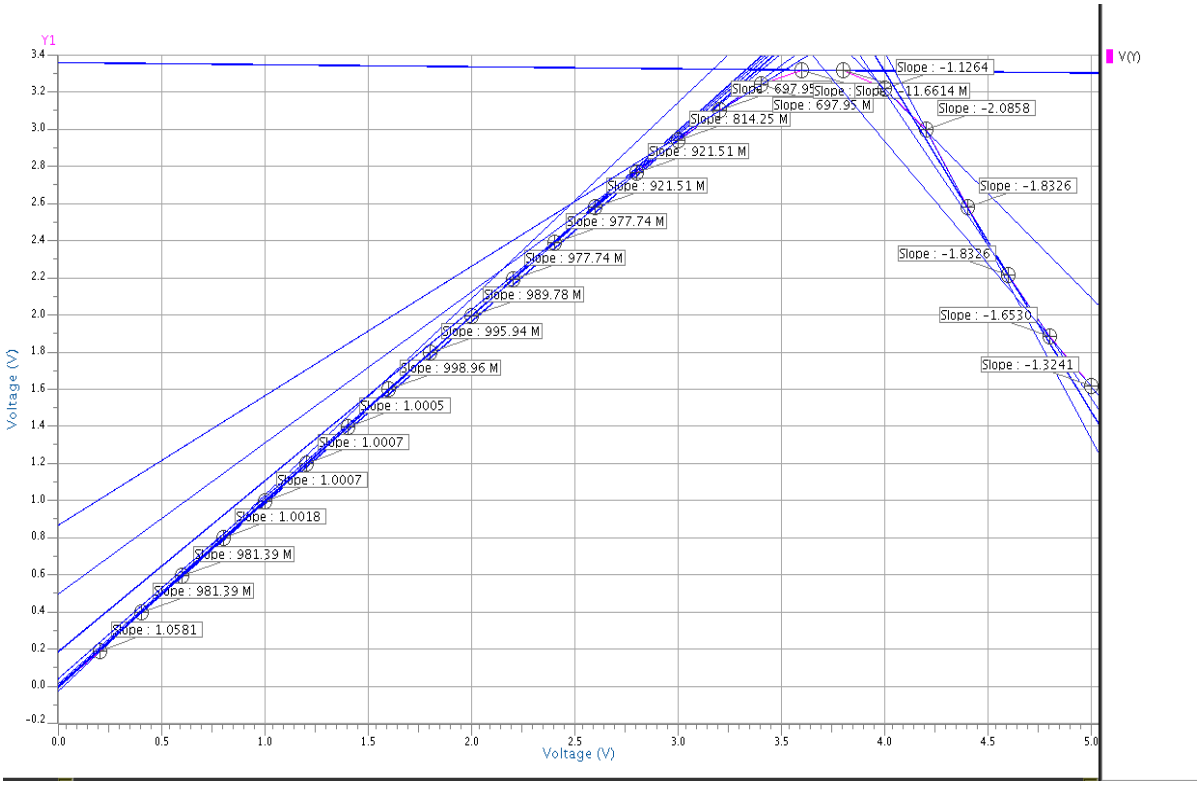


Fig. 13(b): *DC Analysis (Vdd Sweep from 0 to 5 V).*

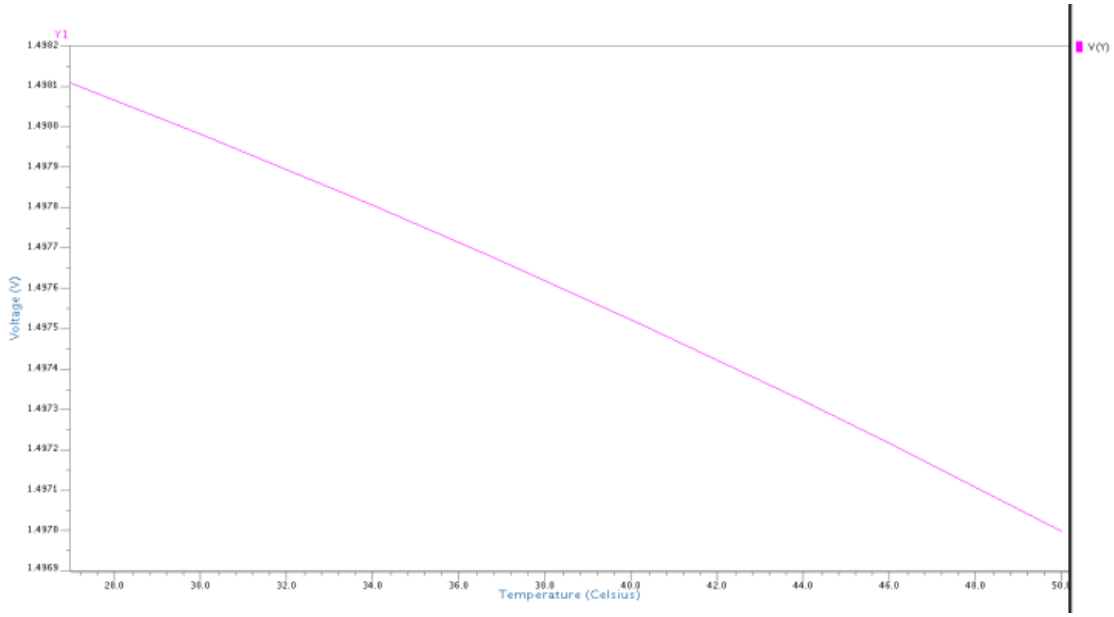


Fig. 14: *Temperature Sweep Analysis.*

Table 1 shows the calculated values of offset voltages for both the rising and falling edge of the output voltage for different current values of current source (ISS).

Table 1: *Offset Voltage Measurement for Different ISS.*

Current source value	Offset voltage (rising edge)	Offset voltage (falling edge)
60 µA	−49.904 mV	−38.977 mV
40 µA	−17.885 mV	−19.394 mV
20 µA	−0.804 mV	−2.205 mV
10 µA	1.133 mV	−0.444 mV
0.5 µA	4.227 mV	−0.379 mV

Table 2 shows power dissipation, rise-time and fall-time analysis for different values of current ISS.

Table 2: *Different Parameter Calculations for Different Values of ISS.*

Current source value	Power dissipation	Rise time	Fall time
60 µA	145.22 µW	4.6790 ns	0.9996 ns
40 µA	100.17 µW	3.7595 ns	1.0289 ns
20 µA	61.23 µW	1.9437 ns	2.2892 ns
10 µA	47.68 µW	1.5276 ns	2.1906 ns
0.5 µA	35.4693 µW	1.6180 ns	2.5255 ns

Table 3 shows the results of the basic comparator which has been implemented in the 90 nm technology and again it has been compared with the other topologies in Results section.

Table 3: *Implementation Results of Basic Comparator in 90 nm Technology.*

Property	Basic comparator[2] (90 nn)
Rise time	1.5276 ns
Fall time	2.1906 ns
Power dissipation	47.68 µW
Supply voltage	1.5 V
Voltage swing	56.668µV to 1.4987 V

CONCLUSIONS

This paper explains about the comparator and its design in sub-micron and deep sub-micron technologies. The result shows that as the current ISS decreases, power dissipation decreases, rise-time decreases in most of the cases and fall time increases in most of the cases. It can be observed that ISS = 10 µA is the optimum value among all the values of ISS observed.

REFERENCES

1. Phillip E. Allen, Douglas R. Holberg. *CMOS Analog Circuit Design* . OXFORD University Press.
2. R. Jacob Baker, Harry Li, David Boyce. *CMOS Circuit Design, Layout & Simulation.* IEEE press series on microelectronic systems, 2005.
3. Shuzhengxu Vahouikong, Y huazong. An ultra low output resistance and wide swing voltage follower. *ICCCAS* July 2007; 1007-1010p.
4. H Gao, P Baltus, Q Meng. Low Voltage Comparator for High Speed ADC, Systems and Electronics. *ISSSE* 2010; 1.
5. S Lan, C Yuan, YYH Lam, et al. An ultra low-power rail-to-rail comparator for ADC designs. *IEEE* 2011; 2.
6. Y Jung, S Lee, J Chae, et al. Low-power and low-offset comparator using latch load. 2011; 47(3):3–4p.
7. Ili Shairah Abdul Halim, Nurul Aisyah Nadiah Binti Zainal Abidin, A'zraa Afhzan Ab Rahim. Low power CMOS charge sharing dynamic latch comparator using 0.18µm technology. Kota Kinabalu, Malaysia, *IEEE-RSM* 2011; (4).
8. A Vishwakarma, S Sahu, V Vishwakarma, et al. Different parameter analysis of CMOS charge sharing latch comparator using 90nm technology. *IJCA* 2013; 63(11):5–10p.
9. R Wang, Li Kaihang, J Zhang, et al. A high speed high resolution latch comparator for pipeline ADC. *IEEE* 2007; 28-31p.
10. S Sheikaei, S Mirabbasi, A Ivanov. A 0.35µm CMOS comparator circuit for high-speed ADC applications. *IEEE* 2007; 6134-6137p.
11. Khosrov Dabbagh Sadeghipour. Resolution enhanced latch comparator. *IEEE* 2001; 29-35p.
12. Meghana Kulkarni, V Sridhar, GH Kulkarni. The quantized differential comparator in flash analog to digital C design. *IJCNC.* July 2010; 2(4).
13. Hao Gao, Peter Baltus, Qiao Meng. Low voltage comparator for High Speed ADC. *ISSSE* 2010.
14. P Uthaichana, E Leelarasmee. Low power CMOS dynamic latch comparators. *IEEE* 2003; 605-608p.
15. Z Huang, P Zhong. An adaptive analog-to-digital converter based on low-power dynamic latch comparator. *IEEE Conference* 2005; 6p.