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Analysis, design and digital implementation of a shunt active power filter with different schemes of reference current generation

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Abstract: To reduce the harmonics injected by non-linear loads, power quality improvement devices like shunt active power filters (SAPFs) are commonly employed. This study presents a digital signal processor (DSP) TMS320LF2407A based hardware implementation of current error space phasor-based hysteresis controller for SAPF. The proposed controller-based SAPF allows precise compensation of harmonic currents. Design considerations for practical implementation of the proposed space phasor-based current error hysteresis controller for SAPF are explained here. Performance analysis of space phasor-based current error hysteresis controller for SAPF is explained in the study. The controller's self-adaptive nature is studied for different logics of necessary sector changes. Here, the versatile nature of the controller is proved by analysing its performance for different reference compensating current generation methods. The proposed controller works on the principle of switching voltage vectors adjacent to the desired output voltage vector of SAPF (voltage vector at the point of common coupling). This strategy helps in restricting the current error within the desired hexagonal boundary. A comparative study of DSP-based implementation for two different schemes of reference compensating currents generation is presented in this study. Instantaneous reactive power theory and Fryze current computation methods are chosen for this comparative study. Experimental results of reference compensating currents generated by different strategies using DSP are presented in this study.

1 Introduction

Advancement in the field of power electronics has caused widespread use of power electronic devices and non-linear loads thereby deteriorating power quality. As a result, harmonic mitigation and reactive power compensation have become the need of the day and are attracting more research interest. Traditionally, passive filters have been used for compensation of harmonics and reactive power but they suffer from disadvantages such as bulky size, series and parallel resonance, fixed filtering characteristics and filtering characteristics strongly affected by source impedance [1]. To overcome these problems, power electronic-based power quality improvement devices like shunt active power filters (SAPFs) have been developed.

Shunt active filters were initially proposed in 1971 by Sasaki and Machida [2] as a means of removing current harmonics. When the active power filter (APF) is connected in parallel with the harmonic load, it is called shunt APF [3]. The shunt APF is suitable for non-linear loads which introduce current harmonics, while for non-linear loads that produce voltage harmonics, a series APF is used [4].

Many approaches such as notch filter [5], instantaneous reactive power (IRP) theory [6], synchronous detection method [7], synchronous d–q frame method [8], flux based control [9], closed-loop PI controllers [8, 9], sliding mode control [10, 11], ABC theory [12], self-tuning filters [13] and non-linear least squares approach [14] are used to improve the performance of the APFs. The conventional hysteresis current controller (HCC) scheme used in the APFs uses three independent hysteresis controllers one for each phase and hence suffers from lack of coordination between the three individual HCCs, resulting in higher number of switching. Fuzzy logic controllers are used to implement hysteresis controller logic [15, 16]. To decrease the number of switching and in turn the switching frequency, space vector modulation technique is applied to current hysteresis controller which enables the use of zero switching vector along with non-zero vectors [17–20].

This paper emphasises analysis, design and digital implementation of the proposed current error space phasor hysteresis controller-based SAPF for two different schemes of reference compensating current generation – IRP theory and Fryze current computation technique, in order to compensate for the load harmonics. Both the strategies of reference compensating current generation are rigorously simulated for different logics of sector change detection. The proposed controller being self-adaptive in nature (with the help of the outer hysteresis band) does not require any

calculation of point of common coupling (PCC) voltage vector (***E***) for detection of sector change. However, the shape of the supply current is further improved by removing the outer hysteresis band and detecting necessary sector changes for generating the APF compensating currents by synchronising the sector change logic with supply frequency. The proposed current controller allows switching of only adjacent voltage vectors in a given sector of voltage space phasor of APF thereby avoiding the selection of random (non-adjacent) voltage vectors. Selection of non-adjacent voltage vectors is, generally, the attribute of conventional HCC-based APFs. Systematic design approach for arriving at proper values of SAPF inductor (L), dc-link capacitance (C_{dc}) and dc-link capacitor voltage (V_{dc}) is also presented in the proposed studies.

A current error space phasor-based hysteresis controller is implemented by using DSP TMS320LF2407A. This paper mainly focuses on the implementation considerations of both the strategies for reference compensating current generation using the DSP. It is systematically evaluated that the Fryze current computation technique is easier to implement and a better resolution can be obtained in the calculations to achieve the reference compensating currents than obtaining the same with IRP theory with the same DSP.

2 Shunt APF

The SAPF feeds compensating current which includes the harmonics present in non-linear load current, at the PCC. These compensating currents should be similar to the reference compensating current obtained by different reference compensating current generation schemes. This is ensured by appropriate switching of APF using a current controller. The current compensation characteristic of the SAPF is shown in Fig. 1*a*.

3 Reference compensating current calculation

Harmonic currents are extracted from a non-linear load current by various reference compensating current calculation methods. The compensating characteristic of an SAPF is dependent on the method adopted for reference compensating current calculation.

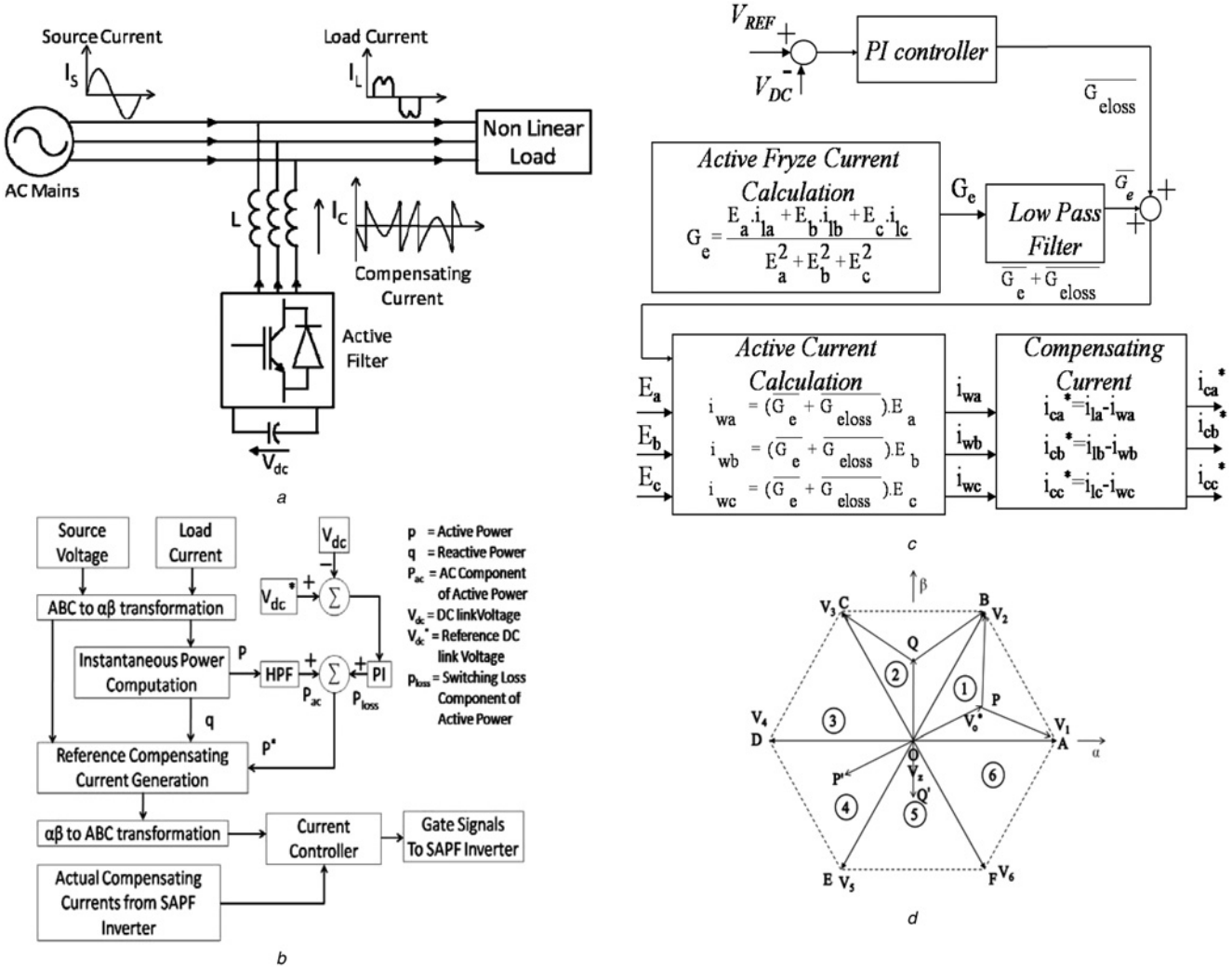

Fig. 1 *Proposed controller based SAPF*

a SAPF
b Control scheme for IRP theory
c Control scheme for Fryze current computation technique
d Voltage space phasor structure and direction of current error space phasor for APF

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3.1 IRP theory [6, 21]

Fig. 1*b* shows the control schematic for implementation of the IRP theory. Based on the IRP theory, the compensated currents are derived by measuring line voltage E_a, E_b, E_c, load current i_{la}, i_{lb}, i_{lc} and then, transforming them into two orthogonal reference vectors $\boldsymbol{E}_\alpha$, $\boldsymbol{E}_\beta$ and $i_{l\alpha}$, $i_{l\beta}$ by Clarke's transformation

$$p = p_{dc} + p_{ac} = E_\alpha i_{l\alpha} + E_\beta i_{l\beta} \tag{1}$$

$$q = q_{dc} + q_{ac} = E_\alpha i_{l\beta} - E_\beta i_{l\alpha} \tag{2}$$

where p_{dc}, q_{dc} are the dc components of active and reactive power, respectively, p_{ac}, q_{ac} are the ac components of active and reactive power, respectively.

The compensated currents are calculated as follows

$$i_{c\alpha}{}^* = \frac{E_\alpha\left(p_{ac} + p_{loss}\right) - E_\beta q}{E_\alpha{}^2 + E_\beta{}^2} \tag{3}$$

$$i_{c\beta}{}^* = \frac{E_\alpha q + E_\beta\left(p_{ac} + p_{loss}\right)}{E_\alpha{}^2 + E_\beta{}^2} \tag{4}$$

where $i_{c\alpha}{}^*$, $i_{c\beta}{}^*$ are the reference compensating currents along the α- and β-axes.

Therefore compensating currents in three phase form are

$$i_{ca}{}^* = \sqrt{\frac{2}{3}} i_{c\alpha}{}^* \tag{5}$$

$$i_{cb}{}^* = \sqrt{\frac{1}{6}} i_{c\alpha}{}^* + \sqrt{\frac{1}{2}} i_{c\beta}{}^* \tag{6}$$

$$i_{cc}{}^* = -\sqrt{\frac{1}{6}} i_{c\alpha}{}^* - \sqrt{\frac{1}{2}} i_{c\beta}{}^* \tag{7}$$

where $i_{ca}{}^*$, $i_{cb}{}^*$, $i_{cc}{}^*$ are the reference compensating currents of a, b and c phase, respectively.

3.2 Fryze current computation technique

If linearity between voltage and current is desired while performing power compensation, an extension of the minimisation techniques guarantees linearity, even under distorted and/or unbalanced source voltages. This alternative method of compensation is known as the generalised Fryze currents minimisation method [22]. The approach for implementation of the Fryze current computation technique is explained in Fig 1*c*.

The desired reference compensating currents calculated from the active current, after compensation, can be written as

$$i_{ca}{}^* = i_{la} - i_{wa}, \quad i_{cb}{}^* = i_{lb} - i_{wb}, \quad i_{cc}{}^* = i_{lc} - i_{wc} \tag{8}$$

where i_{wa}, i_{wb} and i_{wc} are the generalised Fryze currents.

4 Principle of current error space phasor-based hysteresis controller

The space phasor of the APF current (i_c) and voltage (V_k) as well as the voltage at the PCC ($\boldsymbol{E}$) are, respectively, given by the following equations

$$i_c = \frac{2}{3} \times \left(i_{ca} + a i_{cb} + a^2 i_{cc}\right) \tag{9}$$

$$V_k = \frac{2}{3} \times \left(V_a + a V_b + a^2 V_c\right) \tag{10}$$

$$E = \frac{2}{3} \times \left(E_a + a E_b + a^2 E_c\right) \tag{11}$$

where

$$a = e^{j((2\pi)/3)}$$

For Fig. 1*a*, the relationship between the voltage vector of the APF and the voltage vector at the PCC can be given as in (12). These two voltage vectors are separated by an inductor L. Basically, it is analogous to the inverter and motor voltage and current equation used in [23, 24]

$$V_k = L\frac{di_c}{dt} + E \tag{12}$$

Now, rate of change of compensating current is

$$\frac{di_c}{dt} = \frac{1}{L}\left(V_k - E\right) \tag{13}$$

where L = APF inductor.

Now, the current error space phasor is

$$\Delta i = i_c - i_c^* \tag{14}$$

where i_c^* is the reference current space phasor.

Thus, the rate of change of the current error is

$$L\frac{d\Delta i}{dt} = \left(V_k - E\right) - L\frac{di_c^*}{dt} \tag{15}$$

To eliminate the current error Δi, the desired output voltage vector $\boldsymbol{V}_o{}^*$ is obtained from (15) as

$$V_o{}^* = E + L\frac{di_c^*}{dt} \tag{16}$$

The direction at which the current error space phasor moves is given by

$$\frac{d\Delta i}{dt} = \frac{V_k - V_o{}^*}{L} \tag{17}$$

Different strategies have been proposed to choose the desired SAPF voltage vector to keep the current error space phasor within the boundary [23–31]. The derivative $d\Delta i/dt$ plays a vital role in diminishing the number of switchings. Choosing a voltage vector V_k, which results in a minimum value of $d\Delta i/dt$ is a necessity to accomplish this task. For the conventional HCC technique, coordination of the switching does not exist. However, space phasor-based technique causes reduced switching. On the other hand, the utilisation of non-zero vectors instead of zero vectors gives a steep slope for the current error because of large voltage difference $V_K - V_o{}^*$. This causes limit cycle oscillations in the conventional HCC-based APF. Thus, a set of voltage space vectors, two active voltage vectors and the zero

voltage vector, is to be applied depending on the position of the desired space voltage vector V_o^*.

5 Proposed current error space phasor-based hysteresis controller

In the proposed hysteresis controller, the current error space phasor is kept within a boundary, by applying one of the three voltage vectors of the APF which are adjacent to the voltage vector V_o^* (in the same sector of voltage space phasor structure of APF) so that deviation of the current error space phasor is minimum. Fig. 1*d* shows the APF voltage vectors and direction of current error space phasor movement for positions of desired output space voltage vector V_o^* in two different sectors (i.e. Sector 1 and Sector 2). When V_o^* is in Sector 1 (OP); PA, PB and OP' are the directions along which minimum deviation of the current error takes place when V_1, V_2 and V_z are switched, respectively. Similar is the case for other sectors.

The sets of directions along which the current error space phasor moves for switching of vectors V_1, V_2 and V_Z in sector 1 is shown in Fig. 2*a* [24]. Movement of the current error space phasor is restricted by placing boundaries along these sets of directions. For example, if the current error space phasor moves in a direction parallel to any direction bounded by the directions of OA and OF, it can touch a boundary *XZ* as shown in Fig. 2*a*. This boundary can be decided to be anywhere at a distance '*h*' along the j_C-axis. Similarly, the directions OC and OB define another boundary *YX* along the j_A-axis and the directions OD and OE define the third boundary along the j_B-axis. The same triangular boundary exists for all the odd sectors [24]. In the same manner, the triangular boundary shown in Fig. 2*b* exists for all the even sectors.

5.1 APF voltage selection for given sector

This hysteresis controller uses only voltage vectors which are adjacent to V_o^*. As mentioned earlier, within a sector, when a particular voltage vector of the APF is switched, it makes the current error space phasor move towards one of the sides of the boundaries (Figs. 2*a* and *b*). The APF voltage vector is continued till the current error space phasor reaches another side of the boundary. Once the current error space phasor hits another side of the boundary, the APF voltage vector is changed so that the current error space phasor is brought back within the boundary, and moves towards the opposite side of the triangular boundary. The proposed controller divides the triangular boundary into three regions and each of these regions is associated with a suitable voltage vector of the APF (depending on the sector) which will take the current error space phasor towards the opposite side of the triangular boundary. The triangular boundary of the odd sectors is split into three regions R_1, R_2 and R_3, while that of the even sectors is divided into $\overline{R_1}$, $\overline{R_2}$ and $\overline{R_3}$ as shown in Figs. 2*c* and *d*. When the current error space phasor hits anywhere in a particular region, a voltage vector is selected so that the error space phasor moves towards the opposite side.

For the odd sectors, the boundaries are placed along the j_A-, j_B-, and j_C-axes (which are 120° apart and orthogonal to the *A*-, *B*- and *C*-axes, respectively) and for even sectors the boundaries are placed along the $-j_A$-, $-j_B$- and $-j_C$-axes and this would result in the combined starfish boundary as shown in Fig. 3*a*. For this starfish shaped (overall) boundary, the current error space phasor moves to double

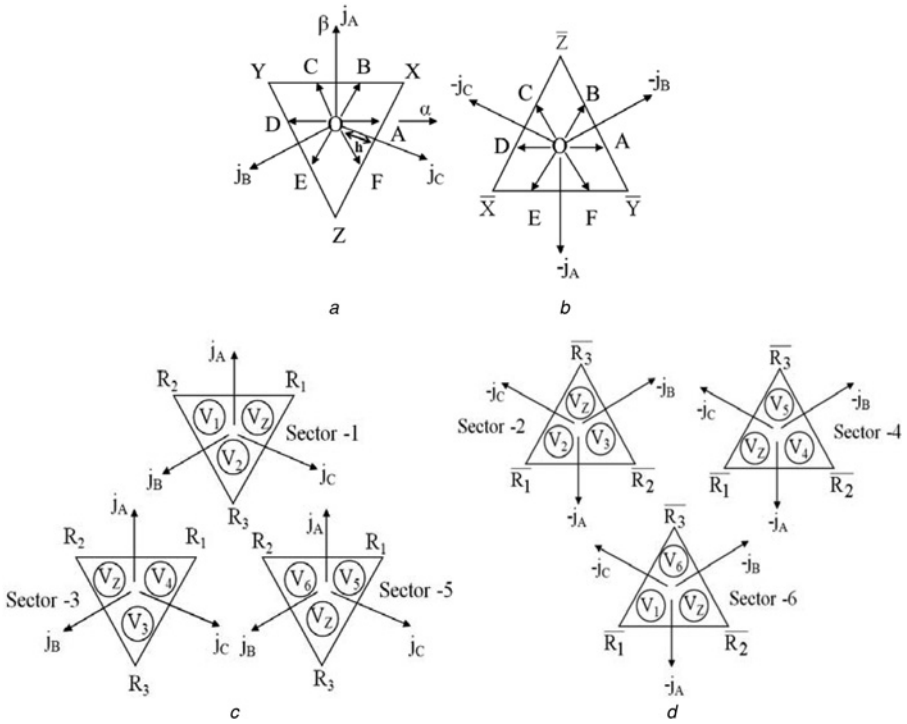

Fig. 2 *Boundary of Δi*

a For any odd sector
b For any even sector
c Regions and corresponding voltage vectors for odd sectors
d Regions and corresponding voltage vectors for even sectors

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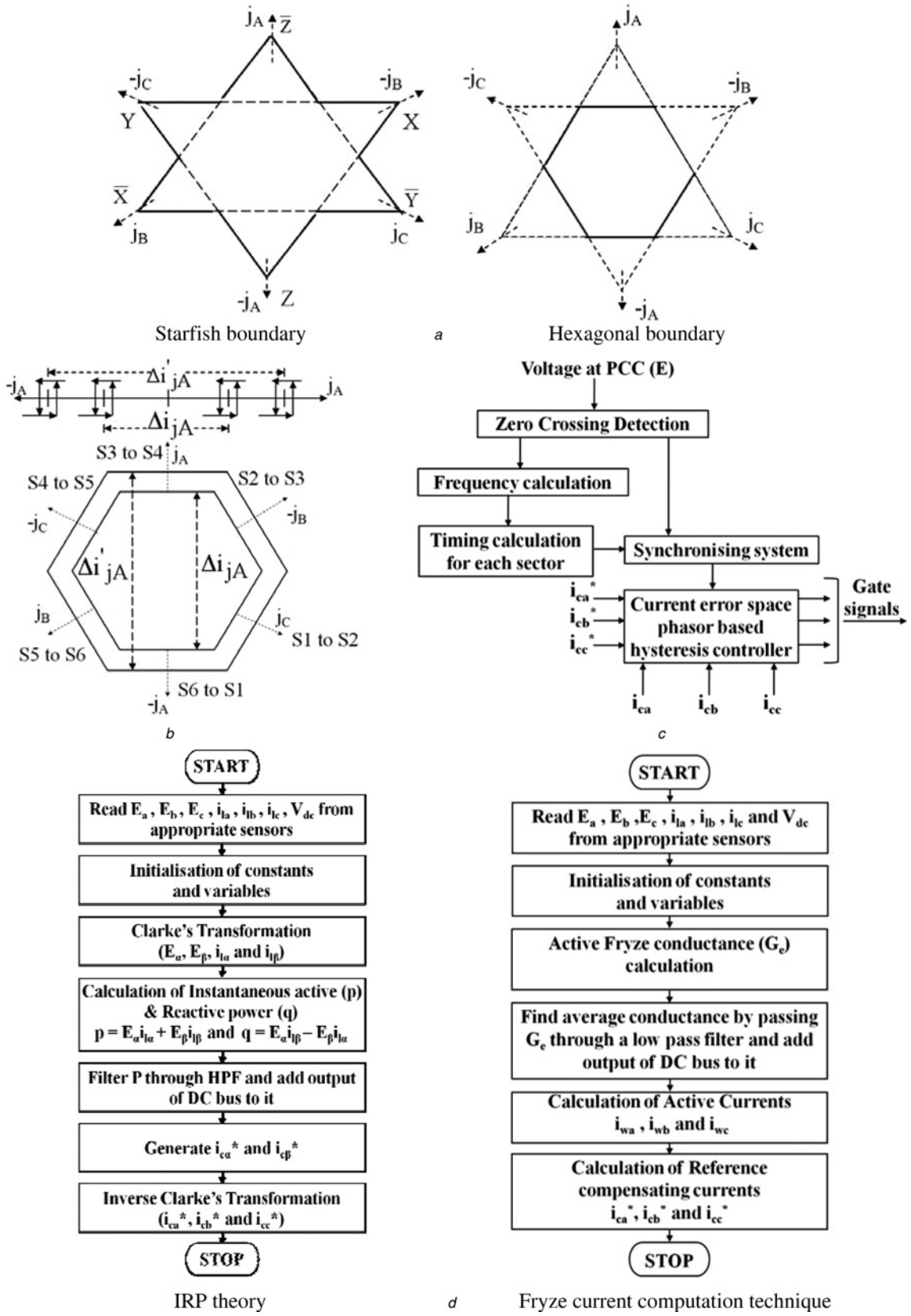

Fig. 3 *Boundaries and algorithms used for the proposed controller based SAPF*

a Boundary of Δi
b Outer hysteresis band and the sector changeovers
c Block diagram of sector change detection logic without using the outer hysteresis band by zero crossing detection of PCC voltage
d Flowchart of the IRP theory and Fryze current computation technique

the distance, along the $-j_A$-, $-j_B$- and $-j_C$-axes in the case of odd sectors and along the j_A-, j_B- and j_C-axes for the even sectors. If the boundaries are placed along all these axes, for both odd as well as even sectors, it would result in a hexagonal boundary as shown in Fig. 3*a*. In the proposed work, the hysteresis controller is implemented with this

Table 1 Selection of unique voltage vector for different regions of various sectors

Sector	Regions					
	R_1	R_2	R_3	$\bar{R}_1$	$\bar{R}_2$	$\bar{R}_3$
1	V_Z	V_1	V_2	—	—	—
2	—	—	—	V_2	V_3	V_Z
3	V_4	V_Z	V_3	—	—	—
4	—	—	—	V_Z	V_4	V_5
5	V_5	V_6	V_Z	—	—	—
6	—	—	—	V_1	V_Z	V_6

hexagonal boundary, where along all the six directions ($-j_A$, $-j_B$, $-j_C$, j_A, j_B and j_C), the current error is held always within the hexagonal boundary limits.

This hexagonal boundary is divided into different regions consistent with the regions of the triangular boundaries defined in Figs. 2*c* and *d*. Each region of the hexagonal boundary is associated with a unique voltage vector for each sector which will force the current error space phasor to the opposite direction. The different regions and respective APF voltage vectors to be switched are shown in Table 1.

5.2 Sector selection logic

Here, two logics are used for sector change detection.

5.2.1 Using the outer hysteresis band: The proposed hysteresis controller uses a self-adaptive logic to identify the instants at which the V_o^* crosses from one sector to another. This sector change is identified with the help of another set of comparators placed a little further than the comparators used for vector selection (hexagonal boundary at distance '*h*'). Fig. 3*b* shows the outer hysteresis band ($\Delta i'_{jA}$) placed along all the axes and the unique direction along which a particular sector change will be detected [24]. For example, it is found that the sector change from Sector 1 to Sector 2 can be detected by the outer hysteresis band placed along the j_C-axis. However, this scheme suffers from the drawback that in every fundamental cycle of the line current the current error goes out of the inner hexagonal boundary six times (during every sector change). This puts a limitation on harmonic elimination in the supply current.

5.2.2 Without using the outer hysteresis band: In this method, the voltage at the PCC is taken as reference and depending on the movement of this voltage space phasor sector change is detected. Fig. 3*c* shows the block diagram of the sector change logic without using the outer hysteresis band by zero crossing detection of PCC voltage. The controller logic calculates the time interval required for each sector. Once positive zero-crossing of the voltage at the PCC is detected, by using the time interval required for each sector, the sector in which V_o^* lies is detected. When V_o^* moves from one sector to another sector, the sector change detection logic updates the sector in controller logic. Here, unlike the above sector change logic, the outer hysteresis comparators are not required. Also, during sector change, the current error will not be allowed to move out of the hexagonal boundary. This results in a better compensation and improved harmonic elimination.

6 Implementation consideration

6.1 Signal conditioning

The current and voltage signals are sensed using the Hall effect sensors and instrumentation amplifiers. This acquisition system is built to reduce the amplitude of the signal reference in the range of 0–3.3 V.

6.2 Digital signal processor (DSP)

Easy implementation of SAPF control strategies with the help of the DSP has increased research interest in the area [32, 33]. TMS320LF2407A is used to implement the active filter.

6.3 Control strategies: practical implementations

The control strategies that are explained in the earlier sections have some differences in implementation using DSP TMS320LF2407A. The flowcharts of the control strategies that are being implemented are shown in Fig. 3*d*. Table 2 shows the comparison of implementation considerations for SAPF based on IRP and Fryze.

6.4 APF inductor and dc-link design

6.4.1 Design for simulation studies:

V_{dc}	dc-link voltage
C_{dc}	dc-link capacitance
E_a	supply phase voltage at PCC
V_{line}	line voltage at PCC
E	energy stored in C_{dc}
P	power rating of the system in VA
T	time of discharge of C_{dc} (value taken as that of two cycles of fundamental i.e. 40 ms)
I	load current rms value

System parameters

$$E_a = 230 \text{ V}, \quad V_{line} = \sqrt{3} \times E_a = 398 \text{ V}, \quad I = 6 \text{ A}$$

dc-Link capacitor voltage (V_{dc}): For a two-level inverter connected to PCC dc-link voltage of inverter is

$$V_{dc} = \sqrt{2} \times E_a \ (\text{for } 1-\Phi \text{ system}) \tag{18}$$

$$V_{dc} = \sqrt{2} \times V_{line} = \sqrt{2} \times 398 \ (\text{for } 3-\Phi \text{ system}) \quad V_{dc} = 563 \text{ V} \tag{19}$$

Thus, V_{dc} is considered as 600 V.

Table 2 Comparison of implementation considerations for different strategies of reference compensating current generation

Parameter	IRP	Fryze
dynamic response	good	poor
linearity	poor	better
execution time in DSP 2407.	6 μs (approx)	3.5 μs (approx)
axis transformation (3Φ–2Φ)	required	not required
zero sequence components	not affected	affected
power definitions	$\alpha\beta$-axis	*abc*-axis
resolution of bits in DSP 2407	poor	better

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dc-Link capacitance C_{dc}

$$P = \frac{V_{\text{line}}}{\sqrt{2}} \times I = \frac{398}{\sqrt{2}} \times 5.67 = 1596 \text{ VA} \tag{20}$$

$$E = \frac{1}{2} \times C_{\text{dc}} \times {V_{\text{dc}}}^2 \tag{21}$$

$$E = P \times T \tag{22}$$

Thus

$$P \times T = \frac{1}{2} \times C_{\text{dc}} \times {V_{\text{dc}}}^2 \tag{23}$$

$$C_{\text{dc}} = \frac{P \times T}{(1/2) \times {V_{\text{dc}}}^2}$$

$$C_{\text{dc}} = \frac{1596 \times 40 \times 10^{-3}}{(1/2) \times (600)^2} \tag{24}$$

$$= 355 \ \mu\text{F}$$

Thus, C_{dc} is taken as rounded off value of 1000 μF.

Inductor design: The maximum value of the SAPF inductor to be considered is given by the equation

$$L = \frac{((V_{\text{dc}})/(\sqrt{2})) - ((V_{\text{line}})/(\sqrt{2}))}{n \times \omega \times I_n} \tag{25}$$

where L is the APF inductor, n is the order of harmonics, I_n is the harmonic current, f is the frequency of supply 50 Hz and $\omega = 2 \times \pi \times f$.

The inductor should allow the flow of compensating current which includes the harmonic components of load current. Also, at the same time, it should be ensured that it does not allow the high frequency harmonics generated because of switching of the inverter to flow to the supply [34]. Fig. 4*a* shows the simulation result of non-linear load current. Table 3 gives the amplitude of each harmonic in the FFT of load current. Triplen and third harmonics are neglected. Contributions of harmonics upto the 19th order are considered for inductor design. Exact value of the inductor is found by substituting the values in (25)

$$\begin{aligned} L = \frac{(600/(\sqrt{2})) - (398/(\sqrt{2}))}{(5 \times 2 \times \pi \times 50 \times 0.25 \times 6} \\ +7 \times 2 \times \pi \times 50 \times 0.17 \times 6 \\ +11 \times 2 \times \pi \times 50 \times 0.12 \times 6 \\ +13 \times 2 \times \pi \times 50 \times 0.09 \times 6 \\ +17 \times 2 \times \pi \times 50 \times 0.07 \times 6 \\ +19 \times 2 \times \pi \times 50 \times 0.06 \times 6) \end{aligned}$$

$$L = 10.4 \text{ mH}$$

Here, for simulation studies L is taken as 1 mH as a result of which it not only blocks the high frequency harmonics caused by switching of the shunt APF inverter but also allows the flow of reference compensating current through it.

6.4.2 Design for practical implementation: System parameters

$$E_a = 100 \text{ V}$$

$$V_{\text{line}} = \sqrt{3} \times E_a = 173 \text{ V}$$

$$I = 1.3 \text{ A}$$

dc-Link capacitor voltage (V_{dc}): For a two-level inverter connected to PCC dc-link voltage of inverter is

$$V_{\text{dc}} = \sqrt{2} \times V_{\text{line}} = \sqrt{2} \times 173$$
$$= 244 \text{ V } (\text{for } 3 - \Phi \text{ system})$$

dc-Link capacitance C_{dc}: Using (20) and (24)

$$P = \frac{V_{\text{line}}}{\sqrt{2}} \times I = \frac{173}{\sqrt{2}} \times 1.3 = 159 \text{ VA}$$

$$C_{\text{dc}} = \frac{P \times T}{(1/2) \times {V_{\text{dc}}}^2}$$

$$C_{\text{dc}} = \frac{159 \times 40 \times 10^{-3}}{(1/2) \times (300)^2} = 141 \ \mu\text{F}$$

Thus, $C_{\text{dc}} = 141$ μF.

Inductor design: using (25)

$$L = \frac{((V_{\text{dc}})/(\sqrt{2})) - ((V_{\text{line}})/(\sqrt{2}))}{n \times \omega \times I_n}$$

Fig. 4*b* shows the experimental result of non-linear load current. Table 4 gives the amplitude of each harmonic in the FFT of load current. Contributions of harmonics upto the 19th order are considered for inductor design. Hence, it will not allow the flow of high frequency switching harmonics which are greater than the 19th order harmonics.

$$\begin{aligned} L = \frac{((300)/(\sqrt{2})) - ((173)/(\sqrt{2}))}{(5 \times 2 \times \pi \times 50 \times 0.7135 \times 1.3} \\ +7 \times 2 \times \pi \times 50 \times 0.4691 \times 1.3 \\ +11 \times 2 \times \pi \times 50 \times 0.107 \times 1.3 \\ +13 \times 2 \times \pi \times 50 \times 0.0368 \times 1.3 \\ +17 \times 2 \times \pi \times 50 \times 0.03 \times 1.3 \\ +19 \times 2 \times \pi \times 50 \times 0.021 \times 1.3) \end{aligned} = 23.35 \text{ mH}$$

7 Simulation results

The proposed current error space phasor hysteresis controller-based shunt APF is modelled and simulated using a Matlab platform and its Power System Blockset of Simulink toolbox. Various simulation results are obtained under ideal balanced mains voltage conditions.

The essential parameters selected for the simulation studies are: fundamental frequency = 50 Hz, rectifier load inductance = 1 mH, rectifier load resistance = 50 Ω, three-phase (line-to-neutral) ac supply voltage = 230 V, dc-link voltage $V_{\text{dc}} = 600$ V, dc-link capacitor $C_{\text{dc}} = 1000$ μF and APF side inductance = 1 mH. Figs. 4*c* and *d* show the sectors of the voltage space phasor structure of the APF where V_o^* lies at a particular instant and the corresponding

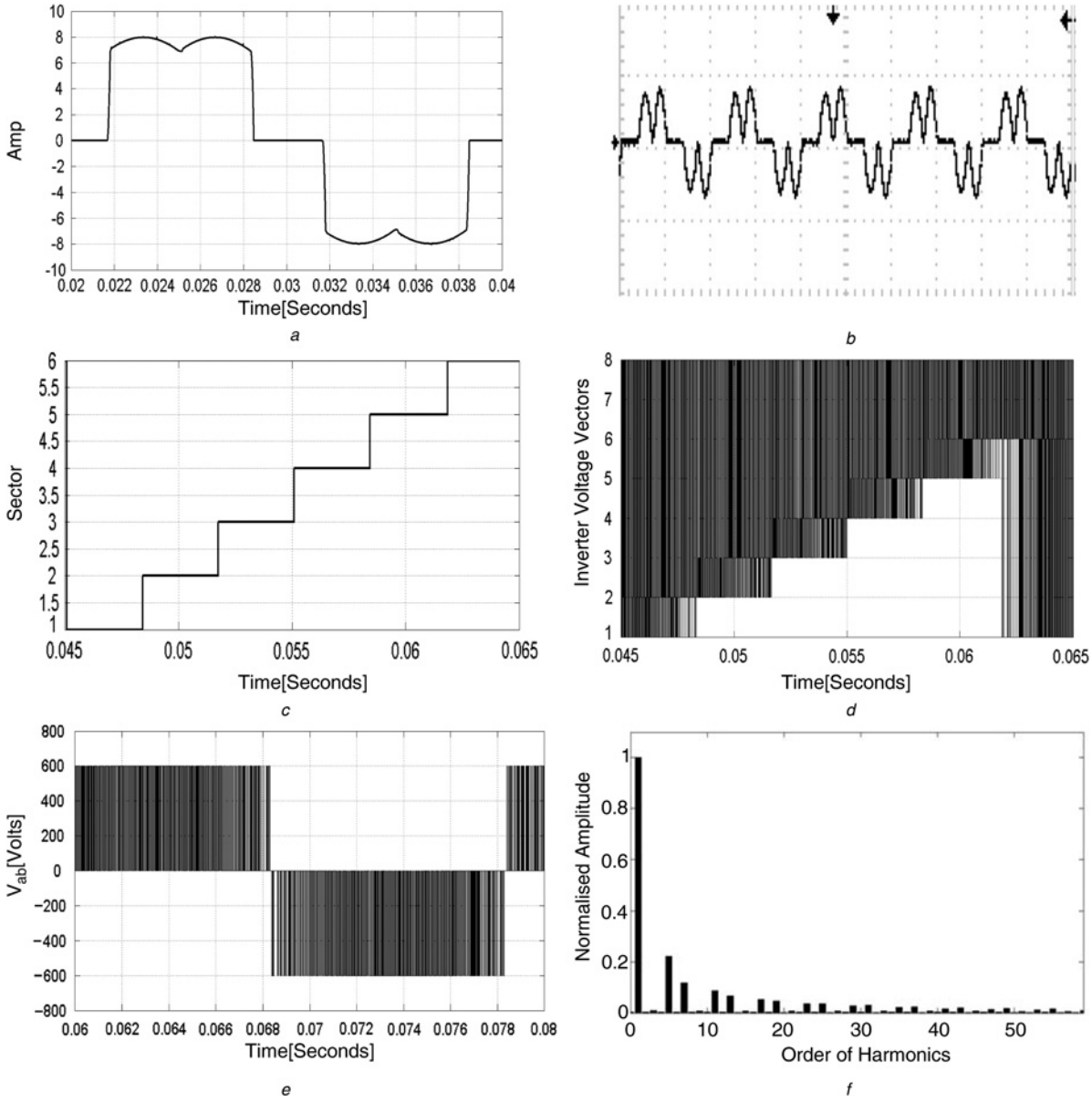

Fig. 4 *Behaviour of the proposed controller based SAPF*

a One fundamental cycle of load current i_{la} (simulation result) [*X*-axis: 0.002 s/div.; *Y*-axis: 2 A/div]
b Load current i_{la} (experimental result) [scale: *X*-axis: 10.0 ms/div.; *Y*-axis: 2 A/div.]
c Sectors of voltage space phasor structure [*X*-axis: 0.005 s/div.; *Y*-axis: 0.5/div.]
d APF voltage vector (adjacent) switched for various sectors [*X*-axis: 0.005 s/div.; *Y*-axis: 1/div.]
e APF output voltage V_{ab} [*X*-axis: 0.002 s/div.; *Y*-axis: 200 V/div.]
f Normalised harmonic spectrum of i_{la} [*X*-axis: 10/div.; *Y*-axis: 0.2/div.]

voltage vectors switched. Output voltage of the APF (between *a*-phase and *b*-phase (V_{ab})) is shown in Fig. 4*e*. Non-linear load current is shown in Fig. 4*a* and its normalised harmonic spectrum is given in Fig. 4*f*. The %THD of this load current is 28.56%. Presence of $6n \pm 1$ harmonics is quite evident in the spectrum as it is for current drawn by a six-pulse converter used as non-linear load in the proposed studies.

Table 3 Contribution of individual harmonics in load current (simulated)

Order of harmonics	Amplitude
5th	0.25
7th	0.17
11th	0.12
13th	0.09
17th	0.07
19th	0.06

Table 4 Contribution of individual harmonics in load current (experimental)

Order of harmonics	Amplitude
5th	0.7135
7th	0.4691
11th	0.107
13th	0.0368
17th	0.03
19th	0.021

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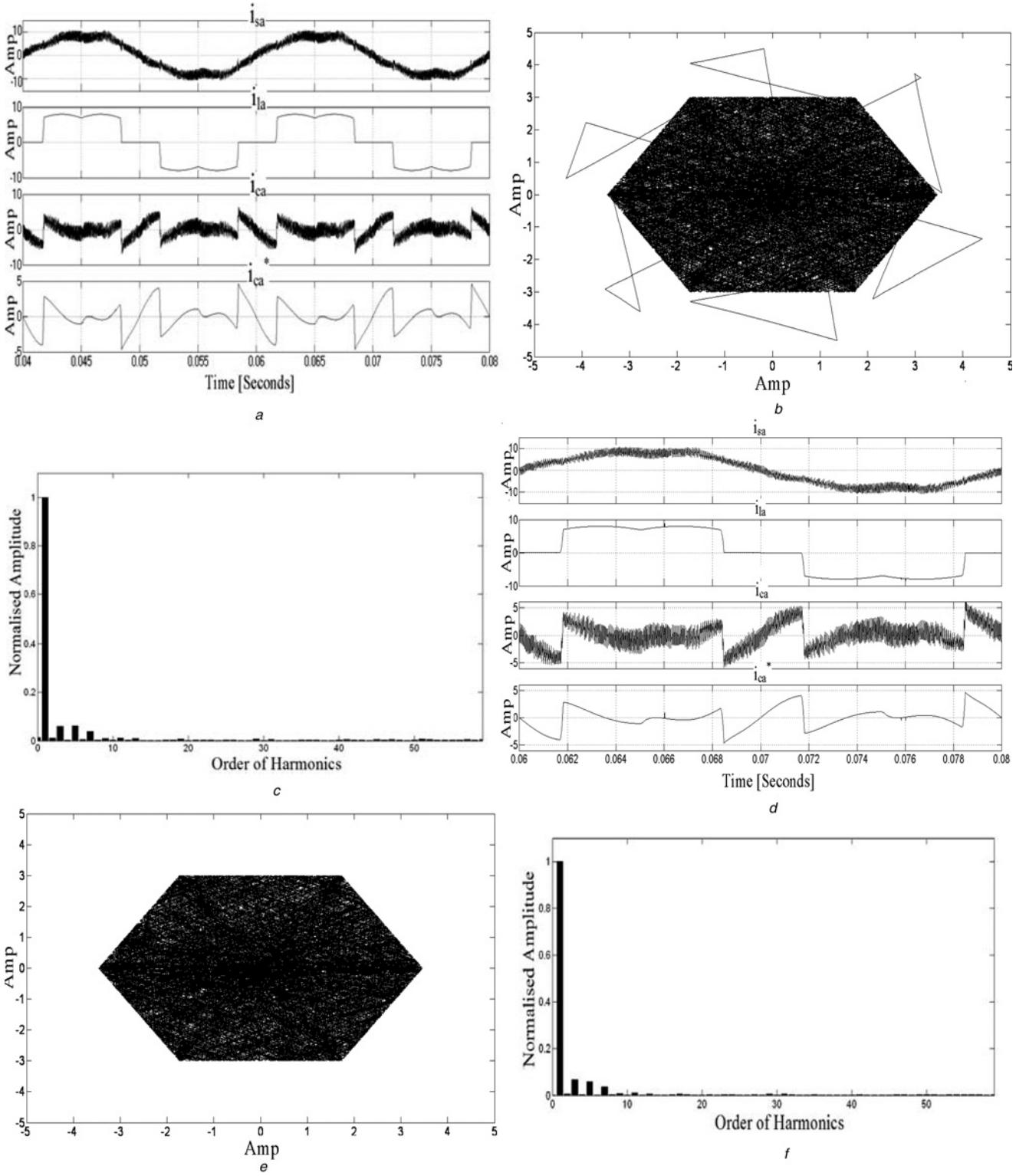

Fig. 5 *Performance of the proposed controller based SAPF for IRP theory*

a IRP theory results for phase *A* – source current (i_{sa}) [*Y*-axis: 10 A/div.]; load current (i_{la}) [*Y*-axis: 10 A/div.]; actual compensating current (i_{ca}) [*Y*-axis: 10 A/div.] and reference compensating current (i_{ca}^*) [*Y*-axis: 5 A/div.]; [*X*-axis: 0.005 s/div.]
b Current error space phasor [*X*-axis: 1 A/div.; *Y*-axis: 1 A/div.]
c Normalised harmonic spectrum of i_{sa} [*X*-axis: 10/div.; *Y*-axis: 0.2/div.]
d IRP theory results (without outer hysteresis band) for phase *A* – source current (i_{sa}) [*Y*-axis: 10 A/div.]; load current (i_{la}) [*Y*-axis: 10 A/div.]; actual compensating current (i_{ca}) [*Y*-axis: 5 A/div.] and reference compensating current (i_{ca}^*) [*Y*-axis: 5 A/div.]; [*X*-axis: 0.002 s/div.]
e Current error space phasor (without outer hysteresis band) [*X*-axis: 1 A/div.; *Y*-axis: 1 A/div.]
f Normalised harmonic spectrum of i_{sa} (without outer hysteresis band) [*X*-axis: 10/div.; *Y*-axis: 0.2/div.]

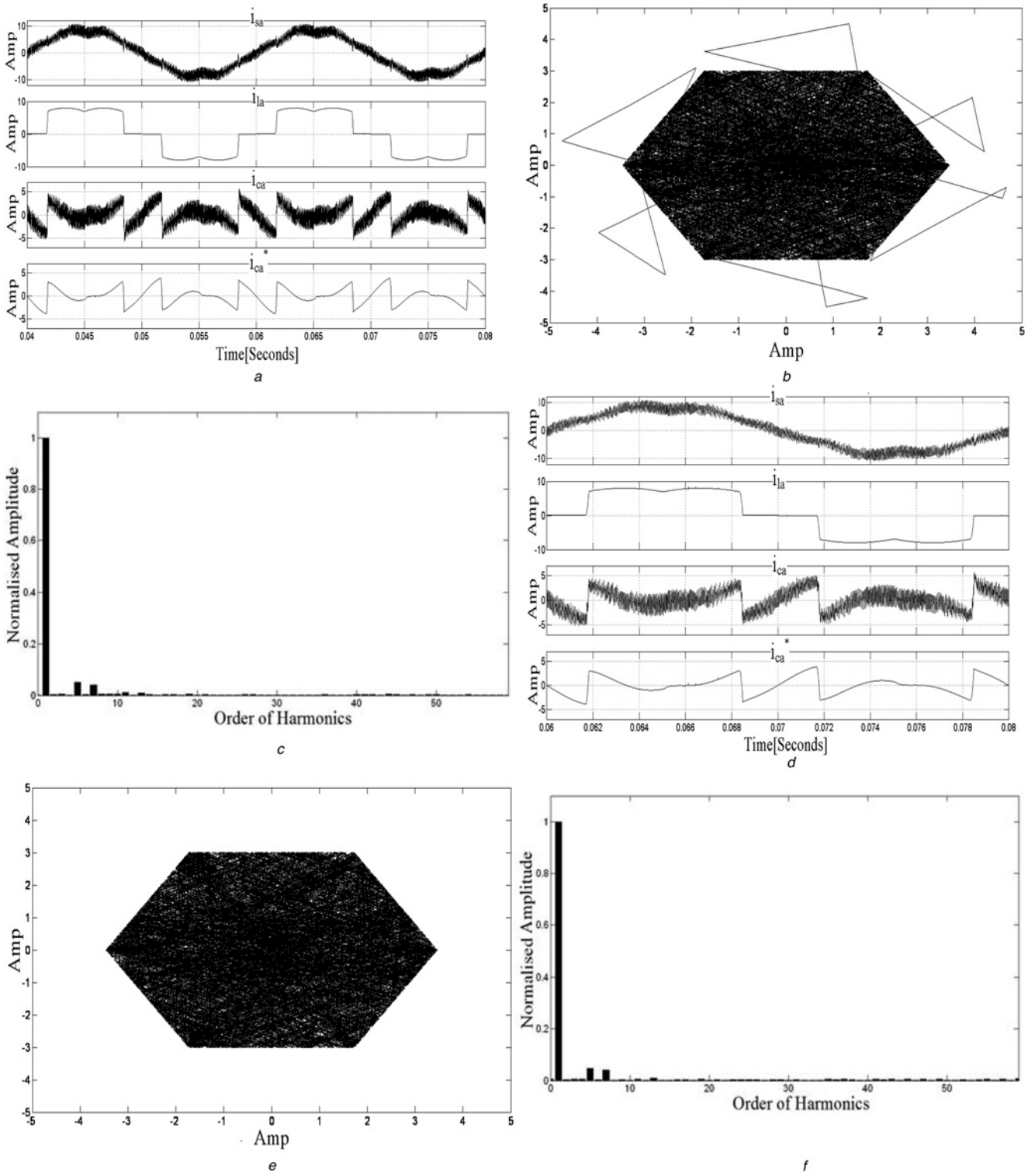

Fig. 6 *Performance of the proposed controller based SAPF for Fryze current computation technique*

a Fryze current computation technique results for phase *A* – source current (i_{sa}) [*Y*-axis: 10 A/div.]; load current (i_{la}) [*Y*-axis: 10 A/div.]; actual compensating current (i_{ca}) [*Y*-axis: 5 A/div.] and reference compensating current (i_{ca}^*) [*Y*-axis: 5 A/div.]; [*X*-axis: 0.005 s/div.]
b Current error space phasor [*X*-axis: 1 A/div.; *Y*-axis: 1 A/div.]
c Normalised harmonic spectrum of i_{sa} [*X*-axis: 10/div.; *Y*-axis: 0.2/div.]
d Fryze current computation technique results (without outer hysteresis band) for phase *A* – source current (i_{sa}) [*Y*-axis: 10 A/div.]; load current (i_{la}) [*Y*-axis: 10 A/div.]; actual compensating current (i_{ca}) [*Y*-axis: 5 A/div.] and reference compensating current (i_{ca}^*) [*Y*-axis: 5 A/div.]; [*X*-axis: 0.002 s/div.]
e Current error space phasor (without outer hysteresis band) [*X*-axis: 1 A/div.; *Y*-axis: 1 A/div.]
f Normalised harmonic spectrum of i_{sa} (without outer hysteresis band) [*X*-axis: 10/div.; *Y*-axis: 0.2/div.]

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Table 5 Performance of SAPF

Reference current generation schemes	Without using SAPF (THD, %)	SAPF using controller with outer hysteresis band (THD, %)	SAPF using controller without outer hysteresis band (THD, %)
IRP	28.56	9.59	9.48
Fryze		6.38	6.26

7.1 IRP theory

Here, a simulation is conducted using generalised IRP theory. The results are shown in Figs. 5*a* and *b*. This APF helps reduce the source current THD from 28.56% (without compensation) to 9.59%. The results of Fig. 5*a* clearly depict that the controller is fast and accurate enough to enable the actual compensating current to track the reference compensating current.

The current error space phasor plot is shown in Fig. 5*b*. It is seen that the current error is restricted well within the hexagonal boundary. Sector change is also clearly visible. Fig. 5*c* shows the normalised harmonic spectrum of i_{sa} for one fundamental cycle.

Also, the results for the current error hysteresis controller without outer band are shown in Fig. 5*d*. This APF helps reduce the source current THD from 28.56% (without compensation) to 9.48%. The results of Fig. 5*d* clearly show that the controller is fast and accurate enough to enable actual compensating current to track the reference compensating current. The current error space phasor plot is shown in Fig. 5*e*. It is seen that the current error is restricted well within the hexagonal boundary and the error during sector change is also being confined well within the boundary. Fig. 5*f* shows the normalised harmonic spectrum of i_{sa} for one fundamental cycle.

7.2 Fryze current computation technique

This method for the APF helps reduce the source current THD from 28.56% (without compensation) to 6.38%. The results are given in Figs. 6*a* and *b*. This method is easy to implement. The current error space phasor plot is shown in Fig. 6*b*. It is seen that the current error is restricted well within the hexagonal boundary. Sector change is also clearly visible. Fig. 6*c* shows the normalised harmonic spectrum of i_{sa} for one fundamental cycle.

Also the results for the current error hysteresis controller without outer band are shown in Fig. 6*d*. This method for the APF helps reduce the source current THD from 28.56% (without compensation) to 6.26%.

The current error space phasor plot is shown in Fig. 6*e*. It is seen that the current error is restricted well within the hexagonal boundary and the error during sector change is also being confined well within the boundary. Fig. 6*f* shows the normalised harmonic spectrum of i_{sa} for one fundamental cycle.

Performance of the SAPF is shown in Table 5 for different schemes of reference compensating current generation with various logics of sector change detection.

8 Experimental results

To validate the performance, a prototype test setup has been built for 415 V and 3–Φ utility. The whole control algorithm, that is, the reference compensating current calculation method and the proposed controller are being implemented using DSP TMS320LF2407A. The load is emulated by a three phase diode bridge rectifier with a resistance of 100 Ω and a smoothing capacitor.

Figs. 7*a* and *b* show the line voltage and non-linear load current when the external offset signal is not used. These experimental results are observed at the DAC terminal of

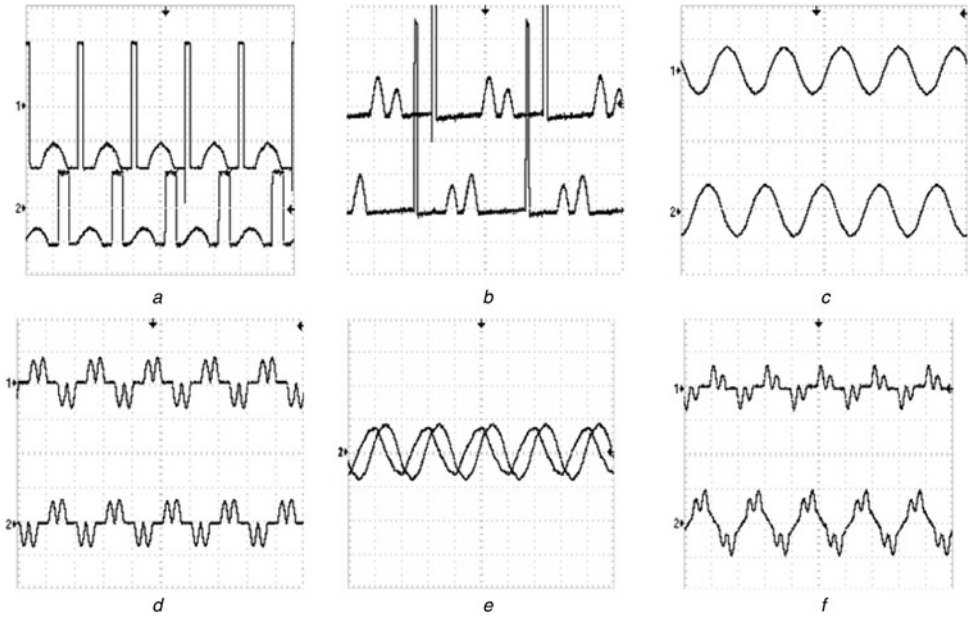

Fig. 7 *Sensing and processing of variables*

a Line voltages without signal conditioning [*X*-axis: 10 ms/div., *Y*-axis: 40 V/div.]
b Non-linear load current without signal conditioning [*X*-axis: 10 ms/div.; *Y*-axis: 2 A/div.]
c Line voltages [*X*-axis: 10 ms/div.; *Y*-axis: 40 V/div.]
d Non-linear load current [*X*-axis: 10 ms/div.; *Y*-axis: 2 A/div.]
e Clarke's transformation of line voltage [*X*-axis: 10 ms/div.; *Y*-axis: 40 V/div.]
f Clarke's transformation of load current [*X*-axis: 10 ms/div.; *Y*-axis: 2 A/div.]

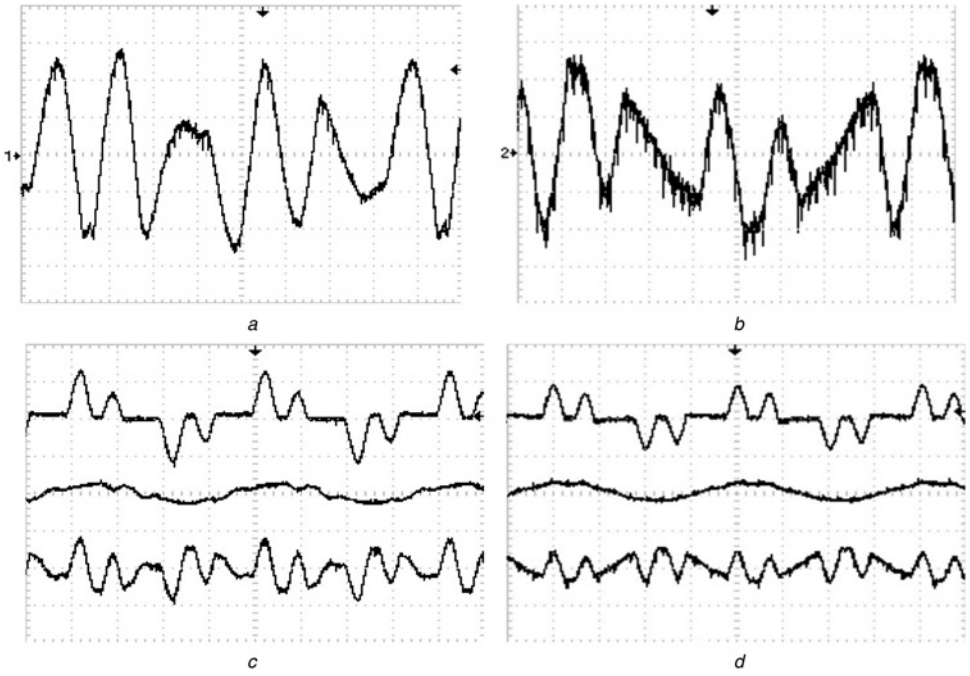

Fig. 8 *Experimental results of reference compensating currents*

a Reference compensating currents (IRP theory) [*X*-axis: 2.5 ms/div.; *Y*-axis: 2 A/div.]
b Reference compensating currents (Fryze current computation technique) [*X*-axis: 2.5 ms/div.; *Y*-axis: 2 A/div.]
c Results of $i_{la} - i_{ca}^*$ (IRP theory) upper trace: load current i_{la}, middle trace: source current i_{sa} ($= i_{la} - i_{ca}^*$), lower trace: reference compensating current i_{ca}^* [*X*-axis: 5 ms/div.; *Y*-axis: 2 A/div.]
d Results of $i_{la} - i_{ca}^*$ (Fryze current computation technique) upper trace: i_{la}, middle trace: i_{sa} ($= i_{la} - i_{ca}^*$), lower trace: i_{ca}^* [*X*-axis: 5 ms/div, *Y*-axis: 2 A/div]

the DSP. It is clearly observed that the negative part of the signal is clipped off when the external offset circuitry is not used. Also, Figs. 7*c* and *d* show the waveforms of the line voltage and the load current using the external offset circuit. Experimental results for Clarke's transformation of voltages and currents using DSP are shown in Figs. 7*e* and *f*, respectively. Figs. 8*a* and *b* show the reference compensating currents obtained using the IRP and the Fryze current computation technique, respectively. Also, Figs. 8*c* and *d* show the source current obtained by subtracting the reference compensating current from the load current using both the methods, respectively.

9 Conclusion

A unique approach of applying the space phasor-based current error hysteresis controller to the SAPF is presented in this paper. Design considerations made for DSP-based implementation of SAPF are also presented. Comparison for DSP TMS320LF2407A-based implementation of IRP theory and Fryze current computation method for generation of reference compensating currents is shown in this paper. Performance of the controller is tested for two different methods of reference compensating current generation applied to the SAPF. Also, controller with different self-adaptive sector change logics is tested and the performance is found to be satisfactory. The results prove the adaptable nature of the controller which can be used for any type of reference compensating current generation technique. The simulation studies show that the response of the controller is good and it is able to maintain the current error within the desired hexagonal boundary. The APF is able to compensate for the harmonics as a result of which the line current is having good THD and low harmonics. Harmonic compensation is better with the Fryze current computation technique as compared with the IRP technique. The results indicate better filtering performance of the APF using the controller without outer hysteresis band as compared with that with outer hysteresis band. Experimental results of reference compensating currents generated using DSP for both methods are presented and found to be in line with the simulation results.

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