Implementation of Anti-Islanding Scheme for Grid Connected Inverter Using ATmega328

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Arup Kumar Saikia
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ABSTRACT

The phenomenon of unintentional islanding due to the distributed generation resources is undesirable. It has potential safety hazards to the utility workers; may damage the DGs, power supply utilities and the consumer load. An anti-islanding scheme which detects the islanding and clears it within 2 seconds is to be developed. This scheme is developed for single phase grid connected inverter. The converter topology has been proposed for the anti-islanding scheme which is to be simulated and later comparing with the hardware results.

An anti-islanding scheme to be developed has to meet the established IEEE standard 1547-2003 and 929-2000, set for the inter connection of distributed resources with the electrical power system. The proposed scheme uses an active method and maintains high power quality by using a combination of periodic current magnitude and AFD (active frequency drift) method. The proposed scheme also maintains lower THD of output current. The scheme is developed and simulated in PSIM software with the parameters for the circuit decided and designed accordingly.

The proposed scheme has to be implemented and fabricated in hardware by modelling the H-bridge inverter using MOSFETs. The gate driver circuit has to be prepared by using microcontroller ATmega328 for the SPWM of the inverter. The proposed anti-islanding scheme is also to be implemented by using ATmega328. The algorithm is to be developed for a single phase inverter using ATmega328 and real time tests are to be carried out.

List of Figures

Abbreviations

DG ..... Distributed Generation
IEC ..... International Electrotechnical Commission
IEEE ..... Institute of Electrical and Electronic Engineers
PCC ..... Point of Common Coupling
IGBT ..... Insulated Gate Bipolar Transistor
OVR ..... Over Voltage Relay
UVR ..... Under Voltage Relay
OFR ..... Over Frequency Relay
UFR ..... Under Frequency Relay
PV ..... Photovoltaic
PWM ..... Pulse Width Modulation
EPS ..... Electrical Power Source
NDZ ..... Non Detection Zone
THD ..... Total Harmonic Distortion
MPPT ..... Maximum Power Point Tracking
ZCD ..... Zero Crossing Detector
AFD ..... Active Frequency Drift
AFDPF ..... Active Frequency Drift with Positive Feedback
AIM ..... Anti Islanding Method
AFDPCF ..... AFD with Pulsation of Chopping Fraction

Nomenclature

P_{inv} ..... Inverter Output Power

V_i ..... Inverter Output Voltage

I_l ..... Load Current

V_{grid} ..... Grid Voltage

f_s ..... Switching Frequency

V_{PCC} ..... Voltage at Point of Common Coupling

P ..... Active Power

Q ..... Reactive Power

ΔP ..... Change in Active Power

ΔQ ..... Change in Reactive Power

Q_f ..... Quality Factor

c_f ..... Chopping Fraction

f ..... System Frequency

L_o ..... Load Inductance

R_o ..... Load Resistance

C_o ..... Load Capatiance

Contents

Chapter 1

INTRODUCTION

Over the past decades, the rapid fall of the PV manufacturing cost has led to the fast development of PV energy system. This has made PV one of the most promising renewable energy resources in distributions generation (DG).[7] So, the abnormal operating conditions that could affect the grid connected PV systems have to be prevented. One of the major safety related issue is the challenge to avoid unintentional islanding of PV inverter.

According to IEEE Standard 1547-2003, *An island is defined as a condition in which a portion of an area EPS is energized solely by one or more local EPSs through one common PCC while that portion of the area of the EPS is electrically separated from the rest of the area EPS.*[5] DG opens, there is the possibility that an island will form. The concern in this situation is the condition in which the amount of isolated load is close to the amount of generation in the island. Under these conditions, the island can have slowly changing voltage or frequency. If the load and generation are not matched (at least a 3-to-1 ratio), then the voltage or frequency will change rapidly, and an unintentional island should not occur.

During islanding mode the utility circuit breaker is opened while the DG is still injecting power supply to the local load. This phenomenon occurs when utility suffers from unpredictable interruption of abnormality, such as voltage shut-down, short-circuit or equipment failure. There are two types of islanding intentional and unin-

tentional islanding. Typically intentional islanding is harmless to the power system because the problem can be solved during or after the grid disconnection. However unintentional islanding can cause a severe impact to the power system stability due to the loss of grid synchronization. Another issue persists in islanding mode whereby the technical workers may be placed under safety hazards as they may not be aware of that section is continuously powered by DG. Anti-islanding protection is one of the most important protecting functions of a grid connected PV system. Its potential dangers can be issue as follows:[9]

a. Islanding may pose a hazard to the maintenance personnel.

b. If the connection was re-established at a point where the island and the grid bear different magnitudes or phases, large current may flow through the connection and damage the equipment nearby.

c. Islanding may disrupt the function of utility reclosers.

d. Three phase loads may be supplied by single phase power source.

When an islanding occurs it takes finite time to detect and react. It is also undesirable for a EPS to island beyond 2 seconds on an unplanned basis. This will cause power-quality and safety problems which will affect the islanded area and local loads. During area EPS repair operations, such as dealing with downed conductors, it is important that workers use their mandatory safe work practices that invariably require them to validate that lines are de-energized or use hot work practices. Unintentional islanding poses threat to the public, emergency response personnel, and utility workers because the source of the DG is always unknown. For example, applying the safety ground to energized conductors (from the unintentional island) will cause a fault and possible injury to area EPS personnel. The local EPS source feeding an unintentional island may not be able to sustain the fault arc and lead personnel to mistakenly beleive that the conductors are de-energized. Service restoration can be delayed as line crews seek to ensure that unintentional DG islanding is not a problem.

Reclosing operation of the upstream breaker or reclosing during unplanned islanding could cause major damage to the DG using the rotation machine because of out-of-phase closing. Area EPS devices (e.g., circuit breaker and reclosers) typically do not monitor load-side voltage and, therefore, assume the line is dead when a reclosing attempt is made. If the island is still energized by a DG, severe transients could result.

1.1 Problem Identification

Islanding of an EPS is hazardous because it leads to safety issues to the utility service personnel and may cause damage to power generation and power supply facilities because of unsynchronized re-closure. To prevent islanding phenomenon many anti-islanding methods have been developed. The passive methods are there but they have very large NDZ but they do not hamper the grid parameters. But active methods are fast and have very small NDZ, but they degrade the power quality and lower the THDi of the output current. Still active method are one of the most preffered one. Many active methods have been proposed for AIM. Untill now, frequency phase shift methods of inverter current is much popular as active AIMs. Out of various anti-islanding methods of which AFD method is the best and the simplest to implement.

But AFD method increases harmonic components of current, and phase variation method decreases the displacement power factor, which cause the lower power quality. Also the THD of the output current is high. The proposed method will be working on to reduce the THD to nominal value. Also AFD method gives fast response i.e. fast islanding detection than other methods. AFD has very small NDZ.

An Anti-Islanding Method is to be developed for a grid connected inverter which will remove the unintentional island formed by the DG within 2 seconds. The DG here is assumed to be a combination of solar array and the solar inverter. The solar inverter is connected to the grid. The solar inverter may be simulated with H bridge inverter and the utility may be simulated with an ac voltage source. And, the load

is to be modeled using a parallel RLC combination. Several options for simulation are available such as MATLAB, PSCAD, and PSIM. However, the circuit may be developed on PSIM as it is user-friendly software. Upon simulation the behavior of the circuit is to be analyzed.

1.2 Literature Survey

a. **Byunggyu Yu, Mikihiko Matsui, Gwonjong Yu, 2010. A review of current anti-islanding methods for photovoltaic power system.**
This paper gives a brief idea about the islanding phenomenon and the anti islanding methods used for the PV systems. The AIMs are classified and studied. The paper shows that active islanding is better compared to the passive one's. However, the active methods deteriorate the power quality. As a result the active islanding methods gives harmonic distortion and degrade the power factor based on the active signal injected. In addition to the evaluation and comparison of the main anti-islanding methods, this paper also summarizes the related anti-islanding standards to evaluate anti-islanding capability for PV system

b. **Y. Jung, J. Choi, B. Yu, G. Yu, J.So, J. Choi, 2005. A novel Active Frequency Drift Method of Islanding Prevention for the grid-connected Photovoltaic Inverter.**
AFD method which is an active AIM is found to be better compared to other AIM methods on the basis of earlier method. This paper gives an overview of AFD method and its improved version AFDPF. It mentions the disadvantages of this method and further go on to propose a novel AFD method with pulsation of chopping fraction. Through several theoretical concepts the authors strengthen the validity of this method. This paper proposes periodic chopping fraction based on AFD method which calculates the optimum value of chopping fraction for better performance of the AIM method.

c. **Byunggyu Yu, Mikihiko Matsui, Junghun So, Gwonjong Yu, 2008. A high power quality anti-islanding method using effective power variation.**

This paper proposes a high power quality active anti-islanding method using effective power variation, which is implemented by periodically increasing or decreasing variation of the inverter current magnitude. Causing the inverter output voltage vary greatly and then AFD method is injected to detect island. This method has reduced power degradation. Flowchart to develop the circuit, theoretical waveforms with the PSIM model is presented.

d. **Wei Yee Teoh, Chee Wei Tan,. "An Overview of Islanding Detection Methods in Photovoltaic Systems",World Academy of Science, Engineering and Technology 58, 2001**

Basic idea about islanding and different schemes of anti-islanding which are used to detect an island and prevent it. The brief idea about active and passive methods used and their operating principle with there advantages and disadvantages. All the passive and active methods are discussed in brief. For each studied AIM the operation analysis is described while the advantages and disadvantages are compared and discussed. The paper concludes that the setup and operation cost is a vital factor for anti-islanding method selection in order to achieve minimal compromising between cost and system quality.

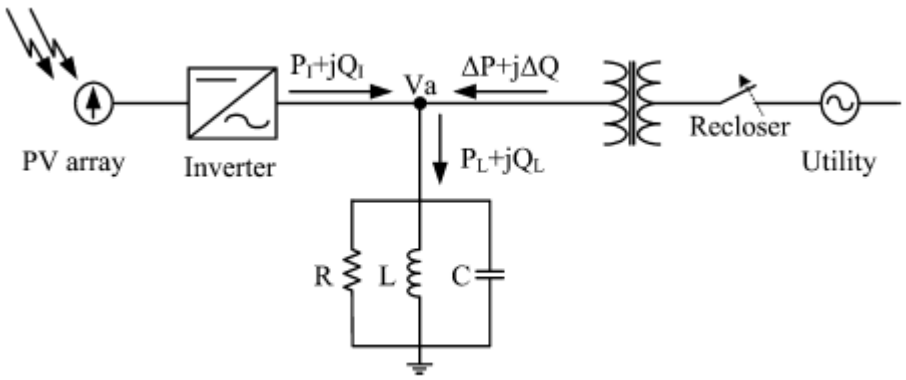

Figure 1.1: Typical grid connected PV system[11]

Chapter 2

ANTI-ISLANDING METHODS

Islanding of an EPS is the independent powering to a portion of the utility system even when the portion has been disconnected from the rest of the utility source. For better understanding of islanding phenomena, two key factors have to be highlighted. The first factor is the non detected zone (NDZ) and the second is the quality factor (Q factor). Both factors are used as the criteria to study the effectiveness of islanding detection methods. The NDZ shows the interval between the moment which islanding is detected to the moment where islanding occurred in the DG.[8] This region gives the power mismatch between DG generating power and local load consuming power, therefore creating a real power variation (ΔP) and reactive power variation (ΔQ).

For this reason, the variations must be significant such that islanding detection takes place within permitted time interval. Hence, NDZ is the sole factor as evaluation index for an islanding detection method. The second feature, which is the Q factor, is defined as *two pi times the ratio of the maximum storage energy to the energy dissipated per cycle at a given frequency.*[4, 8] It exhibits the relative amount of energy storage and energy dissipation in the RLC circuit. A high Q factor may hinder the effectiveness of islanding detection, hence the value of Q factor is directly affected by potential local load inside the island. The

quality factor is directly proportional to the NDZ. So minimizing the NDZ and improving thr response time of islanding detection have become major concern nowadays.

There are many anti-islanding methods developed till now. These are concisely categorized into two families, namely local and remote islanding techniques. The first one depends on measurement of system parameters at the DG and the second one is based on the communication between the utility grid and the DG. Due to the simplicity, the research trend mainly goes to the local AIMs. The other control techniques under the two main families are summarized as shown in the flow chart.

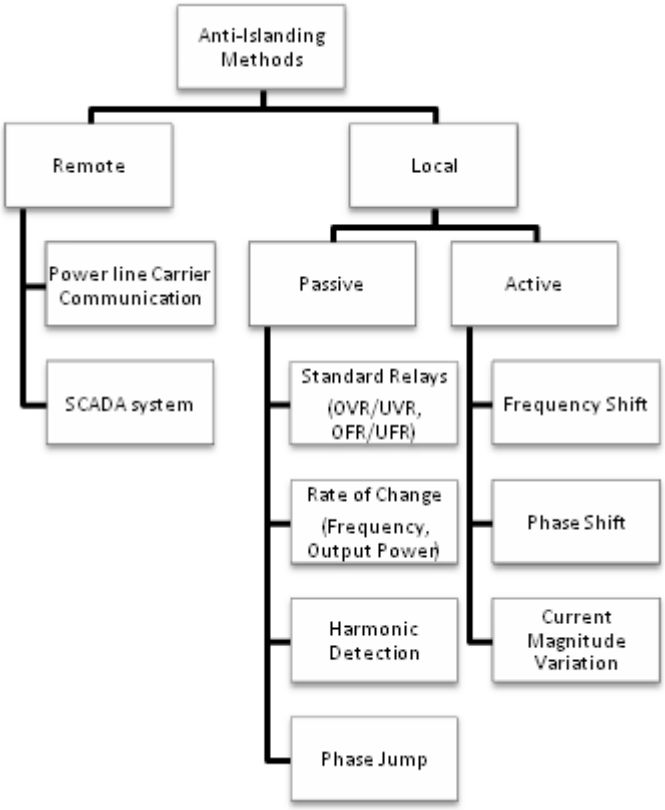

Figure 2.1: Classification of AIMs

2.1 Remote Methods

This method utilizes Power Line Carrier Communications(PLCC) and Supervisory Control and Data Acquisition (SCADA). These techniques rely on communication between utilities and DGs. NDZ in this method is almost zero. The monitoring of system parameters is done by SCADA and the communication is handled by the PLCC system. Some advantages of this method are enlisted as follows.

(1) Robust High cost

(2) Difficult to implement

(3) Need communication infrastructure

2.2 Passive Methods

This method employs measurement of the parameters of the system (such as the variation in the voltage, frequency, harmonic distortion or the power) which causes the inverter to change the output power such that it meets the given specified conditions during islanding conditions during islanding mode of operation. During islanding mode of operation parameters of the system greatly changes at the point of common coupling (PCC).[8] The difference between islanding condition and normal condition is depended on threshold settings of system parameters. To differentiate the conditions between islanding operation and other disturbances in controlled system extreme care should be taken while setting the value of threshold.[8] In general passive islanding detection techniques does not create any disturbance in the system and are fast, however it has large NDZ which could fail islanding detection.

2.3 Active Methods

In active islanding detection method a small disturbance signal is injected to the certain selected parameters at the PCC. When entering in the islanding mode of operation a small disturbance signal which is injected to system will become significant which will help the inverter to cease power conversion. Hence, during the cessation of power conversion the values of system parameter will be varying , and by measuring the corresponding system parameters, islanding condition can be detected.[8]

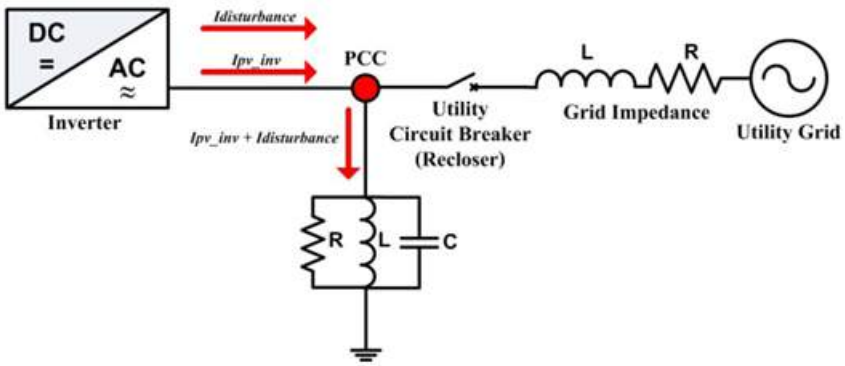

Figure 2.2: The Path of Disturbing Signals During Islanding Conditions[8]

The basic requirements of an anti-islanding scheme would be:

- Minimum NDZ.
- Impact on power quality should be minimum.
- Capability to detect islanding condition should be good enough.
- It should be cost effective.
- Neutrality with respect to DG technologies.
- It should work with multiple DGs.

Active islanding methods usually involves feedback control technique which detects changes in the parameters such as frequency or voltage at the PCC. In

case when the PV inverter behaves as a current source, the current supplied to the utility is expressed by the following equation.

$$i_{PV\_inv} = I_{PV\_inv} sin(\omega_{PV} + \phi_{PV})$$

Where I_{PV_inv} is the inverter current amplitude ($i_{PV\_inv} = I_{PV\_inv} + I_{disturbance}$), ω_{PV} is the frequency and ϕ_{PV} is phase angle.[8] These three parameters can be varied and modified, and can be set as disturbance signals required as per the scheme. Active methods effectively reduces the NDZ to minimum and detect islanding conditions accurately. However the requirement of additional control circuits to create adequate disturbances which increases the complexity for implementation of the scheme. These, additional circuits may cause unpredicted effects to the electric power quality, such as the deterioration of the grid voltage quality and system instability.

Active AIMs are categorised into three parts with respect to what the variation parameter is. These parameters are current magnitude, frequency, and the start phase. More specifically they are described in detail as frequency shift methods, phase shift methods and the current magnitude variation method.[2] All the methods are explained breifly as follows.

2.4 Frequency Shift Methods

Active Frequency Drift (AFD): - In AFD method the frequency of the grid current is set slightly lower or higher than that of grid voltage, and checks the response to find out whether the grid has been cut off. In AFD method a slightly frequency bias signal is forced into the grid via PCC, but recovers back at the end of every half cycle by jumping back into phase when voltage passes zero crossing. This method can be used for multi-inverter systems, however

may bring in some increment of total harmonic distortion (THD) of the grid current.

AFD with Positive Feedback (AFDPF): - AFDPF or Scandia Frequency Shift Method is a new and improved method from AFD. AFDPF using positive feedback by creating a slightly misaligned phase angle at the inverter output current through adding truncations or dead times to the currents waveform. Hence, the inverter output current frequency will be forced to a different value than the grid frequency. This method is not difficult to implement and has very small NDZ. But in this method the power quality of PV inverter is reduced slightly because when it is connected to the grid the positive feedback amplifies the changes that takes place on the grid.

AFD with Pulsation of Chopping Fraction (AFDPCF): - To overcome the weakness of the AFD method, a novel scheme with periodic pulsation of chopping fraction is proposed, which can deviate the frequency instantly away from the nominal value in islanding situation. This scheme is referred to as AFD with pulsation of chopping fraction (AFDPCF).

2.5 Phase Shift Methods

Slip-mode Frequency Shift Method (SMS): - SMS is the method forcing the phase of the inverters output to be slightly miss-aligned with the grid to cause variation in the inverter current.[8] SMS method applies positive feedback to the phase and hence the short term frequency. The phase angle of the current is controlled as a function of the deviation of the frequency of the last cycle from the nominal operating frequency of the utility grid. In this method quality factor and phase angle are directly proportional.[5]

2.6 Current Magnitude Variation Methods

Sandia Voltage Shift (SVS): - SVS uses positive feedback technique to prevent islanding based on amplitude of the voltage at PCC. When utility grid is connected there will be small or no effect on the power of the system. But once the utility is disconnected, there is reduction in V_{PCC}. According to load impedance relationship, this reduction will continue and as a result, current and power output reduces. Therefore this reduction in amplitude of V_{PCC} can be detected by UVR. SVS uses positive feedback technique to prevent islanding based on amplitude of the voltage at PCC.

Periodic Current Magnitude Variation (PCMV): - PCMV is a current magnitude variation method with the same amount of increase and decrease. So the total average output power is maintained during current variation period. Time varying current magnitude variation makes the voltages variation when islanding occurs. One of the advantages for this method is high power quality without injecting harmonic signal or phase angle.[2]

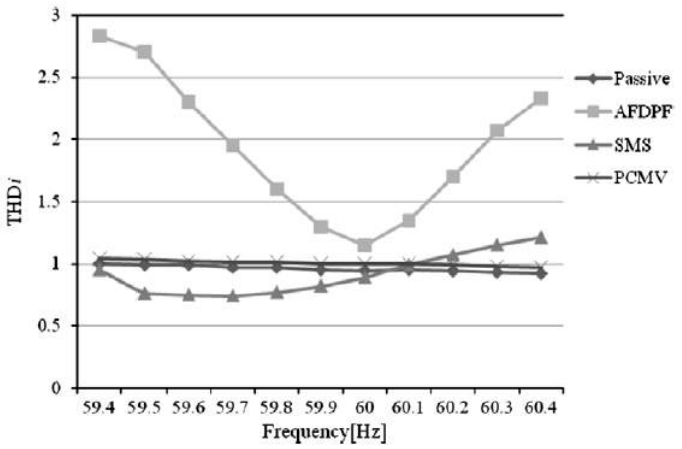

Figure 2.3: Comparison of THD of local AIMs[2]

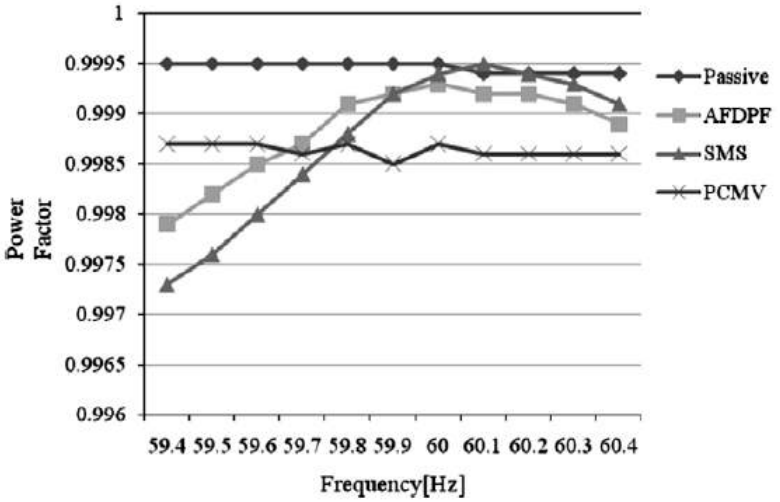

Figure 2.4: Power factor comparison of local AIMs[2]

Chapter 3

ACTIVE FREQUENCY DRIFT METHOD

There are different algorithms defining active frequency drift method. It can be implemented in different ways two of which are explained below.

3.1 Active Frequency Drift (AFD) Method

The typical frequency shift method is active frequency drift (AFD) method, which is easily implemented in PV inverter with a controller. This method is based on injection of a current waveform distortion to the original reference current of the PV inverter, to force a frequency drift in case of islanding operation. By introducing zero conduction time (t_z) at the end of each half cycle, the phase angle of the fundamental component of current is shifted. During normal grid connected operations the inverter usually operates with unity power factor and is synchronized to the grid voltage and will operate at grid frequency. In islanding operation, the added distortion to the current will produce a permanent drift in the operating frequency toward the local load resonance frequency in order to keep unity power factor. This drift will eventually reach the frequency

boundary limits set for islanding detection. In AFD method, the key design parameter is chopping fraction (c_f) defined as the ratio of the zero time (T_z) to half of the period of the voltage waveform ($T_{util}/2$) as shown in the following equation:[2]

$$c_f = \frac{2T_z}{T_{util}} \tag{3.1}$$

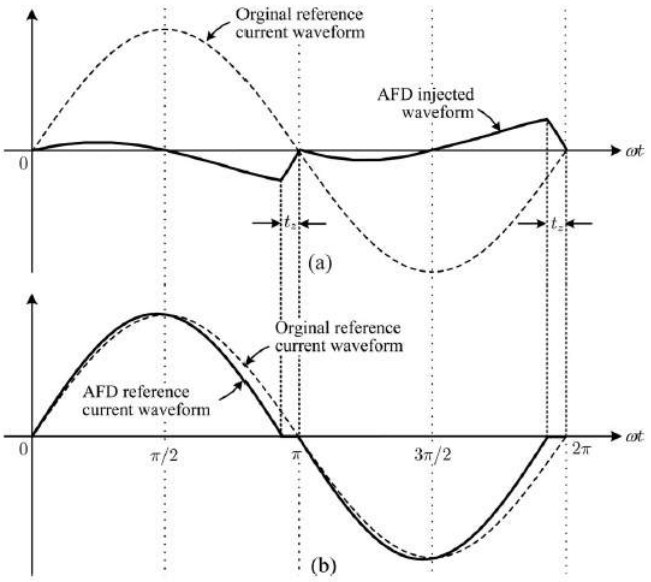

Figure 3.1: AFD method: (a)Original reference current and AFD reference current waveforms. (b) Original reference current and injected current waveforms.[1]

Basically the chopping factor defines the amount of drift introduced to the frequency f. Note that according to Eq 3.1, the greater the t_z, as shown in fig 3.1, the greater the chopping factor , hence larger the perturbation is introduced to the current. In contrast, if $t_z = 0$, from Eq 3.1 c_f is also zero, and the AFD reference current waveform is equal to the original reference current waveform.

Actually, AFD method has a difficulty to detect islanding when the generated reactive power by constant chopping fraction is cancelled by the local load power. This method makes the PV output current to be slightly distorted in order to detect islanding shown as fig 3.2. This method is effective for the resistive loads but has a larger NDZ for some RLC load combinations. To overcome this problem positive feedback AFD methods have been proposed which is explained later in the section.

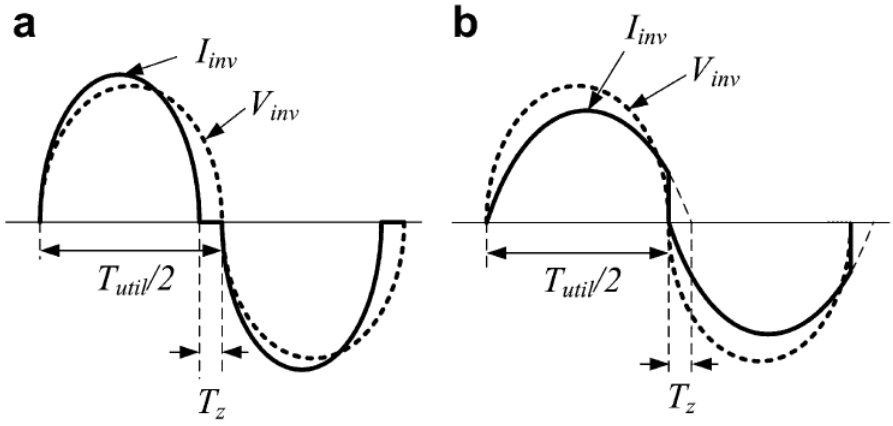

Figure 3.2: Classification of AIMs Voltage and current waveforms with AFD method: (a) positive chopping fraction (b) negative chopping fraction[3]

3.2 AFDPCF (Active Frequency Drift with Pulsation of Chopping Fraction) Method

As a method of overcoming the weaknesses of AFD, a novel AFD scheme, in which pulsation of chopping fraction can deviate the frequency instantly away from nominal. This scheme is referred to as AFD with pulsation of chopping fraction (AFDPCF). It can be modeled as below:[10]

$$c_f = c_{fmax} \text{ if } T_{cfmax\_on}$$

c_{fmin} if T_{cfmax_off}

0 otherwise 3.2

Where, c_{fmax} and c_{fmin} are the maximum and minimum values of c_f respectively. The critical gains of the AFDPCF anti-islanding algorithm are values of c_f and its on-time T_{cf_on}. In order to determine the values of c_f, it is necessary to investigate the characteristic between c_f and current THDi as shown in fig.2.3. The allowable limit of THDi (5%) by the standard, sets an upper/lower limit on the usable value of c_f (i.e. $c_{fmax} = 0.046$, $THDi = 4.88\%$ and $c_{fmim} = -0.045$, $THDi = 4.92\%$). Therefore, THDi of the proposed method is always between 0.9% and 4.92%. The study of NDZ shows that the relationship between power mismatch quantities and the voltage and frequency thresholds is given by:[10]

$$(\frac{V}{V_{max}})^2 - 1 \leq \frac{\Delta P}{P} \leq (\frac{V}{V_{min}})^2 - 1 \tag{3.2}$$

$$Q_f(1 - (\frac{f}{f_{min}})^2) \leq \frac{\Delta Q}{P} \leq Q_f(1 - (\frac{f}{f_{max}})^2) \tag{3.3}$$

According to IEEE Std. 929-2000,$V_{max} = 110\%, V_{min} = 88\%, f_{max} = 60.5Hz, f_{min} = 59.3Hz, Q_f = 2.5$ The above mentioned relationship for the given conditions is as follows:

$$-17.36\% \leq \frac{\Delta P}{P} \leq 29.13\% \tag{3.4}$$

$$-5.94\% \leq \frac{\Delta Q}{P} \leq 4.11\% \tag{3.5}$$

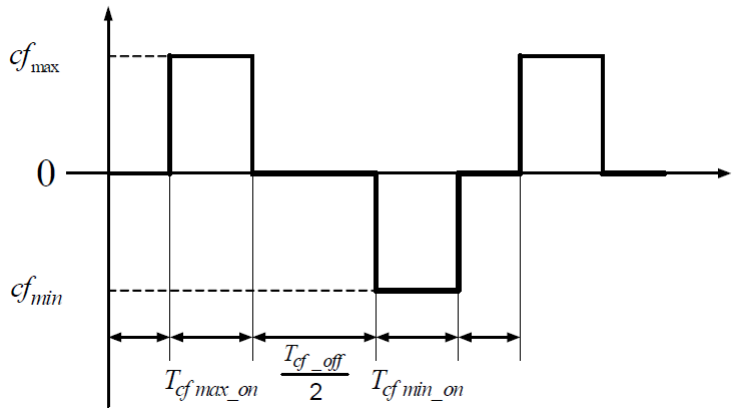

Figure 3.3: Pulsation of chopping fraction[10]

Assuming DPF = 1

$$PF = \frac{P}{S} = \frac{1}{\sqrt{1 + THDi^2}} \tag{3.6}$$

$$\frac{Q}{P} = THDi \tag{3.7}$$

Since AFDPCF perturbs the THDi only, assumed that $\Delta P/P$ is nearly zero. If $\Delta Q/P$ is nearly zero at the moment of islanding situation, the reactive power mismatch by c_{fmax} is

$$\frac{\Delta Q}{P} = 4.88\% \tag{3.8}$$

Therefore, it is out of the range of the Eqn. and AFDPCF can detect the islanding instantly by over frequency relay (OFR) by Eq. 3.1. However, if $\Delta Q/P$ is nearly around low limit (i.e.$\Delta Q/P \approx -5.94\%$) at the moment of islanding situation, the reactive power mismatch by c_{fmax} is

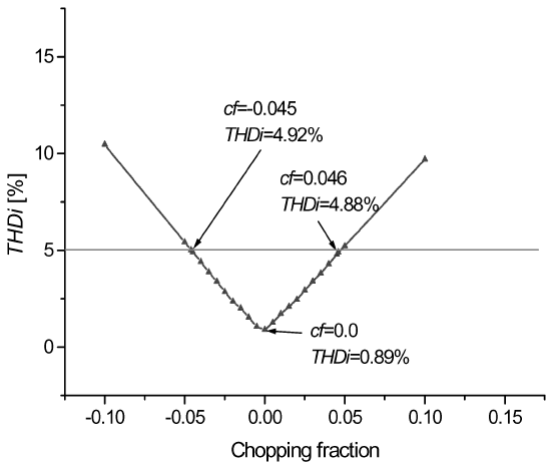

Figure 3.4: Characteristics of THD versus chopping fraction[10]

$$\frac{\Delta Q}{P} = -1.06\% \tag{3.9}$$

It means that the positive pulsation of chopping fraction, which is to increase the frequency, is not sufficient to detect the islanding entirety. Consequently, it is required the negative pulsation of chopping fraction which is to decrease the frequency. For c_{fmin}

$$\frac{\Delta Q}{P} = -10.86\% \tag{3.10}$$

Therefore, it is out of the range of the Eqn. and AFDPCF can detect the islanding instantly by under frequency relay (UFR).

Chapter 4

PROPOSED METHOD

The method proposed for AIM makes the magnitude current reference to be increased to K% higher than nominal value at first line cycle, and then makes that to be decreased to K% lower than the nominal value to the next line cycle.[3] It makes the total average real power from PV to be constant between two consecutive line cycles without affecting the maximum power point tracking (MPPT) function of PV inverter. The operating principle of this scheme can be understood from the flowchart and the operational waveforms given in fig.4.1 and fig.4.2 respectively.

At the start of C_0 cycles, current magnitude is raised by K% for the first cycle and decreased by K% for second cycle. For the next C_1 cycles there is no change in the magnitude of current. Due to this current magnitude variation is employed but average power remains same. Thus power transferred is not affected. If this causes change in the rms value of the voltage beyond a specific threshold, the AFD method is injected and the frequency drift away from normal in case of islanding condition. The AFD injection is removed at the end of C_1 cycles. This maintains the power quality of the inverter when the active signals are not injected.

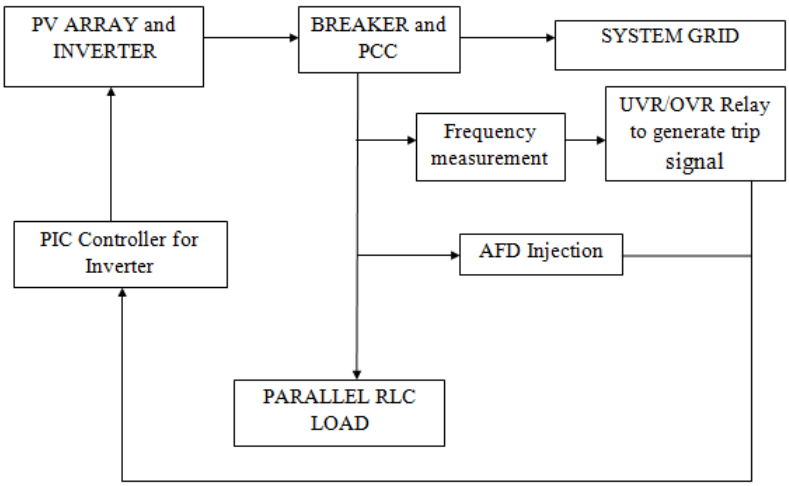

Figure 4.1: Block Diagram of the Proposed Method[3]

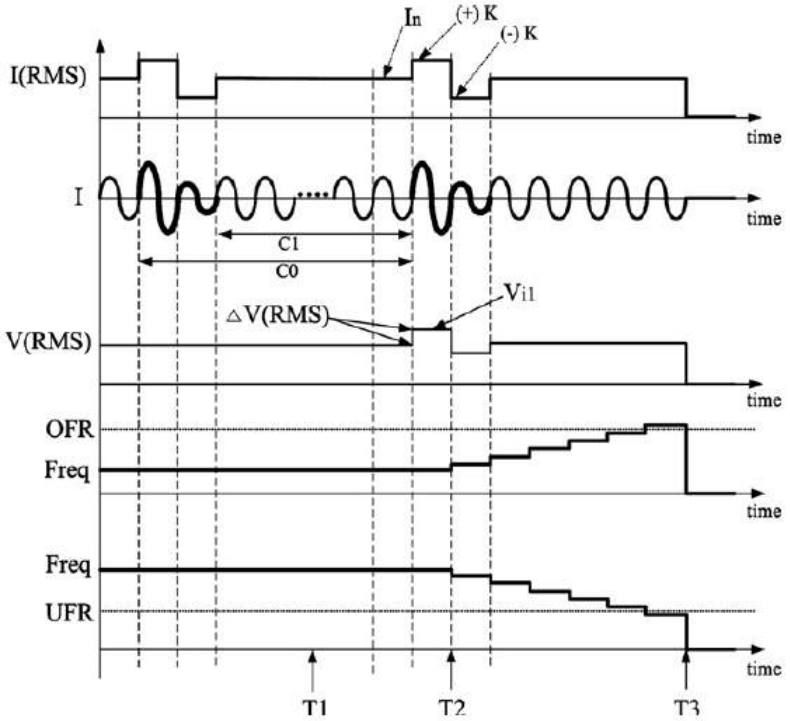

Figure 4.2: Operational waveforms of the proposed method[3]

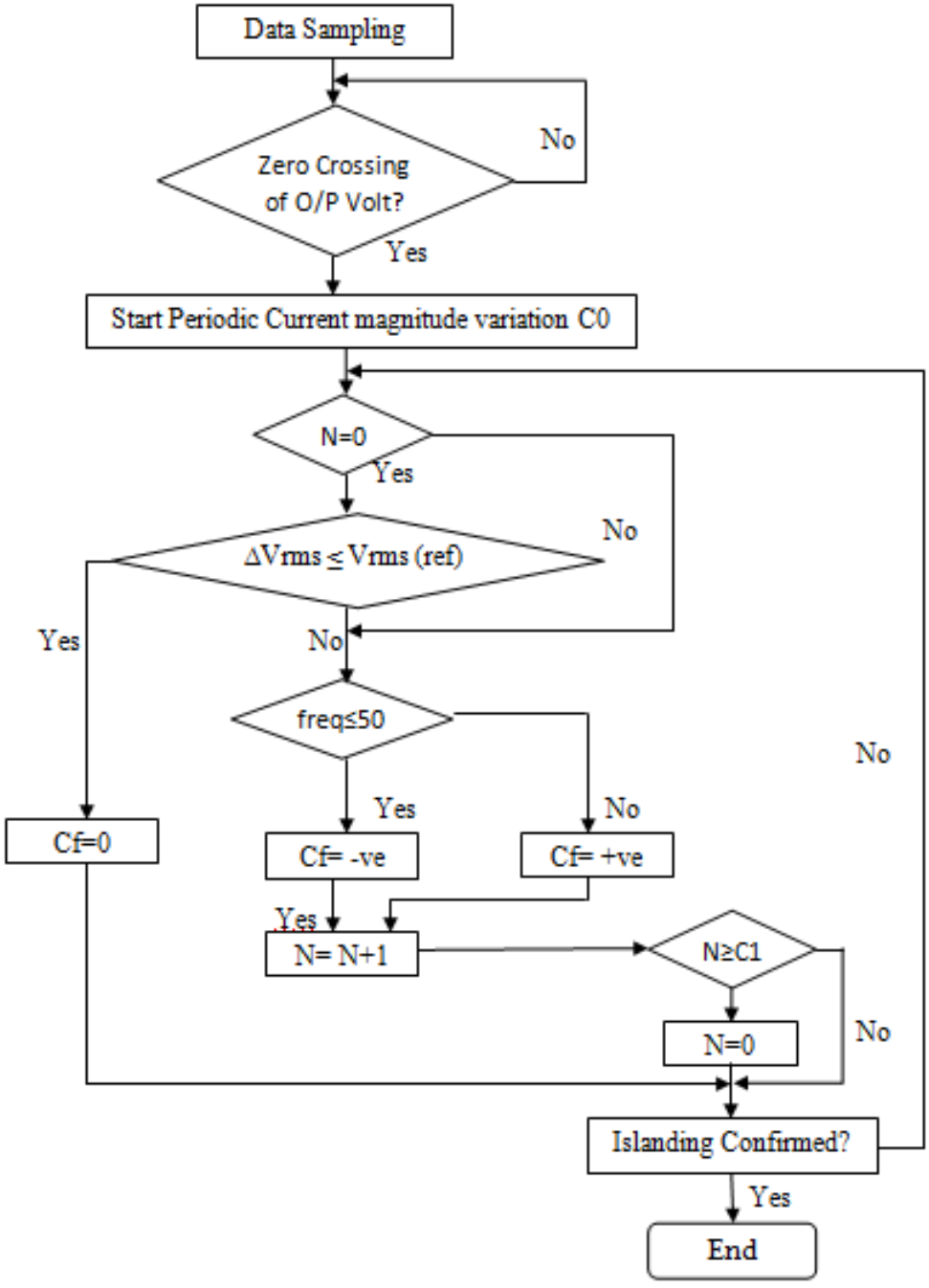

Figure 4.3: Flowchart of the proposed Method

Chapter 5

SIMULATION AND RESULTS

5.1 Circuit, Waveforms and Results

Parameter	Value
Quality Factor (Q_f)	2.5
Voltage (V)	220
Frequency (Hz)	50
K%	12
V(rms),ref (V)	22
Chopping fraction (c_f)%	5
C_0 (cycles)	11
C_1 (cycles)	9
P_{inv} (kW)	3
Local inductive load Q_L (kVar, H)	0.77,0.5
Local Capacitive load Q_C (kVar, nF)	0.77, 50.71

To demonstrate the viability of the AIM method using effective power variation, the simulation of anti-islanding process is tested under the worst case islanding load condition by IEEE Std. 1547. The PV inverter is represented by an H

bridge inverter using unipolar SPWM technique. The frequency monitoring and the generation of PWM pulses is carried out by using dynamic link library (DLL) in PSIM software. Fig.5.1 shows the general circuit diagram and the above table shows the parameters used in the circuit design and the programming of DLL. The 220 V, 50 Hz grid system is modeled by a sinusoidal voltage source.

5.2 Design of RLC Load

The load is designed to have resonant frequency of 50 Hz. The circuit is simulated for unity power factor operation i.e. $Q_i = 0$.[12, 13] The unity power factor combined with the RLC load definition in the following equations, is considered the worst case for islanding detection when active power is 100% matched between load and DG output. As per given values of the parameters in above table we have

Active Power $P_i = 3$ kW

Reactive Power $Q_i = 0$

Quality factor $Q_f = 2.5$

Gird Voltage rms $V_{grid} = 220$ V

Grid Frequency $f = 50$ Hz.

Load Resistance $R_o = \frac{V_{grid}^2}{P_i} = 16.1333336\ \Omega$

Load Inductance $L_o = \frac{V_{grid}^2}{2\pi f Q_f P_i} = 20.54 \times 10^{-3}$ H

Load Capacitance $C_o = \frac{Q_f P_i}{2\pi f V_{grid}^2} = 493.2487 \times 10^{-6}$ F

5.3 Simulation

As shown in the figure the voltage is maintained at 220 V and 50 Hz across the lumped RLC parallel load in the presence of the utility. The simulation results for islanding is discussed. At the t=0.5 sec the utility is disconnected

i.e the breaker is opened. This will create an island resulting some changes in the parameters of the circuit. The resulting waveforms of the circuit voltage, current and frequency are shown in the following figures.

As soon as the breaker opens at 0.5 seconds at 0.522 seconds the variation in the rms value of the load voltage starts and is about 10.16 V. This voltage is within the threshold limits ($88\% < V < 110\%$), thus a passive AIM using OVR/UVR would have not been sufficient. The simulated AIM will vary the magnitude of voltage by K% and under the islanding condition the voltage variation will increase above the threshold level and be visible. As shown in Fig.5.3, the voltage varies by about 29.37 V (13.35%) and it becomes 249.36 V thus the OVR will detect it and generate a tripping signal for the inverter. Thus, the inverter now injects active signal (start of AFD signal) and the frequency drifts out of the trip window of OFR/UFR relays only when an island is formed. This avoids nuisance trip and also help in maintaining the power quality.

The following process takes place:-

- As soon as the breaker opens the frequency at PCC changes at 0.51 sec frequency deviates from 47.58 Hz which is under the preset frequency window of 53-47 Hz. Now at 0.6801 sec AFD is injected and becomes 51 Hz.
- This condition generates a trip signal at 0.6920 sec and the frequency drops to 42 Hz. As the frequency goes outside the trip window of 47-53 Hz, hence the production of reference signal is stopped and the inverter voltage starts dropping to zero. This phenomenon is shown in the fig. 5.5, 5.6 and fig.5.7.
- As shown in the fig. 5.5, the AFD injection start signal goes to high when the rms value of the voltage crosses the set value of 22 V.
- Due to the injection of active signal and the presence of islanding condition the voltage of the system rises to 249.36 V which is beyond the threshold value of 242 V. Frequency of the load voltage rises upto 137.74 Hz.

- For the above condition of islanding the time at which the AFD signal is injected is 0.6801 sec.
- The Trip signal is generated at 0.6920 sec.
- At that instant at the output voltage starts decreasing and becomes zero. The inverter gating pulses cease and inverter turns off.
- Thus, the total time taken to detect islanding is 0.0119 sec. This time is within the permissible limit set by the IEEE standard 1547 of 2 seconds.

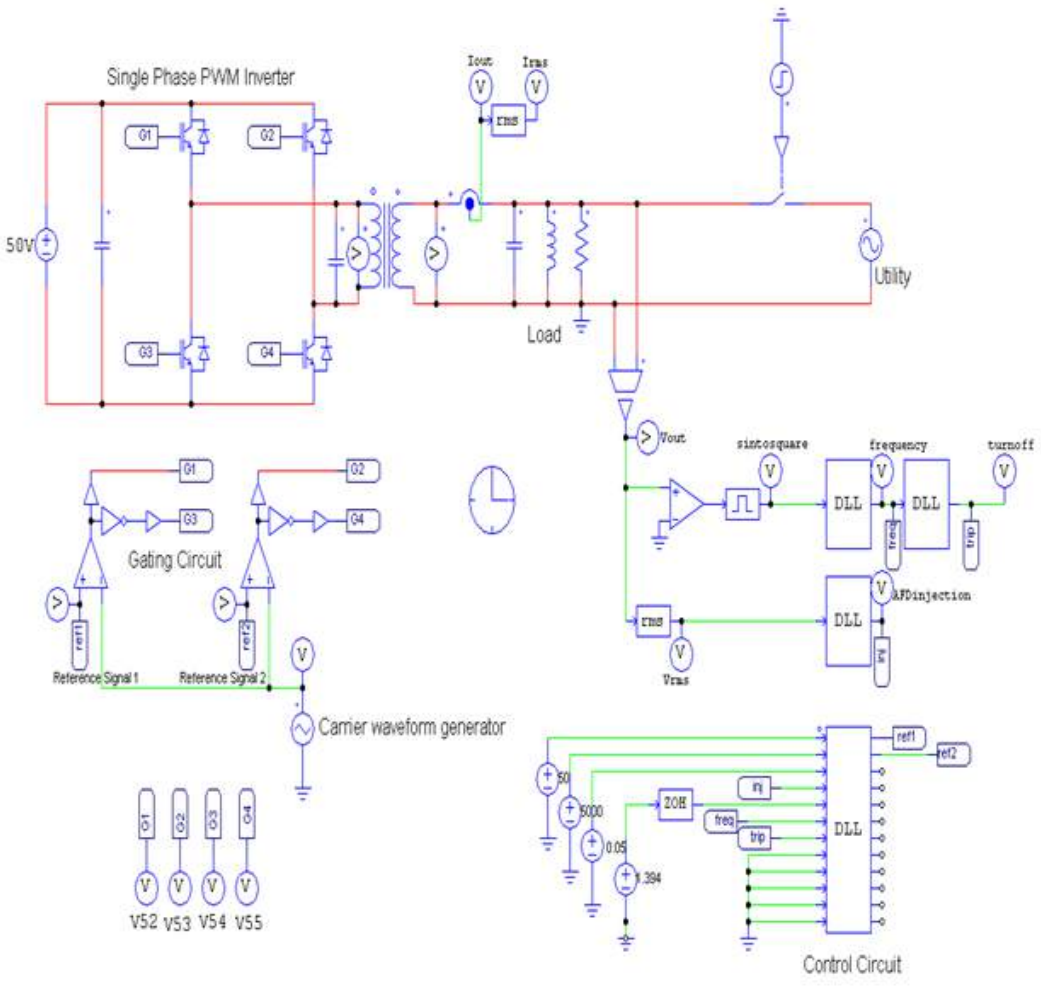

Figure 5.1: Simulation Circuit

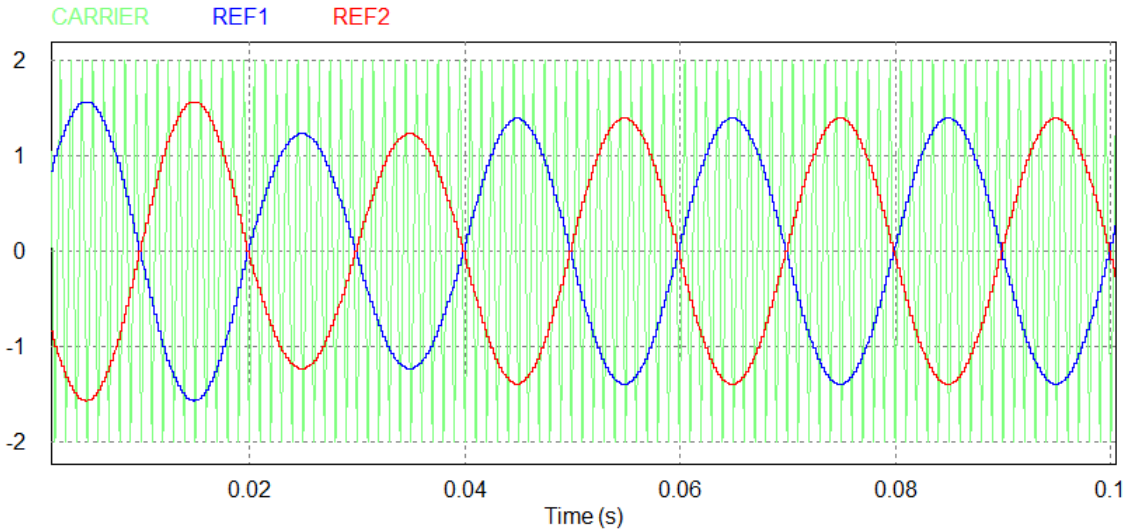

Figure 5.2: Generation of reference and carrier waveforms
X axis: 0.02 sec/div : Y axis: 1V/div

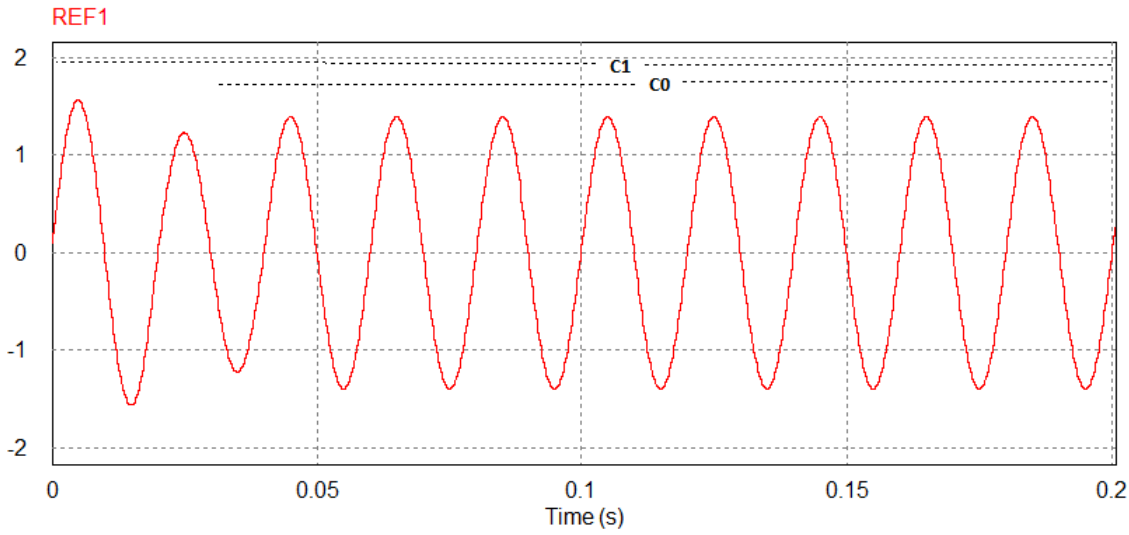

Figure 5.3: Variation by K%
X axis: 0.05 sec/div : Y axis:1 V/div

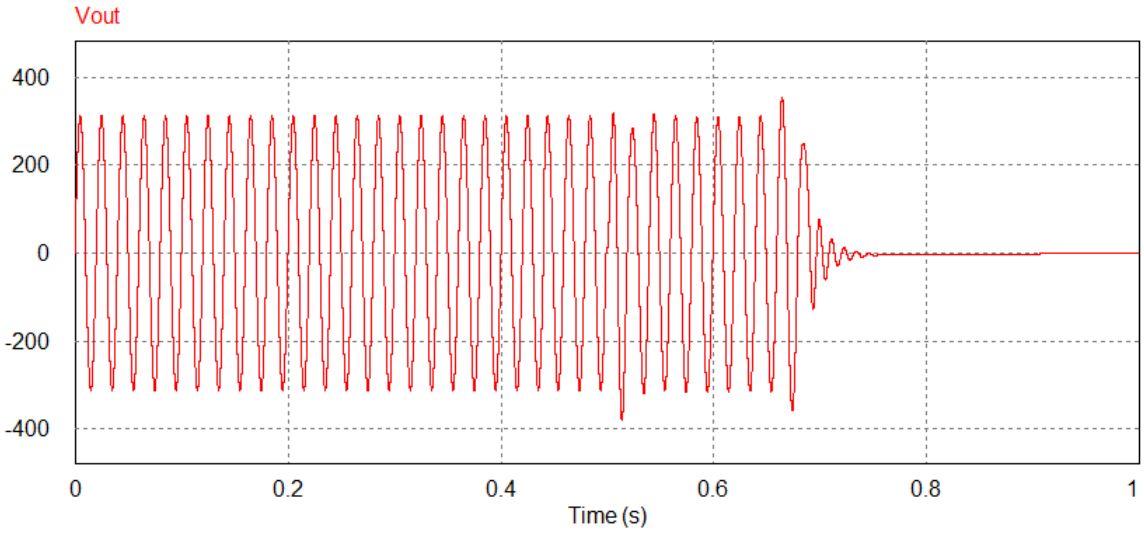

Figure 5.4: Output voltage (Volts)
X axis: 0.2 sec/div : Y axis: 200 V/div

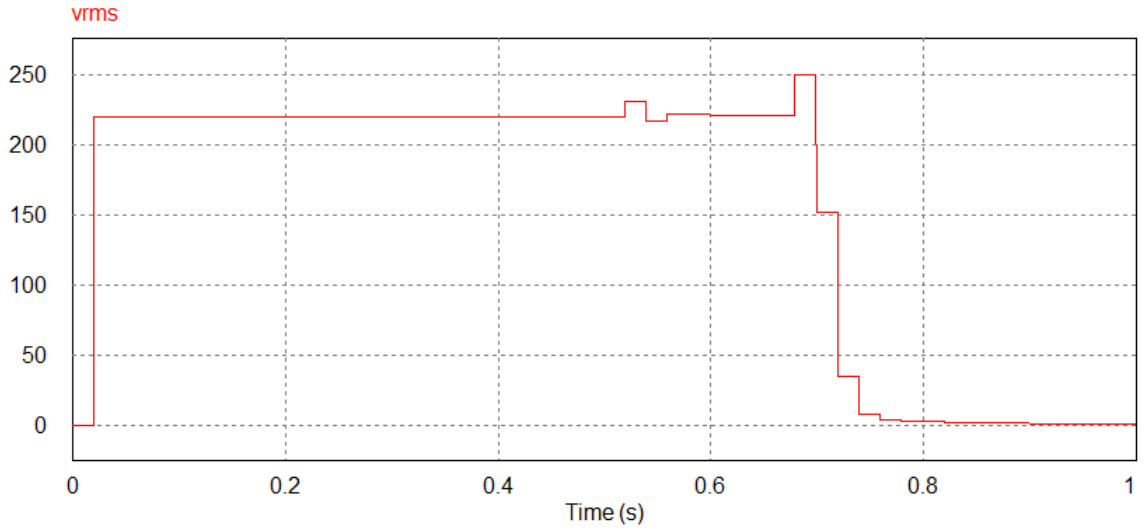

Figure 5.5: RMS value of Output voltage (Volts)
X axis: 0.2 sec/div : Y axis: 50 V/div

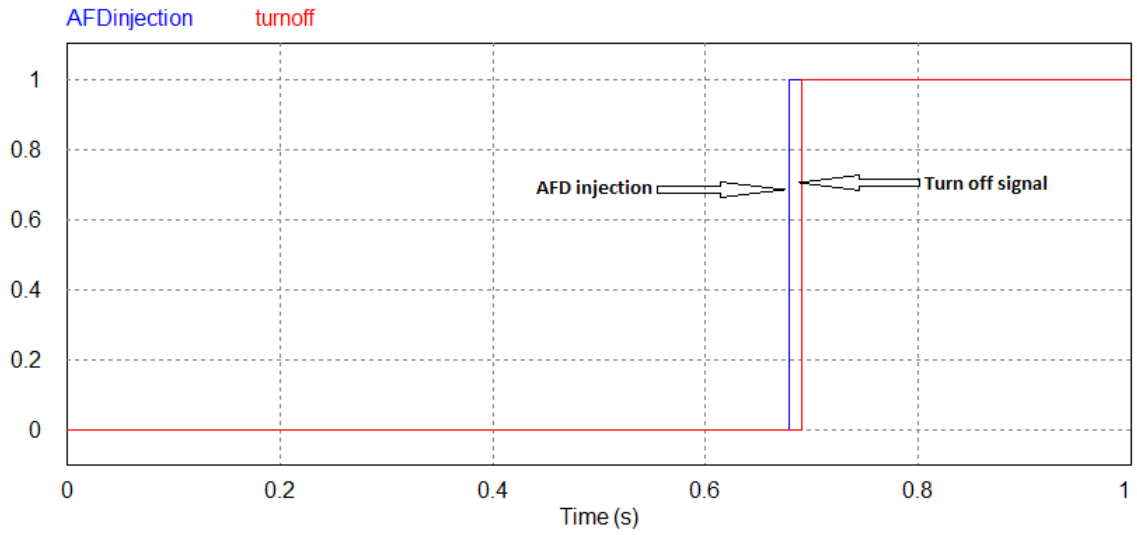

Figure 5.6: AFD signal injection signal and Trip signal
X axis: 0.2 sec/div : Y axis: 0.2 V/div

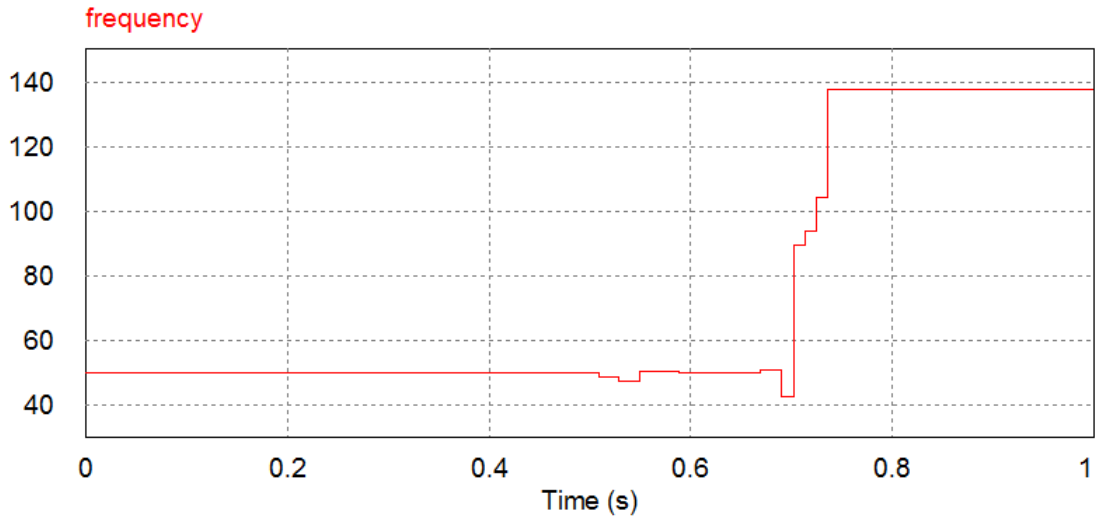

Figure 5.7: Change in Frequency (Hz)
X axis: 0.2 sec/div : Y axis: 40 Hz/div

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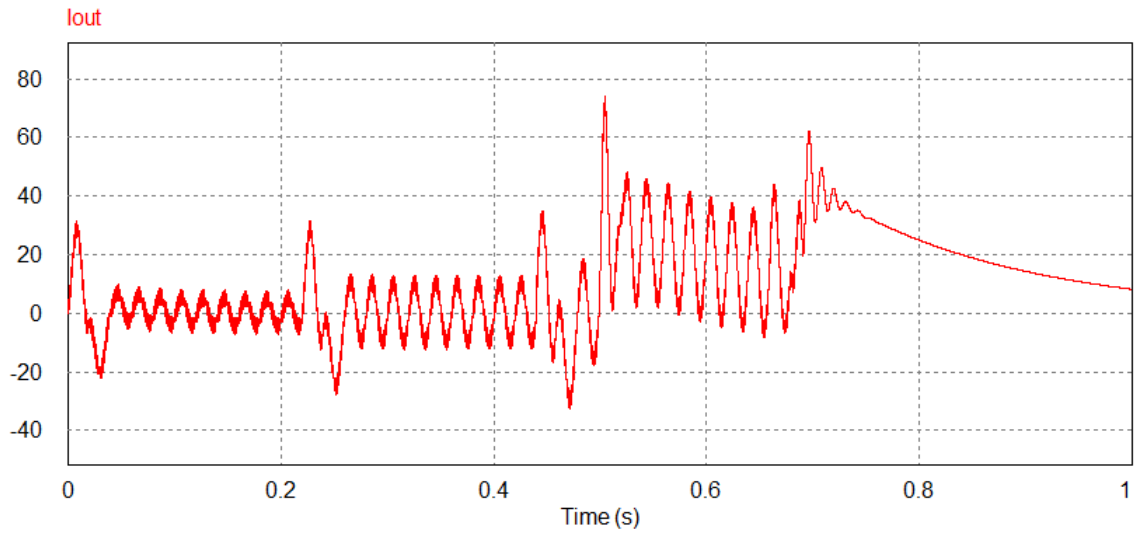

Figure 5.8: Output Current (A)
X axis: 0.2 sec/div : Y axis: 20 A/div

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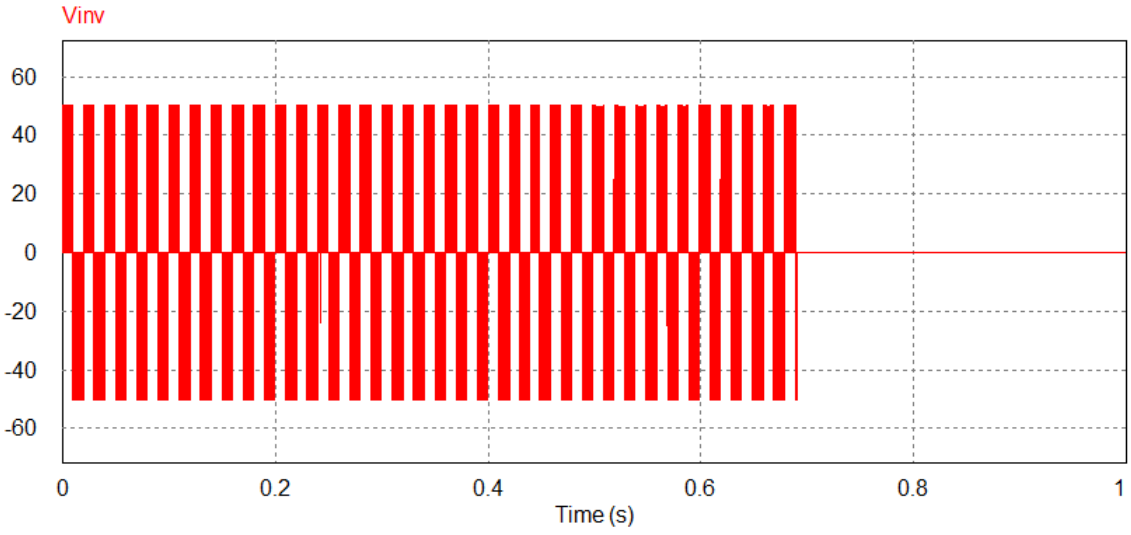

Figure 5.9: Inverter Output Voltage (Volts)
X axis: 0.2 sec/div : Y axis: 20 V/div

Chapter 6

HARDWARE AND RESULTS

The whole hardware setup is divided into different sub parts. Each subpart needs its own power supply, for which separate power supply circuits are made. The regulated +5 V, +12 V and +15 V supply is made for microcontroller, various IC's and drivers of all IGBT's are made using 7805, 7812 and 7915 IC's. The drivers of higher side and lower side of IGBT's are given isolated dc supply.

A power supply and gate driver circuit is needed for each of the four MOSFETs used in the H bridge inverter. When utilizing N channel MOSFETs (used over P channel MOSFETs for better efficiency and reduced power loss)to switch DC voltage across a load, the drain terminals of high side MOSFETs are often connected to the highest voltage in the system. This creates a difficulty, as the gate terminal must be approximately 10 V higher than the drain terminal for the MOSFET drivers are utilized to acheive this difference through charge pumps or booststrapping techniques. These chips are capable of quickly charging the input capacitance of the MOSFET before the potential difference is reached, causing the gate to source voltage to be highest system voltage plus capacitor voltage, allowing it to conduct. Recently MOSFET/IGBT gate drivers like TLP250 are available which can drive both P and N channel as well as higher and lower MOSFETs independently.

6.1 TLP250 Gate Driver Coupler

TLP 250 is a photocoupler IC can dorectly drive medium power IGBT and power MOSFETs. As shown in schematic fig 6.1 there is a LED and integrated photocoupler. The input of the photocoupler is given to the bases of the two complementary transistors Tr_1 (NPN) and Tr_2 (PNP) connected as a class B push-pull power amplifier.

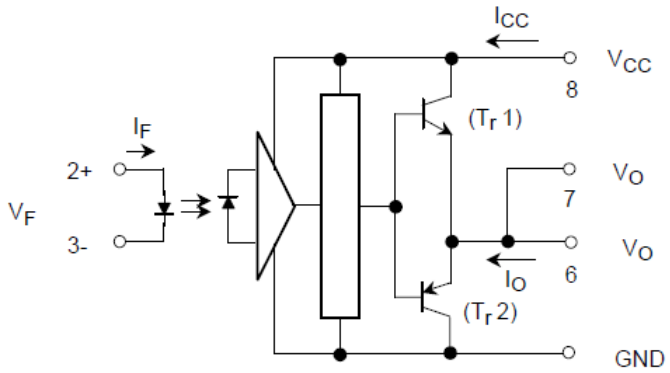

Figure 6.1: Schematic of TLP250

6.2 Dead Band Generation Circuit

Dead time generator is required to provide a delay of few microseconds in rising time of switching pulses. Logic for Dead time generator and schematic diagram of dead time generator circuit, which has been used, is shown in figure 6.2 and figure 6.3 respectively. The dead band of 10μsecond is obtained

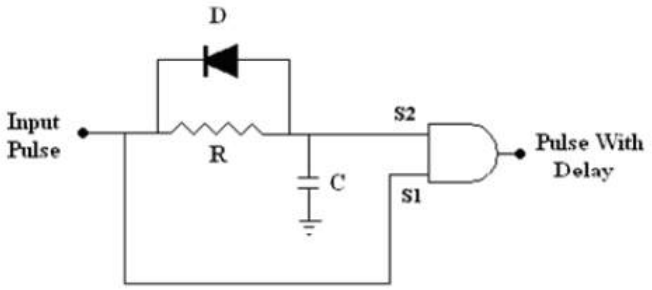

Figure 6.2: Logic of Dead Time Generator

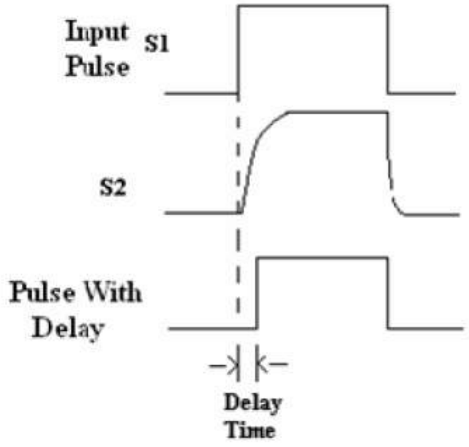

Figure 6.3: Waveform of a Dead Time Generator

6.3 Sine-Triangle PWM Using High Speed Voltage Comparator

The LM710 series are high speed voltage comparators intended for use as an accurate, low level sensor or as a replacement for operational amplifier in comparator applications where speed is of prime importance. The circuit has differential input and a single ended output, with saturated output levels compatible with practically all types of integrated logic. In this case we are giving sine wave to the non-inverting terminal and triangle at inverting terminal. Dual biasing

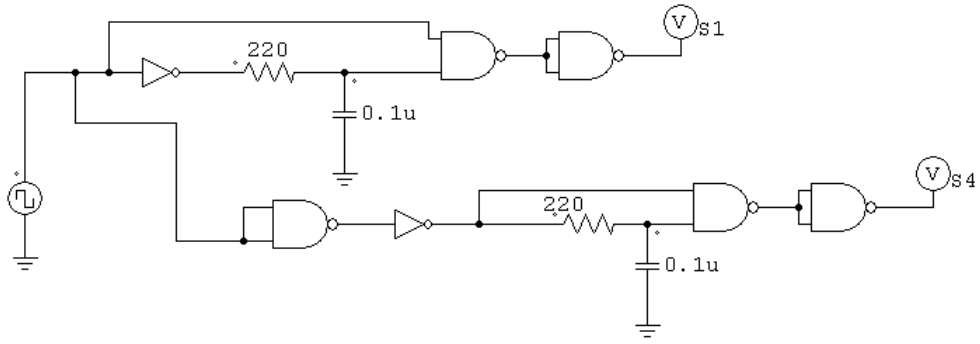

Figure 6.4: Schematic Diagram of a Dead Time Generator

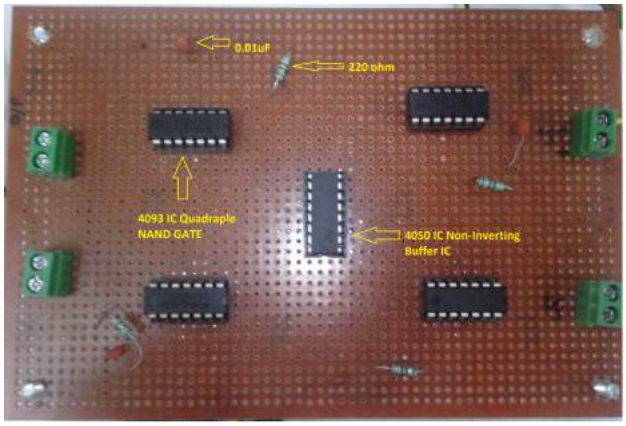

Figure 6.5: Dead Time Generator Circuit

of +12 V and −6 V is provided to the IC. The triangular frequency is kept 1KHz and sine of 50Hz.

The output waveforms of the gate driver circuit is obtained for a single leg of the inverter. Along with the dead band genarated the output pulses of 15 V are generated from TLP250 output which will be required for the turning ON the MOSFETs used in the H bridge inverter. The results are shown as follows.

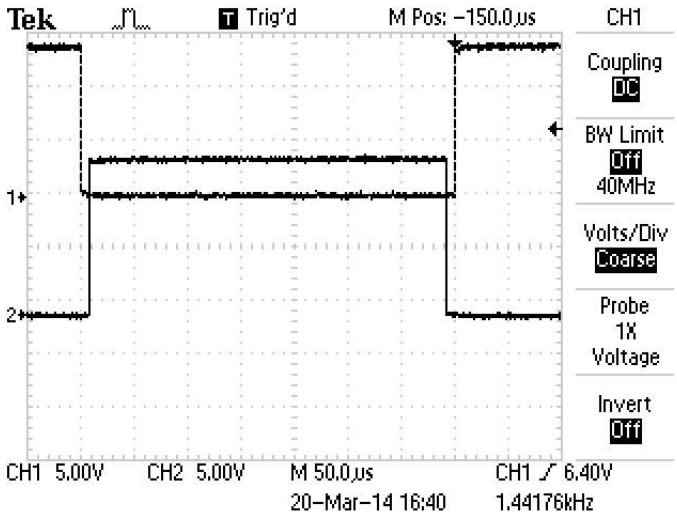

Figure 6.6: Output Waveforms of a Dead Time Generator Circuit
Channel 1: Deadband output 1 Channel 2: Deadband output 1 inverted
X axis: 50μsec/div : Y axis: 5 V/div

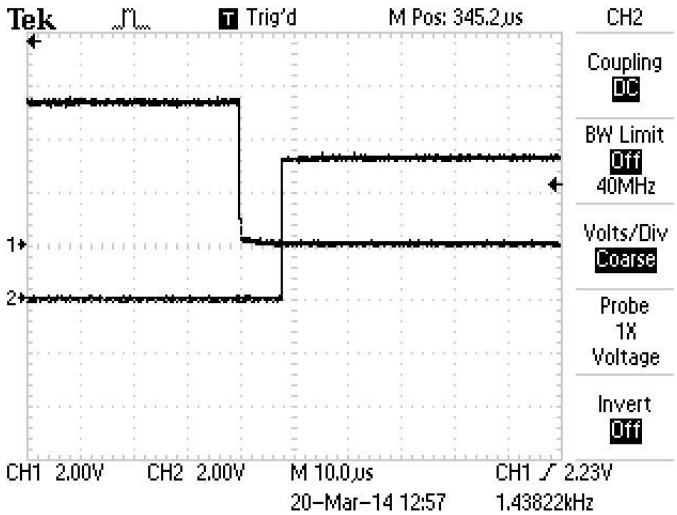

Figure 6.7: Dead Time of 8μsec measured
Channel 1: Deadband output 1 Channel 2: Deadband output 1 inverted
X axis: 10μsec/div : Y axis: 2 V/div

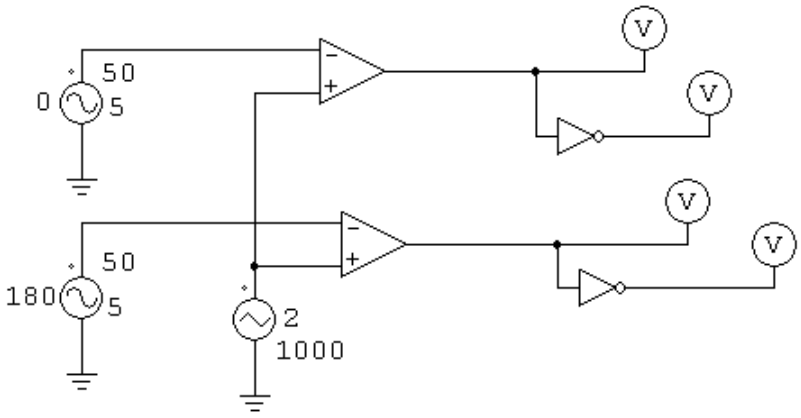

Figure 6.8: Scematics of a comparator circuit

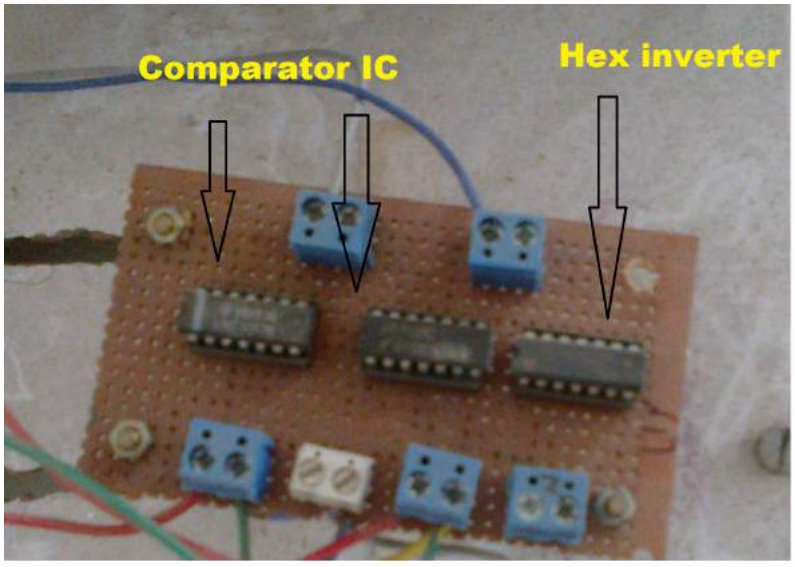

Figure 6.9: Comparator circuit

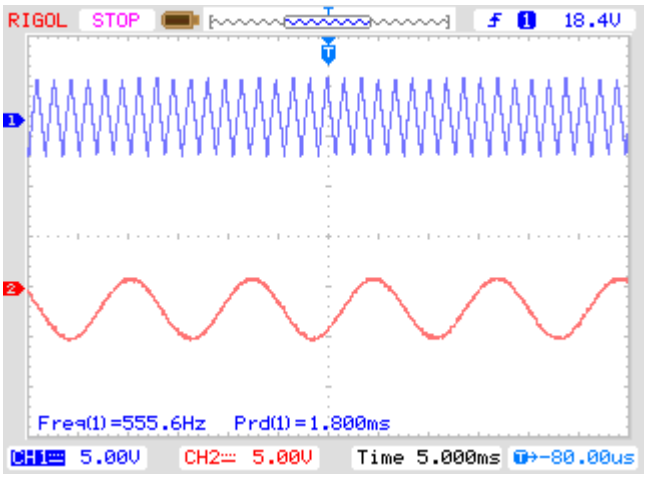

Figure 6.10: Sine and trianglular waveforms of a comparator circuit input
Channel 1: Triangular Waveform 1kHz Channel 2: Sine Wave 50Hz
X axis: 5 msec/div : Y axis: 5 V/div

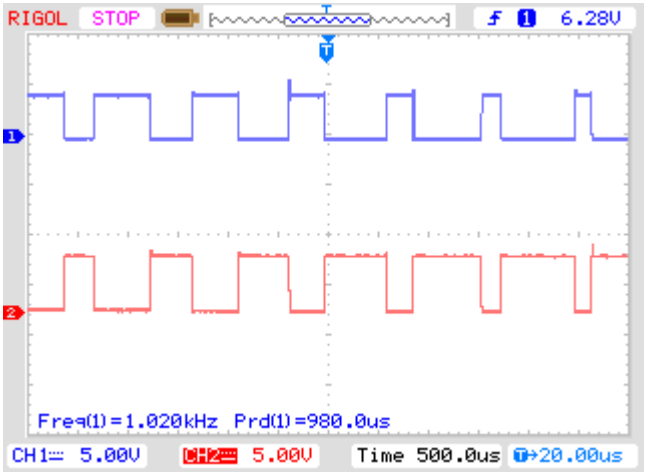

Figure 6.11: Output waveforms of a comparator circuit
Channel 1: Inverter Switch 1 Pulses Channel 2: Inverter Switch 4 Pulses
X axis: 500μsec/div : Y axis: 5 V/div

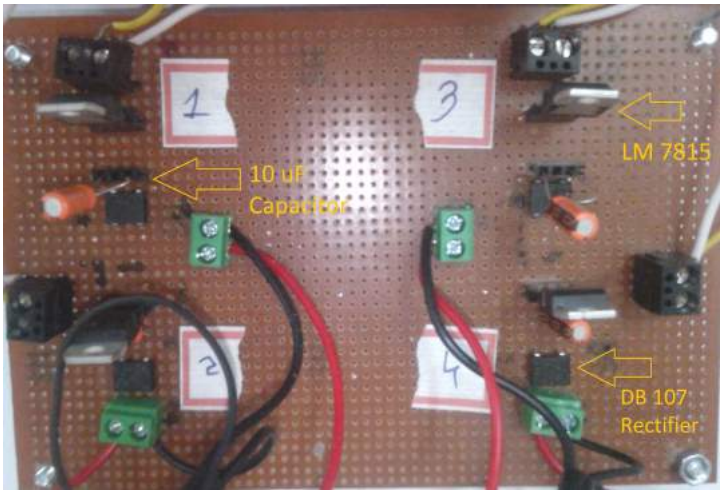

Figure 6.12: Power Suupply for Gate Driver Circuit

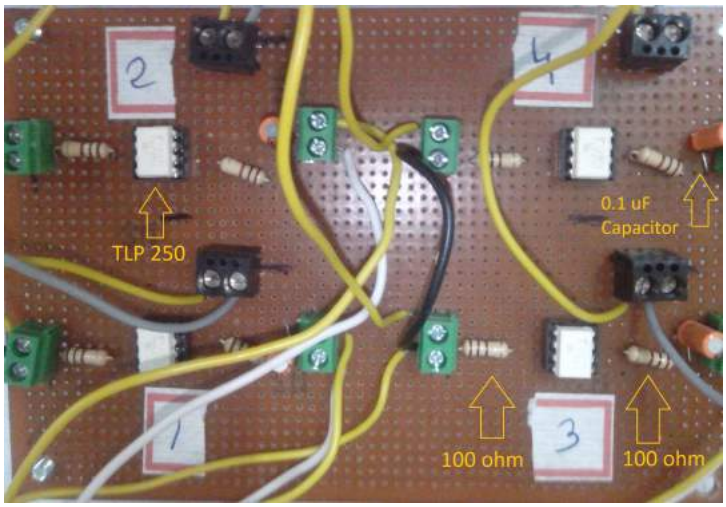

Figure 6.13: Gate Driver circuit

Figure 6.14: H Bridge using MOSFET

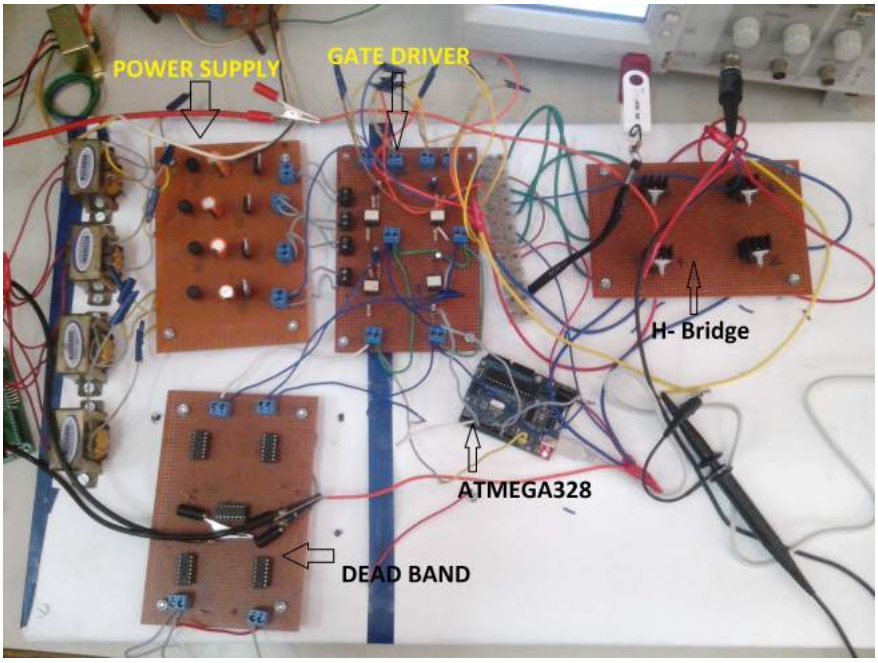

Figure 6.15: Full Experimental Setup

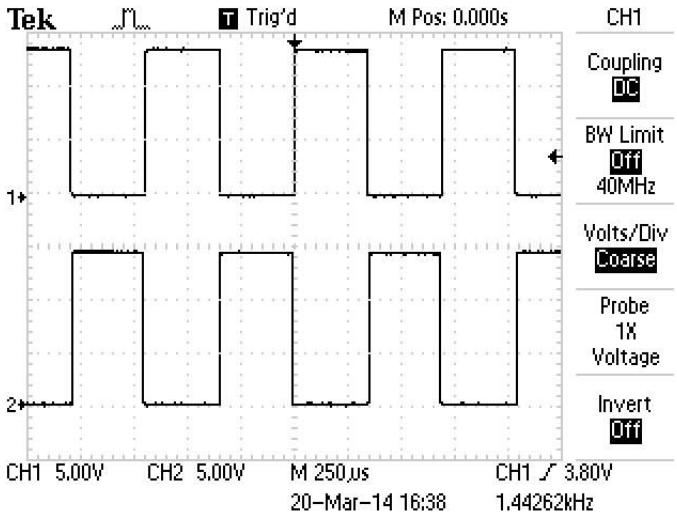

Figure 6.16: Output waveforms of gate driver for same leg of inverter
Channel 1: Switch 1 Pusles Channel 2: Switch 4 Pulses
X axis: 250μsec/div : Y axis: 5 V/div

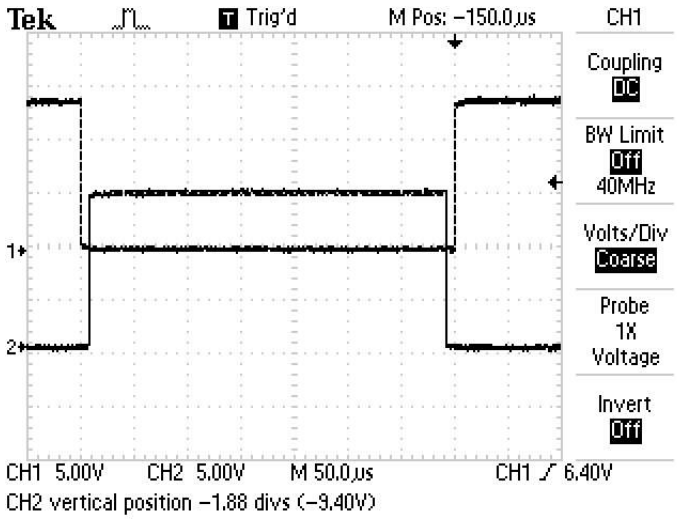

Figure 6.17: Output waveforms of TLP for same leg of inverter with deadband
Channel 1: TLP output 1 Channel 2: TLP output 4
X axis: 50μsec/div : Y axis: 5 V/div

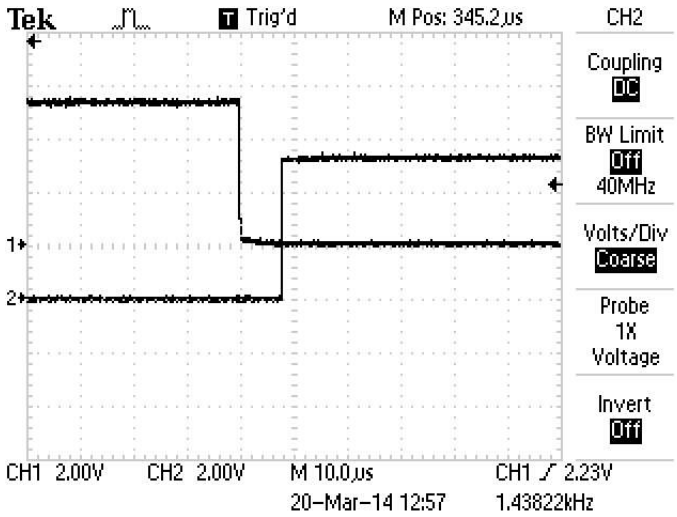

Figure 6.18: Output waveforms of TLP Showing deadband of 8μsec
Channel 1: TLP output 1 Channel 2: TLP output 4
X axis: 10μsec/div : Y axis: 2 V/div

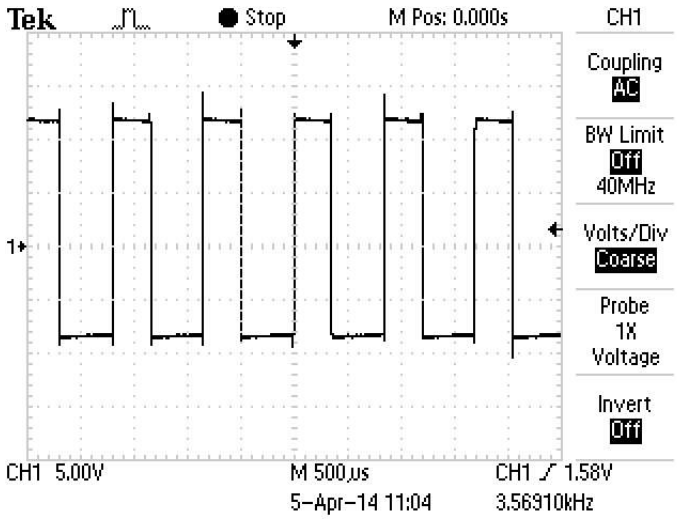

Figure 6.19: Inverter output waveform
Channel 1: Inverter output Waveform
X axis: 500μsec/div : Y axis: 5 V/div

Chapter 7

Arduino Uno Microcontroller Board using ATmega328

7.1 Arduino Microcontroller Board with ATmega328 Microcontroller

Arduino can sense the environment by receiving input from a variety of sensors and can affect its surroundings by controlling lights, motors, and other actuators. The microcontroller on the board is programmed using the Arduino programming language (based on Wiring) and the Arduino development environment (based on Processing). Arduino projects can be stand-alone or they can communicate with software running on a computer (e.g. Flash, Processing, MaxMSP).

The Arduino Uno is a microcontroller board based on the ATmega328. It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button.

The Uno differs from all preceding boards in that it does not use the FTDI

USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter.

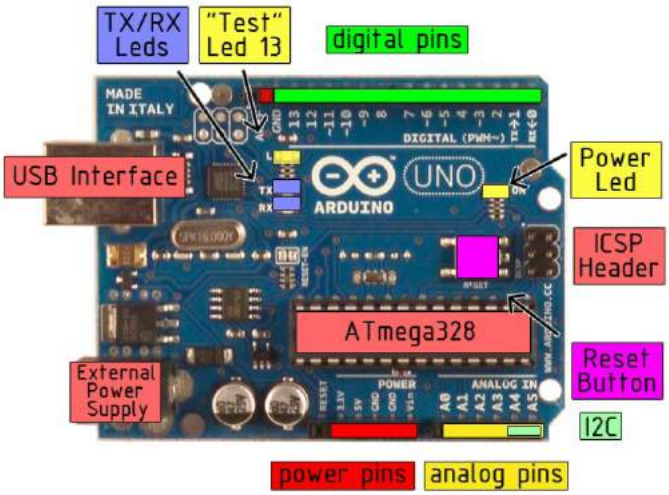

Figure 7.1: Lay Out of Arduino Uno Board

"Uno" means one in Italian and is named to mark the upcoming release of Arduino 1.0. The Uno and version 1.0 will be the reference versions of Arduno, moving forward. The Uno is the latest in a series of USB Arduino boards, and the reference model for the Arduino platform

7.1.1 Device Overview

7.1.2 Technical Specifications

- Microcontroller : ATmega328
- Operating Voltage : 5V
- Input Voltage (recommended) : 7-12V
- Input Voltage (limits) : 6-20V
- Digital I/O Pins : 14 (of which 6 provide PWM output)
- Analog Input Pins : 6

- DC Current per I/O Pin : 40 mA
- DC Current for 3.3V Pin : 50 mA
- Flash Memory : 32 KB of which 0.5 KB used by bootloader
- SRAM : 2 KB
- EEPROM : 1 KB
- Clock Speed : 16 MHz

7.1.3 Power

The Arduino Uno can be powered via the USB connection or with an external power supply. The power source is selected automatically.

External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The power pins are as follows:

- **VIN** : The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.
- **5V** : The regulated power supply used to power the microcontroller and other components on the board. This can come either from VIN via an on-board regulator, or be supplied by USB or another regulated 5V supply.

- **3V3** : A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.
- **GND**: Ground pins.

7.1.4 Memory

The Atmega328 has 32 KB of flash memory for storing code (of which 0,5 KB is used for the bootloader); It has also 2 KB of SRAM and 1 KB of EEPROM .

7.1.5 Input And Output

Each of the 14 digital pins on the Uno can be used as an input or output, using pinMode(), digitalWrite(), and digital Read() functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial:** 0 (RX) and 1 (TX) : Used to receive (RX) and transmit (TX) TTL serial data. TThese pins are connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip .
- **External Interrupts:** 2 and 3 :These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value.
- **PWM**: 3, 5, 6, 9, 10, and 11. Provide 8-bit PWM output with the analog-Write() function.
- **SPI:** 10 (SS), 11 (MOSI), 12 (MISO), 13 (SCK) : These pins support SPI communication, which, although provided by the underlying hardware, is not currently included in the Arduino language.
- **LED: 13 :** There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

The Uno has 6 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the AREF pin and the analog Reference() function. Additionally, some pins have specialized functionality

- **I2C: 4 (SDA) and 5 (SCL)** : Support I2C (TWI) communication using the Wire library.

There are a couple of other pins on the board:

- **AREF** : Reference voltage for the analog inputs. Used with analogReference().
- **Reset :** Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

7.1.6 Communication

The Arduino Uno has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega328 provides UART TTL (5V) serial communication, which is available on digital pins 0 (RX) and 1 (TX). An ATmega8U2 on the board channels this serial communication over USB and appears as a virtual com port to software on the computer. The 8U2 firmware uses the standard USB COM drivers, and no external driver is needed. However, on Windows, an *.inf file is required.

The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the Arduino board. The RX and TX LEDs on the board will flash when data is being transmitted via the USB-to serial chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A Software Serial library allose for serial communication on any of the Uno's digital pins. The ATmega328 also support I2C (TWI) and SPI communication.

7.1.7 Programming

The Arduino Uno can be programmed with the Arduino software . Select "Arduino Uno w/ ATmega328" from the **Tools** > **Board** menu . For details see the reference and tutorials.

The ATmega328 on the Arduino Uno comes preburned with a bootloader that allows to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol (reference, C header files).

Bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header. The ATmega8U2 firmware source code is available . The ATmega8U2 is loaded with a DFU bootloader, which can be activated by connecting the solder jumper on the back of the board and then resetting the 8U2.

7.1.8 Automatic (Software) Reset:

Rather than requiring a physical press of the reset button before an upload, the Arduino Uno is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2 is connected to the reset line of the ATmega328 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.

This setup has other implications. When the Uno is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Uno. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.

The Uno contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN".

7.1.9 USB Overcurrent Protection

The Arduino Uno has a resettable polyfuse that protects your computer's USB ports from shorts and over current. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

7.1.10 Physical Characteristics

The maximum length and width of the Uno PCB are 2.7 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Three screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16"), not an even multiple of the 100 mil spacing of the other pins.

7.2 Inverter Programmig

A program to compare the sine-triangle wave in Arduino is as follow. In this program,the sine wave has assigned 50Hz frequency. AnalogRead command reads the value from the voltage sensor by analog pin A0, returning a range from 0 to 1023. Digital-Write command writes a digital value to a pin can be any value between 0 and 255. Then sine wave and triangular mathematical function is created in the programme. If magnitude of the sine wave is greater than the magnitude of the triangular wave it shows pin no.6 and pin no.11 in HIGH state otherwise it is in LOW state. If magnitude of the triangular wave is greater than the magnitude of the sine wave it shows pin no.3 and pin no.5 in HIGH state otherwise it is in LOW state while the triangle wave has assigned 1kHz frequency. Figure 7.2 shows the output PWM pulses for two legs (four switches) of inverter (Two are same and two are complementry). Figure 7.3 shows the deadband between two switches of opposite legs.

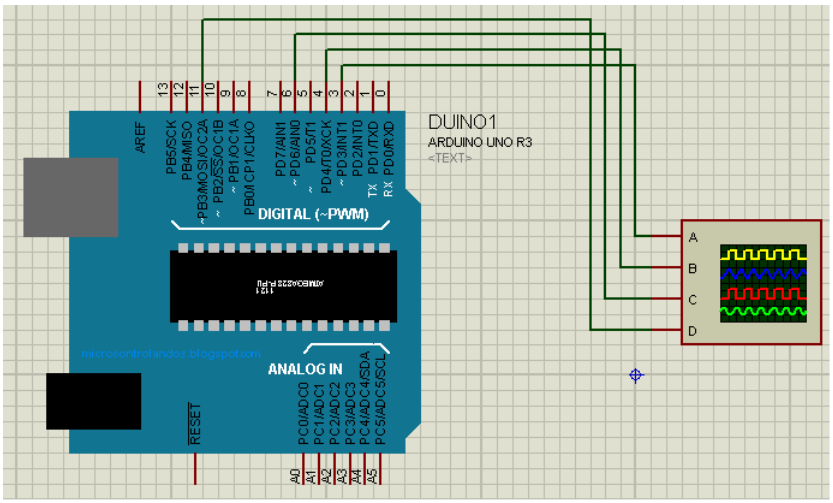

Figure 7.2: Arduino schematic simulation circuit in Proteas

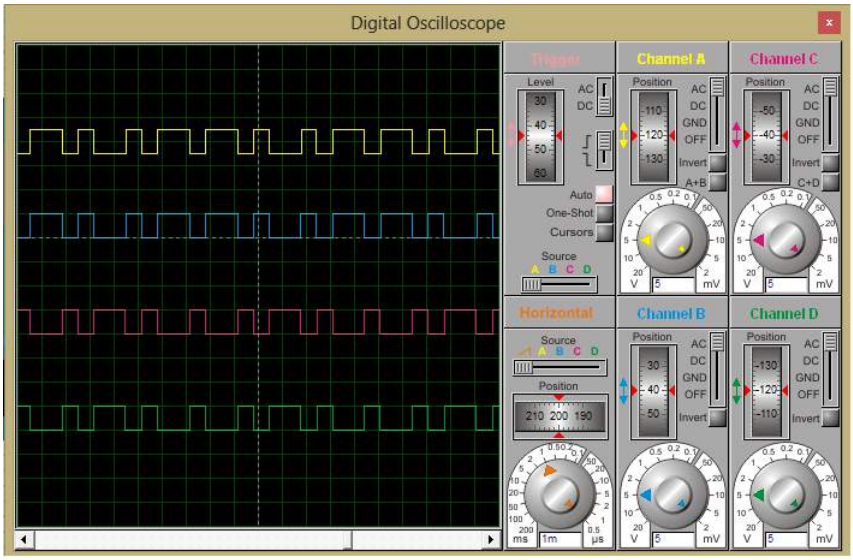

Figure 7.3: Gating pulses generated by Arduino

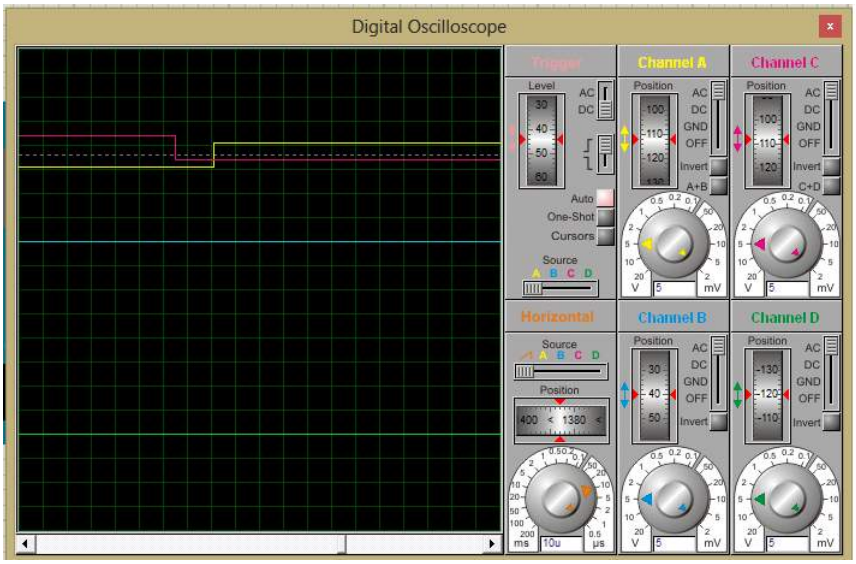

Figure 7.4: Gating pulses generated by Arduino with dead band

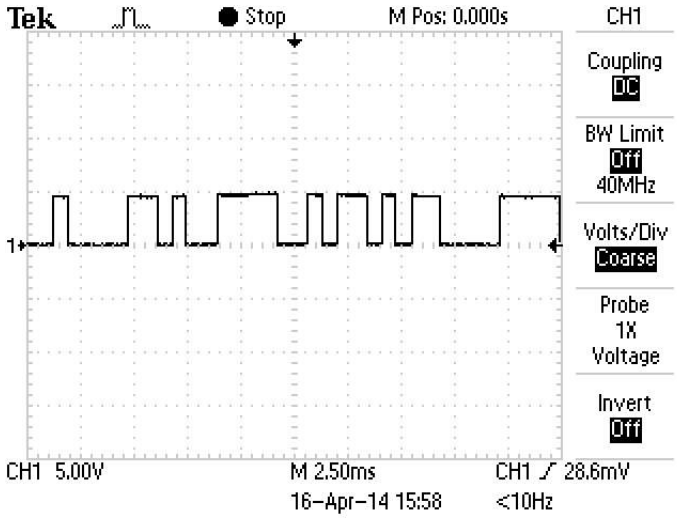

Figure 7.5: Gating pulses generated by Arduino for inverter
Channel 1: Arduino pulses for one switch
X axis: 2.50 msec/div : Y axis: 5 V/div

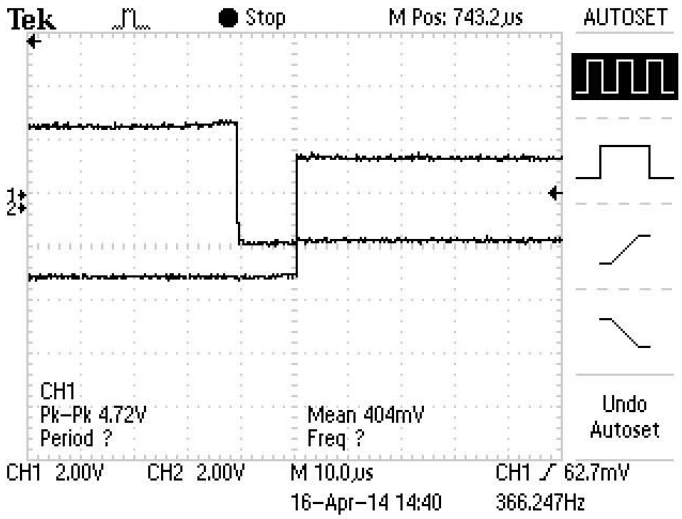

Figure 7.6: Gating pulses generated by Arduino for same leg of inverter with dead band 10μsec
Channel 1: Arduino pulses switch 1 : Channel 2: Arduino Pulses for Switch 4
X axis: 10μsec/div : Y axis: 2 V/div

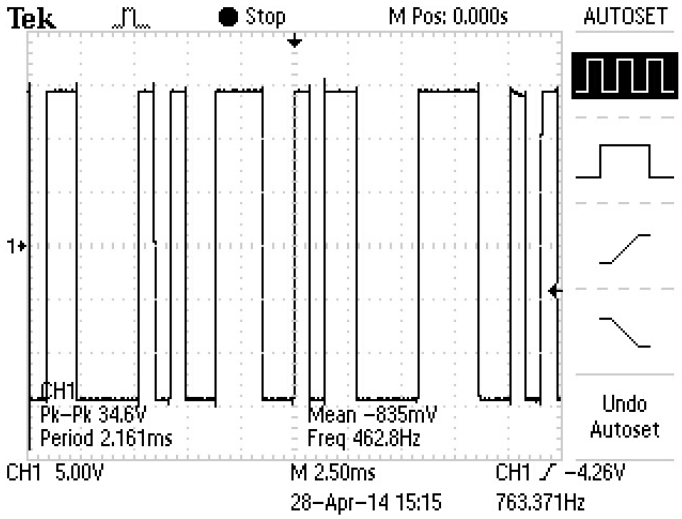

Figure 7.7: Inverter output waveform operated by Arduino
Channel 1: Inverter Output
X axis: 2.50 msec/div : Y axis: 5 V/div

Chapter 8

CONCLUSION AND FUTURE SCOPE

A high power quality AIM was simulated for the worst case islanding condition. The proposed inverter topology for the anti-islanding method is been developed in PSIM. The proposed scheme uses the combination of AFD method and periodic current magnitude variation method. The inverter control senses the variation in output voltage and it starts injection of AFD signal to the inverter which is further amplified above the tripping window. And the inverter trips within time. The results in terms of detecting the islanding and the time taken for it are found to be 0.011 seconds which is under the requirements of the IEEE std. 1547. The AIM is able to detect the islanding in its worst case within 2 seconds. The power quality of the output is within the limits. The developed AIM has less NDZ and upon making improvements they can be eliminated further to some extent. The THD of output current was also found to be 4.8% which is with the limits of 5%. All anti-islanding techniques including the developed AIM have few limitations and till date no perfect AIM has been developed.

The hardware setup has been fabricated with TLP250 as gate driver and MOSFETs as the inverter switches and tested with their operational results sucess-

fully. The power testing of the H Bridge was completed sucessfully using ATmega328 microcontroller and the SPWM operation was sucessfully completed.

The proposed method of AIM for the developed converter topology of AFD can be implemented on hardware using ATmega328. The algorithm may run on actual hardware setup with using proper sensors. The results obtained from the hardware may be compared with the simulated results and the effectiveness of the developed circuit can be verified.

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