"IMPLEMENTATION OF 3-LEVEL ACTIVE SHUNT POWER FILTER USING CONVENTIONAL HYSTERESIS CONTROLLER"

Major Project Report

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For The Degree Of

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IN

ELECTRICAL ENGINEERING

(Power Electronics, Machines and Drives)

By

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I **Naveen H. Patelia**, Roll No. **12MEEP19**, give undertaking that the Major Project entitled **"Implementation Of 3-Level Active Shunt Power Filter Using Conventional Hysteresis Controller"** submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Power Electronics Machines** & **Drives, Electrical Engineering**, under Institute of Technology of Nirma University, Ahmedabad, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

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This is to certify that the Major Project Report entitled **"Implementation Of 3-Level Active Shunt Power Filter Using Conventional Hysteresis Controller"** submitted by **Mr. Naveen H. Patelia (12MEEP19)** towards the partial fulfillment of the requirements for the award of degree in **Master of Technology (Electrical Engineering)** in the field of **Power Electronics, Machines & Drives** of Nirma University is the record of work carried out by him under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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Abstract

Non-linear load has caused a fluctuating and harmonic currents which resulted low efficiency, poor power factor, additional losses and overheating of equipment that lead to the degradation of power quality. The active power filter is effectively compensates the current harmonics and reactive power at point of common coupling by inject compensating currents in to the source to cancel the harmonics contained in the load current. It is achieved by using Instantaneous Reactive Power Theory (P-Q theory) and Fryze Current Computation Technique. Voltage source inverter(VSI) based SAPF's are widely used for compensating the load current harmonics, improving the power factor for nonlinear loads. This VSI switching signals are generated through advanced three-level hysteresis current controller (HCC) that achieves significant reduction in the magnitude and variation of the switching frequency improved performance. The adaptive hysteresis band current controller changes the hysteresis bandwidth according to modulation frequency, supply voltage, DC capacitor voltage and slope of the reference compensator current wave.

List of Figures

Abbreviations

SAPF ..... Shunt Active Power Filter
VSI ..... Voltage Source Inverter
IRP ..... Instantanious Reactive Power Theory
THD ..... Total Harmonic Distortion
IEEE ..... Institute of Electrical and Electronic Engineers
PWM ..... Pulse Width Modulation
IGBT ..... Insulated Gate Bipolar Transistor
UPS ..... Uninterrupted Power Supply
PLCs ..... Programmable logic controller
ASDs ..... Adjustable speed drive
LPF ..... Low Pass Filters)
APF ..... Active Power Filters
NPC ..... Neutral Point Converter
FC ..... Flying Capacitor

Nomenclature

ϕ ..... Phase

G_e ..... Average value of Conductance

$I_{ca}*$ ..... Reference Compensating Current ..... [A]

I_α ..... α axis current ..... [A]

I_β ..... β axis current ..... [A]

$I_{c\alpha}$ ..... α axis compensating current ..... [A]

$I_{c\beta}$ ..... β axis compensating current ..... [A]

$I_{q\alpha}$ ..... αaxis compensating current ..... [A]

$I_{q\beta}$ ..... β axis compensating current ..... [A]

I_{la} ..... a phase non-linear load current ..... [A]

I_{lb} ..... b phase non-linear load current ..... [A]

I_{lc} ..... c phase non-linear load current ..... [A]

I_{sa} ..... a phase source current ..... [A]

I_{wa} ..... Active currents phase a ..... [A]

I_{wb} ..... Active currents phase b ..... [A]

I_{wc} ..... Active currents phase c ..... [A]

$I_{\overline{wa}}$ ..... Active currents phase a ..... [A]

p ..... Active Power ..... [W]

$\overline{p}$ ..... Mean value of the instantaneous real power ..... [W]

p_{loss} ..... Alternating value of the instantaneous real power ..... [W]

v_α ..... α axis voltage ..... [V]

v_β ..... β axis voltage ..... [V]

v_a ..... Voltage of phase a ..... [V]

v_b ..... Voltage of phase b ..... [V]

v_c ..... voltage of phase c ..... [V]

V_{dc} ..... DC link Voltage ..... [V]

Contents

Chapter 1

Introduction

1.1 Background

Power Quality is characterized by expressing harmonic pollution, reactive power and load unbalancing. The right technology a variety of power quality problems can be solved rendering installations trouble free and more efficient and can render them complaint with even the strictest requirements. Meanwhile, it is very important to solve the problems of harmonics caused by that equipment which is already installed [1].

1.2 Problem Identification

With the rapid development of modern industrial technology and growing use of non-linear loads especially the power-electronics equipment in power system, harmonic currents and reactive power are drawn into the grid. Recent wide spread of power electronic equipment has caused an increase of the harmonic disturbances in the power systems. The nonlinear loads draw harmonic and reactive power components of current from AC mains. Current harmonics generated by non-linear loads such as adjustable speed drives, static power supplies and UPS. The harmonics causes problems in power systems and in consumer products such as equipment overheating,

capacitor blowing, motor vibration excessive neutral currents and low power factor. Power pollution owing to the nonlinear loads results in the degradation of power quality in the distribution system. The non-sinusoidal balanced or unbalanced currents generate harmonics, reactive power, excessive neutral current and unbalance loading of the mains[2][3].

The presence of harmonics in the power line results in following problems:

a. Greater power losses due to higher currents resulting from reactive power and harmonic current in the distribution network.

b. Interference in the communication system

c. Operation failure of electronic equipments

1.3 Literature

1.3.1 Evolution of electric power theory

At the end of 19^{th} century the development of alternating current (AC) transmission system was based on sinusoidal voltage at constant frequency generation[2]. Sinusoidal voltage with constant frequency has made easier the design of transformer, machines and transmission lines. If the voltage will be non-sinusoidal then it will create many complications in the design of transformer, machine and transmission system. Conventional power theory was based on active, reactive and apparent-power definitions were sufficient for design and analysis of power systems. Nevertheless, some papers were published in the 1920's, showing the conventional concept of reactive and apparent power losses its usefulness in non-sinusoidal cases. Then, two important methods to power definitions under non sinusoidal condition were introduced by Budeanu in 1927's[2] and Fryze in 1932.Fryze defined power in time domain whereas Budeanu did it in frequency domain. Subsequently power electronics was introduced in 1960's[2], non-linear loads that consume non sinusoidal current have

increased significantly. Now in this day power electronics based equipment are used in residential an industrial purpose. In 1976, Harshima, Inaba and Tsuboi presented, probably for the first time, the term "Instantaneous Reactive Power" for a single phase circuit. That same year, Gyugyi and Strycula used the term "Active AC Filters" for the first time. A few years later, in 1981, Takahashi, Fujiwara, and Nabae published two papers giving the hint of the appearance of the instantaneous power theory or "P-Q theory"[2].

1.3.2 Power Quality

The PQ issue is defined as "any occurrence manifested in voltage, current, or frequency deviations that results in failure, damage, upset, or misoperation of end-use equipment[1]. Today, most of the power quality issues are related to the power electronics equipment which is used in commercial, domestic and industrial application. The applications of power electronics equipment for residential purposes TVs, PCs, Refrigerator etc, for business purposes-copiers, printers etc, for industrial purposes-PLCs (Programmable logic controller), ASDs (Adjustable speed drive), rectifiers, inverters etc. Today almost all electrical equipment is based on power electronics which causes harmonics, inter-harmonics, notches and neutral currents. Transformers, motors, cables, interrupters, and capacitors (resonance) are some of the equipment which is affected by harmonics[3]. Notches are produced mainly because of the converters, and they basically affect the electronic control devices. Neutral currents are produced in that equipment which uses switched-mode power supplies, such as printers, photocopiers, PCs, and any triplets generator. Neutral current affects the neutral conductor temperature and transformer capability. Inter-harmonics are generated because of cyclo-converters, static frequency converters, arching devices and induction motors. The presence of harmonics in the power lines results in greater power losses in distribution, and cause problem by interfering in communication systems and, sometime cause operation failures of electronic equipment, which are more and

more critical because it consists of microelectronic control systems, which work under very low energy levels. Because of these problems, the power quality issues delivered to the end consumers are of great concern[2].

The major causes of power quality problems are due to the wide spread application of nonlinear loads such as fluorescent lamps, saturable devices, static power electronic converters and arch furnaces. These equipments draw harmonic and reactive power components of current from the ac mains. In three phase system, they can cause unbalance and draw excessive neutral currents. The injected harmonic, reactive power burden, and excessive neutral currents cause low system efficiency and poor power factor, they also cause disturbance to other consumers. So far to come out of this problems shunt passive filters (consist of tuned LC filters and/or high pass filters) have been used to improve power factor and to reduce harmonics in power systems. But, shunt passive filters was not giving desired performance which leads to the development of "Active Power Filters (APF's)"[2][4].

1.4 Objective of the Work

a. Filter is a kind of equipment for eliminating harmonic currents and reactive power.

b. To establish the compensation methods for the shunt active power Filter.

c. To develop flowchart of the compensation methods and simulate the same in Matlab/Simulink software.

d. Implementation of the compensation methods using Controller.

Chapter 2

Active Power Filters

2.1 Active Power Filters

2.1.1 Introduction

The basic principle of compensation of active power filters were proposed around 1970 [Bird et al., 1969] and 1976 [Gyugyi and Strycula]. Sometimes the active power filters are also called active power line conditioners and are able to compensate current and voltage harmonics, reactive power, regulate terminal voltage, suppress flicker and to improve voltage balance in three phase systems. The advantage of active is that it automatically adapts to changes in the network and load fluctuations. They can compensate for several harmonic orders and are not affected by major changes in network characteristics, eliminating the risk of resonance between the filter and impedance network. Another plus is that they take up very little space compared with traditional passive compensators[2].

2.1.2 Types of Active Power Filters

Active power lters can be classied based on the type of converter, topology, control scheme ,and compensation characteristics. The most popular classication is based on the topology such as shunt ,series ,or hybrid. The hybrid conguration Is a

combination of passive and active compensation.

a. **Shunt Active Power Filter:-** Shunt active power lters are widely used to Compensate current harmonics , reactive power ,and load current unbalanced. It can also be used as a static var generator in power system networks for stabilizing and improving voltage prole[2].

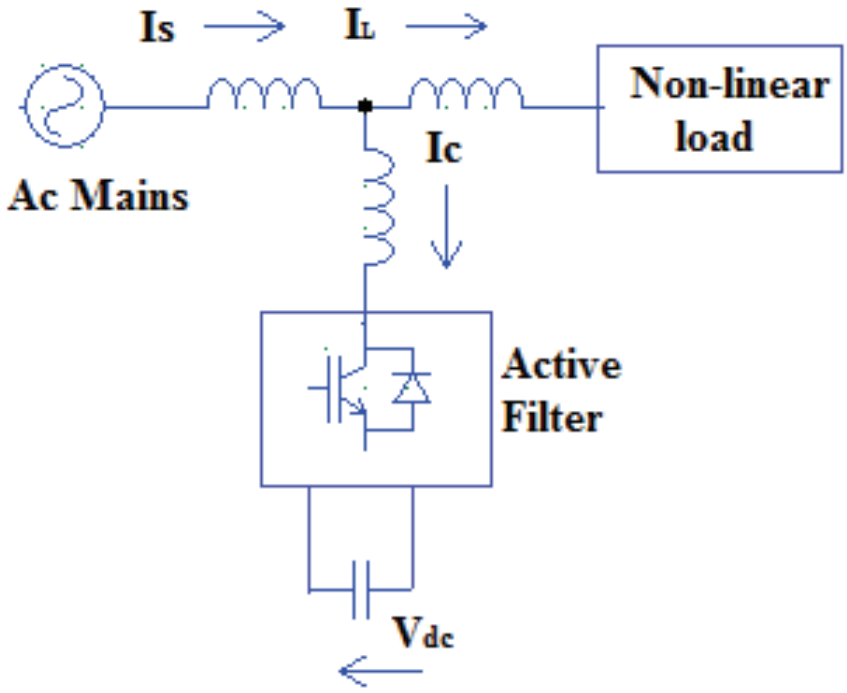

Figure 2.1: Shunt Active Power Filter

b. **Series Active Power Filter:-** Series active power lters is connected before the load in series with the ac mains, through a coupling Transformer to eliminate voltage harmonics and to balance and Regulate the terminal voltage of the load or line[2].

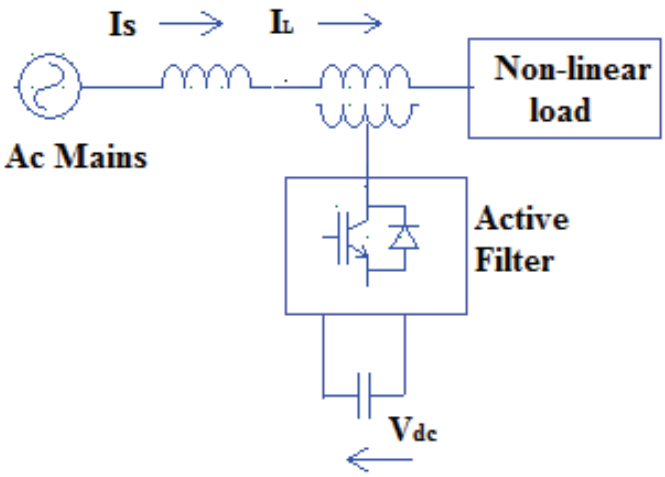

Figure 2.2: Series Active Power Filter

c. **Hybrid Active Power Filter:-**

The hybrid conguration is a combination of series active lter and passive shunt lter. This topology is very convenient For the compensation of high power systems, because the rated Power of the active lter is signicantly reduced[2].

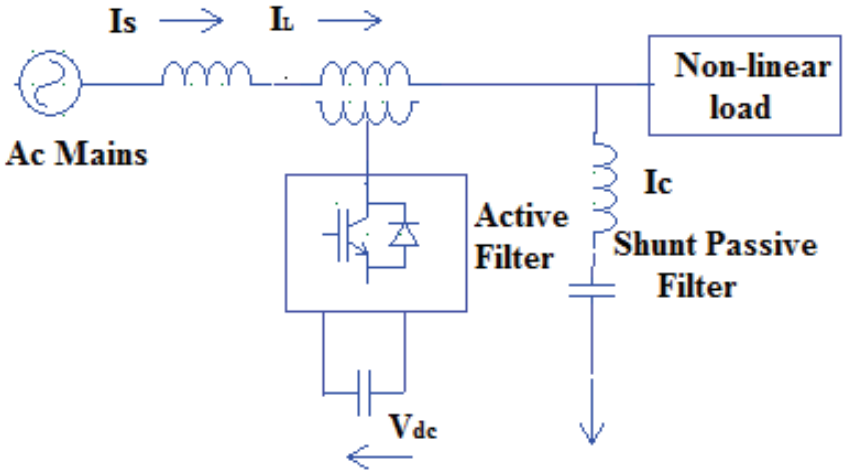

Figure 2.3: Hybrid Active Power Filter

2.1.3 Principle and Operation of Shunt Active Power Filter

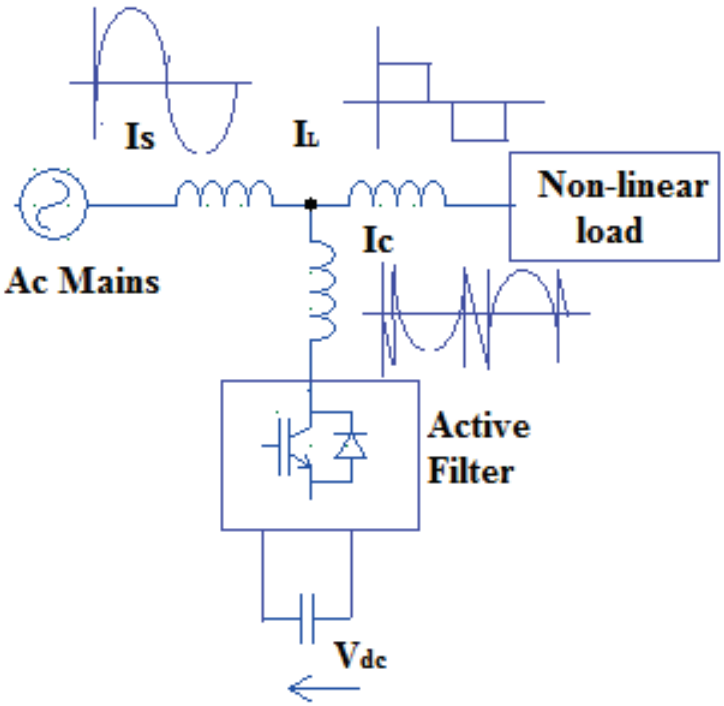

Figure 2.4: Operation of Shunt Active Power Filter

Fig 2.4 shows the basic compensation principle of the three phase shunt APF. It is designed to be connected in parallel with the nonlinear load to detect its harmonic and reactive current and to inject into the system a compensating current. In the conventional p-q theory based control approach for the shunt APF, the compensation current references are generated based on the measurement of load currents. However, the current feedback from the SAPF output is also required and therefore, minimum six CSs are desired in a unbalanced system[5].

In addition, the reference current calculation algorithm are simplified and easily implemented in the experimental prototype. In the reduced current measurement control algorithm, sensing only three-phase voltages, three source currents and a DC-link voltage is adequate to compute reference currents of the three phase SAPF. In this

way, the overall system design becomes easier to accomplish and the total implementation cost is reduced[3][6].

2.1.4 Power Circuit of Shunt Active Power Filter

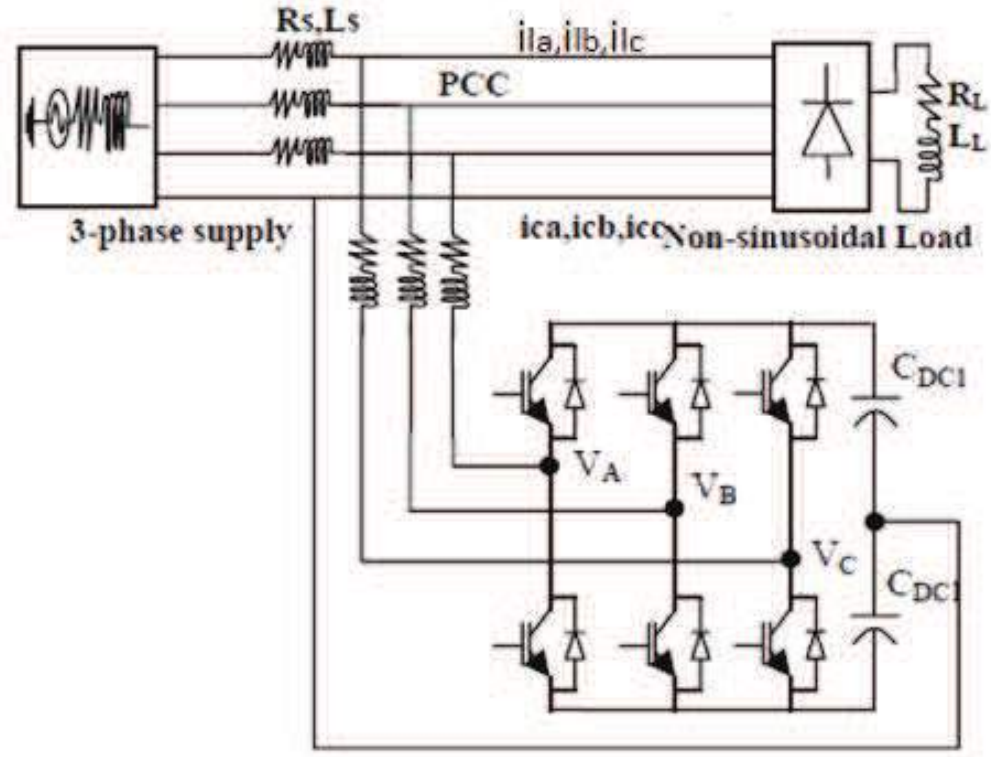

Figure 2.5: Power Circuit of Active Power Filter Shunt

The conventional power circuit of the voltage source inverter based active power filter connected at the point of common coupling, as shown in fig 2.5. The voltage source inverter has six power transistors with freewheeling diodes and two energy storages capacitor on DC-side that is implemented as a four wire active power filter. The three-phase four-wire AC power supply connected to the unbalanced non-linear load. The source draws non-sinusoidal or harmonic current due to the non-linear load. This nonlinear load current contains the fundamental signals and harmonic current components[2][5].

2.2 Power Electronics Converter

Here generally two types of 3-level inverters are used:

a. Three-level neutral point clamped inverter

b. Three-level flying capacitor inverter

2.2.1 Three level Neutral Point Clamped Inverter

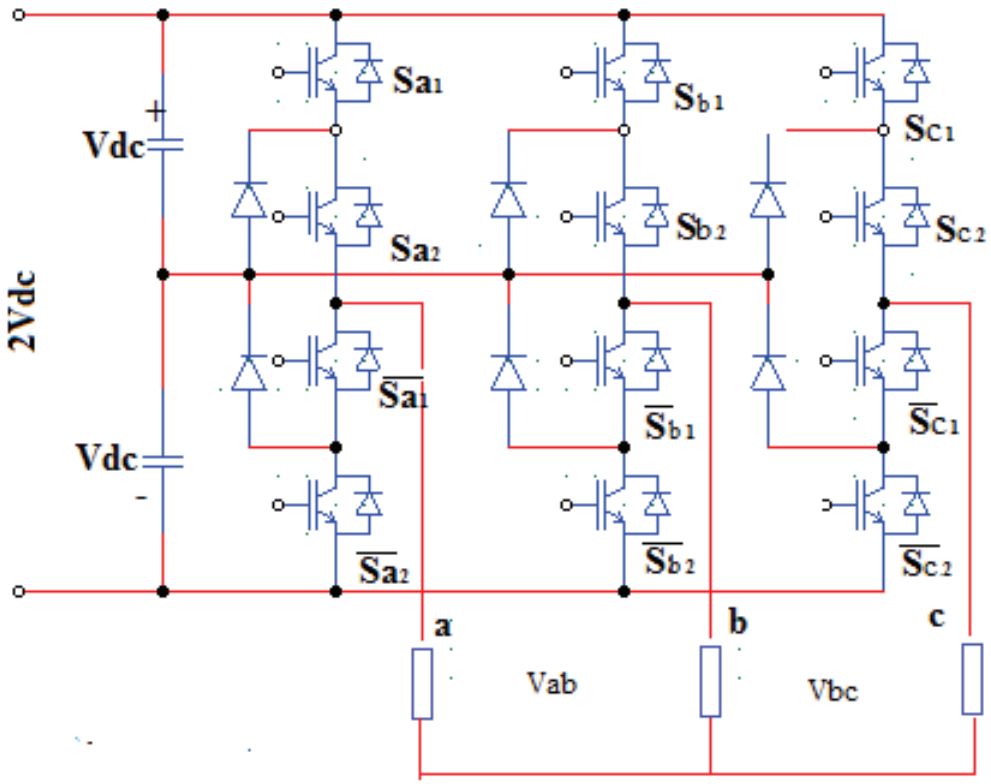

Figure 2.6: 3-level Neutral Point Clamped Inverter

In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors,C_1 and C_2. The middle point of the two capacitors n can be defined as the neutral point[7].

The output voltage Van has three states: $V_{dc/2}$, 0, and $V_{dc/2}$. For voltage level $V_{dc/2}$, switches S_1 and S_2 need to be turned on; for $-V_{dc/2}$, switches S_1' and S_2' need to be turned on; and for the 0 level,S_2 and S_1' need to be turned on. Note that out of the four possible switch combinations, only three are allowed since state 4 generates a high impedance output and does not provide a current flow path for the output load current[8].

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_2. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S_1 and S_2 turn on, the voltage across a and 0 is V_{dc}, i.e.$V_{ao} = V_{dc}$. In this case D_1, balances out the voltage sharing between S_1' and S_2' with S_1 blocking the voltage across C_1 and S_2' blocking the voltage across C_2[9].

Notice that output voltage V_{an} is ac, and V_{ao} is dc. The difference between V_{an} and V_{ao} is the voltage across C_2, which is $V_{dc/2}$. If the output is removed out between a and 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc} ,$V_{dc/2}$, and 0[7][8].

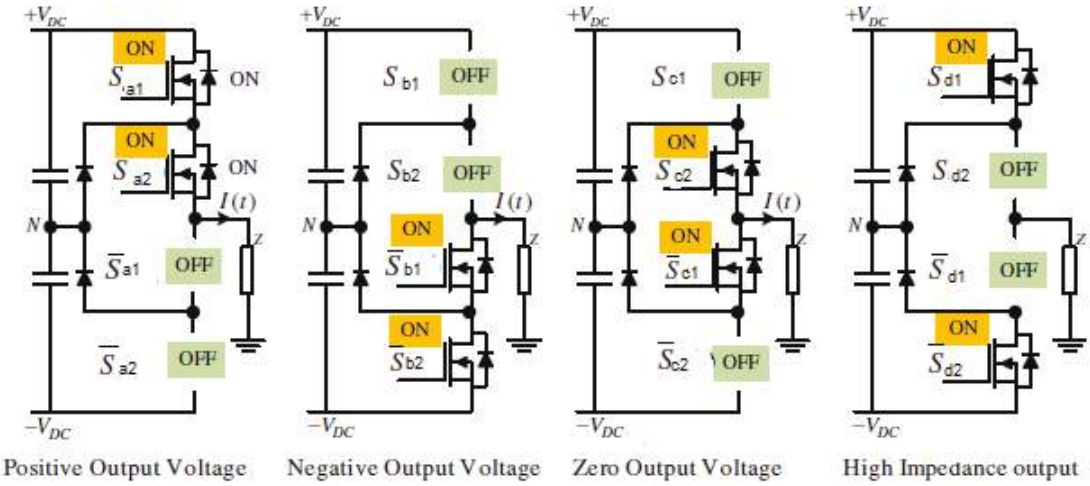

Figure 2.7: Switching Of Neutral Point Converter

The advantages of diode-clamped multilevel inverter

- Voltages across the switches are only half of the dc-link voltage.
- The first group of voltage harmonics is centered around twice the switching frequency.
- The control method is simple.

The disadvantages of diode-clamped multilevel inverter

- This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress.

2.2.2 Three-level flying capacitor inverter

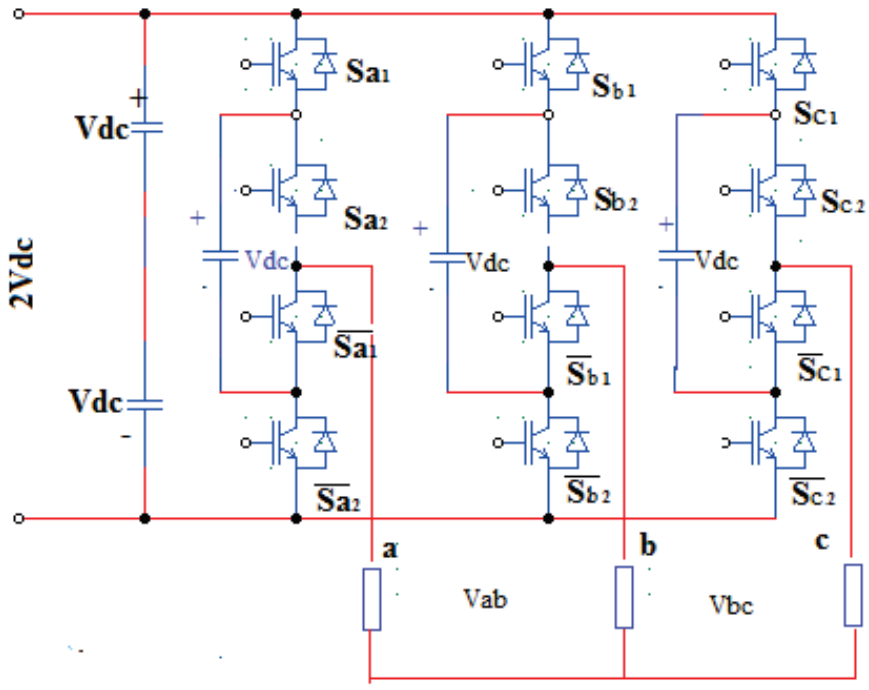

Figure 2.8: 3-level Flying Capacitor Inverter

Fig 2.8 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter with independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig 2.9 provides a three-level output across a and n, i.e., $V_{an} = V_{dc/2}$, 0, $-V_{dc/2}$. For voltage level $V_{dc/2}$, switches S_1 and S_2 need to be turned on; for $V_{dc/2}$, switches S_1' and S_2' need to be turned on and for the 0 level, either pair (S_1, S_1') or $(S_2, S_2$) needs to be turned on[7].

The 0 level, either pair (S_1, S_1') or (S_2, S_2) needs to be turned on. Clamping capacitor C_1 is charged when S_1 and S_1' are turned on, and is discharged when S_2 and S_2' are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination[8].

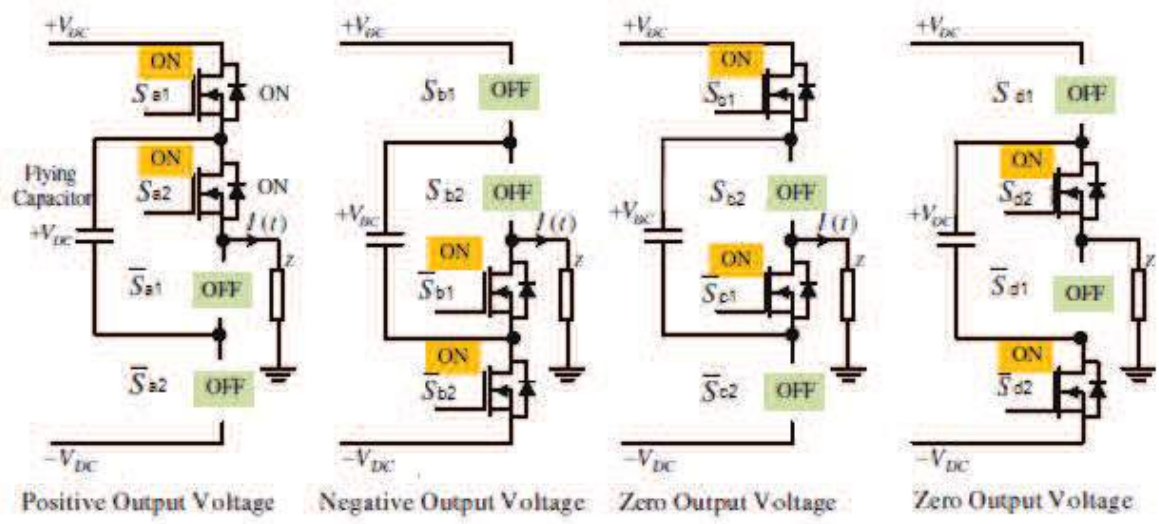

Figure 2.9: Switching Of Flying Capacitor Converter

The advantages of Flying Capacitor topology are

- This topology naturally limits the $\frac{dV}{dt}$ stress across the devices.
- Introduces additional switching states that can be used to help maintain the charge balance in the capacitors.

The disadvantages of Flying Capacitor topology are:

- The flying capacitor topology might require more capacitance than the equivalent diode clamped topology. In addition, it is obvious that rather large RMS currents will flow through these capacitors.
- High-level inverters are more difficult to package with the bulky power capacitors and are more expensive.

Chapter 3

Different Techniques of Reference Current Generation

3.1 Different Techniques of Reference Current Generation

a. The Instantaneous Reactive Power Theory.

b. Synchronous Reference Frame Theory

c. DC link voltage Regulation Method.

d. Fryze Current Computation Methods.

3.1.1 The Instantaneous Reactive Power Theory

Akagi et al proposed a theory on instantaneous values in three-phase power systems with or without neutral wire, and is valid for steady-state or transitory operations, as well as for generic voltage and current waveforms called as Instantaneous Power Theory or Active- Reactive (P-Q) Theory which consists of an algebraic transformation

(Clarke) of the three-phase voltages in the a-b-c coordinates to the $\alpha\beta 0$ coordinates[2][4].

3.1.2 The P-Q theory

In 1983 Akagi et al proposed a new theory for the control of active filters in three-phase power systems called "Generalized Theory of the Instantaneous Reactive Power in Three-Phase Circuits", also known as "Theory of Instantaneous Real Power and Imaginary Power", or "Theory of Instantaneous Active Power and Reactive Power", or "Theory of Instantaneous Power", or simply as "P-Q Theory". The theory was initially developed for three-phase three wire systems, with a brief mention to systems with neutral wire[2][3].

Since the P-Q theory is based on the time domain, it is valid both for steady-state and transient operation, as well as for generic voltage and current waveforms, allowing the control of the active filters in real-time.

Another advantage of this theory is the simplicity of its calculations, since only algebraic operations are required. The only exception is in the separation of some power components in their mean and alternating values. However, as it will be shown in this paper, it is possible to exploit the symmetries of the instantaneous power waveform for each specific power system, achieving a calculation delay that can be as small as 1/6 and never greater than 1 cycle of the power system frequency. It is also shown that calculations for reactive power and zero-sequence compensation do not introduce any delay.

Furthermore, it is possible to associate physical meaning to the P-Q theory power components, which eases the understanding of the operation of any three-phase power system, balanced or unbalanced, with or without harmonics.

The P-Q theory implements a transformation from a stationary reference system in a-b-c coordinates, to a system with co-ordinates $\alpha\beta 0$. It corresponds to an algebraic transformation, known as Clarke transformation[3].

3.1.3 Clarke's Transformation

A change of variables is often used to reduce the complexity of these differential equations. Using these transformations, many properties of electric machines can be studied without complexities in the voltage equations. The transformation of stationary circuits to a stationary reference frame was developed by E. Clarke. The stationary two-phase variables of Clarkes transformation are denoted as α and β,α-axis and β -axis are orthogonal. No zero sequence voltage and current exists in a three phase three wire system so that v_o and i_o can be eliminated. The Clarke's Transformation and its inverse transformation of the three phase generic voltages are given by[2][10]:-

$$\begin{pmatrix} V_0 \\ V_\alpha \\ V_\beta \end{pmatrix} = \sqrt{(2/3)} \begin{pmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{3.1}$$

Its inverse transformation is given by

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = \sqrt{(2/3)} \begin{pmatrix} 1/\sqrt{2} & 1 & 1 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & /2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} V_0 \\ V_\alpha \\ V_\beta \end{pmatrix} \tag{3.2}$$

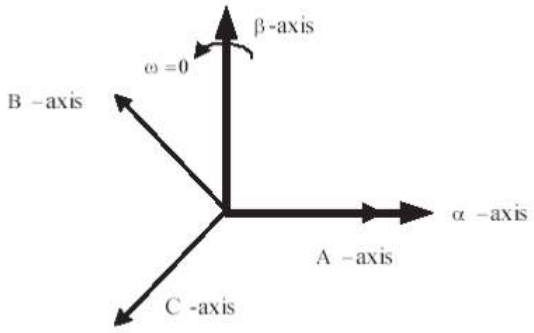

Figure 3.1: Three Phase Generic Current

Three phase generic current are given by:-

$$\begin{pmatrix} i_0 \\ i_\alpha \\ i_\beta \end{pmatrix} = \sqrt{(2/3)} \begin{pmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \tag{3.3}$$

Its inverse transformation is given by

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \sqrt{(2/3)} \begin{pmatrix} 1/\sqrt{2} & 1 & 1 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & /2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} i_0 \\ i_\alpha \\ i_\beta \end{pmatrix} \tag{3.4}$$

3.1.4 Active Power In Terms Of Clarkes Transformation

This feature is very suitable when the focus is put on the analysis of instantaneous power in three-phase systems. The three-phase instantaneous active power, P3is calculated from the instantaneous phase voltages and line currents as follows

$$P3\phi(t) = V_{a(t)}i_{a(t)} + V_{b(t)}i_{b(t)} + V_{c(t)}i_{c(t)} \tag{3.5}$$

$$P3\phi = V_a i_a + V_b i_b + V_c i_c \tag{3.6}$$

where v_a,v_b and v_c are the instantaneous phase voltages and i_a,i_b and i_c the instantaneous line currents. In a system without a neutral wire, v_a,v_b and v_c are measured from a common point of reference. Sometimes it is called as "ground" or "fictitious point". For instance, if the b phase is chosen as the reference point, the measured "phase voltages" and the three-phase instantaneous active power,$P3\phi$, are calculated as[2][4]:

$$P3\phi = (V_a - V_b)i_a + (V_b - V_b)i_b + (V_c - V_b)i_c = V_{ab}i_a + V_{cb}i_c \tag{3.7}$$

$$q = V_\alpha i_\beta V_\beta i_\alpha = 1/3[(V_a - V_b)i_c + (V_b - V_c)i_a + (V_c - V_a)i_b] \tag{3.8}$$

The three-phase instantaneous active power can be calculated in terms 0 components as follows:-

$$P3 = V_a i_a + V_b i_b + V_c i_c = V_\alpha i_\alpha + V_\beta i_\beta + V_0 i_0 \tag{3.9}$$

3.1.5 The P-Q Theory In $3-\phi$ And 3-Wire System

A new definition of instantaneous complex power is possible, using the instantaneous vectors of voltage and current. The instantaneous complex power s is defined as the product of the voltage vector e and the conjugate of the current vector i*, given in the form of complex numbers:

$$s = ei* = (V_\alpha + jV_\beta)(i_\alpha + ji_\beta) = (V_\alpha i_\alpha + v_\beta i_\beta) + j(V_\beta i_\alpha - V_\alpha i_\beta) \tag{3.10}$$

The original definition of instantaneous active and reactive power is:-

$$p = V_\alpha i_\alpha + V_\beta i_\beta = p + p_{loss} \tag{3.11}$$

where P= Mean value of the instantaneous real power.
The instantaneous powers defined in the $\alpha\beta 0$ reference frame are the real power p,imaginary power q, and the zero sequence power P_0[2]. They are given by:-

$$\begin{pmatrix} p0 \\ p \\ q \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & V_\alpha & V_\beta \\ 0 & -V_\beta & V_\alpha \end{pmatrix} \begin{pmatrix} i_0 \\ i_\alpha \\ i_\beta \end{pmatrix} \tag{3.12}$$

However, instantaneous values of voltage and currents are used here and physical meaning of the imaginary power q agrees with the basic definition of the instantaneous reactive power given in its definition. Akagi suggested a new unit for q the Imaginary Volt-Ampere (VA)[2]. A new algorithm to determine the instantaneous reactive currents can be derived from the sub matrix. The $\alpha\beta$ reactive currents are calculated:

$$\begin{pmatrix} i_{q\alpha} \\ i_{q\beta} \\ \end{pmatrix} = \frac{1}{V_\alpha^2 + V_\beta^2} \begin{pmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{pmatrix} \begin{pmatrix} 0 \\ q \end{pmatrix} \tag{3.13}$$

The inverse transformation of $i_{q\alpha}$ and $i_{q\beta}$ results in :

$$\begin{pmatrix} i_{qa} \\ i_{qb} \\ i_{qc} \end{pmatrix} = \sqrt{(2/3)} \begin{pmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{pmatrix} \begin{pmatrix} i_{q\alpha} \\ i_{q\beta} \end{pmatrix} \tag{3.14}$$

It should be noted that, a-b-c phase voltages are influenced by zero sequence components, while the voltages and power q are not affected by these components. One may choose to compensate imaginary the imaginary power along with oscillating power p_{osc} of the real power p is given by[3]

$$\begin{pmatrix} i_{c\alpha} \\ i_{c\beta} \end{pmatrix} = \frac{1}{V_\alpha^2 + V_\beta^2} \begin{pmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{pmatrix} \begin{pmatrix} p + p_{osc} \\ q \end{pmatrix} \tag{3.15}$$

Using inverse Clarke's Transformation we get the final compensating currents for three phase using the equations shown below

$$i_{ca}* = (2/3)i_\alpha*, i_{cb}* = (1/6)i_\alpha * + (1/2)i*, i_{cc}* = -(1/6)i_\alpha * - (1/2)i_\beta \tag{3.16}$$

3.1.6 Block Diagram

The block diagram calculates the real and imaginary powers of the non - linear load that should be compensated by the shunt active filter. According to the P-Q Theory only real and imaginary powers exists, because the zero sequence power is always zero. Additionally, the dc voltage determines an extra amount of real power, represented by p_{loss}, that causes an additional low of energy to the dc capacitor in order to keep its voltage around a fixed reference value[11].

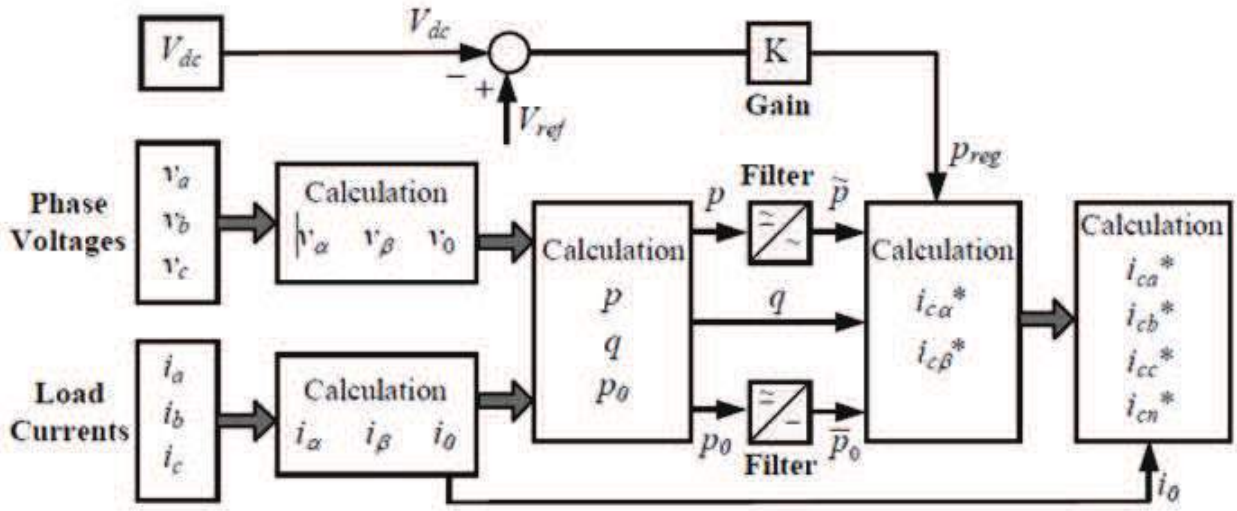

Figure 3.2: Block diagram Instantaneous Reactive Power Theory

This real power p_{loss} is added to the compensating real power p_{ac} which together with the compensating imaginary power q_c are passed to the current reference calculation. It determines the instantaneous compensating current references from the compensating powers and voltages.

A dc voltage regulator should be added to control strategy in a real implementation as shown. In fact, a small amount of average real power (p_{loss}) must be drawn continuously from the power losses to supply switching and ohmic losses in PWM. Otherwise, this energy would be supplied by the dc capacitor, which would discharge continuously. The real power of the non-linear load should be continuously separated into its average ($\overline{p}$)and oscillating ($\widetilde{p}$) parts. In a real implementation, the separation of ($\overline{p}$) and ($\widetilde{p}$) from p is realized through a low pass filter. The low pass filter and its cut off frequency must be selected carefully as to the inherent dynamics that lead to compensation errors during transients. The oscillating real power is determined by the difference, that is ($\widetilde{p} = p - \overline{p}$). A lower cutoff frequency in the low pass filter may be required, depending on the spectral components included in ($\widetilde{p}$) that is to be compensated[2][3][4].

3.2 Fryze Current Computation Method

In 1932 ,S.Fryze developed new control method that facilitates extracting the fundamental component of load current, commonly known as Fryze power theory. In 1979 N.Depenbrock promoted the power analysis method based on Fryze power theory and it was further modified by F.Buchholz. This improved is now known as FBD and it is used in time domain analysis[2].

The time domain FBD approach is an alternative that is used to analyze the relationship of voltage, current and reactive power calculation is adopted. The VSI switching signals are derived from adaptive-hysteresis current controller. Fryze power theory (or Fryze current minimization) based active filter for power line conditioning. The shunt APLC is implemented with three-phase PWM-voltage source inverter and is connected at PCC for compensating the current harmonics by injecting equal but opposite harmonic compensating current.

The reference currents are extracted using Fryze power theory method. The inverter gate drivel signals are derived from adaptive-hysteresis current controller. This Fryze power method maintains the dc-side capacitance voltage of the inverter constant without any external controller circuit. The shunt APLC system is investigated under diode and thyristor rectifier load conditions. A comparative assessment of fixed-HCC and adaptive-HCC are done[12].

3.2.1 Block Diagram Fryze Power Theory

The generalized Fryze power theory method presents a minimum rms value so that the same three phase average active power is drawn from the source as the original load current shown in Fig 3.3 This reduces the ohmic losses in the transmission line and guarantees linearity between the supply voltage and compensated current. The instantaneous equivalent conductance (G_e) is calculated from the three phase instantaneous active power (p3Θ)[12].

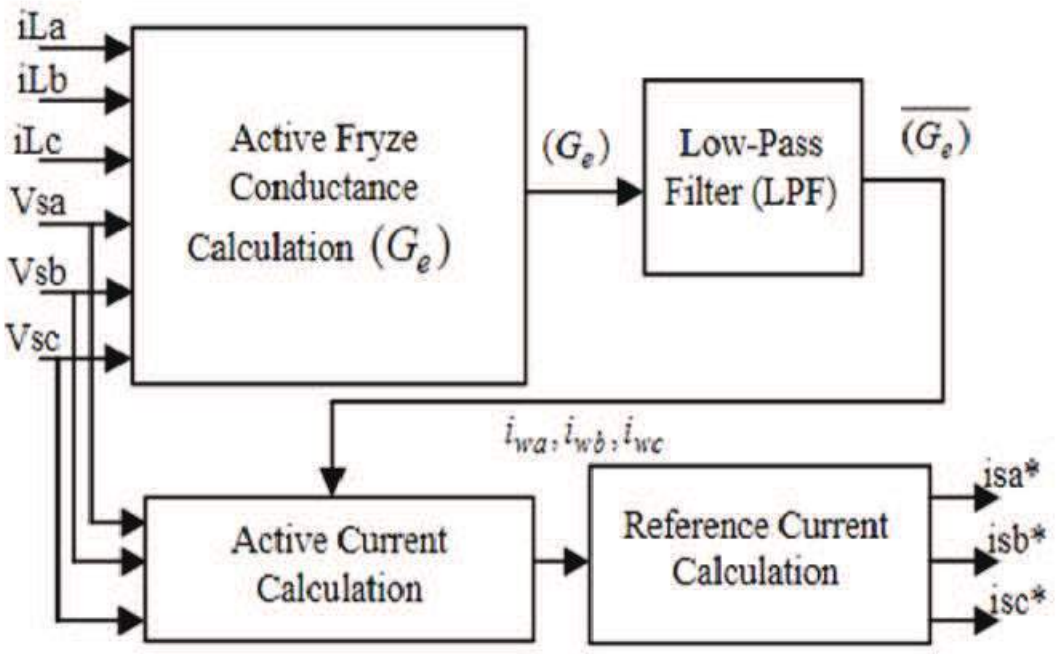

Figure 3.3: Block Diagram Fryze Power Theory

$$P3_{\Theta(t)} = V_{sa(t)} i_{sa(t)}) + V_{sb(t)} i_{sb(t)} + V_{sc(t)} i_{sc(t)} \tag{3.17}$$

$$p3_{\Theta(t)} = P_{sa(t)} + P_{sb(t)} + P_{sc(t)} \tag{3.18}$$

Moreover the root mean square (rms) aggregate voltage is derived from the instantaneous value of phase voltages, its given as,

$$V\Sigma = \sqrt{({V_{sa(t)}}^2 + {V_{sb(t)}}^2 + {V_{sc(t)}}^2)} \tag{3.19}$$

The conductance or admittance (G_e) is represented by an average value instead of a varying instantaneous value. The instantaneous conductance is calculated from the three phase instantaneous phase voltages $V_{a1}, V_{b1} V_{c1}$ calculated from the positive sequence voltage detector V+1 and load currents i_{la}, i_{lb} i_{lc}[2][10]. Its derived as

$$G_e = \frac{v_{a1}i_{la} + v_{b1}i_{lb} + v_{c1}i_{lc}}{v_{a1}^2 + v_{b1}^2 + v_{c1}^2} \tag{3.20}$$

The average conductance(G_e) pass through Butterworth design based Low Pass Filter (LPF). The LPF cutoff or sampling frequency is assigned 50 Hz fundamental frequency that allows only the fundamental signals to the active current section. The instantaneous active currents i_{aw}, i_{wb}, i_{wc} and, of the load current are directly calculated by multiplying (G_e) by phase voltages V_a, V_b, V_c respectively and are defined as[2][12]

$$i_{wa} = \overline{G_e}V_a \tag{3.21}$$

$$i_{wb} = \overline{G_e}V_b \tag{3.22}$$

$$i_{wc} = \overline{G_e}V_c \tag{3.23}$$

The desired reference source currents calculated from the active current, after compensation, can be written as

$$i_{sa}* = i_{wc} = I_{rms}sint \tag{3.24}$$

$$i_{sb}* = i_{wb} = I_{rms}sin(t - 120) \tag{3.25}$$

$$i_{sc}* = i_{wc} = I_{rms}sin(t + 120) \tag{3.26}$$

Chapter 4

Hysteresis Current Control

4.1 Hysteresis Current Control

Active filters produce a nearly sinusoidal supply current by measuring the harmonic currents and then injecting them back into the power system with a 180^0 phase shift. A controlled current inverter is required to generate this compensating current. Hysteresis current control is a method of controlling a voltage source inverter so that an output current is generated which follows a reference current waveform[13].

This method controls the switches in an inverter asynchronously to ramp the current through an inductor up and down so that it tracks a reference current signal. Hysteresis current control is the easiest control method to implement (Brod and Novotny 1985). One disadvantage is that there is no limit to the switching frequency, but additional circuitry can be used to limit the maximum switching frequency (Malesani et al 1996)[14].

A hysteresis current controller is implemented with a closed loop control system and is shown in diagrammatic 4.1. An error signal, e(t), is used to control the switches in an inverter. This error is the difference between the desired current, $i_{ref(t)}$, and the current being injected by the inverter, $i_{actual(t)}$. When the error reaches an upper limit, the transistors are switched to force the current down[13].

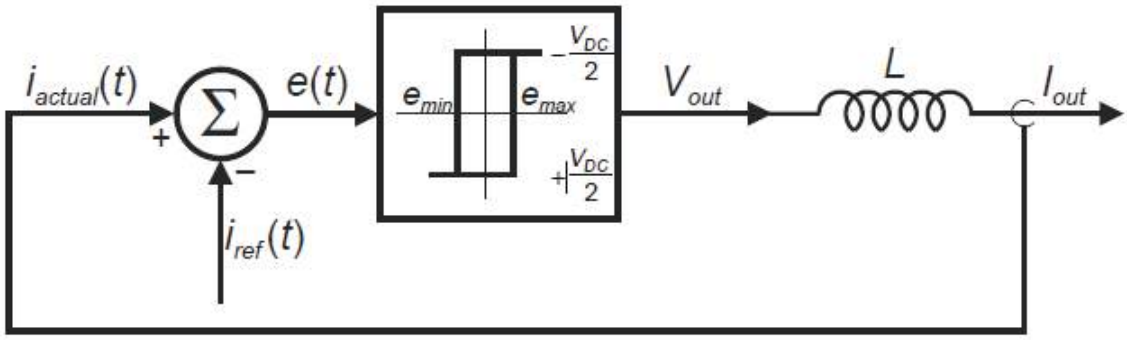

Figure 4.1: Hysteresis current controller

When the error reaches a lower limit the current is forced to increase. The minimum and maximum values of the error signal are e_{min} and e_{max} respectively. The range of the error signal, e_{max} e_{min}, directly controls the amount of ripple in the output current from the inverter and this is called the Hysteresis Band[15].

The hysteresis limits, e_{min} and e_{max}, relate directly to an offset from the reference signal and are referred to as the Lower Hysteresis Limit and the Upper Hysteresis Limit. The current is forced to stay within these limits even while the reference current is changing. The ramping of the current between the two limits is illustrated in Figure 4.2[16].

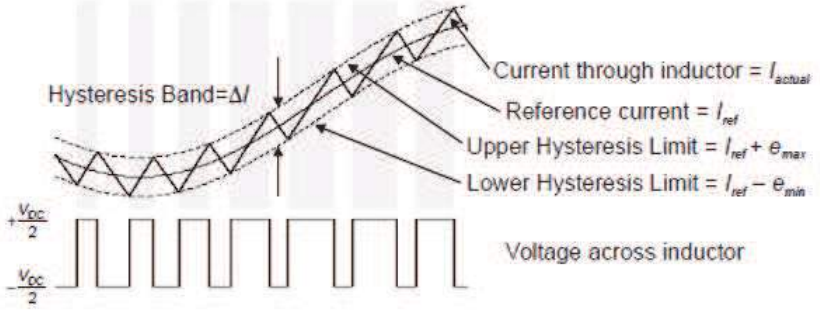

Figure 4.2: Operational waveform

The switching frequency is altered by the width of the hysteresis band, the size of the inductor that the current flows through (L in Figure 4.1) and the DC voltage applied to the inductor by the inverter. A larger inductance will yield a smaller $\frac{di}{dt}$[17].

4.1.1 Hysteresis Current Control of using NPC

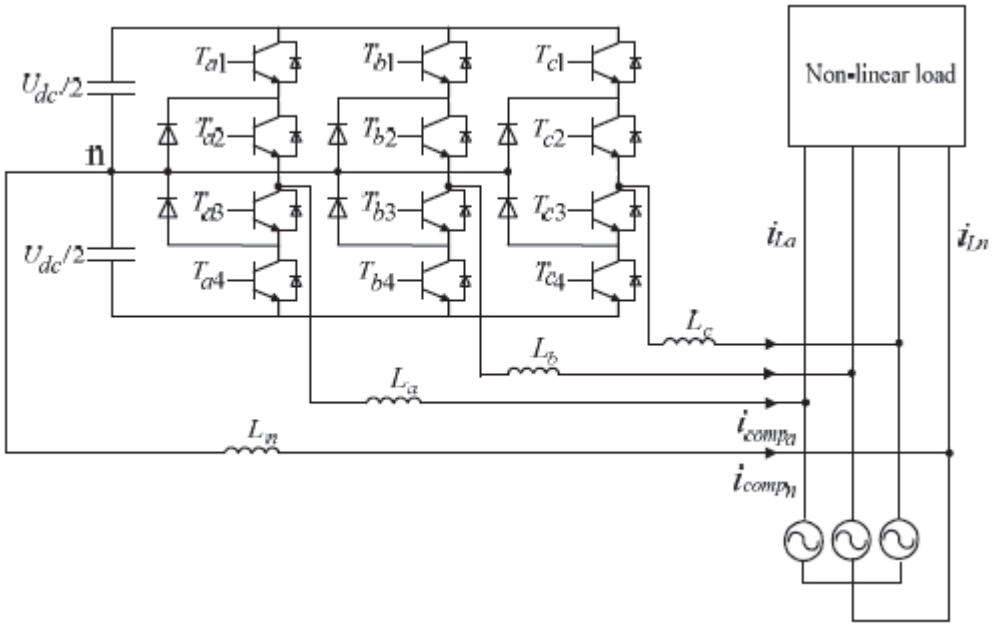

Figure 4.3: Three-phase, four-wire, three-level compensator system

In recent years, multi-level inverters are gaining significance in various applications because of their merits. Evolving alongside are different control strategies for these inverters. Some techniques involve adapting the modulation period, switching using adjacent voltage vectors of the vector space, double band modulation and monitoring slopes of current, resulting in an increased complexity of the controller. Hence, the need is for a simple three-level current control scheme, devoid of complexity[17].

In the present work, an improved three-level hysteresis control has been developed by pushing the dead zones away from the reference waveform. Utilisation of the previous input state is made, to determine the next input to be applied[19].
The influence of sampling rate on the switching logic and its limiting case are discussed in detail. The schemes are compared on the basis of certain quantitative performance indices[20].
For the considered load compensation application, a three-level, three-leg, neutral point clamped (NPC) inverter topology is used, as given in Fig 4.3. Each leg consists of four switches and two clamping diodes with an anti-parallel diode connected across every switch. The midpoint of the two identical capacitors C_{dc} is connected to the neutral wire (N-n) of the system. The three levels achievable through this configuration are V_{dc}, $2V_{dc}$ and 0, referred to as states $+1$, -1 and 0, respectively.
For the split-capacitor configuration shown in Fig 4.3 balancing the capacitor voltages becomes an inherent and unavoidable issue The output voltage across points i (i = a, b, c) and n0 is given in Table for various switch combinations[18][19].

4.1.2 Basic Three-Level Logic

To develop a switching scheme for the three-level inverter, the zero voltage level should be applied only at appropriate instants. The switching logic must ensure that there is no successive transition between +1 and -1 states, as this will increase the frequency of switching. This scheme also requires the value of tracking error (error). A dead zone(δ)is necessary in the hysteresis band(h), to avoid switching towards two-level scheme, because of finite sampling rate of error[19].

Table I: Possible voltage levels

S11	S12	S13	S14	output
1	1	0	0	+Vdc
0	1	1	0	0
0	0	1	1	-Vdc

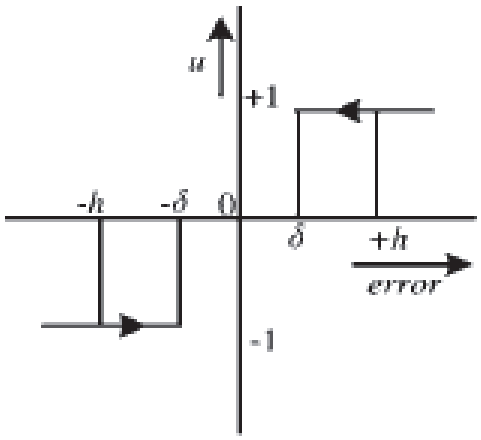

Figure 4.4: Basic Three-Level Logic

Without the dead zone, when the error becomes zero and is not detected, the opposite polarity of forcing function (u)follows, resulting in a two-level scheme. However, the introduction of dead zone increases the tracking error and has to be chosen to a minimum value, depending on the best sampling speed that can be achieved. If u represents the input state to be applied[14].

If error > 0 then

u = 1 for error $\geq h$

u= 0 for error $\leq \delta$

Else if error < 0 then

u= -1 for error $\leq -h$

u =0 for error $\geq -\delta$

The above logic represented in Fig 4.4, tracks reference current either in the lower band (through 0 and 1 states) or in the upper band (through -1and +1 states). It can be seen from Fig 4.4 that the transition from lower to upper band or vice versa occurs only through zero state. The transition from lower to upper band occurs automatically when the rate of fall of reference current waveform is higher than that of actual current. Similarly, the transition from upper to lower band occurs when the rate of rise of reference current waveform is higher than that of actual current. Although this scheme offers definite advantages over the two-level scheme, in terms of reduced losses and reduced frequency of switching, the performance is seen to be degraded in terms of total harmonic distortion (THD) and root mean square errors (RMSE) of the actual current waveform. This is due to larger deviation from the reference waveforms, since both upper and lower bands are not used simultaneously. Therefore, a modified three-level control is proposed to incorporate the advantages of both the two-level and the basic three-level schemes[19][21].

4.1.3 Improved Three-Level Logic

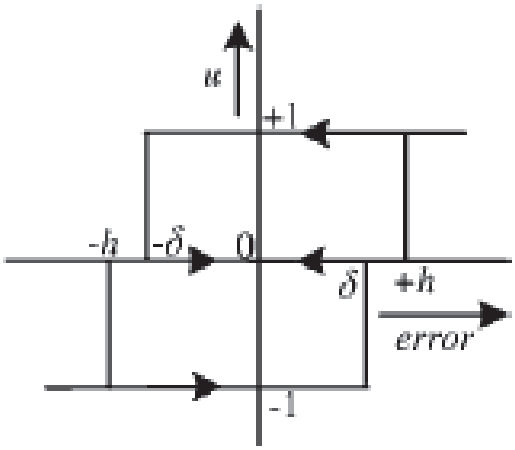

Figure 4.5: Improved Three-Level Logic

If error $\geq h$

then u = 1

If error $\leq$-δ and u_p=1

then u =0

If error $\leq -h$

then u =-1

If error $\geq\delta$ and u_p =-1

then u =0

The basic three-level scheme is modified in such a way that the lower (upper) dead zone is well extended into the upper (lower) band a little lesser than h, resulting in the overlapping of the dead zones into opposite bands. This is illustrated in 4.5. Hence, the actual current utilises both the bands for tracking, hence closely following the reference, with reduced error than in the basic scheme. Since the dead zones are overlapping, the value of error alone is not sufficient to define the switching logic. It is to be noted that the definition of dead zones is different in the basic and improved three-level schemes. The dead-zone lines are near the reference waveform in the basic scheme and near the hysteresis boundary in the improved scheme. The modified dead zones and it is clear that the zero state is applied only at δ levels[16][18][19].

Chapter 5

Arduino Uno Microcontroller ATmega328

5.1 Arduino Uno Microcontroller ATmega328

Arduino can sense the environment by receiving input from a variety of sensors and can affect its surroundings by controlling lights, motors, and other actuators. The microcontroller on the board is programmed using the Arduino programming language (based on Wiring) and the Arduino development environment (based on Processing). Arduino projects can be stand-alone or they can communicate with software running on a computer (e.g. Flash, Processing, MaxMSP).

The Arduino Uno is a microcontroller board based on the ATmega328. It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button.

The Uno differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter.

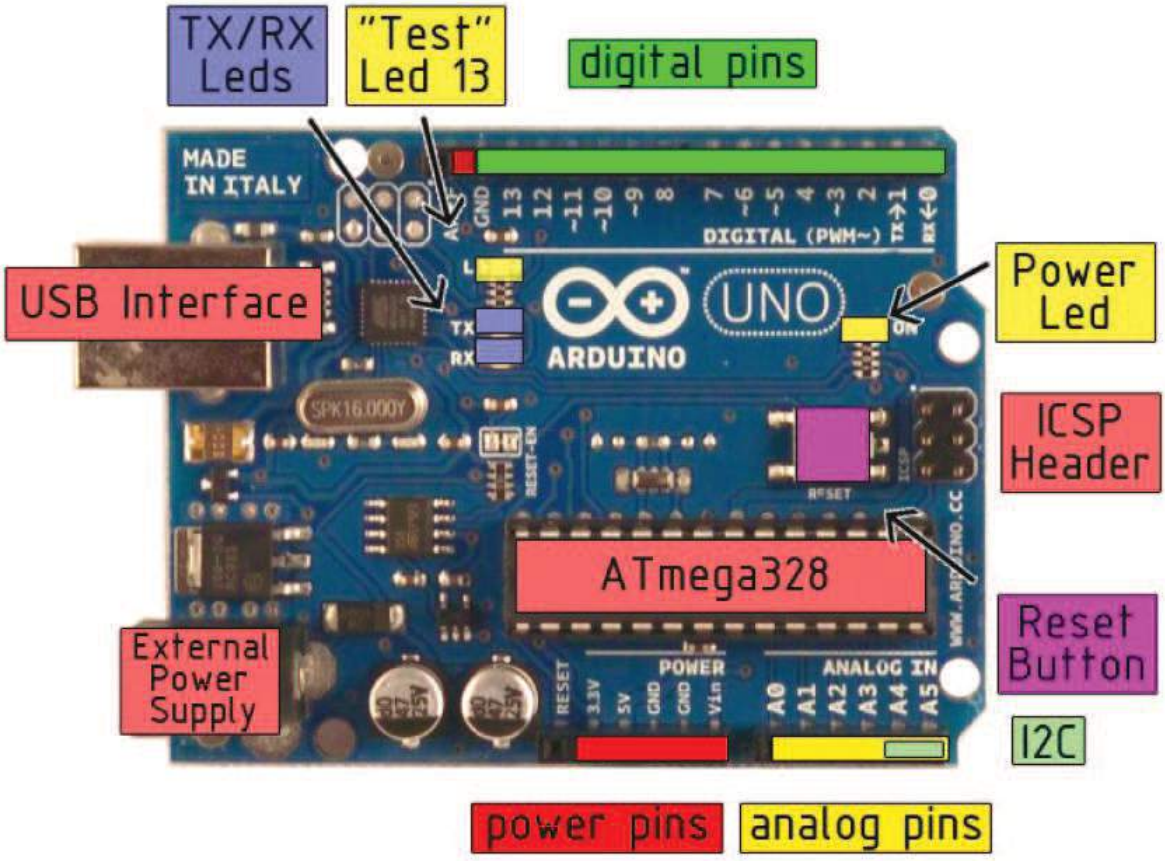

Figure 5.1: Lay Out of Arduino Uno

"Uno" means one in Italian and is named to mark the upcoming release of Arduino 1.0. The Uno and version 1.0 will be the reference versions of Arduno, moving forward. The Uno is the latest in a series of USB Arduino boards, and the reference model for the Arduino platform

5.1.1 Device Overview

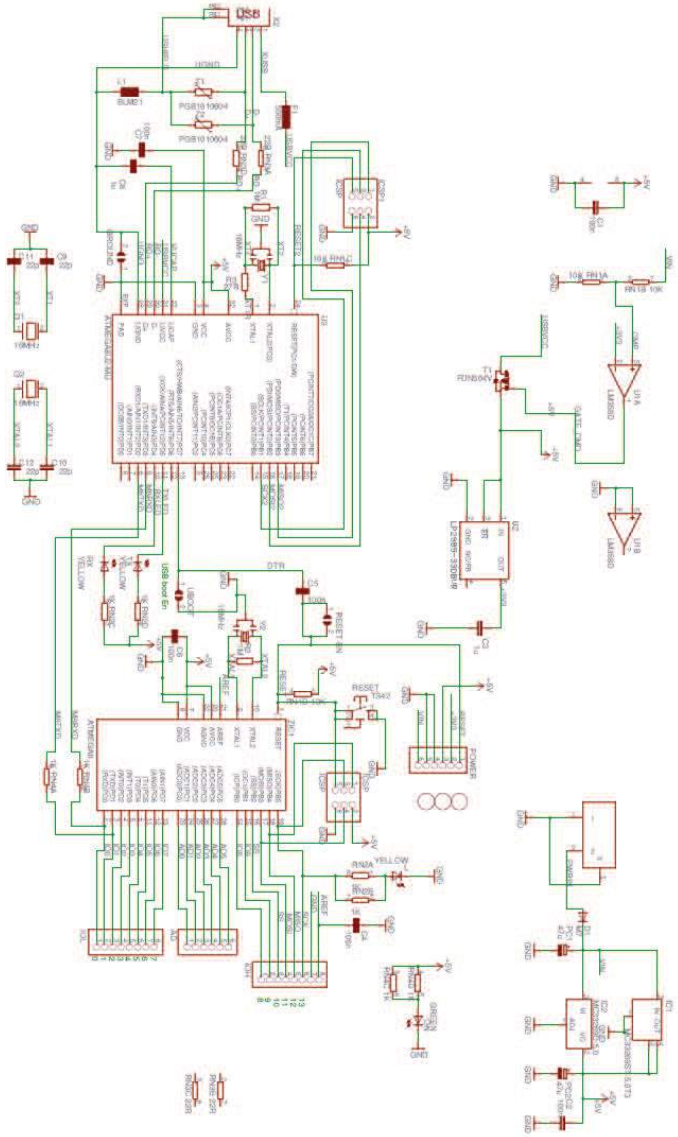

Figure 5.2: Arduino Uno Functional Block Diagram

5.1.2 Technical Specifications

- Microcontroller : ATmega328
- Operating Voltage : 5V
- Input Voltage (recommended) : 7-12V
- Input Voltage (limits) : 6-20V
- Digital I/O Pins : 14 (of which 6 provide PWM output)
- Analog Input Pins : 6
- DC Current per I/O Pin : 40 mA
- DC Current for 3.3V Pin : 50 mA
- Flash Memory : 32 KB of which 0.5 KB used by bootloader
- SRAM : 2 KB
- EEPROM : 1 KB
- Clock Speed : 16 MHz

5.1.3 Power

The Arduino Uno can be powered via the USB connection or with an external power supply. The power source is selected automatically.
External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The power pins are as follows:

- **VIN** : The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.
- **5V** : The regulated power supply used to power the microcontroller and other components on the board. This can come either from VIN via an on-board regulator, or be supplied by USB or another regulated 5V supply.
- **3V3** : A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.
- **GND**: Ground pins.

5.1.4 Memory

The Atmega328 has 32 KB of flash memory for storing code (of which 0,5 KB is used for the bootloader); It has also 2 KB of SRAM and 1 KB of EEPROM .

5.1.5 Input And Output

Each of the 14 digital pins on the Uno can be used as an input or output, using pinMode(), digitalWrite(), and digital Read() functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial:** 0 (RX) and 1 (TX) : Used to receive (RX) and transmit (TX) TTL serial data. TThese pins are connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip .
- **External Interrupts:** 2 and 3 :These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value.
- **PWM**: 3, 5, 6, 9, 10, and 11. Provide 8-bit PWM output with the analogWrite() function.
- **SPI:** 10 (SS), 11 (MOSI), 12 (MISO), 13 (SCK) : These pins support SPI communication, which, although provided by the underlying hardware, is not currently included in the Arduino language.
- **LED: 13 :** There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

The Uno has 6 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the AREF pin and the analog Reference() function. Additionally, some pins have specialized functionality

- **I2C: 4 (SDA) and 5 (SCL)** : Support I2C (TWI) communication using the Wire library.

There are a couple of other pins on the board:

- **AREF** : Reference voltage for the analog inputs. Used with analogReference().
- **Reset :** Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

5.1.6 Communication

The Arduino Uno has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega328 provides UART TTL (5V) serial communication, which is available on digital pins 0 (RX) and 1 (TX). An ATmega8U2 on the board channels this serial communication over USB and appears as a virtual com port to software on the computer. The 8U2 firmware uses the standard USB COM drivers, and no external driver is needed. However, on Windows, an *.inf file is required.

The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the Arduino board. The RX and TX LEDs on the board will flash when data is being transmitted via the USB-to serial chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A Software Serial library allose for serial communication on any of the Uno's digital pins. The ATmega328 also support I2C (TWI) and SPI communication.

5.1.7 Programming

The Arduino Uno can be programmed with the Arduino software . Select "Arduino Uno w/ ATmega328" from the **Tools** > **Board** menu . For details see the reference and tutorials.

The ATmega328 on the Arduino Uno comes preburned with a bootloader that allows to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol (reference, C header files).

Bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header. The ATmega8U2 firmware source code is available . The ATmega8U2 is loaded with a DFU bootloader, which can be activated by connecting the solder jumper on the back of the board and then resetting the 8U2.

5.1.8 Automatic (Software) Reset:

Rather than requiring a physical press of the reset button before an upload, the Arduino Uno is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2 is connected to the reset line of the ATmega328 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.

This setup has other implications. When the Uno is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Uno. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.

The Uno contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN".

5.1.9 USB Overcurrent Protection

The Arduino Uno has a resettable polyfuse that protects your computer's USB ports from shorts and over current. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

5.1.10 Physical Characteristics

The maximum length and width of the Uno PCB are 2.7 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Three screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16”), not an even multiple of the 100 mil spacing of the other pins.

Chapter 6

Simulation Results

The simulation based on the Instantaneous Reactive Power theory and Fryze current computation technique is being carried out using Matlab/Simulink. The simulation model consists of a three phase voltage supply followed by a three Phase diode bridge rectifier followed a R-L load. Simulation Results are carried out by

V=415 V

R = 1 Ω

L= 0.00003 H

Proportional gain of PI = 0.1

6.1 Instantaneous Reactive Power Theory

Using Instantaneous Reactive Power Theory , there is produce the Reference compansating current. Here in this theory there is use P-Q theory. By using P-Q Theory convert three phase (a,b,c) in (α, β). So the tolal time require for complete for the system is reduced.

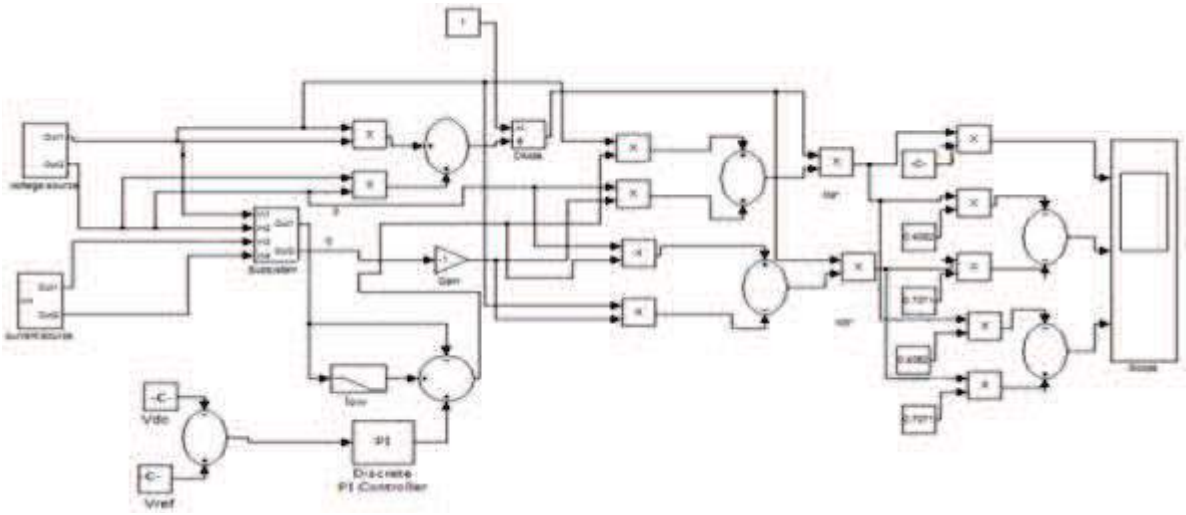

Figure 6.1: Model of Instantaneous Reactive Power Theory

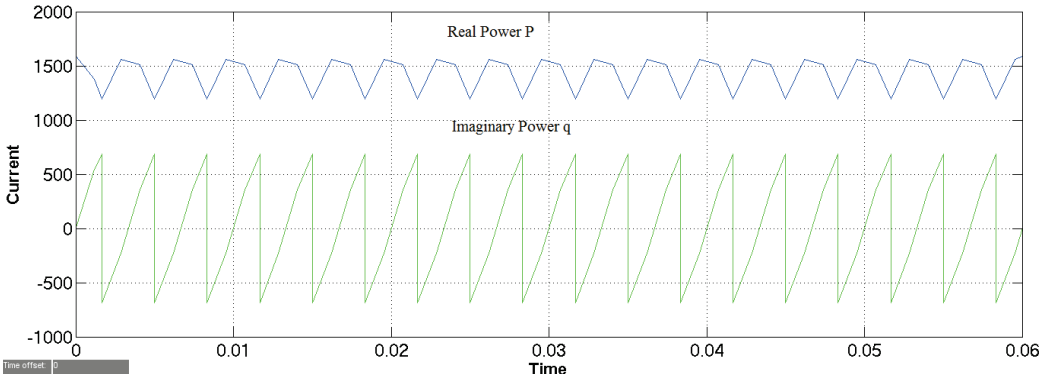

Figure 6.2: Upper:Real power P, Lower:Imaginary power Q [Scale:X-axis:0.01 s, Y-axis: 1.00 A/div]

The reference compensating currents obtained with this method are shown in Figure:-

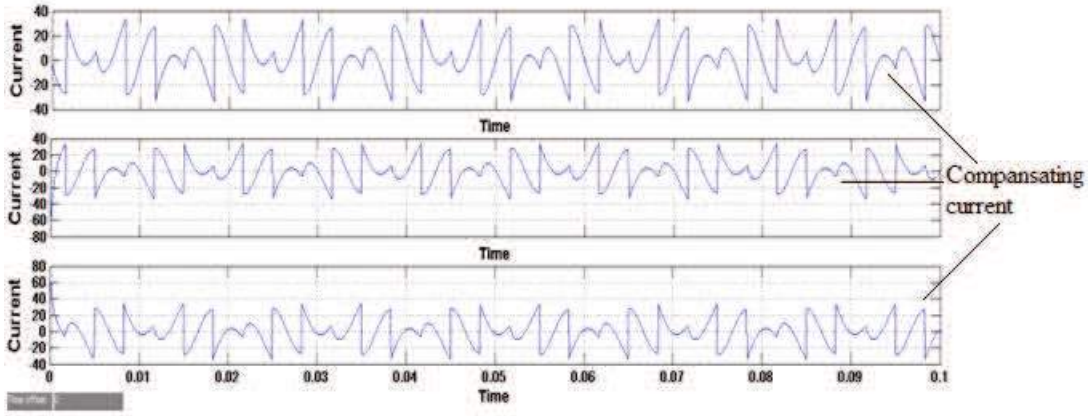

Figure 6.3: Reference compensating currents [Scale:X-axis:0.01 s, Y-axis: 20 A/div]

The result of I_{la}-$I_{ca}*$ is shown in figure:-

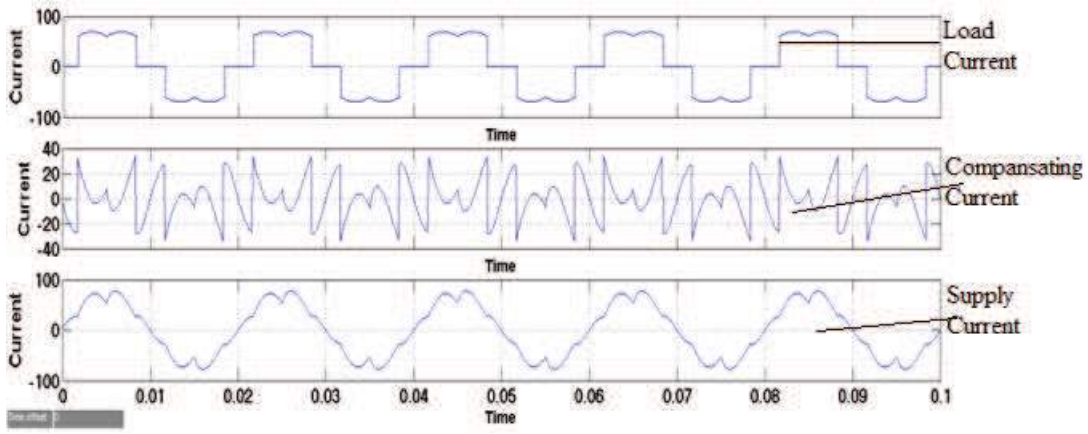

Figure 6.4: Upper Trace: I_{la}, Middle Trace:$I_{ca}*$, Lower Trace:$I_{la} - I_{ca}*$[Scale:X-axis:0.01 s, Y-axis:200 A/div]

The FFT plot of the source current so obtained is shown in figure:-

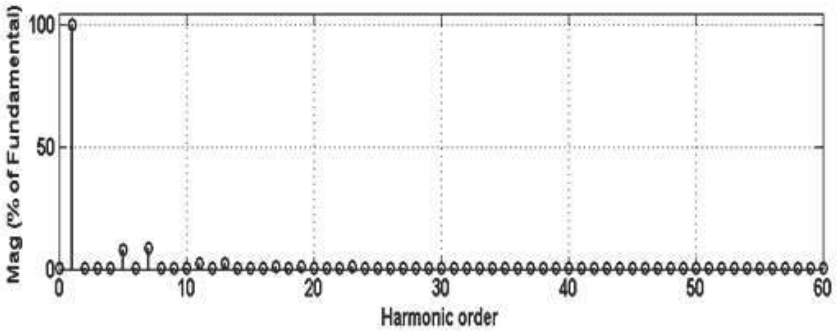

Figure 6.5: FFT of reactive power

6.2 Three-level neutral point clamped inverter

Here Simulation Results are carried out at R = 10 Ω and L= 100e-3 H.

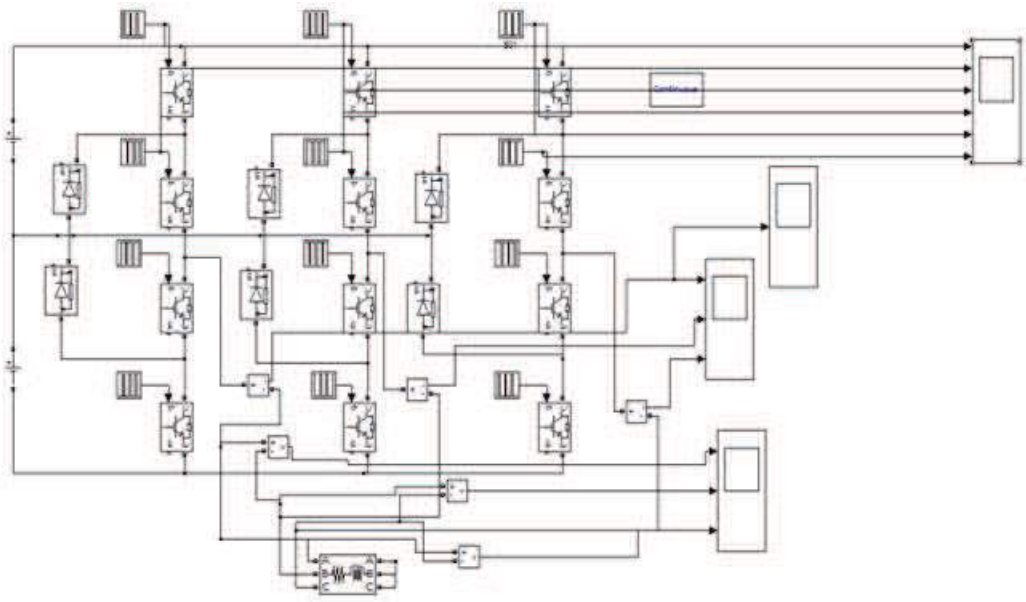

Figure 6.6: 3-level Neutral Point Clamped Inverter

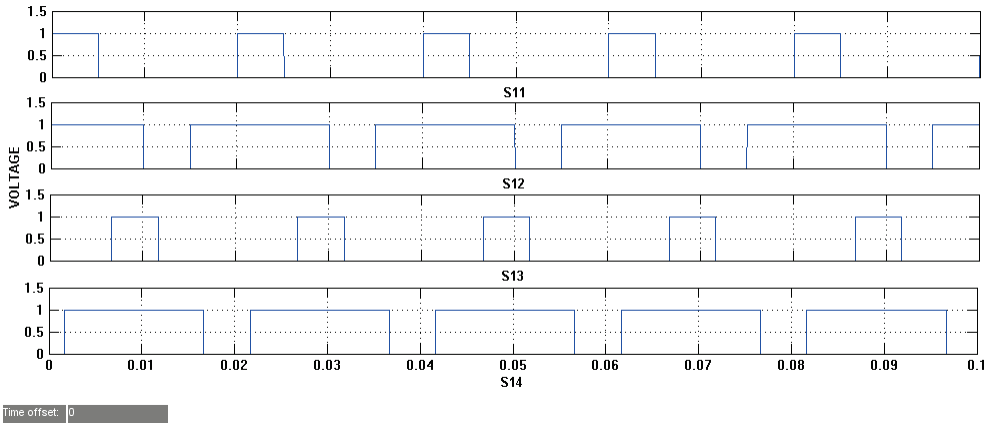

Figure 6.7: Gate pulses for 1-phase of inverter [Scale:X-axis:0.01 ms, Y-axis: 1 V/div]

Here Gate pulses for single phase of inverter shown in fig 6.7. Here Switches S_{11} and S_{13} are complementary. And S_{12} and S_{14} are complementary.

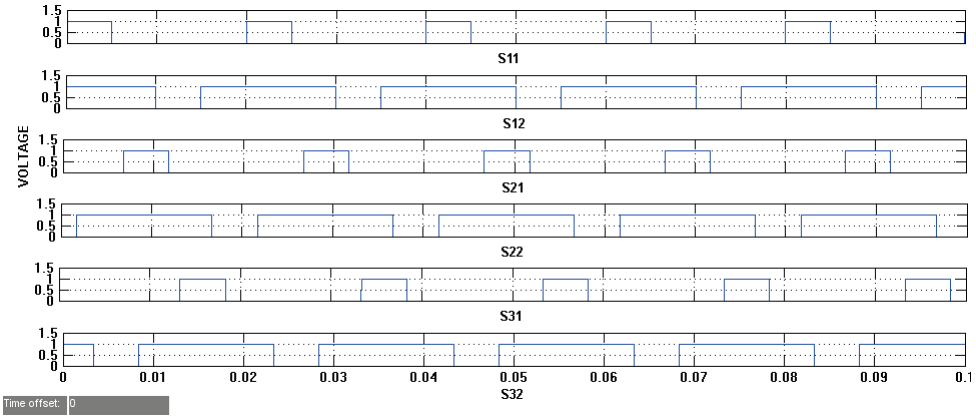

Figure 6.8: Gate pulse for 3-phase 3-level inverter inverter [Scale:X-axis:0.01 s, Y-axis: 1 V/div]

Here shown that switching Of upper switches. The lower switches are complementary of upper switches.

The output result line voltage waveform is given by:-

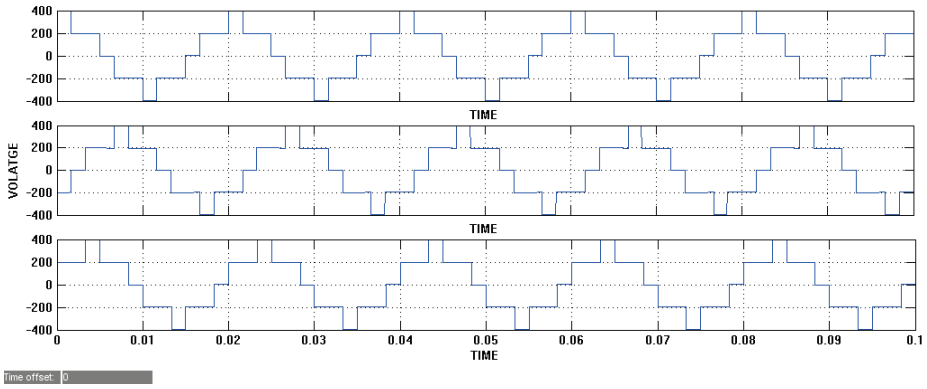

Figure 6.9: Line voltage for 3 level inverter[Scale:X-axis:0.01 s, Y-axis: 200 V/div]

6.3 Hysteresis Current Controller Using IRP

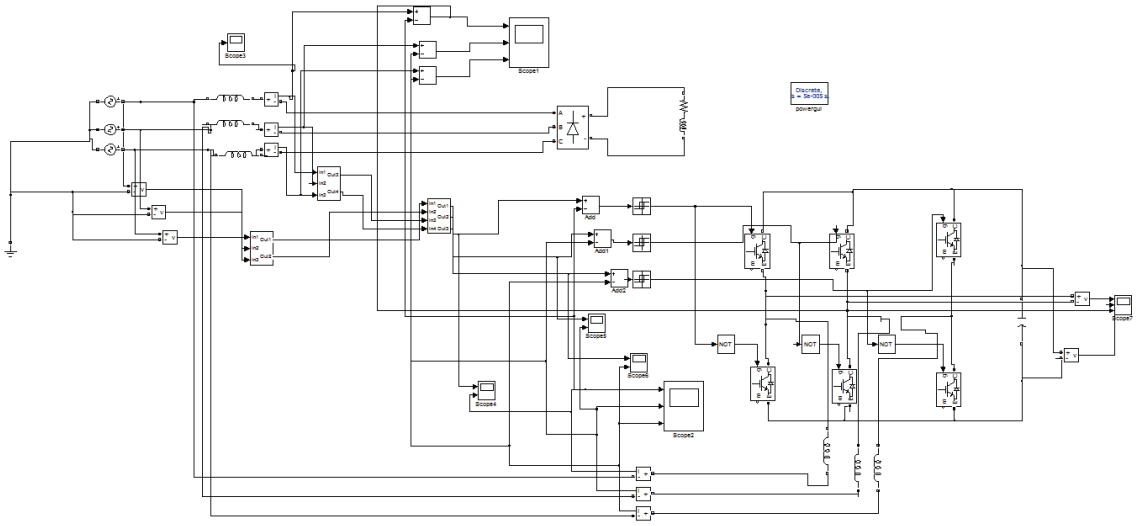

Figure 6.10: Simulink Model Of Hysteresis Current Controller Using IRP

Now when comparing actual current to the Reference current then the error is generated and it go through the hysteresis loop. Here in hysteresis ,the limit is fixed. When error is touch upper limit then lower switch is on. When error touch lower band then the upper switch is turn on. So the error will not go outside of the limit. So the error moves in fixed limit. Here switching time is less so the switching frequency is more. Compensating current using hysteresis current controller is given as per fig 6.11.

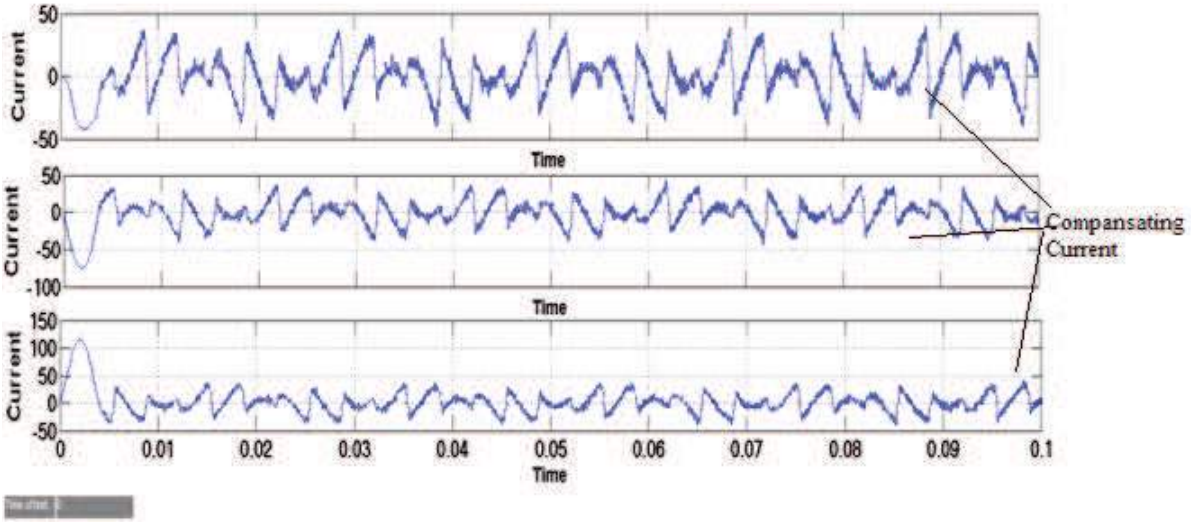

Figure 6.11: Compensating current using HCC [Scale:X-axis:0.02 s, Y-axis: 50 A/div]

When the compansating current injects 180_0 phase shift with the nonlinear load current to the PCC then it compansats and reduce the harmonics of load current. So the source current is non-linear before compensated is now nearly sinusoidal. Due to this the total harmonic distortion is reduced. So the losses reduced and efficiency is increased.

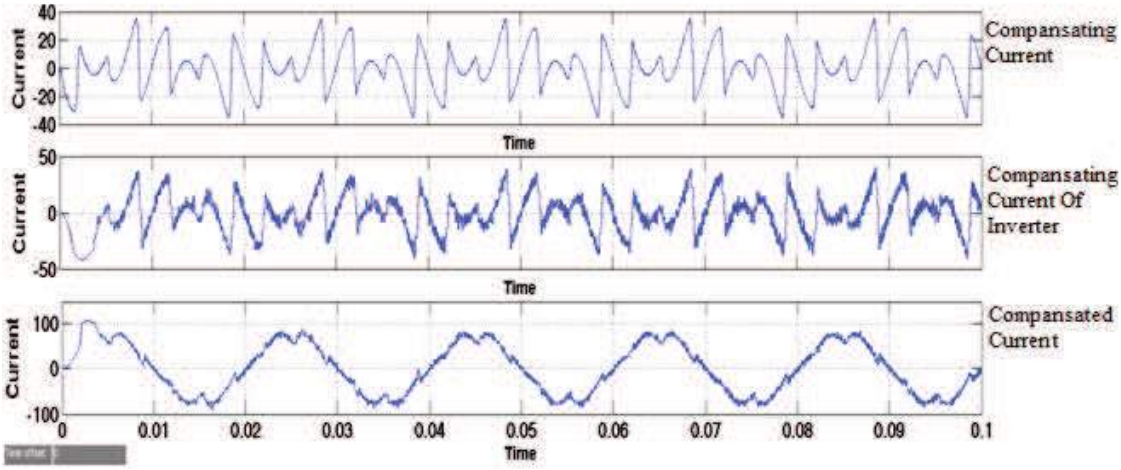

Figure 6.12: Upper Trace: I_{la}, Middle Trace: $I_{ca}*$, Lower Trace : I_{sa}=I_{la}-$I_{ca}*$[Scale:X-axis:0.02 s, Y-axis: 50 A/div]

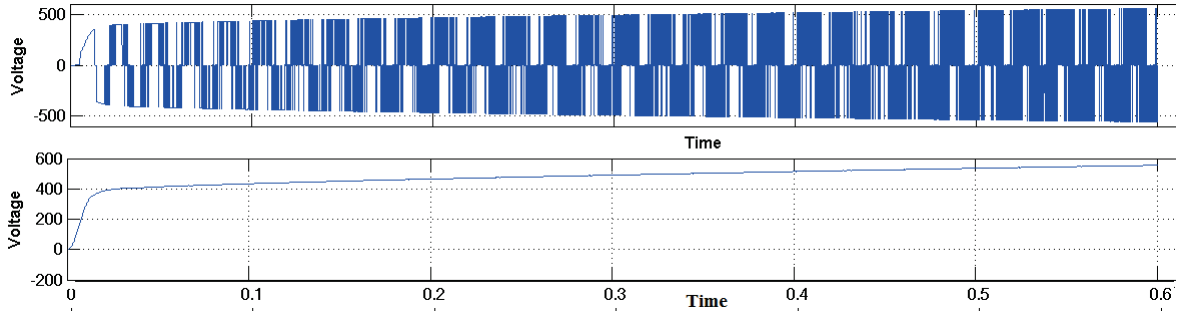

Figure 6.13: Upper Trace: Line Voltage Of Inverter, Lower Trace : DC link Capacitor Voltage[Scale:X-axis:0.1 s, Y-axis: 200 A/div]

6.4 Fryze current computation method

The fryze power theory active power filter is like line conditioning. The reference currents are extracted using Fryze power theory method. The reference compensating

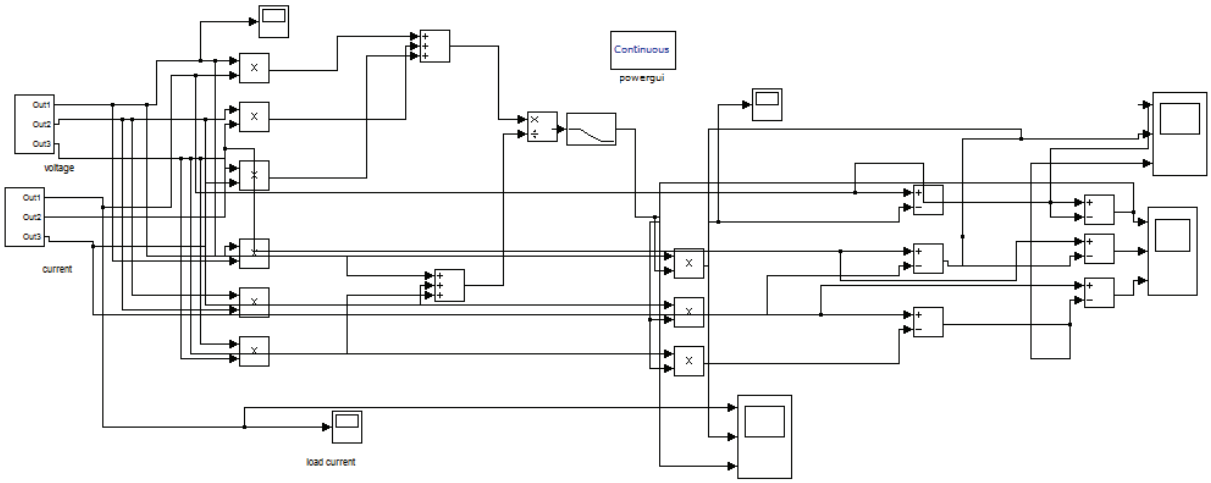

Figure 6.14: Model of Fryze current computation method

currents obtained with this method are shown in Figure:-

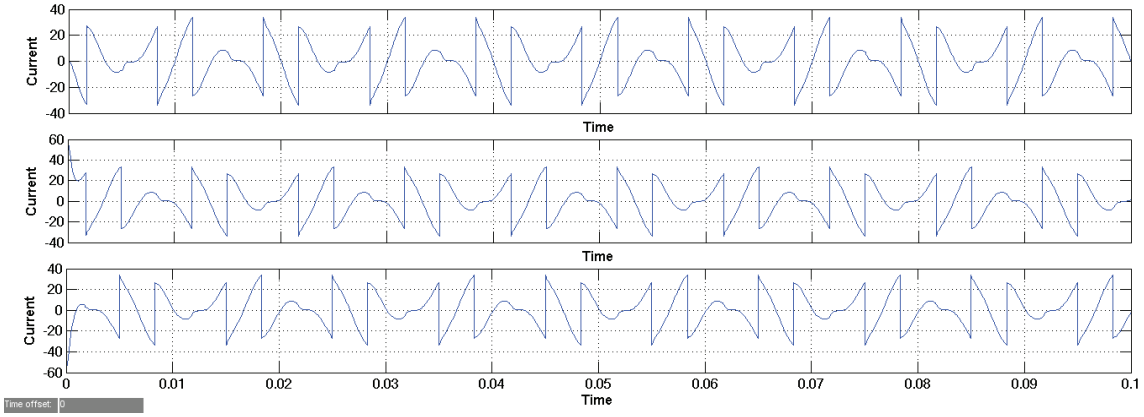

Figure 6.15: Reference compensating currents[Scale:X-axis:0.01 s, Y-axis: 20 A/div]

The result of I_{la}-$I_{ca}*$ is shown in figure:-

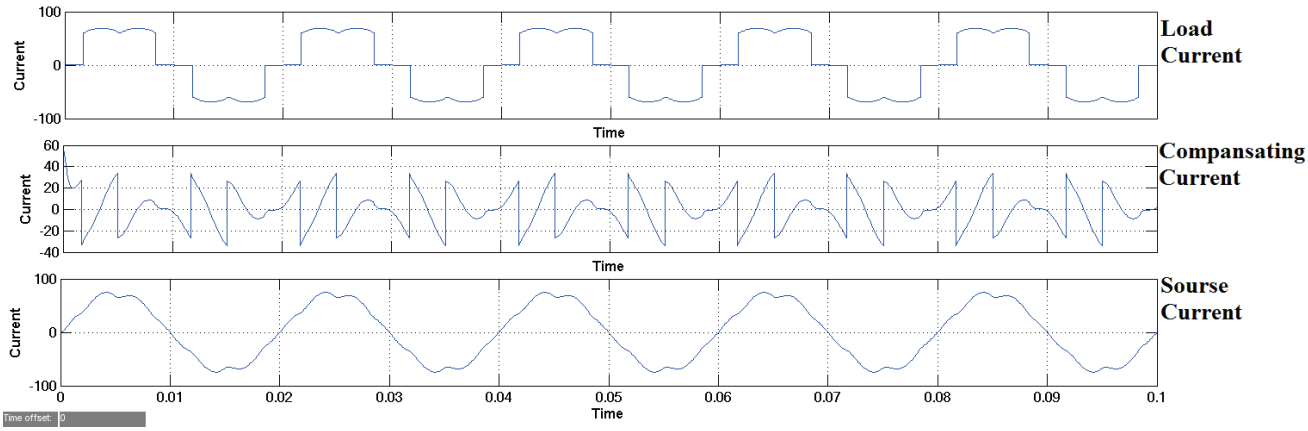

Figure 6.16: Upper:Ila, Middle: I*ca, Lower : Ila-I*ca [Scale:X-axis:0.01 s, Y-axis: 50 A/div]

The FFT plot of the source current so obtained is shown in figure:-

It was found that the THD was 6.49 according to the simulation carried out using the Instantaneous Reactive Power Theory.

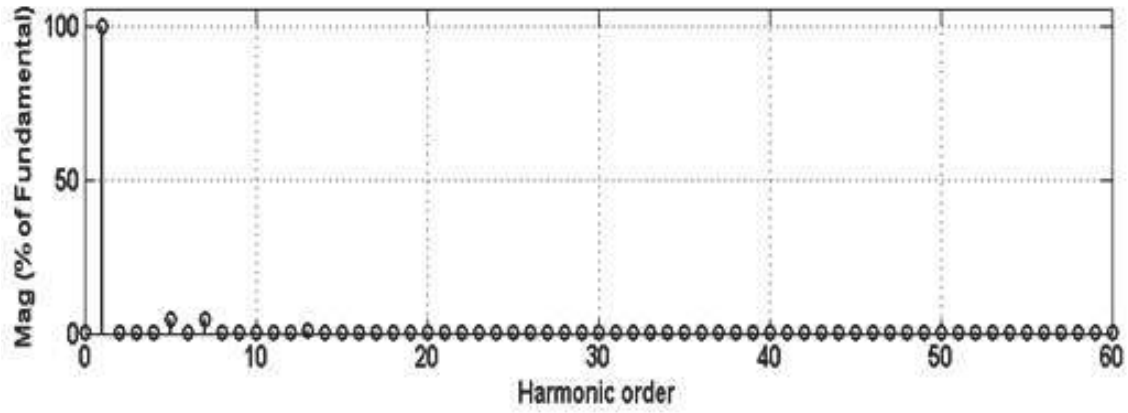

Figure 6.17: FFT analysis

6.5 Hysteresis Current Controller Using Fryze Current Computation Method

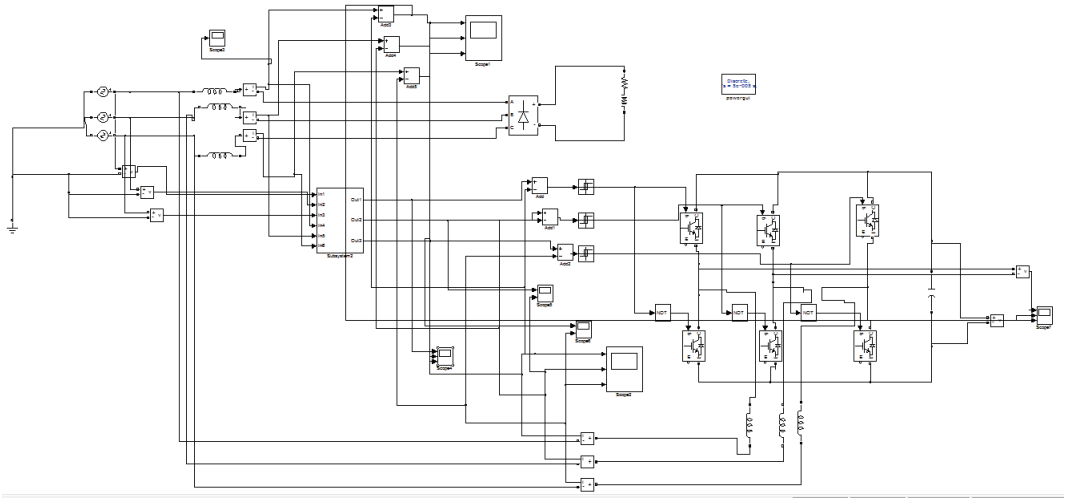

Figure 6.18: HCC Using Fryze Theory

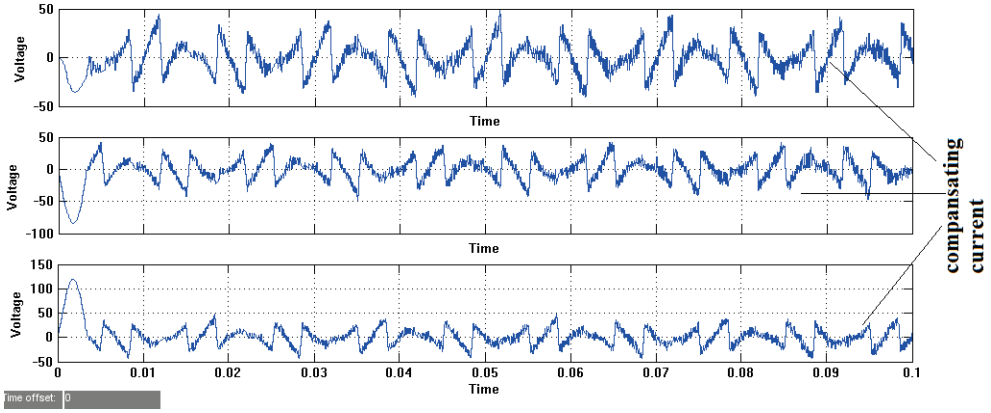

Figure 6.19: Compensating current using HCC [Scale:X-axis:0.01 s, Y-axis:20 A/div]

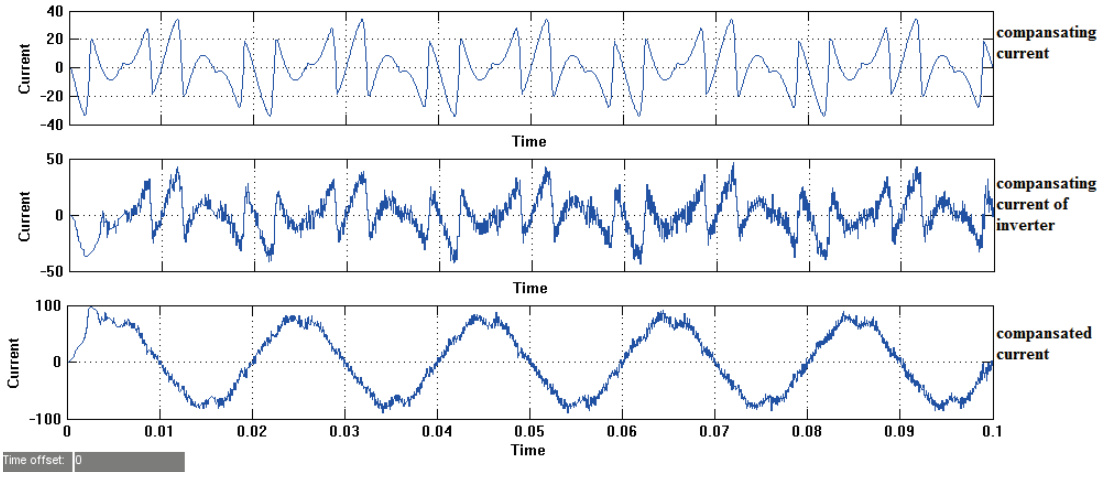

Figure 6.20: Upper Trace: I_{la}, Middle Trace: $I_{ca}*$, Lower Trace : I_{sa}=I_{la}-$I_{ca}*$,[Scale:X-axis:0.01 s, Y-axis:20 A/div]

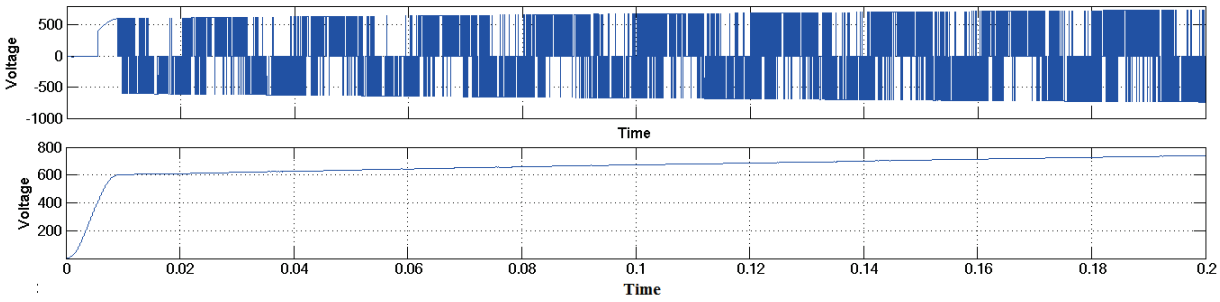

Figure 6.21: Upper Trace: Line Voltage Of Inverter, Lower Trace : DC link Capacitor Voltage[Scale:X-axis:0.1 s, Y-axis: 200A/div]

Chapter 7

Hardware Results

7.1 12V DC Source

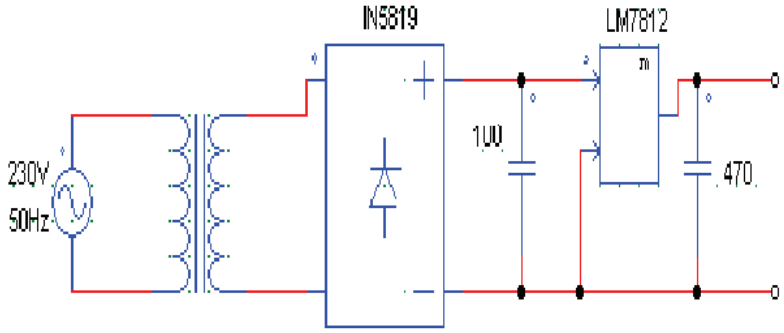

Figure 7.1: Circuit diagram for 12V DC source

CIRCUIT DESCRIPTION:

- 230V/14V step down transformer
- IN5819 bridge rectifier
- LM 7812 voltage regulator
- 100F,470F capacitor

FEATURES OF LM7812 :

- Output Current up to 1 A
- Output Voltages: 5, 6, 8, 9, 10, 12, 15, 18, 24 V
- Thermal Overload Protection
- Short-Circuit Protection
- Transistor Safe Operating Area Protection

7.2 Driver Circuit Using TLP 250

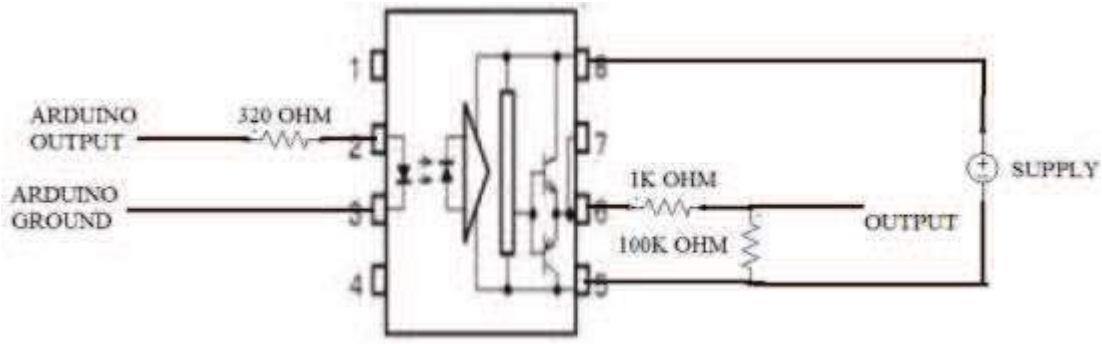

Figure 7.2: Diagram of driver circuit

Here pin 2 is connected to arduino output pin from which pwm signal is generated. A resistance of 320 ohm is connected in series with pin 2 to limit the current. Pin 3 is connected to arduino ground. Pin 1, pin 4, pin 7 is not connected. Supply is connected across pin 8 and pin 5. From pin 6 output is taken. A resistance of 1 Kohm is connected in series with pin 6 to limit the current. A pull up resistance of 100 Kohm is connected across pin 6 and pin 5.

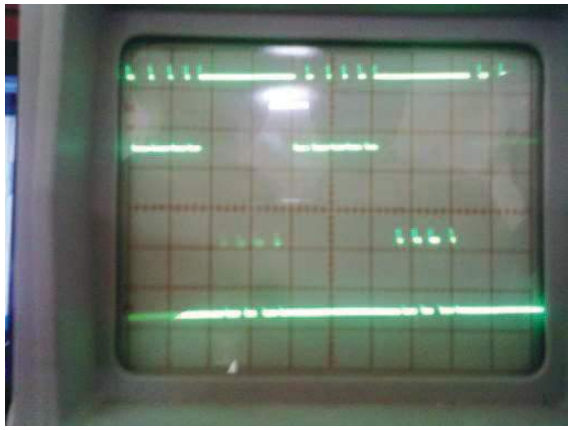

Figure 7.3: Output of driver circuit with high amplification[Scale:X-axis:10 ms, Y-axis:5 V/div]

Here pulses of controller is given to the TPL250 then the output is taken out as per results.It is purely square.

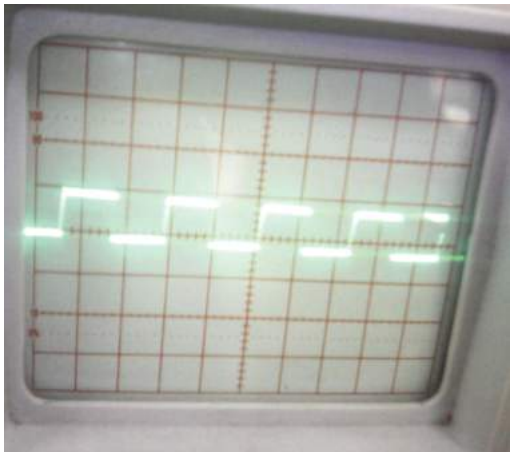

Figure 7.4: Output of driver circuit using TLP250 [Scale:X-axis:10 ms, Y-axis:5 V/div]

7.3 FABRICATION OF 3 LEVEL INVERTER

FEATURES OF MUR860

- Ultrafast Recovery t_{rr} = 70 ns (@ IF = 8 A)
- Max Forward Voltage,V_F = 1.5 V (@T_C4= 25C)
- 400 V, 600 V Reverse Voltage and High Reliability
- Avalanche Energy Rated
- RoHS Compliant

FGA25N120ANTD IGBT

- V_{CES} Collector-Emitter Voltage= 1200 V
- V_{GES}Gate-Emitter Voltage=±20 V
- I_CCollector Current @ TC = 25∘C 50 A
- I_C Collector Current @ TC = 100∘C 25 A
- RoHS Compliant

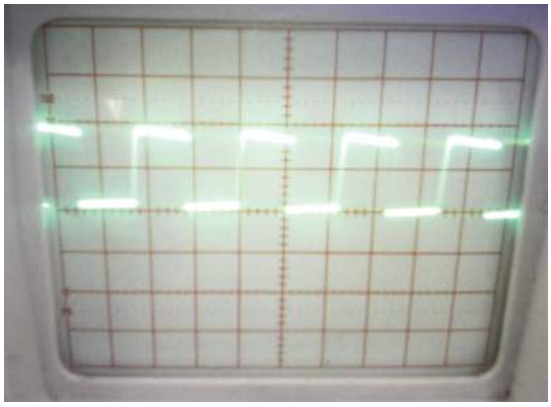

Figure 7.5: Output of inverter for upper two switches [Scale:X-axis:10 ms, Y-axis:5 V/div]

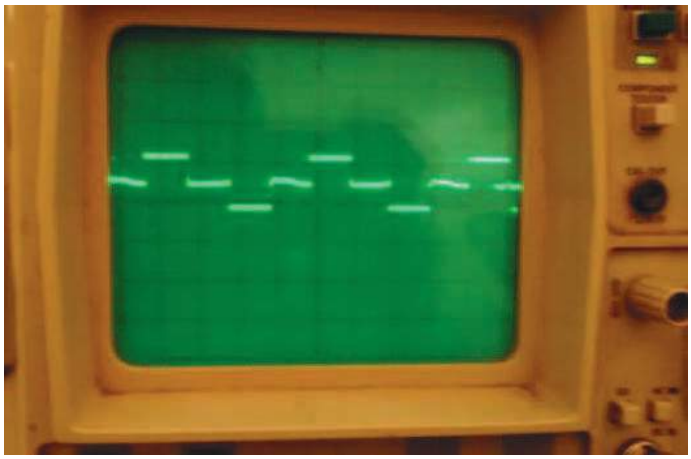

Figure 7.6: Output of phase voltage with 6V dc link voltage of inverter [Scale:X-axis:10 ms, Y-axis:5 V/div]

7.4 FLOW CHART OF CONTROLLER

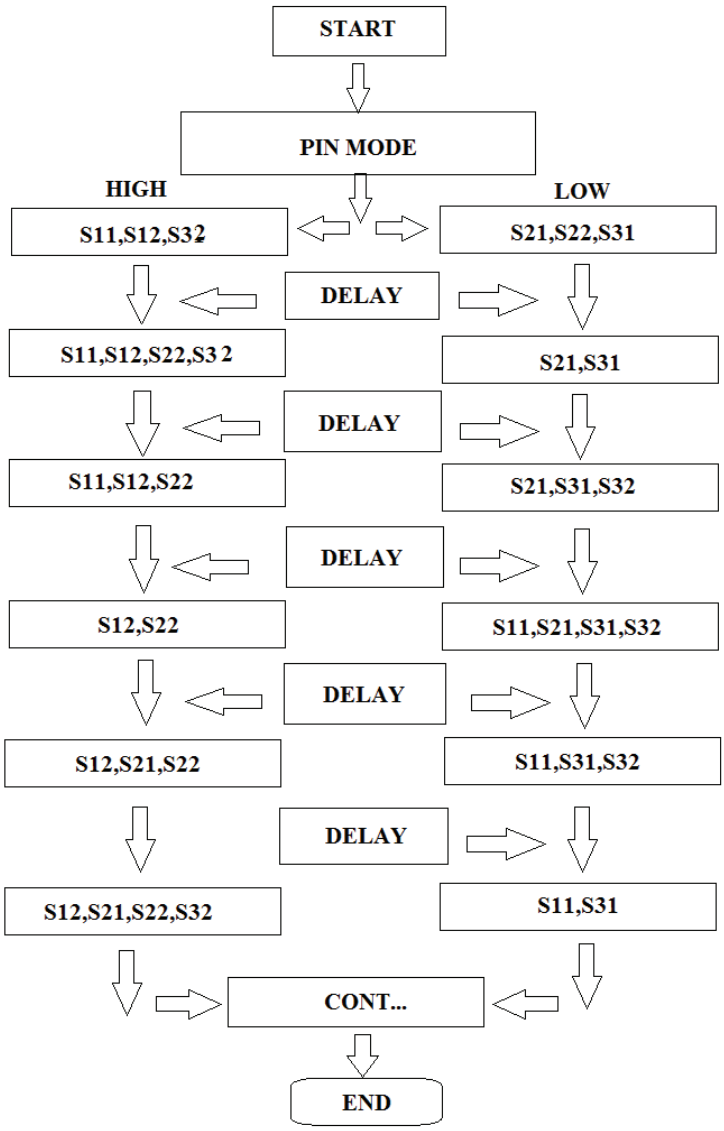

Figure 7.7: Flow chart of controller

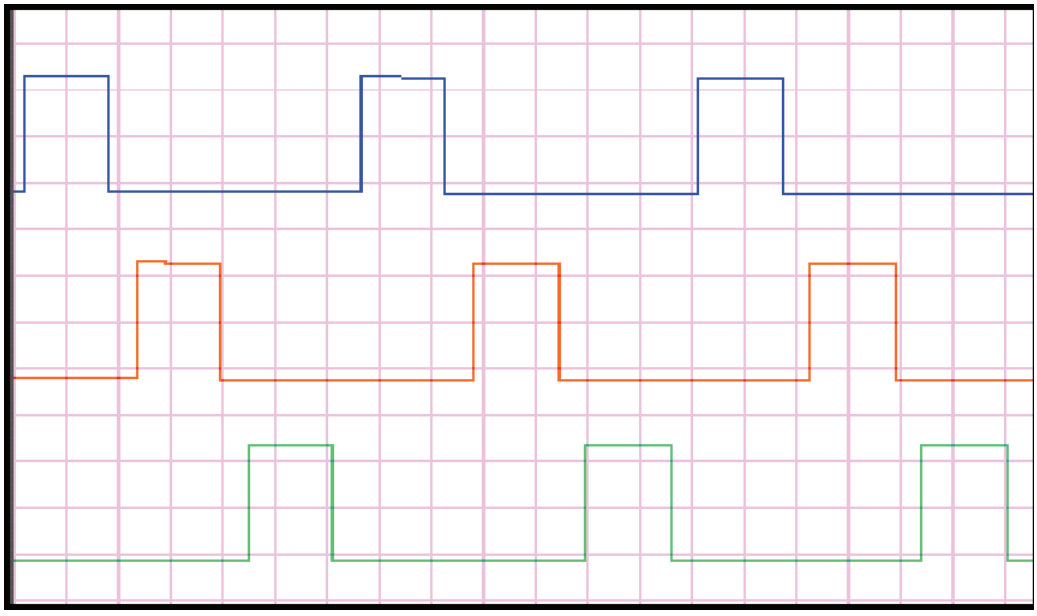

Figure 7.8: PWM pulse for upper switches

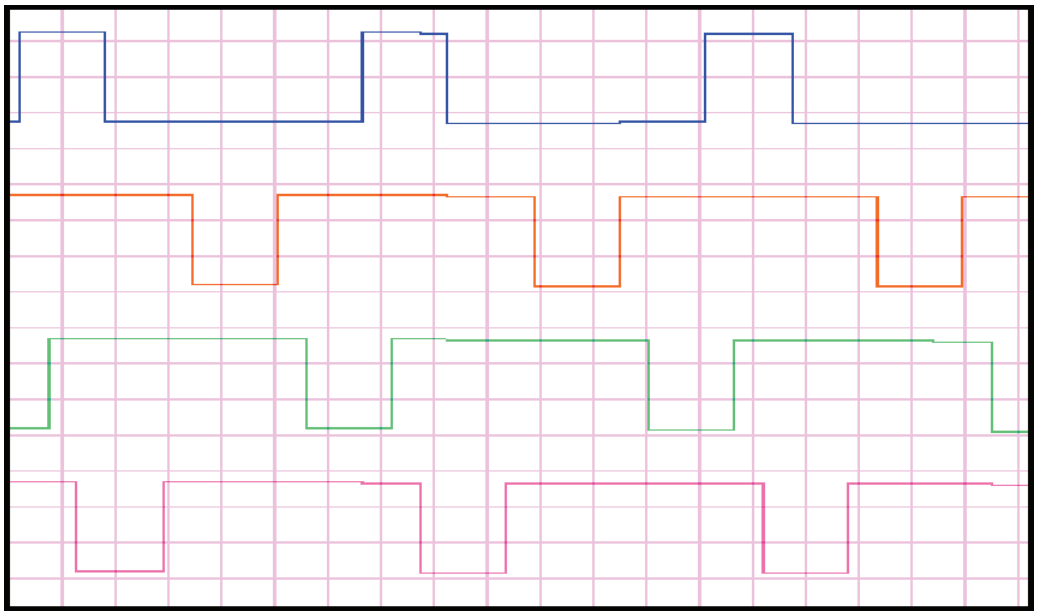

Figure 7.9: PWM pulse in proteus software

Chapter 8

Conclusion And Future Work

8.1 Conclusion

Power quality is the major problems with the domestic as well as industrial loads. Due to the non-linear loads,there is present harmonics in the current and voltage waveforms. By this problems the losses are increase and efficiency is decrease. So there is need to improvement of the power quality to compensation of voltage and current. The harmonic current compensation is done by generating reference current and using active shunt filter. Here strategy implemented is the Instantaneous Reactive Power and Fryze current computation method. By using these methods ,here generating reference compensating current. The reference compensating current is given to the load current at PCC to 180^o phase shift. Then the harmonics are reduced and the overall efficiency is increased. Here three level Voltage source inverter is used as shunt active power filter. Here three level inverter hardware and all the setup is simulated, implementation using controller and results carried out.

8.2 Future Work

Using 3-level inverter and suitable current control technique and different experimental analysis can be done on Shunt Active Power Filter by developing model.

References

1 Muhammad H. Rashid"POWER ELECTRONICS HANDBOOK DEVICES, CIRCUITS, AND APPLICATIONS"

2 H. Akagi, Edson Hirokazu,mauricio Aredes "Instantanious Power Theory And Applications To Power Conditioning"

3 Y. Kanazawa, H. Akagi and A. Nabae, "Instantaneous Reactive Power Compensator Comprising Switching Devices Without Energy Storage Components", IEEE Transactions Industrial Applications, Vol. IA-20, no. 3, pp. 625 - 630.

4 M. J. Sepulveda Freitas, Joao L. Afonso and Julio S. Martins, "P-Q Theory Power Components Calculations", IEEE International Symposium on Industrial Electronics, ISIE 2003, ISBN: 0-7803-7912-8.

5 VIKASH ANAND,Dr. S. K. SRIVASTAVA "Performance Investigation of Shunt Active Power Filter Using Hysteresis Current Control Method"International Journal of Engineering Research Technology (IJERT) Vol. 1 Issue 4, June - 2012 ISSN: 2278-0181.

6 C. N. Bhende, S. Mishra and S. K. Jain "TS-Fuzzy-Controlled Active Power Filter for Load Compensation" IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 21, NO. 3, JULY 2006.

7 Jose Rodriguez, Steffen Bernet,Peter K. Steimer, Fellow, and Ignacio E. Lizama "A Survey on Neutral-Point-Clamped Inverters" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 57, NO. 7, JULY 2010.

8 Jos Rodrguez, Jih-Sheng Lai,and Fang Zheng Peng," Multilevel Inverters: A Survey of Topologies,Controls, and Applications" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 4, AUGUST 2002.

9 Oleg Vodyakho, Taehyung Kim and Sangshin Kwak "Three-Level Inverter Based Active Power Filter for the Three-Phase, Four-Wire System" 2008 IEEE.

10 Shweta Gautam,Rajesh Gupta, Member "Three-level Inverter based Shunt Active Power Filter using Generalized Hysteresis Current Control Method",2010 IEEE.

11 Mehmet Ucar ,Engin Ozdemir, Murat Kale "An Analysis of Three-phase Four-Wire Active Power Filter for Harmonic Elimination Reactive Power Compensation and Load Balancing Under Non-Ideal Mains Voltage" 2004 35th Annual IEEE Power Elecrronics Specialisrs Conference Aachen, Germany, 2004.

12 Karuppanan P, Kamala Kanta Mahapatra, Jeyaraman.K and Jeraldine Viji "Fryze Power Theory with Adaptive-HCC based Active Power Line Conditioners" International Conference on Power and Energy Systems (ICPS) , Dec 22 - 24, 2011, IIT-Madras.

13 Karuppanan P, Saswat Kumar Ram, Kamala Kanta Mahapatra "Three Level Hysteresis Current Controller based Active Power Filter for Harmonic Compensation" ICETECT 2011.

14 Yangle Ping, Alian Chen, Chenghui Zhang "A Novel Adaptive Hysteresis Band Current Control Method for Three-level Based Active Power Filter" 2012 IEEE 7th International Power Electronics and Motion Control Conference -ECCE Asia June 2-5, 2012.

15 Murat Kale*, Engin Ozdemir "An adaptive hysteresis band current controller for shunt active power filter" Electric Power Systems Research 73 (2005) 113119.

16 R. Davoodnezhad, D.G Holmes, B.P McGrath "Three-Level Hysteresis Current Regulation for a Three Phase Neutral Point Clamped Inverter"15th International Power Electronics and Motion Control Conference, EPE-PEMC 2012 ECCE Europe, Novi Sad, Serbia

17 Yangle Ping, Alian Chen, Chenghui Zhang "A Novel Adaptive Hysteresis Band Current Control Method for Three-level Based Active Power Filter" 2012 IEEE 7th International Power Electronics and Motion Control Conference - ECCE Asia June 2-5, 2012 .

18 Nitin Gupta and S. P. Singh, S. P. Dubey "Fuzzy logic controlled shunt active power filter for reactive power compensation and harmonic elimination" International Conference on Computer Communication Technology (ICCCT)-2011.

19 S. Srikanthan M.K. Mishra R.K.V. Rao,"Improved hysteresis current control of three-level inverter for distribution static compensator application"IET Power Electron., 2009, Vol. 2, Iss. 5, pp. 517526 doi: 10.1049/iet-pel.2008.0126.

20 Ferhat UCAR, Resul COTELI, Besir DANDIL "Three Level Inverter Based Shunt Active Power Filter Using Multi-Level Hysteresis Band Current Controller"PRZEGLAD ELEKTROTECHNICZNY (Electrical Review), ISSN 0033-2097, R. 88 NR 11a/2012

21 Ibrahim A. Altawil Khaled A. Mahafzah "Shunt Active Power Filter Based on Diode Clamped Inverter And Hysteresis Band Current Controller" IRNet Transactions on Electrical and Electronics Engineering .

22 H. Akagi, "New Trends in Active Filters for Power Conditioning", in IEEE Trans. on Industry Applications, vol. 32, no. 6, pp. 1312-1322, Nov./Dec. 1996.

Appendix

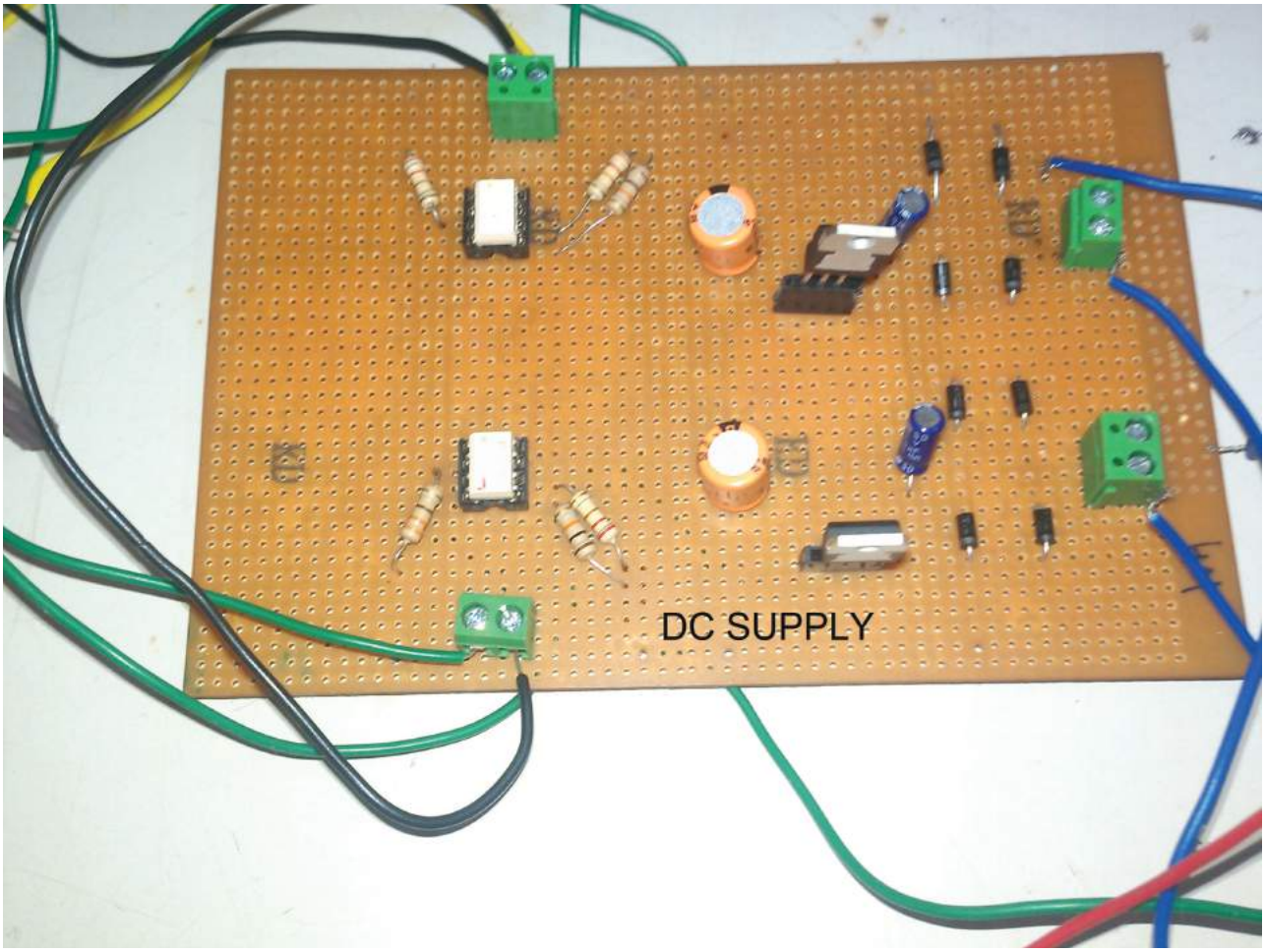

Figure 8.1: Hardware implementation of DC source

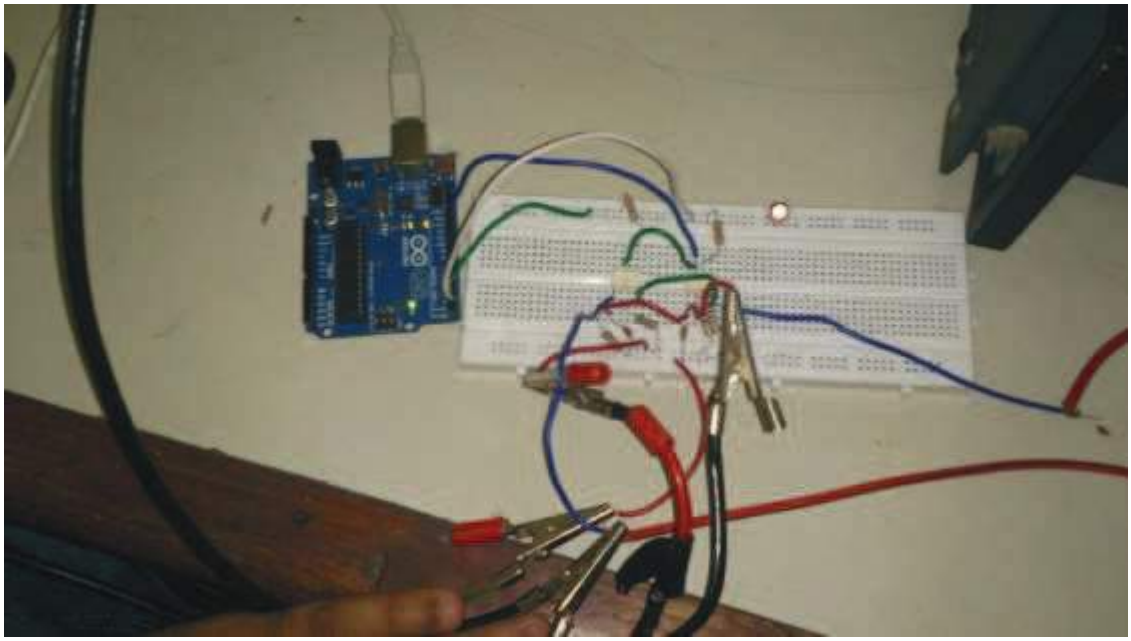

Figure 8.2: Hardware implementation of DC source

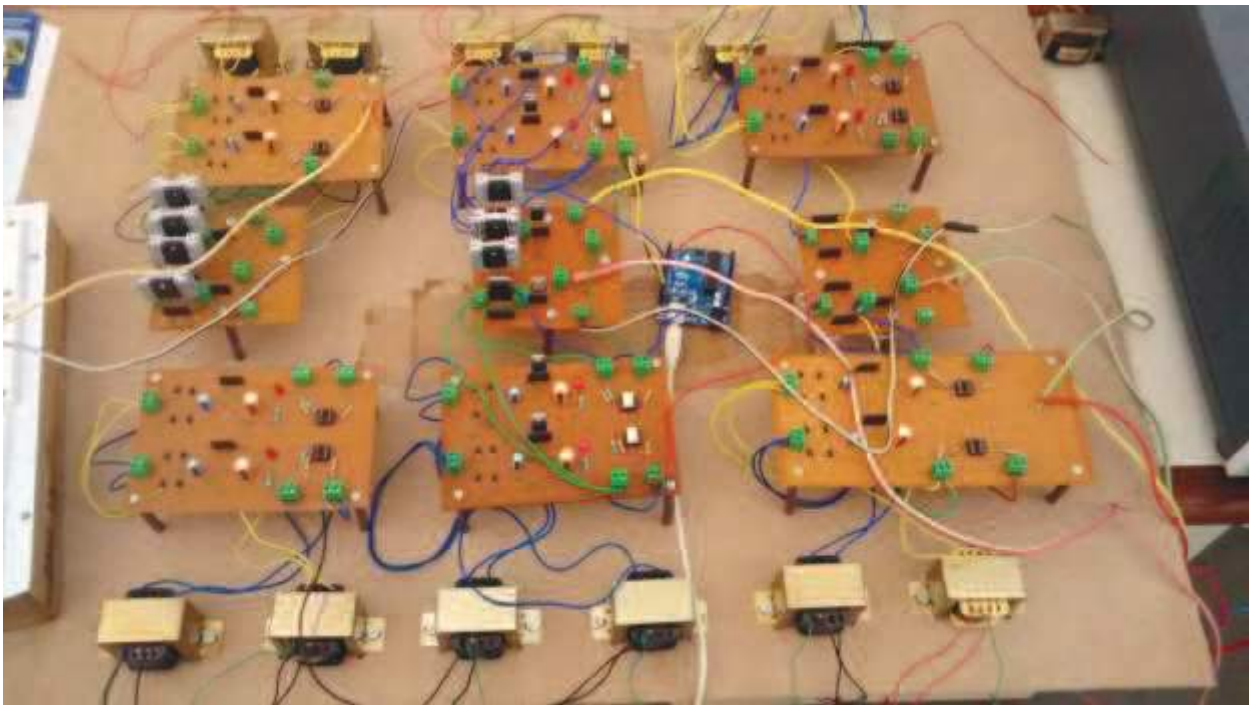

Figure 8.3: Hardware implementation three level inverter

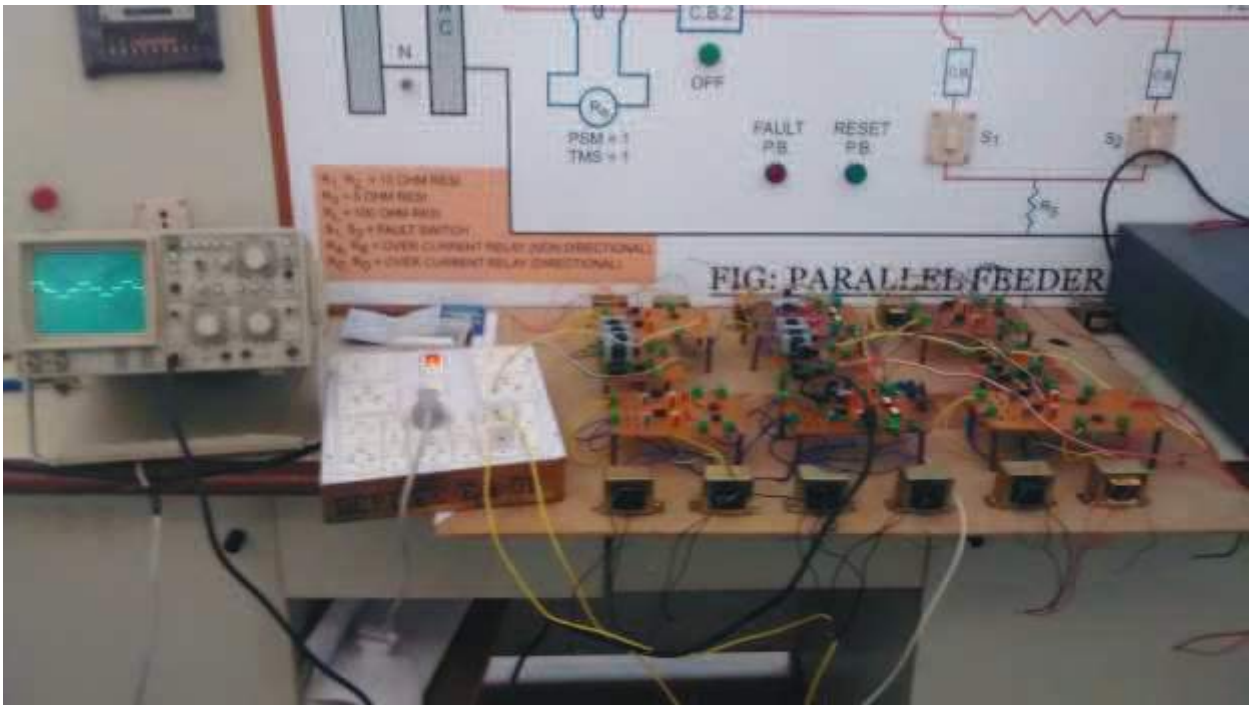

Figure 8.4: Complete Hardware implementation three level inverter