"DESIGN AND IMPLEMENTATION OF COMPACT AND ISOLATED LOW VOLTAGE HIGH CURRENT DC POWER SUPPLY USING SYNCHRONOUS RECTIFIER"

Major Project Report

Submitted in partial fulfillment of the requirements for

Degree of

Master of Technology
In
Electrical Engineering

(Power Electronics, Machines & Drives)

By

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12MEEP24

DEPARTMENT OF ELECTRICAL ENGINEERING
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MAY 2014

Certificate

This is to certify that the Major Project Report entitled **"Design and Implementation of Compact and Isolated Low-Voltage High-Current DC Power Supply using Synchronous Rectifier"** submitted by **Ms.Shah Grishma K.(12MEEP24)** towards the partial fulfillment of the requirements for the award of degree in **Master of Technology (Electrical Engineering)** in the field of **Power Electronics, Machines & Drives** of Nirma University is the record of work carried out by her under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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Dedicated to My Family...

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I **Grishma Ketankumar Shah**, Roll No. **12MEEP24**, give undertaking that the Major Project entitled **"Design and Implementation of Compact and Isolated Low-Voltage High-Current DC Power Supply using Synchronous Rectifier"** submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Power Electronics Machines** & **Drives, Electrical Engineering**, under Institute of Technology of Nirma University, Ahmedabad, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

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Acknowledgements

First of all, I would like to thank AMTECH Electronics(I) Ltd., Gandhinagar, for giving me an opportunity to perform the project under its premises and give me the industrial exposure. I express my sincere gratitude to Mr.Vinod Patel, AGM(R&D), AMTECH Electronics (I) Ltd., Gandhinagar, for his valuable guidance and co-operation. His perfectionism has made me improve many details of my work. He challenged me to find technical solutions to realistic problems. He always helped me and gives sincere advice and innovative ideas throughout the period we have worked together.

My sincere appreciation must be extended to my institute guide Dr.P.N.Tekwani, Head of Department, Department of Electrical Engineering, Nirma University for his valuable suggestions and inspiration and for allowing me to do my project work at AMTECH Electronics.

I would like to thank Mr. Bharat Pandya, Assistant Manager (R&D), for his support and advice. His extensive knowledge and helpful attitude gains my sincere admira- tion. I would also like to thank to Mr.Vijyendra Kharbikar, Mr.Parth Patel, Mr.Bhavin Bhakhtaria and Mr.Dinesh Bharada for their continual efforts and support towards my project work.

Finally I gratefully appreciate the patience, support and motivation of all my family members and friends to achieve my goal.

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Abstract

With advances in modern power electronics, Low-Voltage High-Current DC power supply is used extensively in industrial applications like arc furnace, fusion technology, arc welding etc. In conventional dissipative techniques, it has many disadvantages like lower efficiency, higher weight and size. The main aim of this project is to meet industrial needs like isolation between source and load, minimize the switching loss, high conversion efficiency, lower distortion in output voltage, current and also reduces the power supply package size using high frequency converters. Different Isolated Converter topologies such as Forward Converter, Flyback Converter, Push-Pull Converter, Half-Bridge Converter and Full-Bridge Converter, among all these topologies Phase Shifted Full-Bridge topology has been selected in order to achieve the High Power applications. In this topology PWM techniques are used for power switches, so that they are going to switch at high frequencies which results in the reduction of the size of transformer, weight and cost of the overall power supply. At a lower switching frequencies and without use of Quasi Resonant Converter, the switching losses (turn on and turn off losses) are significant part of the power losses, which reduces the efficiency and increase the size of overall Power Supply. An attractive alternative method to reduce the switching losses and improve the efficiency is that to replace the hard switching by soft switching in which zero voltage/zero current switching is used. In Low-Voltage applications, conduction loss of the diode bridge rectifier contributes significant power losses in the Power Supply compared to the synchronous rectifier. Feed forward technique has been adapted to minimize the output ripple from the DC link. The simulation of whole system was done in PSIM software and along with DLL block. After examining the simulation results the whole scheme implemented in hardware. The simulation of 900 W and 15 kW DC Power Supply was carried out and hardware of 900 W Prototype DC Power Supply was implemented. The 15 kW High Frequency Transformer is designed and prepared.

Abbreviation

ADC ..... Analog to Digital Converter
DSP ..... Digital Signal Processor
EMI ..... Electromagnatic Interference
IGBT ..... Insulated Gate Bipolar Transistor
MOSFET ..... Metal Oxide Semiconductor Field Effect Transistor
PWM ..... Pulse Width Modulation
PI ..... Proportional Integral
QRC ..... Quasi Resonant Converter
SMPS ..... Switched Mode Power Supply
VSI ..... Voltage Source Inverter
ZVS ..... Zero Voltage Switching

NOMENCLATURE

a_p ..... area of primary winding
a_s ..... area of secondary winding
a_t ..... area of tersary winding
A_c ..... Area of Core
A_w ..... Area of Window
A_p ..... Area of Product
B_m ..... Maximum flux density
C_{oss} ..... IGBT's output Capacitances
C_R ..... Resonant Capacitance
C_{XFMR} ..... Transformer Capacitance
D ..... Duty cycle
F_s ..... Switching Frequency
F_{RES} ..... Resonance frequency
I_{IN} ..... Input Current
I_o ..... Output Current
I_p ..... Transformer Primary Current
J ..... Current Density
K_w ..... Window utilization factor
L_R ..... Resonant Inductor
N_p ..... Number of primary turns
N_s ..... Number of secondary turns
P_o ..... Output Power
P_{IN} ..... Input Power
P_{Lcu} ..... Cu loss
P_{Lcore} ..... Core loss
V_d ..... Diode Voltage Drop
V_{IN} ..... Input Voltage
V_o ..... Output Voltage
η ..... Efficiency

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 General Overview

DC Power supplies are extensively used in industrial applications. Some critical application cannot tolerate failure of power supply as well variation in supply. The isolated low-voltage and high-current DC power supply is widely used in many applications like arc furnace, fusion technology, welding power supply etc. There are many DC-DC power conversion applications where the voltage source has to be converted to a low output voltage, high efficiency, high power density, high reliability and low EMI. These are some of the most desirable features for these converters. In conventional Full-Bridge inverter, the transformer voltage is asymmetrical, so transformer core gets saturated and due to the high switching frequency the circuit parasitic have negative effects on the converter performance, so switching losses increases in high power applications. This creates the need of snubbers that increase the overall losses and bringing down the efficiency. If one is going for higher voltage rating, then its conduction losses increases and cost also increases. So to eliminate this problem, Phase Shifted full bridge inverter is selected. In this topology, When QA & QC both are ON then transformer voltage is zero so the core winding is reset and there is no dc saturation problem, at that time energy is freewheeling. There is no energy transfer from primary to secondary. As compared to Resonant Converter, Quasi-Resonant Converters are able to control output voltage in wide range and it is comparatively easy to achieve the control of duty cycle. It is advantageously to use the parasitic circuit elements to achieve the zero voltage switching or zero current switching so there is no need of extra Resonant components. In the Quasi-Resonant Converters, a high-frequency resonant tank circuit is connected across the switch which is employed to shape the switch current and voltage so that high-current and high-voltage is never present simultaneously. As a result, stresses and switching losses in the devices are greatly reduced. Depending on how the high-frequency resonant circuit is

connected to the switch, the Quasi -Resonant Converters can be either ZCS-QRCs or ZVS-QRCs, accordingly it eliminates either turn-off or turn-on loss [1]. The majority of power loss comes from the rectification on the low-voltage side. So Synchronous rectification by using MOSFETs is recommended in place of Diode rectification [2]. Isolation is required in some of important industrial applications. Switched mode power regulators do not provide the necessary isolation. Hence two stage conversion DC-AC and AC-DC is required. The isolation is provided by inter stage high frequency transformer.

1.2 Scope of the Work

The main aim of this project is to set up hardware model of Low-Voltage High-Current Power Supply with isolation and compact power supply package size. The High Frquency Transformer is designed to achieve the ZVS (Zero Voltage Switching) to eliminate the turn on losses as well as to provide the isolation between source and load. As far we have seen, in Low-Voltage applications, conduction losses of the diode bridge rectifier contribute significant power losses in the Power Supply compared to the synchronous rectifier. So the synchronous rectifier is used in place of diode bridge recifier to achieve the high effeciency. The 900 W Prototype DC Power Supply is fabricated and tested.
The work is divided in to four stages. In the first stage: Selection of the topology for isolated DC-DC converter and designing of converter was done. In the second stage, simulation was done using PSIM software and various control schemes with analog as well as DLL blocks was developed. In the third stage, hardware component design was required and hardware module was set up. In the fourth stage, software was need to be implemented using DSP based control and finally combined hardware set up was tested.

1.3 Objectives

To design and implement a low-voltage high-current power supply with a regulated output voltage using DSP. Main objectives are to design a converter with the following requirements:

- Cost efficient AC/DC converter
- Output power:15 kW
- Output voltage:(0-30) V

- Output current:500 A
- Input voltage(3-ph):415V ± 15%
- Switching frequency of inverter:18000 Hz
- Output voltage ripple:40 mV(rms)
- Efficiency > 90%

1.4 Literature Survey

Literature survey plays a very important role in the project. Literature survey consists of power topology, control schemes and related papers that includes mathematical modeling, simulation and experimental results. Some important information related to isolated DC-DC converters, phase shifted full-Bridge topology, high frequency transformer, Synchronous rectifier. Papers were taken from IEEE conference proceedings, journal proceedings, standard publications and application notes of different manufactures.
In this paper titled "Resonant,quasi-resonant,multi-resonant and soft swiching techniques-merits and limitations" The quasi resonant converter achieves high efficiency, due to limitation of switching losses. turn on losses are limited because of inductive character of the load. The turn off losses are reduced by snubber capacitors, paralelly connected to power transistors.With charging and discharging of these capacitors, we can achieve the zero voltage switching mode. This quasi-resonant converter is able to control output voltage in wide range compared to resonant converter [1].

In this paper titled "Design of a 2.5 kW DC/DC Full-bridge Converter" It was found that by going from 20 kHz to 100 kHz the converter weight can be reduced by approximate 10% and by using the center-tap instead of full wave-bridge rectification the efficiency can improve by approximately 1-3%, from 94% up to approximately 97% efficiency can be achieved [2].

In this paper titled "Efficiency Improvement Techniques of High Current Low Voltage Rectifiers Using MOSFETs" This paper presents techniques for loss minimization in high-current low-voltage power supplies. Due to the use of synchronous rectification using MOSFETs offers the advantage of reducing the conduction losses significant compared to conventional rectification, with the possibility of achieving almost zero conduction losses through parallel connection. The design considerations for paralleling MOSFETs are briefly discussed in this paper, as paralleling is requied for high current requirements [7].

In this thesis, "Compact Isolated High Frequency DC/DC Converters Using Self-Driven Synchronous Rectification" This thesis introduces a mimimize of conduction losses using self-driven method to drive the secondary side synchronous rectifiers. Mimimize of conduction losses using self-driven method introduces two additional transformers that increase the overall size of the converter. Also, this topology introduced a new magnetic integration method to eliminate the need for the two additional gate driver magnetic cores, The magnetic integration reduces the overall converter size[9].

In this paper titled "Switching Analysis of Synchronous Rectifier MOSFETs with Phase-Shifted Full-Bridge Converter and Current Doubler" in this paper discussed the switching analysis of synchronous rectifier used the switch as MOSFETs in a phase-shifted full-bridge converter topology with a current doubler. Mainly two types of topologies are introduced for gate pulses of synchronous rectifier (SR) MOSFETs. The two different gate pulses introduced the Synchronous rectifier MOSFET operations during every stage for both topologies and the calculation of losses foe each and every stage is discussed[11].

In this paper titled "Design of Phase Shifted Full Bridge Converter with Current Doubler Rectifier" A wide range of isolated topologies are available for the dc-dc stage, high power rating could be realized with either a half-bridge or full-bridge. A full-bridge has half the rms current compared to a half-bridge, and it has been used for higher power rating applications, also it can be implemented with phase shifted control which provides Zero Voltage Switching (ZVS) for primary side switches, current doubler rectifier with synchronous rectification is the most suitable for high current application, as it splits the output current between two filter inductors, which reduces conduction losses, improves thermal distribution, and allows for lower profile, in addition to the ripple cancellation effect on the output capacitance [12].

In this paper titled "Phase-Shifted Full-Bridge, Zero-Voltage Transition Design Considerations" In this note highlight the design considerations in a high frequency power supply using the Phase Shifted PWM control technique. In this switching technique including comparisons for fixed frequency non resonant and variable frequency Zero Voltage Switching (ZVS) is discussed [13].

In this paper titled "ZVS Phase Shift Full Bridge CFD2 Optimized Design" in this paper the ZVS (Zero Voltage Switching) phase shifted full bridge converter is used in IFX board achieves this reduction of switching losses due to a zero voltage turn-on of the MOSFETs. In this design the ZVS operation is maintained from full load to light

load, but due to higher leakage inductance duty loss in secondary side transformer is higher [14].

In this paper titled "High Efficiency Current-Doubler Rectifier with Low Output Current Ripple and High Step-Down Voltage Ratio" This paper presents a current-doubler rectifier with high step-down voltage ratio and low output current ripple. In this proposed scheme, two extra inductors are introduced to extend the duty ratio of switches, and two extra diodes are used to provide discharge paths for the two extra inductors. To check the merits of the proposed rectifier, its performance indexes, such as secondary winding peak current of the isolation transformer, output current ripple and voltage gain function are discussed and compared with the conventional current-doubler rectifier [16].

In this paper titled "Design of efficient low voltage high current dc to dc power supply" In this paper low voltage high current DC to DC power supply is analysied. The converter is using single switch forward converter. On secondary side rectification, synchronous rectifiers are used. The voltage conversion ratio of the converter is high. Transformer based topologies are used for converters requiring high conversion ratio. The suitability of the proposed winding arrangement is used to improve the efficiency of the power supply. The magnetic design of the secondary winding arrangement is given. The loss calculation and the experimental results of the power supply are presented [19].

In this paper titled "Analysis and design of an Auxiliary Commutated Full Bridge DC/DC Converter Topology including the effect of Leakage Inductance" the transformer has high turns ratio between the primary and secondary windings, the value of leakage inductance is relatively high. This high value of leakage inductance is not large enough to achieve the zero voltage switching (ZVS) over the wide range of load conditions, but it can be used to minimize the circulating current of the auxiliary commutation circuit [27].

Chapter 2

Isolated Topologies for DC-DC Converter

2.1 Introduction

Power supplies which are used extensively in industrial applications are often required to meet all or most of the following conditions.

a. Isolation between the source and the load.

b. Controlled direction of power flow.

c. High power density for reduction of size and weight.

d. High conversion efficiency.

Depending upon the output voltage, the power supplies can be categorized into two types:

1. DC POWER SUPPLIES

2. AC POWER SUPPLIES

Controlled DC Power supply can be obtained from the phase controlled rectifiers, but there are certain disadvantages, which led to the Switched Mode Power Supplies. An AC to DC rectifiers operates at supply frequency of 50 Hz so to obtain almost negligible ripple in the DC output voltage, physical size of the filter circuits required is large. This makes the DC power supply bulky, inefficient and weighty. In the other side, SMPS works like a DC chopper. By operating the on/off switch very rapidly, ripples can be easily filtered by the using of L and C filter circuits, which are small

in size and less weighty. By varying the duty cycle of the switching device by PWM techniques controls the output DC voltage [2] [3].

There are five common configurations for isolated DC-DC Power supply on primary side:

- Flyback topology
- Forward topology
- Push-Pull topology
- Half-Bridge topology
- Full-Bridge topology

2.2 The Flyback Converter:

2.1 shows that use of a single transistor switch means that the transformer can only be driven asymmetrical, this results in a large core size. The Flyback is an isolated version of the buck-boost, so it is not used as a transformer but used as a coupled inductor. When the transistor is turned on, current flowing through the primary winding and energy is stored in the core. When the transistor is turned off, When the switch is turned off, current flowing through the secondary side and energy is released to the output.

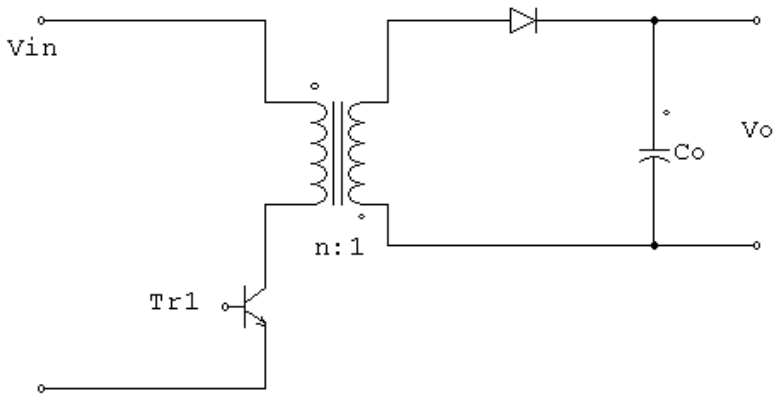

Figure 2.1: Flyback Converter Circuit

2.2 shows that the Forward Converter is also a single switch isolated topology, this is based on the buck converter with the addition of a inductor and another diode

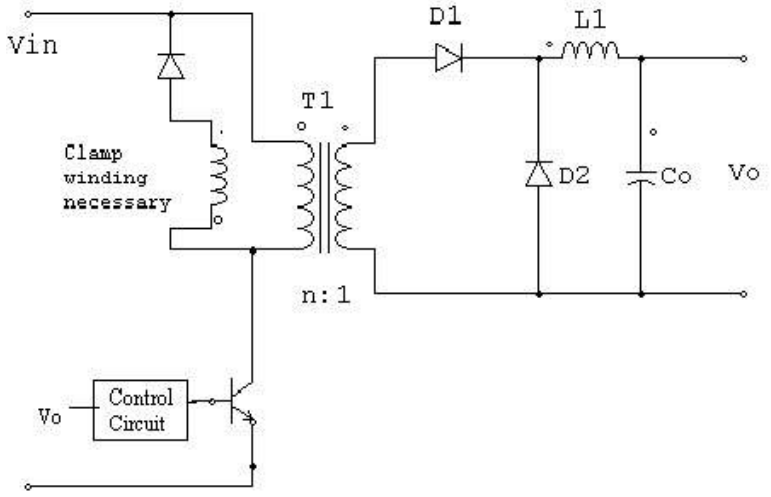

Figure 2.2: Forward Converter Circuit

in the output circuit. In contrast to the Flyback, the Forward Converter has a true transformer action, When the transistor is turn on, energy is transferred directly to the output through the inductor. The polarity of the secondary winding is opposite to flyback, hence current flowing through diode D1.

2.3 The Push-Pull Converter:

2.3 shows that one of the best symmetrical types of converter, this permits much smaller transformer sizes and it provides higher output power. The primary is a center-tapped arrangement and each transistor switch is driven alternately, here transformer drives in both direction. The Push-Pull transformer is half the size of that for push-pull and flyback, it resulting in a more compact design compared to other converter.

2.4 The Half-Bridge Converter:

2.4 shows that the Half-Bridge Converter is also referred to as the single ended Push-Pull, and in principal is a balanced version of the Forward Converter. The two main bulk capacitors C1 and C2 are connected in series and an artificial input voltage mid-point is provided. The two transistors switches are driven alternately, and this connects each capacitors across the single primary winding each half cycle.

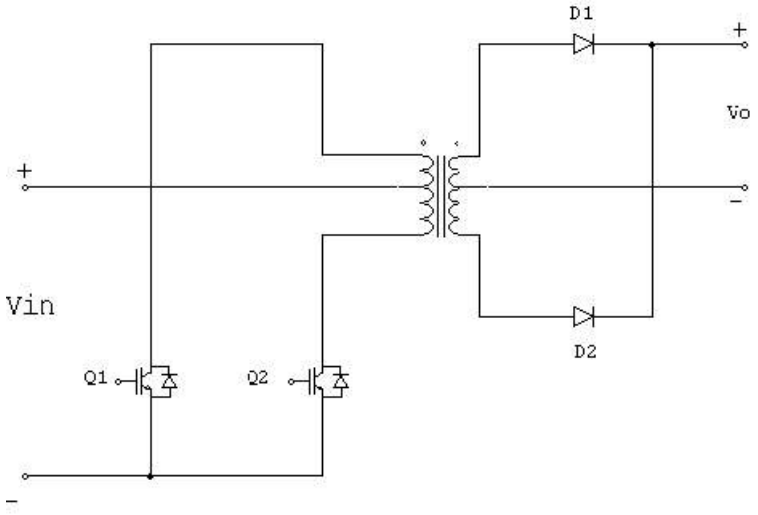

Figure 2.3: Push-Pull Converter Circuit

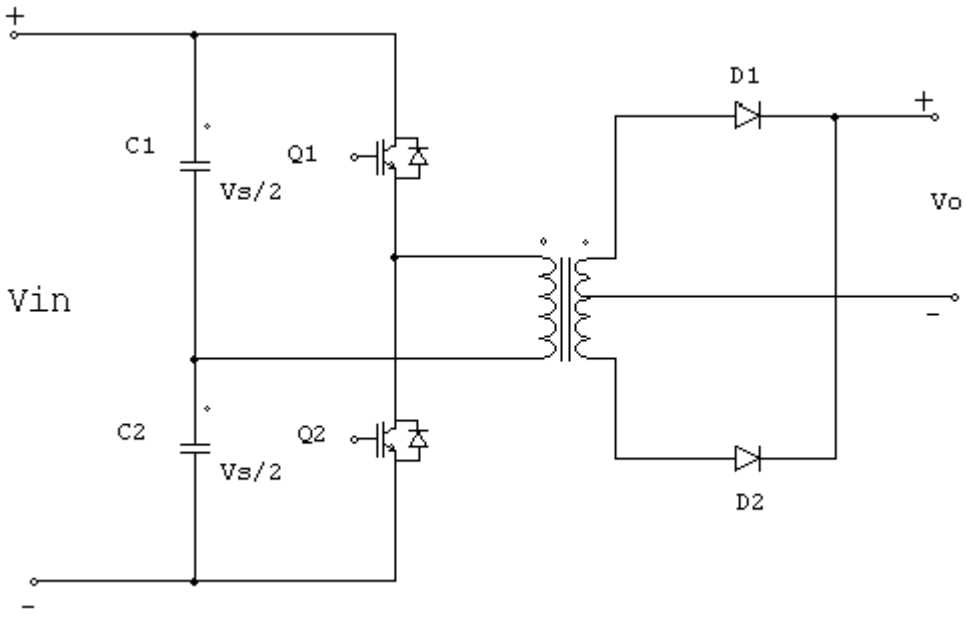

Figure 2.4: Half-Bridge Converter Circuit

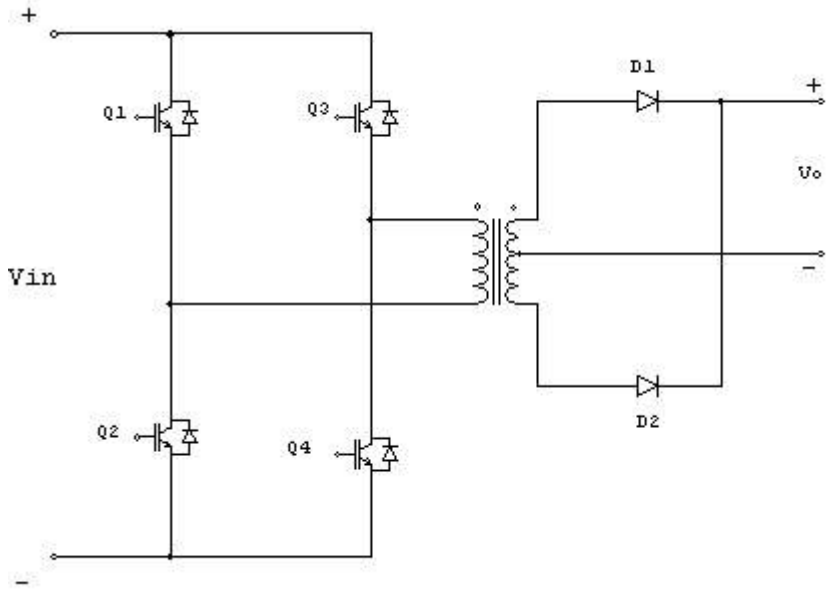

Figure 2.5: Full-Bridge Converter Circuit

2.5 The Full-Bridge Converter:

2.5 shows that the Full-Bridge Converter is a higher power version of the Half-Bridge, and provides the highest output power level of any of the converters which are discussed. The maximum current ratings of the power transistors will determine the upper limit of the output power of the half-Bridge. These levels can be doubled by using the Full-Bridge, which is obtained by adding another two transistors and clamp diode to the Half-Bridge arrangement [4] [5] [6].

So on primary side(high-voltage) selected topology is Full-Bridge converter, for the high(several kilowatts) power applications this topology is widely used. One should kept in mind that it has more cost than other topology because maximum switches are use.

2.6 Isolated topologies for Secondary Side (Low-Voltage)

The topology selection for a high frequency, compact, low voltage and high current converter is driven by thermal performance and power density. The converters ef-

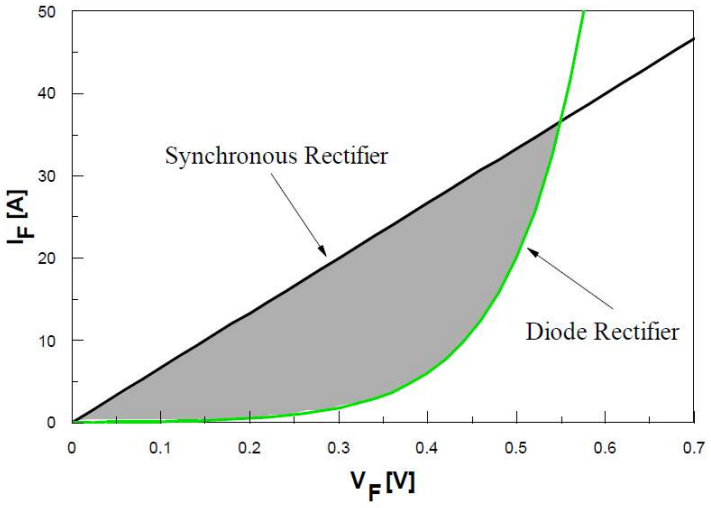

Figure 2.6: Comparison between Synchronous Rectifier and Diode Rectifier Conduction loss

ficiency must be maximized and the hot spots must be eliminated to improve the thermal performance in applications where a heat sink cannot be applied. In this application large step-down ratio is required, such as a 560 volt input to less than 35 volt output, the efficiency could be optimized with the use of a step down high transformer. On the secondary side conduction losses are dominant. So to minimize the conduction losses, MOSFET synchronous rectifiers (SR) can replace the diodes but the circuit implementation becomes more complex. The parallel combination of multiple synchronous rectifiers can further reduce the conduction losses. The parallel combination of multiple synchronous rectifiers will lower the effective Rds(on) and therefore it reduce I2 * R losses. so the RMS current is divided between each synchronous rectifier, the losses are distributed and the thermal burden reduced.

In low output-voltage applications, the conduction loss of diode rectifier contributes significantly to the overall power loss. The rectifier conduction loss is proportional to the product of its forward-voltage drop (V_F) and the forward conduction current(I_F). But the Forward Voltage drop of a synchronous rectifier can be lower than that of a diode rectifier, it reduces the rectifier conduction loss. So the synchronous rectifiers are widely used in Low voltage applications. 2.6 shows that the comparison between synchronous rectifier and diode rectifier conduction losses [7] [8] [20].

Secondary Side Different Synchronous Rectifier Topologies:

Isolated topologies can have multiple of secondary topologies, The four most commonly used secondary side topologies are the Full-Wave, Forward, Center-tap and Current-Doubler Rectifiers.

2.7 shows that during the power delivery period of the Full-wave Synchronous Rectifier, the filter inductor current is conducting through two mosfets in series. The conduction losses of the Full-wave Rectifier are twice of the Current-Doubler Rectifiers, Forward rectifiers, Center-tap and Current-Doubler Rectifiers. it is not suitable for Low-Voltage, High-Current applications but used in High- Voltage applications.

2.8 shows that the Forward Synchronous Rectifier has the most basic structure and it contains a simple two switches, high frequency transformer, a single filter inductor and a capacitor. This topology is least suitable for High-Current, Low-Voltage applications because the Forward Rectifier has a larger filter inductor and larger rectification losses. The filter inductor is sized to support the full load current at the converter's switching frequency. During the power delivery period the inductor current will flow through Q1, and during the freewheeling period Q2 will carry the full inductor current.

2.9 shows that Current-Doubler Circuit, Compared to the Forward and Center-tap Rectifiers, the current doubler has an additional filter inductor. The frequency seen by the filter inductors is the same as the switching frequency in the current doubler, but the size of these inductors can also be reduced. The filter inductors size reduction comes from a partial cancellation of the ripple current due to the interleaving properties of the Current Doubler.

2.10 shows that the Center-tap Synchronous Rectifier compared to the Forward topology, the filter inductor in the Center-tap Synchronous Rectifier is designed at twice the switching frequency which results in a smaller inductance value and also reduce the size. The filter inductor value is inversely proportional to the effective ripple current frequency, which results in a fifty percent reduction in the required inductance value. During the freewheeling period in a symmetrically driven Center-tap Rectifier the filter inductor current is evenly distributed between both rectifiers Q1 and Q2 resulting in lower rectifier conduction losses [9].

So on secondary side (low voltage)Center-tap Synchronous Rectifier is selected, due to the main advantage of the filter inductor in the Center-tap Synchronous Rectifier is designed at twice the switching frequency resulting in a smaller inductance value and lower conduction losses.

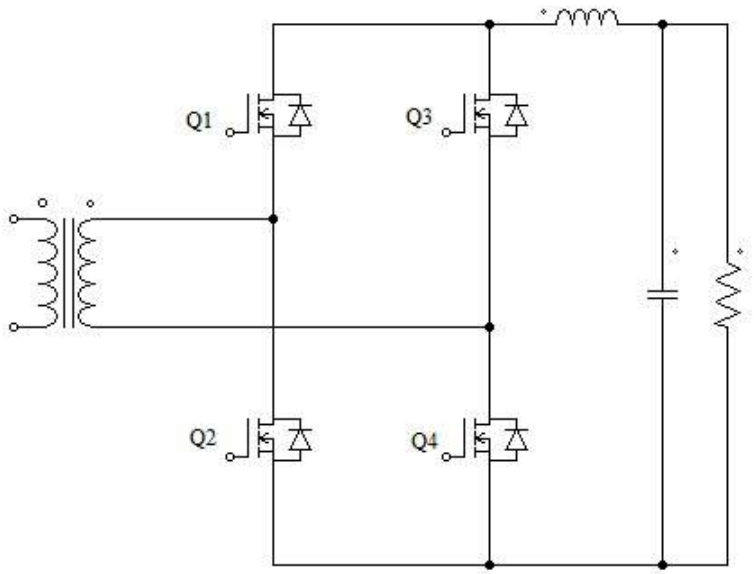

Figure 2.7: Full-Wave Synchronous Rectifier

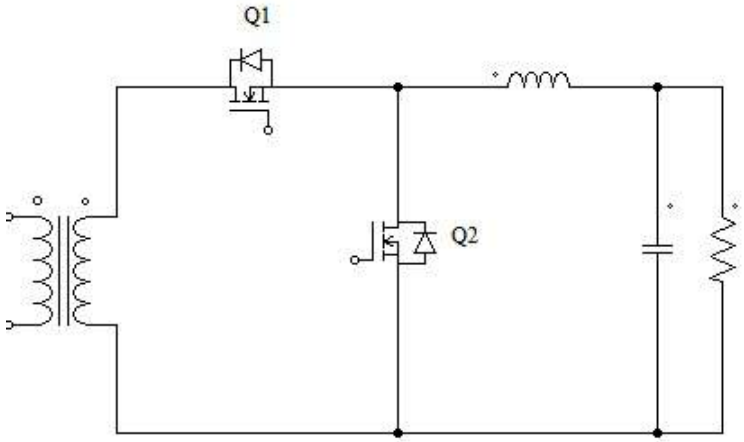

Figure 2.8: Forward Synchronous Rectifier

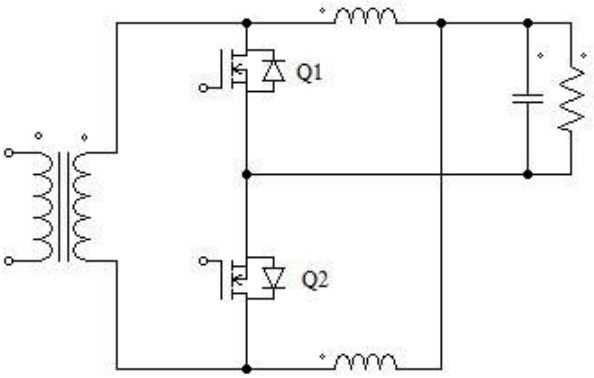

Figure 2.9: Current-Doubler Synchronous Rectifier

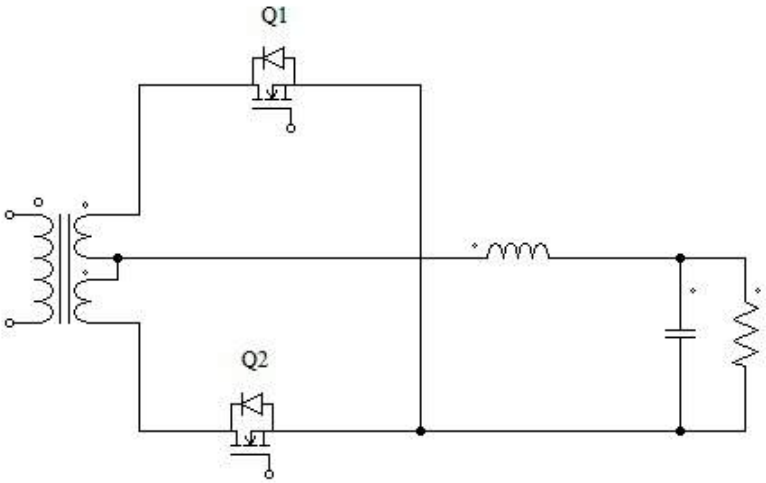

Figure 2.10: Center-tap Synchronous Rectifier

Chapter 3

Quasi Resonant Converter

3.1 Introduction

In the Quasi Resonant Converters, a high-frequency resonant tank circuit connected around the PWM switch is employed to shape the switch current and voltage so that high current and high voltage are never present simultaneously. As a result, stresses and switching losses in the devices are greatly reduced. Depending on how the high-frequency resonant circuit is connected to the switch, the Quasi -Resonant Converters can be either ZCS-QRCs or ZVS-QRCs, accordingly it eliminates either turn-off or turn-on loss [10][27]. In the Quasi Resonant Converters compared to Resonant Converter, it is able to control output voltage in wide range and it is comparatively easy to achieve and it is advantageously used the parasitic circuit elements to achieve the zero voltage switching or zero current switching so no need of extra resonant component.

3.1.1 Advantages of ZVS (Zero voltage switching)

In a hard switching device, in order to reduce the switching losses for the semiconductor components, paralleling of passive components such as resistors, inductors and capacitors can be used. This different kind of parallel combinations of passive components is called snubber. Lossy snubbers are needed in order to absorb and dissipate voltage and current transients on the switching devices. so efficiency is decreses and cost is increses, but in a soft switching device, ZVS (Zero Voltage Switching) is achieved through the switching element of parasitic output capacitances resonate with the leakage inductance of the transformer and oscillate the switch voltage to zero before the switch turn on. At this stage, ZVS (which means no switching loss) occurs and a significant improvement in efficiency gained.

- Reduce or eliminate voltage and current spikes.

- Limit di/dt or dv/dt.
- Shape the load line to keep it within the safe operating area (SOA).
- Transfer power dissipation from the switch to a resistor.
- Reduce total losses due to switching.
- Reduce EMI by damping voltage and current ringing.

3.2 Why select the Phase Shifted Full-Bridge Topology?

In order to reduce the size and the weight of magnetic components it is desirable to increase the switching frequency for DC-DC converters. When conventional PWM converters are operated at high frequencies, the circuit parasitic has negative effects on the converter performance. Switching losses increase in high power applications and snubbers and/or other means of protection are required, which introduce significant losses and lower the efficiency. In the case of the conventional full bridge converter, the diagonally opposite switches (SA and SB, or SC and SD) are turned on and off simultaneously. When all four switches are turned off, the load current freewheels through the synchronous rectifier. In this case the energy stored in the leakage inductance of the power transformer causes severe ringing with IGBT Junction capacitance. This creates the need for using snubbers that increase the overall losses due to that efficiency is decreased. If snubbers are not used, the selection of the devices becomes more difficult as the voltage rating for these switches has to be much higher. The conduction losses and as a result the overall losses increase. At the same time the cost is also increases. So in order to minimize the parasitic ringing, the Phase Shifted Full-Bridge Topology is selected. In this topology the gate signals of SC and SD are delayed (Phase-Shifted) with respect to those of SA and SB as shown in 3.1, There is a small amount of overlap between SA and SB, and SC and SD, which is called PWM delay (PWM delay AB, and PWM delay CD). PWM delay will prevent the same-side IGBTs (SA and SB, or SC and SD) from turning on simultaneously, which would result in a short circuit that burns out the IGBTs. In addition, the delay time helps so that the primary of the transformer is either connected to the input voltage or shorted. The leakage inductance current is never interrupted, thus solving the problem of parasitic ringing associated with the Conventional Full-Bridge PWM converter. When the PWM pulse is off, the snubber inductance Lr, by way of storage energy, will resonate with the output capacitances of the IGBTs and oscillate the IGBT voltage to zero before the IGBTs turn on. At this stage, ZVS (which means

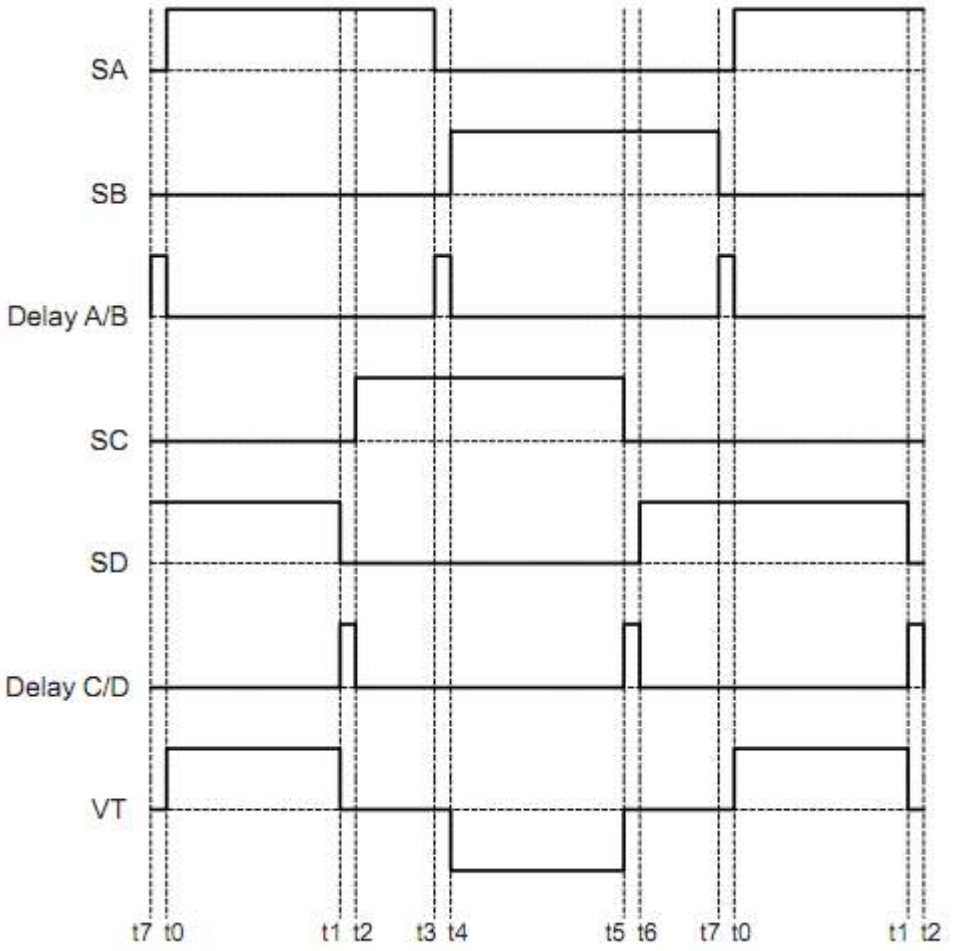

Figure 3.1: Gate Pulses of Phase Shifted PWM control waveform

no switching loss) occurs and a significant improvement in efficiency is gained [11].

The energy stored in the leakage inductance can be used to discharge the energy stored in the IGBT junction capacitance to achieve zero voltage switching (ZVS) conditions for all four switches in the primary side. In this case, the converter requires no additional resonant components [12] [13].

3.3 Resonant Circuit Design with 18kHz Switching Frequency of 15 kW Power Supply

3.3.1 Resonant Capacitance C_R

The specified IGBT switch output capacitance C_{oss} will be multiplied by 4/3 factor as per the IGBT manufacturers application note to approximate the correct average capacitance value with a varying drain voltage. During each transition,two switch capacitances are driven in parallel,doubling the total capacitance to $8/3{*}C_{oss}$. Transformer capacitance C_{XFMR} must also be added as it is not negligible in many high frequency application.

$$C_R = \frac{8}{3}C_{oss} + C_{XFRM} \tag{3.1}$$

$C_R = \frac{8}{3}(25n) + 5n$

C_R =$71nF$

The capacitive energy required to complete the transition W_{CR} :

$$W_{CR} = \frac{1}{2}C_R V_I^2 \tag{3.2}$$

The energy can be expressed as :

$$W_{CR} = \frac{1}{2}(\frac{8}{3}C_{oss} + C_{XFRM})V_I^2 \tag{3.3}$$

3.3.2 Resonant Inductor L_R

ZVS may be lost partially or completely due to lack of energy or insufficient dead time. During no load and light load conditions,ZVS may be lost if the inductive energy available in the circuit is not sufficient to charge and discharge the output capacitance of the two IGBTs in the same bridge leg in addition to the transformer capacitance.
Calculate the resonant inductor value L_R (L_R= External series inductance+ Leakage inductance) and minimum primary current required for any application. These parameters are calculated as per the following equations.

The first criterion for achieving ZVS is:

$$\frac{1}{2} \times L_R \times I_P^2 > \frac{1}{2} \times C_R \times V_I^2 \tag{3.4}$$

$$L_R > \frac{C_R \times V_I^2}{I_P^2} \tag{3.5}$$

$L_R > \frac{(71n)\times(415)^2}{(28.2)^2}$

$L_R > 16\mu H$

So for Zero voltage switching requirement must be greater than 16 μH but primary side leakage inductance of transformer is 32 μH so external inductance is not require to connect in series with primary winding of transformer[14].

3.3.3 Energy and Dead time conditions for achieving ZVS:

The second criterion for achieving ZVS is that the delay time is long enough to allow resonant voltages to finish the energy transfer in C_{oss} and L_R. Assuming the frequency of the resonant is F_{RES}.

$$T_{RES} = \frac{1}{F_{RES}} \tag{3.6}$$

While the C_{oss} of the IGBT discharges from V_I = max. to zero and the C_{oss} of the IGBT charges from V_I= zero to max. The delay time(dead band) must be greater than $\frac{1}{4}T_{RES}$.

$$F_{RES} = \frac{1}{2\Pi\sqrt{L_R C_R}} \tag{3.7}$$

$F_{RES} = \frac{1}{2\Pi\sqrt{(30\mu)(70n)}}$

F_{RES}=109.82 KHz

T_{RES}=9.10 μs

The resonant tank period must be at least four times higher than the transition time to fully resonant within the maximum transition time T_R at light load.

$$T_R = \frac{1}{4} T_{RES} \tag{3.8}$$

T_R=2.27 μs

But for achieving the ZVS, the delay time or dead band (t_{max}) must be greater than $\frac{1}{4}T_{RES}$. Otherwise the IGBT cannot achieve ZVS. If Delay time below $\frac{1}{4}T_{RES}$ will cause switching at a non-zero voltage(partial ZVS), on the other hand, delay time higher than $\frac{1}{4}T_{RES}$ will cause extra body diode conduction losses, furthermore, might cause losing ZVS if the resonant circuit is highly damped (or lossy). The larger delay time will cause the maximum duty cycle to be smaller, impacting the hold-up time performance [15].

$$T_{MAX} > \frac{1}{4} T_{RES} \tag{3.9}$$

Select the value of T_{MAX}=2.2 μs

3.3.4 Minimum(critical) Primary current

The minimum primary current required for the phase-shifted application can now determined because below this critical current level will result in lossy transition and also ZVS can not be achieved below critical current.

$$I_{PRI} = \sqrt{\frac{C_R \times V_I^2}{L_R}} \tag{3.10}$$

I_{PRI} = 19.1 A

But transformer primary current in this case is 28.2 A, which is more than minimum primary current [16] [17].

3.4 Resonant Circuit Design with 18 kHz Switching Frequency of 900 W Prototype Power Supply

3.4.1 Resonant Capacitance C_R

$$C_R = \frac{8}{3} C_{oss} + C_{XFRM} \tag{3.11}$$

$C_R = \frac{8}{3}(5n) + 5n$

C_R =15.66 nF

Where,
C_{oss}= output capacitance of IGBT which is mention in IGBT's datasheet
V_I= Input voltage= 415 V
I_P= Input current= 2.4 A

The capacitive energy required to complete the transition W_{CR} :

$$W_{CR} = \frac{1}{2} C_R V_I^2 \tag{3.12}$$

The energy can be expressed as :

$$W_{CR} = \frac{1}{2}(\frac{8}{3} C_{oss} + C_{XFRM}) V_I^2 \tag{3.13}$$

3.4.2 Resonant Inductor L_R

The first criterion for achieving ZVS is

$$\frac{1}{2} \times L_R \times I_P^2 > \frac{1}{2} \times C_R \times V_I^2 \tag{3.14}$$

$$L_R > \frac{C_R \times V_I^2}{I_P^2} \tag{3.15}$$

$L_R > \frac{(15.66n) \times (415)^2}{(2.4)^2}$

$L_R > 440 \mu H$

So for Zero voltage switching requirement must be greater than 440 μH but primary side leakage inductance of transformer is 600 μH so external inductance is not require to connect in series with primary winding of transformer[15].

3.4.3 Energy and Dead time conditions for achieving ZVS:

The second criterion for achieving ZVS is that the delay time is long enough to allow resonant voltages to finish the energy transfer in C_{oss} and L_R. Assuming the frequency of the resonant is F_{RES}.

$$T_{RES} = \frac{1}{F_{RES}} \tag{3.16}$$

While the C_{oss} of the IGBT discharges from V_I = max. to zero and the C_{oss} of the IGBT charges from V_I= zero to max. The delay time(dead band) must be greater than $\frac{1}{4}T_{RES}$.

$$F_{RES} = \frac{1}{2\Pi\sqrt{L_R C_R}} \tag{3.17}$$

$F_{RES} = \frac{1}{2\Pi\sqrt{(440\mu)(15.66n)}}$

F_{RES}=60.63 kHz

T_{RES}=16.5 μs

$$T_R = \frac{1}{4}T_{RES} \tag{3.18}$$

T_R=4.12 μs

Select the value of T_{MAX}=3.2 μs

3.4.4 Minimum(critical) Primary current

The minimum primary current required for the phase-shifted application can now determined because below this critical current level will result in lossy transition and also ZVS can not be achieved below critical current.

$$I_{PRI} = \sqrt{\frac{C_R \times V_I^2}{L_R}} \tag{3.19}$$

I_{PRI} = 2.14 A

But transformer primary current in this case is 2.4 A, which is more than minimum primary current [16] [17].

Chapter 4

Design of 18 kHz High Frequency Transformer

4.1 Introduction

The fundamental requirements of magnetic material for power transformers are the lowest core loss, highest relative permeability, the largest saturation flux density and the lowest remanent flux density. magnetic material using as the cores of power transformers keep charging as the operating frequency increased. At the line frequency of 50/60 Hz, iron, silicon steel are the major materials for the cores of the power transformers. They have high saturation flux density, thus they can handle high power transformer at low operating frequency. when the operating frequency of power transformer increased, the eddy current inside the magnetic cores becomes a critical problem for the transformer designers. Although the laminated core material have been used, the power loss generated inside magnetic core can destroy whole power transformer. As the operating frequency is increased more and more magnetic materials have been introduced for high frequency power transformer application [18].

4.1.1 The characteristics of High Frequency Transformer windings:

When the operating frequency increases, the total number of turns decreases significantly. Therefore the total length of the copper winding is also decreased dramatically. The power loss due to DC resistance almost becomes zero suddenly. It is very good for the power transformer design. However, with disappearing of the DC. At high frequencies, the major loss within windings is due to eddy currents produced by the skin and proximity effects.These effects can cause the windings losses to be significantly greater than the I^2Rloss calculated using the DC resistance of the copper winding.

4.1.2 Properties of Ferrite Core

Ferrite is a class of ceramic material with useful electro magnetic properties. It is basically a mixture between iron oxide and different kinds of metal oxides. These kinds of metal oxide in various amounts allows the manufacturer to produce many types of ferrites for different applications. Ferrite cores have very high permeability. Resistivity is really high so eddy currents can be neglected when it comes to ferrite cores and for high frequency range ferrite core is widely used.

4.2 Design and Flowchart for High Frequency Transformer

Steps for designing the High Frequency Transformer is as follows:
step1:
Calculate the output power.

step 2:
Calculate the area product.

Step 3:
Select the Core from the table with a value close to the calculated one.

Step 4;
Calculate the core losses in mw/g from the graph of flux density, frequency and core losses for the ferrite core.

Step 5:
Calculate the primary and secondary turns.

Step 6:
Find the wire gauge and calculate the resistance of the resistance of the windings.

Step 7:
Calculate the copper losses and the total losses.

Step 8:
Check whether the turns fit into the effective window area.

The inequality is as follows:

$A_W K_W > \Sigma A_I N_I$

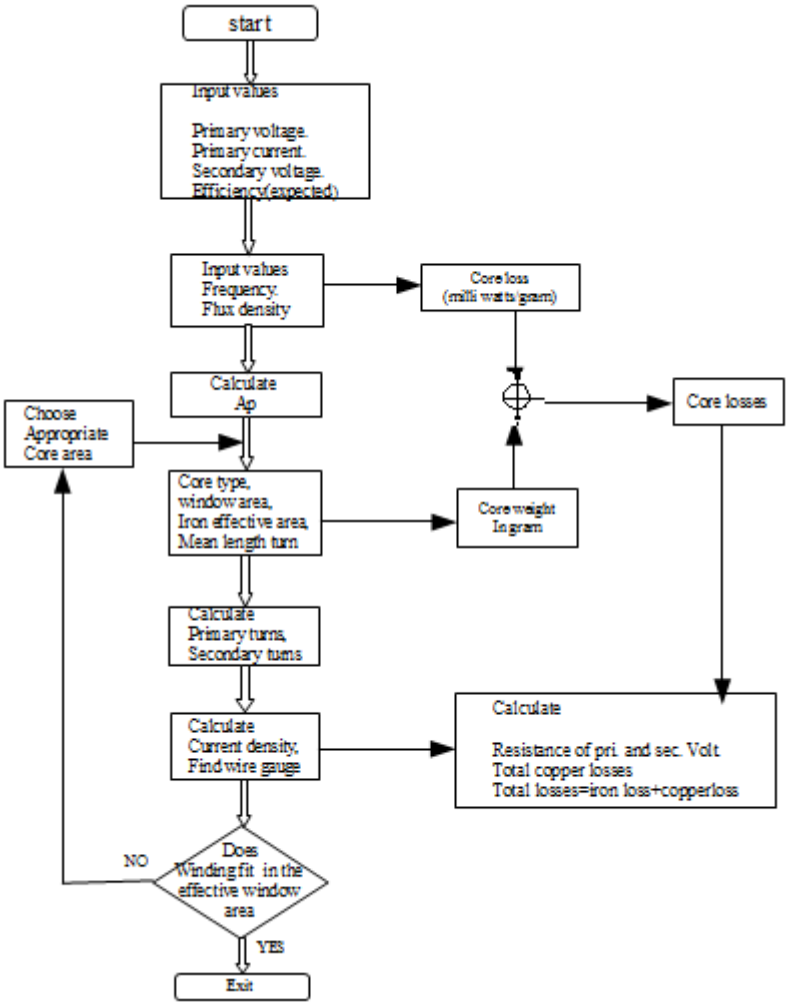

Figure 4.1: Flowchart for Design of High Frequency Transformer

Where $A_W K_W$ is the effective window area available for the winding.$\Sigma A_I N_I$ is the area occupied by the winding.

4.3 Design and Development of 900 VA,18 kHz Transformer for Prototype Power Supply

The AC-DC low-voltage high-current power supply requires DC-DC converter, a ferrite Core Transformer, Synchronous rectifier, L-C filter. So the following criteria were followed [19].

4.3.1 Design Specifications:

- 3-ph Input Voltage(V_{IN})= 415 V±15%
- Input Current(I_{IN})=2.40 A(rms)
- Output Voltage(V_O)= 0-30 V
- Output Current(I_O)=30 A
- Switching Frequency(F_s) =18 kHz

Output Power (P_O):

$$P_O = V_O \times I_O \tag{4.1}$$

$P_O = 30 \times 30$

P_O=900 W

If we consider 90% efficiency, then Input Power(P_{IN}) becomes;

$$P_{IN} = \frac{P_O}{\eta} \tag{4.2}$$

P_{IN}= 1000 W

Input Current (I_{IN}):

$$I_{IN} = \frac{P_{IN}}{V_{IN}} \tag{4.3}$$

I_{IN}=2.40 A(rms)

The governing equation for Full-bridge configuration is given by:

$$P_O = V_O I_O + V_d I_O + P_{Lcu} + P_{Lcore} \tag{4.4}$$

Where,

V_d=Diode Voltage drop=1 V

V_O=Output Voltage=30 V

$P_{Lcu} + P_{Lcore}$= Cu Losses and Core Losses = 10 % of $V_O I_O$=90 W

$P_O(withlosses)$=1020 W

4.3.2 Selection of Magnetic Core:

Area of Product(A_P):

$$A_P = A_C A_W \tag{4.5}$$

$$A_P = \frac{P_O(\sqrt{2} + \frac{1}{\eta})}{4K_W J B_m F_s} \tag{4.6}$$

Where,

A_P=Area of Product

A_c=Area of core

A_W= Window area

K_w= Window utilization factor=0.4

B_m= Maximum flux density=0.2 Tesla

J=Current Density=2-5 A/mm^2 is good compromise between conductor resistance and window area. Here it is taken 3A/mm^2.

So put all these value in to equ.4.6

Table I: Dimension of EE 65/32/27 Ferrite Core

Core No.	a mm	b mm	c mm	d mm	e mm	f mm
EE 65/32/27	65 mm	32 mm	27 mm	44.2 mm	22 mm	20mm

Table II: Dimension of EE 65/32/27 Ferrite Core

Core No.	Ap mm^4	Ac mm^2	Aw mm^2
E 65/32/27	3,04,616 mm^4	567 mm^2	537.24 mm^2

A_P=2,98,128 mm^4

From the product area, Selected core is E65/32/27.

4.3.3 Dimension of EE 65/32/27 Ferrite Core:

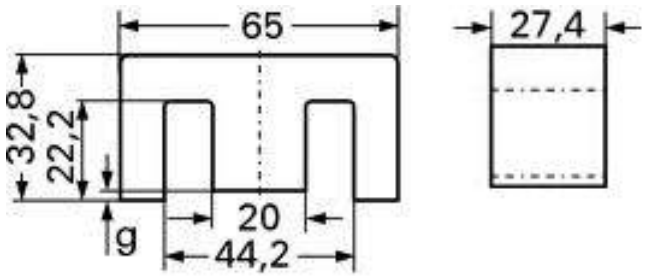

Figure 4.2: Dimension of EE 65/32/27 Ferrite Core

The dimensions and performance parameters of EE 65/32/27 Ferrite Core are given in Table 4.1 and 4.2;

4.3.4 Calculation of Number of turns:

Primary Turns(N_p):

$$N_p = \frac{V_{IN}}{2A_C B_m F_s} \tag{4.7}$$

N_p= 110 turns

Secondary turns(N_s):

$$N_s = \frac{E_s}{2A_C B_m F_s} \tag{4.8}$$

$$where, E_s = \frac{V_O + V_d + (0.1V_O)}{D_{max}} \tag{4.9}$$

E_s= 40 V

Hence $N_s = N_t$=9 turns

Wire cross section area of primary winding(a_p):

$$ap = \frac{I_{pri}}{J} \tag{4.10}$$

ap=0.66 mm^2

So take the 3 parallel wire of SWG-25.
NOTE: Current flowing through SWG-25 is 608 mA.
Wire cross section area of secondary winding(a_s):

$$a_s = \frac{I_{sec}}{J} \tag{4.11}$$

$a_s = at$= 7 mm^2 so take the 14 parallel wire of SWG-25.

Cross-check:

a_p=0.66mm^2

$a_s = at$= 7mm^2

N_p= 110 turns

$N_s = N_t$= 9 turns

A_w= 537.24 mm^2

$K_w = 0.4$

$$A_w K_w > a_p N_p + 2a_s N_s \tag{4.12}$$

214 $mm^2 > 198mm^2$

So,the above condition is satisfied, So core selection is proper.

4.3.5 Development of Transformer

To make transformer following steps were followed;

a. Make the bobbin as per dimensions of selected core.

b. Wound the primary,secondary and tertiary windings in such a way that gives sufficient leakage inductance.

c. The insulation layer between primary and secondary winding should be such that it gives desired isolation between them.

d. Measurement of magnetizing inductance of primary,secondary and tertiary windings also measure the leakage inductance and resistance.

4.3.6 Theoretical Calculations:

Primary Resistance=0.2268 Ω

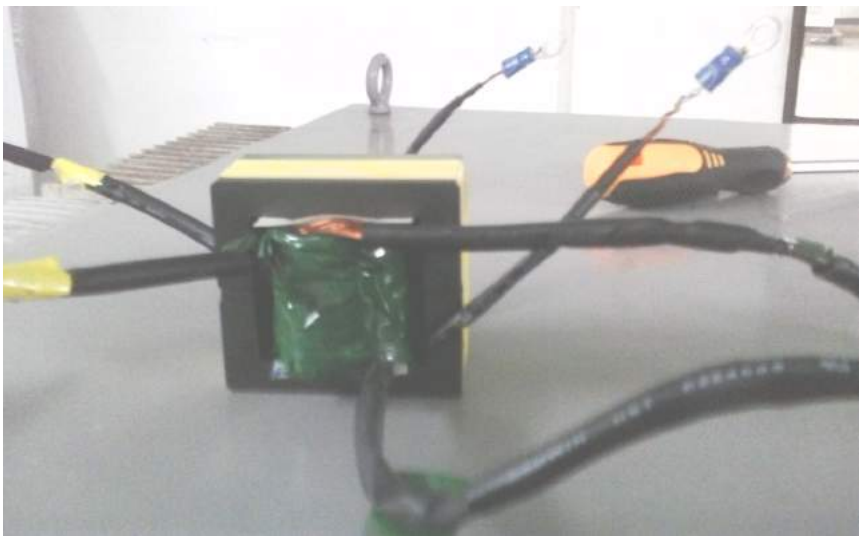

Figure 4.3: Overall view of 18 kHz, 900 VA Transformer

Secondary Resistance=18.9 mΩ

Tertiary Resistance=18.9 mΩ

Magnetizing Inductance=95.5 mH

Leakage Inductance of primary winding=440 μH

Leakage Inductance of secondary winding=4 μH

Leakage Inductance of tertiary winding=4 μH

4.3.7 Practical Results:

Primary Resistance=0.5 Ω

Secondary Resistance=14 mΩ

Tertiary Resistance=15.2 mΩ

Magnetizing Inductance=87 mH

Leakage Inductance of primary winding=440 μH

Leakage inductance of secondary winding=1.2 μH

Leakage Inductance of tertiary winding=1.3 μH

4.4 Design of L-C Filter

To filter the output voltage and current low-pass L-C filter is needed.

4.4.1 Calculate the value of Inductor

In a inductor, the core flux is decided by the load current. Thus if the load current increases, there is possibility that the core may saturate and inductance will come down. So before decide the value of inductor maximum load current must be known.

$$L = \frac{V_o \times (1 - D)}{\Delta I \times F_s} \tag{4.13}$$

Where,

Output voltage= V_o=30 V

Duty cycle= 0.85

ΔI= ripple current= 40% of output current=12 A

Switching Frequency=F_s=18 kHz

$L = 20\mu H$

4.4.2 Calculate the value of Capacitor

$$C = \frac{D \times I_o}{\Delta V \times F_s} \tag{4.14}$$

Where,

Output current= I_o=30 A

Duty cycle= 0.85

ΔV= ripple voltage= 40m% of output voltage= 1.2 V

Switching Frequency=F_s=18 kHz

C=1.66 mF

4.5 Development of 20 μH Inductor

Primary consideration in designing an inductor is that value of maximum load current (37 A) and to select the core, which does not saturate at this current. With provision of appropriate air gap in the coil so it can carry considerably larger current without saturating the core [18] [20].

4.5.1 Selection of Magnetic Core

For the selection of Core, Area of product can be calculated. The Energy and Area of product calculations are as follows;

$$E = \frac{1}{2} L I_m^2 \tag{4.15}$$

E=0.0137 joules

$$A_p = \frac{2E}{K_w K_c J B_m} \tag{4.16}$$

Where,

There is only one winding so K_c=1

K_w=0.4

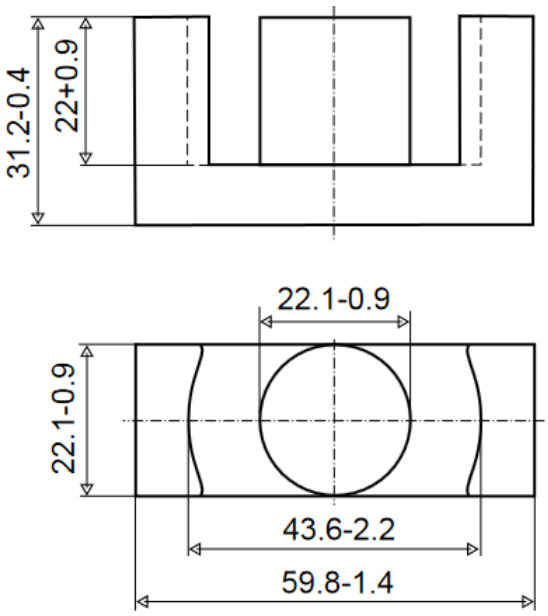

Figure 4.4: Dimension of ETD 59 Ferrite Core

J=3 A/mm^2

B_m=0.2 Tesla

A_p=114.08 mm^4

From core selection table, Selected core is ETD 59 whose Area of product is 142.15 mm^4, which is greater than calculated.

4.5.2 Calculation of Numbers of Turns

Calculate the Number of turns:

$$N = \frac{LIm}{AcB_m} \tag{4.17}$$

Where,

Im=37 A

Ac=358.02 mm^2

Aw=473 mm^2

Number of turns:12 turns

wire gauge used: SWG 25
Note:Here maximum allowable current in SWG 25 is 608 mA
So Numbers of parallel wires required = 50

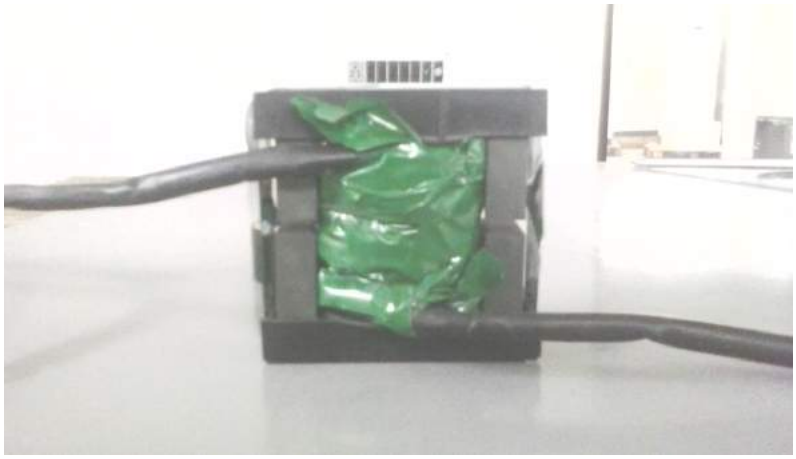

Figure 4.5: Overall view of $20\mu H$ Inductor

4.5.3 Calculate the length of airgap

$$lg = \frac{\mu o \times N^2 A_c}{mm^2} \tag{4.18}$$

$lg = 0.66cm$

4.6 Design of 18 kHz,15 kVA Transformer

The AC-DC low-voltage high-current power supply requires DC-DC converter, a ferrite Core Transformer, Synchronous rectifier, L-C filter. So the following criteria were followed [18] [19].

4.6.1 Design Specifications:

- 3-ph Input Voltage(V_{IN})= 415 V±15%
- Input Current(I_{IN})=40 A(rms)
- Output Voltage(V_O)= 0-30 V
- Output Current(I_O)=500 A
- Switching Frequency(F_s) =18 kHz

Output Power:

$$P_O = V_O \times I_O \tag{4.19}$$

$P_O = 30 \times 500$

P_O=15 kW

If we consider 90% efficiency,then Input Power(P_{IN}) becomes;

$$P_{IN} = \frac{P_O}{\eta} \tag{4.20}$$

P_{IN}= 16.67 kW

Input Current:

$$I_{IN} = \frac{P_{IN}}{V_{IN}} \tag{4.21}$$

I_{IN}=40 A(rms)

The governing equation for full bridge configuration is given by:

$$P_O = V_O I_O + V_d I_O + P_{Lcu} + P_{Lcore} \tag{4.22}$$

Where,

V_d=Diode Voltage drop=1 V

V_O=Output Voltage=30 V

$P_{Lcu} + P_{Lcore} = 10\% of V_O I_O$=1500 W

$P_O(withlosses)$=17 kW

4.6.2 Selection of Magnetic Core:

Area of Product(A_P):

$$A_P = A_C A_W \tag{4.23}$$

$$A_P = \frac{P_O(\sqrt{2} + \frac{1}{\eta})}{4 K_W J B_m F_s} \tag{4.24}$$

Where,
A_P=Area of Product

A_c=Area of core

A_W=Window area

K_w=Window utilization factor=0.4

B_m= Maximum flux density=0.2 Tesla

J=Current Density=2-5 A/mm^2 is good compromise between conductor resistance and window area. Here it is taken 3A/mm^2.

Table III: Dimension of UU93/76/30 Ferrite Core

Core No.	a mm	b mm	c mm	d mm	e mm
U 93/76/30	93 mm	76 mm	30 mm	34.6 mm	48 mm

Table IV: Dimension of UU93/76/30 Ferrite Core

Core No.	AP mm^4	AC mm^2	AW mm^2
U 93/76/30	16450560 mm^4	5040 mm^2	3264 mm^2

So put all these value in to equ.4.24

A_P=2484405 mm^4

From the product area, Selected core is UU93/76/30.

NOTE: But here We have combine the two UU Core so two U core in series and after that three UU core is used in parallel so total 12 U93/76/30 core is used.So we have higher the cross-sectional area. Dimension of

UU93/76/30 Ferrite Core

The dimensions and performance parameters of UU93/76/30 Ferrite Core are given

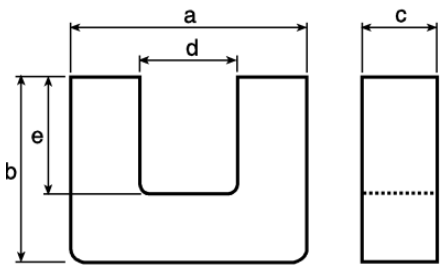

Figure 4.6: Dimension of UU93/76/30 Ferrite Core

in Table 4.3 and 4.4;

4.6.3 Calculation of Number of turns:

Primary Turns:

$$N_p = \frac{V_{IN}}{2A_C B_m F_s} \tag{4.25}$$

N_p= 12 turns

Secondary turns:

$$N_s = \frac{E_s}{2A_C B_m F_s} \tag{4.26}$$

$$where, E_s = \frac{V_O + V_d + (0.1V_O)}{D_{max}} \tag{4.27}$$

E_s= 40 V

Hence $N_s = N_t$=1 turn

Wire cross section area of primary winding:

$$a_p = \frac{I_{pri}}{J} \tag{4.28}$$

a_p=13.33 mm^2

So take the 66 parallel wire of SWG-25.
NOTE: Current flowing through SWG-25 is 608mA.

Wire cross section area of secondary winding:

$$a_s = \frac{I_{sec}}{J} \tag{4.29}$$

$a_s = a_t$= 120 mm^2

Cross-check:

a_p=13.33 mm^2

$a_s = a_t$=120 mm^2

N_p= 12 turns

$N_s = N_t$= 1 turn

A_w= 3264 mm^2

$K_w = 0.4$

$$A_w K_w > a_p N_p + 2a_s N_s \tag{4.30}$$

1305.6 $mm^2 > 400mm^2$
So,the above condition is satisfied,so core selection is proper.

NOTE: Here high current is passing through in the secondary and tersary side so utilise the more cross-sectional area, we have require only 1 turn (So for higher $a_s = a_t = 120mm^2$, Cu Plate is used for only one turn and high current is passing through this). Here core's window area is enough to accomodate the winding properly.

4.6.4 Theoretical Calculations:

Primary Resistance=8 mΩ

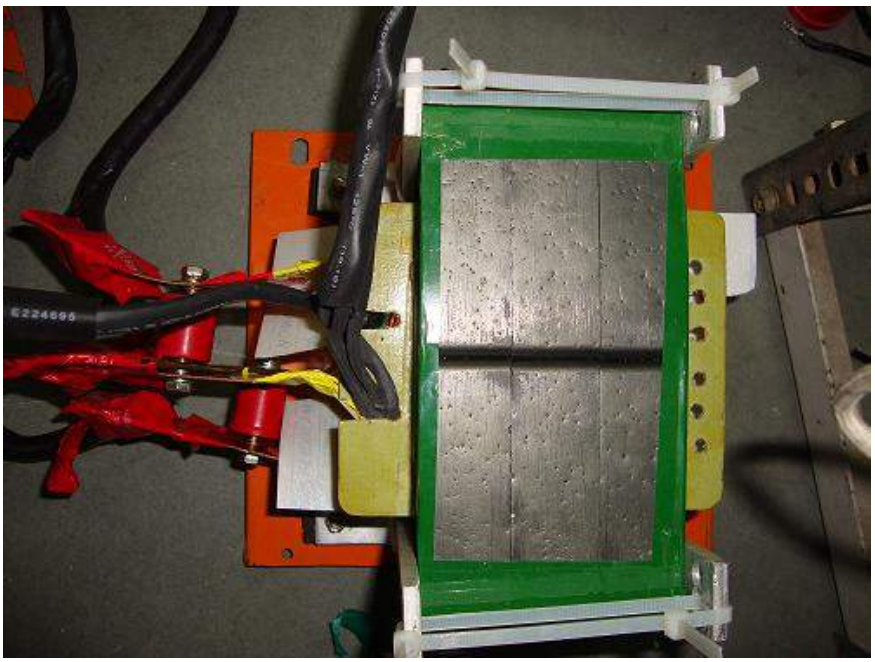

Figure 4.7: Top View of 18KHz,15KVA Transformer with UU 93/76/30 Ferrite Core

Secondary Resistance=26.7 $\mu\Omega$

Tertiary Resistance=26.7 $\mu\Omega$

Magnetizing Inductance=4.92 mH

Leakage Inductance of primary winding=32μH

Leakage Inductance of secondary winding=0.228 mH

Leakage Inductance of tertiary winding=0.228 mH

4.7 Design of L-C Filter

To filter the output voltage and current low-pass L-C filter is needed.

4.7.1 Calculate the value of Inductor

In a inductor, the core flux is decided by the load current. Thus if the load current increases, there is possibility that the core may saturate and inductance will come

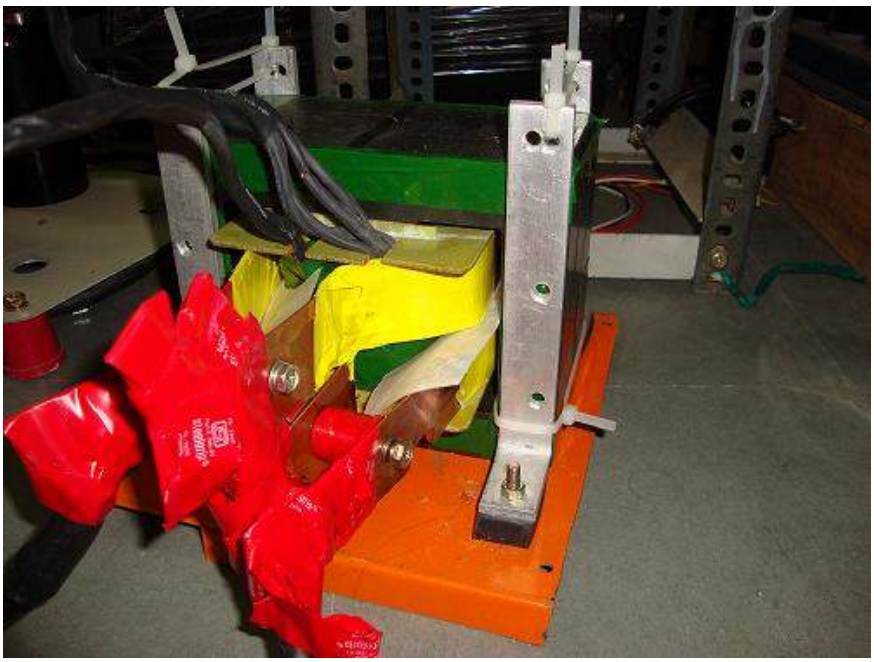

Figure 4.8: Overall View of 18 kHz,15 kVA Transformer with UU 93/76/30 Ferrite Core

down. So before decide the value of inductor maximum load current must be known.

$$L = \frac{V_o \times (1 - D)}{\Delta I \times F_s} \tag{4.31}$$

Where,

Output voltage= V_o=30 V

Duty cycle= 0.85

ΔI= ripple current= 40% of output current= 200 A

Switching Frequency=F_s=18 kHz

L=3.33 μH

4.7.2 Calculate the value of Capacitor

$$C = \frac{D \times I_o}{\Delta V \times F_s} \tag{4.32}$$

Where,

Output current= I_o=500 A

Duty cycle= 0.85

ΔV= ripple voltage= $40m\%$ of output voltage= 1.2 V

Switching Frequency=F_s=18 kHz

C=20 mF

Chapter 5

Simulation of Isolated 15 kW DC Power supply

5.1 Introduction

Linear regulator often plays important role in implementing power supply capable of constant voltage/current control. It always provides lots of advantage such as low ripple noise, low EMI, good regulation, ease control strategy. However due to bulky size, low efficiency switch mode technique has become an inevitable development trend for raising the power density, power efficiency and dynamic performance. The Full-Bridge converter is one of the isolated converter topology that use in high power rating. The block diagram of it is shown in 5.1. The feedback signal of voltage is given to the DSP control card for control and protection purpose [20].

5.2 Closed Loop Control

All switching converter output voltage is a function of the input voltage, duty cycle and load current, as well as converter circuit component values. The output voltage should be constant regardless of variation in input voltage, load current and converter circuit parameter values. The load current may vary from no load to full load. In addition, the load may vary from no load to 50% load in step, and vice versa. The converter circuit components will have some tolerance. Despite variation, it is desired that the output voltage be within a certain limit. This is not practical to achieve without negative feedback, and setting the duty cycle to a single value. There are two basic methods to control the duty cycle to keep the output voltage within the specified limit: voltage mode control and current mode control [21].

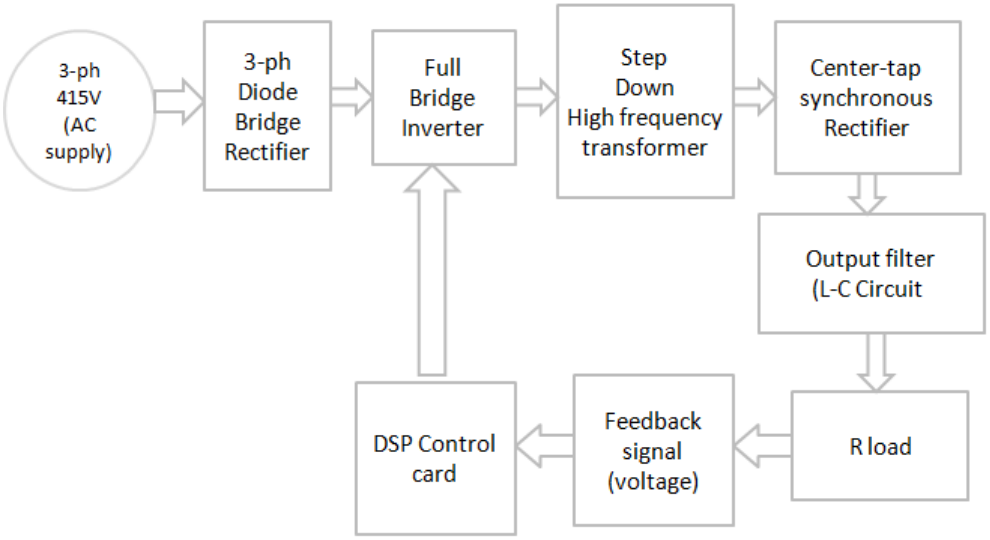

Figure 5.1: Block Diagram of Over all Power supply with feedback signal

5.2.1 Voltage Control method(CV mode control)

The transient response of voltage mode control is slow when the input voltage is changing because it has only one feedback loop. It can be seen that input voltage varying only after the variation of output voltage occurs. In fact,the transient response of voltage mode control is slow for any variations of power stage because voltage mode control doesn't have non-lag feedback loop. A feedback loop can be constructed for regulation of the output voltage. The output voltage v(o) is compared to a reference voltage Vref, and it generates an error signal. This error signal is applied to the input of a PI controller and the output of a PI controller given to the limiter and it regulate the duty cycle [20].

5.2.2 Feed-Forward Control

To minimize the ripple content from the output voltage and current feed forward method is used. The effect of input voltage variation on the output voltage can be minimized by implementing input voltage feed-forward control. It is easy to implement feed-forward control when using a digital controller with input voltage sense, compared to using an analog control method. In the feed-forward control method, the digital controller starts taking the appropriate adaptive action as soon as any

change is detected in the input voltage, before the change in input can actually affect the output parameters [5].

5.3 Simulation of 500 A and 30 V Power Supply with 18 kHz Switching Frequency

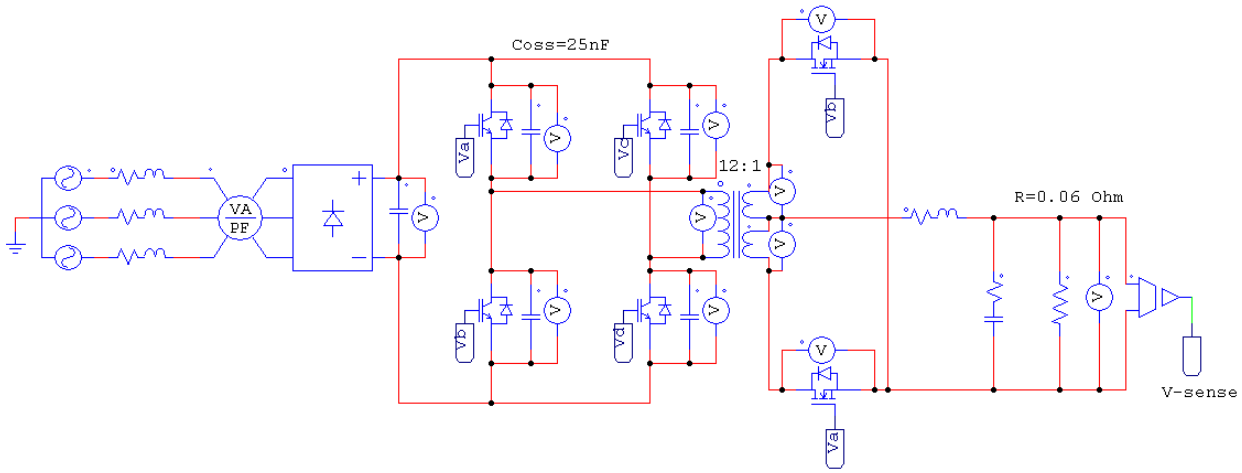

Figure 5.2: Simulation Diagram of 500 A and 30 V DC Power Supply

5.2 and 5.3 shows that the closed loop Simulation Diagram of 500 A and 30 V power supply. In this 5.4 is Gate pulse generation circuit.

5.5 shows that the maximum phase shifting between s/w a & d, Due to higher leakage inductance there is a duty loss in the transformer secondary voltage.

5.6 and 5.7 shows that the ZVS is achieved at s/w a & c, so before the gate pulse is given to the switch its drain to source voltage becomes zero and its body diode is conducting.

5.8 shows that input current and transformer primary current and 5.9 shows that Output Current and Output Voltage at full load and max. duty cycle.

5.10 shows that Reference signal compared with error signal and gate pulse of switch. 5.11 shows that there is a dead band between s/w a & b and s/w c & d.

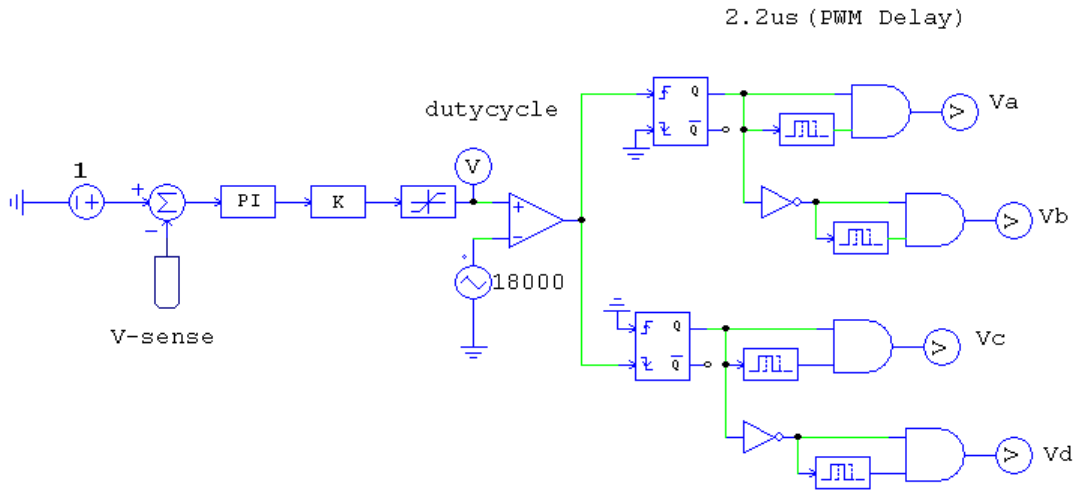

Figure 5.3: Gate pulse generation circuit

5.13 and 5.14 shows that there is a current flowing through source to drain direction.

5.15 shows that the current flowing through inductor and voltage across inductor, its frequency is doubled (36 kHz) due to center-tap high frequency. 5.16 shows that there is a ripple content in output voltage and output current.

5.17 shows that the Feed Forward method which is used to minimize the output ripple from the DC-link.5.18 shows that Output voltage and output current with 40mv ripple at 100% load(R=1Ω)

5.19 shows that Output voltage and output current with 40mv ripple at 75% load(R=1.33Ω). 5.20 shows that Output voltage and output current with 40mv ripple at 50% load(R=2Ω).

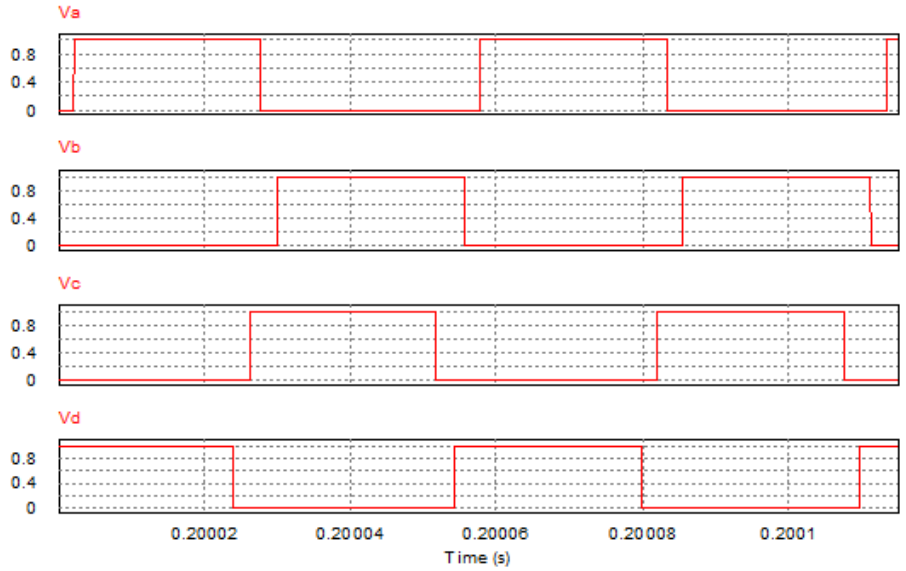

Figure 5.4: Gate pulses For IGBTs at full load and minimum phase shifting V_{duty}=0.44
X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V

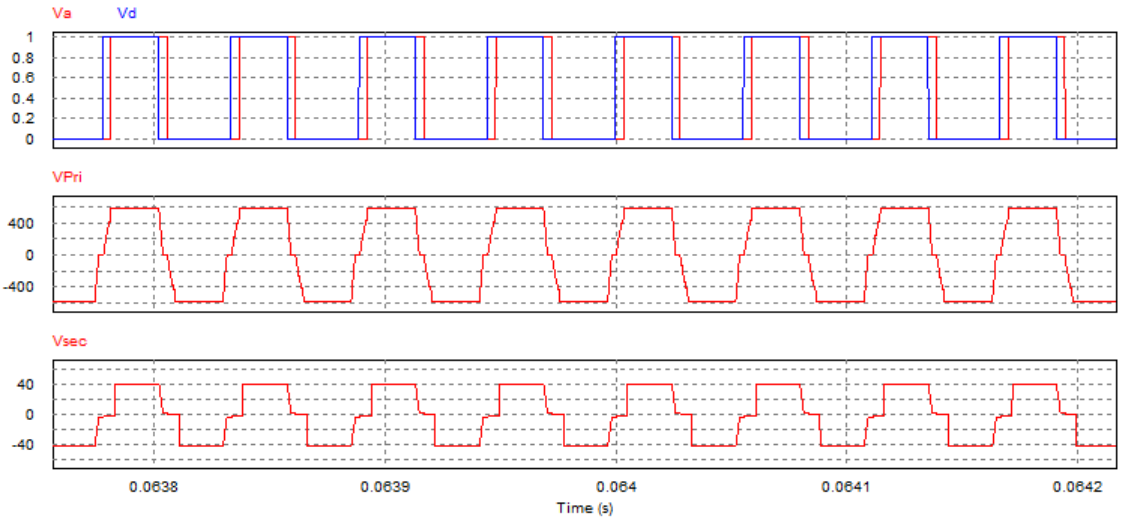

Figure 5.5: Phase shift in duty cycle, Transformer Primary Voltage, Transformer Secondary Voltage
Gate Pulses: X-axis: 1 div: 20μs, Y-axis: 1 div: 0.2 V
Transformer Primary Voltage: X-axis: 1 div: 20 μs, Y-axis: 1 div: 200 V
Transformer Secondary Voltage:X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 V

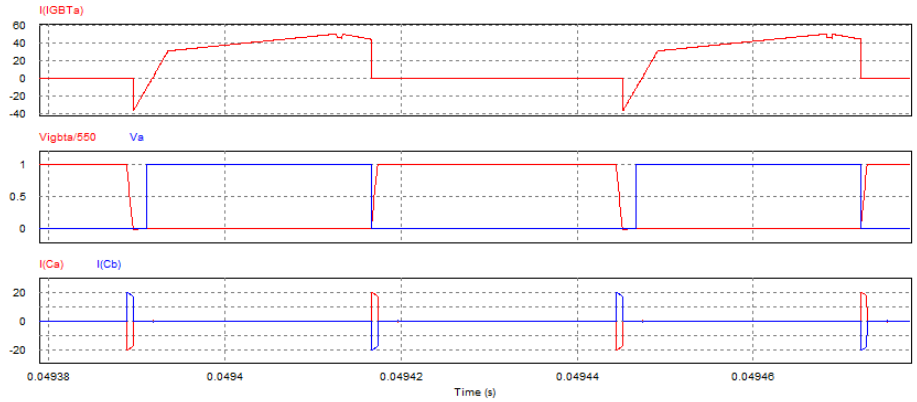

Figure 5.6: Current flowing through IGBTa, Zero Voltage Switching across IGBTa, Current flowing through capacitor a & b

Current flowing through IGBT a: X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 A
Zero Voltage Switching across IGBT a: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.5 V
Current flowing through capacitor a & b: X-axis: 1 div: 20 μs, Y-axis: 1 div: 10 A

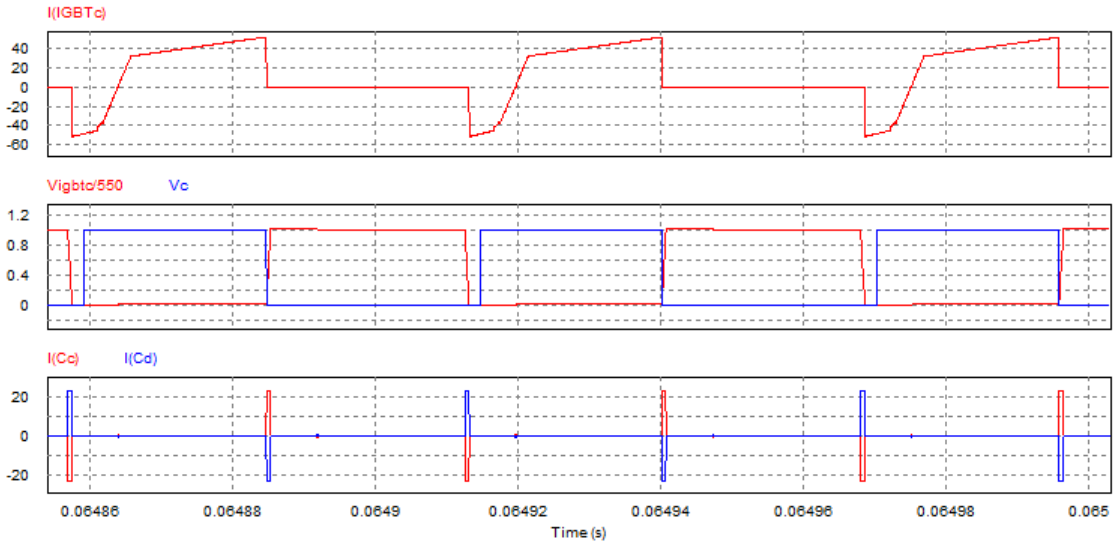

Figure 5.7: Current flowing through IGBTc, Zero Voltage Switching across IGBTc, Current flowing through capacitor c & d

Current flowing through IGBT c: X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 A
Zero Voltage Switching across IGBT c: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V
Current flowing through capacitor c & d: X-axis: 1 div: 20 μs, Y-axis: 1 div: 10 A

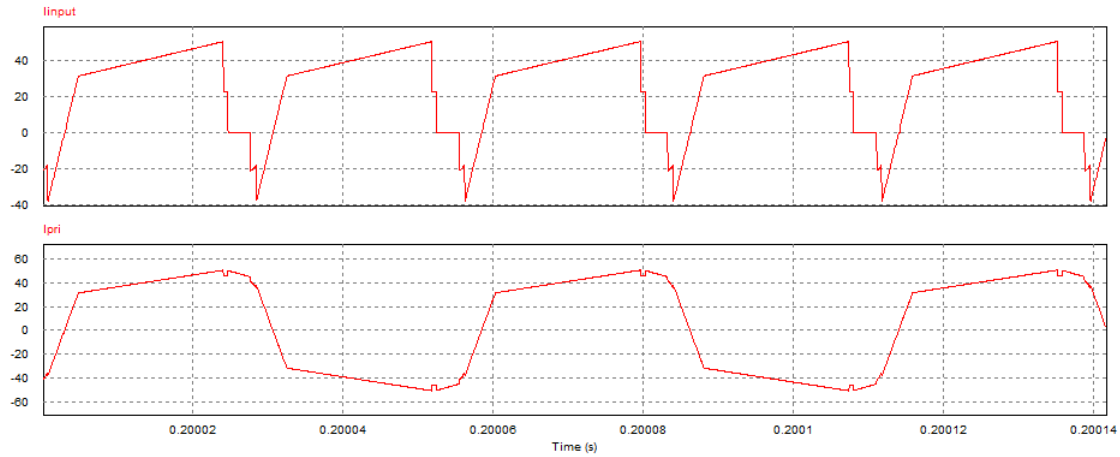

Figure 5.8: Input current, Transformer primary current
Iutput Current: X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 A
Transformer primary current : X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 A

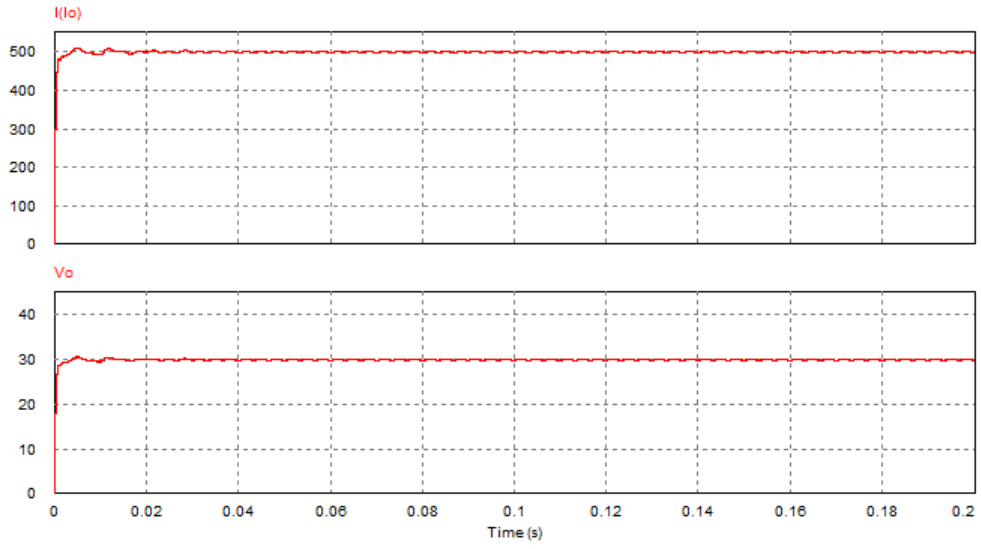

Figure 5.9: Output Current and Output Voltage at full load and max. duty cycle
Output Current: X-axis: 1 div: 20 μs, Y-axis: 1 div: 100 A
Output Voltage: X-axis: 1 div: 20 μs, Y-axis: 1 div: 10 V

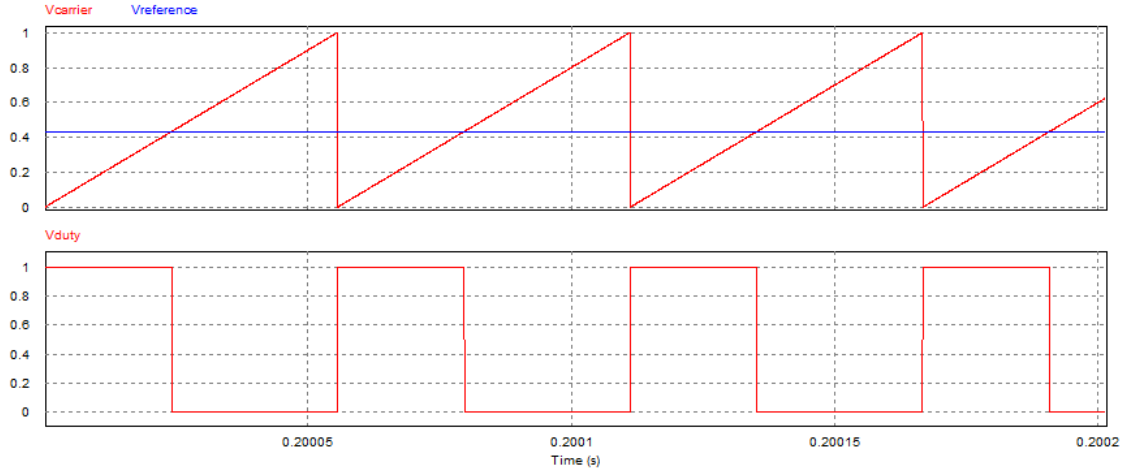

Figure 5.10: Reference signal compared with error signal, Compared pwm pulse
Carrier Signal: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V
Gate Pulse: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V

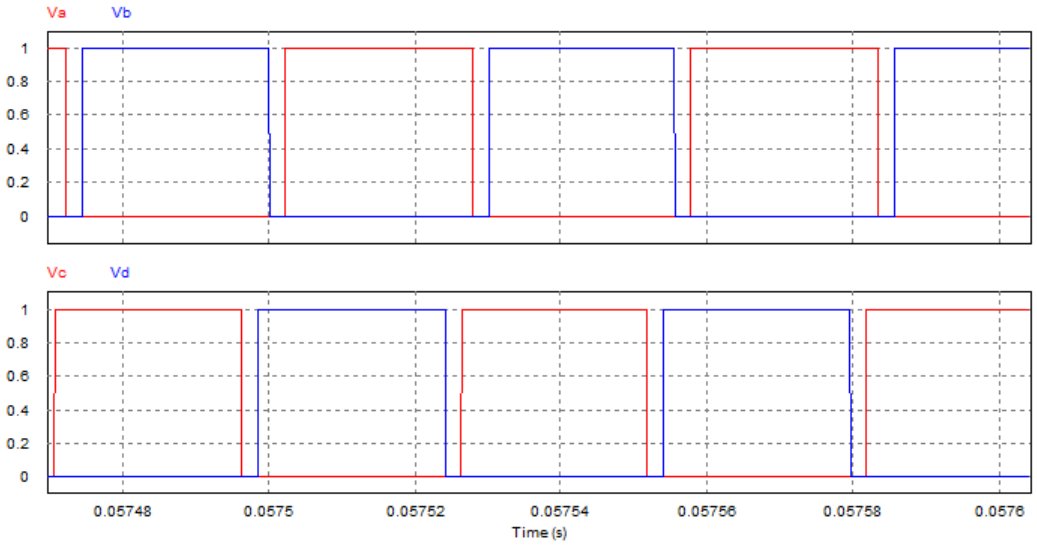

Figure 5.11: PWM Delay of 2.2 us between IGBT a & b, IGBT c & d
Dead band: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V

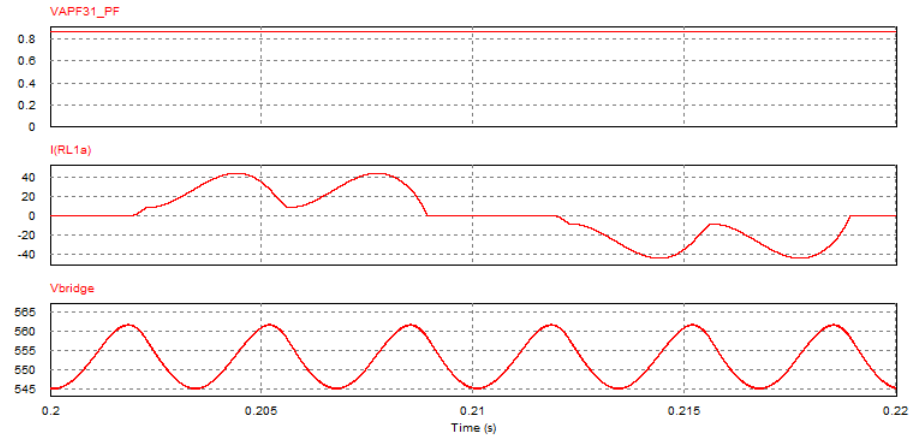

Figure 5.12: input Power factor, current flowing through line choke, Voltage across diode bridge

input Power factor: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V

current flowing through line choke: X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 A

Voltage across diode bridge: X-axis: 1 div: 20 μs, Y-axis: 1 div: 5 V

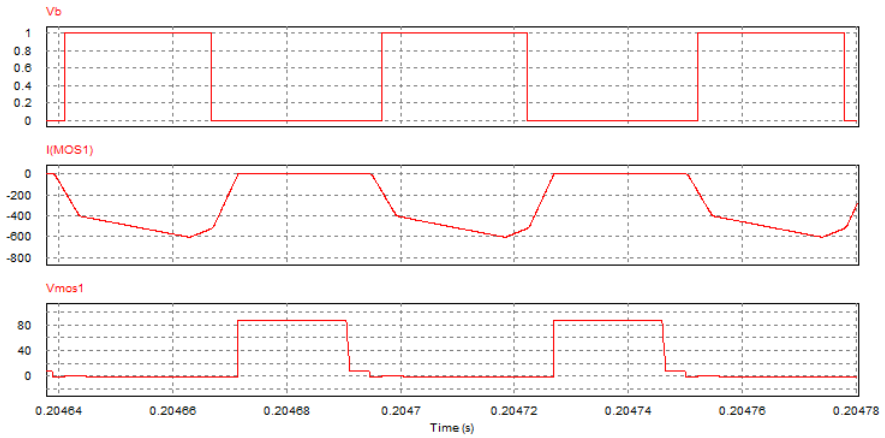

Figure 5.13: gate pulse for MOSFET1, current flowing through MOSFET1, Voltage across MOSFET1

Gate pulse for MOSFET1: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V

current flowing through MOSFET1: X-axis: 1 div: 20 μs, Y-axis: 1 div: 200 A

Voltage across MOSFET1: X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 V

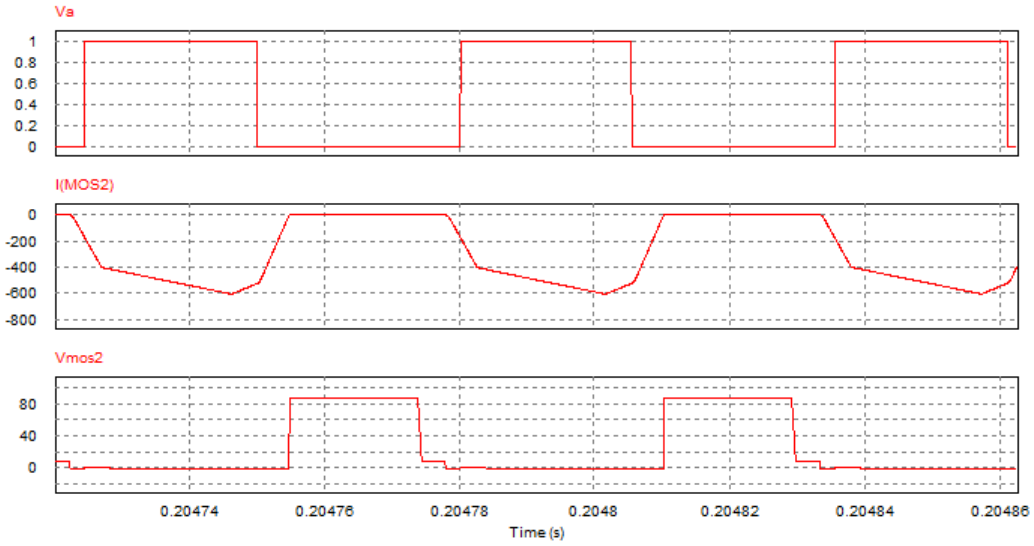

Figure 5.14: gate pulse for MOSFET2,current flowing through MOSFET2, Voltage across MOSFET2

Gate pulse for MOSFET2: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V
current flowing through MOSFET2: X-axis: 1 div: 20 μs, Y-axis: 1 div: 200 A
Voltage across MOSFET2: X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 V

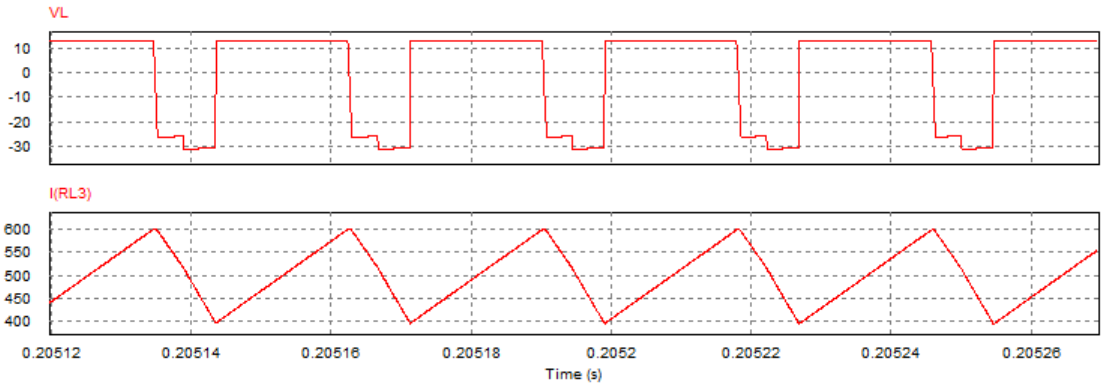

Figure 5.15: Inductor voltage and Inductor current
Inductor voltage: X-axis: 1 div: 20 μs, Y-axis: 1 div: 10 V
Inductor current: X-axis: 1 div: 20 μs, Y-axis: 1 div: 50 A

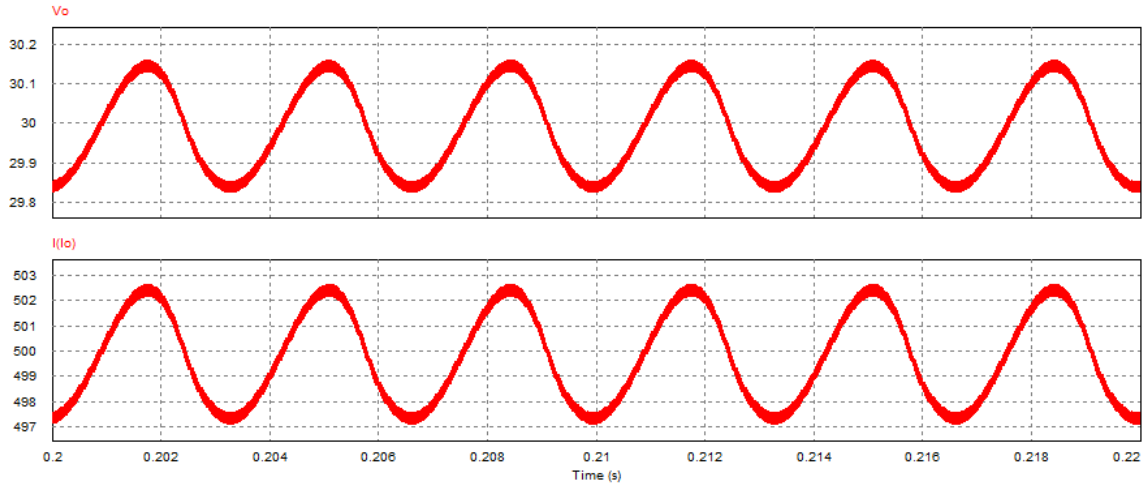

Figure 5.16: Output voltage and Output current with ripple
Output voltage: X-axis: 1 div: 2 ms, Y-axis: 1 div: 10 mV
Output current: X-axis: 1 div: 2 ms, Y-axis: 1 div: 0.2 A

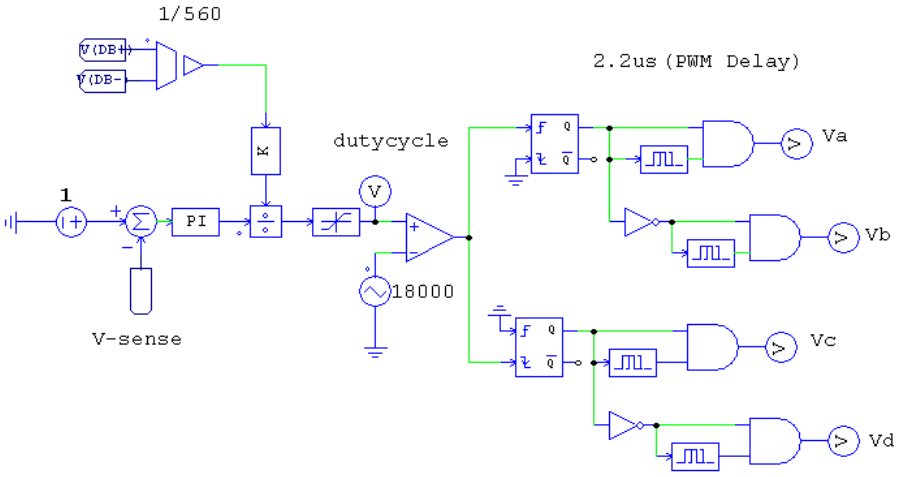

Figure 5.17: Feed-Forward method

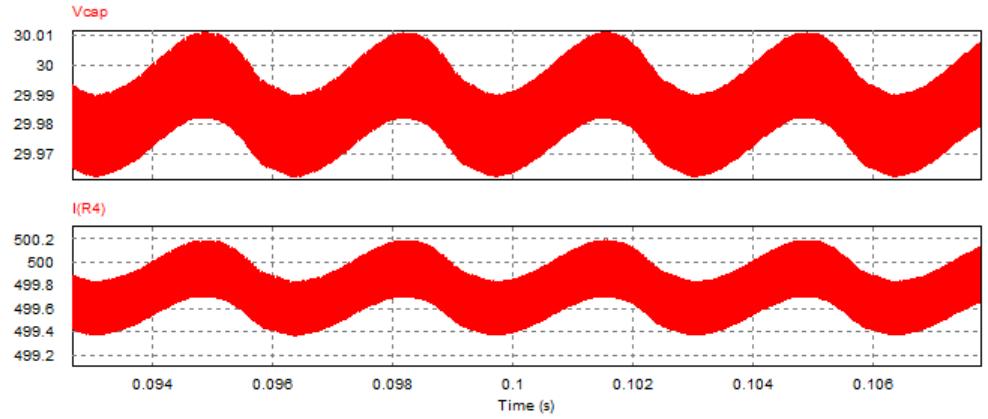

Figure 5.18: Output voltage and output current with 40mv ripple at 100% load
Output voltage: X-axis: 1 div: 2 ms, Y-axis: 1 div: 10 mV
Output current: X-axis: 1 div: 2 ms, Y-axis: 1 div: 0.2 A

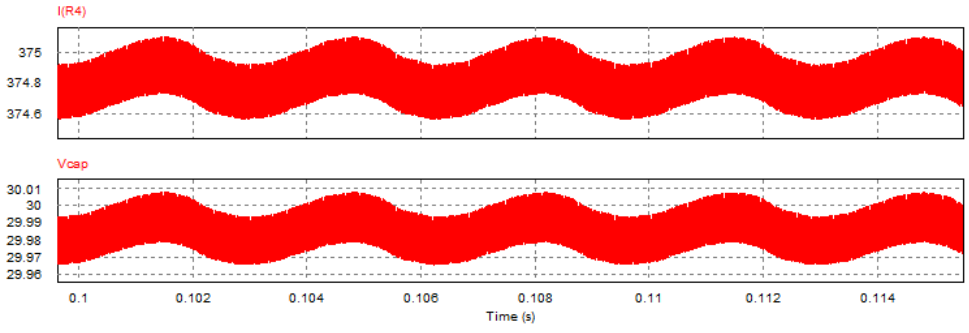

Figure 5.19: Output voltage and output current with at 75% load
Output voltage: X-axis: 1 div: 2 ms, Y-axis: 1 div: 10 mV
Output current: X-axis: 1 div: 2 ms, Y-axis: 1 div: 0.2 A

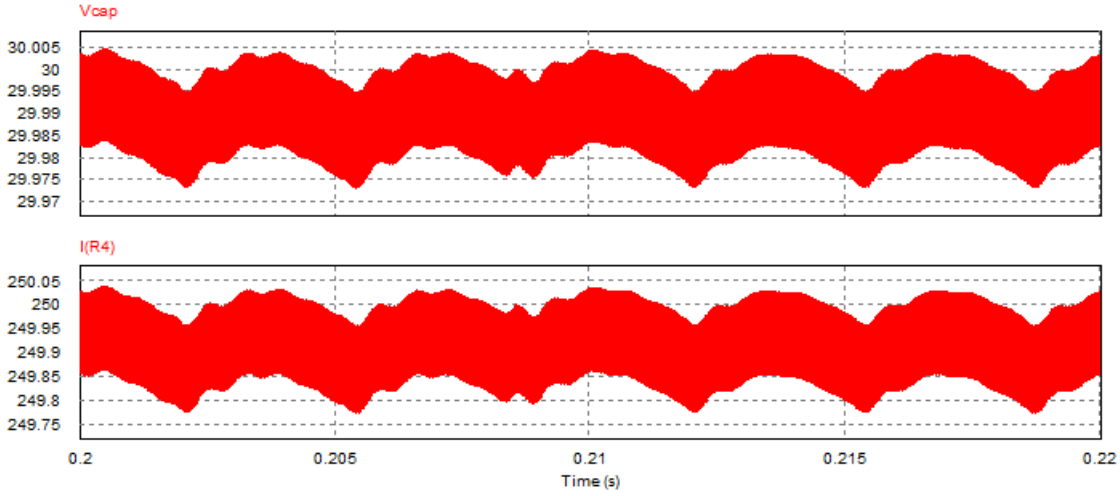

Figure 5.20: Output voltage and output current with at 50% load
Output voltage: X-axis: 1 div: 2 ms, Y-axis: 1 div: 10 mV
Output current: X-axis: 1 div: 2 ms, Y-axis: 1 div: 0.2 A

Chapter 6

Simulation of 900 W Prototype Power supply with DLL

6.1 Simulation of Close-Loop Control through DLL Block

PSIM software provides facility to incorporate software part with hardware part. This helps to interface actual control logic through programming with DSP. It gives more realistic results as compared to discrete component circuit. For the implementation of close-loop control logic,a simulation block called DLL block is used. This block receives n inputs,process it according to the written C-program linked with it and provides specific output as per program logic. This block allows to write control logic in own code in C,compile it into the DLL block and link it with PSIM. PSIM calls the DLL routine at each simulation time step.

6.1 shows that the closed loop Simulation Diagram of 30 A and 30 V power supply with DLL block. In this 6.2 is Gate pulse generation circuit at Vref=1.

6.3 and 6.5 shows that the ZVS is achieved at s/w a & d, so before the gate pulse is given to the switch its drain to source voltage becomes zero and its body diode is conducting.6.4 shows that input current and transformer primary current

6.6 shows that Transformer Primary and tersary Voltage, due to higher leakage inductance there is a duty loss in the transformer tersary voltage.and 6.7 shows that Transformer Primary current, Secondary current and tersary current.

6.8 shows that Transformer Primary voltage and output voltage achieve at Vref=1, R(Load)=1Ω, Vduty=0.43 (So according to reference voltage, output voltage is settled down and there is a variation in phase shifting).

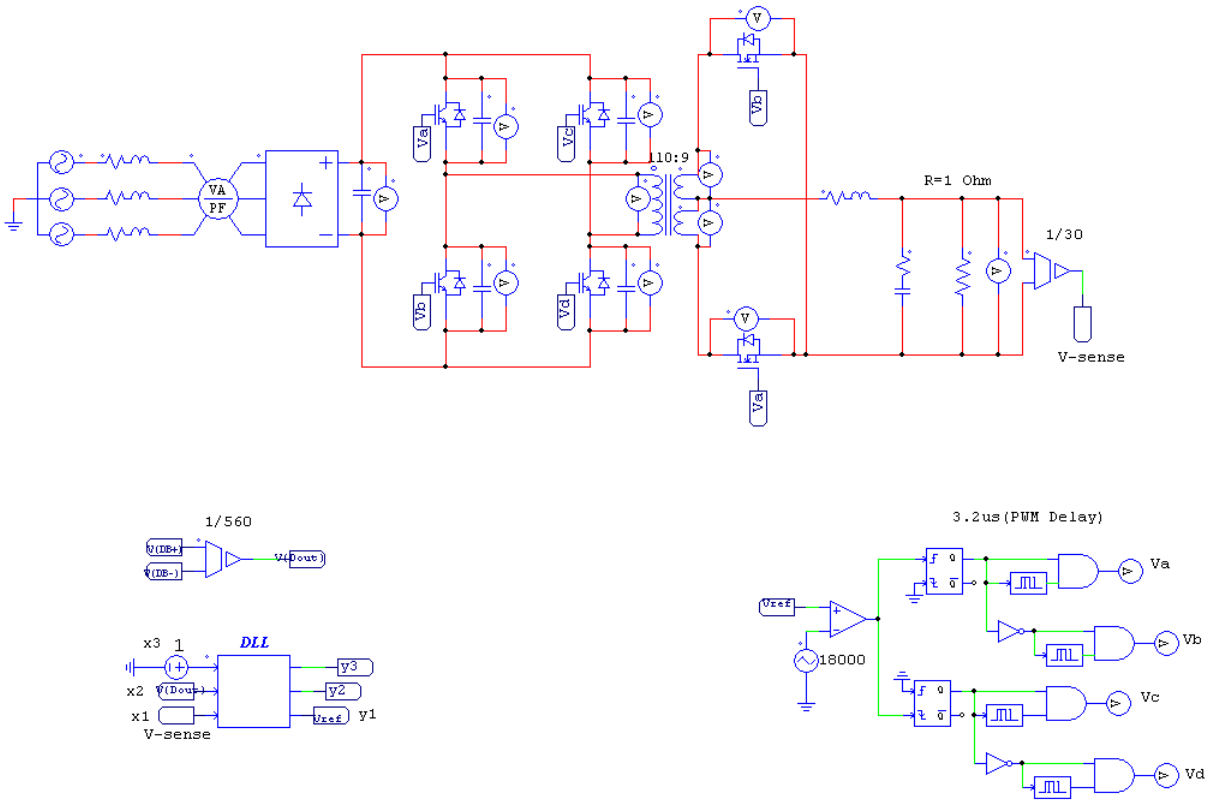

Figure 6.1: Simulation of close loop circuit with DLL block

6.9 shows that Transformer Primary voltage and output voltage achieve at Vref=0.8, R(Load)=1Ω, Vduty=0.34

6.10 shows that Transformer Primary voltage and output voltage achieve at Vref=0.5, R(Load)=1Ω, Vduty=0.21

6.11 shows that Transformer Primary voltage and output voltage achieve at Vref=0.3, R(Load)=1Ω, Vduty=0.10

6.12 shows that there is output voltage and output current at full load.6.13 shows that Output voltage and output current with 40mv ripple at 100% load(R=1Ω)

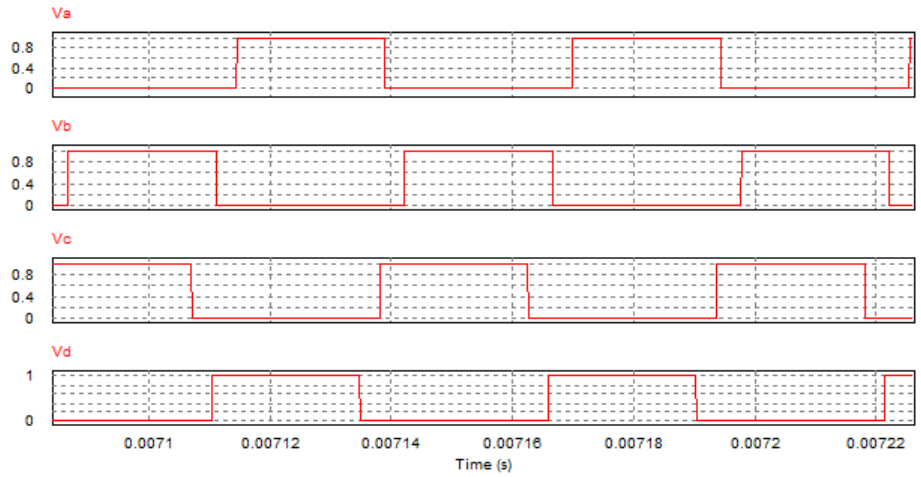

Figure 6.2: Gate Pulse Generation Circuit at Vref=1
X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V

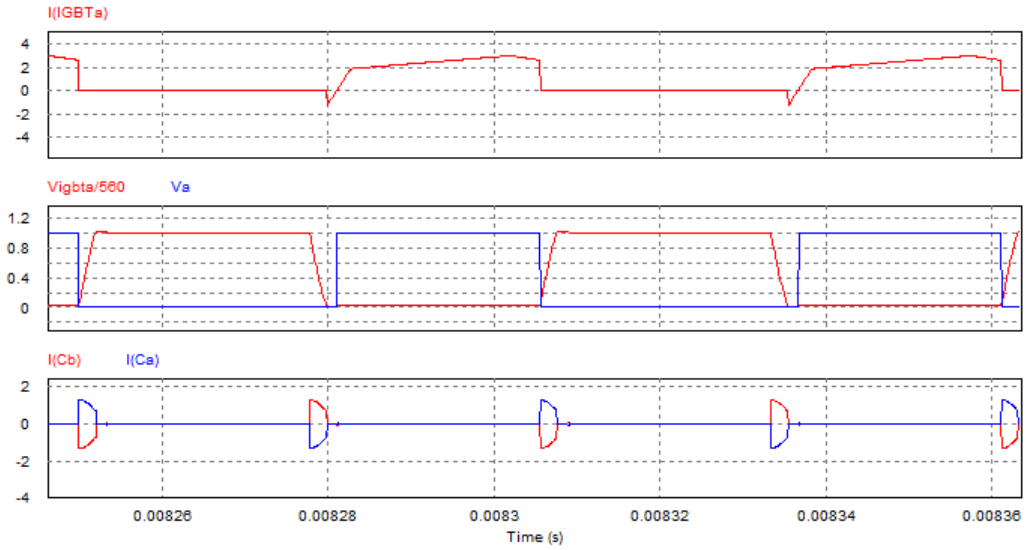

Figure 6.3: Current flowing through IGBT a,Zero voltage switching across IGBT a & gate pulse for Switch a, Current flowing through capacitor a & b
Current flowing through IGBT a: X-axis: 1 div: 20 μs, Y-axis: 1 div: 2 A
Zero Voltage Switching across IGBT a: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V
Current flowing through capacitor a & b: X-axis: 1 div: 20 μs, Y-axis: 1 div: 2 A

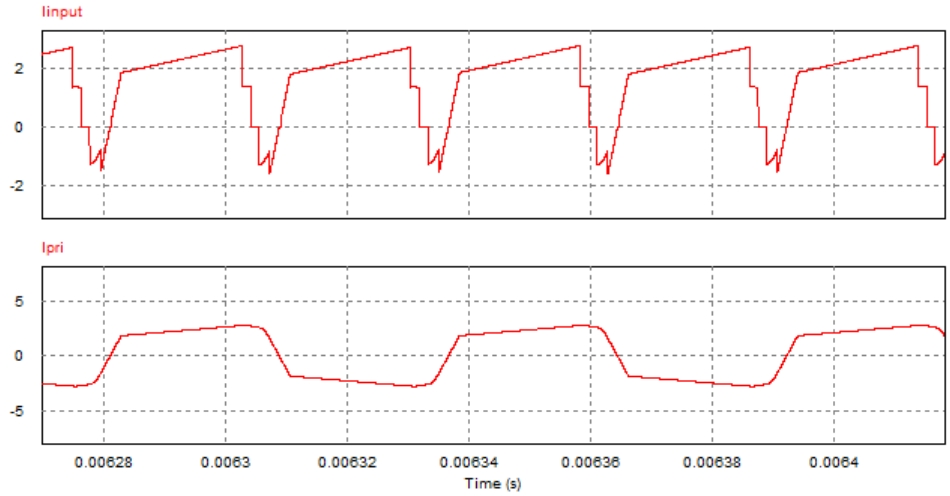

Figure 6.4: Input current,primary current
Input current: X-axis: 1 div: 20 μs, Y-axis: 1 div: 2 A
Primary Current of Transformer: X-axis: 1 div: 20 μs, Y-axis: 1 div: 5 A

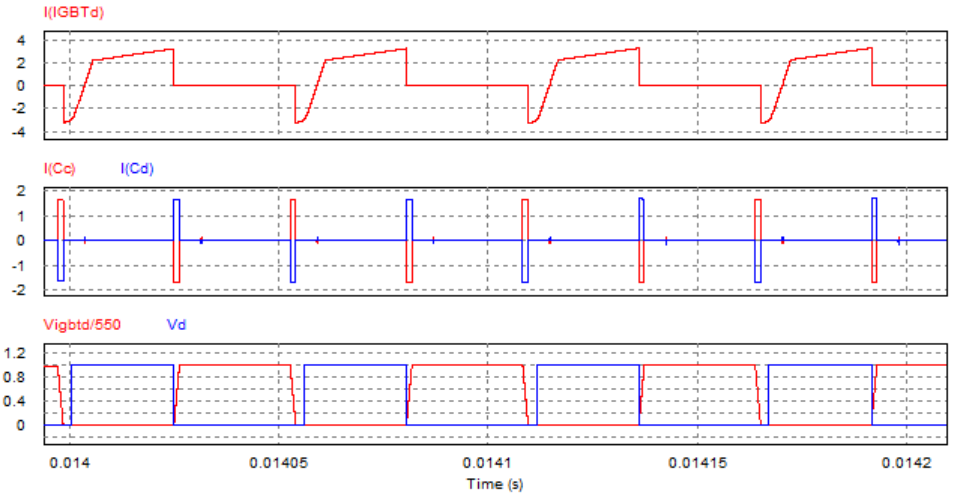

Figure 6.5: Current flowing through IGBTd, Zero voltage switching across IGBTd & gate pulse for Switch d, Current flowing through c & d
Current flowing through IGBT d: X-axis: 1 div: 20 μs, Y-axis: 1 div: 2 A
Zero Voltage Switching across IGBT d: X-axis: 1 div: 20 μs, Y-axis: 1 div: 0.2 V
Current flowing through capacitor c & d: X-axis: 1 div: 20 μs, Y-axis: 1 div: 2 A

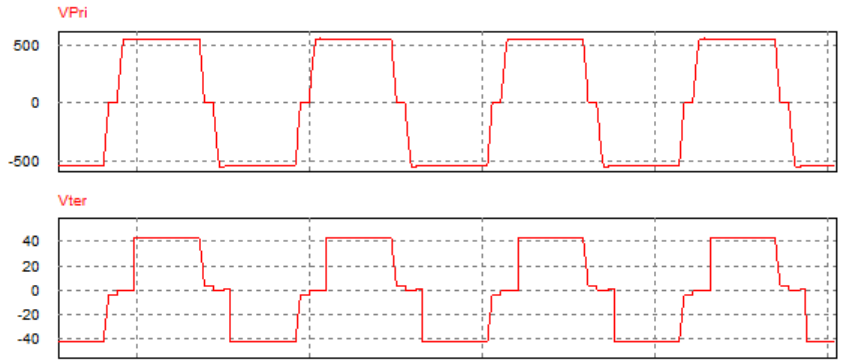

Figure 6.6: Transformer Primary and tersary Voltage
Transformer Primary Voltage: X-axis: 1 div: 20 μs, Y-axis: 1 div: 500 V
Transformer Secondary Voltage:X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 V

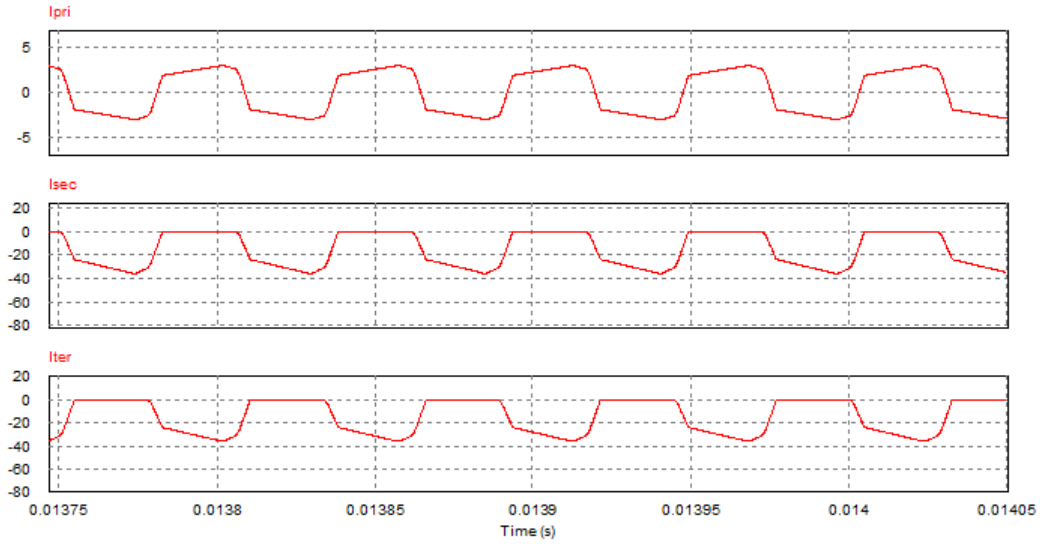

Figure 6.7: Primary current, Secondary current and tersary current
Transformer Primary Current: X-axis: 1 div: 20 μs, Y-axis: 1 div: 5 A
Transformer Secondary Current:X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 A
Transformer Tersary Current:X-axis: 1 div: 20 μs, Y-axis: 1 div: 20 A

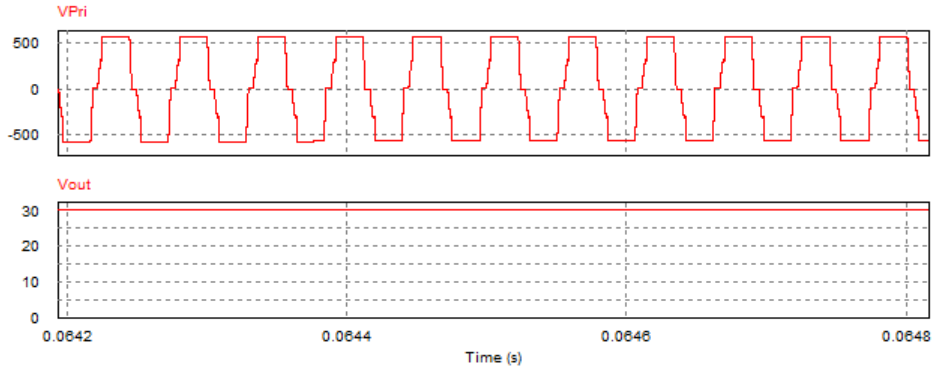

Figure 6.8: Transformer primary voltage and output voltage at Vref=1, Vduty=0.43 and Vout=30V

O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:5 V

Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:500 V

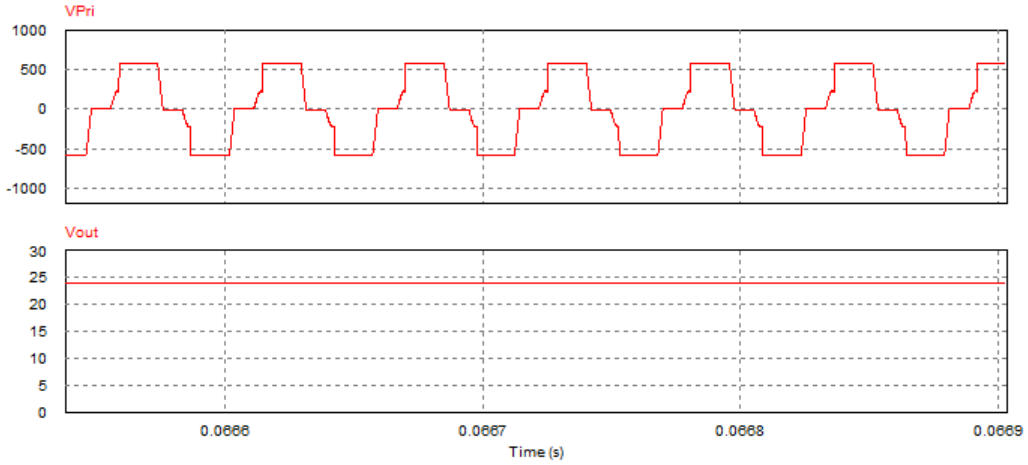

Figure 6.9: Transformer Primary Voltage and Output Voltage at Vref=0.8, Vduty=0.34 and Vout=24V

O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:5 V

Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:500 V

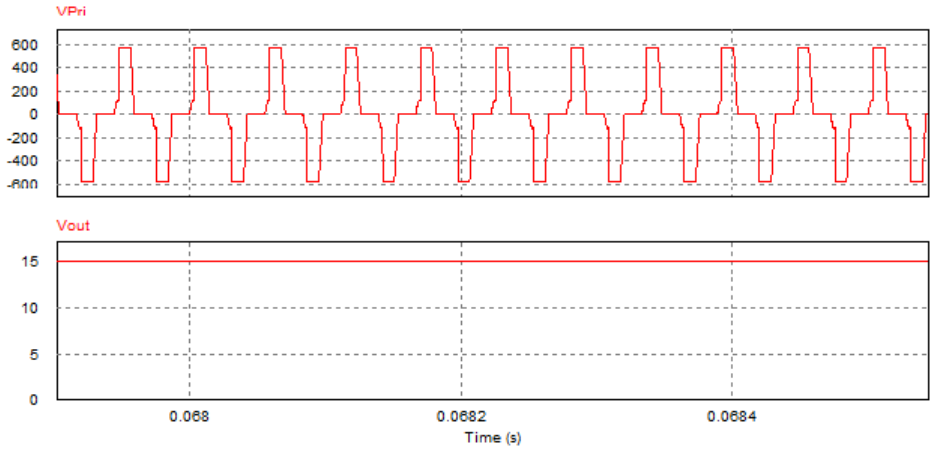

Figure 6.10: Transformer Primary Voltage and Output Voltage at Vref=0.5, Vduty=0.21 and Vout=15V

O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:5 V

Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:200 V

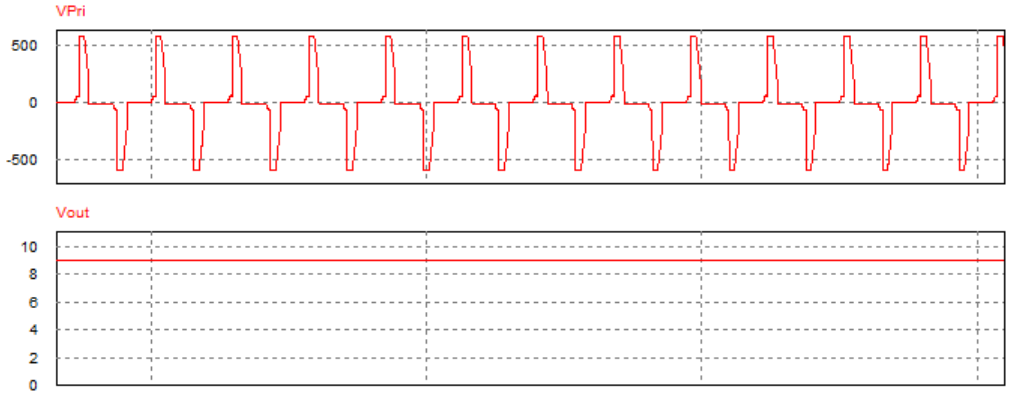

Figure 6.11: Transformer primary voltage and output voltage at Vref=0.3, Vduty=0.10 and Vout=9V

O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:2 V

Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:500 V

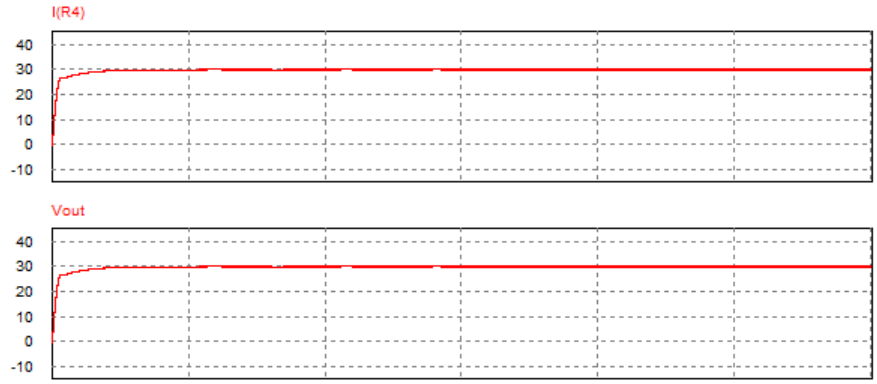

Figure 6.12: Output Voltage and Current at full load
Output voltage: X-axis: 1 div: 2 ms, Y-axis: 1 div: 10 mV
Output current: X-axis: 1 div: 2 ms, Y-axis: 1 div: 0.2 A

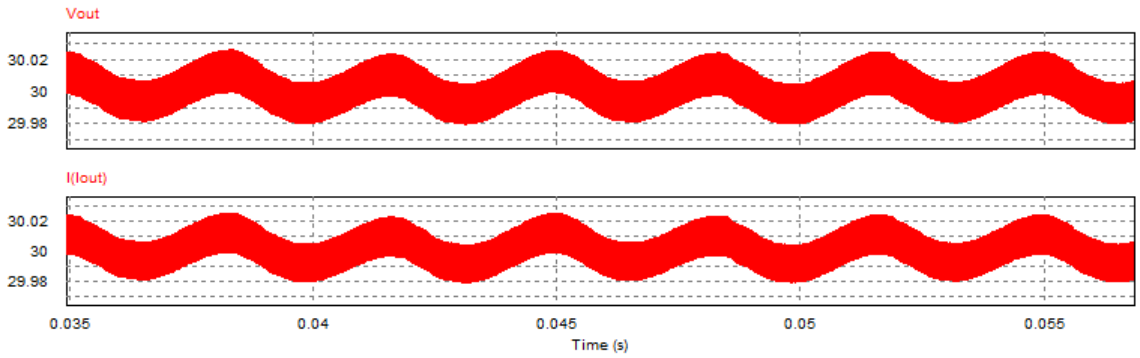

Figure 6.13: Output voltage and Current with 40 mv (Peak-Peak) ripple
Output voltage: X-axis: 1 div: 5 ms, Y-axis: 1 div: 20 mV
Output current: X-axis: 1 div: 5 ms, Y-axis: 1 div: 20 mA

Chapter 7

Hardware Results of 900 W in Open-Loop Control

7.1 Theoritical Calculation of Losses

7.1.1 Total Losses of IGBT

[1]Conduction losses of IGBT

$$Avg.conductionlosses = (V_{CEO}I_{avg} + r_c I_{rms^2}) \times D \tag{7.1}$$

Avg. conduction losses=2 W

[2]Switching losses of IGBT

$$TurnONlosses = \frac{1}{6} \times V_{CE(max)} \times I_{c(max)} \times D \times t_r \tag{7.2}$$

Turn ON losses=3.5 W

$$TurnOFFlosses = \frac{1}{6} \times V_{CE(max)} \times I_{c(max)} \times (1 - D) \times t_f \tag{7.3}$$

Turn OFF losses=4.1 W

7.1.2 Losses Of Mosfet

Conduction losses of Mosfet

$$P_{con} = (I_{rms^2} R_{ds(on)}) \times D \tag{7.4}$$

$P_{con} = 2.16W$

Suppose We used Schottkey Diode in place of Mosfet then its conduction losses becomes:

7.1.3 Losses Of Schottkey Diode

$$P_{con} = (V_{do} I_{avg} + r_d I_{rms^2}) \times D \tag{7.5}$$

$P_{con} = 7.58W$

7.2 Practical Results of Conduction losses

Table I: Conduction Losses of Schottky Diode(DSS2x101-02A)

Current (A)	Voltage drop (V)	Conduction loss (W)
6	0.581	3.42
12	0.638	7.6
18	0.665	11.84
24	0.680	16.25

Table II: Conduction Losses of MOSFET (IRFP4668PbF)

Current(A)	Voltage drop(V)	Conduction loss(W)
6	0.11	0.66
12	0.157	1.91
18	0.223	4.014
24	0.332	7.9

So from this comparison it is prove that Mosfet Conduction losses are less than Diode Conduction Losses [22].

7.3 Complete Circuit Diagram of Hardware Setup

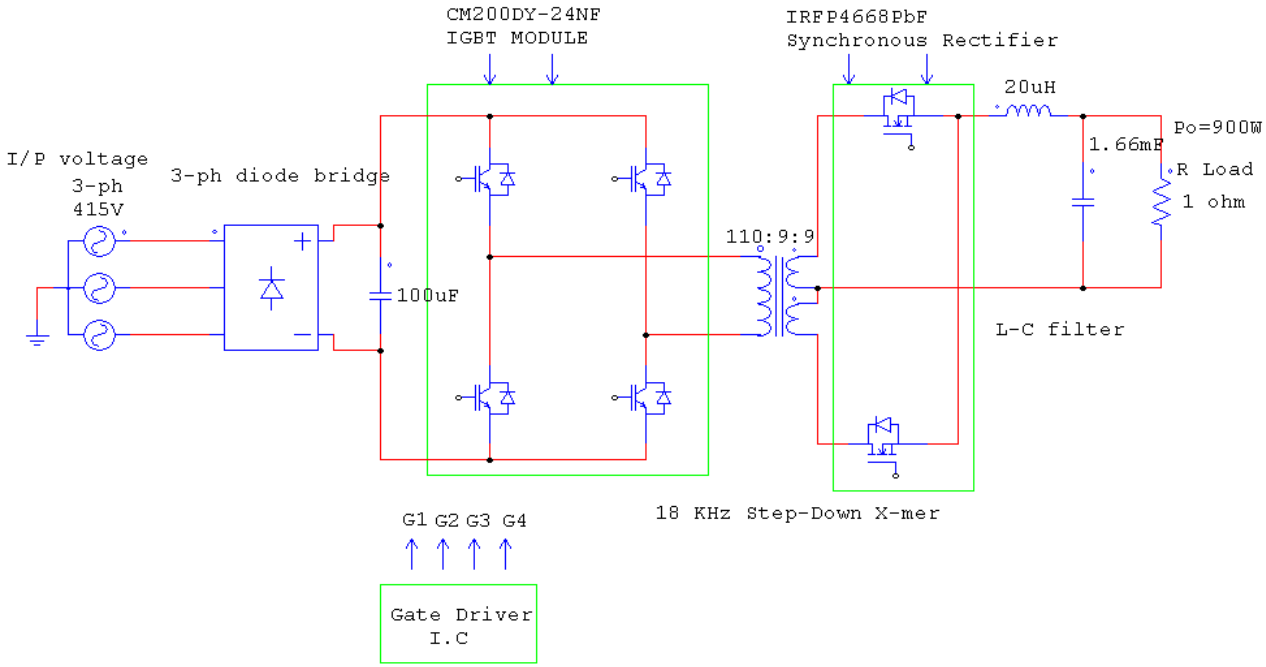

Figure 7.1: Circuit of Hardware Setup for 900W Isolated DC Power Supply

Due to variation in input voltage, load and in phase shifting, there is a change in output voltage at fixed switching frequency. This hardware results in open loop control, the readings are at 1Ω load(100%load) and 18 kHz switching frequency.

- Input voltage=405 V(rms)
- Input current=2.4 A(rms)
- Switching Frequency=18000 Hz
- Diode bridge output=572 V(DC)
- Output Voltage=30.15 V
- Output Current=30.6 A
- Load=1Ω

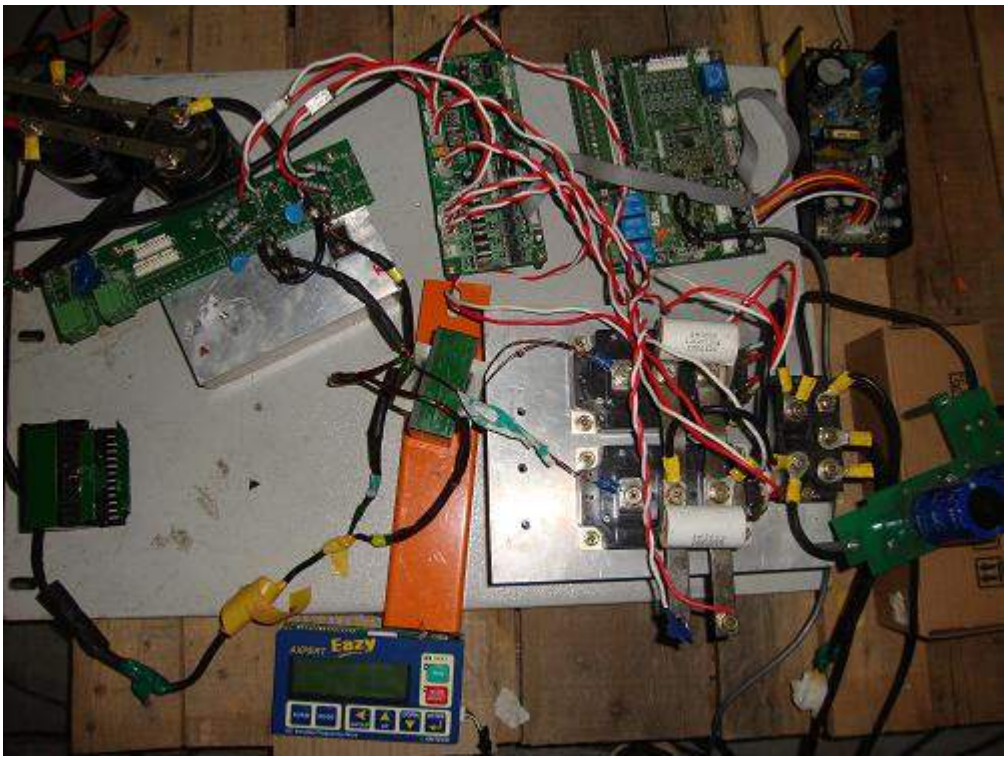

Figure 7.2: Hardware Setup

7.1 shows that the open loop Block Diagram of 30 A and 30 V DC power supply.7.2 shows that the open loop hardware setup of 30 A and 30 V DC power supply.

7.4 shows that Gate pulse with the amplitude of 19.4 V and 7.5 shows that Gate pulse of 18KHz Switching frequency.

7.6 shows that there is a ($3.2\mu s$) of dead band between s/w a&b and s/w c&d. 7.7 shows that Voltage across IGBT a (Here shows that there is no spike across the IGBT during turn off process)

7.8 shows that gate pulses of s/w a and d at 40% phase shifting, 7.9 shows that transformer primary current.

7.10 shows that transformer primary voltage at 40% phase shifting of s/w a and d and 7.11 shows that transformer secondary voltage at 40% phase shifting of s/w a and d.

7.12 shows that the output voltage across the load (R=1Ω), 7.13 shows that the voltage across the MOSFET.

7.14 shows that that the ZVS is achieved at s/w a, so before the gate pulse is given to the switch its drain to source voltage becomes zero and its body diode is conducting. so turn on losses are eliminated.

7.15 shows that transformer tersary voltage and gate pulse of MOS 2 (So here to get the desire output, we have to synchronize the gate pulses of MOS 1 with transformer secondary voltage and gate pulses of MOS 2 with transformer tersary voltage so on secondary side it is called synchronous rectifier)

7.16 shows that gate pulses of s/w b and Voltage across IGBT b at R=2Ω (So at that time energy is not sufficient on primary side so ZVS cannot be achieved) and 7.17 shows that output voltage across Load (Vout=30 V) at R=2Ω (this circuit is works on constant voltage mode so at R=2Ω it can achieve the 30 V at Vref=1)

7.4 Need Of Snubbers

Snubbers are circuits which are placed across semiconductor devices for protection and to improve performance.Snubbers can do many things:

- Reduce or eliminate voltage and current spikes.
- Limit di/dt or dv/dt.
- Shape the load line to keep it within the safe operating area (SOA).
- Transfer power dissipation from the switch to a resistor.

- Reduce total losses due to switching.
- Reduce EMI by damping voltage and current ringing.

7.4.1 Design of RC Snubber

A RC snubber, placed across the switch can be used to reduce the peak voltage at turn-off and to damp the ringing. A small RC turn-off snubber can be used to prevent voltage spikes and voltage oscillations across a MOSFET during device turn-off. The large peak current handling capability of the MOSFET and the fact that switching speed can be easily controlled by controlling the gate current [24] [25].

Calculation of R_s and C_s

Choose a resistor of RC network that is non-inductive. so select a carbon composite resistor, wire wound type resistor can be avoided because it is inductive. Choose a capacitor which is able to withstand the high peak voltage and currents in snubbers [26].

To achieve a significant damping Cs must be equal to twice the output capacitance of the switch. So here selected value of Cs=10 nF

Assuming worst condition of voltage spikes across the switch turn-off is 150V, due to that time peak current flows through RC snubber.

$$R_s = \frac{V_{peak}}{I_{peak}} \tag{7.6}$$

From the 7.6 equation, R_s=28 Ω

So when Cs is charged and discharged then the power dissipation in Rs at given switching frequency is:

$$P_{diss} = \frac{1}{2} \times C_s \times V_{peak^2} \times F_s \tag{7.7}$$

P_{diss}=1.5 W

Depending upon ringing actual power dissipation is higher than calculated. So select the 5W Rating of R_s. 7.3 shows that Overall View of RC snubber

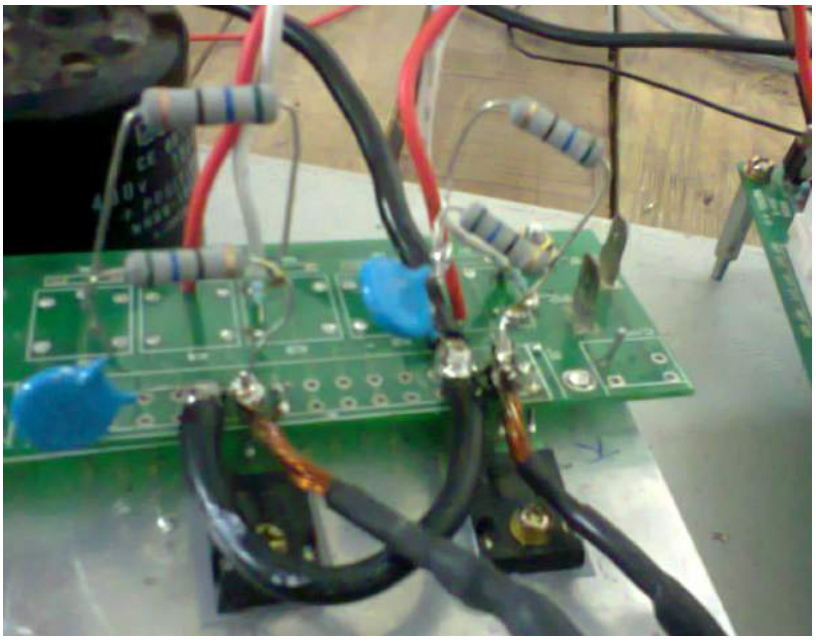

Figure 7.3: Overall View of RC snubber

Table III: R= 1Ω (Load) with MOSFET

I/P Voltage(rms)(V)	I/P Current (A)	O/P Voltage(V)	O/P Current (A)
29.74	0.21	1.73	1.74
93.5	0.43	6.65	6.87
176.3	0.92	13.01	13.71
248.9	1.38	18.55	19.4
308.7	1.9	23.15	23.8
396.8	2.4	30.15	31.3

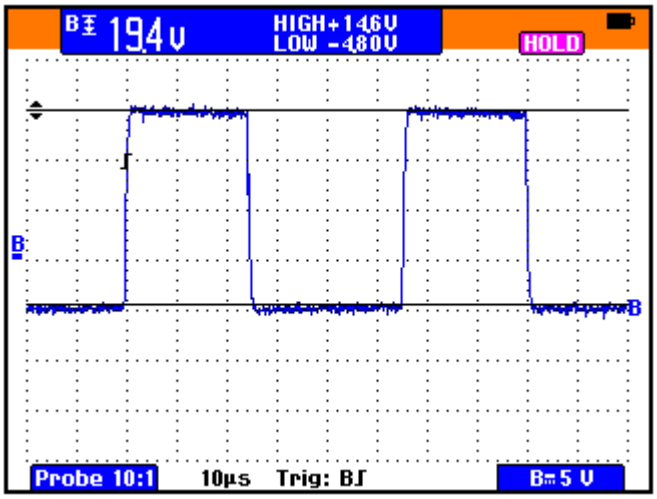

Figure 7.4: Gate pulse with the amplitude of 19.4 V
X-axis: 1 div: 10μs, Y-axis: 1 div: 5 V

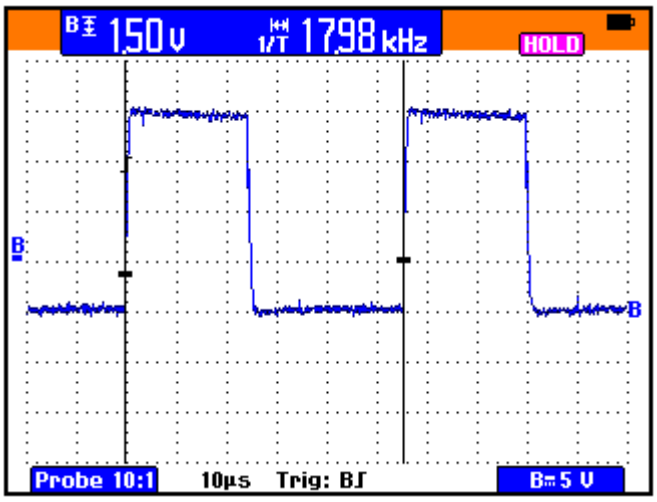

Figure 7.5: Gate pulse of 18KHz Switching frequency
X-axis: 1 div: 10μs, Y-axis: 1 div: 5 V

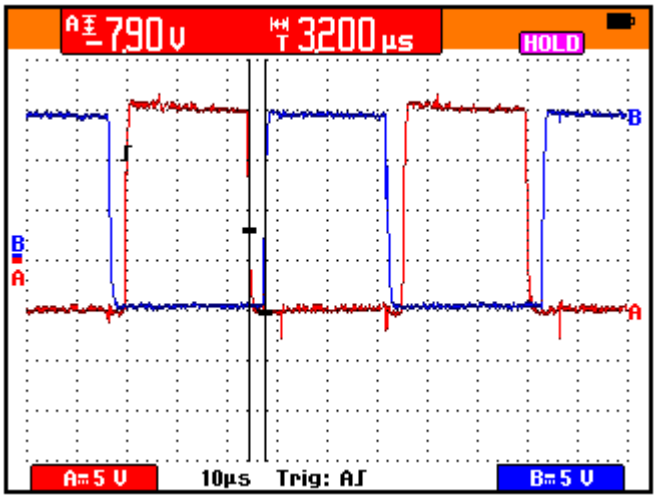

Figure 7.6: Deadband between s/w a&b and s/w c&d ($3.2\mu s$)
X-axis: 1 div: 10μs, Y-axis: 1 div: 5 V

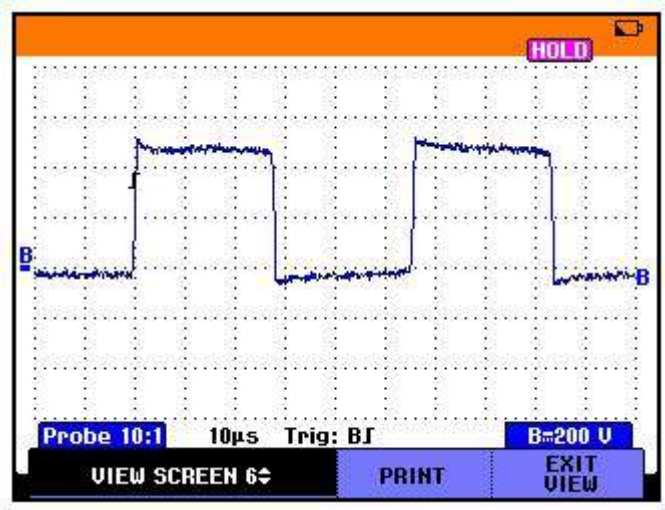

Figure 7.7: Voltage across IGBT a V_{IGBTa}=570 V
X-axis: 1 div: 10μs, Y-axis: 1 div: 200 V

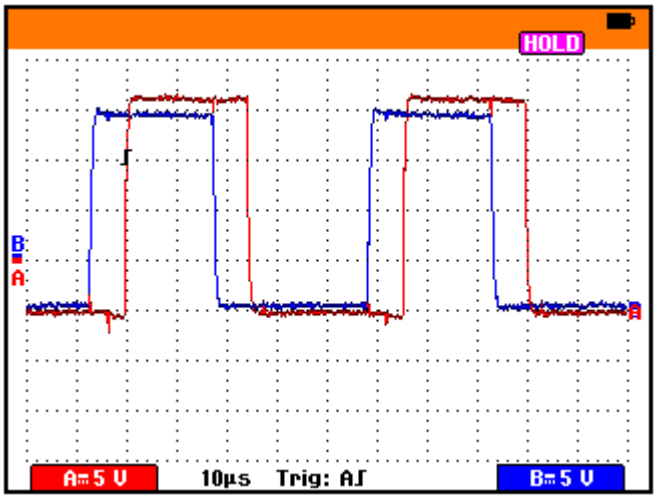

Figure 7.8: Gate pulses of s/w a and d at 40% phase shifting
Blue Colour:Gate pulses of s/w d:X-axis:1 div:10μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w a:X-axis:1 div:10μs, Y-axis:1 div:5 V

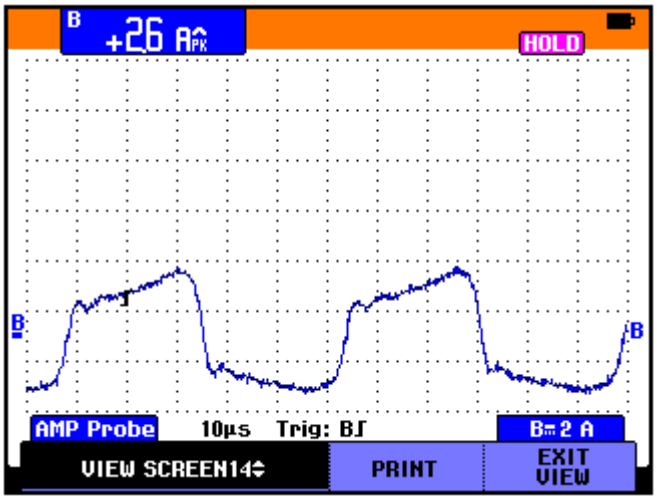

Figure 7.9: Transformer primary current
X-axis: 1 div: 10μs, Y-axis: 1 div: 2 A

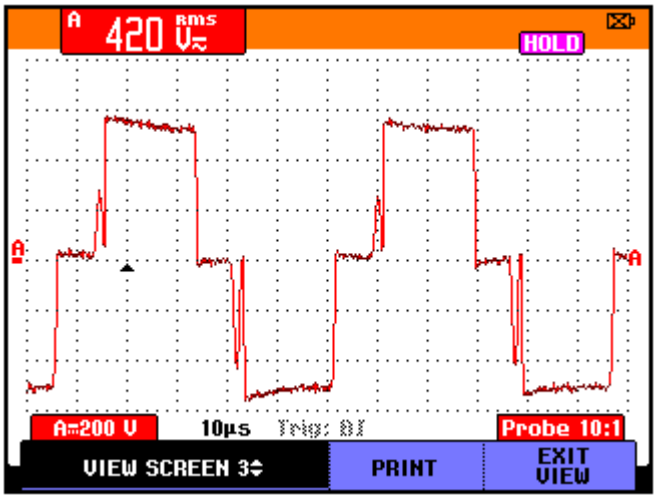

Figure 7.10: Transformer primary voltage at 40% phase shifting and V_{pri}=±570V
X-axis: 1 div: 10μs, Y-axis: 1 div: 200 V

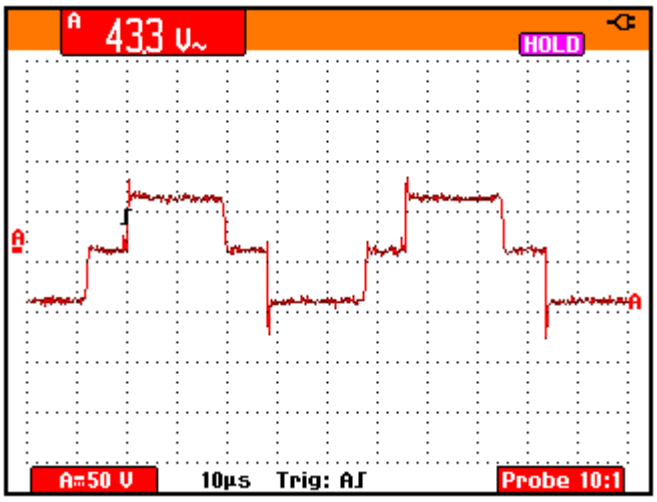

Figure 7.11: Transformer secondary voltage at 40% phase shifting and V_{sec}=±45V
X-axis: 1 div: 10μs, Y-axis: 1 div: 50 V

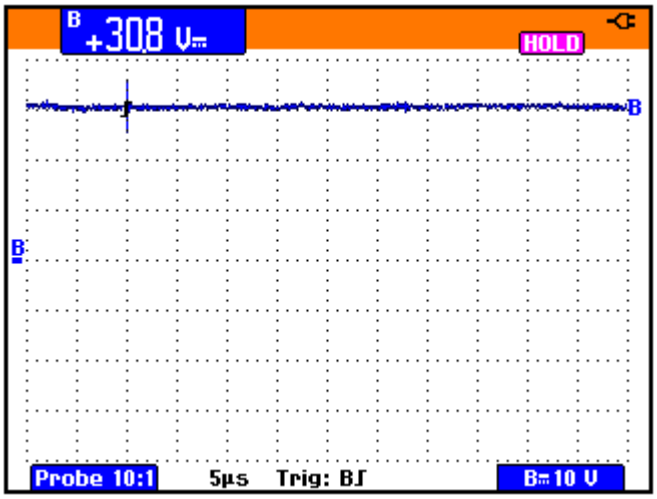

Figure 7.12: Output voltage across Load (Vout=30.8 V) at R=1Ω
X-axis: 1 div: 5μs, Y-axis: 1 div: 10 V

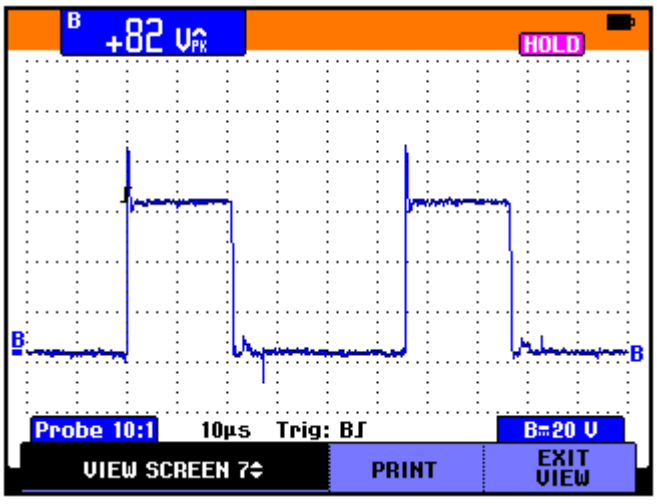

Figure 7.13: Voltage across MOS 1 V_{MOS1}=80V(Peak)
X-axis: 1 div: 10μs, Y-axis: 1 div: 20 V

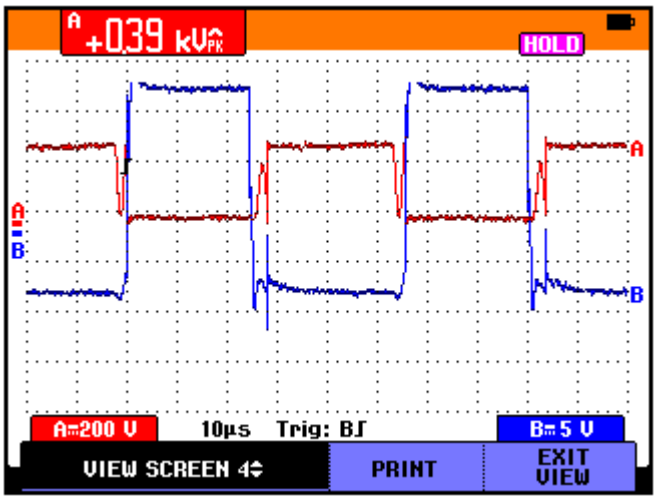

Figure 7.14: Gate pulses of s/w a and Voltage across IGBT a
Blue Colour:Gate pulses of s/w a:X-axis:1 div:10μs, Y-axis:1 div:5 V
Red Colour:Voltage across IGBT:X-axis:1 div:10μs, Y-axis:1 div:200 V

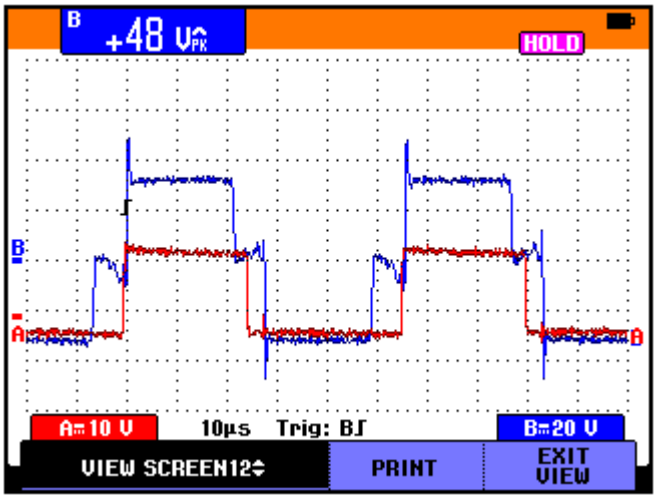

Figure 7.15: Transformer tersary voltage and Gate pulse of MOS 2
Blue Colour:Transformer tersary voltage: X-axis:1 div:10μs, Y-axis:1 div:20 V
Red Colour:Gate pulse of MOS 2: X-axis:1 div:10μs, Y-axis:1 div:10 V

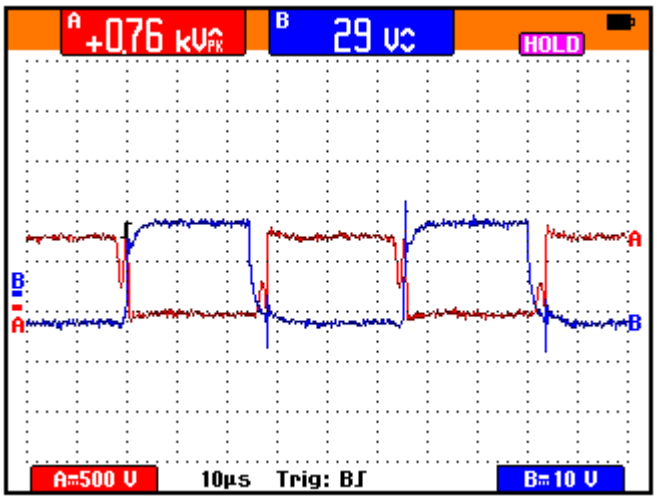

Figure 7.16: Gate pulses of s/w b and Voltage across IGBT b at R=2Ω
Blue Colour:Gate pulses of s/w a:X-axis:1 div:10μs, Y-axis:1 div:10 V
Red Colour:Voltage across IGBT:X-axis:1 div:10μs, Y-axis:1 div:500 V

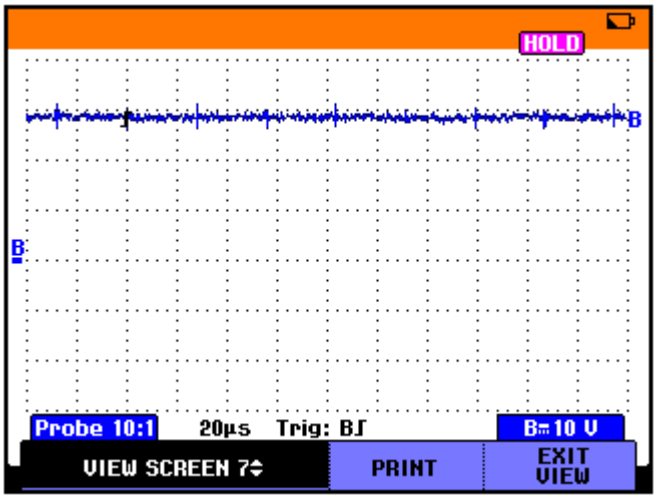

Figure 7.17: Output voltage across Load (Vout=30 V) at R=2Ω
X-axis: 1 div: 20μs, Y-axis: 1 div: 10 V

Chapter 8

Hardware Results of 900 W in Closed Loop Control

8.1 Closed Loop Conrol

All switching converter output voltage is a function of the input voltage, load current and duty cycle. The output voltage should be constant regardless of variation in input voltage, load current and converter circuit parameter values. The load current may vary from no load to full load. In addition, the load may vary from no load to 50% load in step, and vice versa. The converter circuit components will have some tolerance. Despite variation, it is desired that the output voltage be within a certain limit. This is not practical to achieve without negative feedback, and setting the duty cycle to a single value. There are mainly two methods to control the duty cycle to keep the output voltage within the specified limit: voltage mode control and current mode control [20].

When the input voltage is changing, the transient response of voltage mode control is slow, because it has only one feedback loop. It can be seen that input voltage varying only after the variation of output voltage occurs. In fact, the transient response of voltage mode control is slow for any variations of power stage because voltage mode control doesn't have non-lag feedback loop. A feedback loop can be constructed for regulation of the output voltage. The output voltage v(o) is compared to a reference voltage Vref, and it generates an error signal. This error signal is applied to the input of a PI controller and the output of a PI controller is given to the limiter and it regulate the duty cycle [21].

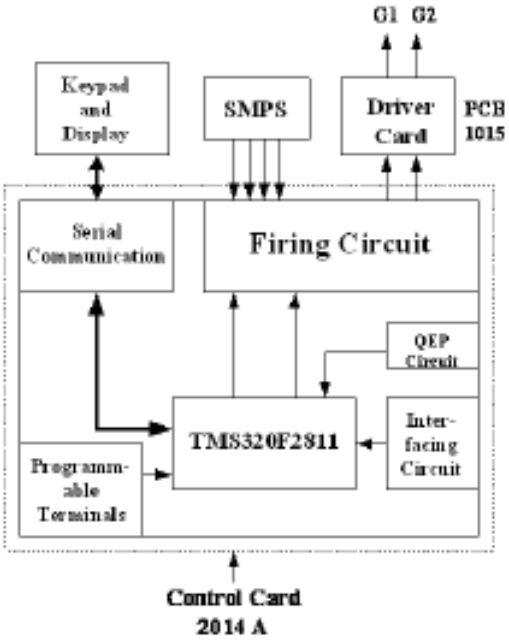

Figure 8.1: Block diagram of close-loop control through DSP

8.1.1 Closed Loop Control Algorithm through DSP TMS320F2811

DSP(Digital signa processor) is the dominating controller for the PWM applications.So the gate pulses is generated through DSP TMS320F2811.The control card houses the TMS320F2811 DSP processor with appropriate interfac- ing circuitry. The current sensor sense the input current, similarly voltage sensor senses the DC link and output voltage and fed to the DSP processor. A SMPS provides the DC supply to the control card and driver IC. The interrupts are also provided for the over current, over voltage and over temperature protection. The DSP system has high speed A/D converter and 16 PWM o/p channels.
The display card is used which is developed on visual basic and it display quan- tities like i/p AC voltage and current, o/p DC voltage and current, PI gain and time constant, frequency setting, reference voltage setting for the o/p voltage regu- lation etc are display and easy to change through software.

8.2 Hardware Results in Closed Loop Conrol

In the Close-Loop Control, if any changes in the input voltage or load variation then the output voltage becomes stable, because this circuit works on constant voltage

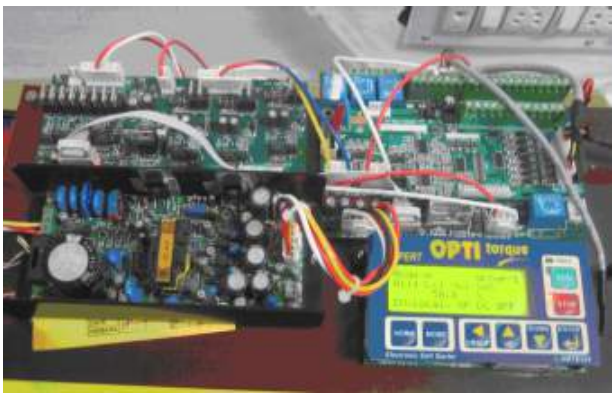

Figure 8.2: Close-loop control setup with control card PCA 2014A

mode. The output voltage is settled according to reference voltage and then error is produced, it is given to the PI controller. According to PI controller's output phase shifted Gate pulses are generated.After that any changes in input voltage or in load then there is no change in output voltage but its phase shifting are changes.

- Input Voltage=415 V(rms)
- Input Current=2.4 A(rms)
- Switching Frequency=18000 Hz
- Diode Bridge Output=582 V(DC)
- Output Voltage=30.15 V
- Output Current=30.6 A
- Load=1Ω

8.3 shows that input current and 8.4 shows that transformer primary current.

8.5 shows that gate pulses of s/w a & d V_{duty} = 0.42, 8.6 shows that Gate pulses of s/w a & c V_{duty} = 0.42 and 8.7 shows that transformer primary voltage and DC output voltage across the load so V_o=30V(DC) settled at V_{ref}=1 & V_{duty} = 0.42

8.8 shows that gate pulses of s/w a & d V_{duty} = 0.34, 8.9 shows that Gate pulses of s/w a & c V_{duty} = 0.34 and 8.10 shows that transformer primary voltage and DC output voltage across the load so V_o=24V(DC) settled at V_{ref}=0.8 & V_{duty} = 0.34 (So

according to reference voltage, output voltage is settled down

8.11 shows that gate pulses of s/w a & d $V_{duty} = 0.22$, 8.12 shows that Gate pulses of s/w a & c $V_{duty} = 0.22$ and 8.13 shows that transformer primary voltage and DC output voltage across the load so V_o=15V(DC) settled at V_{ref}=0.5 & $V_{duty} = 0.22$ (So according to reference voltage, output voltage is settled down and there is a variation in phase shifting).

8.14 shows that gate pulses of s/w a & d $V_{duty} = 0.10$, 8.15 shows that Gate pulses of s/w a & c $V_{duty} = 0.10$ and 8.16 shows that transformer primary voltage and DC output voltage across the load so V_o=9V(DC) settled at V_{ref}=0.3 & $V_{duty} = 0.10$ (So according to reference voltage, output voltage is settled down and there is a variation in phase shifting).

8.17 shows that shows that that the ZVS is achieved at s/w a, so before the gate pulse is given to the switch its drain to source voltage becomes zero and its body diode is conducting. so turn on losses are eliminated and 8.18 shows that shows that that the ZVS is achieved at s/w c, so before the gate pulse is given to the switch its drain to source voltage becomes zero and its body diode is conducting. so turn on losses are eliminated.

8.19 shows that gate pulses of s/w c and Voltage across IGBT c at $V_{ref} = 0.7$ (So at that time energy is not sufficient on primary side so ZVS cannot be achieved) and 8.20 shows that the output voltage only contain ripple at R=1Ω.

So in hardware setup, still feed forward technique cannot be successfully achieved, this part is remaining.

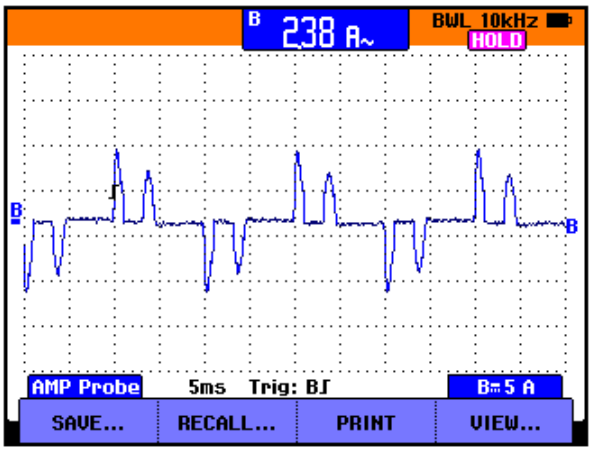

Figure 8.3: Input current Iin=2.38 A(rms)
X-axis: 1 div: 5 ms, Y-axis: 1 div: 5 A

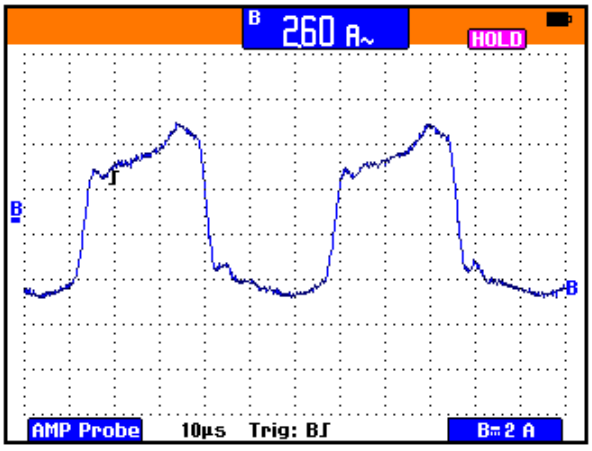

Figure 8.4: Transformer primary current=2.60A(rms)
X-axis: 1 div: 10μs, Y-axis: 1 div: 200 V

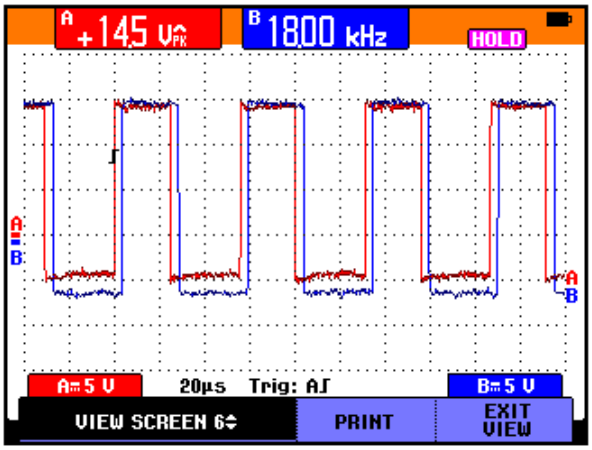

Figure 8.5: Gate pulses of s/w a & d $V_{duty} = 0.42$
Blue Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w d:X-axis:1 div:20μs, Y-axis:1 div:5 V

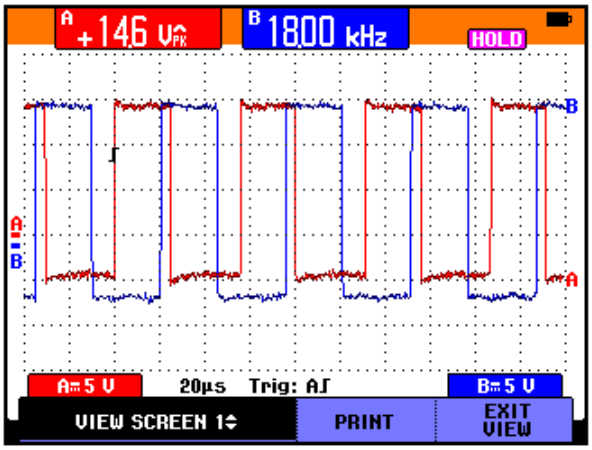

Figure 8.6: Gate pulses of s/w a & c $V_{duty} = 0.42$
Blue Colour:Gate pulses of s/w c:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V

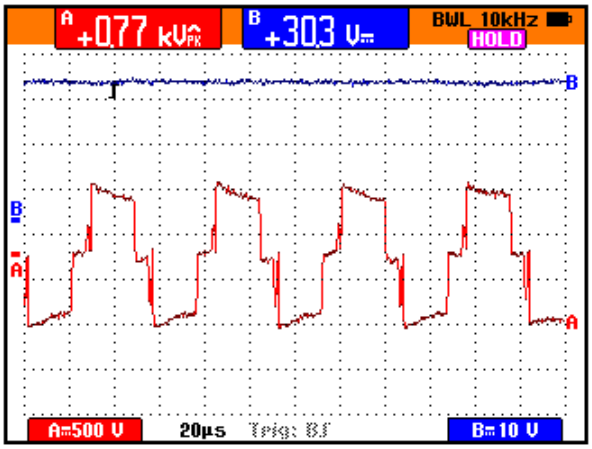

Figure 8.7: V_o=30V(DC) settled at V_{ref}=1 & V_{duty} = 0.42
Blue Colour:O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:10 V
Red Colour:Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:500 V

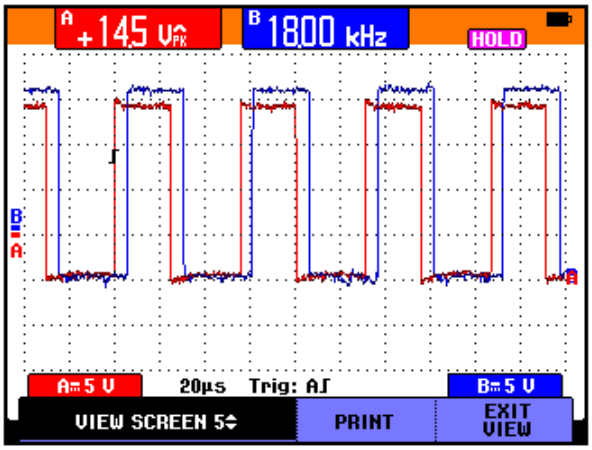

Figure 8.8: Gate pulses of s/w a & d V_{duty} = 0.34
Blue Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w d:X-axis:1 div:20μs, Y-axis:1 div:5 V

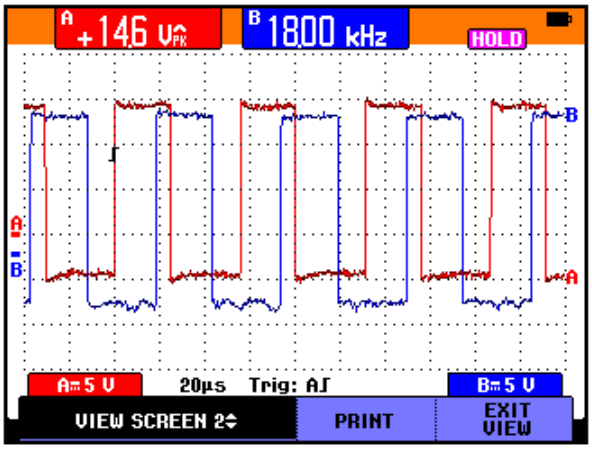

Figure 8.9: Gate pulses of s/w a & c $V_{duty} = 0.34$
Blue Colour:Gate pulses of s/w c:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V

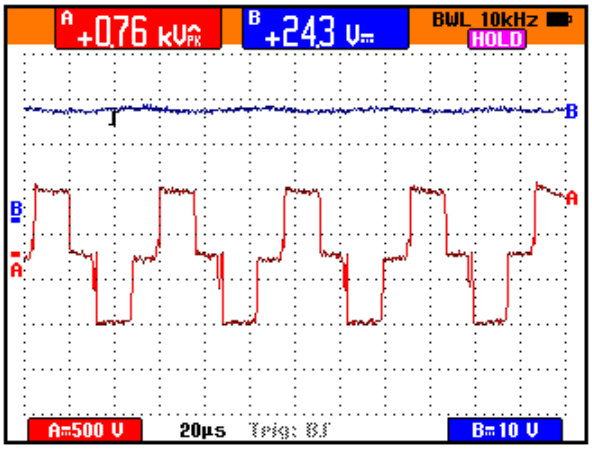

Figure 8.10: V_o=24V(DC) settled at V_{ref}=0.8 & $V_{duty} = 0.34$
Blue Colour:O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:10 V
Red Colour:Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:500 V

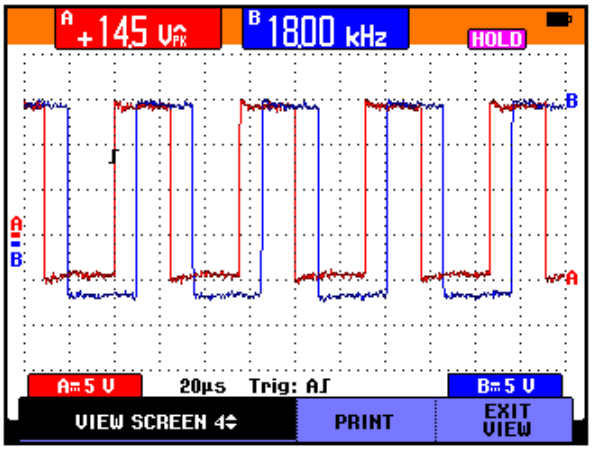

Figure 8.11: Gate pulses of s/w a & d $V_{duty} = 0.22$
Blue Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w d:X-axis:1 div:20μs, Y-axis:1 div:5 V

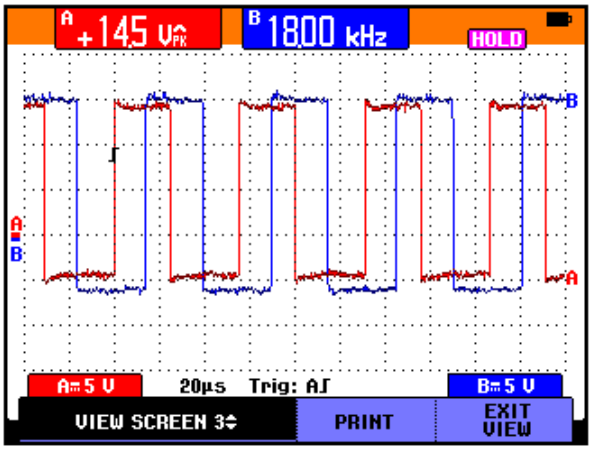

Figure 8.12: Gate pulses of s/w a & c $V_{duty} = 0.22$
Blue Colour:Gate pulses of s/w c:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V

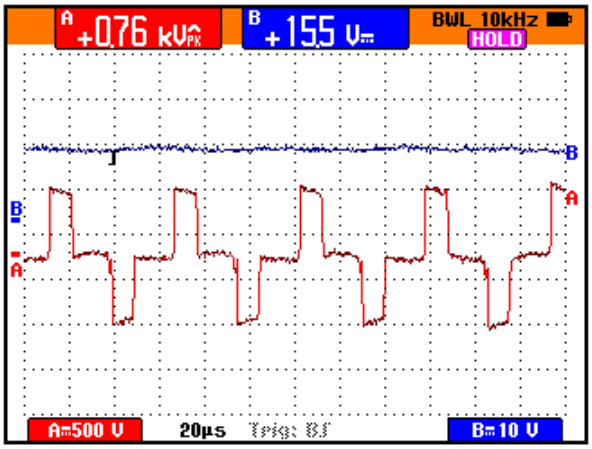

Figure 8.13: V_o=15V(DC) settled at V_{ref}=0.5 & V_{duty} = 0.22
Blue Colour:O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:10 V
Red Colour:Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:500 V

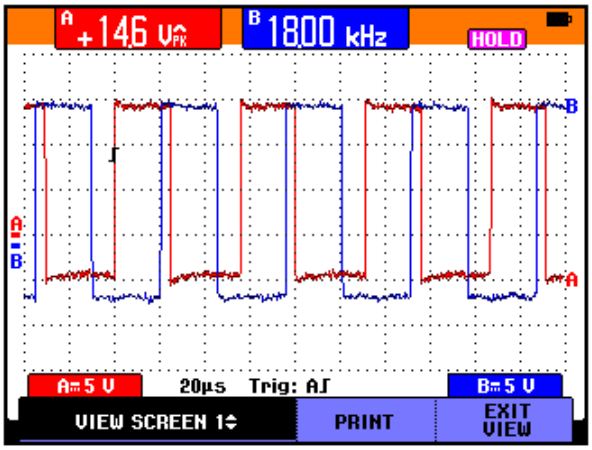

Figure 8.14: Gate pulses of s/w a & d V_{duty} = 0.10
Blue Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w d:X-axis:1 div:20μs, Y-axis:1 div:5 V

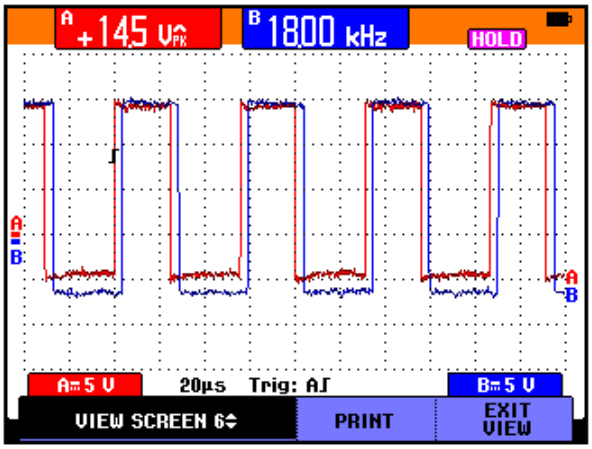

Figure 8.15: Gate pulses of s/w a & c $V_{duty} = 0.10$
Blue Colour:Gate pulses of s/w c:X-axis:1 div:20μs, Y-axis:1 div:5 V
Red Colour:Gate pulses of s/w a:X-axis:1 div:20μs, Y-axis:1 div:5 V

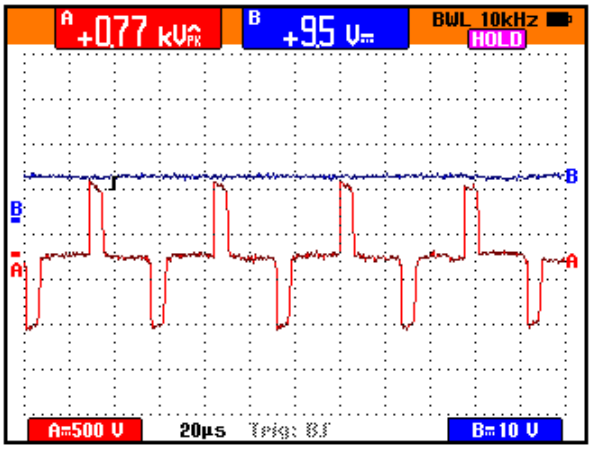

Figure 8.16: V_o=9V(DC) settled at V_{ref}=0.3 & $V_{duty} = 0.10$
Blue Colour:O/P Voltage:X-axis:1 div:20μs, Y-axis:1 div:10 V
Red Colour:Transformer Priamry Voltage:X-axis:1 div:20μs, Y-axis:1 div:500 V

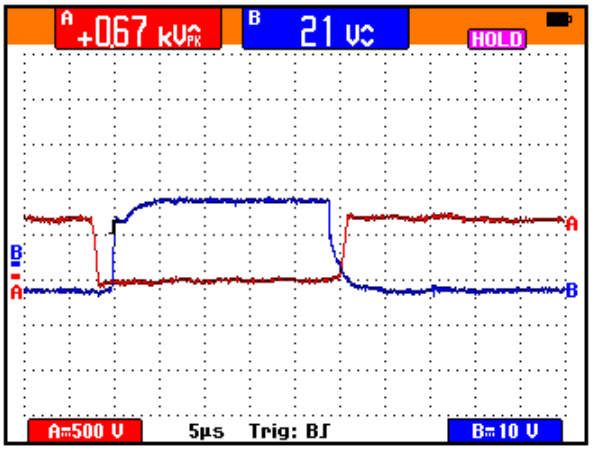

Figure 8.17: Gate pulses of s/w a and Voltage across IGBT a
Blue Colour:Gate pulses of s/w a:X-axis:1 div:5μs, Y-axis:1 div:10 V
Red Colour:Voltage across IGBT a:X-axis:1 div:5μs, Y-axis:1 div:500 V

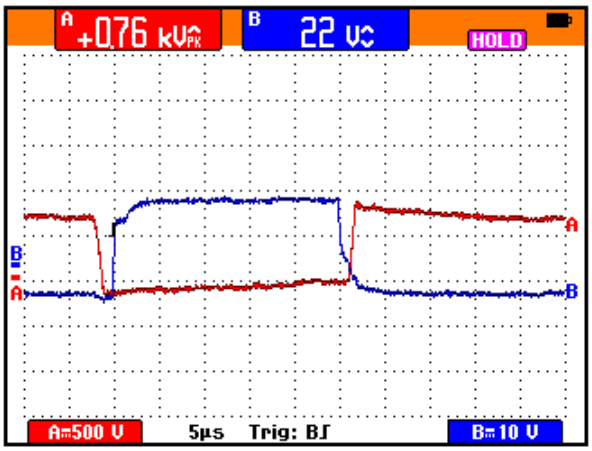

Figure 8.18: Gate pulses of s/w c and Voltage across IGBT c
Blue Colour:Gate pulses of s/w c:X-axis:1 div:5μs, Y-axis:1 div:10 V
Red Colour:Voltage across IGBT c:X-axis:1 div:5μs, Y-axis:1 div:500 V

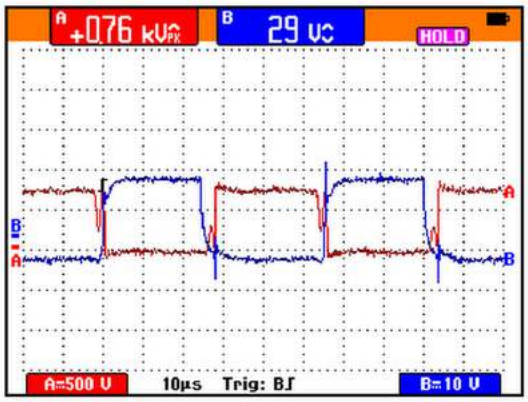

Figure 8.19: Gate pulses of s/w c and Voltage across IGBT c at $V_{ref} = 0.7$
Blue Colour:Gate pulses of s/w c:X-axis:1 div:5μs, Y-axis:1 div:10 V
Red Colour:Voltage across IGBT c:X-axis:1 div:5μs, Y-axis:1 div:500 V

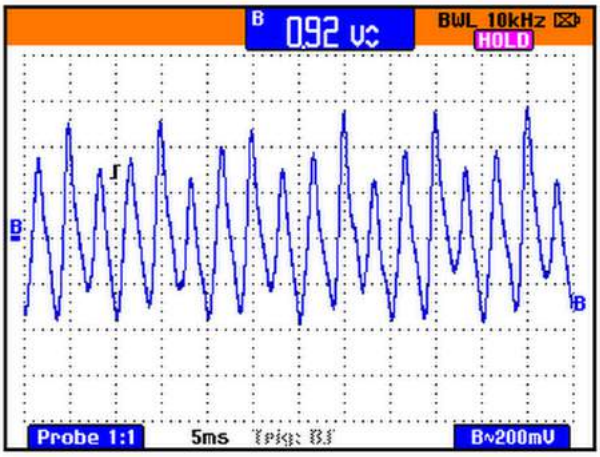

Figure 8.20: Output voltage with ripple
X-axis: 1 scale: 5ms, Y-axis: 1 scale: 200mV

Chapter 9

Hardware Results in Isolated 15 kW Power Supply

9.1 Practical Results

To check out the transformer current and voltage capacity, at the initial stage on secondary side just connected the R load and check out the all results.

- Input Voltage=405 V(rms)
- Input Current=7.3 A(rms)
- Switching Frequency=18000 Hz
- Diode Bridge Output=590 V(DC)
- Transformer Primary Voltage=±590V
- Transformer Secondary and tersary voltage=±45V
- Output Voltage=±90 V
- Load=0.8Ω

9.1 shows that the open loop Block Diagram of 15 kW DC power supply.9.2 shows that the open loop hardware setup of 15 kW DC power supply.

9.3 shows that the input current, 9.4 shows that transformer primary voltage and 9.5 shows that transformer Secondary and tersary voltage.

9.6 show that output Voltage across Load.

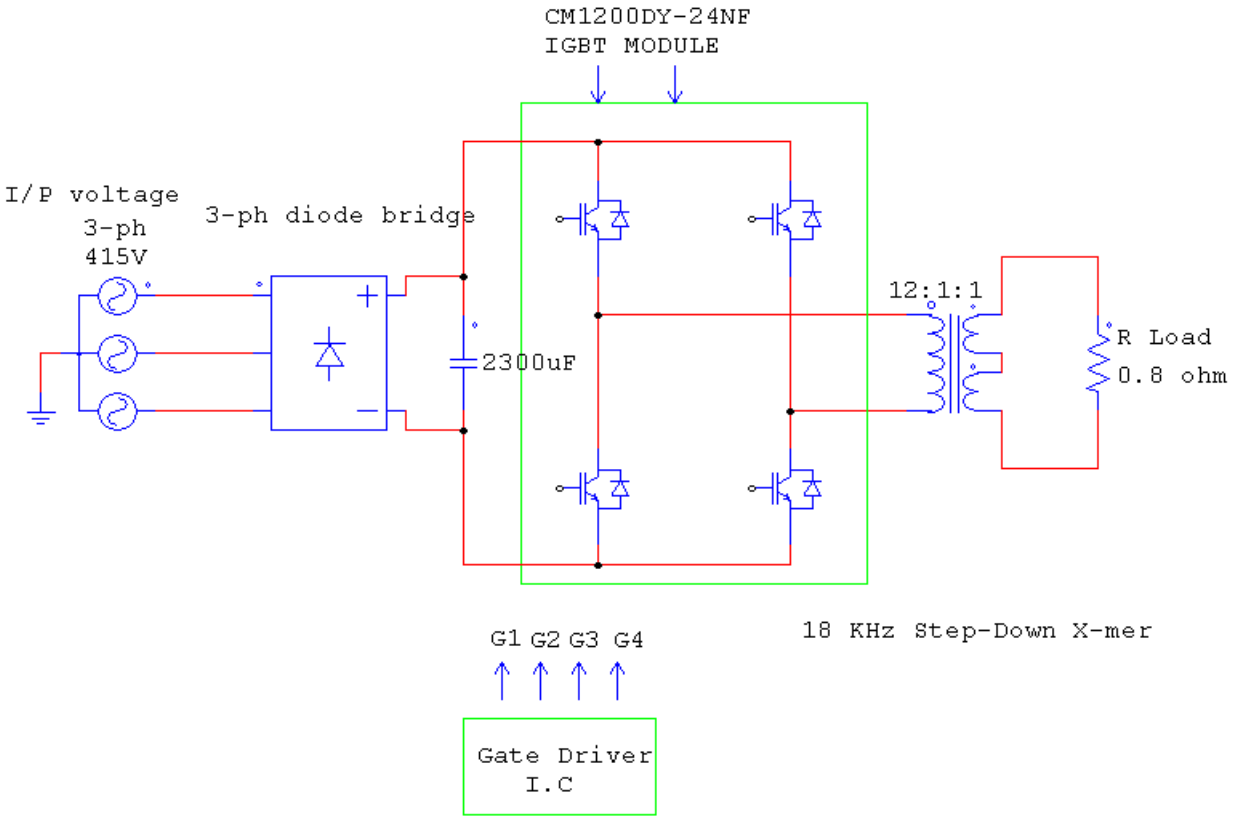

Figure 9.1: Circuit Diagram for Hardware Setup

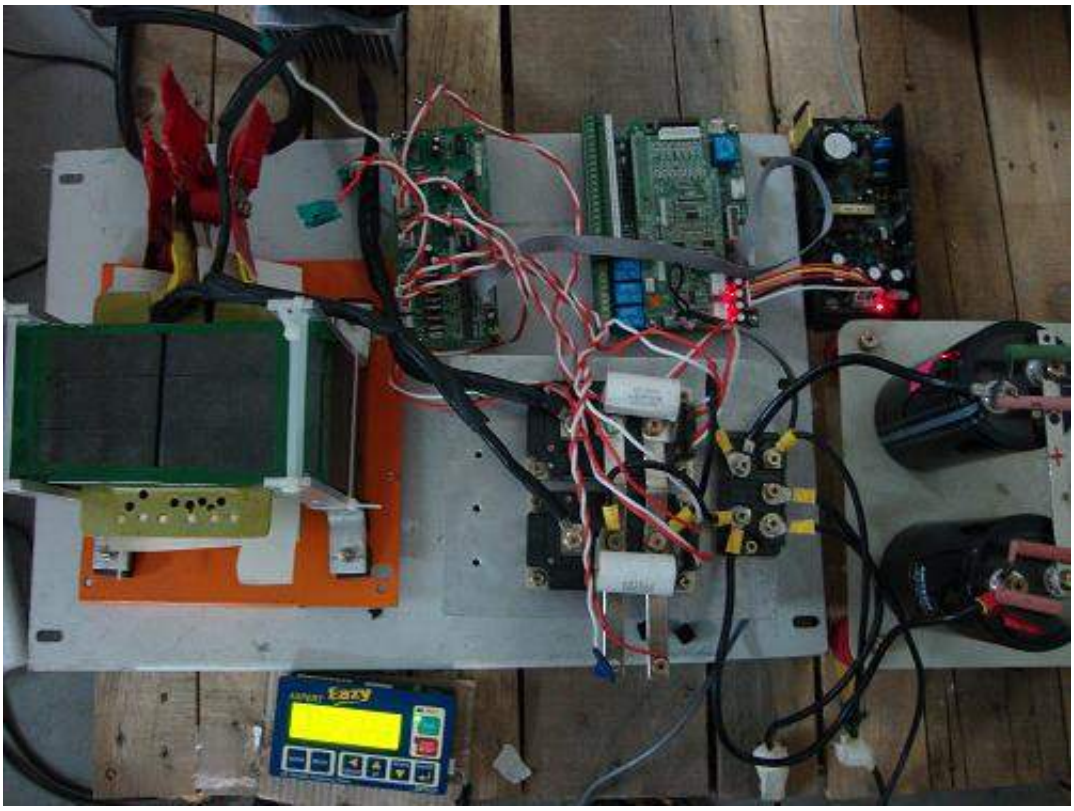

Figure 9.2: Overall view of Hardware setup
X-axis: 1 div: 20 ms, Y-axis: 1 div: 20 A

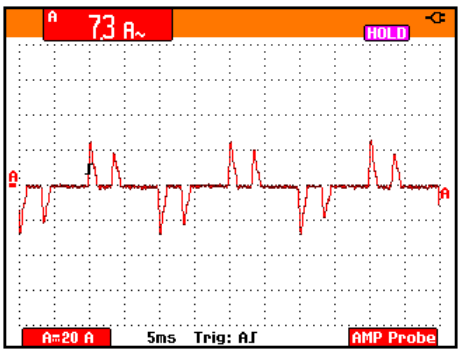

Figure 9.3: Input current
X-axis: 1 div: 10μs, Y-axis: 1 div: 20 A

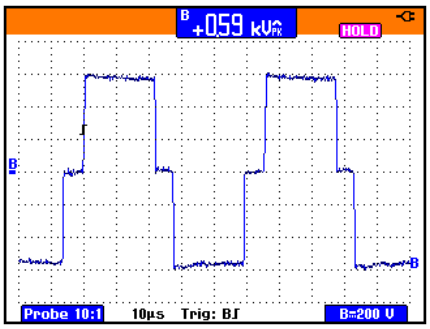

Figure 9.4: Transformer Primary Voltage=±590 V
X-axis: 1 div: 10μs, Y-axis: 1 div: 50 V

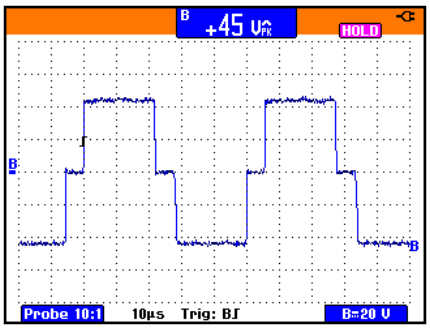

Figure 9.5: Transformer Secondary and tersary voltage=±45 V
X-axis: 1 div: 10μs, Y-axis: 1 div: 20 V

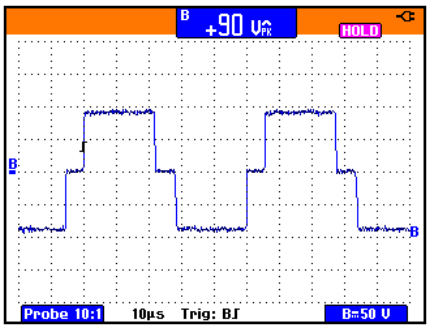

Figure 9.6: Output Voltage across Load=±90V
X-axis: 1 div: 10μs, Y-axis: 1 div: 50 V

Chapter 10

Conclusion and Future Scope

10.1 Conclusion

The 900 W DC power supply is successfully implemented with isolated phase shifted full-bridge DC-DC converter. Hardware results and simulation results are identical. Due to high switching frequency, magnetic components size are decreased. The Isolated 900 W Power Supply with using the Quasi Resonant Converter to eliminate the turn on losses is presented. Design procedure is given and from the Simulation and Hardware results, ZVS (Zero voltage Switching) can be achieved so turn on losses are eliminated. To regulate the DC Output voltage in any variation in load condition and also variation in input voltage, Constant voltage mode(CV) can be achieved through simulation and hardware results.
The Complete Hardware set up with close loop with fixed Switching frequency control through DSP TMS320F2811 was implemented for the 900W converter. The Close loop System is tested with different input voltage, load variation as well as Reference Voltage. The Reference Voltage is very from 0.1 to 1, accordingly output voltage is settled from 3 V to 30 V and also phase shifting is changeover to settle the output voltage.
From the theoretical and practical results, it is proven that in low voltage applications, Synchronous Rectifier conduction losses are less compared to diode bridge.

10.2 Future Work

- To achieve the 40 mV ripple, Feed forward technique can be used.
- Build up the 15 kW power supply and check the output results with simulation results.

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