PROTECTION SYSTEM FOR HIGH POWER INVERTERS

By

Harshil J Shah

12MEEP41

DEPARTMENT OF ELECTRICAL ENGINEERING

INSTITUTE OF TECHNOLOGY

NIRMA UNIVERSITY

AHMEDABAD-382481

May 2014

PROTECTION SYSTEM FOR HIGH POWER INVERTERS

Major Project Report

Submitted in partial fulfillment of the requirements for the degree of

Master of Technology

in

Electrical Engineering

(Power Electronics, Machines and Drives)

By

Harshil J Shah

12MEEP41

DEPARTMENT OF ELECTRICAL ENGINEERING

INSTITUTE OF TECHNOLOGY

NIRMA UNIVERSITY

AHMEDABAD-382481

May 2014

Undertaking for Originality of the Work

I **Harshil J Shah**, Roll No. **12MEEP41**, give undertaking that the Major Project entitled **"Protection System For High Power Inverters"** submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Power Electronics Machines** & **Drives, Electrical Engineering**, under Institute of Technology of Nirma University, Ahmedabad, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

.....

Signature of Student

Date:

Place:

.....

Industry Guide

Mr. D M Choudhary

AGM, R&D Department

Electrotherm (India) Ltd.

Ahmedabad.

.....

Institute Guide

Prof. S N Jani

Department of Electrical Engineering

Institute of Technology

Nirma University

Ahmedabad.

Certificate

This is to certify that **Mr. Harshil J Shah (Roll No: 12MEEP41)** of semester-IV M.Tech Electrical (P.E.M.D) has satisfactorily completed the major project at Electrotherm (India) Ltd., Ahmedabad as mentioned in the following report during the time span of 15^{th} July, 2013 to 2^{nd} May, 2014.

.....

Industry Guide

Mr. D M Choudhary

AGM, R&D Department
Electrotherm (India) Ltd.

Ahmedabad.

.....

Institute Guide

Prof. S N Jani

Department of Electrical Engineering
Institute of Technology

Nirma University
Ahmedabad.

Head of Department

Department of Electrical Engineering
Institute of Technology
Nirma University
Ahmedabad

Director

Institute of Technology
Nirma University
Ahmedabad

Acknowledgement

First of all, I would like to thank ELECTROTHERM (I) Ltd., Ahmedabad, for giving me an opportunity to perform the project under its premises and give me the industrial exposure.

I wish to express my sincere gratitude to Mr. D M Choudhary, AGM, *R&D* department, ELECTROTHERM (I) Ltd., Ahmedabad, for his guidance and support. His technical expertise and vast experience has always helps me to find technical solutions to realistic problems. He always helped me and encouraged me throughout the period we have worked together.

I like to thank my institute guide Mr. Swapnil N Jani (Assistant professor, Nirma University) for providing many insightful comments and constructive suggestion in every reviews of my dissertation.

I am thankful to Dr. P.N.Tekwani (HOD, EE Dept.) for allowing me to do my project work at ELECTROTHERM (I) Ltd., Ahmedabad.

Further I am thankful to all colleagues for their continuous support during my project work.

Special thanks to my parents and my family members for their continuous support and encouragement.

Harshil J Shah
12MEEP41

Abstract

According to the title PROTECTION SYSTEM FOR HIGH POWER INVERTERS, during the whole project work there is a focus on various modified topologies of protection and regulation system of high power inverters in industrial application systems. First of all for that, simulation of high power inverters is necessary with various topologies, some of the modifications will be done and best designing of the circuit will be done so according to the research based results of simulation, the hardware implementation of the high power inverter protection system will be developedThese topic illuminates to develop the protection system for high power inverters using FPGA(field programmable gate array) controller. The current system consist of thyristor for the high power inverters and according to the simulation results hardware implementation is done with FPGA controller board. For the reference values for FPGA code generation, one power circuit can be developed with ZCD circuit and Triggering circuit, according to the result of the power circuit FPGA controller will work in such a way that if any fault occurs in the system then the system will be protected. Parameters like power factor, harmonics, frequency variation, voltage and current ratio is maintained. Here voltage across Thyristor, Output voltage and Current waveforms are being sensed by FPGA Controller and FPGA board can be interface with the hardware and in software of FPGA program can be developed for the feedback of the protection system. FPGA developed system will consider all parameters for the protection purposes of high power inverters. However the system which can be developed in hardware or power circuit can be modify also with other power ratings and according to that FPGA controller will work and the system for the protection of the high power inverters can be easily implemented.

List of Figures

2.1 voltage sourced inverter 6
2.2 current sourced inverter 7
2.3 SPWM control 7
2.4 Elliptical boundary control 7
2.5 SPWM and Elliptical boundary control 8

3.1 Basic running topology 10

4.1 Basic layout of induction furnace showing all its components 12
4.2 Frequency response of the induction circuits 13
4.3 Zero crossing detector output 14
4.4 Capacitive and zero voltage output 14
4.5 Resonant frequency and voltage control monitoring 15

5.1 Equivalent circuit of SCR 17
5.2 Equivalent circuit without Snubber 17
5.3 Voltage across SCR 18
5.4 Current through SCR 18
5.5 Basic Snubber circuit 19
5.6 Voltage across SCR 19
5.7 Current through SCR 20
5.8 Main circuit configuration 21
5.9 Configuration of small scale equipment 21

6.1 Conventional inverter with PI controller 24
6.2 Distorted output by DC offset 25
6.3 Distorted output by non-linear load 25
6.4 Proposed single phase transformer based inverter 27
6.5 PMSM PWM rectifier system 28
6.6 PMSM and boost chopper control system 29

7.1 Basic inverter circuit with modification 31
7.2 Output voltage and R-phase waveforms 32
7.3 Y and B phase waveforms 33

7.4 High power module circuit 33
7.5 Voltage across Thyristors 34
7.6 VC1 waveforms 34
7.7 Mcmurray inverter Bedford circuit 36
7.8 Output voltage waveforms 36
7.9 Single phase Mcmurray inverter circuit 37
7.10 Output voltage waveforms 37
7.11 Three phase thyristor circuit 38
7.12 Output voltage waveforms 39
7.13 Single phase thyristor circuit in PSIM 40
7.14 Output voltage waveforms 41
7.15 Basic Protection Circuit 41
7.16 Protection System For High Power Inverters 42
7.17 Voltage Across Thyristor 43
7.18 Output Voltage Waveform 43
7.19 Current Waveform 44
7.20 Current and Voltage Waveforms 45
7.21 Voltage Across Thyristor, Output Voltage And Current Waveforms . 45

8.1 5547 ADC 48
8.2 DAC 7671 48
8.3 Block diagram of FPGA 49
8.4 Functional block diagram of FPGA 50
8.5 Analog block of FPGA 51
8.6 Device block of FPGA 52
8.7 Loop timer 52
8.8 Saturation block 53
8.9 Help block 53
8.10 Loop timer output block 54

9.1 Block Diagram Of Power Circuit For Protection System 56
9.2 ZCD Circuit 57
9.3 ZCD Circuit 58
9.4 ZCD Circuit Voltage Testing 58
9.5 ZCD Circuit Testing 59
9.6 ZCD Circuit Waveforms [Scale: X-axis: 10ms, Y-axis: 5 V/ div] . . . 59
9.7 MOSFET Driver Circuit 60
9.8 24V Output Circuit 60
9.9 MOSFET Triggering Pulses[Scale:X-axis:10ms,Y-axis:5 V/div] 61
9.10 MOSFET Triggering Pulses[Scale:X-axis:10ms,Y-axis:5 V/div] 61
9.11 Protection System Testing 62
9.12 Protection System Testing Circuit 62
9.13 Voltage Variation Testing 63

9.14 Setup in Openloop 63
9.15 Output Voltage Waveforms Of Thyristor[Scale:X-axis:10ms,Y-axis:5 V/div] 63
9.16 Output Voltage Waveforms Of Thyristor[Scale:X-axis:10ms,Y-axis:5 V/div] 64
9.17 Output Voltage Waveforms Of Thyristor[Scale:X-axis:10ms,Y-axis:5 V/div] 64
9.18 FPGA Controller Paper view 65
9.19 SPARTAN-3E Starter Kit FPGA 66
9.20 Schematic Of PWM Components 67
9.21 Digital Clock Manager 67
9.22 Schematic of High Frequency Counter based PWM Generator 68
9.23 Schematic of Counter based PWM Generator 69
9.24 For Duty Cycle Of 25 Percentage 69
9.25 For Duty Cycle Of 75 Percentage 69
9.26 Design Flow Of FPGA Controller 70
9.27 Compared waveforms[Scale:X-axis:10ms,Y-axis:5 V/div] 71
9.28 ZCD And FPGA Interfacing Waveforms[Scale:X-axis:10ms,Y-axis:5 V/div] 71
9.29 Voltage Across Thyristor Waveform for Detection[Scale:X-axis:10ms,Y-axis:5 V/div] 72
9.30 Zero Voltage At The Output Side[Scale:X-axis:10ms,Y-axis:5 V/div] . 72
9.31 Voltage Waveform With Reduced Amplitude 73

List of Tables

Nomenclature

V_s ..... Supply Voltage

I_s ..... Supply Current

n ..... turns ratio of Autotransformer

L_{s1}, L_{s2} ..... Ac Line Reactance

V_x ..... Secondary side voltage of Active IPT

V_m ..... Primary side voltage of Active IPT

I_x ..... Injected current into auxilliary winding of Active IPT

N_x ..... No. of turns of auxilliary winding of Active IPT

N_m ..... No. of turns of Primary winding of Active IPT

V_d ..... Load Voltage

I_d ..... Load Current

I_{d1} ..... Output Current from Rectifier-1

I_{d2} ..... Output Current from Rectifier-2

V_{d1} ..... Output Voltage from Rectifier-1

V_{d2} ..... Output Voltage from Rectifier-2

c ..... Filter Capacitor

R ..... Load Resistance

Contents

Undertaking iii

Certificate iii

Acknowledgement v

Abstract vi

List of Figures vii

List of Tables x

Nomenclature xi

Contents xii

1 OVERVIEW 1
- 1.1 Introduction . . . 1
- 1.2 Basic overview . . . 2
- 1.3 Basic methodology . . . 3
- 1.4 Problem identification . . . 3
- 1.5 Scope of work . . . 4
- 1.6 Expected outcome . . . 4

2 BASIC INVERTERS 5
- 2.1 Single phase inverters . . . 5
- 2.2 Voltage source inverters . . . 5
- 2.3 Current source inverters . . . 6

3 RUNNING SCHEMES 9
- 3.1 Overview . . . 9

4 HIGH POWER INVERTERS 11
- 4.1 Basic methods . . . 11

5 BASIC PROTECTION SYSTEMS 16
5.1 OVERVIEW WITH SNUBBERS 16
5.2 Simulation results 20
5.3 With GTO 20

6 VOLTAGE MONITORING AND DIGITAL CONTROL 23
6.1 Digital control 23
6.2 Proposed topology 26
6.3 Basic overview 27

7 Simulation analysis and results 30
7.1 PSIM Simulation Circuits 30
7.2 Further Overview 38

8 HARDWARE appraoch and FPGA Controller 47
8.1 Basic overview 47
8.2 FPGA Controller 47
8.3 FPGA working 49

9 Hardware tests and result analysis 55
9.1 Hardware Analysis 55
9.2 FPGA Based Results 66

10 FUTURE WORK AND CONCLUSION 74
10.1 Conclusion 74
10.2 Future Work 74

References 75

Chapter 1

OVERVIEW

1.1 Introduction

Power electronics is the application of solid-state electronics for the control and conversion of electric power. It also refers to a subject of research in electronic and electrical engineering which deals with design, control, computation and integration of nonlinear, time varying energy processing electronic systems with fast dynamics.

Applications of power electronics range in size from a switched mode power supply in an AC adapter, battery chargers, fluorescent lamp ballasts, through variable frequency drives and DC motor drives used to operate pumps, fans, and manufacturing machinery, up to gigawatt-scale high voltage direct current power transmission systems used to interconnect electrical grids. Power electronic systems are found in virtually every electronic device.

DC to AC converters produce an AC output waveform from a DC source. Applications include adjustable speed drives (ASD), uninterruptable power supplies (UPS), active filters, Flexible AC transmission systems (FACTS), voltage compensators, and photovoltaic generators. Topologies for these converters can be separated into two distinct categories: voltage source inverters and current source inverters. Voltage source inverters (VSIs) are named so because the independently controlled output is

a voltage waveform. Similarly, current source inverters (CSIs) are distinct in that the controlled AC output is a current waveform.

Being static power converters, the DC to AC power conversion is the result of power switching devices, which are commonly fully controllable semiconductor power switches. The output waveforms are therefore made up of discrete values, producing fast transitions rather than smooth ones. The ability to produce near sinusoidal waveforms around the fundamental frequency is dictated by the modulation technique controlling when, and for how long, the power valves are on and off. Common modulation techniques include the carrier-based technique, or pulse width modulation, space-vector technique, and the selective-harmonic technique. So by seeing all these specifications protection system is required for the high power inverters at any cost and at any conditions so that our system is safe and it works according to expected values.

Basically in this topic Protection system for high power inverters all the necessary data and reference materials should be considered. In this topic first of all designing and implementation of the high power inverter circuit is to be made so that we get the basic idea about the high power module devices. For particular topology of this topic we should test the basic medium voltage and high voltage power module then and then only we come to know about the modified high power module.

1.2 Basic overview

In high power circuit we can use many components with suitable to each values and other parameters and also for the precision of the output we can change the particular circuit weather it is semiconductor devices or the other element of power electronics. So basically by doing modifications many times we will come to know about the particular topology and so that we can implement hardware skills also by understanding the basic fundamentals.

1.3 Basic methodology

As we are doing our major project in ELECTROTHERM, they suggested us to do our topic for the protection system for the high power inverters. In industry basically currently running schemes are good but further implement and future scope also should be considered so all the minor fault and then designing of the high power module should be implemented. During our training period we have understood all the working principle and all the skims that are currently running in the industry so for better output better modification should be implemented so in this topic we are working on designing for high power module circuits right now and also with the help of simulation result we can understand the basic outcome for the particular topology. After designing the particular topology we have to obtain design simulation results and also by observing all the faults and all the parameters we will make close loop control system with the help of the microcontroller so for that we will develop some logic for the input systems in MATLAB and PSIM also so that exactly circuit of the close loop system for high power inverter will be implemented and then the controller circuit with protection system of this high power inverter will be implemented and then hardware system of this power module will be implemented.

1.4 Problem identification

The main problem in high power module is that currently the schemes which is in the implement is good but for further analysis in detail and to minimise the losses in high power module one proper topology with protection system should be necessary so fault like common mode voltage, harmonics, reactance, impedance and reactive power are there and for high power module all the minor faults are considered so that the designing of the circuit should be properly implemented because right now the basic schemes which is running does not satisfy all the minor fault so some losses and other fault are considered in high power so that all expected outcome is depend on

the microcontroller logic data and according to that the protection system for high power inverters.

1.5 Scope of work

Basically the scope of this topic is to develop a protection system for the high power module so that all the losses and fault occurs while running basic circuit for the high power induction furnace will be minimised and protection system with snubber circuit will be implemented and then hardware circuit for the basic model will be implemented for the high power induction furnaces. The main aim of this topic is to run a device with high power without any fault and any disturbances so by doing proper designing and hardware implement it will minimise this all disturbances.

1.6 Expected outcome

The main outcome of this topology will be the particular topology with protection system. So this whole protection system with different methods will be implemented for the high power module and also with using microcontroller this particular system will be implemented for the high power induction melting furnace.

Chapter 2

BASIC INVERTERS

2.1 Single phase inverters

Basically for understanding of any inverter topology first of all the fundamentals and the parameters of the inverters should be considered, so that single phase and then three phase topology of the inverters should be focused. In that voltage source inverters and current source inverters with full bridge and half bridge circuits should be understood. Weather Inverter system is with high power or lower but proper semiconductor devices with particular frequency and other parameters should be implemented. In practical ways with the use of the MATLAB and PSIM, we can analyse the simulation results of the topology so that for the high power inverters it is easy to understand and many parameters like power factor, frequency, voltage and current waveforms, FFT analysis, transiet conditions, common mode voltage elimination are available for the designing of the high power inverters systems.

2.2 Voltage source inverters

The geometric approach to switching power converter control design has generated much interest a method for dc-dc converters, Hysteresis, sliding mode, current mode and similar control techniques have geometric interpretations and are based on the

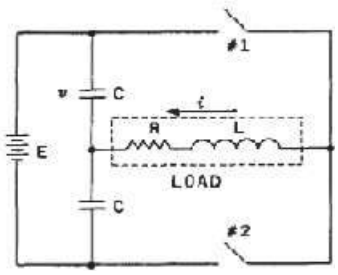

Figure 2.1: voltage sourced inverter

generalised notion of a switching boundary. Some three-phase inverter control schemes rely heavily on geometric concepts in a transformed space.Control of single-phase inverters has traditionally been implemented using pulse width modulation (PWM) with sinusoidally varying duty cycle , or hysteresis control with sinusoidally varying reference waveform . The approach presented here can be considered a generalisation of dc-dc geometric methods which are based on the more general theory of variable structure control. It will be shown that with state feedback alone it is possible to obtain the desired oscillatory output without having to introduce a reference time function.

2.3 Current source inverters

Basically, in this circuits of voltage and current sourced inverters, from waveforms we can analyse the starting and initial conditions of the inverter output. Here also we can observe the peak value and total voltage and time output systems with each fundamental cycles the output is obtained according to the firing angle given to the thyristors.

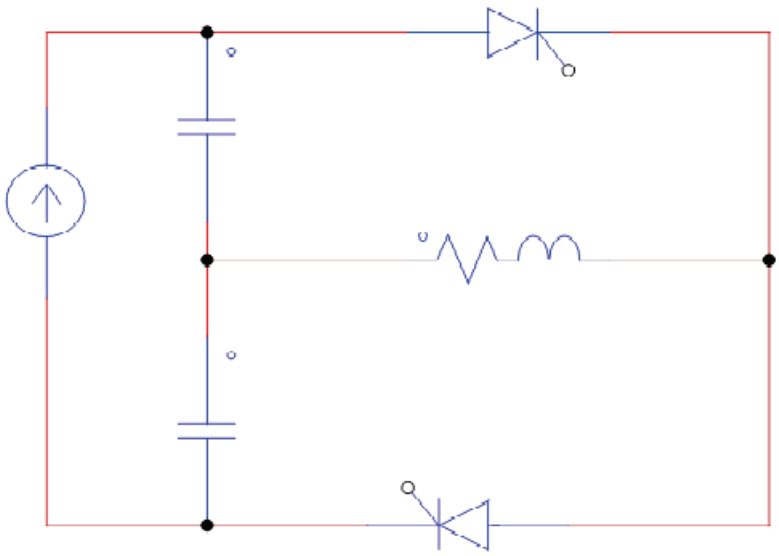

Figure 2.2: current sourced inverter

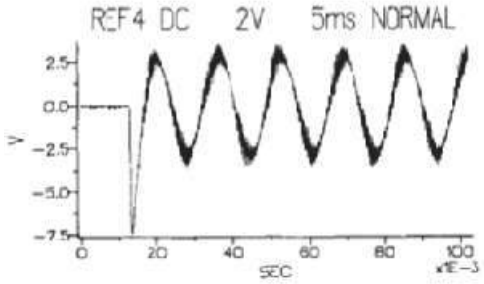

Figure 2.3: SPWM control

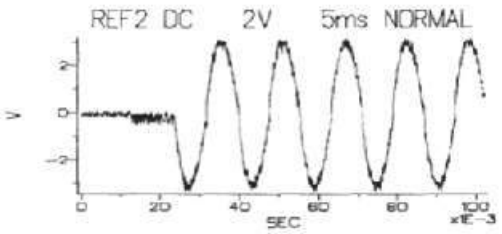

Figure 2.4: Elliptical boundary control

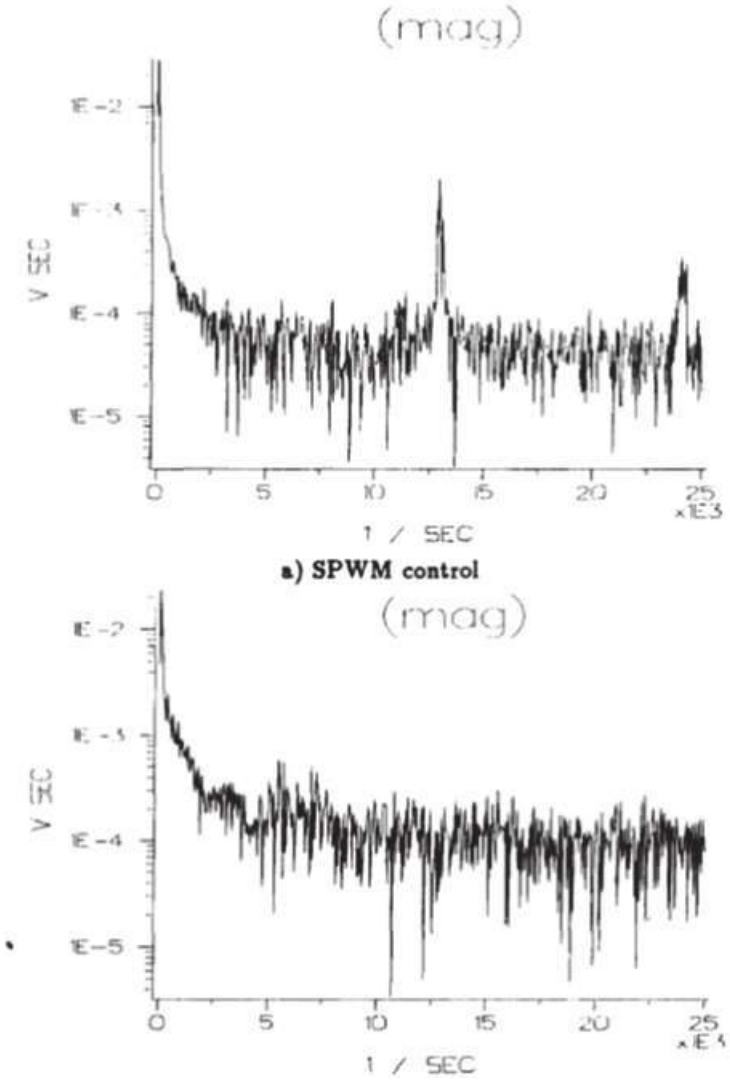

Figure 2.5: SPWM and Elliptical boundary control

Chapter 3

RUNNING SCHEMES

3.1 Overview

Basically in ELECTROTHERM currently schemes working based on the 850*4*1.35. So in that during receiving side 4 converters are connected in series and 850V are divided into 4 converters and according to that it gives supply to the inverters. So in this topic modification in this all topology are required. In this basic topology basically three phase supply is given to the converter and all three converters are series connected so that 850*4 supply is given to the input side. According to the present topology this output supply is given to the inverter topology and so that this inverter protection and control schemes for high power is needed basically therefore this topic is based on the protection system for high power inverters.

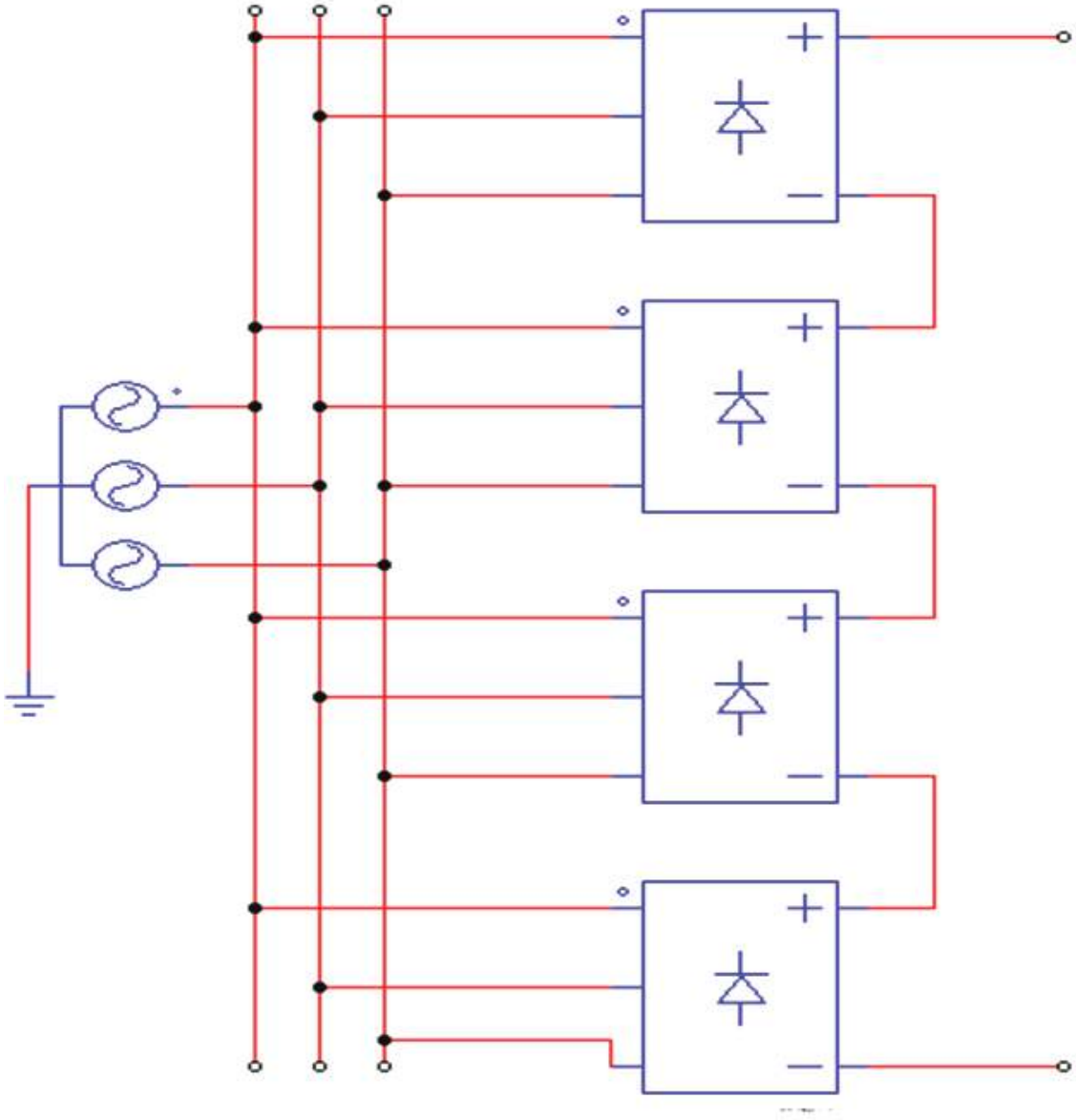

Figure 3.1: Basic running topology

Chapter 4

HIGH POWER INVERTERS

4.1 Basic methods

The inductive nature of induction - heating loads have facilitated the use resonant capacitors to compensate for their reactive power demands. Operation at resonance also has the advantage of ensuring reduced switching losses in the power source, thereby allowing high conversion efficiencies. The work-piece geometry, conductivity and permeability of different metals tend to change the inductance of the heating coil when inserted into it. Considering the fact that the resonant capacitance is FED, the tank circuit is driven to its new resonant frequency by changing the switching frequency of the power source. The automatic frequency control system (AFC) implemented has an operating range of 135kHz (85kHz - 220kHz).

1 A 2kW continuous-mode front-end power factor pre regulator derived from a non isolated boost converter stage.

2 2- A 2kW switch-mode DC current-source derived from a buck converter.

3 A full-bridge current-fed inverter employing power MOSFETs as the switching elements

4 A parallel resonant induction-heating load comprising a resonant capacitor bank

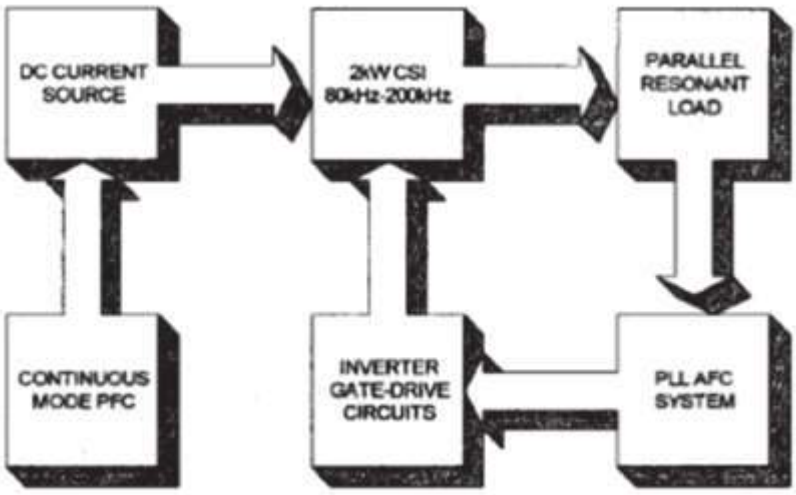

Figure 4.1: Basic layout of induction furnace showing all its components

and a water-cooled induction heating coil. An alumina-fused silica crucible is placed inside the heating coil, which holds the metal to be heated.

5 The automatic frequency control system, which monitors the load resonant frequency and provides the clocking signal to the gate drive circuitry.

6 The level-shifted gate drive circuitry used to drive the power MOSFETs in the H-Bridge configuration.

The unloaded coil has a relatively high Q (approximately 18). When the coil is loaded the Q tends to decrease (8.25 for copper and 2.56 for steel). The resonance locked loop tracks the operating pointsf0,fi and h for different load conditions and therefore maintains maximum real power transfer to the load throughout the heating cycle.

An automatic frequency control system for a miniature high frequency induction furnace has been developed. The system was proven to have a number of advantages as mentioned earlier. The implementation of the actual circuit utilizes a minimum number of components and therefore provides a relatively cost effective approach

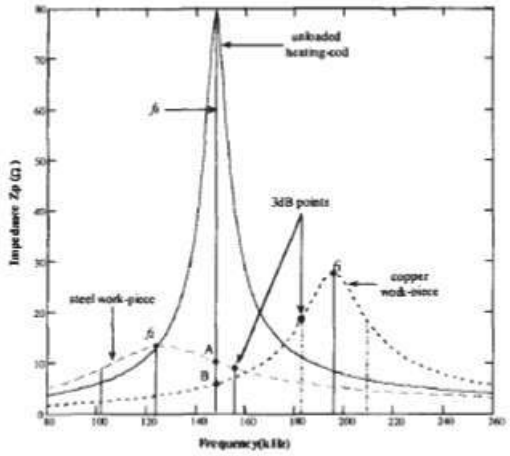

Figure 4.2: Frequency response of the induction circuits

for frequency control. The implementation of AFC eliminates the need for manual open loop frequency control and has optimized the inverter performance. The ZVS achieved has eliminated the need for snubber circuitry and also allows the MOSFET switches to be driven closer to their maximum voltage ratings.

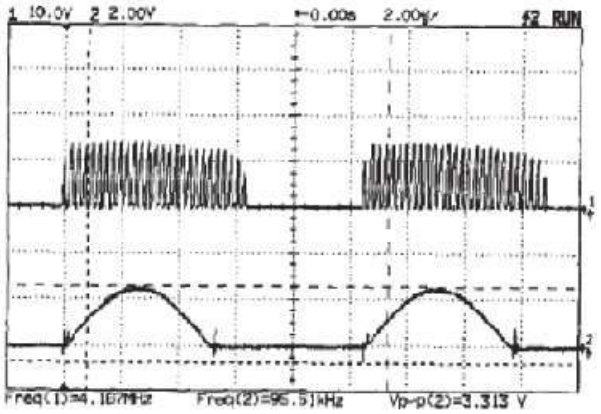

Figure 4.3: Zero crossing detector output

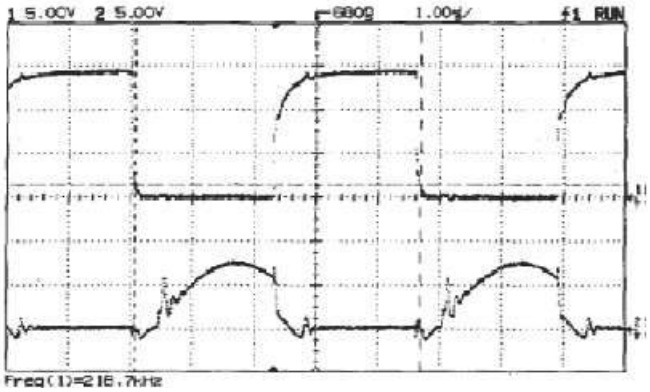

Figure 4.4: Capacitive and zero voltage output

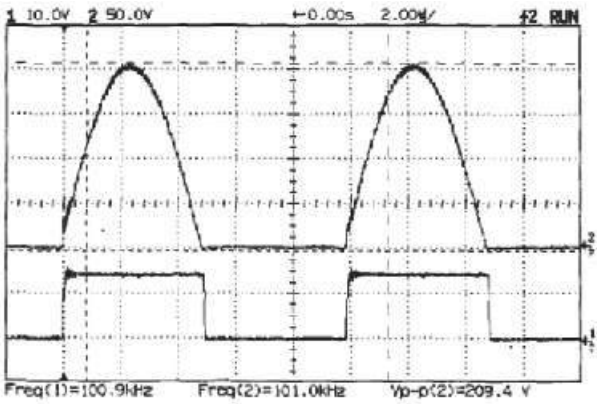

Figure 4.5: Resonant frequency and voltage control monitoring

Chapter 5

BASIC PROTECTION SYSTEMS

5.1 OVERVIEW WITH SNUBBERS

Snubbers are indispensible in power electronics. Snubbers are small networks of parts in the power switching circuits whose function is to control the effects of circuit reactance. Snubbers are an essential part of power electronics. Snubbers are any of several simple energy absorbing circuits used to eliminate voltage spikes caused by circuit inductance when a switch is either mechanical or semi-conductor opens.

Snubber circuits enhance the performance of the switching circuits and result in higher reliability, higher efficiency, higher switching frequency, smaller size, lower weight, and lower EMI. The basic intent of a snubber is to absorb energy from the reactive elements in the circuit. The benefits of this may include circuit damping, controlling the rate of change of voltage or current or clamping voltage overshoot. In performing these functions, a snubber limits the amount of stress which the switch must endure and this increases the reliability of the switch.

The objective of the snubber is to eliminate the voltage transient and ringing that occurs when the switch opens by providing an alternate path for the current flowing through the circuits intrinsic leakage inductance. Snubbers in switch mode power supplies provide valuable functions:

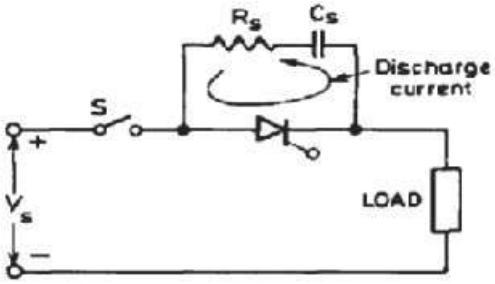

Figure 5.1: Equivalent circuit of SCR

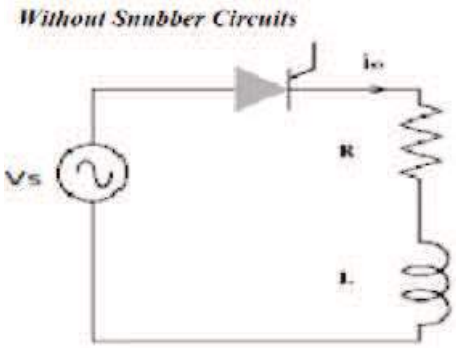

Figure 5.2: Equivalent circuit without Snubber

1 Reduces or eliminates voltage or current spikes.

2 Limit di/dt or dv/dt.

3 Shape the load line to keep it within the safe operating area.

4 Transfer power dissipation from the switch to a resistor or a useful load.

5 Reduce total losses due to switching the devices.

6 Reduce EMI by damping voltage and current ringing.

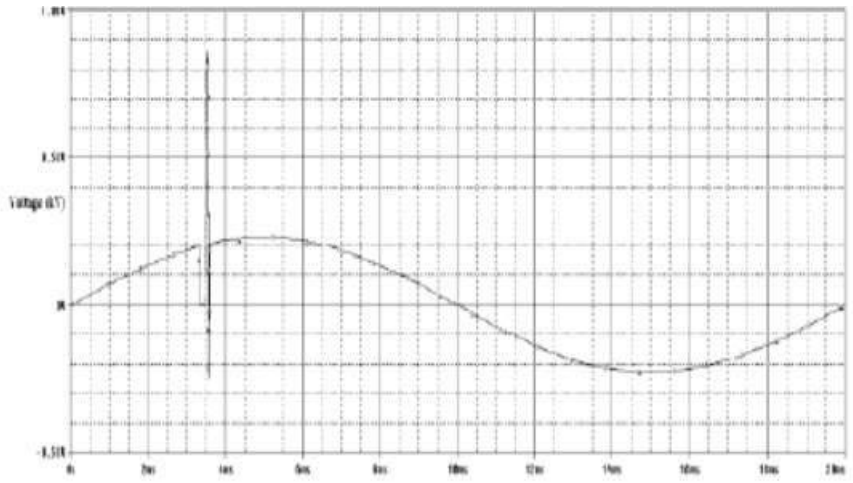

Figure 5.3: Voltage across SCR

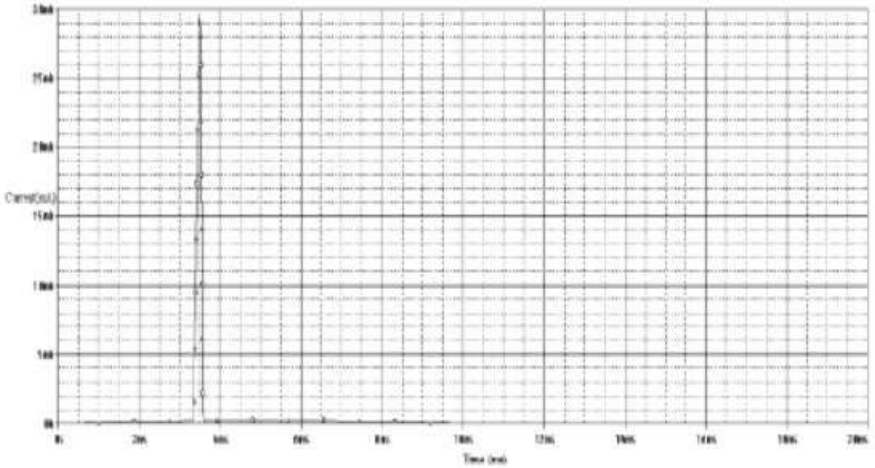

Figure 5.4: Current through SCR

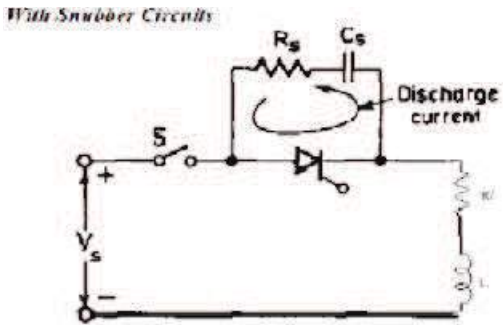

Figure 5.5: Basic Snubber circuit

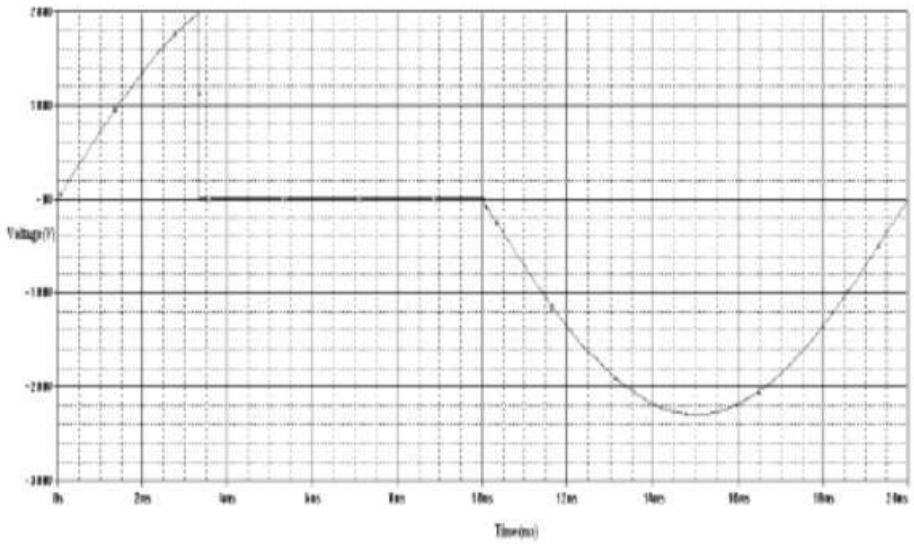

Figure 5.6: Voltage across SCR

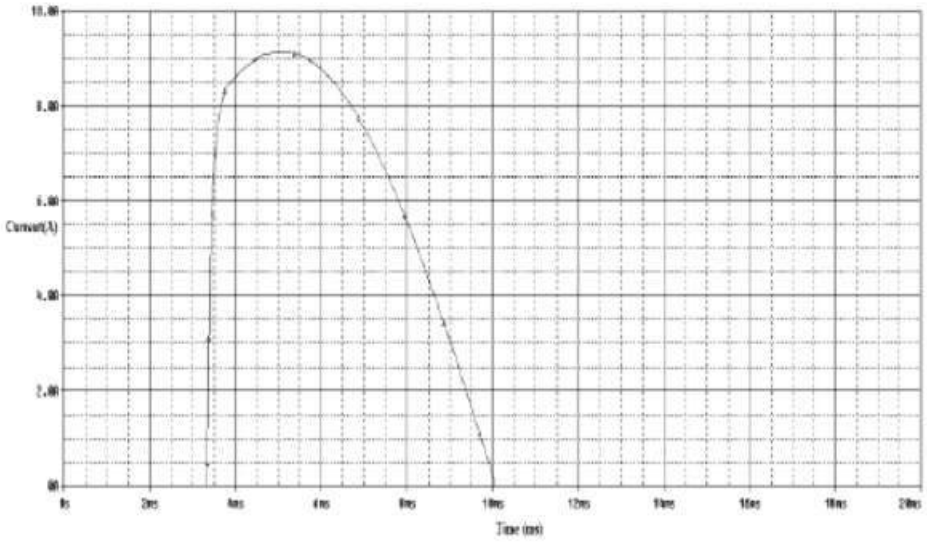

Figure 5.7: Current through SCR

5.2 Simulation results

5.3 With GTO

A large-capacity inverter using high-power gate turn-off (GTO) thyristors that can he used instead of a cyclo converter in ac drives is presented. With the techniques of multiple configuration and GTO series connection, the inverter capacity is increased effectively. High conversion efficiency is obtained by using low-loss snubber circuits for GTOs. It is confirmed that the low-loss snubber circuits using energy recovery uNts (ERUs) have good performance in PWM operation. High-energy recovery efficiency is obtained, especially in leading operation (turn-on operation when freewheeling diodes conduct). These snubber have the superior ability for clamping overvoltage at GTO turn-off. The 2750-kVA inverter with low-loss snubber circuits using high-power GTOs is fabricated and evaluated. The main snubber capacitor CS2 is charged and discharged alternatively. When the GTOs in the negative arm are turned off, CS2 is charged. And when the GTOs in the positive arm are turned off, CS2 is discharged.

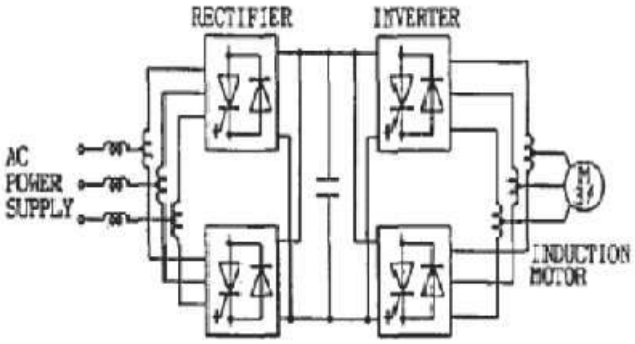

Figure 5.8: Main circuit configuration

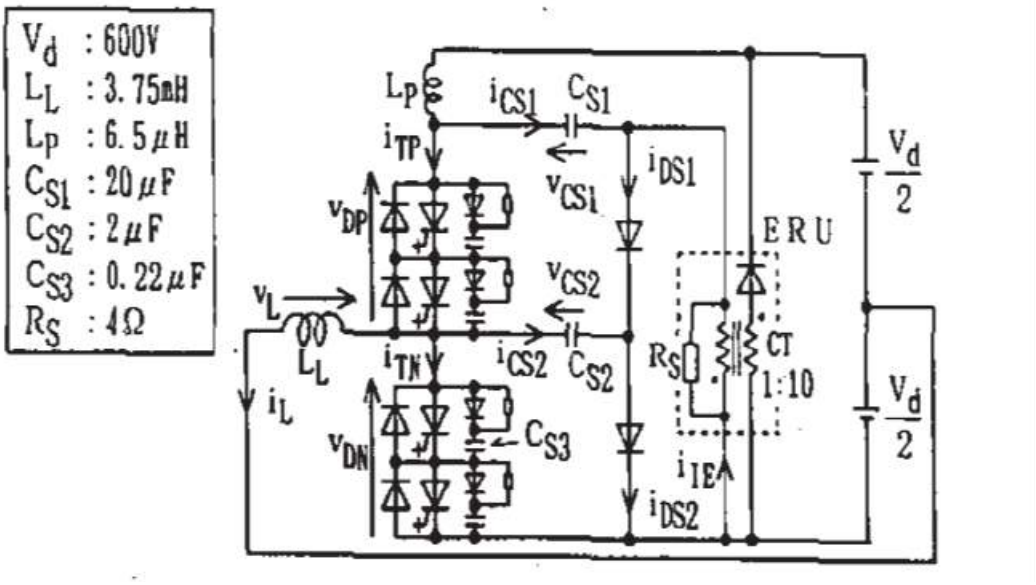

Figure 5.9: Configuration of small scale equipment

On the other hand, the capacitor CS1 is used in a charged state up to dc link voltage. As the capacity of capacitor CS1 is selected as ten or more times that of CS2, the capacitor CSl has the effect of clamping overvoltage at GTO tum-off.

Chapter 6

VOLTAGE MONITORING AND DIGITAL CONTROL

6.1 Digital control

A new digital-controlled single-phase transformer-based inverter for non-linear load applications is also required. A capacitive full-bridge circuit is added to provide instant current under non-linear load condition and thereby reducing the harmonics significantly to meet the required harmonic standard, IEEE 519-1992, even under non-linear load condition. The redundant capacity, cost, size and weight of line frequency transformer can therefore be dramatically reduced. Moreover, a new integrated controller for inverter control is proposed to eliminate both DC current component and steady state error even under heavy load condition.

The proposed integrated controller consists of a Proportional (P) controller acts as voltage controller, DC offset canceller, an RMS compensator and non-linear load compensator. Experimental results derived fromaDSP-based inverter system will be presented. The inverter rating is 1.5 kVA. It will be shown that both redundant capacity of line frequency transformer and voltage harmonics are significantly reduced even with non-linear load. It will also be demonstrated that the DC current compo-

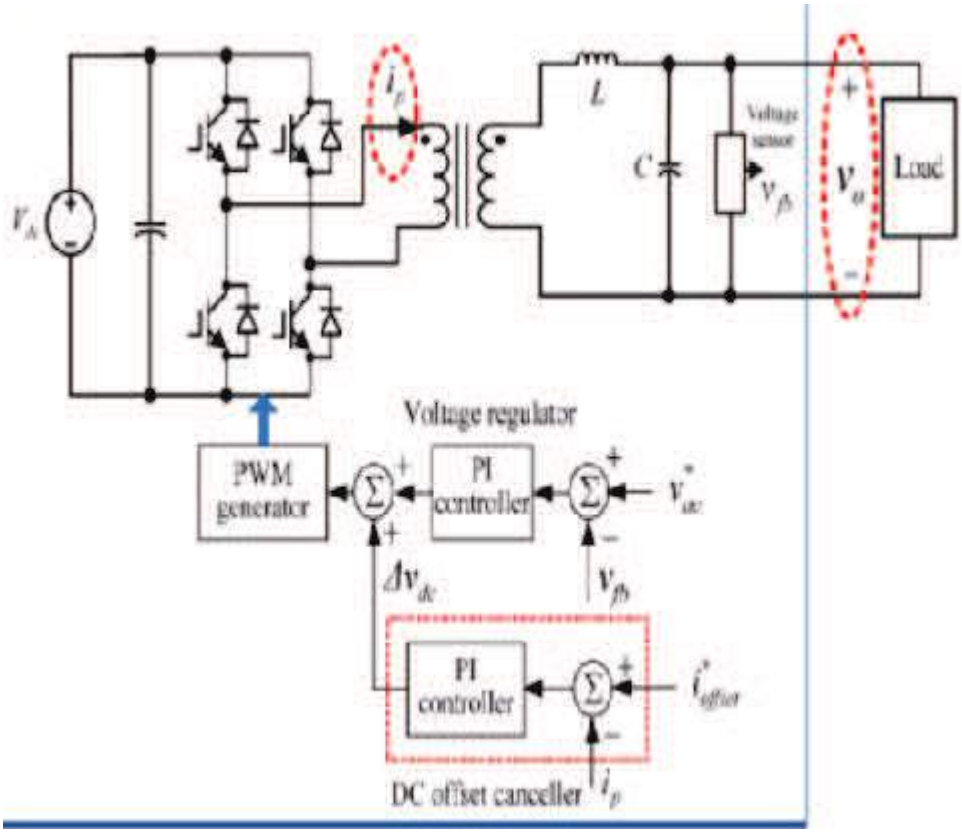

Figure 6.1: Conventional inverter with PI controller

nent and steady state error are eliminated even under heavy load condition. These experimental results therefore confirm the superb performance of the proposed inverter and control techniques. For a single-phase transformer-based inverter, theDC voltage is difficultly suppressed to zero at output. The resources of DC component may be yielded from the following mechanisms.

1 DC offset in PWM circuit or finite data length effect for counter-based PWM circuit.

2 DC offset voltage in feedback voltage signal.

3 Dead-time effect.

4 Unmatched characteristics of power switches and its driving circuits.

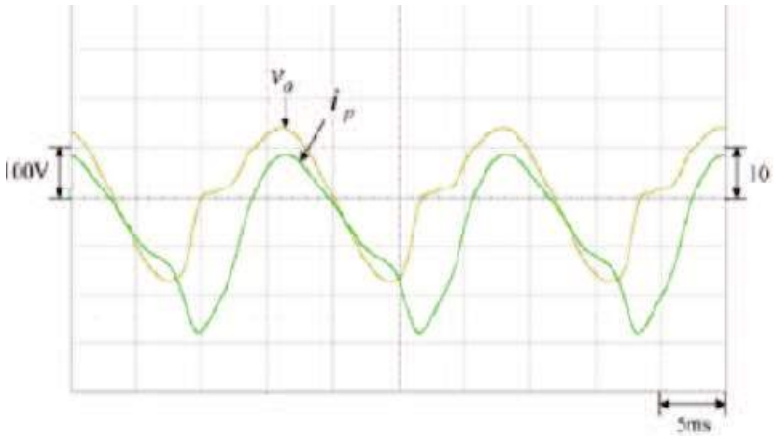

Figure 6.2: Distorted output by DC offset

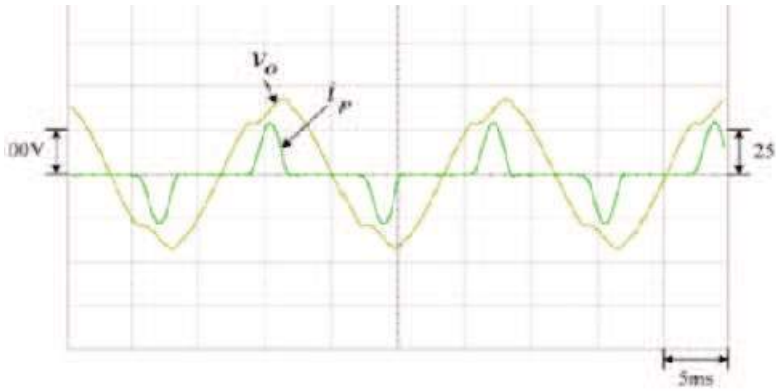

Figure 6.3: Distorted output by non-linear load

As a consequence of the DC components may lead to flux saturation in transformer, the inverter may conduct unstable voltage control which may destroy the power switches of the inverter. Because the output current is affected by loaded conditions for the voltage control application, one may not use current regulator to avoid flux saturation. It is difficult to design proper flux level to meet the requirement of flux in wide frequency range. To meet the requirement of both size and cost of transformer, we usually let the flux level be saturated in low frequency. And this design will cause more voltage harmonics at low frequency operation.

In practice, to modulate high frequency signal using both finite carrier frequency and fixed-sampling rate by microprocessor will introduce voltage harmonics. For line frequency transformer, flux saturation may occur contributed by large non-linear load current and DC component. One of the examples reported in figure for single-phase rectifier, the total harmonic distortion of input current goes up to 136

We need to avoid flux saturation of the transformer is one of the important topics in galvanic isolated inverter. In figure there is a conventional transformer-based single phase inverter with voltage controller and DC offset canceller. Although the research using DC offset canceller to release the influence of DC offset voltage on transformer, the time delay yielded by detected DC current results in deterioration of voltage control using both proportional and integral voltage controller.

6.2 Proposed topology

It mainly consists of a full-bridge DC-AC module, a line frequency transformer and a non-linear load compensating module. Conventionally, an LC filter is installed in the output of DC-AC module to obtain sinusoidal voltage.

Then, a line frequency transformer is connected to the other end of LC filter. This structure is simple and generally leads to rather good voltage measurement at LC filter output. In order to reduce the loading effect on LC filter, a leakage inductance of the transformer and a capacitor installed at load side of the transformer are used to replace

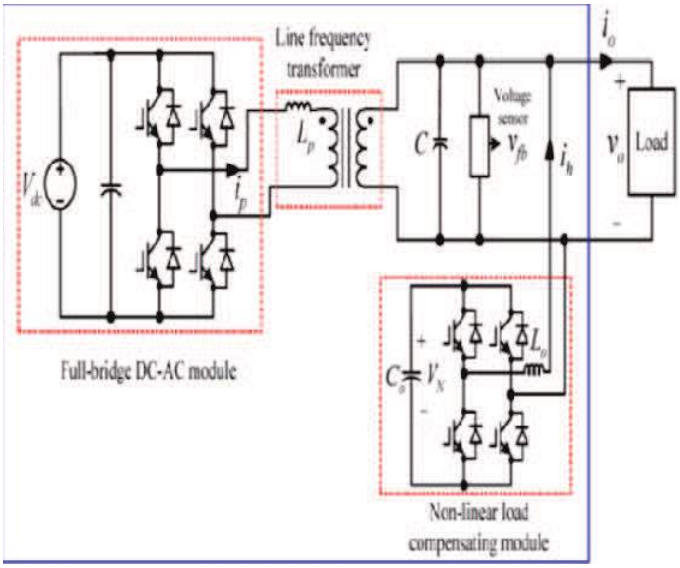

Figure 6.4: Proposed single phase transformer based inverter

the traditional LC filter in the proposed inverter. The voltage sensor is installed in load side of the transformer. The non-linear load compensating module connected in load side is constructed by a full-bridge circuit, an inductor and a capacitor which acts as energy buffer instead of a DC power source. Under non-linear load condition, the capacitor releases energy to share part of the inrush current with the inverter, and supplements its energy from the inverter under constant DC-link voltage with PFC control.

6.3 Basic overview

Space vector PWM (SVPWM) three-phase voltage source inverters (VSI) are an important interface between the grid and distributed generation systems. However, traditional SVPWM brings drawbacks to current controller, because it cannot deal with the grid voltage harmonic disturbance and nonlinearity of the system. PI controller, predictive algorithms and real-time sampling techniques have become basic methods to solve these problems. Most of these methods depend on the measure

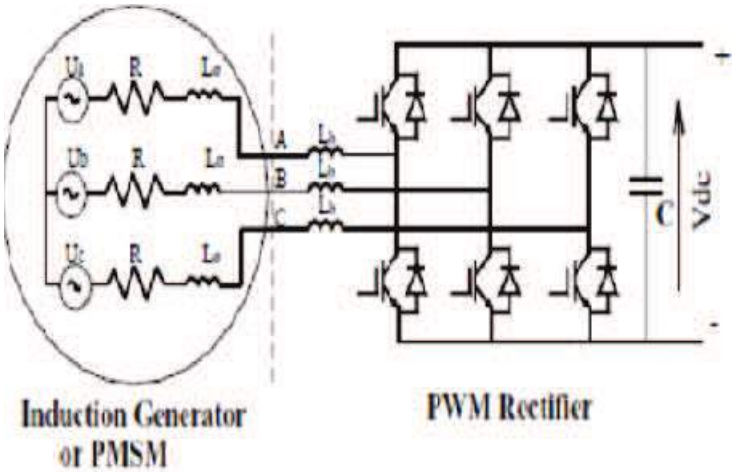

Figure 6.5: PMSM PWM rectifier system

voltage and current accuracy. If DC voltage (Vdc) sensor, one of the most important sensors, sends out an incorrect signal, not only could the output current quality be below the requirements of some standards, but also the inverter can be damaged in some serious situations. In this paper, PI and predictive methods are simultaneously utilized to control a three phase grid-connected inverter. PI controller is given a new function: Monitoring and controlling Vdc. In this new control structure, the output current of the inverter has high quality, and more importantly, Vdc can be double checked to guarantee the inverter reliability and safety. If a Vdc sensor fails or cannot send out the accurate signal, the PI controller will become a Vdc protection controller to ensure the inverter normal operation.

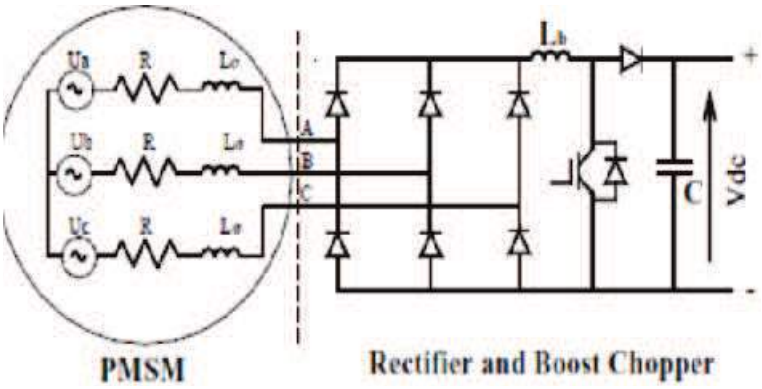

Figure 6.6: PMSM and boost chopper control system

Chapter 7

Simulation analysis and results

7.1 PSIM Simulation Circuits

During literature survey of the project some of the simulation work of the basic inverter circuits and then modification of the inverter circuits in PSIM is being processed. With the use of this simulation results of the high power inverter circuits, further implementation can reduce the complexity of the particular topology. Here for the analysis purposes basic rectifier and inverter circuit some of the simulation has been done so that according to that result variation in the results and parameters have been obtained. By basic simulation circuit, further correction and shaping in voltage waveforms and current waveforms are being obtained.

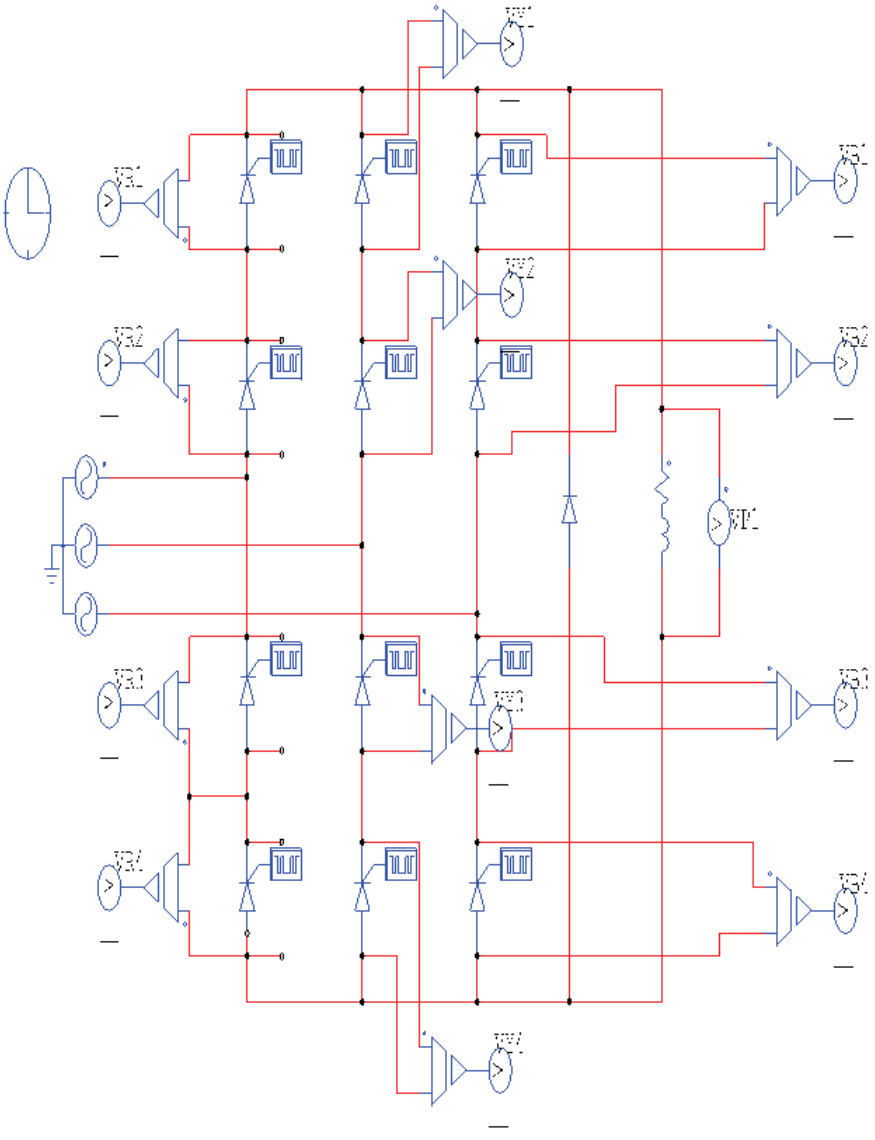

Figure 7.1: Basic inverter circuit with modification

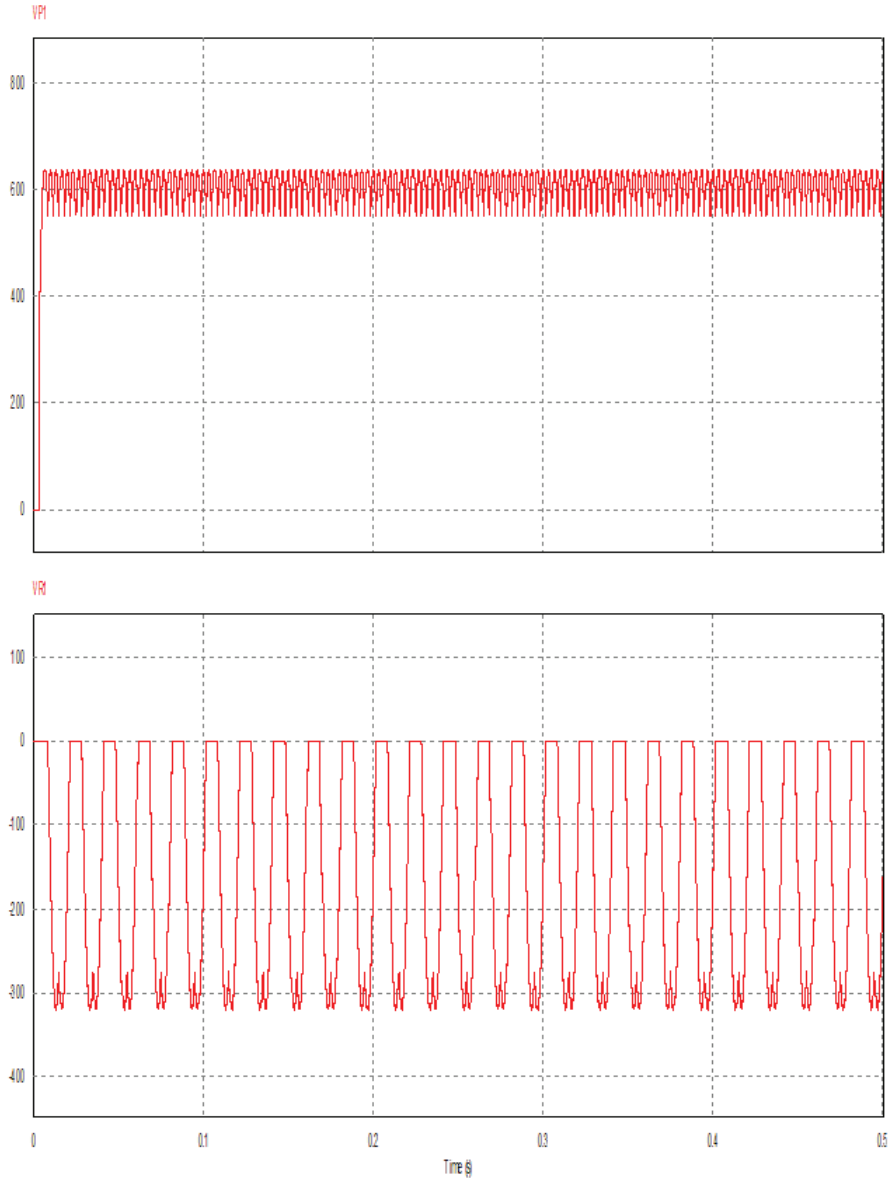

Figure 7.2: Output voltage and R-phase waveforms

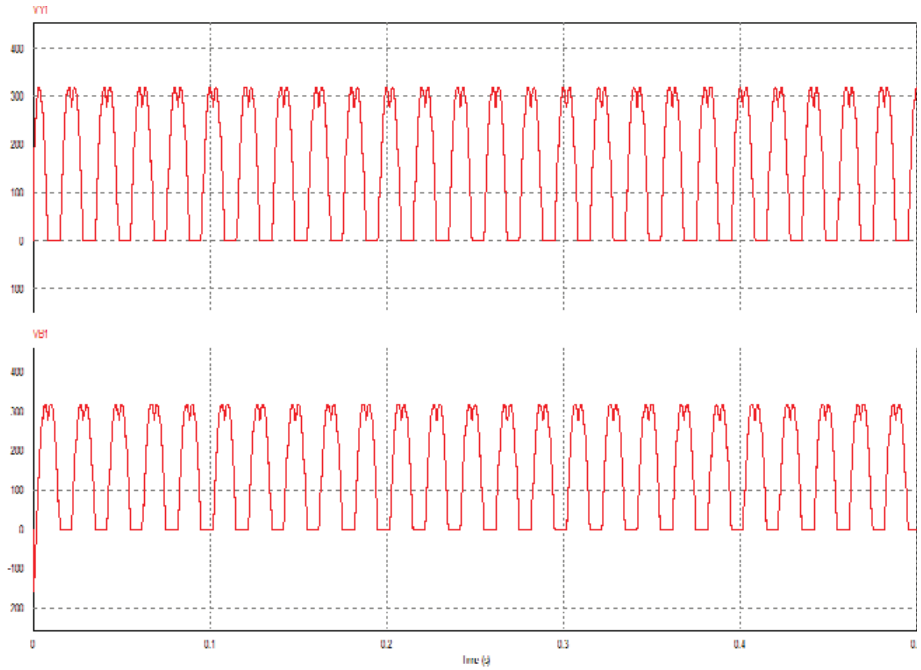

Figure 7.3: Y and B phase waveforms

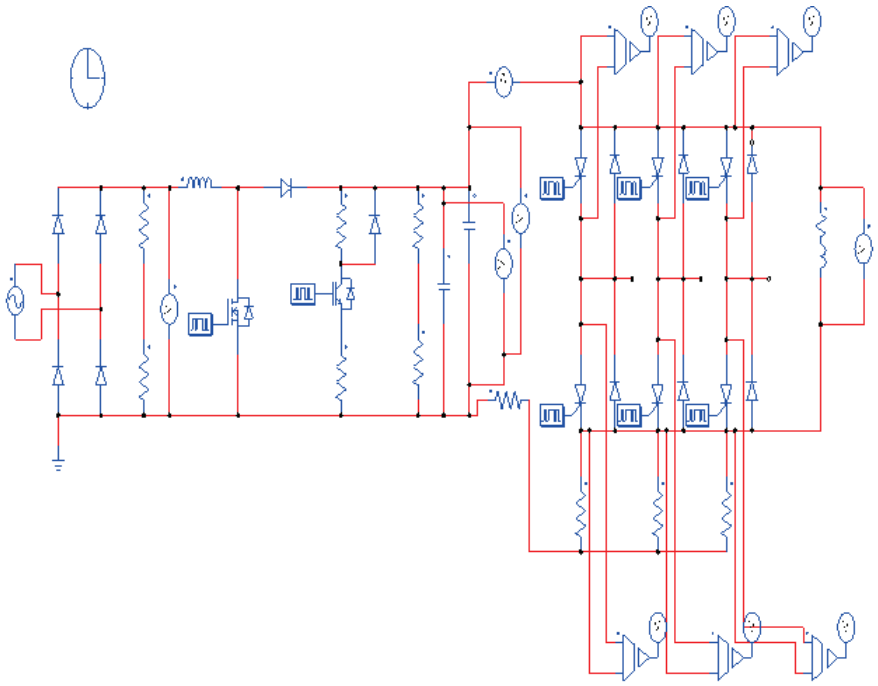

Figure 7.4: High power module circuit

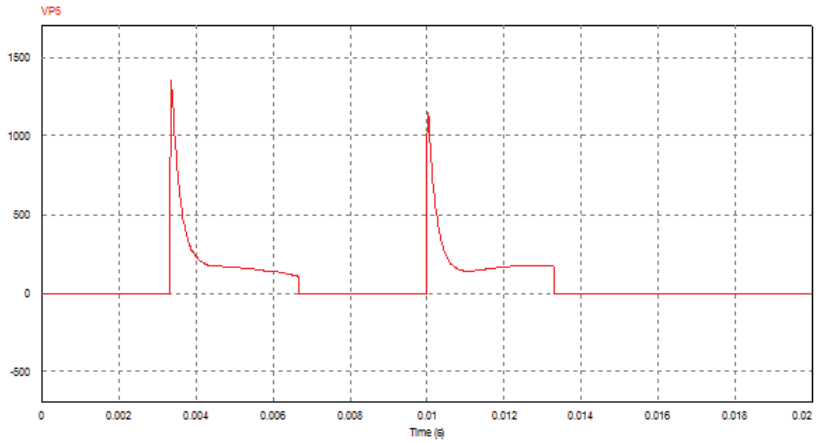

Figure 7.5: Voltage across Thyristors

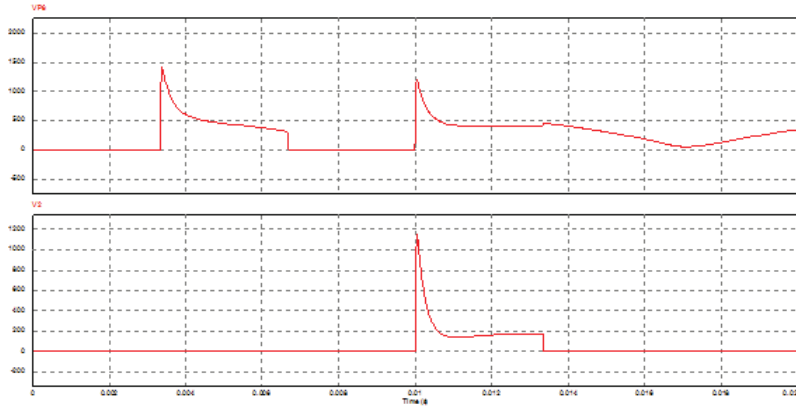

Figure 7.6: VC1 waveforms

Thus we can say that these are the basic inverter with protection sensors and also a high power device module circuits. In basic inverter, we can observe the waveforms of the circuits and then we can further modify the results to eliminate harmonics and losses in the running schemes.

So currently this basic simulation work is based on the thyristor switch and with the high power circuit of the inverter with proper fault analysis is going on. According to this simulation results, further modification and then the close loop system of the protection control circuits will be done for the development of the protection system for high power inverters. If we go further in simulation work we have to change and vary many parameters according to output as we obtained. So in this protection system for high power inverters simulation work is required not only for result purposes but also for the parameters verification so that we can exactly come to know about the protection systems. So in this process of the development of the protection system, many inverter skims have been used and according to that result we can obtain the parameters perfectly.

With single phase and three phase circuits of the inverter, Mcmurray inverter system is also required for the simulation because in Electrotherm right now they are using mcmurray inverter system and they want to implement this system with single phase and three phase system with thyristor and FPGA control systems. So I have added some of the simulation results of mcmurray inverter and three phase inverter also for the better output. And also the result and view for the FPGA controller. So after simulation result ,in FPGA controller, programming will be done for the protection parameters and then hardware will be developed. The programming of the FPGA is according to the output required and then FPGA controller will be connected with the hardware for the results.

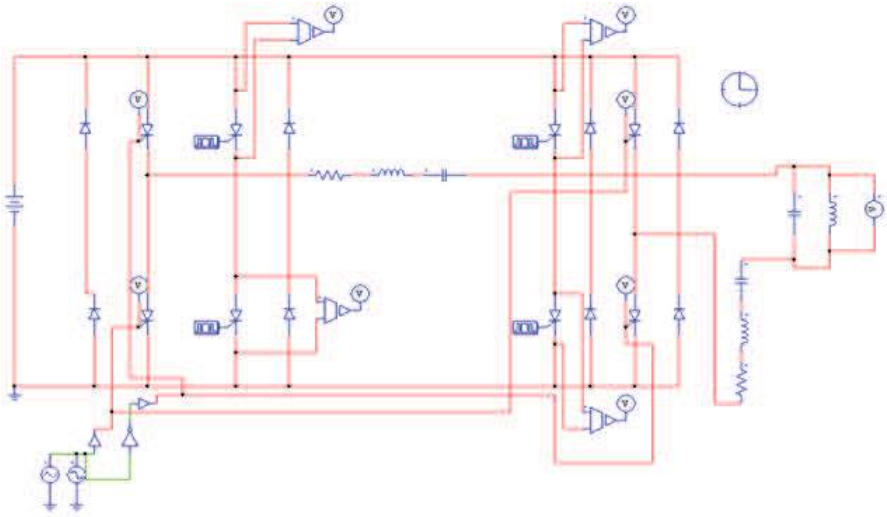

Figure 7.7: Mcmurray inverter Bedford circuit

Here in Fig7.7 and Fig7.8, it shows that in mcmurray inverter, load side waveforms are being measured for the analysis and implementation of hardware as well as FPGA Controller.

Here in Fig7.9, it shows the single phase mcmurray inverter circuit in which four Thyristor are connected and its results are shown in Fig7.10. Here three phase analysis can be done also for the protection purposes. And according to that further implementation is being developed. And according to that FPGA Controller results

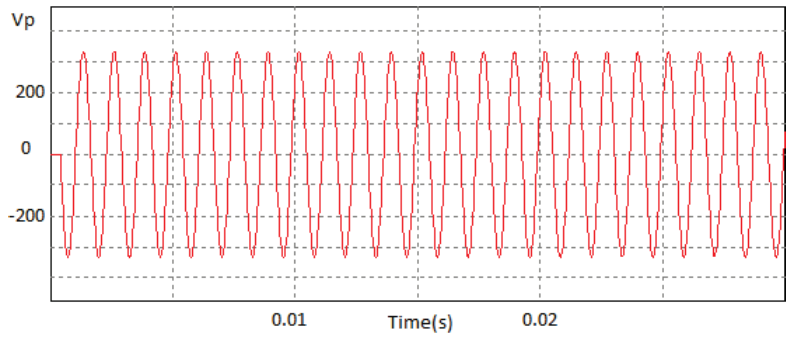

Figure 7.8: Output voltage waveforms

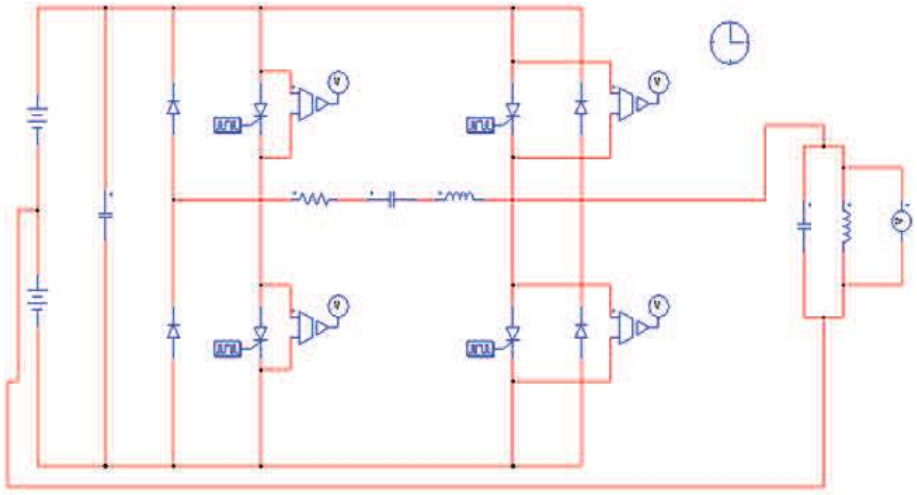

Figure 7.9: Single phase Mcmurray inverter circuit

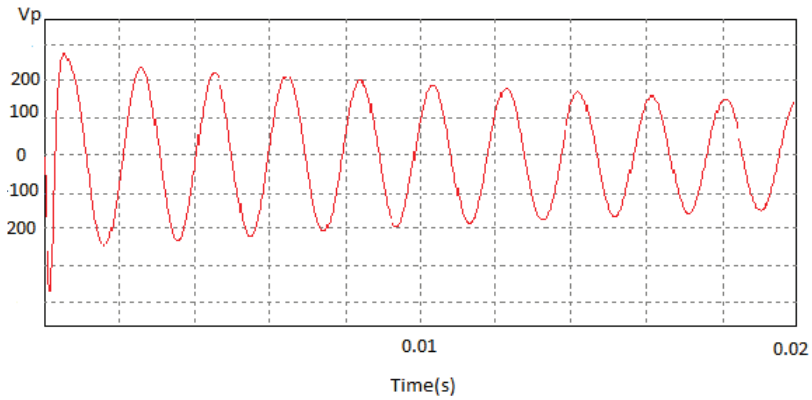

Figure 7.10: Output voltage waveforms

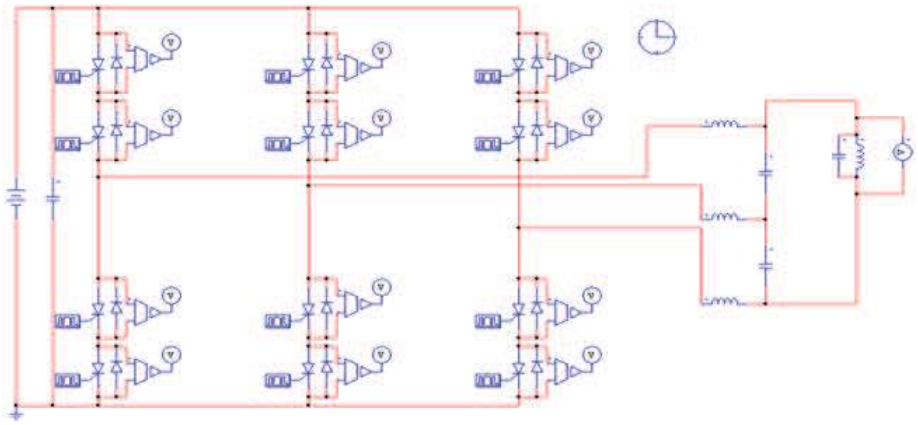

Figure 7.11: Three phase thyristor circuit

are being obtained.

7.2 Further Overview

Basically in this topic Protection system for high power inverters all the necessary data and reference materials should be considered. In this topic first of all designing and implementation of the high power inverter circuit is to be made so that we get the basic idea about the high power module devices. For particular topology of this topic we should practice the basic medium voltage and high voltage power module then and then only we come to know about the modified high power module.

In high power circuit we can use many components with complementary to each other and also for the precision of the output we can change the particular circuit weather it is semiconductor devices or the other element of power electronics. FPGA analysis is very important in this protection system development and as the system is high power, protection system should be suitable for instatnt fault correction. According to the simulation results, hardware implement is done and according to this hardware result, logic is developed in FPGA(field prgrammable gate array) controller and according to that protection system for high power inverters is developed. Ac-

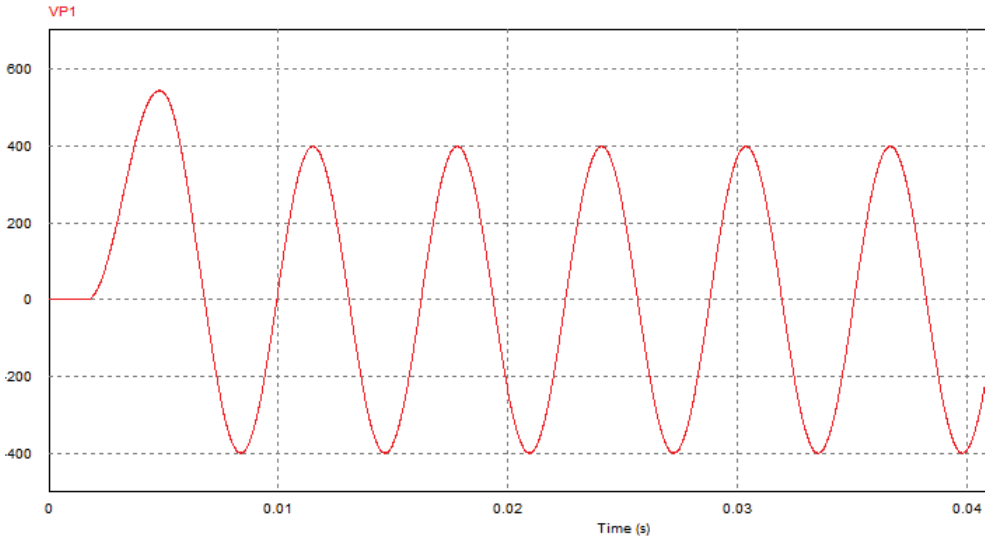

Figure 7.12: Output voltage waveforms

cording to the simulation results, output of hardware for the refrence values of FPGA is being obtained.

This figure 7.1, presents basically protection which is given to the high power inverters. In that basically, RC snubber and voltage balancing is require for the thyristor for protection purpose. And other parameters also should be considered. Here we can say that protection of all the parameters should be considered. Here Snubber circuit, Thyristor, Load circuit, Filter and supply side, all the components and parameters should be taken in to account for the analysis purposes for the protection system.

Basically this figure7.16, shows the protection system for high power inverters. In that,four thyristor are connected in one lag and total eight thyristors are connected in single phase. Filter is placed for the ringing waveforms and as soon as waveforms are obtained from load side, its being compared with comparator and one semiconductor switch is placed for 500us and after that it will get closed so that output result is not affected. Voltage and current is being obtained by sensor and by giving NOT gate to comparator both output pulses of comparator is given to the gate terminal of thyristor. Waveforms results of voltage across thyristor, voltage , current, output

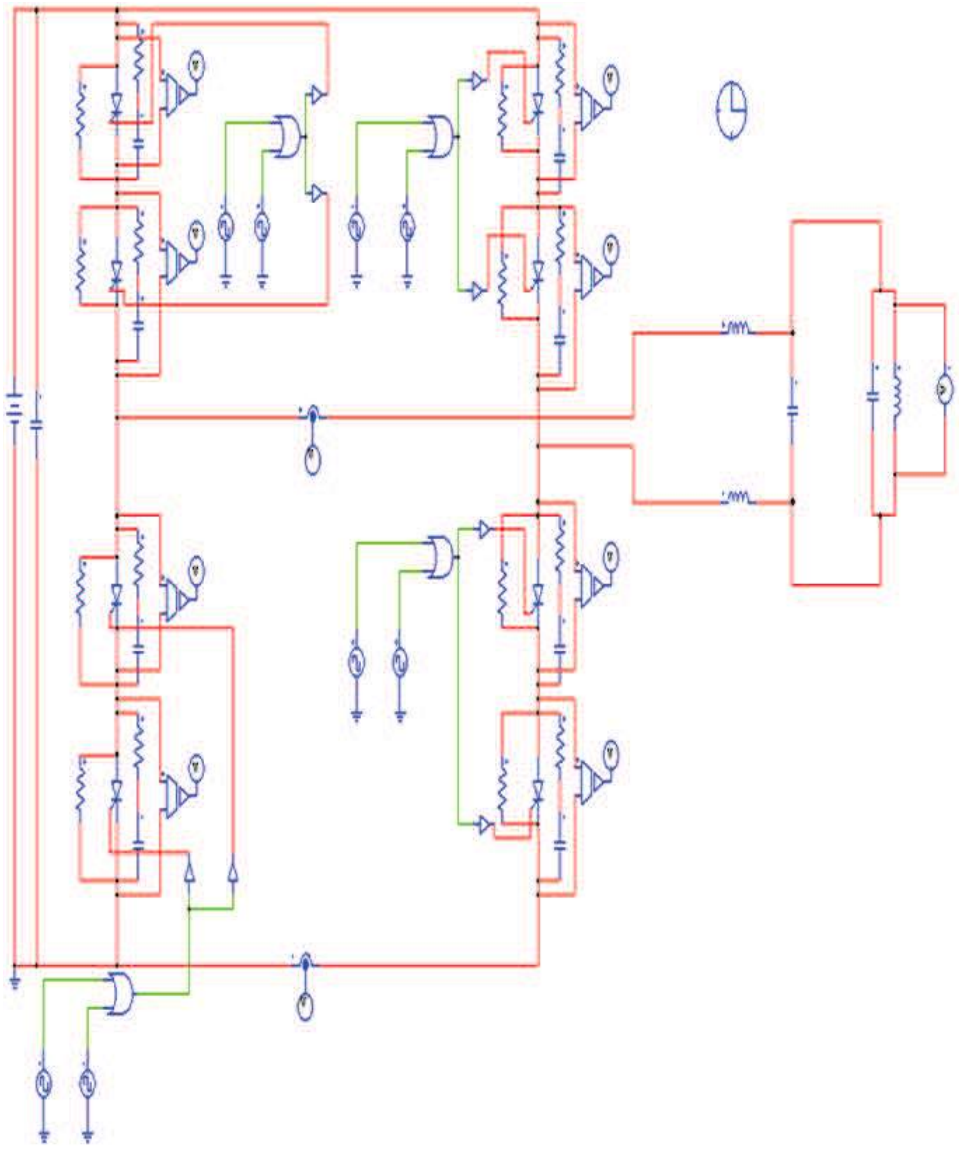

Figure 7.13: Single phase thyristor circuit in PSIM

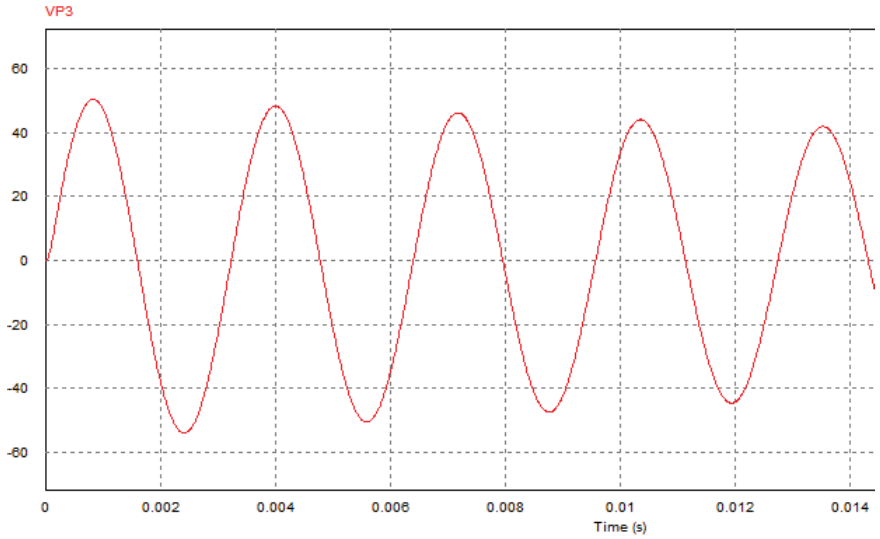

Figure 7.14: Output voltage waveforms

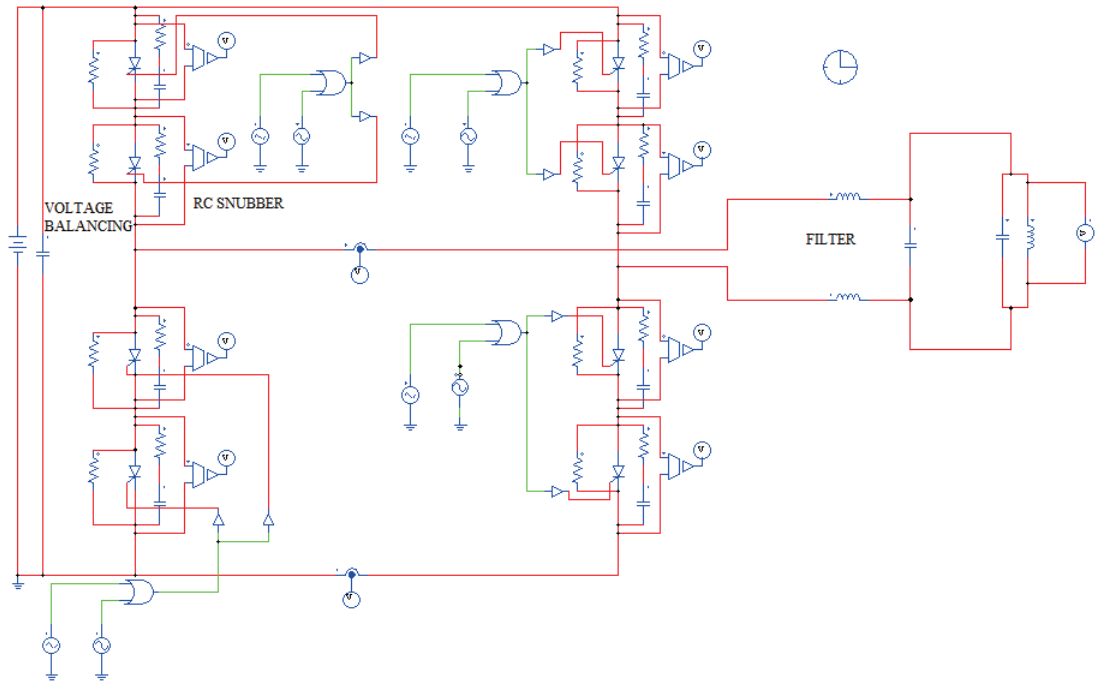

Figure 7.15: Basic Protection Circuit

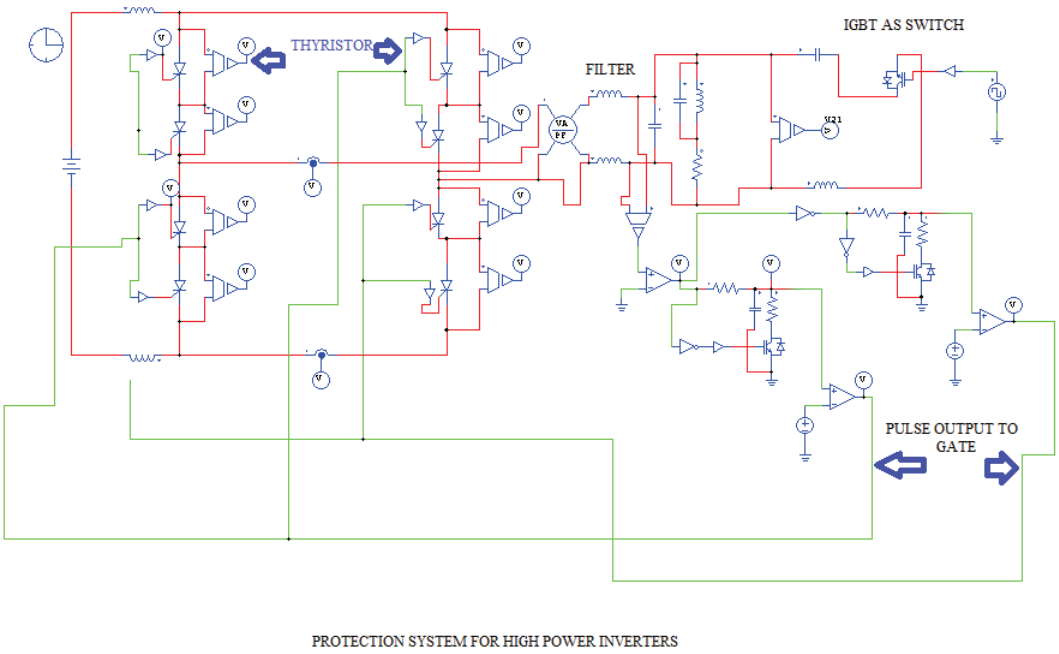

Figure 7.16: Protection System For High Power Inverters

voltage are being obtained for the analysis of FPGA controller.

Here in Fig7.17, it shows the voltage waveform across the thyristor and here in this system in single phase four thyristor are connected in one lag, it means two thyristors are in series in one lag so during positive half cycle four thyristor will conduct and negative half cycle other four thyristor will conduct in single phase system. Here the same voltage across thyristor waveforms we can get in hardware also which can be taken as a reference for the controller section. If we are using two thyristor are in series then the results of that two thyristor will be almost same because thay are blocking same voltage but the voltage will get divide so as many thyristor used in a system we can say that the voltage will get balanced, so the load or stresses on each thyristor will get reduced. So according to the simulation and hardware results are being observed. By changing the parameters current and output voltage waveforms can also be varied.

Here in Fig7.18, it shows the output voltage waveforms of the system, basically

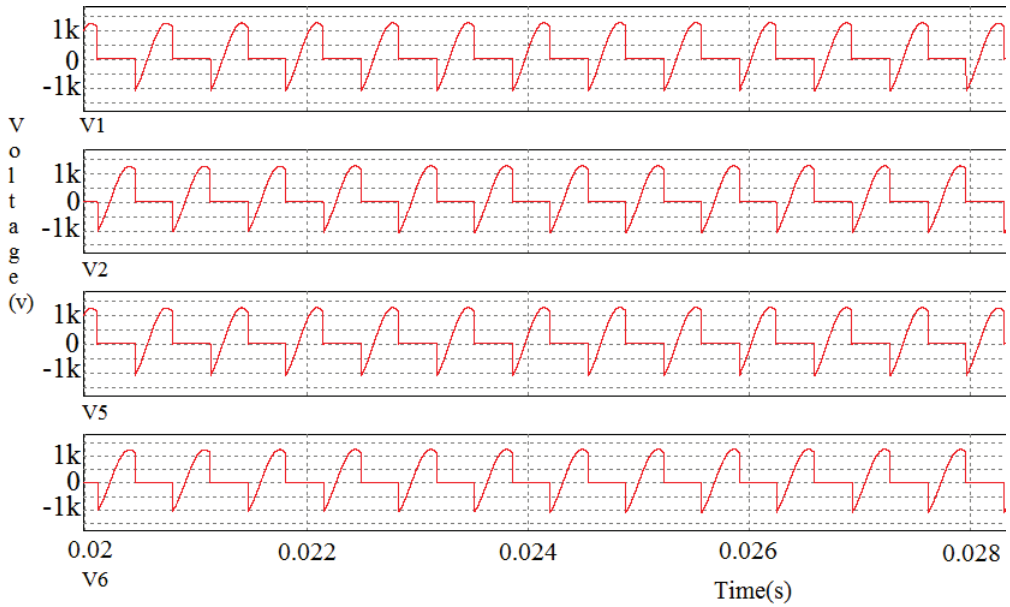

Figure 7.17: Voltage Across Thyristor

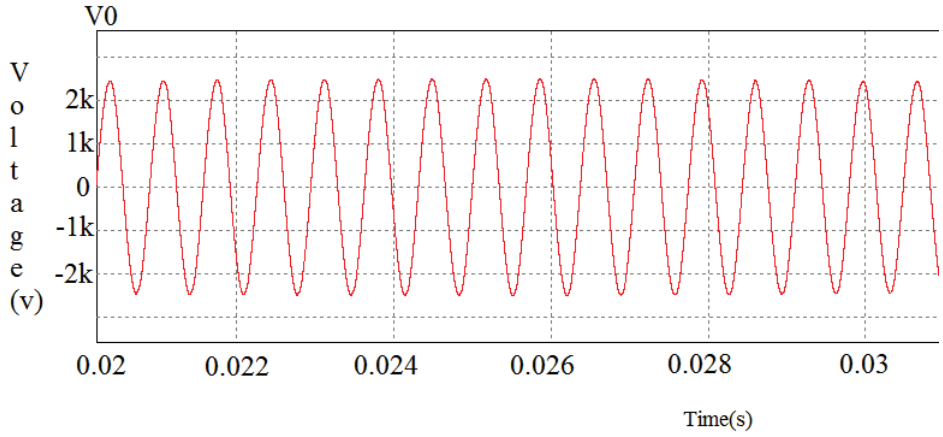

Figure 7.18: Output Voltage Waveform

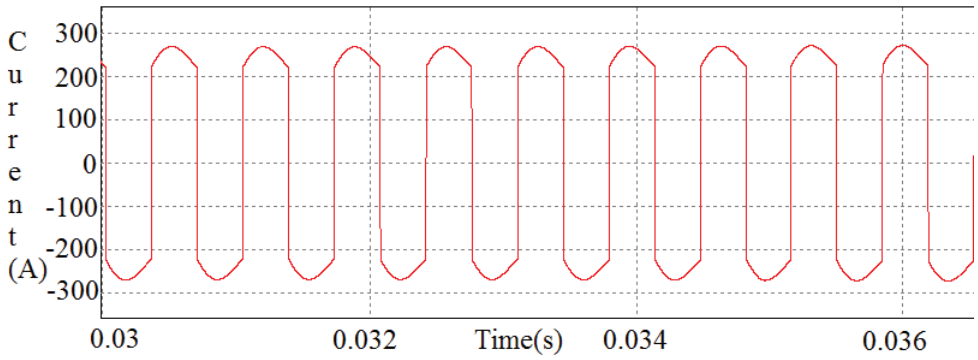

Figure 7.19: Current Waveform

here output voltage waveform should be pure sinewave and it describe the system without any fault or losses. Basically this output voltage waveforms are pure sinusoidal and which can be obtained by using LC filter also if harmonics or spikes are there.

Here in Fig7.19, it shows the current waveforms through the system and according to charging and discharging mode, positive and negative cycle, waveforms to be obtained. Basically during operation periods, voltage across the thyristor which are shown in Fig are due to inductive load so during positive half cycle, it slightly goes below zero due to inductive load and current which are shown in Fig.4 is depend on load which are connected. So according to the calculation of parameter, voltage and current waveforms can be varied as load changes. Other thing is to be consider as a power factor balancing, PF is maintained throughout the system nearer to unity as much as possible to get desired values so here we are getting PF is around 0.95 which very much nearer to the unity and that shows the ratio of low losses in the system. PF should be in proper manner.

Here Fig7.20, shows the voltage and current waveforms together and other Fig7.21, shows the voltage, current and voltage across thyristor waveforms of both positive and negative half cycle. Here we can observe many things and most importantly PF which

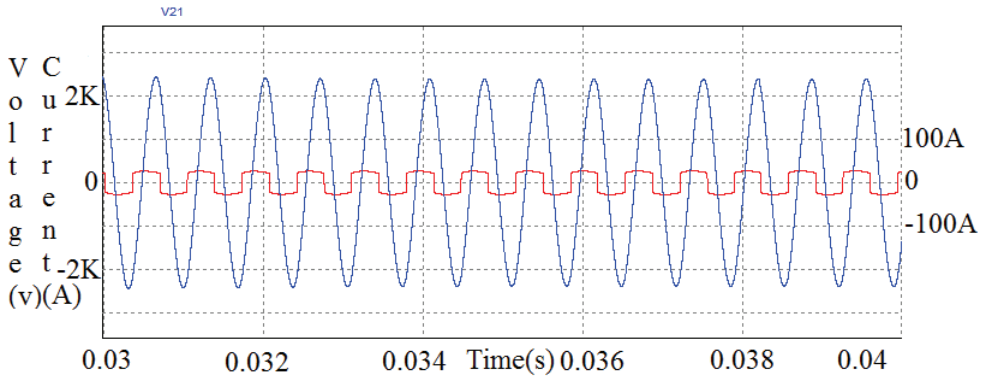

Figure 7.20: Current and Voltage Waveforms

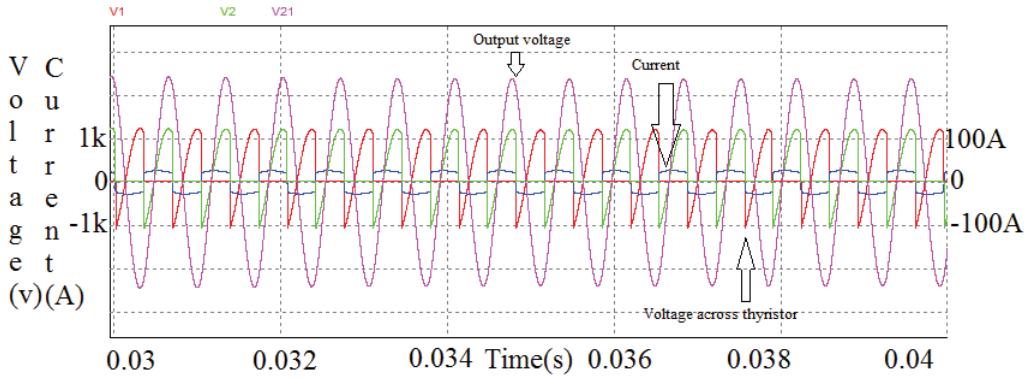

Figure 7.21: Voltage Across Thyristor, Output Voltage And Current Waveforms

shows 0.95 value. The hardware results we are getting are same as the simulation results of voltage across thyristor, current, output voltage waveforms etc. Thus it is easy to interphase this simulation results with FPGA controller and according to this simulation results limits for the protection system to be developed in such a way that the whole inverter of high power should be protected. Here limit for each of the parameter is created in FPGA so that values goes above or below that value the controller works and gives feedback. So according to that whole system is protected.

Chapter 8

HARDWARE appraoch and FPGA Controller

8.1 Basic overview

Basically in this protection system , many hardware components are required for the systems. In which buffer, ADC ,DAC some of the main components are there with ALTERA FPGA Controller IC.

8.2 FPGA Controller

This Field Programmable Gate Arrays (FPGA) design and development tutorial provides a high level overview of programming techniques and architectures for rapid development of FPGA-based hardware with National Instruments Compact RIO and R Series intelligent DAQ systems. Use this guide to understand how Lab VIEW graphical programming tools can enable you to quickly develop reconfigurable hardware logic and successfully architect complex applications containing FPGAs, real-time processors, networking and general purpose PCs. This document illustrates recommended software architectures and introduces you to the hundreds of built-in functions and tools in Lab VIEW that streamline the development of sophisticated embedded appli-

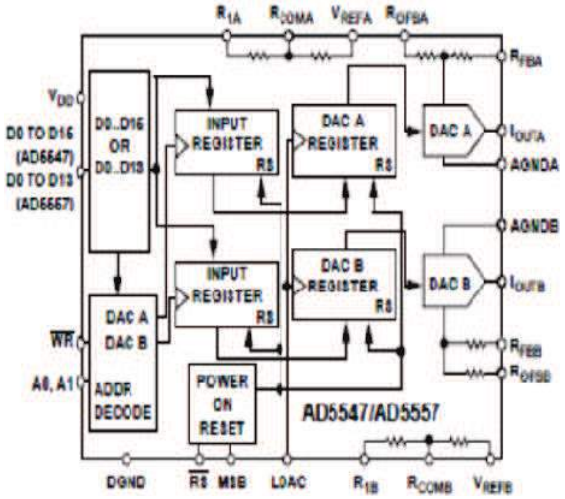

Figure 8.1: 5547 ADC

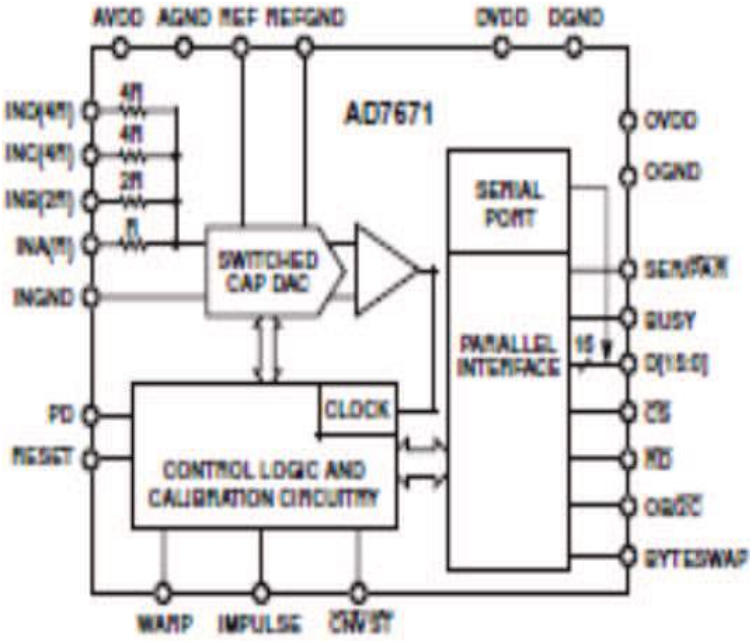

Figure 8.2: DAC 7671

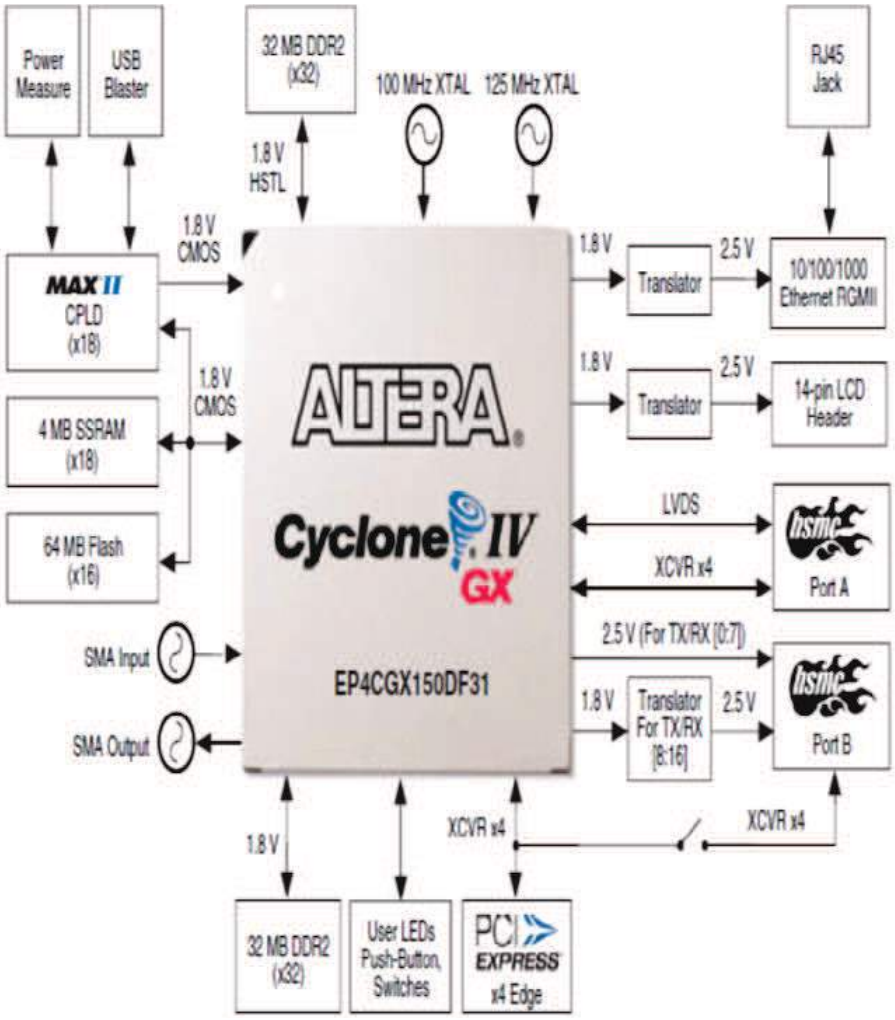

Figure 8.3: Block diagram of FPGA

cations. These integrated hardware/software tools enable you to quickly and reliably design, prototype and deploy advanced reconfigurable FPGA systems.

8.3 FPGA working

Lab VIEW FPGA application development is the first step involving interaction with the I/O modules and analyzing the acquired signals. The FPGA makes it easy to create advanced applications requiring high-speed control, precise timing, triggering

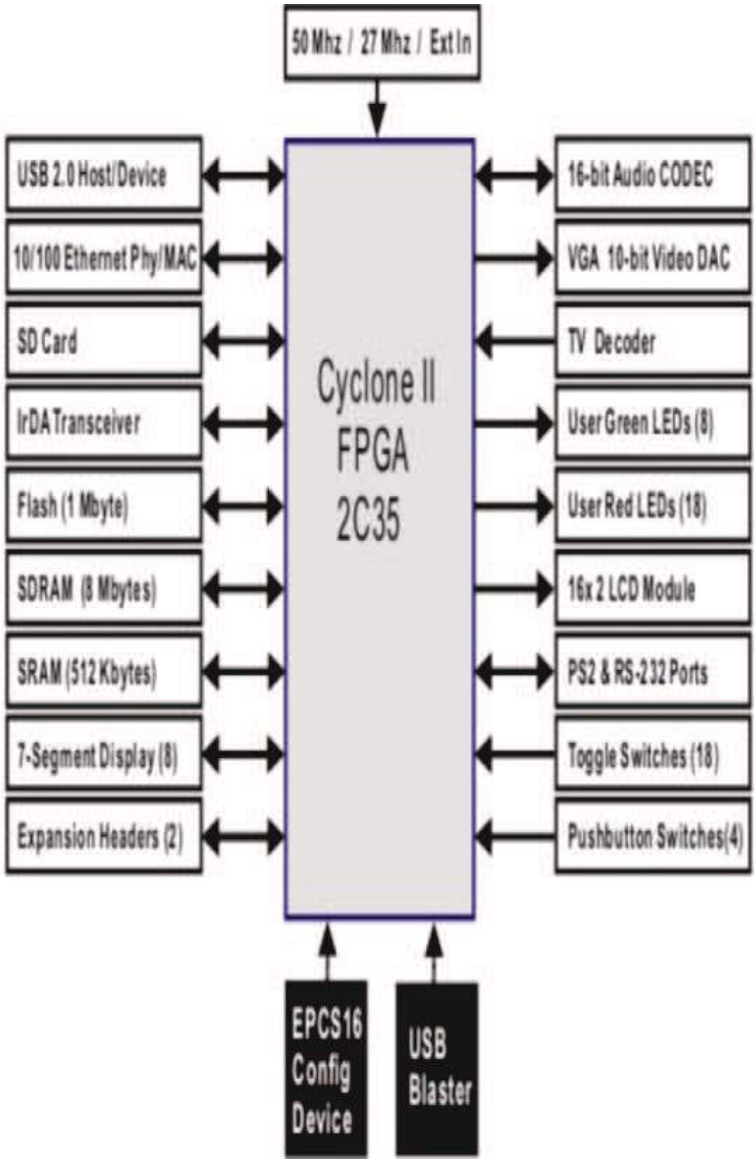

Figure 8.4: Functional block diagram of FPGA

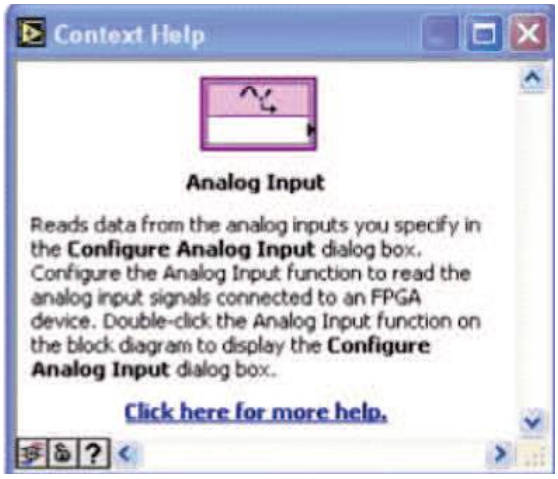

Figure 8.5: Analog block of FPGA

and synchronization. Lab VIEW FPGA offers intuitive function blocks (called Virtual Instruments or VIs) that make the process of acquiring and generating both analog and digital signals straightforward. Functions from the FPGA Device I/O pallet can be used for any application requiring interaction with signals; ranging from a simple analog input reading from a thermocouple to generating PWM signals for precise control of a servo motor.

With Lab VIEW FPGA you can customize hardware to acquire at high rates with high accuracy. You can precisely control timing in your application by placing a Loop Timer. The Loop Timer gives you the option to control the timing of a loop as either a multiple of the hardware clock with rates in the order of nanoseconds or in microseconds or milliseconds. With a hardware clock rate of 40 MHz the Loop Timer can be used to achieve loop rates as multiples of 25 nanoseconds.

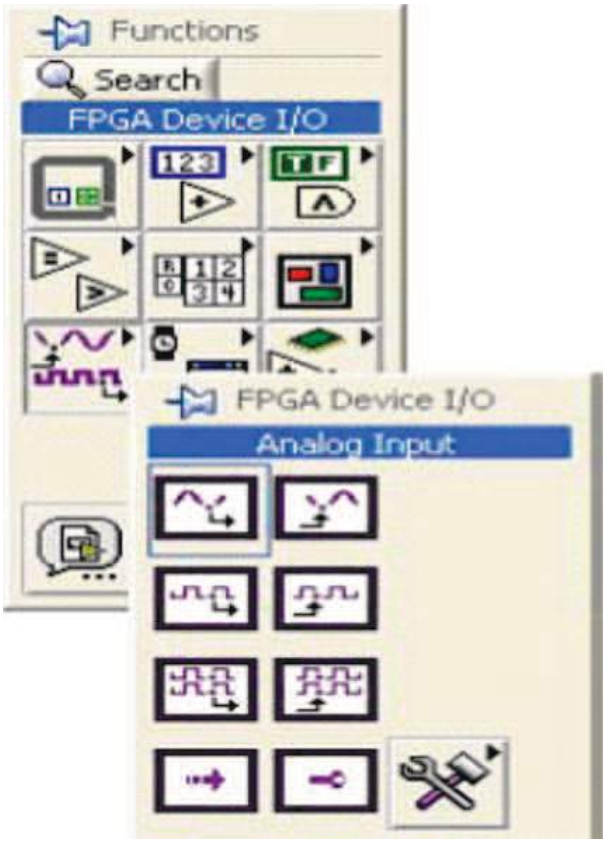

Figure 8.6: Device block of FPGA

Figure 8.7: Loop timer

Figure 8.8: Saturation block

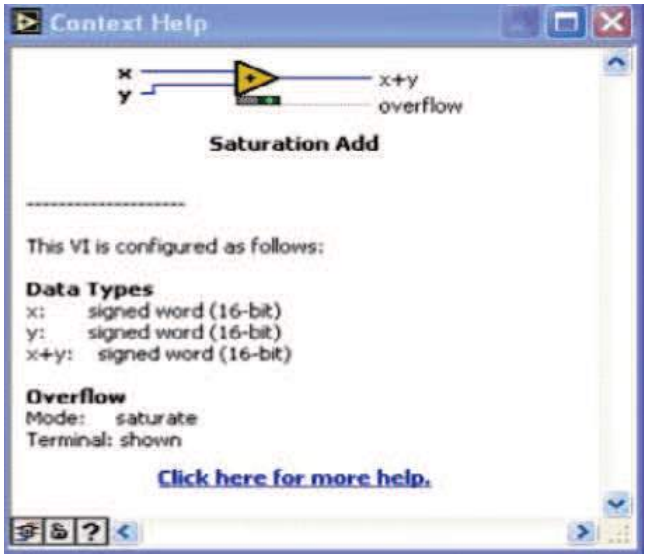

Figure 8.9: Help block

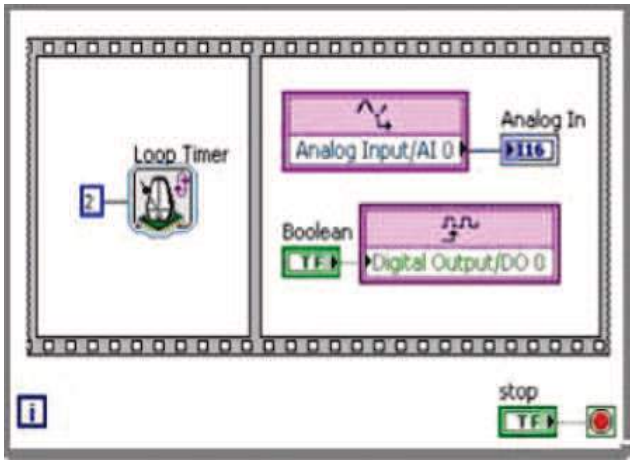

Figure 8.10: Loop timer output block

Here we have shown the basic block analysis of the FPGA Controller which are being carried out for the hardware approach and according to the variation of the parameters and results, the whole system is being developed.

Chapter 9

Hardware tests and result analysis

LabVIEW FPGA application development is the first step involving interaction with the I/O modules and analyzing the acquired signals. The FPGA makes it easy to create advanced applications requiring high-speed control, precise timing, triggering and synchronization. LabVIEW FPGA offers intuitive function blocks (called Virtual Instruments or VIs) that make the process of acquiring and generating both analog and digital signals straightforward. Functions from the FPGA Device I/O pallet can be used for any application requiring interaction with signals; ranging from a simple analoginput reading from a thermocouple to generating PWM signals for precise control of a servo motor.

9.1 Hardware Analysis

Here basically in hardware implement, one power circuit with ZCD is developed and the values with parameters like voltage across thyrisor, current in the system, reactance, impedance, capacitance etc should be measured and with taking the reference values of this parameters, power circuit is being developed. ZCD produce narrow pulses to every zero crossing point, its pulses are applied to the port of a FPGA controller. The output of this is ANDed with astable output of 555 or by triggering circuit or driver circuit of MOSFET as a high frequency signal. And output of AND

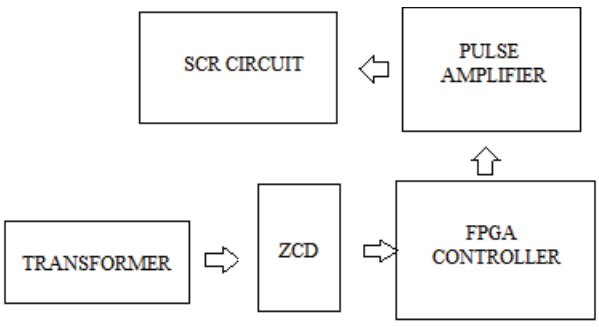

Figure 9.1: Block Diagram Of Power Circuit For Protection System

gate will be through amplifier & pulse transformer send to SCR gate. Reference values which can be generated by the analysis of power circuit can be modify also by varying the values in power circuit as well as ZCD output analysis. The waveforms which we are getting in this power circuit in oscilloscope are similar to the simulation results, according to that limits in FPGA controller can be decided and programme for the close loop feedback is generated. And we can also say that this whole system can be implement in high rating also for the protection of the system in some industry or somewhere. Programming in FPGA CONTROLLER is the heart of this implement of the system because all the analysis of feedback and other parameters are depend on the controller section. So basically we can say that here ZCD is used to generate 5V waveforms and that will used as a supply of FPGA Controller and it will turn on Controller section. So from controller we can generate pulses according to the load variation takes place and that pulses with combination of Triggering pulses of MOSFET will use by additional 24 DC circuit with pulse Transformer 1:1 Ratio to trigger Thyristor. And from that result we can analyze voltage waveforms of Thyristor and Voltage across Thyristor waveforms. Current and Voltage waveforms are being analyze for the power factor improvement. Basically here we want this kind of waveforms only for the closeloop analysis and for the programming point of view for the FPGA Controller, because here we want to develop protection system for the high power inverters and we have to put limit in our inverter with FPGA Data analysis. Here

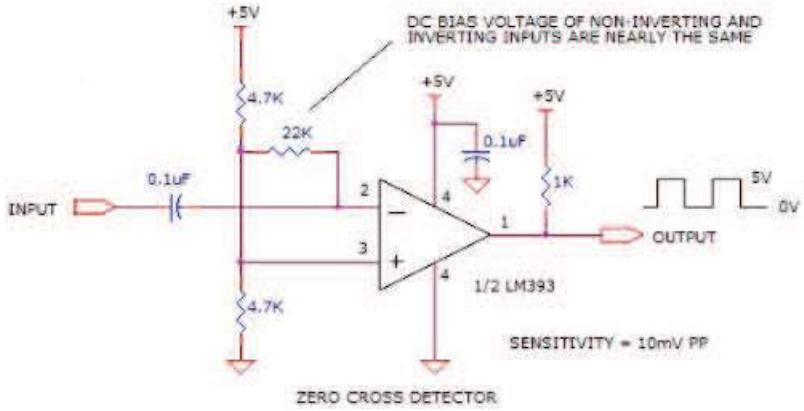

Figure 9.2: ZCD Circuit

this limit is developed in FPGA programming for protection purposes, in Peak value of the voltage across Thyristor, Snubber circuit, Current protection, Voltage analysis, Harmonic analysis and overall protection. So here limit is being fixed in all the protection parameters to give value feedback by FPGA Controller and for protection analysis, the FPGA will work according to limit, weather the voltage or current goes above or below desired value the FPGA Controller will sence accordingly. So here as soon as fault occures, the FPGA Controller will sense this fault and will give feedback in such a way that it will either stop the system or will reduce amplitude according to programming developed.

Hardware should be in such a way that simulation results which we have obtained are very much similar to the hardware results. Here in Fig shows the ZCD circuit that can be used in a power circuit to get the result of the parameters so that it can be used as reference for the FPGA controller limit code generation. The values we can see that LM393 is the regulator IC which can easily balance the voltage levels, capacitors with the values of 0.1uF are used with at least 5V rating. Resistors used here are 4.7K, 22K, 1K values. Basically output port of LM393 gives square wave signal as zero crossing detector circuit. Basically we want 5V output to give controller so from transformer we will supply to ZCD circuit and from ZCD we will get 5V detected

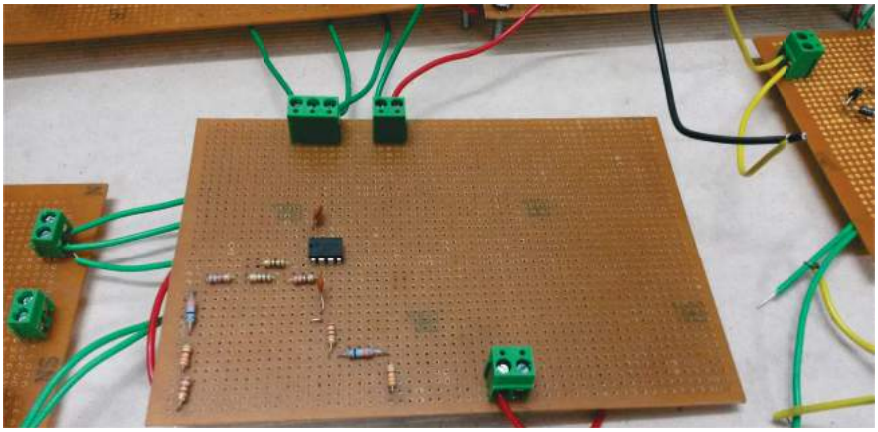

Figure 9.3: ZCD Circuit

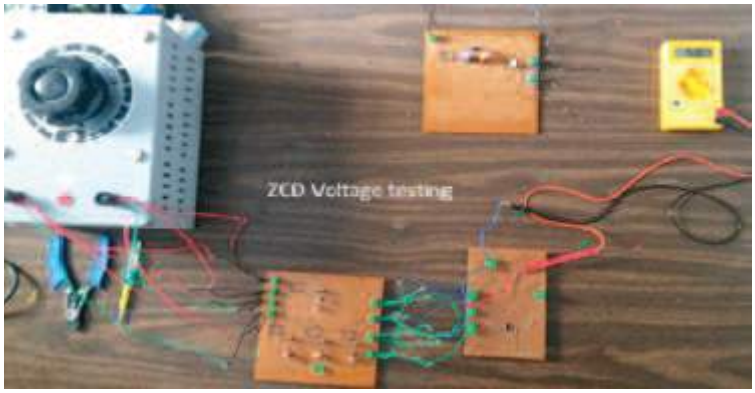

Figure 9.4: ZCD Circuit Voltage Testing

output which will given to the controller section.

Here in ZCD circuit, square wave with 5V output waveforms are being obtained. And this pulses are given to the FPGA Controller for the triggering of Mosfet and then that pulses are given to pulse transformer through 24V supply circuit to trigger THYRISTOR.

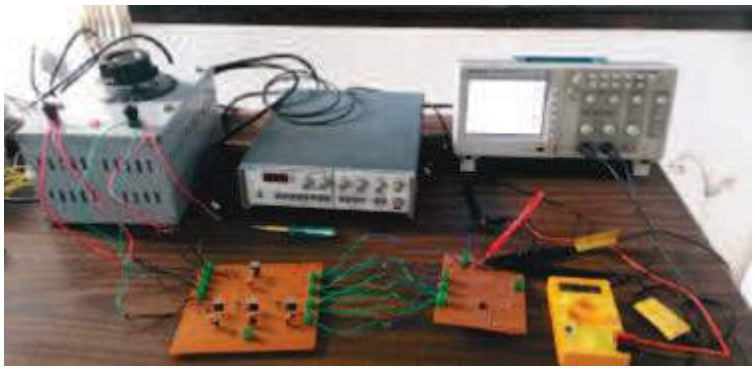

Figure 9.5: ZCD Circuit Testing

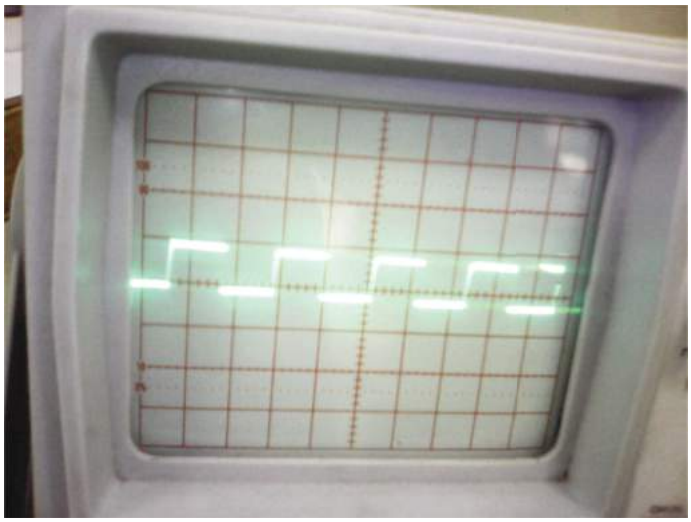

Figure 9.6: ZCD Circuit Waveforms [Scale: X-axis: 10ms, Y-axis: 5 V/ div]

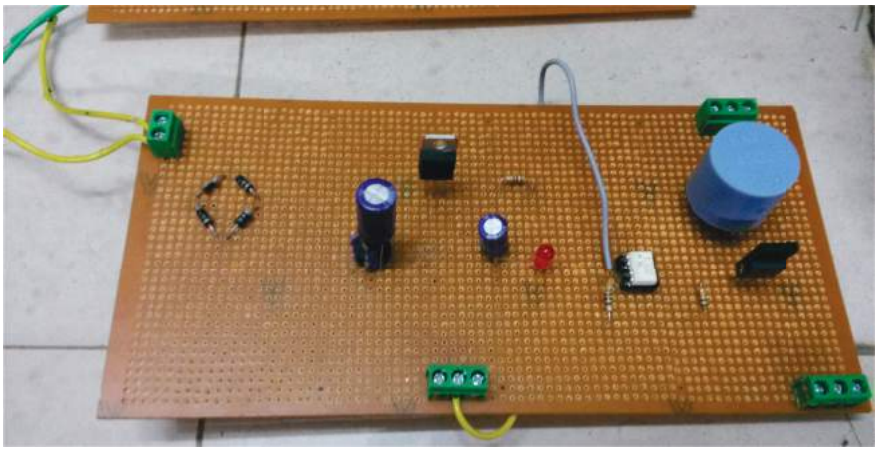

Figure 9.7: MOSFET Driver Circuit

Figure 9.8: 24V Output Circuit

Figure 9.9: MOSFET Triggering Pulses[Scale:X-axis:10ms,Y-axis:5 V/div]

Here in Fig 9.9 and Fig9.10, we are getting square pulses of the circuit which is being used to trigger MOSFET and the result of this circuit with combination of FPGA Controller is used to trigger Thyristor and for getting voltage across Thyristor waveforms.

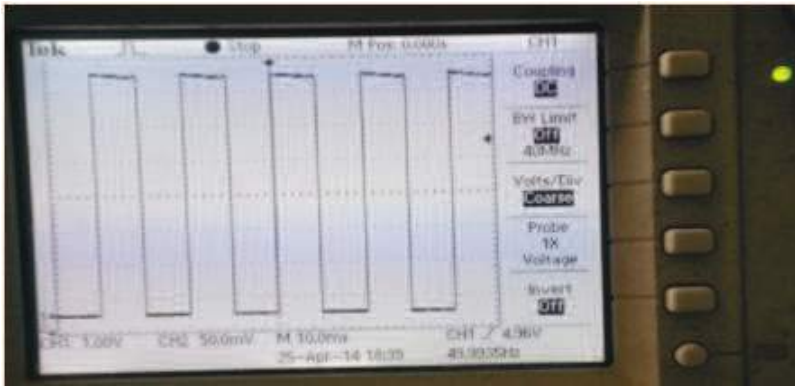

Figure 9.10: MOSFET Triggering Pulses[Scale:X-axis:10ms,Y-axis:5 V/div]

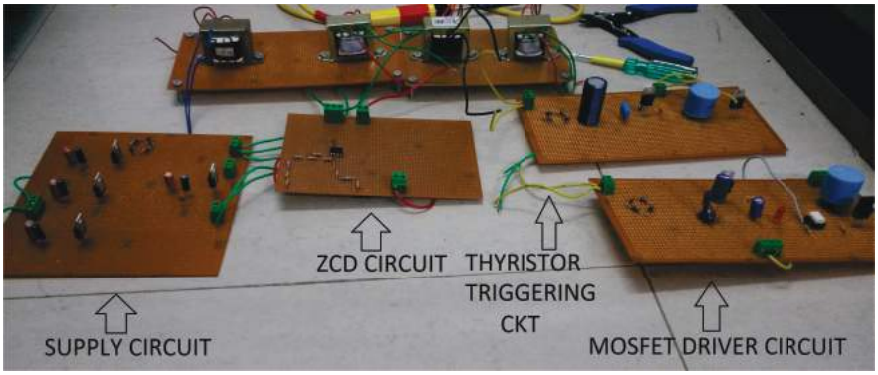

Figure 9.11: Protection System Testing

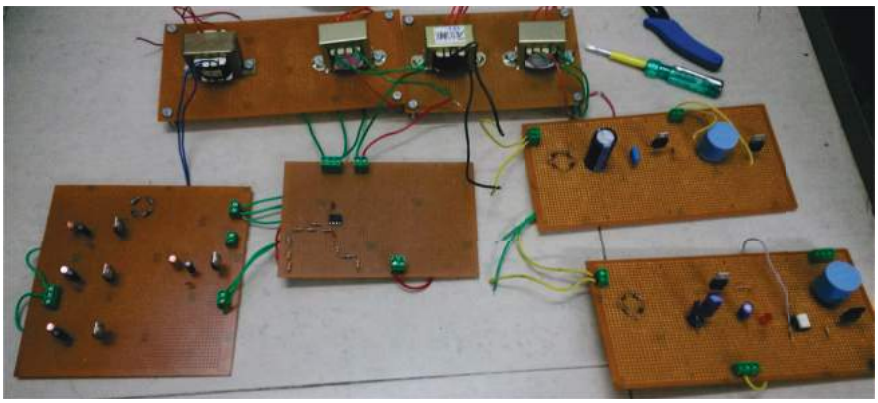

Figure 9.12: Protection System Testing Circuit

Here are the figures for getting of the Output voltage waveforms which have been obtained as a testing purposes.

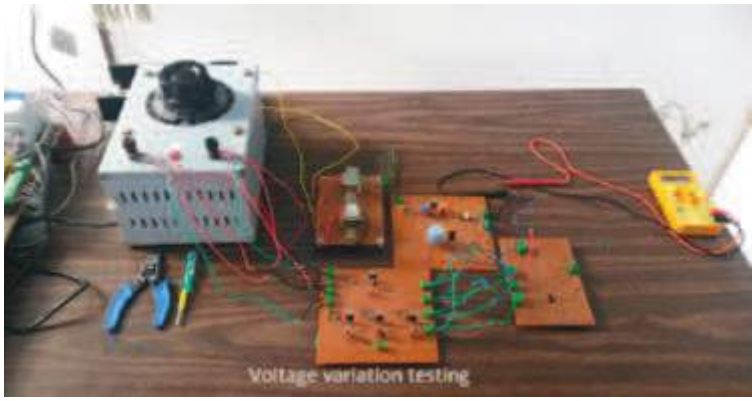

Figure 9.13: Voltage Variation Testing

Figure 9.14: Setup in Openloop

Figure 9.15: Output Voltage Waveforms Of Thyristor[Scale:X-axis:10ms,Y-axis:5 V/div]

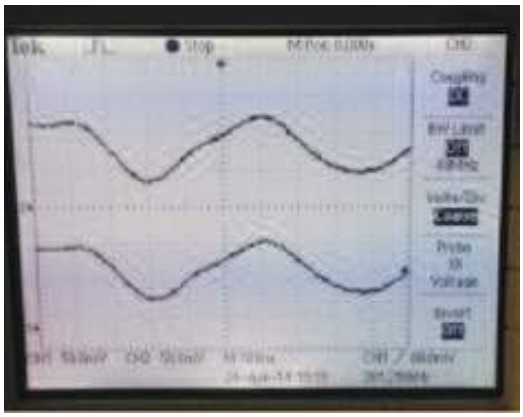

Figure 9.16: Output Voltage Waveforms Of Thyristor[Scale:X-axis:10ms,Y-axis:5 V/div]

Figure 9.17: Output Voltage Waveforms Of Thyristor[Scale:X-axis:10ms,Y-axis:5 V/div]

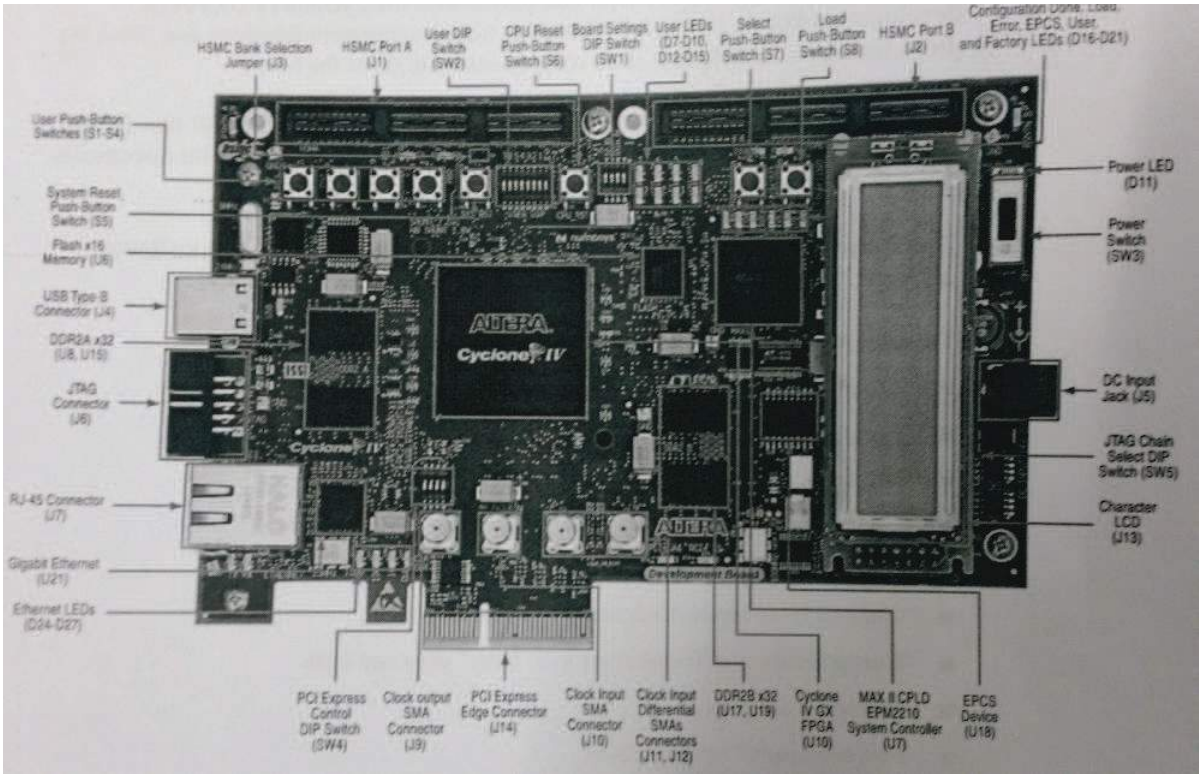

Figure 9.18: FPGA Controller Paper view

Here in the FPGA Controller in Fig 9.18, which is being used for the programming for the protection system for high power inverters. Basically here Buffer, ADC, DAC, Control switches are there for the proper analysis and it contains several blocks for the parameters and according to the programming it gives feedback to the system. It is more user friendly than the DSP because of the blocks containes. For protection we can put some limits in the controller, so as soon as the system contains faults or any error or it may goes above or below the limits, the FPGA will work accordingly. So with using this FPGA Controller development of programming is developed for the protection system for the high power inverters.

9.2 FPGA Based Results

There is option of Generate Target PROM/ACE on the process tab of Xilinx ISE which converts the BIT file to the PROM or ACE file. This PROM or ACE file can be downloaded directly into the FPGAs memory cells. We have to make sure that FPGA is connected to the PC where we are developing this design. After we download PROM or ACE file into the FPGA the FPGA is ready to be used as PWM Generator. We can give different input combination to see how the output of FPGA varies. This input can be given by switches whose pin number has been assigned to PWM generator input. The output can be seen by LED whose pin number has been assigned to PWM Generator output.

Figure 9.19: SPARTAN-3E Starter Kit FPGA

The design of processor that generates the signals, which give the output of PWM, requires a comparator that compares between two values. The first value represents the sawtooth signal and the second value represents the data that is entered by using switches or buttons on the FPGA board.The input signal can take another form

such as sinusoidal signal. When the design requires generating a sinusoidal PWM in FPGA, it must generate LUT using MATLAB and these data must be saved in block memory to control the PWM output.

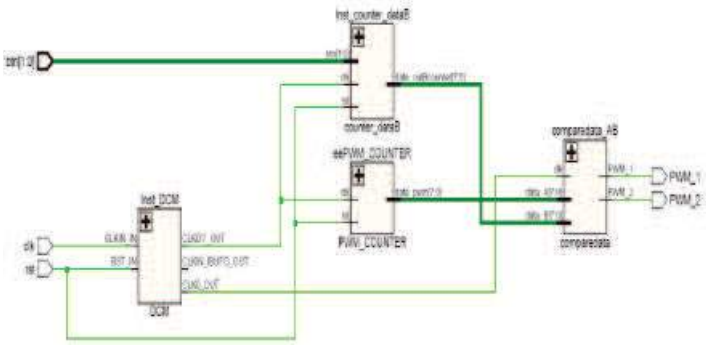

Figure 9.20: Schematic Of PWM Components

The properties of DCMs depend on the FPGA frequency and the type of this chip. DCMs provide advanced clocking capabilities to FPGA application. In this design, pin CLKDV is used to generate clk output with a frequency 3 MHz. This value is used to increase PWM counter. When CLKIN frequency is 50 MHz in FPGA SPARTAN3- AN, the output frequency of digital clock manager is created.

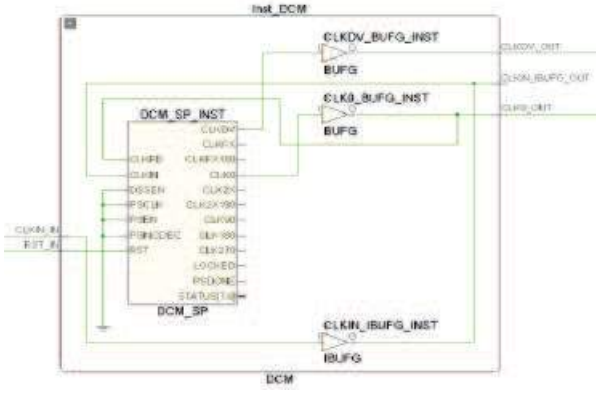

Figure 9.21: Digital Clock Manager

The Xilinx ISE simulator was used for functional verification of PWM Generator

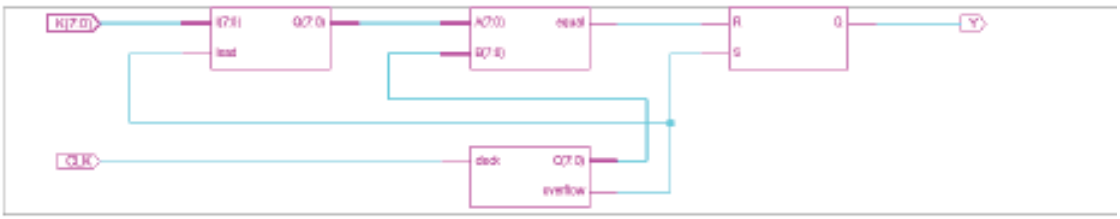

Figure 9.22: Schematic of High Frequency Counter based PWM Generator

topologies. The resulting simulations for 4-bit data input configuration of PWM generation unit for different duty cycle is shown in Fig. After doing Placing and Routing the VHDL code of PWM Generator was downloaded into the Spartan 3E FPGA board and Real time debugging was done for the architecture. The input word K was given by 4 switches present in FPGA board. The clock for the architecture was provided by clock (C9) present in FPGA board. The frequency of the clock was 50 MHz. One LED was assigned to see PWM output. The software ChipScope Pro Analyser was used to see the real timing waveform of PWM output as we change the K value on the FPGA board by different configuration of switches. There was also reset button which can stop the operation of PWM generator.

Figure 9.23: Schematic of Counter based PWM Generator

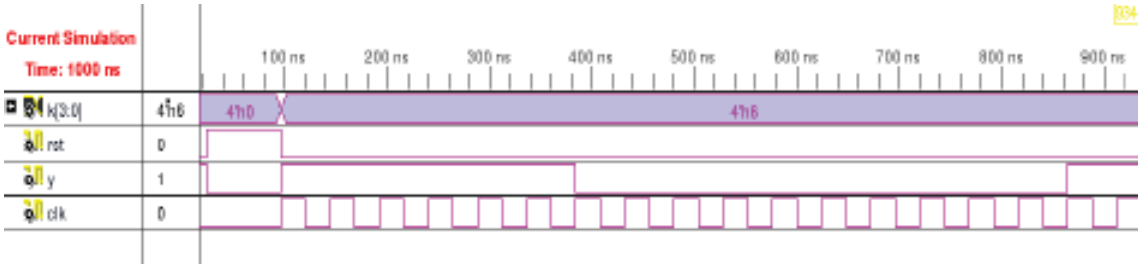

Figure 9.24: For Duty Cycle Of 25 Percentage

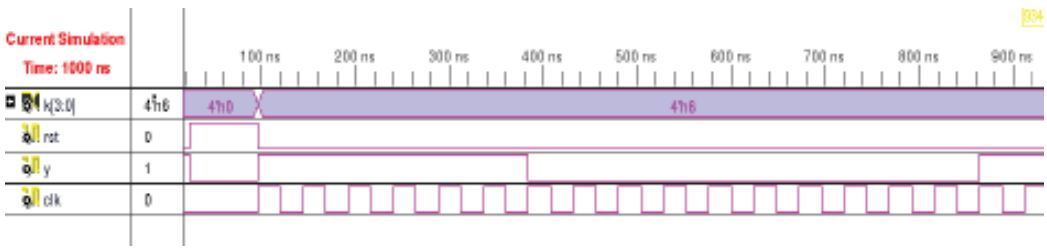

Figure 9.25: For Duty Cycle Of 75 Percentage

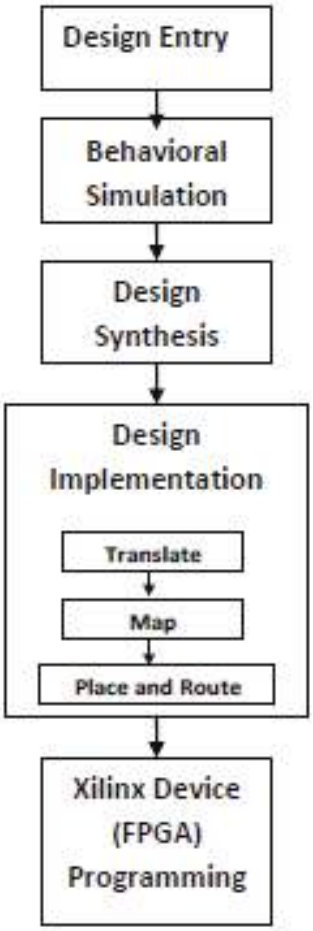

Figure 9.26: Design Flow Of FPGA Controller

Here it is shown that in Fig9.27, the waveforms for the FPGA Output and the triggering circuit have been obtained by controller. In Fig9.28, it shows the waveforms interfacing of the FPGA Controller and ZCD circuit. It shows that how changes in the controller makes the changes in other parameters and waveforms also. In Fig9.29, It shows the voltage across thyristor waveforms at the peak values and at the peak side limit has been given in the FPGA Controller so that any fault occures in the system will either reduce the amplitude of the system or shows zero voltage at the output side in the system, that means that the whole system is being stopped and protection system is being developed. In Fig9.30, it shows that the output voltage

is zero as the protection of the semiconductor and device is concern because of fault occures in the system, at the peak side FPGA will detect the limit and gives feedback to the input side to reduce voltage according to the programming is developed in the controller. And in Fig9.31, It shows that as soon as fault occures in the system than FPGA will sence it and reduce the Amplitude of the system so that the device will get protected. So according to this concept Protection system for the high power inverters using FPGA Controller is being Developed.

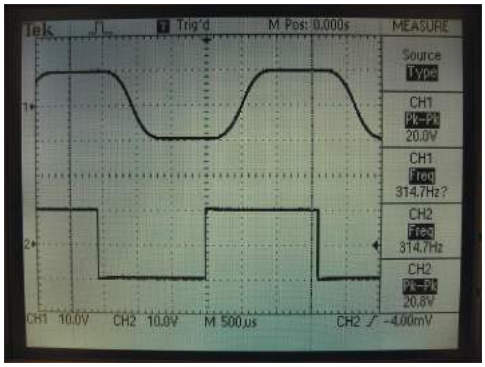

Figure 9.27: Compared waveforms[Scale:X-axis:10ms,Y-axis:5 V/div]

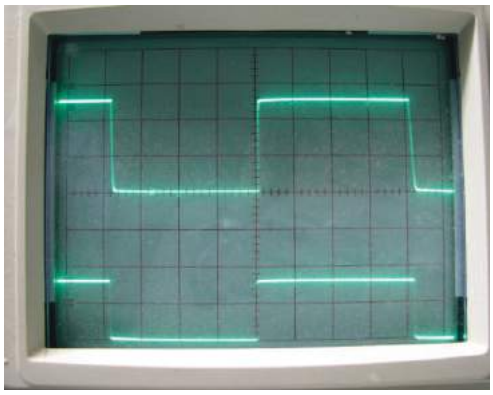

Figure 9.28: ZCD And FPGA Interfacing Waveforms[Scale:X-axis:10ms,Y-axis:5 V/div]

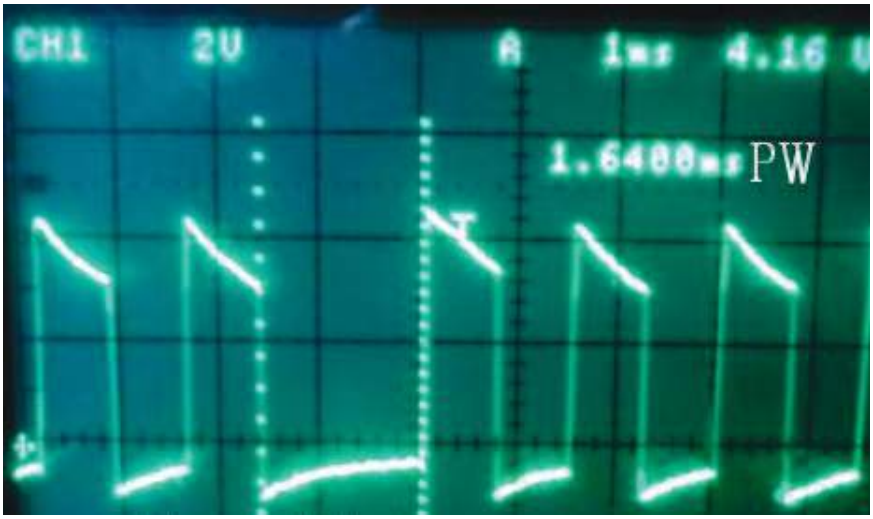

Figure 9.29: Voltage Across Thyristor Waveform for Detection[Scale:X-axis:10ms,Y-axis:5 V/div]

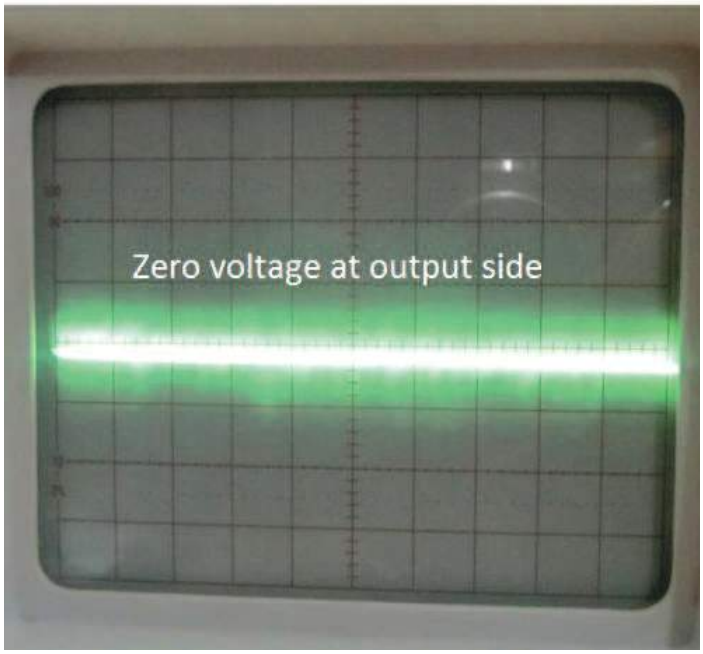

Figure 9.30: Zero Voltage At The Output Side[Scale:X-axis:10ms,Y-axis:5 V/div]

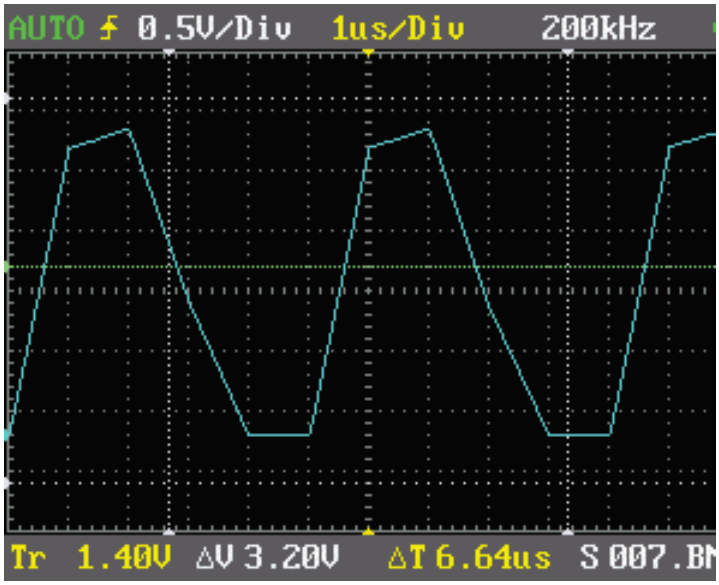

Figure 9.31: Voltage Waveform With Reduced Amplitude

Chapter 10

FUTURE WORK AND CONCLUSION

10.1 Conclusion

Basically from this topic "Protection system for high power inverters", we can conclude that according to the simulation result analysis the protection system for high power is implemented and we can also say that the analysis of hardware is also being implemented for prototype of inverter with controller. The system results which we are getting at the output shows that the system is being protected by the FPGA Controller. Thus the Protection system for the high power inverter is being implemented with FPGA Controller.

10.2 Future Work

In future work we can say that the protection system for high power inverter can be implemented in live panel in industry purposes also for extream high power protection of the inverter using FPGA Controller.

References

[1] SWITCHING BOUNDARY GEOMETRY AND THE CONTROL OF SINGLE-PHASE INVERTERS, IEEE URBANA.

[2] A Large-Capacity GTO Inverter with Low-Loss Snubber Circuits.

[3] N. Kawakami, S. Ueda, Member, IEEE, M. Hombu, Senior Member, IEEE, A. Ueda, Member, IEEE, and Y. Jifuku.

[4] AN IMPROVED CONTROL SCHEME FOR A SERIES CAPACITIVE REACTANCE COMPENSATOR BASED ON A VOLTAGE SOURCE INVERTER.

[5] Bruce S. Rigby Ronald G. Harley, Fellow IEEE.

[6] Frequency Control of a Current-Fed Inverter for Induction Heating.I. Khan, J. Tapson and I. De Vries, Automatic Frequency Control of an Induction Furnace, Proc. IEEE Con, A@icon 99, v01.2, September 1999, pp. 913-916.

[7] D.H.Wolaver, Phase-Locked Loop Circuit Design, New Jersey, Prentice Hall, 1991.

[8] An Effective Control Technique for Medium- Voltage High Power Induction Motor Drives Ge Baoming1, 2 and Fang Zheng Peng2, Fellow, IEEE 1. School of Electrical Engineering, Beijing Jiaotong University, Beijing 100044, China.

[9] Digital-Controlled Single-Phase Transformer-Based Inverter for Non-Linear Load Applications Ming-Shi Huang, Member, IEEE, Po-YiYeh, Student Member, IEEE, U-Ting Yeh, and Meng-Gu Huang.

[10] Protection of High-Voltage Power Supplies (HVPSs) in Single and Multiple HVPS Applications, Ultraviolet manual.

[11] International Journal of Emerging Science and Engineering (IJESE) ISSN: 23196378, Volume-1, Issue-5, March 2013. Design of Snubber Circuit for Thyristors Using Pspice by Nancy Merin Thomas.

[12] A system for inverter protection and real-time monitoring, microelectronics ltd.

[13] Protection system for three phase inverters, International Rectifier Unit.

[14] Power electronics by R.S.Bhimbhara.

[15] Analog devices pvt ltd manuals.

[16] Altera devices pvt ltd manuals.

[17] FPGA Altera development board manuals.