DESIGN AND DEVELOPMENT OF VSC BASED FACTS CONTROLLER

Major Project Report

Submitted in Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY
IN
ELECTRICAL ENGINEERING

(Electrical Power Systems)

By

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May 2014

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I, **Garach Dimple Vinodbhai** , Roll No.**12MEEE11**, give undertaking that the Major Project entitled **"Design and development of VSC based FACTS controller** submitted by me, towards the partial fulfillment of the requirements for the degree of Master of Technology in **Electrical Power Systems** of Nirma University, Ahmedabad, is the original work carried out by me and I give assurance that no attempt of plagiarism has been made. I understand that in the event of any similarity found subsequently with any published work or any dissertation work elsewhere; it will result in severe disciplinary action.

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This is to certify that the Major Project Report entitled **Design and development of VSC based FACTS controller** submitted by **Ms. Dimple V. Garach (12MEEE11)** towards the partial fulfillment of the requirements for the award of degree in Master of Technology (Electrical Engineering) in the field of Electrical Power Systems of Nirma University is the record of work carried out by her under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this major project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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Acknowledgement

The work presented in this thesis was carried out under the supervision of Prof. Chanakya B. Bhatt, Nirma University, Institute of Engineering and Technology, Ahmedabad. I wish to thank Prof. Chanakya B. Bhatt for his valuable and inspiring guidance. I would also like to thank Dr. P. N. Tekwani, Head of Electrical Engineering Department for providing the infrastructure to carry out the project work in the campus. I express my sincere appreciation and thanks to Dr. S.C. Vora for constant encouragement and needful help during various stages of work. I am also thankful to Nirma University for providing all kind of required resources. I would like to thank my family and friends for their continuous support and encouragement.

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Abstract

A transmission line needs controllable compensation for power flow control and voltage regulation. Initially passive compensator were used for this and now semiconductor based converter topologies have replaced them. This can be achieved by different types of FACTS controllers. In particular, the emphasis is on series connected VSC into transmission line known as Static Synchronous Series Compensator (SSSC) which is capable of providing reactive power compensation to a power system.

SSSC topology has been simulated using simulation tool and various performance parameters has been evaluated. Verified simulated results, used to develop a prototype model of SSSC. This system is based on 6-pulse VSC converter which is connected in series with transmission line via grid connected transformer. Controlling technique developed has been used to evaluate and control various conditions like power enhancement, voltage control. Prototype model performance has been evaluated. This model involves the three phase inverter operation at low and high voltages.

ABBREVIATIONS

FACTS .... Flexible AC Transmission System
PLL .... Phase Lock Loop
PWM .... Pulse Width Modulation
SPWM .... Sinusoidal Pulse Width Modulation
SSSC .... Static Synchronous Series Compensator
TCSC .... Thyristor Controlled Series Capacitor
VSC .... Voltage Source Converter

NOMENCLATURE

Active power .... P_q
Dc offset angle .... β
DC-to-AC gain .... K_{inv}
Direct axis current component .... i_d
Direct axis voltage component .... V_d
Injected Voltage .... V_q
Maximum injected SSSC voltage .... V_{qmax}
Maximum transmission line current .... $I_{linemax}$
Output current angle .... θ_i
Output voltage angle .... θ_v
Phase angle .... δ
Phase currents .... I_a, I_b, I_c
Phase voltages .... V_a, V_b, V_c
Quadrature axis current component .... i_q
Quadrature axis voltage component .... V_q
Quadrature/ compensating reactance .... X_q
Reactive power .... Q_q

Receiving end voltage .... V_r

Reference angle .... θ

Reference current angle .... θ_{ir}

Sending end voltage .... V_s

Sinusoidal voltage/Reference voltage wave .... $v_{control}$

Stationary reference frame voltages .... V_α, V_β Transmission line drop .... V_L

Transmission line reactance .... X_L

Triangular voltage .... v_{tri}

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Chapter 1

Introduction

1.1 Real Power Management

In recent years, greater demands have been placed on the transmission network, which will continue to increase because of the increasing number of non- utility generators, this is the problem that it is very difficult to acquire new rights of way. Increased demands on transmission have reduced quality of supply. Attempts should be made to transmit only active power as far as possible over the high voltage transmission lines and the required reactive power should be generated locally by different means. Extracting the highest possible power transmission capacity on any given line is a high priority for any transmission system. Also, higher power loads are made possible by developing new control devices. For solving this problem a simple system is considered. A schematic diagram of a simple power transmission line, represented by its inductive reactance, connecting a sending-end voltage source and a receiving end voltage source is depicted in Figure 1.1.

The voltage magnitudes at the two ends are chosen to be nearly equal and the phase difference between the two ends is defined as the load angle. The active and reactive power flow on a line between two ends (which can be in either direction) is a function of the magnitudes of the voltage at both ends, the line impedance and the

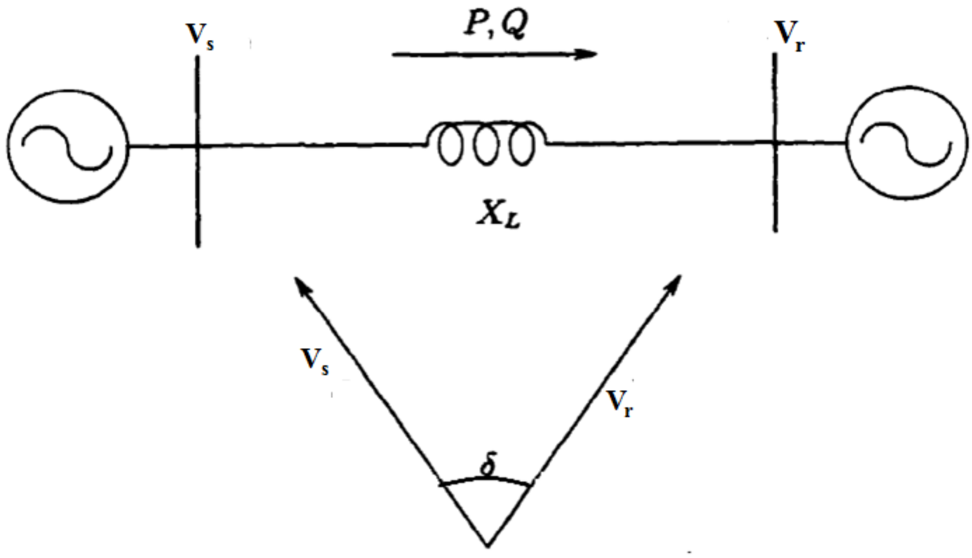

Figure 1.1: Elementary power transmission system

load angle, followed by equation:

$$\begin{aligned} P &= \frac{V_s V_r}{X_L} \sin(\delta_s - \delta_r) \\ &= \frac{V^2}{X_L} \sin\delta. \end{aligned} \tag{1.1}$$

$$\begin{aligned} Q &= \frac{V_s V_r}{X_L} (1 - \cos(\delta_s - \delta_r)) \\ &= \frac{V^2}{X_L} (1 - \cos\delta). \end{aligned} \tag{1.2}$$

where V_s, and V_r are the magnitudes of the voltage at the two ends $|V_s| = |V_r| = |V|$, X_L is the line impedance (assumed purely inductive) and δ = (δ_s - δ_r) is the load angle. Generally, the transmitted power can be controlled by varying the voltages, impedance and load angle. When the power transfer requirement for a given length of line increases, higher transmission voltages (V_s,V_r) must be selected. However, since power networks operate as voltage sources, it is desirable to hold the node voltages at near rated values. Therefore, the active power can be influenced mainly by phase shifters (acting only upon δ) or by means of changing the line impedance.

1.2 Need of Series Compensation

The series compensator is primarily applied to solve the power flow problem. There are two main causes for the problems associated with power flow. First, the power flow problem may be related to the length of the line. This maybe compensated to meet the transmission requirements by a fixed capacitor or inductor. Second, the power flow problem may be related to the structure of the transmission network. Network related problems typically result in power flow unbalance. There is a phenomenon called inadvertent interchange in a power system. Inadvertent interchange occurs when the power system tie-line schedule becomes corrupted. In other words, there is an unexpected change in load on a distribution feeder that causes the demand for power on that feeder to increase or decrease. If this occurs generators need to be turned on or off to compensate for the change in load. If the generators are not activated quickly enough, voltage sags or surges can occur. Network related problems might require controlled series compensation particularly if contingency or planned network changes are anticipated.

Series compensation, if correctly controlled, can provide a significant improvement in transient stability for post-fault systems and can be very effective in damping power oscillations. There are two ways in which series compensation can be accomplished. Series compensation is accomplished either using a **variable impedance-type series compensator** or using **a switching converter-type series compensator**.

The following table shows the comparison of Static Synchronous Series Compensator(SSSC)and Thyristor Controlled Series Capacitor(TCSC).

Difference	SSSC	TCSC
Working Principle	- Voltage source converter type compensator - Injects the voltage that lags or leads the line current by 90° - The injected voltage can be dependent or independent	- Variable impedance type compensator - By varying the firing angle of thyristor the effective impedance can be varied - The voltage across the capacitor is a function of line current
Operating region	- Wide operating region from inductive to capacitive compen -sation and vice versa	- Prohibited region between the inductive and capacitive compensation because of internal resonance
Switching devices	- Devices has capability to turn on and off	- No turn off capability
Interface with external dc source	- Has the ability to interface	- No interface.
Coupling method	- It is coupled to the transmission line via transformer	- Directly coupled to the transmission line

Table 1.1: Comparison of SSSC and TCSC

1.3 Objective of Dissertation

The scope of this thesis is to examine the use of a Static Synchronous Series Compensator(SSSC) in an electrical power transmission line for real power control under various operating conditions.

- The performance of the SSSC is evaluated for providing series compensation in a power system comprising a long transmission line fed by two infinite buses at the ends.

- The system will be based on 6-pulse VSC converter which will be connected in series with transmission line via grid connected transformer.

- Verified simulated results will be used to develop a prototype model of SSSC.

1.4 Literature Survey

- **N. G. Hingorani and L. Gyugyi," Understanding FACTS : Concepts and technology of flexible AC transmission systems" [3] and K.K.Sen, "SSSC-static synchronous series compensator: theory, modelling and applications"**
  It gives the information about all series type facts controller design and the basic defination, which define that how the series facts controller differ from the shunt controller for the compensation of reactive power. Sen et.al[4] describes the theory and the modelling technique of a FACTS device, namely, Static Synchronous Series Compensator (SSSC) using an Electromagnetic Transient Program (EMTP) simulation package. This paper helps understanding the control strategy of SSSC. Also its book regarding FACTS controller designing gives wide idea about the designing.

- **A. H. Norouzi and A. M. Sharaf, "Two control schemes to enhance the dynamic performance of the STATCOM and SSSC"**[7]
  It describes the dynamic performance of the static synchronous series compensator(SSSC). The proposed control scheme based on the effect of PLL on the dynamic performance of SSSC. The control scheme basically made with reference to the line cuurent and accordingly the gate pattern is generated. Simulation contains 48-pulse GTO voltage source converter of STATCOM and SSSC FACTS devices.

- **Anil C. Pradhan and P.W. Lehn, "Frequency Domain Analysis of the Static Synchronous Series Compensator"**[8]
  It presents an analytical formulation of the frequency domain characteristics of the Static Synchronous Series Compensator (SSSC). The paper investigates the characteristics using two different types of SSSC schemes- one with quadrature voltage regulation (V_q controlled SSSC) and another with impedance regula-

tion (X_q controlled SSSC). The influence of the controller parameters on the characteristics is investigated.

- **"FACTS CONTROLLERS IN POWER TRANSMISSION AND DISTRIBUTION" by K.R.Padiyar**[5]
  It covers the basics of the modelling. This help in designing the different controllers in appropriate manner. The book also serves as quick reference for the modelling purpose.

- **Sasan Salem and V.K.Sood ,"Modeling of SSSC with EMTP RV"**[11]
  It describe about the modelling of SSSC with the two different modes of operation i.e direct and indirect controller. Here, the synchronisation is made based on RWG(Reference Wave Generator) where it contains symmetrical components transformation. Based on that stability of the proposed SSSC under various system condition is then investigated.

- **Nitus Voraphonpiput, Teratam Bunyagul, and Somchai Chatratana, "Power Flow Control with Static Synchronous Series Compensator (SSSC)"**
  [1]Paper helps in developing the prototype model and its implementation into the system.[6] It proposes two control schemes for the power flow control. The first scheme, which is called Reactance Emulation Scheme, the SSSC performs a function of the series impedance connected to the transmission line. This performance can be achieved by controlling the quadrature voltage of the SSSC in relation to the transmission line current and, the required series impedance compensation. The second control scheme, which is called Quadrature Voltage Control Scheme, the SSSC injects a quadrature voltage into the transmission line.

- **S.K.Sethy, J.K.Moharana,"Design, Analysis and Simulation of Linear Model of a STATCOM for Reactive Power Compensation with Variation of DC-link Voltage"**[10]

  The paper describes the linear modeling of STATCOM along with design of current and voltage controllers. Also the designed controllers with variation of DC-link voltage have been applied to the STATCOM and suitable DC link voltage has been selected on basis of responses i.e spike and over shoot. They have designed the system parameters on basis of selected DC-link voltage used for the design and fabrication of a STATCOM and based on it respective calculation is made. They have developed a simulink model by developing the control strategy.

- **Se-Kyo Chung,"A Phase Tracking System for Three Phase Utility Interface Inverters"**[2]

  Paper describes about the analysis and design of the phase-locked loop (PLL) system for the phase tracking system of the three phase utility interface inverters. The dynamic behavior of the closed loop PLL system is investigated in both continuous and discrete-time domains. In particular, the performance of the three phase PLL system is analyzed in the distorted utility conditions such as the phase unbalancing, harmonics, and offset caused by the nonlinear load conditions and measurement errors. The tracking errors under these distorted utility conditions are also derived.

1.5 Thesis Organization

Chapter1: Provides the introduction to the real power management, need of series compensation, comparison of SSSC and TCSC and the literature survey regarding the SSSC operation.

Chapter2: This chapter focus on the basic working of Voltage Source Converter(VSC) and Pulse Width Modulation(PWM)technique.

Chapter3: It focus on the working of the Static Synchronous Series Compensator(SSSC). The detailed working of control scheme is explained.

Chapter4: It covers the simulation of SSSC operation at steady state condition. The simulation implemented is for high voltage applications. The control scheme implemented the same as that explained in chapter3.

Chapter5: It involves the prototype model simulation of the same covered in chapter4 and description of hardware. Hardware involves mainly the operation of three phase inverter.

Chapter6: It incorporates the conclusion and future work involved.

Chapter 2

Voltage Source Converter

2.1 Introduction

Voltage source converter generates AC voltage from a DC voltage. It is, often referred to as an inverter, even though it has the capability to transfer power in either direction. The magnitude, phase angle and the frequency of the output voltage can be controlled with this type of converter.

2.2 Operating Principle

The three-phase VSC, shown in figure 2.1 configure for FACTS application, is a two-level bridge composed of six switches. Each switches is made of semiconductor turn-off capable switches and an antiparallel diode. The switches should be designed only for forward blocking voltage, as the diodes serve the purpose that the voltage polarity of each switch is unidirectional.

Figure 2.2 shows the output waveforms of three phase VSC operation. Considering the period of 2π radians, each switches is triggered in sequence after an interval of $\pi/3$. In the commutating pattern, three switches conduct at a time and by identifying them one can easily obtained the line voltage waveform, for example here the waveform shown for V_{ab}, and the other two similar waveforms will be displaced by 120° in time.

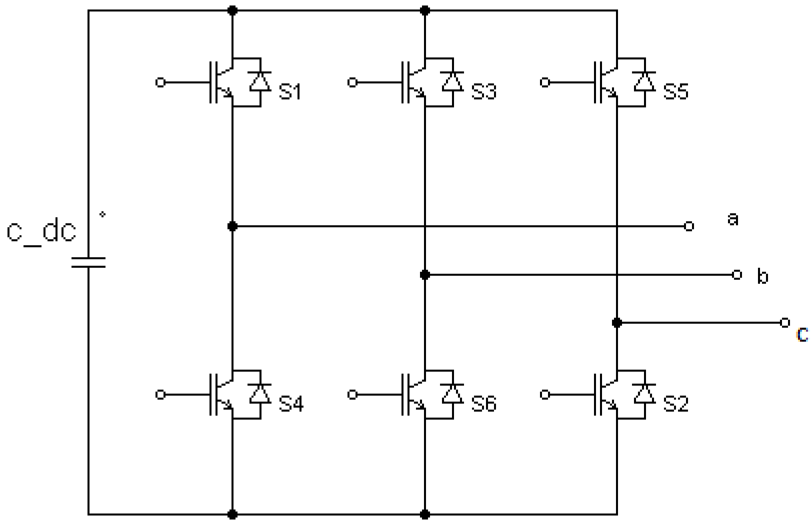

Figure 2.1: Three phase, two level VSC circuit

Equations (2.1) to (2.3) show that the line voltages have values defined by the intervals of conduction and they do not depend on the type of load. Therefore, any linear, balanced or unbalanced load, or even any combination of resistance, inductance and capacitance is possible to be connected at the output terminals. Also, the equations (2.1) to (2.3) show that the triple harmonies are not present in the line voltages. The phase voltage has been drawn for a resistive load connected in a star configuration at the output terminals. Thus, for the first three intervals, the phase voltage V_a equals in sequence $\frac{V}{3}$, $\frac{2V}{3}$ and again $\frac{V}{3}$, following the same shape in the negative cycle as well ($-\frac{V}{3}$, -$\frac{2V}{3}$ and -$\frac{V}{3}$).

$$V_{ab} = \sum_{n=1,3,5....}^{\infty} \frac{4V}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t + \frac{\pi}{6}) \tag{2.1}$$

$$V_{bc} = \sum_{n=1,3,5....}^{\infty} \frac{4V}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t - \frac{\pi}{2}) \tag{2.2}$$

$$V_{ca} = \sum_{n=1,3,5....}^{\infty} \frac{4V}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t - \frac{\pi}{6}) \tag{2.3}$$

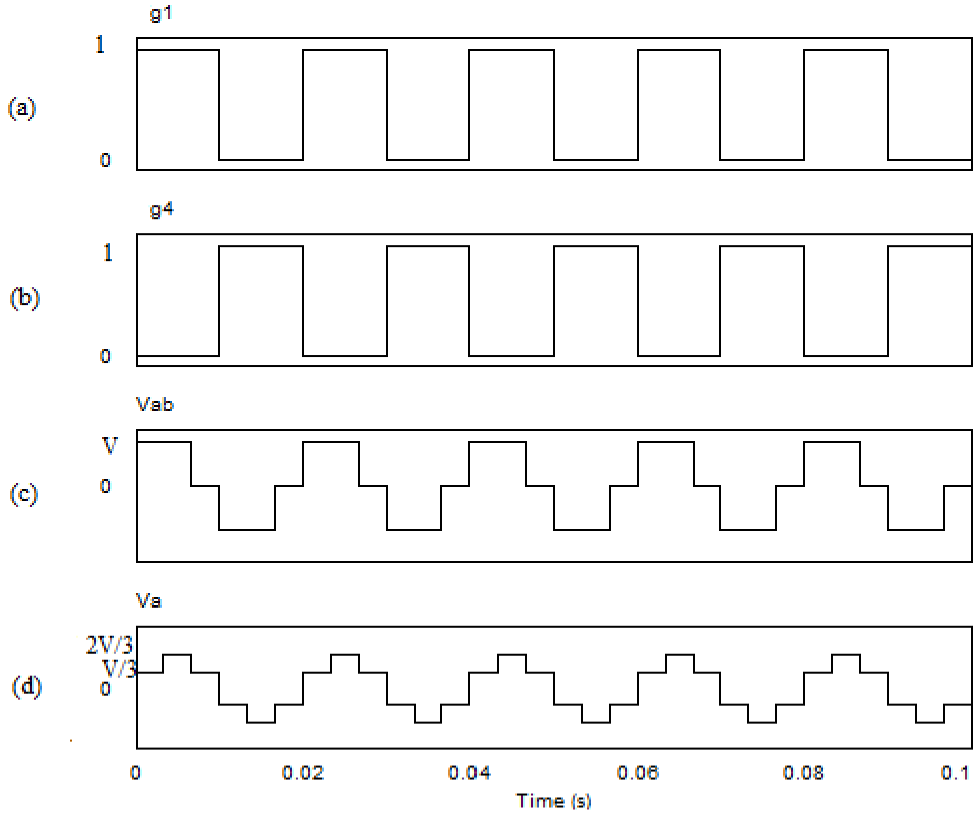

Figure 2.2: Waveforms of three phase bridge inverter:(a) & (b) gate pulses, (c)Phase voltage,V_a, (d)Line-to-line voltage,V_{ab}

For FACTS application, it is always assumed that the output voltage waveform has a fixed frequency equal to the fundamental frequency of a power system to which the converter is connected, as high voltage and power harmonics could create many problems.

On the other hand, keeping the input DC voltage fixed and varying the gain of the converter output voltage can be control. This type of control of the output voltage magnitude is normally accomplished by Pulse-Width-Modulation (PWM) control; the converter gain in this case is defined as the ratio of the ac output voltage to the DC input voltage. There are various schemes to pulse-width-modulate the converter switches in order to shape the output AC voltage to be as close to a sine wave as possible.

2.3 Pulse Width Modulation (PWM)

The main advantage of PWM converters is the possibility of controlling the converter gain and consequently the converter output voltage. In the most popular PWM method, the width of each pulse is varied in proportion to the amplitude of a **sine wave** or control waveform.

Fig 2.3(a) shows the waveform where sine($V_{control}$) is compared with triangular(V_{tri}) and its output voltage obtained is shown in fig 2.3(b). This waveform shown here is for the single phase arrangement.

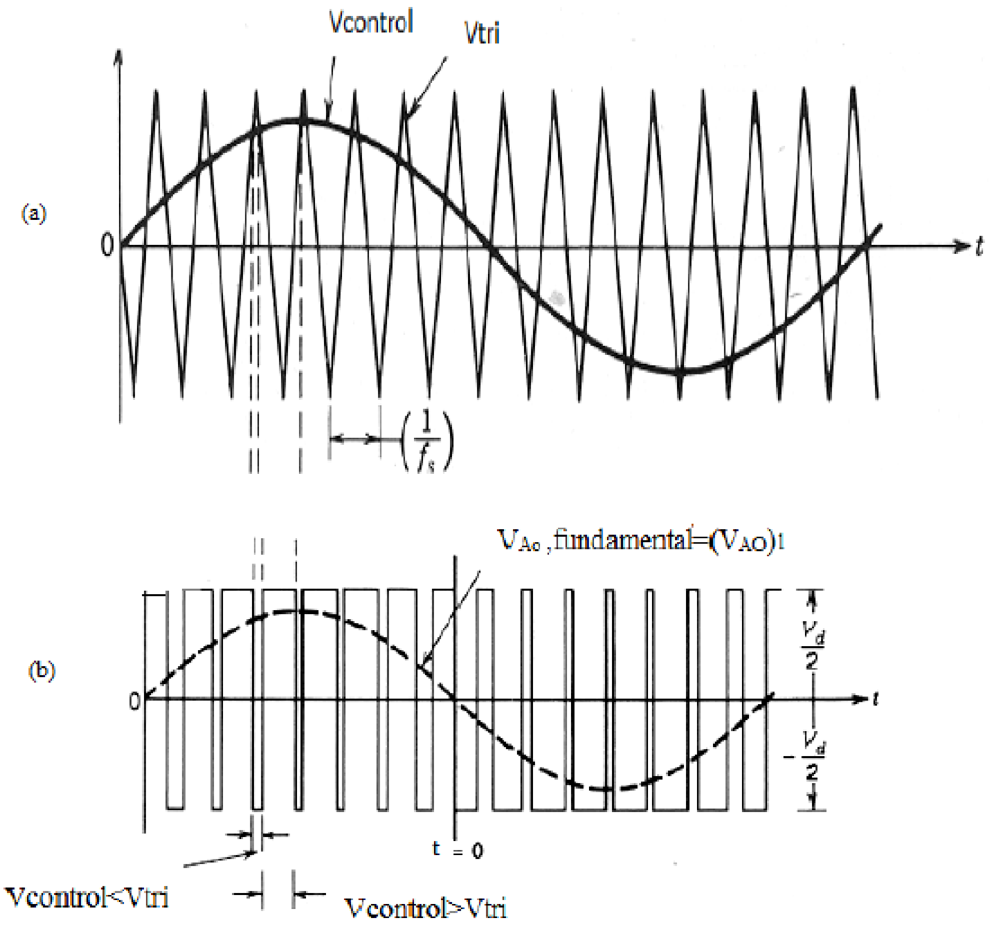

Figure 2.3: (a)Sine-Triangular comparison (b)PWM output

For three-phase SPWM, a triangular voltage waveform (V_{tri}) is compared with three sinusoidal control voltages (V_a, V_b, and V_c), which are 120° out of phase with each other and the relative levels of the waveforms are used to control the switching of the devices in each phase leg of the inverter.

A six-step inverter is composed of six switches S_1 through S_6 with each phase output connected to the middle of each inverter leg as shown in figure 2.1. Two switches in each phase make up one leg and open and close in a complementary fashion.

The peak of the sine modulating waveform is always less than the peak of the triangle carrier voltage waveform. When the sinusoidal waveform is greater than the triangular waveform, the upper switch is turned on and the lower switch is turned off. Similarly, when the sinusoidal waveform is less than the triangular waveform, the upper switch is OFF and the lower switch is ON. Depending on the switching states, either the positive or negative half DC bus voltage is applied to each phase. The switches are controlled in pairs ((S_1;S_4), (S_3;S_6), and (S_5;S_2)) and the logic for the switch control signals is:

- S_1 is ON when $V_a > V_{tri}$ and S_4 is ON when $V_a < V_{tri}$
- S_3 is ON when $V_b > V_{tri}$ and S_6 is ON when $V_b < V_{tri}$
- S_5 is ON when $V_c > V_{tri}$ and S_2 is ON when $V_c < V_{tri}$

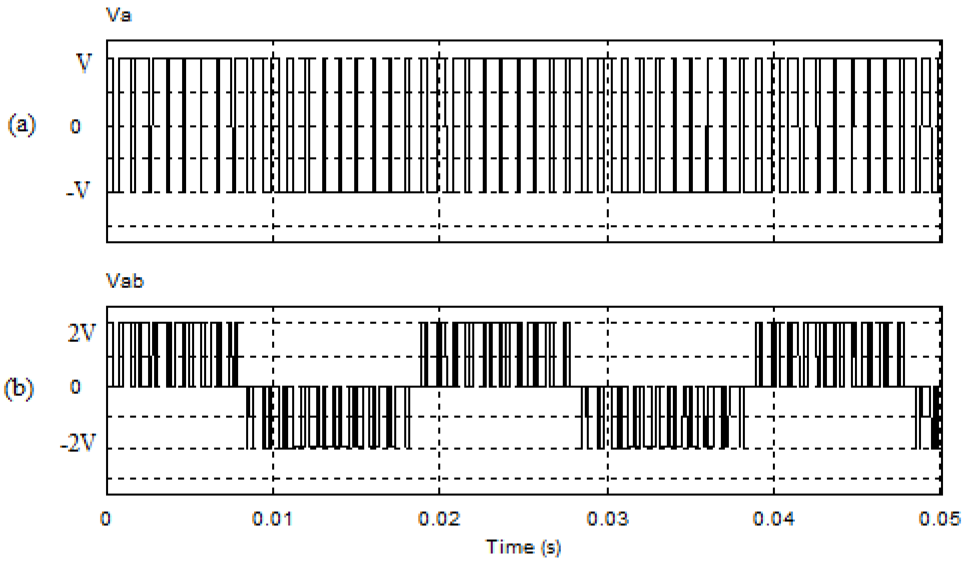

Figure 2.4: PWM output for three phase:(a)a-phase voltage,(b)line-to-line voltage,V_{ab}

The output voltage waveform is shown in figure 2.4 where the switching takes place as per the above logic. Thus here the output voltage is differed from the voltage shown in the figure 2.2.

Chapter 3

Static Synchronous Series Compensator

3.1 Power Circuit of SSSC

Figure 3.1 shows a single line diagram representation of SSSC in an AC transmission system[4]. The transmission system includes a sending end voltage source, V_s and receiving end voltage source, V_r. The SSSC comprises of a voltage source inverter and coupling transformer that is used to insert the ac output voltage of the inverter in series with transmission line.

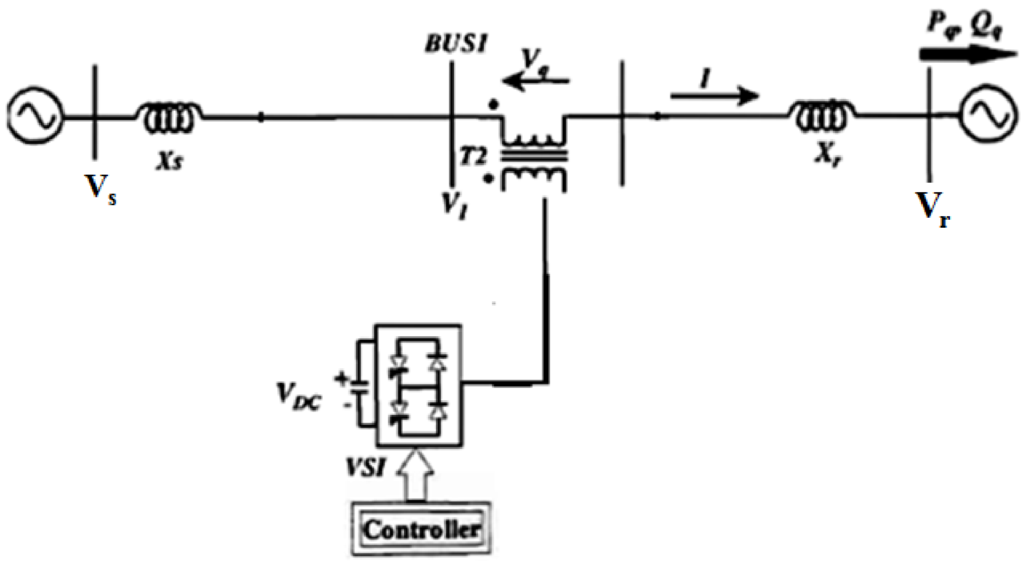

Figure 3.1: Single line diagram of SSSC

3.2 Operating Principle of SSSC

Basically, SSSC generates a sinusoidal voltage, with controllable amplitude in nearly quadrature with line current. Consequently, the injected voltage emulates either a capacitive or an inductive reactance in series with the transmission line that increases or decreases the total transmission line reactance. As a result, the power flow will change in the line. Hence, the SSSC is a powerful device to control transmission line current.

In fact, power exchange is controlled by the magnitude of the injected voltage to the transmission line, and angle control is used to regulate the active power exchange. The inductive and capacitive mode of operation is set by the injected voltage phase angle with respect to the transmission line current. When the injected voltage is leading the line current, reactive power is absorbed and the SSSC operates in inductive mode; in capacitive mode injected voltage is lagging the line current and injects reactive power into the transmission line. The representation of the operation is shown in figure 3.2

Theoretically, the SSSC voltage phasor can operate in all four quadrants, by setting the phase angle of the SSSC output voltage V_q with respect to the transmission line current. However, there are some practical limitations in power systems, i.e voltage range in the receiving end which must be kept between 0.95 p.u. to 1.05 p.u. and the magnitude of injected voltage , if SSSC in capacitive mode must be less than the voltage drop across the transmission line $V_q < V_L$, else the power flow in the line will be reversed and that is not desired.

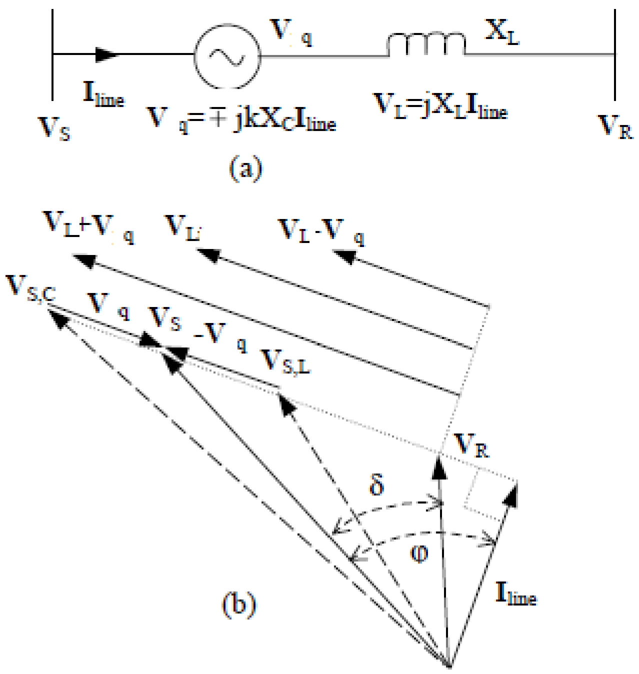

Figure 3.2: (a) Single line representation (b) Capacitive and inductive mode of operation

The SSSC output current corresponds to the transmission line current, which is affected by power system impedance, loading and voltage profile, as well as by the actions of the SSSC. Thus, the relationship between the SSSC and the line current is complex. The fundamental component of the SSSC output voltage magnitude is, on the other hand, directly related to the DC voltage that is either constant or kept within certain limits, depending on the chosen design and control of the SSSC.

The active and reactive power exchanged between the SSSC and the transmission line can be calculated as follows:

$$\begin{aligned} P_q &= V_q I_{line} \cos\varphi \\ &= \frac{V_s V_r}{X_L - X_q} \sin\delta. \end{aligned} \tag{3.1}$$

$$\begin{aligned} Q_q &= V_q I_{line} \sin\varphi \\ &= \frac{V_s V_r}{X_L - X_q} (1 - \cos\delta). \end{aligned} \tag{3.2}$$

3.3 Rating of SSSC

The SSSC ratings and, therefore, the amount of the real and reactive power that can be exchanged with the power system, are determined by ratings of its components, namely, the dc capacitor VSC, and the series connected coupling transformer. The SSSC volt-ampere rating of the series coupling transformer is determined by a product of the maximum injected SSSC voltage and the maximum transmission line current, i.e MVA $= I_{linemax} V_{qmax}$.

3.4 SSSC Controller

The three control requirements of an SSSC can be described as follows:

1. Phase Angle Control: The compensating voltage vector V_q, injected in series with the transmission line by an SSSC must lag the line current vector I by 90°, if the SSSC is operated in the capacitive mode; V_q must lead I by 90° in the inductive mode of operation.

2. Magnitude Control: The magnitude of the compensating voltage vector must be proportional to the magnitude of the line current vector.

$$V_q = kIe^{-j\pi/2} \tag{3.3}$$

3. DC Voltage Regulator: The DC voltage on the inverter's storage capacitor (i.e. the inverter's voltage source) must be regulated to the required value by shifting a small component of the compensating voltage vector in phase with the line current vector in order to replenish the losses in the inverter. However, this third requirement only applies to a stand-alone SSSC, where there is no auxiliary source to supply the DC side of the inverter.

Figure 3.3 shows control block diagram of a two-level inverter-based SSSC[4, 8]. It is dissected into three corresponding sub-sections, namely, angle control, magnitude control and DC voltage regulator. The SSSC injects a voltage that is a function of the line current (constant reactance mode) or independent of the current (constant quadarture voltage mode). The following section contain detail description of different blocks.

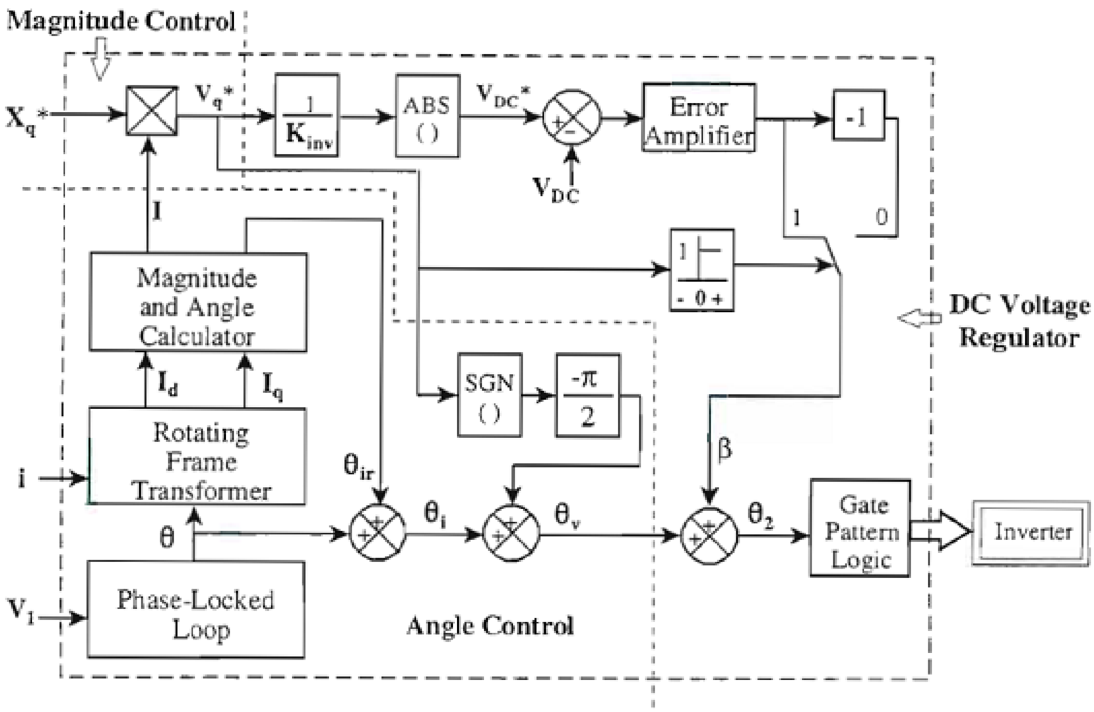

Figure 3.3: Control block diagram

3.4.1 Phase lock loop

The basic configuration of the PLL system is shown in figure 3.4. The phase voltages V_a, V_b, V_c, are obtained from sampled line to line voltages. These stationary reference frame voltages are transformed to voltages V_α, V_β and then voltages are transformed to V_d, V_q rotating reference frame. The angle θ used in these transformations is obtained by integrating a frequency command ω, in other words, by synchronizing the PLL rotating reference frame and the voltage vector.

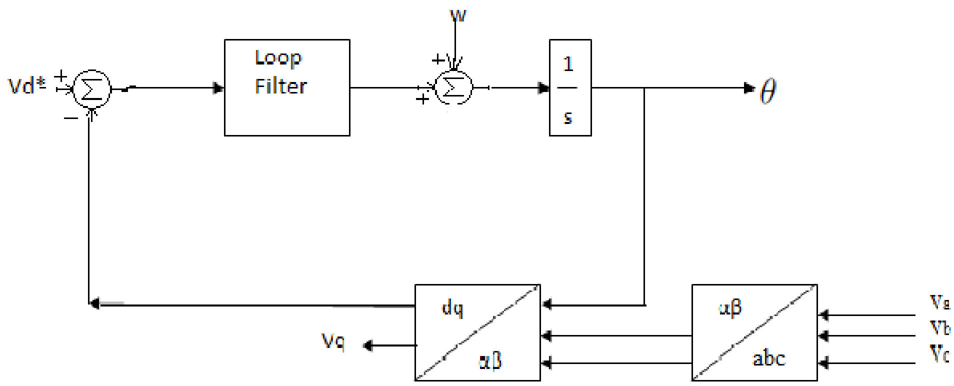

Figure 3.4: Block diagram of PLL

In the given method, a PI regulator is used to obtain the value of θ which drives the feedback voltage V_d to a commanded value V_d^*. In other words, the regulator results in a rotating frame of reference with respect to which the transformed voltage V_d, has the desired DC value V_d^*. The frequency of rotation of this reference frame is identical to the frequency of the utility voltage.

Figure 3.5 shows the three-phase system voltage and the phase angle of system voltage from PLL.

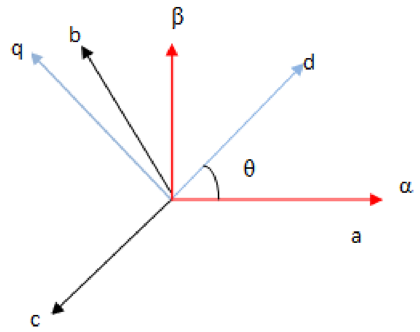

Figure 3.5: Vector representation of PLL

For implementing here, firstly the instantaneous voltages v_a, v_b and v_c at the SSSC bus (bus 1 in Figure 3.1) are sensed. These instantaneous a, b, and c voltages are converted to stationary frame i.e α-β form using the following equation:

$$V_\alpha = \frac{2}{3}(v_a - \frac{1}{2}v_b - \frac{1}{2}v_c) \tag{3.4}$$

$$V_\beta = \frac{2}{3}(\frac{\sqrt{3}}{2}v_b - \frac{\sqrt{3}}{2}v_c) \tag{3.5}$$

It is desirable to find the components of v in a d-q co-ordinate frame which

- rotates at exactly the system frequency (i.e. synchronously rotating) and;
- is positioned such that there is no component of the voltage vector,v along its q-axis

The main aim of finding such a co-ordinate frame is: firstly, the line current vector will always appear stationary in such a frame; secondly, the d-axis component of line current in such a frame is, by definition, the real (active) component of line current while the q-axis component of the line current in such a frame is, the reactive component of line current.

Now, the synchronous reference frame d-q component can be represented in terms of stationary frame, α-β as:

$$V_d = V_\alpha \cos\theta + V_\beta \sin\theta \tag{3.6}$$

$$V_q = V_\beta \cos\theta - V_\alpha \sin\theta \tag{3.7}$$

Equations (3.4) and (3.5) have shown how V_d and V_q can be obtained from V_α and V_β if the correct transformation angle θ is known at every instant. In practice, the angle θ in the SSSC controls is obtained from the output of a phase locked loop. If the angle θ output by this PLL is incorrect, then the components V_d and V_q of vector V in the synchronous co-ordinate frame will also be incorrect; in particular the component V_q will not be zero.

3.4.2 Line current frame

Figure 3.6 shows the detail diagram of the control scheme. Here now, with the correct value of θ obtained from the above-mentioned phase locked loop, this angle and the same set of transforms is used to calculate the magnitude and the angle of the transmission line current.

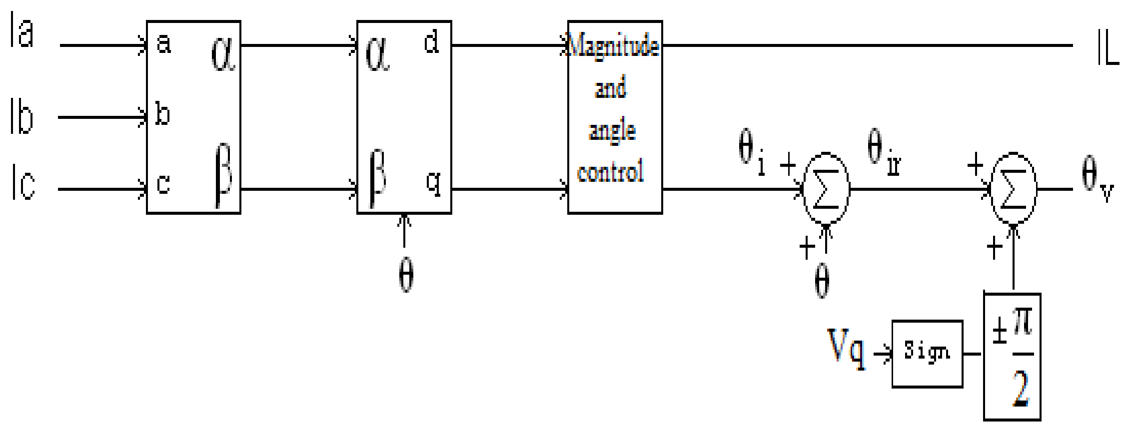

Figure 3.6: Detailed diagram of control scheme

From i_d and i_q, the magnitude of the transmission line current vector and the angle

θ_{ir} of this current vector relative to the synchronously rotating coordinate frame can be calculated. Using this angle subsequently the actual angle, θ_i of the line current vector in stationary coordinates, measured from the position of a space vector that lies along the phase a axis at time t =0, i.e $\theta_i = \theta + \theta_{ir}$.

Now the required angle θ_v of a voltage vector to be injected in series with the line is obtained such that this voltage vector will be exactly 90° ahead of or behind the line current vector, i.e $\theta_v = \theta_i \pm 90°$,where the positive or the negative sign is decided by which mode (capacitive or inductive) the SSSC is required to operate in.

3.4.3 Amplitude of compensating voltage

The second requirement of the SSSC controller is such that the amplitude of the AC compensating voltage V_q required from the SSSC's inverter is determined by multiplying the magnitude of the line current vector I (as determined in the previous section) by the compensating reactance demand X_q, i.e. $V_q =$ I X_q.

Also, the required sign of V_q is determined from the sign of the compensating reactance demand, i.e. at the input to the SSSC controls, X_q is positive if the SSSC is to emulate a capacitive reactance and negative if the SSSC is to emulate an inductive reactance.

3.4.4 Inverter DC voltage regulator

The SSSC controller considered here, have a fixed DC-to-AC gain across the inverter, so the demanded value of AC voltage V_q determines (after accounting for the inverter's constant DC-to-AC gain K_{inv}) the demanded inverter DC voltage V_{dc}^* sent to the input of the voltage regulator.

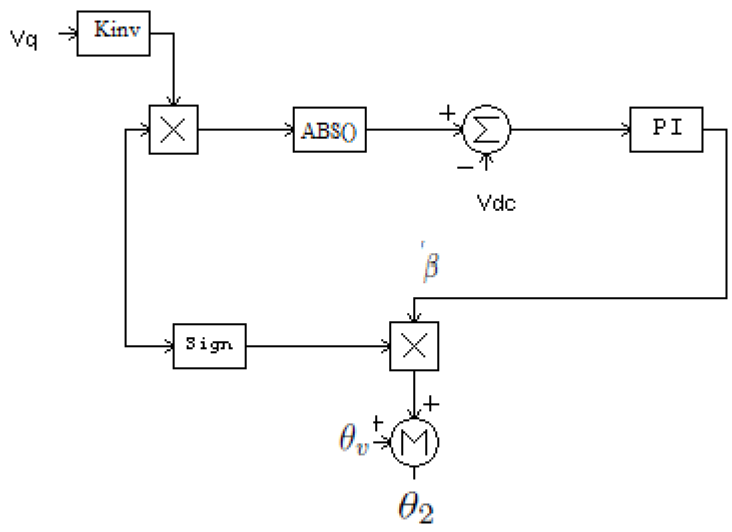

Figure 3.7: Detailed diagram of DC voltage regulator

Detailed diagram of the DC voltage regulator (sub-section of the SSSC controller in figure 3.3) now shown in figure 3.7. In Figure 3.7 the demanded value is compared to the actual DC voltage V_{dc} and the error is used to drive a PI controller. The output from this PI controller determines the angular phase offset applied to the injected AC voltage V_q (away from quadrature). However the sign of the angle required to generate the required active power at the ac terminals of the SSSC depends on the mode of operation (capacitive or inductive) of the SSSC. Thus the sign is altered according to the sign of X_q (which is positive for capacitive mode and negative for inductive mode).

Chapter 4

Simulation and Results

Given data:-

$V_s = V_r$ =138 kV

$\delta = 30°$

frequency, $f = 50$ Hz

Source resistance, $R_s = 1.0053\ \Omega$

Source reactance, $X_s = 7.438\ \Omega$

Transmission line resistance, R_r and reactance,X_r are 3 Ω and 22.316 Ω respectively.

Here, also assumed that the system have X/R ratio to be 7.4.

The voltage source converter uses PWM switching techniques, mainly SPWM to ensure fast response and to generate a sinusoidal wave form.

Figure 4.1 and 4.2 shows the sending end and receiving end voltages having phase difference of 30° and system MVA and its power factor.

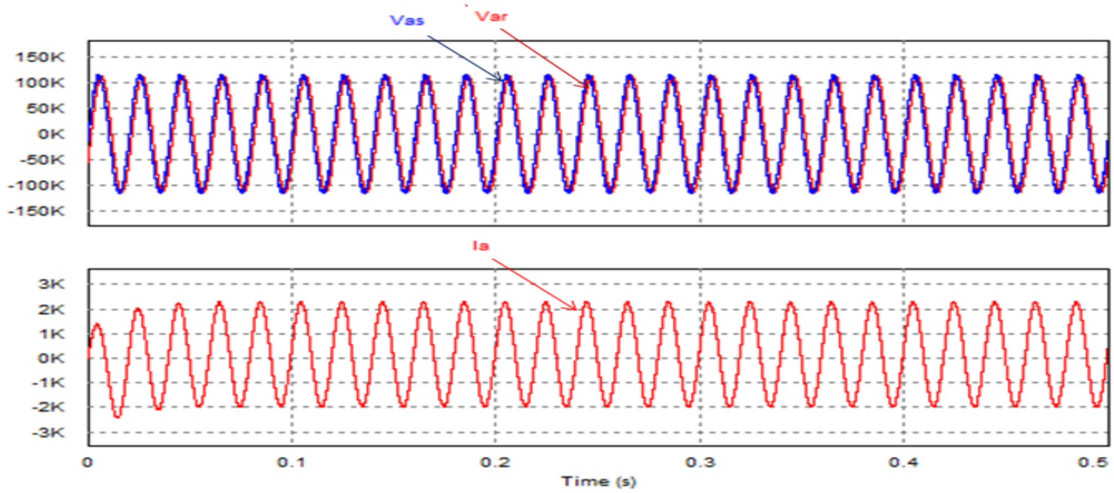

Figure 4.1: Sending and Receiving end voltage and current of the system for phase-a

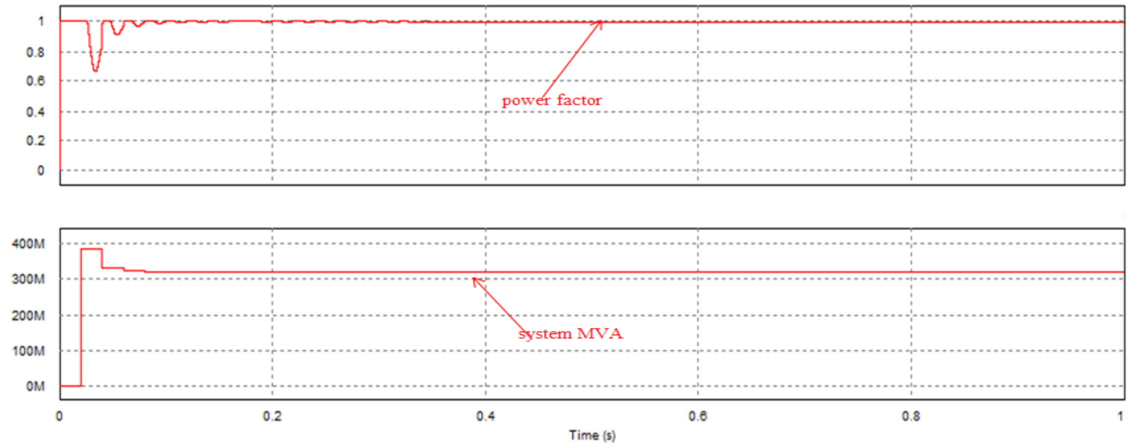

Figure 4.2: power factor and MVA

Figure 4.3 shows the system when it is connected to the system, where, DC voltage is considered to be 40 kV and switching frequency to be 900 Hz.

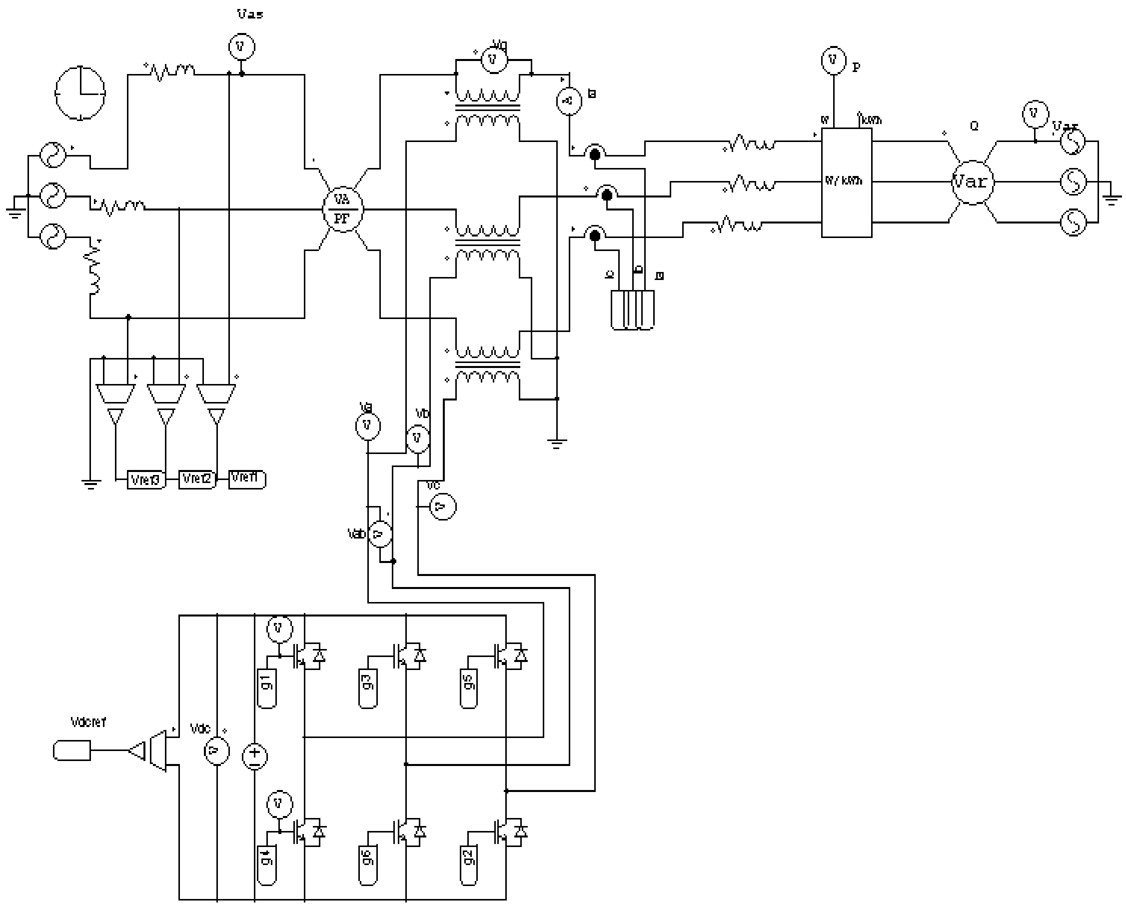

Figure 4.3: Power circuit

Figure 4.6 mainly covers the control of the transmission line reactance. The sending voltage is considered as reference and based on this, phase lock loop is made shown in figure 4.4 and 4.5. With reference to this the current is measured. Further the current magnitude is multiplied with compensating reactance($X_q = kX_L$) and this value compared with DC voltage.The output angle formed is now given to reference voltage V_d and V_q. This voltage will form the new reference value, it is then compared with triangular wave so as to obtain the pulses. This arrangement is shown in figure 4.7 and 4.8 respectively.

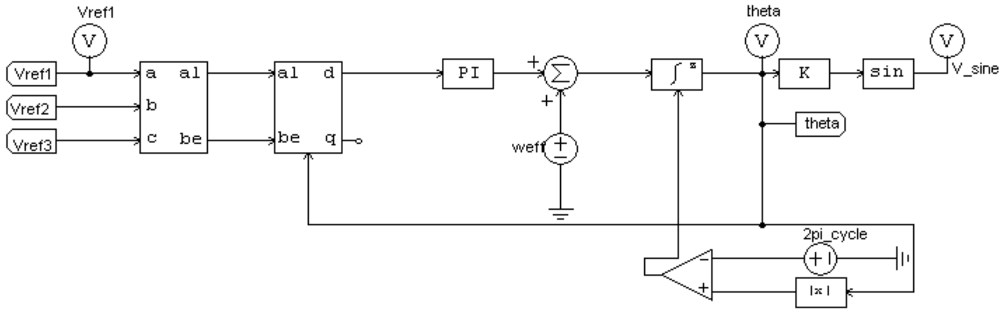

Figure 4.4: Phase lock loop

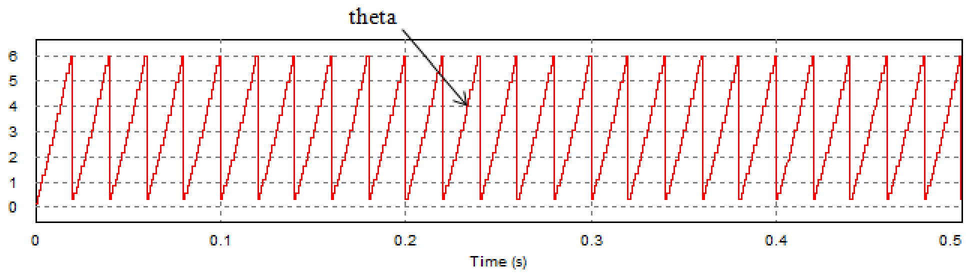

Figure 4.5: PLL output

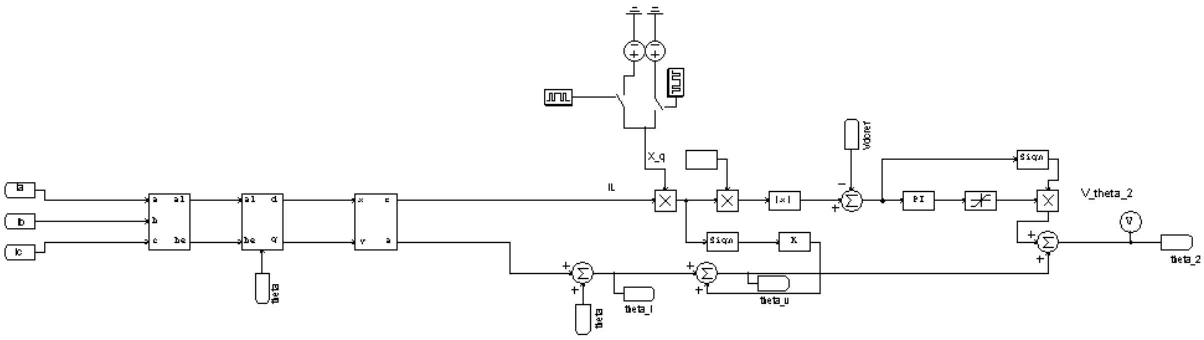

Figure 4.6: Control circuit

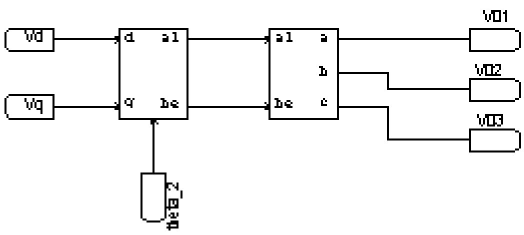

Figure 4.7: Output voltage

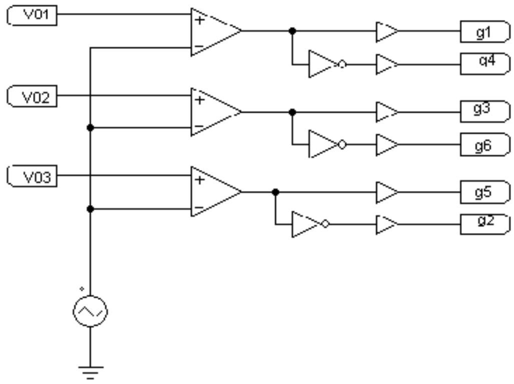

Figure 4.8: Gating signal to the switches

Considering first the compensation to be made for X_q to be 2.23 Ω. Also when the compensation is made to be capacitive the value of X_q is consider to be positive while for inductive its value is consider to be negative. The following figure shows both the operation results. The thing to be noted here is when the operation is capacitive power both active and reactive is increased while for inductive operation its value is decreased. Figure 4.10 and 4.11 shows the relation between injected voltage and transmission line current for both the operation. As shown in figure 4.12 the value of active power for uncompensated, capacitive and inductive operation is 300 MW, 392.05 MW and 208.29 MW respectively. While the value of reactive power for uncompensated, capacitive and inductive operation is -219.7 MVAR, -112.53 MVAR and -118.95 MVAR respectively.

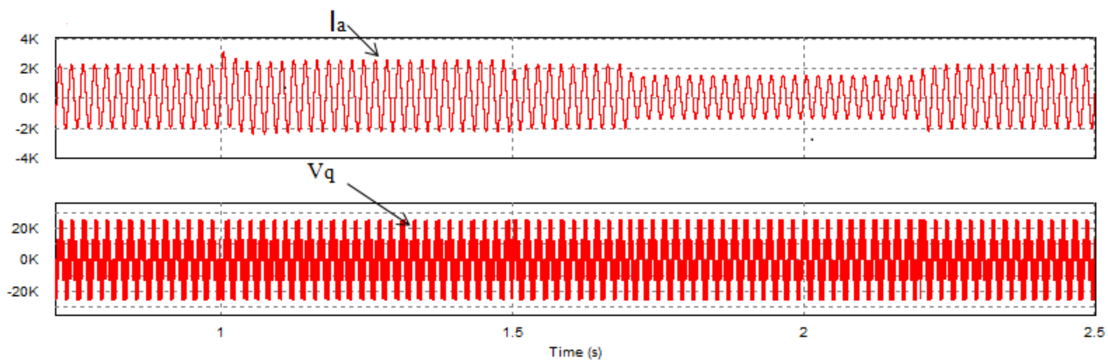

Figure 4.9: Transmission line current and injected voltage

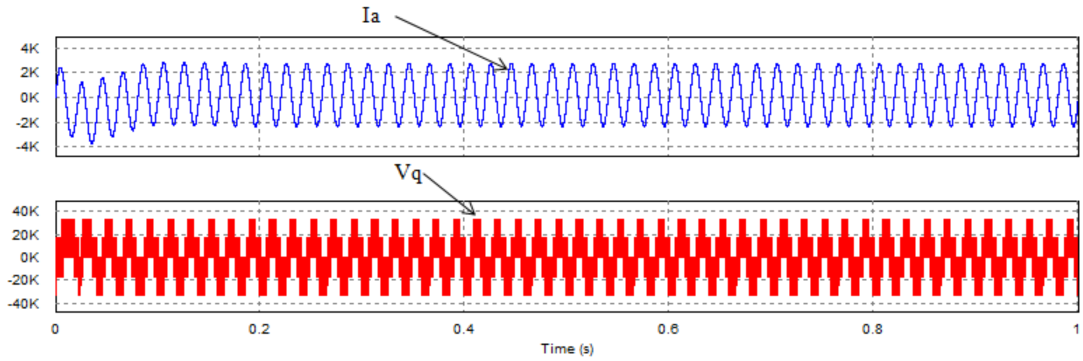

Figure 4.10: Current and voltage,V_q of phase-a for capacitive operation

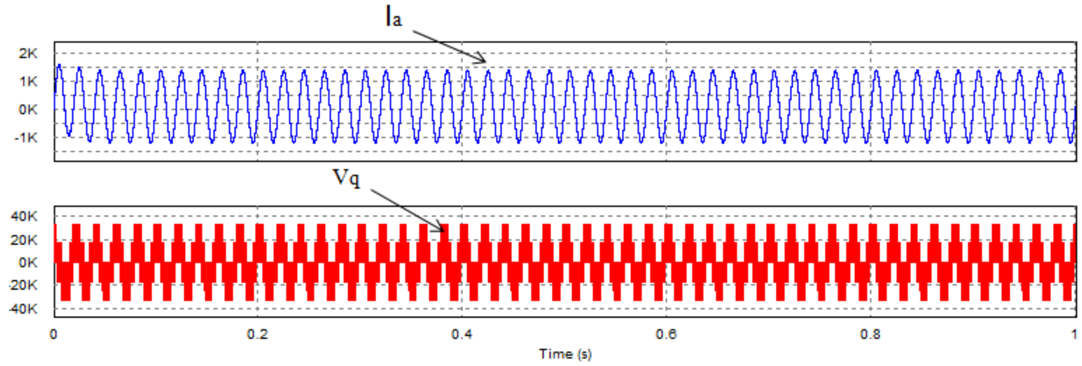

Figure 4.11: Current and voltage,V_q of phase-a for inductive operation

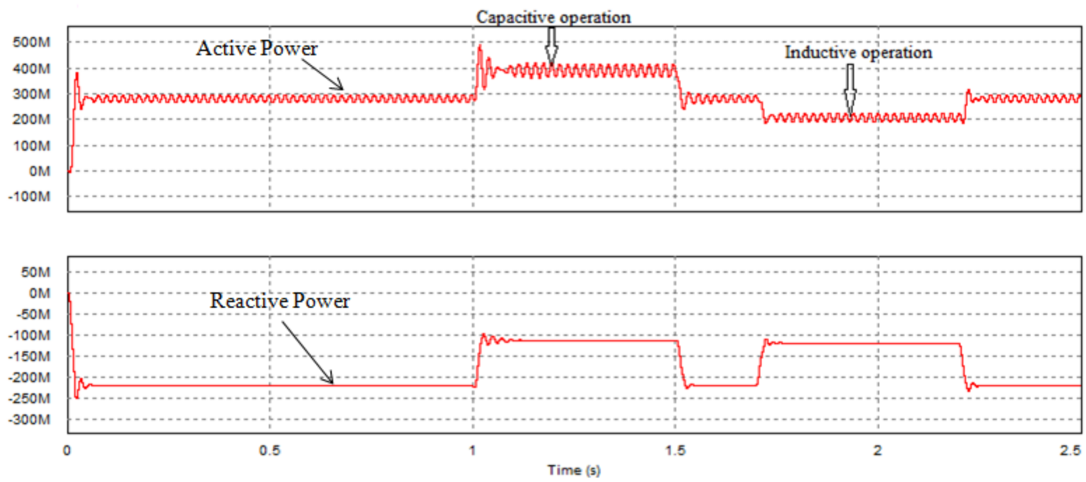

Figure 4.12: Active power and Reactive power

Chapter 5

Prototype Model

5.1 Scaled Down Model Simulation

Assuming the system of 2 kVA and 415 V, 50 Hz the related transmission parameter is obtained to have resistance and reactance of 4 ohm and 31.7 ohm respectively. Also the value of DC voltage is obtained to be 150 V. With these value the simulation results obtained are shown as follows. Figure 5.1 shows the transmission line current for phase-a having the effect of compensation and figure 5.2 indicates the compensating reactance fed to the system.

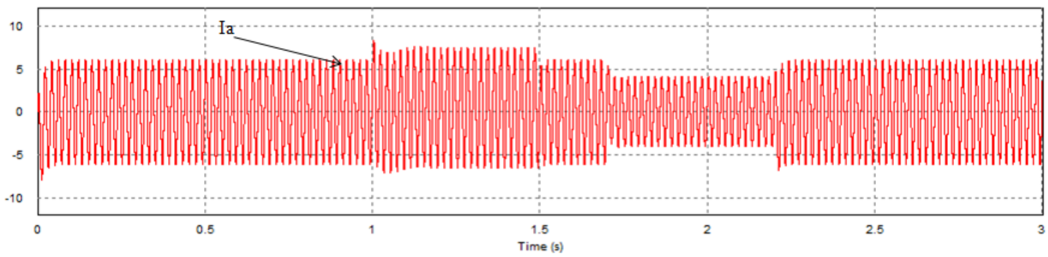

Figure 5.1: Transmission line current

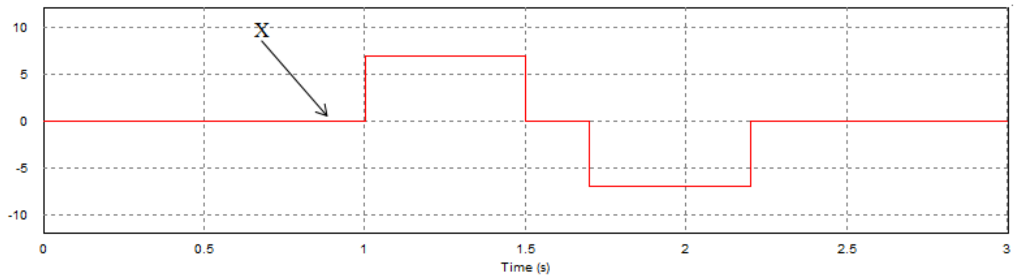

Figure 5.2: Compensating reactance

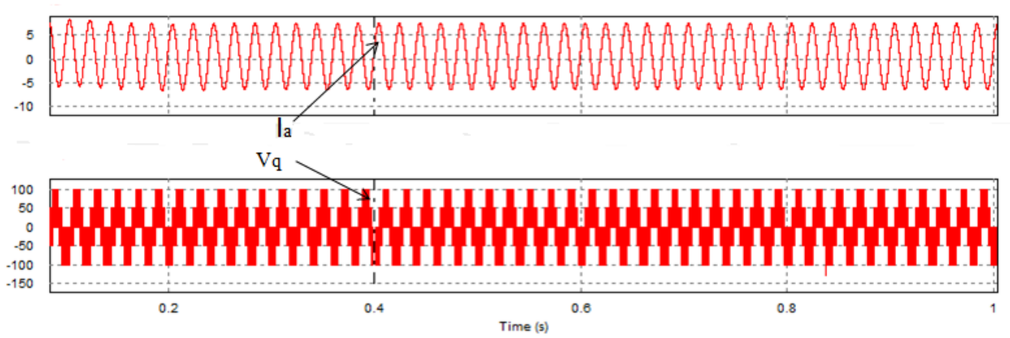

Figure 5.3: Transmission line current and injected voltage in capacitive operation

Figure 5.3 and 5.4 shows the injected voltage and transmission line current relation for capacitive and inductive operation.
Figure 5.5 shows the effect of power in the form of active power and reactive power during uncompensated, capacitive and inductive operation as 2.435 KW & -1.86 KVAR, 3.39 KW & 0.914 KVAR and 1.786 KW & -1.02 KVAR respectively.

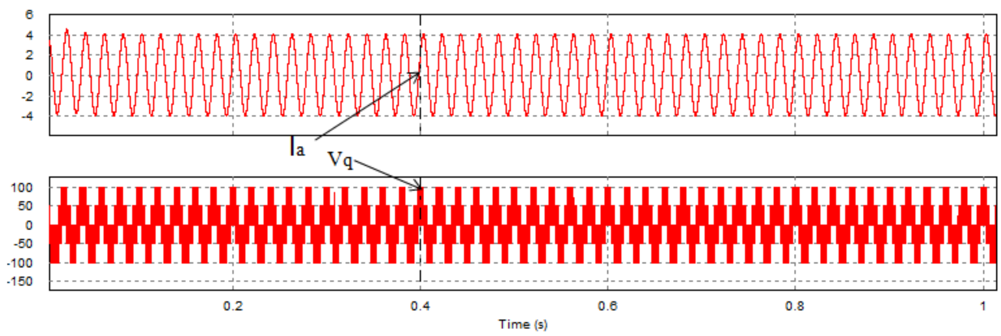

Figure 5.4: Transmission line current and injected voltage in inductive operation

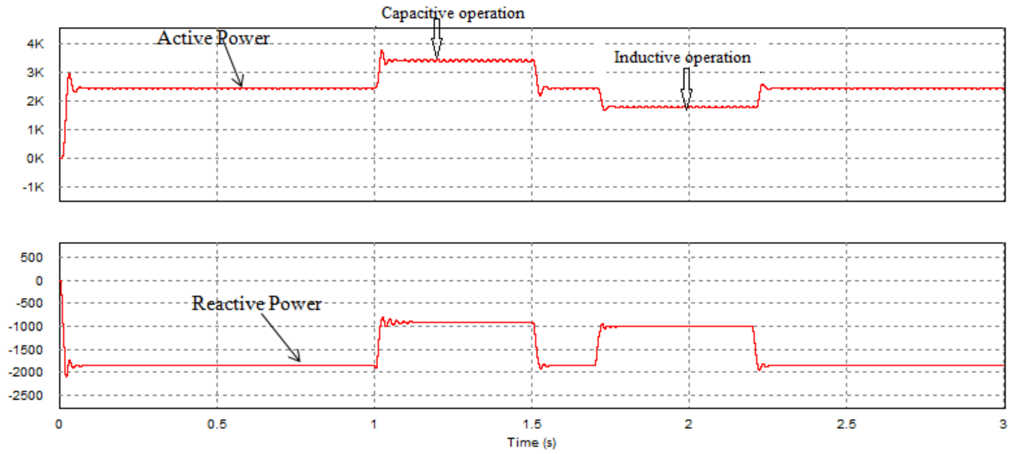

Figure 5.5: Active and Reactive power

5.2 Hardware Description

5.2.1 Driver circuit

Power supply

Gate driver power supply circuit is shown in figure 5.6. The transformer is first stepped down to 15 V and with the help of regulator IC 7815 its voltage is set fixed to 15 V which is given to the input of driver IC or else to the V_{CC}(pin 3).

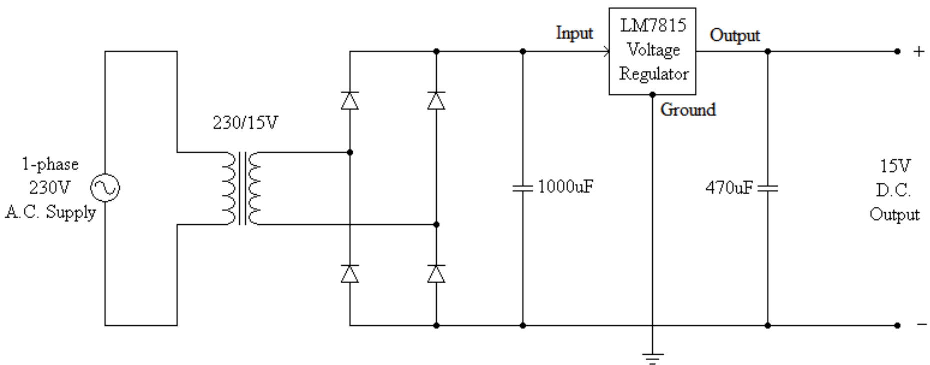

Figure 5.6: Power supply to the gate driver circuit

Driver IC IR21110

The IR2110 is high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Features of IR2110

- Floating channel designed for bootstrap operation. Fully operational to +500 V or +600 V. Tolerant to negative transient voltage.
- Gate drive supply range from 10 to 20 V
- 3.3 V logic compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs

Driver circuit connection

Figure 5.7 shows the arrangement of driver IC IR2110 where D1, C1 and C2 along with the IR2110 form the bootstrap circuitry, while D2 and D3 discharge the gate capacitances of the IGBT quickly, bypassing the gate resistors, reducing the turn-off time. R1 and R2 are the gate current-limiting resistors. Figure 5.8 shows model developed also its pin description is shown in the table 5.1.

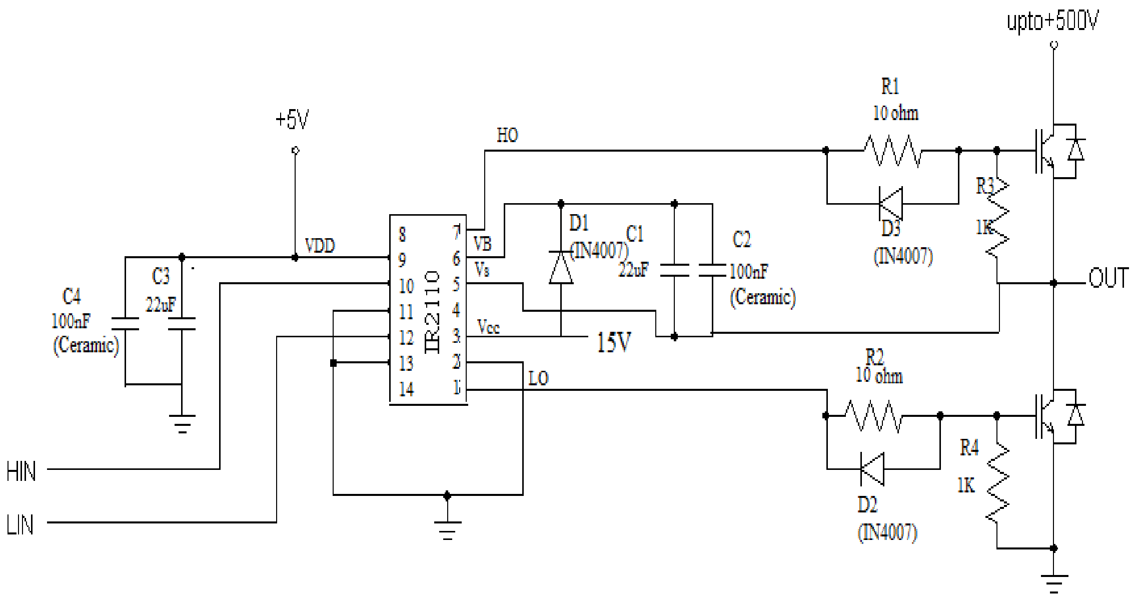

Figure 5.7: Driver circuit IR2110 connections

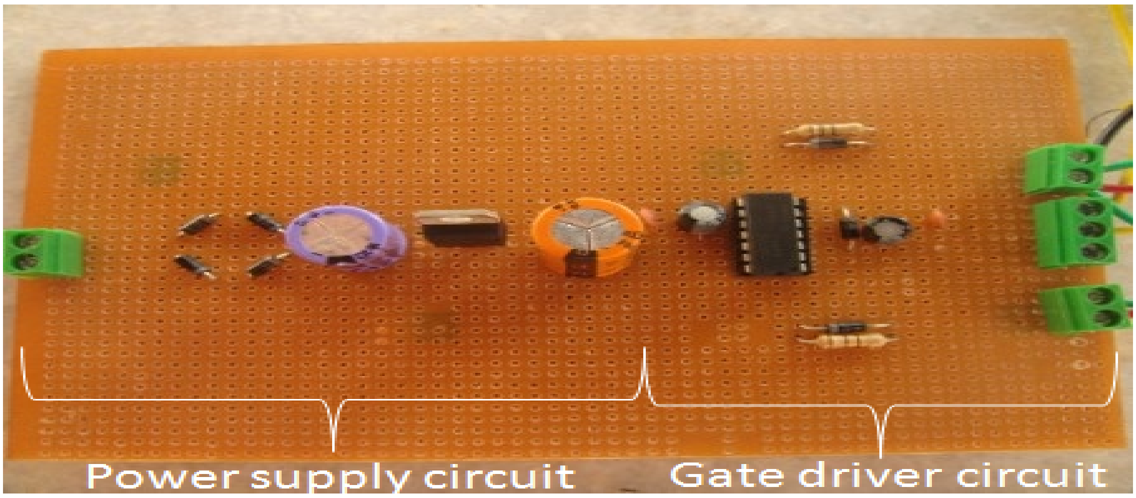

Figure 5.8: Gate driver circuit model

Pin	Symbol	Description
1	LO	Low side gate drive output
2	COM	Low side return
3	Vcc	Low side supply
5	Vs	High side floating supply return
6	Vb	High side floating supply
7	HO	High side gate drive output
9	Vdd	Logic supply
10	HIN	Logic input for high side gate driver output (HO), in phase
11	SD	Logic input for shutdown
12	LIN	Logic input for low side gate driver output (LO), in phase
13	Vss	Logic ground
4,8,14	-	Not connected

Table 5.1: Pin description

Output waveform

Figure 5.9 shows the output pulses of driver circuit. The upper pulses indicate the pulses of LO and lower pulses indicate HO.

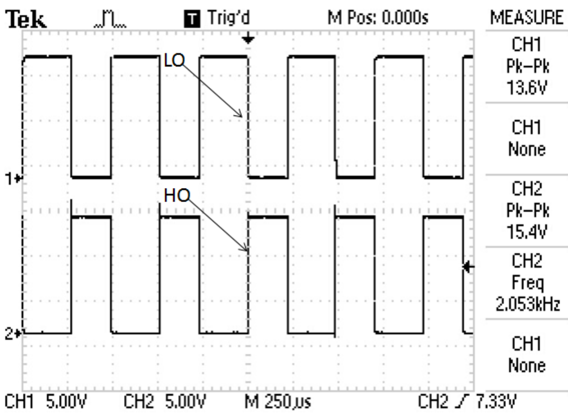

Figure 5.9: Driver output pulses(LO and HO)

5.2.2 Power circuit

Figure 5.10 shows the three-phase-bridge that has been fabricated. The power circuit is mainly made up of the IGBT and a snubber circuit.

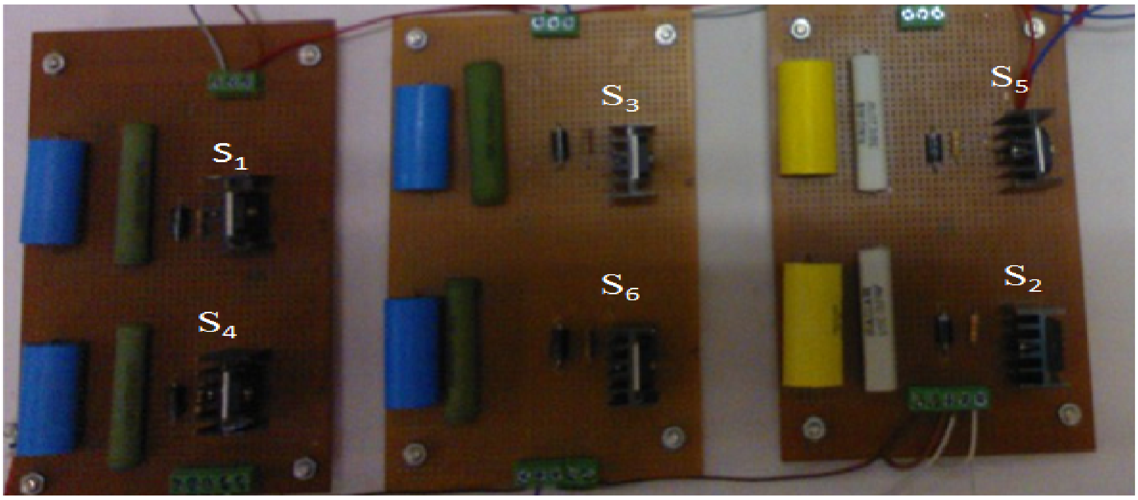

Figure 5.10: Three-phase bridge

The IGBT (FGA25N120ANTD) manufactured by Fairchild which has an anti-parallel diode is chosen here. It has a collector-emitter voltage of 1200 V and a gate-emitter voltage of ±20 V. It has a collector current rating of 50 A at a temperature of 25 °C and 25 A at 100 °C.

Here, RCD snubber circuit is connected across each IGBT as shown in figure 5.11. The diode chosen is 1N5408, the resistor is 10 kΩ, 10 W and the capacitor is 100 nF, 2000 V. It is a supplementary circuit used in the converter circuit to reduce stress on the power semiconductor devices. The snubber circuit suppresses $\frac{dv}{dt}$ and $\frac{di}{dt}$ so as to reduce stress on the device.

This helps to suppress over-voltage at turn-off to reduce the switching losses. The snubber capacitor is completely discharged at turn-on, and it is fully recharged at turn-off. The circuit helps to reduce IGBT $\frac{dv}{dt}$ during turn-off.

5.2.3 Inverter operation

Figure 5.12 shows the three phase inverter setup where it firstly operated at low voltage. Figure 5.13, 5.14,5.15 shows the pulses of each phase and 5.16 shows the dead band waveform. Figure 5.17 shows the three phase inverter output between

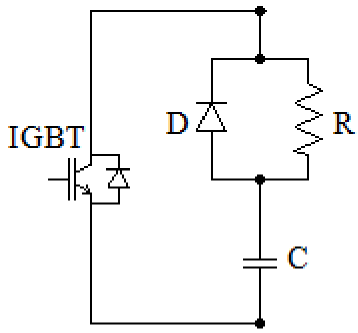

Figure 5.11: RCD snubber circuit

two phases. Further figure 5.18 shows the inverter output of one of the two phases operated at high voltage level(150 V).

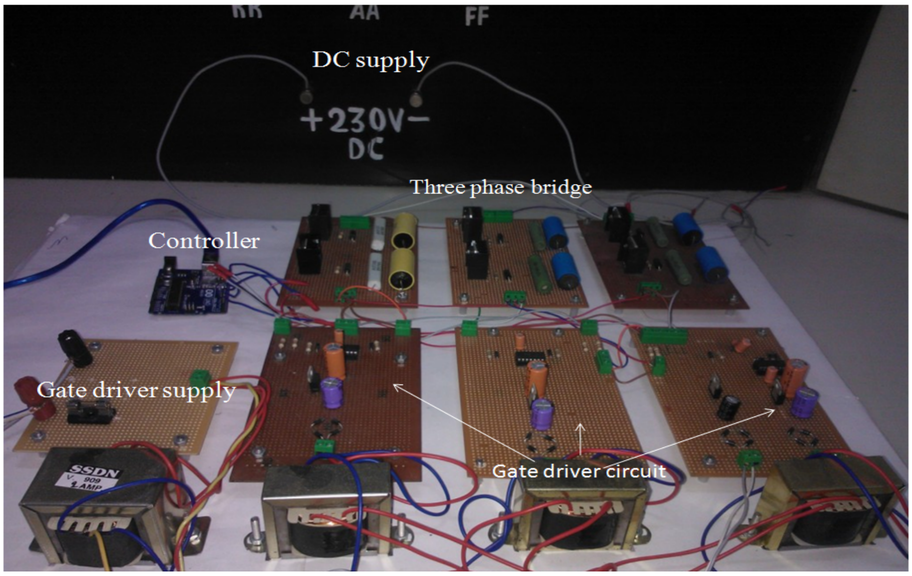

Figure 5.12: Complete setup of three phase inverter

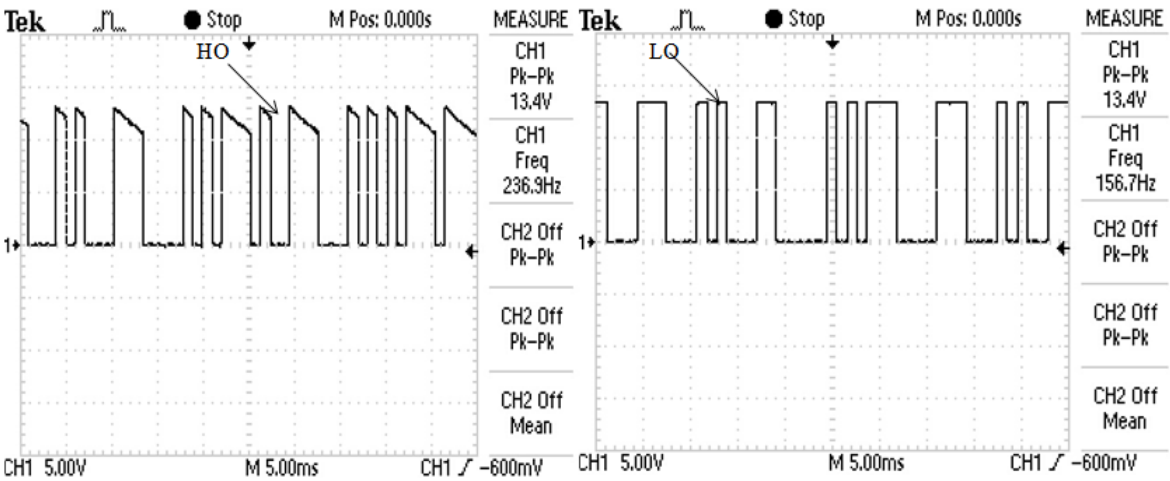

Figure 5.13: Output pulses of phase-a

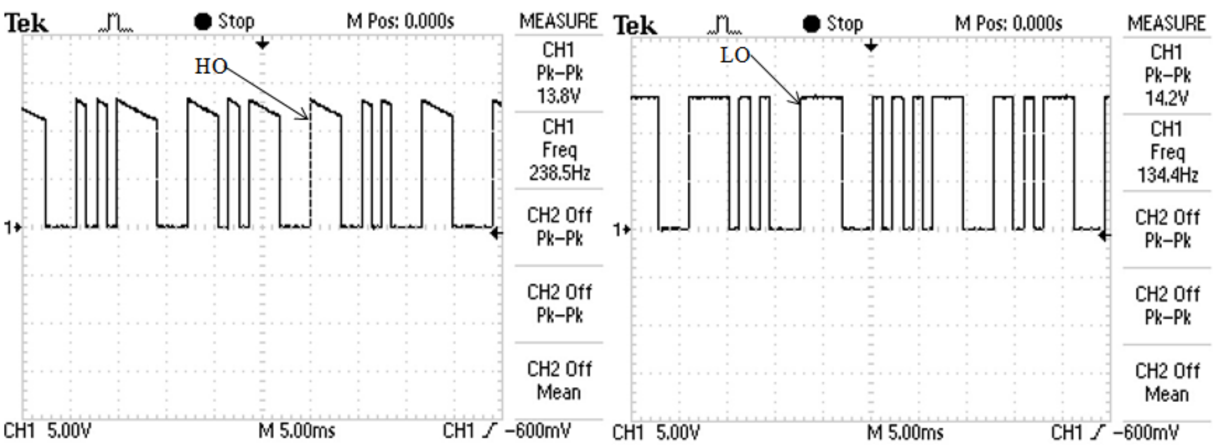

Figure 5.14: Output pulses of phase-b

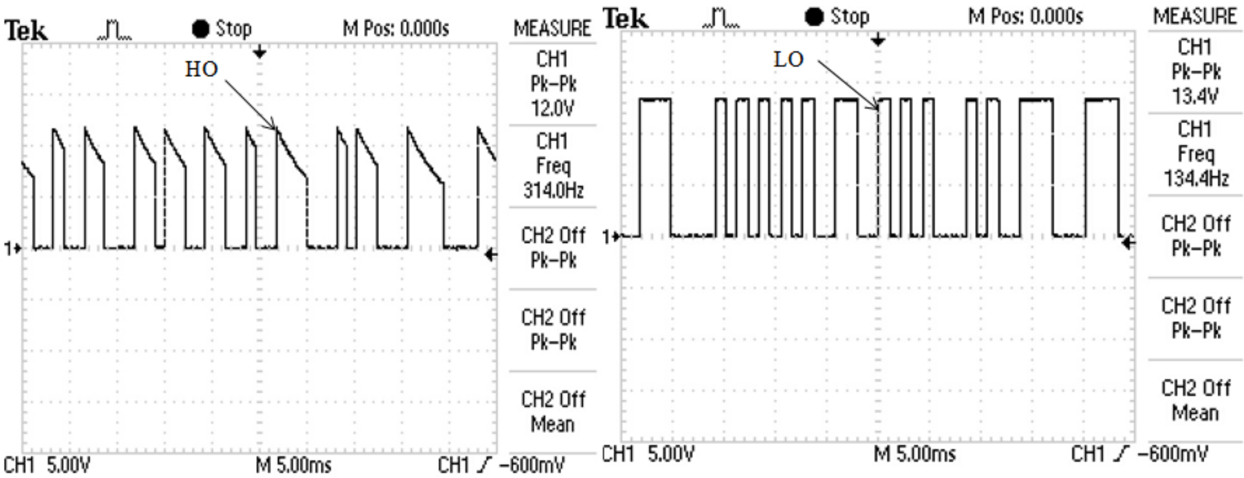

Figure 5.15: Output pulses of phase-c

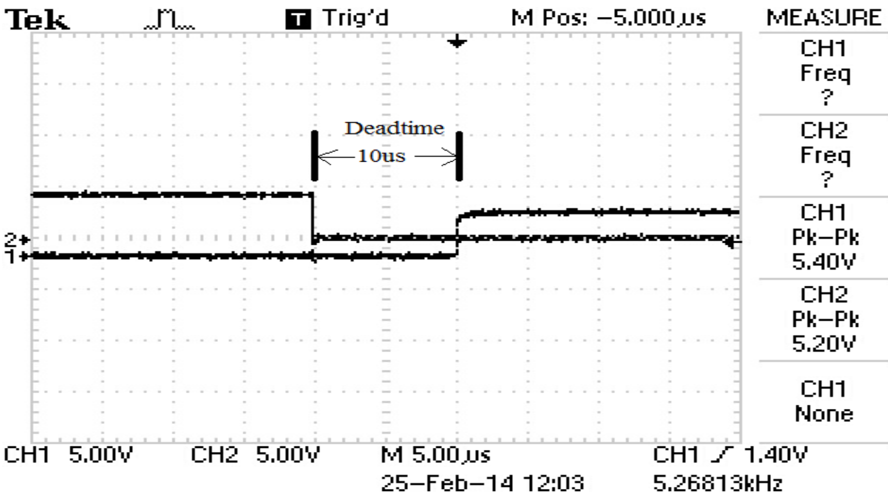

Figure 5.16: Dead band waveform

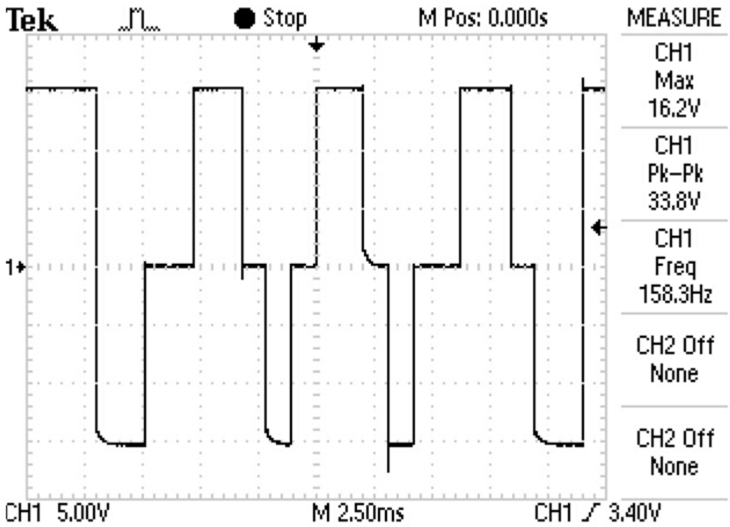

Figure 5.17: Inverter output voltage between Phase-a & b

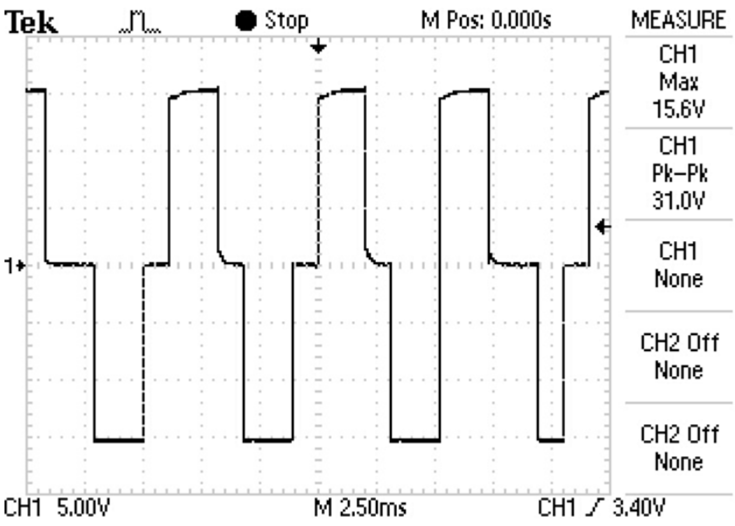

Figure 5.18: Inverter output voltage between Phase-b & c

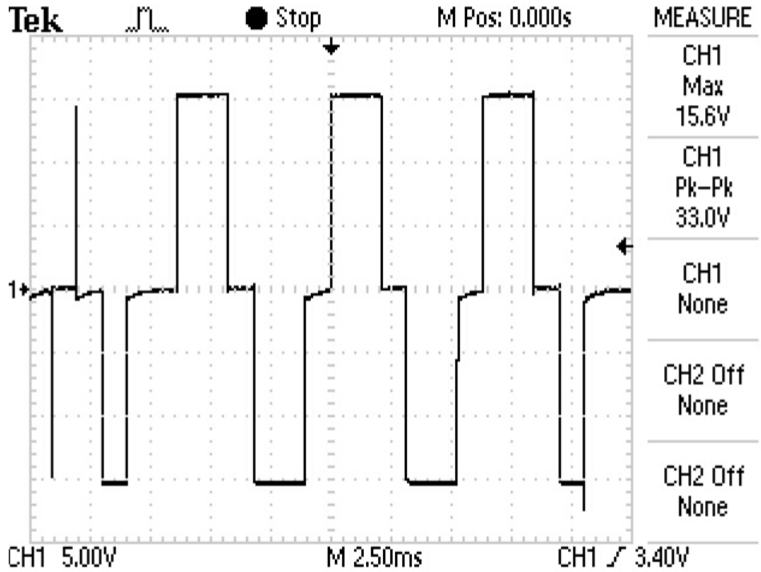

Figure 5.19: Inverter output voltage between Phase-c & a

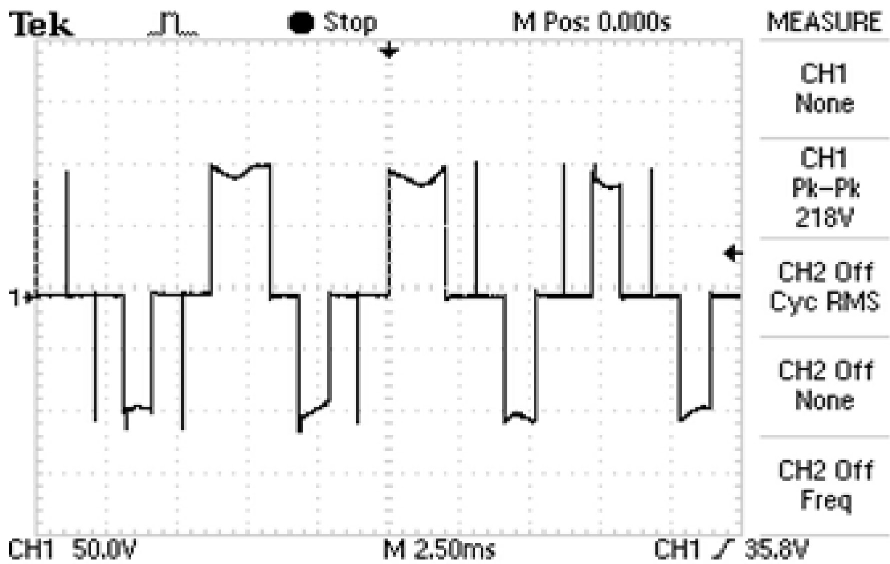

Figure 5.20: Inverter output at high voltage, 150 V

Chapter 6

Conclusion and Future work

6.1 Conclusion

It has been found that SSSC is able to control the power flow in the transmission line. It can also inject fast changing voltage in series with the line irrespective of the magnitude and phase of the line current. The operation of SSSC at steady state condition was shown.

With the help of its control circuit the performance was observed. The control scheme implemented involves the synchronous reference frame theory. This performance shows that when the compensating reactance value fed is positive, the transmission power is increased which shows capacitive operation. While when the compensating reactance value fed is negative, the transmission power is increased which shows inductive operation.

Also the same was implemented for scaled down model. Further fabrication of the hardware prototype was developed which covered the operation of 3-phase inverter both at low and high voltages.

6.2 Future Work

- The complete operation of the SSSC in different modes can be implemented.
- The operation can be made for multilevel inverter topology.
- Implementation of control scheme by varying the magnitude of injected voltage can be made.
- Further the operation of SSSC can be made for damping the oscillations and transient stability.

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