Automation of IP Qualification Test Vehicle Verification Environment

Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Hardik J Doshi

(12MECV34)

Department of Electronics & Communication Engineering

Institute of Technology

Nirma University

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Declaration

This is to certify that

1. The Project Report comprises of my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

2. Due acknowledgement has been made in the text to all other material used.

Hardik J Doshi

Certificate

This is to certify that the Major Project entitled "*Automation of IP Qualification Test Vehicle Verification Environment*"submitted by *Hardik J Doshi* (*12MECV34*), towards the partial fulfillment of the requirements for the degree of Master of Technology in Electronics and Communication Engineering Branch of Institute of Technology, Nirma University, Ahmedabad is the record of work carried out by him under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination. The results embodied in this major project, to the best of my knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Guide	
Dr. N.M.Devashrayee	Dr. N.M.Devashrayee
PG Co-ordinator (VLSI Design)	PG Co-ordinator (VLSI Design)
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Dr. P.N Tekwani	Dr K Kotecha
Professor & Head, EE	Director, IT-NU
Date: ----------	**Place: Ahmedabad**

Acknowledgement

I would have never succeeded in completing my Project Report without the cooperation, Encouragement and help provided to me by various people.

Firstly, my sincere thanks to the Test Chip team, especially the Test Chip Front End team, for their help during this training. Their wisdom, clarity of thought and support motivated me to bring this project to its present state.

I am highly indebted to my Group manager **Mr. Jawlant Joshipura** project manager, **Mr. Balwant Singh**, my immediate supervisors **Mr. Rajesh kumar Immadi** and **Mr. Vikas Sharma** for providing necessary information regarding the project and also for their constant guidance, supervision, kind co-operation, and invaluable support in all aspects.

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Hardik J Doshi

(12MECV34)

Abstract

Purpose of TestChip is to verify the invented Technology and IPs added in SOC which implementation in silicon wafer possibility. It includes all the IPs which are to be used for Researched Technology or SOC applications. TestChip provides post silicon validation details included Library of Memory,RO,Standard-Cell,Analog or any other IP. A test chip implemented in the FDSOI 28nm process is designed and fabricated, containing numerous test structures aimed of Testing silicon functionality and investigating process variation.Scan chain and Boundary scan are inserted for better testing capability.

Before any SOC/ASIC Mass Productions, Test Chip gives us better silicon parameters and testability. It makes such structure that testing made easy and less time consuming. It included BIST and BISC which are used for Testing and Characterizing chip itself automatically. BIST (Build In Self Test) include the logic of the memory testing algorithm of memory, by setting up the some of the internal register pins. BISC (Built In Self Characterization) used for Setup Time Characterization, Maximum Frequency Characterization, Access Time Characterization of chip.

Test Patterns are similar to test vectors except these are cycle based patterns. Patterns for the testing are deliver to the Fabrication after the tape-out. These Patterns are almost same except which IP are being tested so that I have responsibility to make these patterns automatically generated. Fulfillments of this tool gives better quality of test patterns,accurate and less time consuming to generate. It also helps in quick verification of RTL/netlist of any block or while chip. This thesis presents a test chip methodology and automatic generation of test pattern to help achieve these fundamental goals.

ST Microelectronics At A Glance

- A world leader in providing the semiconductor solutions that help our customers improve quality of life for everyone, both today and in the future
- Among the world's largest semiconductor companies
- A leading Integrated Device Manufacturer serving all electronics segments
- A leading technology innovator (around 12,000 researchers approx. 21,500 patents)
- Key strengths in Multimedia Convergence, Power Applications and Sensors
- Rich, balanced portfolio (ASICs, Application-Specific Standard Products and Multi-Segment Products)
- A pioneer and visionary leader in sustainability
- President and CEO: Carlo Bozotti
- 2011 revenue $9.73 billion
- Approximately 50,000 employees including STEricssion at December 31, 2011
- Advanced research and development centers in 10 countries
- 12 main manufacturing sites
- Corporate Headquarters Geneva, Switzerland

- Global presence with sales offices all around the world
- Public since 1994 - shares traded on New York Stock Exchange (NYSE: STM), Euronext Paris, and Borsa Italiana
- Created as SGS-THOMSON Microelectronics in June 1987, from merger of SGS Microelettronica (Italy) and Thomson Semiconducteurs (France)
- Renamed ST Microelectronics in May 1998

Group Introduction

The TR&D is a group in ST which works on integrated products (IPs). Its work is to provide quality Library Solutions and services to divisions, in the company's drive in time to market, IP Reuse and Super Integration. There are various types of IPs:

- Test Chip and Design Flow : Test Chip works on making the device more testable, works on Boundary Scan, Scan Chain,ATPG and make the Test Patterns of the device and give to IC Fabrication Lab to help in testing on-chip silicon. Test Pattern are the inputs given to IC ,verifies the functionality whole chip as well as Module basis and check that IC has any faults (deflectable) or not.The customer, as per his requirements, gives the specifications to the flow team. These requirements are analyzed and as the needs, the features required for the design are noted. These are sent to the Back End Team for the designing. After the design is ready, it is checked for the specifications and then sent to the Front End for the characterization and functional modeling.

- Memories : A device or an electrical circuit used to store a single bit (0 or 1) is called a memory cell. Examples of memory cell are flip flop, a charged capacitor etc. Semiconductor memories are capable of storing large amount of Digital information. The amount of memory required in a particular system depends on the type of application but the no. of transistors required for storage of data are always much larger than the no of transistors used for logic operations and other purposes. The ever increasing demand of high storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently towards higher data storage densities.

- Digital Design : It is the layout of basic sequential and combinational circuits which are used to make bigger circuits. It is the basic building block of all the circuits. It is a component within an integrated circuit with known functional

and timing characteristics, which can be used as an element in building a larger circuit. Example of standard cells include Inverter, Flip-flop (FD), Latch (LD), Multiplexer (MUX), NAND, NOR, AND, OR, XOR, XNOR, Full Adder (FA), Half Adder (HA).

- Concept Of Library : A library is collection of cells all of which reference the same technology file. The cells are the smallest functional unit. Attached to every library is a technology file. A technology file is a large data file that specifies, in one central location, all of the technology-dependent parameters associated with that particular library. The purpose of library is to reduce the design cycle of the designer.
  - Basic building blocks: Digital (AND, OR); Analog (amplifier).
  - Complex building block: Digital (Microcomputer); Analog (PLL, DAC).
  - Memories: Single or dual port SRAM, ROM etc.

  The cells are delivered as a set of different views. These views are used by different tools in a given Design flow. These cells are used until the physical implementation.

Contents

List of Figures

Chapter 1

Testchip Introduction

RTL is large architecture of low level constructs called standard cell. This architecture is taken from standard-cell library consisting of pre-characterized collections of gates.Standard cell is typically particular to the planned manufacturer of the ASIC or System On Chip.

Standard Cell is fundamental cell which are used frequently in design of chip (e.g. OR,AND,XOR,XNOT,Inverter). It includes Latch and Flip flops types of storage elements. Common usage function are already includes in standard cells and used directly from standard cells library like element of XOR,XNOT,NAND,NOR. This library is specific to particular technology.

In order to meet diverse SoC application requirements, it is not practical to design the whole system from scratch. Hence the approach is to integrate complex blocks that have been individually designed. These blocks are called intellectual property (IP) cores. An IP core is a reusable unit of logic, cell, or chip layout design and is the intellectual property of one party. IP cores may be licensed to another party or can also be owned and used by a single party alone.

The SoC containing test-structures for memories, mixed IPs, standard cells and sensors is used as test chip for post silicon validation. It provide assurance that functionality of IPs, standard cells and other components are correct and it's maturity is high enough for the mass productivity.

1.1 Testchip:- Concept

There is large financial and time loss if any bugs or functional defect captured in new SOC/ASIC production. To resolve where Errors are occurred after packaging or at production level is very time consuming and might be unresolved for production level which suffers financial loss as well as takes time.

Testchip is way to mature latest technology to verify its functionality of different IP blocks and implementation of the logic on to the physical silicon chip. It makes good view in term of fabrication process of latest technology's or any SOC's Testability, Functionality and Reliability.

Testchip also includes extended Testability of the Chip itself so that time to market consumes less and need inexpensive tester. It has very on-chip pattern generator and testing algorithms for memories. It ensures the maturity of th invented technology on silicon and finds out the fabrication defect for same.

Advantage

- It provides the best design flexibility for upcoming production of the chip.
- High performance and High density by resolving the problem which occurred at the Testchip.
- Highlighting CAD vs Silicon results differences of different IPs
- Effort to make Low Power Consumption for Latest Technology.
- Implement the Best Test Environment for the Market Deliver Chips.
- Gives Less Financial loss if Technology has any fabrication incompatibility.

Limitation

- Silicon wastage because testchip is not in any SOC applications so testchip targets to test as more as different IP in silicon area.

1.2 Testchip Design Flow

Technology development now not only driven to improve the circuit speed and density, but also concentrating on reducing the power consumption. Power is emerging as the most critical issue in system-on-chip design today so scaling would be mandatory and Smaller dimension circuit have been preferred which lesser and lesser nm technology is chosen.It is important to have detailed understanding of the power consumption behavior of a chip.

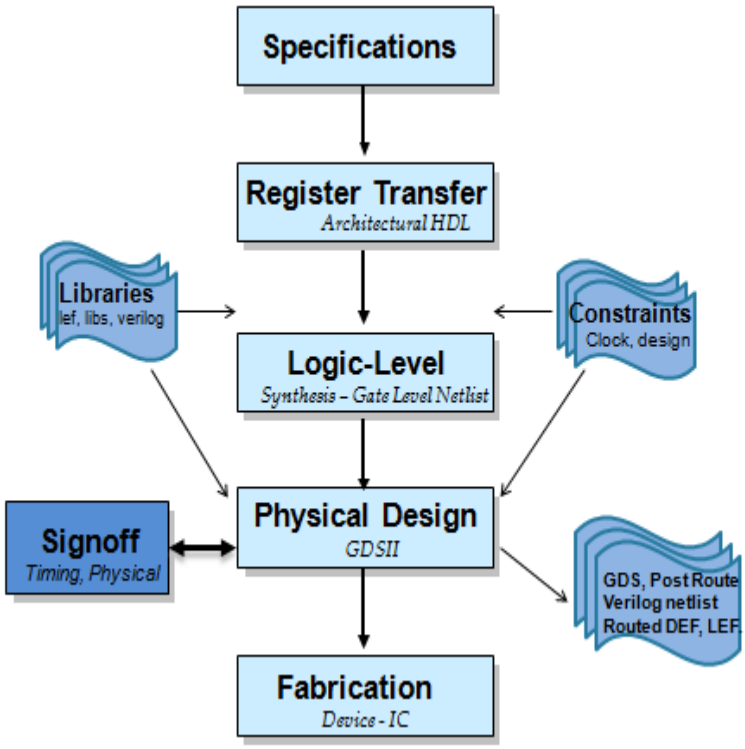

Figure 1.1: Testchip Design Flow

The IC design process starts with a given set of requirements. After the development, this initial design is tested against the initial design requirements. When these requirements are not satisfied, the design must be improved. If such improvement is either not possible or too costly, then the requirements must be revised and the IC design process re-starts with the new modified requirements.

The failure to properly verify a design in its early phases typically causes significant and expensive re-design at a later stage, which ultimately increases the time to market. Thus, the verification of the design plays a very important role in every step. Fig.1 provides a view of the Very large scale integration (VLSI) design flow based on schematic capture systems.Although top-down design flow provides an excellent design process control, in reality, there is no truly unidirectional top down design flow. Both top-down and bottom-up approaches have to be combined. For instance, if a chip designer defined architecture without close estimation of the corresponding chip area, then it is very likely that the resulting chip layout will exceed the area limit of the available technology. In such a case, in order to fit the architecture into the allowable chip area, some functions may have to be removed and the design process must be repeated. Such changes may require significant modification of the initial requirements. Thus, it is very important to feed forward low-level information to higher levels (bottom up) as early as possible.

1.3 Expectations of Testchip

As stated above that Testchip is chip to target testing of different IP in silicon wafer before any mass productions in SOC Integration/any new technology to set up for production. Testchip design flow helps to design flow of chip mass productions because of new technology cells and library is not mature at production level. The cycle time of the Testchip has to be tight so that necessary action can be taken to improve the IP or flow before the actual product out to the market. Design flow of testchip schedules from 1 to 4/5 months depending on the complexity of testchip.

1.4 Cost if bug detects at production time

SOC fabricates for mass production without made testchip and on silicon validation specification. Large Financial loss has to be suffered for company if any functional errors or bugs occurs. It might be solved sometimes any minor errors at packaging level like any output have attenuated logic level.

The Pentium FDIV bug was a bug in the Intel P5 Pentium floating point unit (FPU). Because of the bug, the processor would return incorrect results for many calculations used in math and science. The error was rarely encountered by users. Intel were criticized very heavily and ultimately recalled the defective processors.

1.5 Components added to Testchip

- Memory IP
- Standard Cell
- Analog Mixed IP

1.6 Problem Statement and Its Solution

Test chip utilize before usage of any of IPs in SOC application, it would be tested first in silicon chip and its functionality is verified for physical silicon. Test chip is used for detailed information of the post silicon validation and used for better implement logic to the physical silicon chips. Therefor, SOC integration starts after the testify with test chip. There is any delay in test chip development as SOC will have to be delayed. There is challenge to reduce time for test chip. It reduce time to market SOC or ASIC if it may reduce the time for test chip.

Any SOC/testchip reduce time to market by how fast verification is performed so reduce time to verified the Design of Test Chip is very important. Design of testchip is almost reached at least time.Challenge is be to verified testchip so that we can ensure that SOC might have been right functionality except any fabrication defects.

By Introducing AUTO TEST PATTERN GENERATION TOOL, It generates the test patterns automatically by giving the Design mapping Document of IP and Design activation IP Documents.Design mapping Document has the mapping information that which top pins related to the IP pins at the low level hierarchy and their execution cycle file values of top pins. Design activation IP Document has its block select value which used for active particular block and its down hierarchy block called as CUT where actual IPs and their supported driven blocks.Design mapping Document also has input data bus width and address bits.

Basically Test chip have different Memory IP with compiler supported. Different Test Chip have same compiler but have different mapping pins from the Memory IP pins to TOP level so that Every time test patterns have to written according to the Test chip. Now After developing AUTO TEST PATTERN GENERATION TOOL, Patterns are related to a Compiler not TEST CHIP so It would be easy to maintain patterns algorithm templet according to compiler because Memory IP

compilers are almost repeatedly in all TEST CHIP.

Tool makes the Patterns to not related to Specific Test chip because the top of TEST CHIP always being changed,not MEMORY IPs. Design Mapping Document of Specific Test chip is provided by the Test Chip Developers which are used to generate the mapping files in the patterns and other files and algorithms are always being generic to Memory IP. Tool has the list of the patterns of algorithms and list of Memory IP those are being likely to generate.

1.7 Importance of Verification Environment Automation

As Testchip design flow is very tight and short, from Design,implementation,verification and sign-off have to completed very quick. As Verification is very time consuming depending on the complexity of design. Verification would be made quickly if test patterns(test bench) for designs are created automatically. These type of automation is very time saving and effective for verification. Also, Quality of Verification is very much improved.

1.8 About Project: Test Pattern Automation

Testing semiconductor memories is increasingly important today because of the high density of current memory chips. In this thesis report we investigate on the various functional fault models present for todays memory technology and discuss about the ways and means to detect these faults. Emphasis is laid on classical Walking, Galloping and March pattern tests, which are widely used today for testing chip level, array level and board level functional memory defects. Classical fault models are not sufficient to represent all important failure modes in a RAM; Functional Fault models should be employed. Memory Fault models can be classified under the

categories shown below, brief descriptions of the models are given as follows.

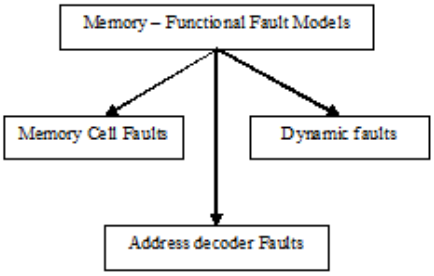

Figure 1.2: Basic Memory Fault Models

To detect the functional and address defect, some of the testing algorithms are made

- Conventional Algorithms
- March Algorithms
- Advance Marching/mats Algorithms

Write the test patterns for the different memory blocks with different address range and output-input range.This blocks are selected by using the testchip additional register and decoders. The internal tool language is used to write such algorithms test patterns and checked by the converting verilog code and analyses the simulation result. The functional bug will not be contained then it would be finalized test patterns and forward the test patterns to the fabrication. It would be checked that verification results and the testing results are totally same.

These test patterns are written with manually efforts so its consuming quite a large time to make these patterns. My Responsibility to make the automation of creating test patterns of memory blocks with different patterns of memory modes. By converting automatically pattern from the design documents, Quality of test patterns are very much improved. It includes Some Testing algorithm test patterns, Simulation work and Scripting part.

Chapter 2

Memory IP and Standard cell

2.1 Standard Cell

Standard Cell is fundamental cell which are used frequently in design of chip (e.g. OR,AND,XOR,XNOT,Inverter). It includes Latch and Flip flops types of storage elements. Common usage function are already includes in standard cells and used directly from standard cells library like element of XOR,XNOT,NAND,NOR.This library is specific to particular technology. Test chip contains the whole standard cells library in post silicon validation. A standard cell library is a consolidated data used in designing a soc(system on chip). It is a collection of low level logic functions such as AND, OR, INVERTER, flip-flops, latches and buffers. These cells are realized as fixed height variable width full-custom cells. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. The cells are typically optimized full custom layouts, which minimize delay and area. Full-custom design is no longer feasible as Complexity of the design is continuously increasing. Standard cell contains layouts and power calculations.

2.2 Memory IP

SOC integration is not possible of without any memory component. Memory IP is very vital part of SOC and any reason of failure of memory IP result SOC application failure. Memory is being different types based on SOC application.

Semiconductor Memories are classified according to the type of data storage and the type of data access mechanism into the following two main groups

- Non-volatile Memory (NVM) also known as Read-Only Memory(ROM) which retains information when the power supply voltage is off. With respect to the data storage mechanism NVM are divided into the following groups:
  - Mask programmed ROM. The required contents of the memory is programmed during fabrication,
  - Erasable PROM (EPROM). Data is stored as a charge on an isolated gate capacitor (floating gate). Data is removed by exposing the PROM to the ultraviolet light.
  - Electrically Erasable PROM (EEPROM) also known as Flash Memory. It is also base on the concept of the floating gate. The contents can be re-programmed by applying a suitable voltages to the EEPROM pins. The Flash Memories are very important data storage devices for mobile applications.

- Read/Write (R/W) memory, also known as Random Access Memory (RAM). From the point of view of the data storage mechanism RAM are divided into two main groups:
  - **SRAM (Static Random Access Memory)**
  - **DRAM (Dynamic Random Access Memory)**

Our Targets for test chip are SRAM and ROM memory. SRAM used as cache memory in micro-controllers , like the primary caches in powerful microprocessors, such as the x86 family, and many others,to store the registers and parts of the state-machines used in some microprocessors on application specific ICs, or ASICs (usually in the order of kilobytes).ROM is used extensively in graphic cards, hard disks, DVD drives, TFT screens.

2.3 Static RAM

The memory cell is a 6 transistor circuit which is a flip flop comprising two cross-coupled inverters and two access transistors, the access transistors turn on when the word line is selected (high) and its voltage rises to Vdd, and they connect the flip flop to the bit lines. Sizing of the transistors in the memory cells is very important especially for speed and chip cost.

The sense amplifier is important in the total performance of the SRAM chip since the sense delay time directly affects the access time. Sense amplifier is used to sense the small changes in voltage that results when a particular cell is switched onto the bit line. One stage differential pair of sense amplifier is utilized here. The sense amplifier circuit is controlled by a clock signal, which is synchronized with the pre-charging and word-line signals.

- **TYPE OF SRAM:-**
  - **Single Port static Random Access Memory (SPRAM)**
  - **Dual Port static Random Access Memory (DPRAM)**

2.3.1 Single Port Random Access Memory (SPRAM)

SPRAM is a single port synchronous static RAM contains single port to used for read and write operation.When clock goes to negative logic edge to positive logic edge, CSN and WEN is low, Memory is written whatever data is given to data port at current address given at address bus. When WEN is HIGH, CSN is low and CLK goes to POSEDGE, Memory is read at current address given by address bus and data reflects on the Output Bus.

- Memory has logic low control pin of CSN and WEN.
- WEN - Write Enable logic low Write when Logic low otherwise read.
- CSN - Chip select logic low Chip selected Write when Logic low otherwise disable.
- Memory has SLEEP which is used to switch off peripheral. Memory also has test mode,scan chain pins,special testing pins.

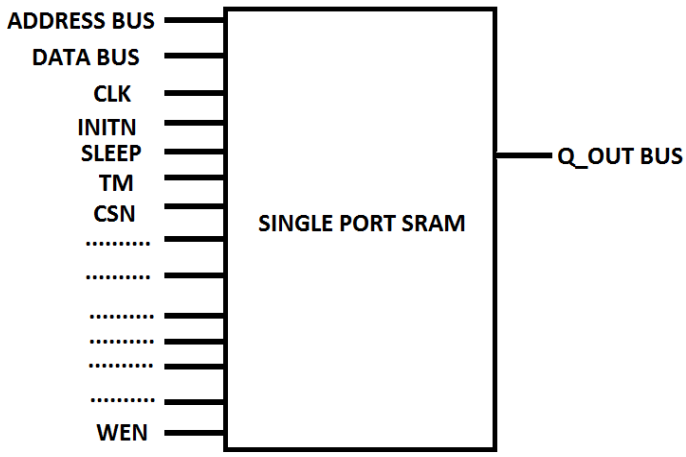

Figure 2.1: SINGLE PORT SRAM

2.3.2 DUAL Port Static Random Access Memory (DPRAM)

DUAL Port SRAM gives advantage of read and write perform simultaneously by adding extra data bus, address bus and extra control signal.In some application like Video RAM , Elevators to Robot Control, Commercial Aircrafts to Unmanned Flight Controls, Surveillance cameras to Night vision systems.Dual Port Memory has increased bandwidth approximately 2x the speed of a similar single port RAM.

2.3.2.1 DUAL Port Static Random Access Memory TYPE-1

This type of dual port memory has only one data port though it contains read and write different address bus as well as different chip selection bit. It has one write enable signal common for both. When Memory is going to read, Address is captured from read address bus and when Memory is going to write, address is captured from write address bus. Both read and write also have different chip selection pins.This dual port memory has limitation that it can read or write at a time.

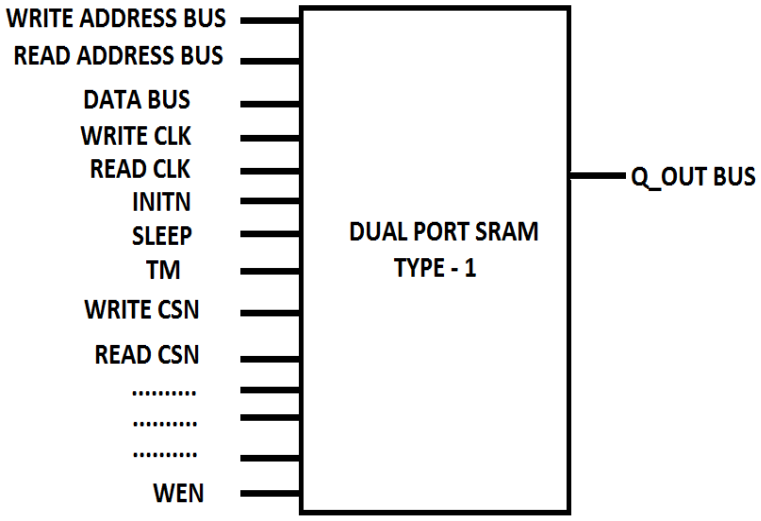

Figure 2.2: DUAL PORT RAM TYPE - 1

2.3.2.2 DUAL Port Static Random Access Memory TYPE-2

This type of dual port memory has two data port though it contains read and write different address bus as well as different chip selection bit. It also contains different write enable signal which gives permission to read and write at a time.

Memory has two data inputs port , two cheap selection enable , 2 write enable , 2 Address Bus as well as 2 Output Data ports. It is same like two SPRAM (Single Port SRAM) are going to attached together.

DUAL PORT SRAM port is independent of each other. Both port have their own WEN and CSN signals as well as their operating frequency.

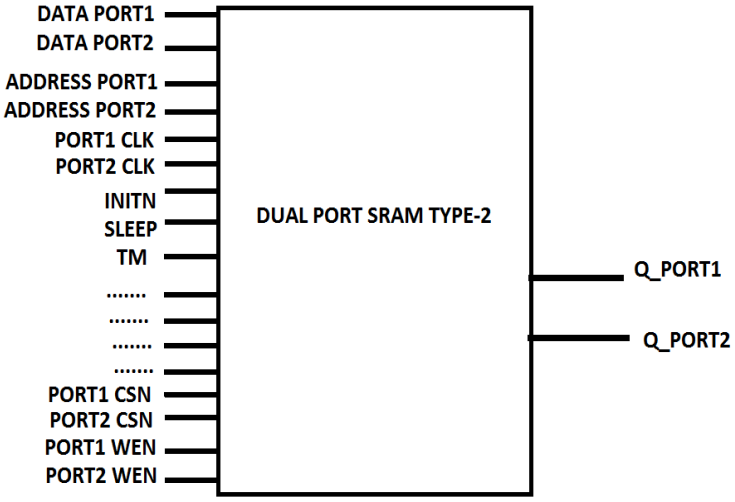

Figure 2.3: DUAL PORT RAM TYPE - 2

Chapter 3

TestChip Architecture

3.1 Purpose Of Testchip

Test chip is single chip contains different type of IP blocks which includes for silicon qualification and functionality test.It has RAM and ROM type memory includes single, dual port RAM.It has Memory-BIST and BISC for easy testing Methodology. BIST has in-built Memory testing algorithms which enable by the registers performs the memory testing algorithms to all Memory IPs. Then output gives the bad and repair signal for that particular memory.

Test chip is special purpose silicon Qualification chip which performs to many testing on implemented blocks. It has tested with different Power, voltage and temperature. It has radiation test,life time test which ensures how to improved yield of our product. As much as CAD level data and actual data correlated that let yield and productivity of chip goes to high.

The list of blocks which includes in Test chip are as below

- Memory Blocks
- PLL Blocks
- Standard cell Blocks and RO Chain Blocks

Testchip is needed to give post silicon validation parameter to our customer. Testchip is testify that our IP,standard cell Library, Analog and mixed IPs performs normal expected functionality. Ideally, Testchip should be made first before any Maturity level of any technology library or SOC Integration but Practically TestChip will be made parallel with SOC integration. Testchip's testing result and post silicon data comes before SOC final implementation. SOC modification does if TestChip results reflects it.

Flow of Maturity of Library is given below :-

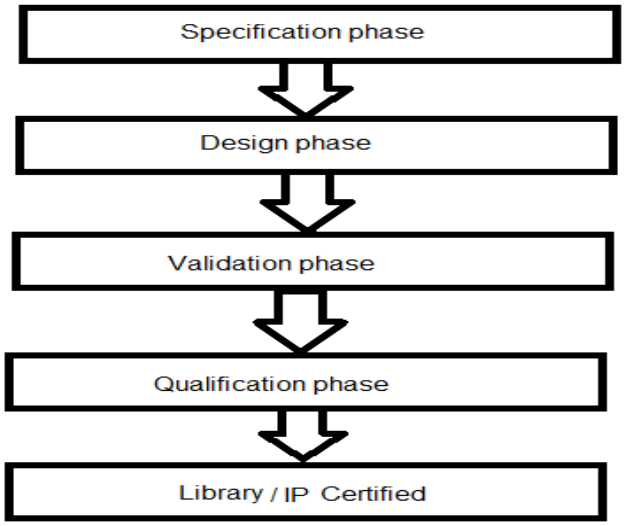

Figure 3.1: Maturity flow of Library and IP

- First step :- Define a new technology platform. There is no specification at this time and no library component. It takes list of component from old library.

- Second step :- Next, the specification is set and it includes all component of new technology platform (process,libraries,CAD tools) After Design is completed with help of library cells and components. Layouts and characterizing performed at this level.Some other components might be defined later also.

- Third step :- This level, the design are validated on the silicon. Here the Functionality and characterizing of library by testchip.
- Fourth step :- At last level, Testability is defined very well. It makes easy to test and must take less time.Yield and productivity must increased of chip.Library and IP is certified at this step with post silicon data.

Testchip is full custom chip from specification to tape-out as well as fully testable so that TestChip contains some of features give below which used accurate and speedy design generation. Automation of Design also can be used if these features available.

- Repetitive design across Memblock
- Design Re-use and standardization
- Reduction of manual effort

3.2 Architecture of Testchip

3.2.1 TOP LEVEL

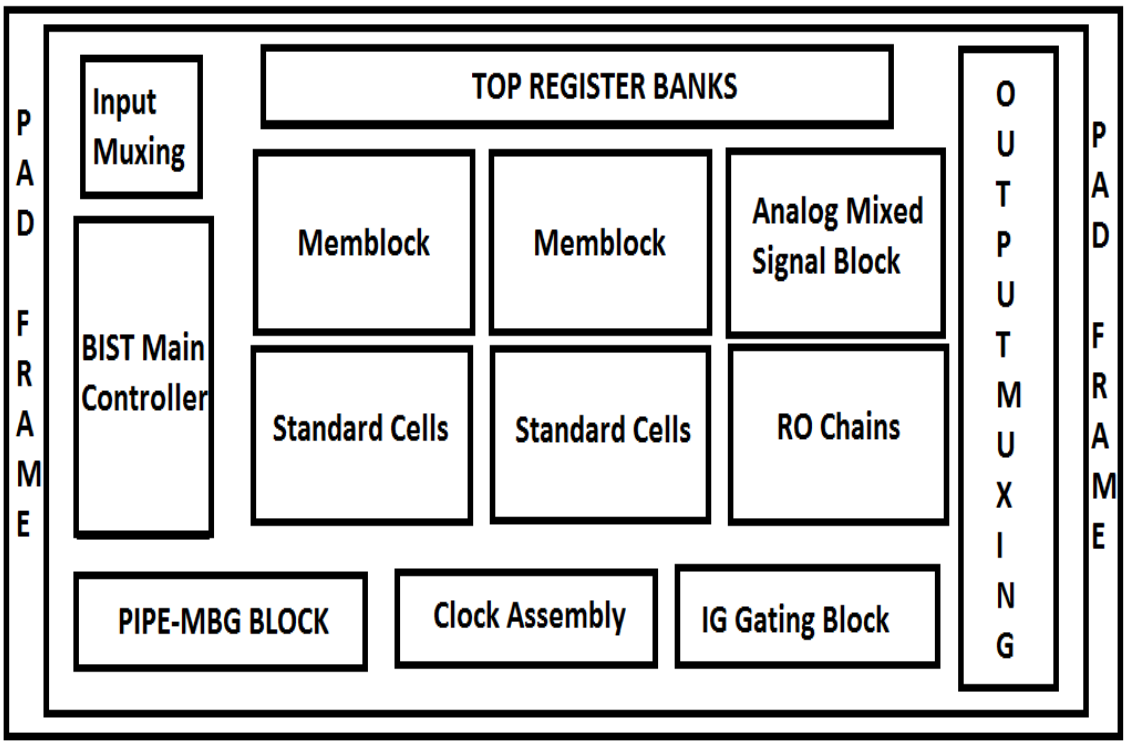

Figure 3.2: Testchip Architecture Block

TestChip Architecture is shown as above with TOP Level hierarchy. Their functionality are given below

- Input Muxing :- Used to take input from external world passing to downwards
- TOP Register Banks :- Register Bank has particular enable pins and IP selection pins of Memblocks and any other blocks
- CLK Assembly :- This block is useful for mapping which clock is used specific memblock and IP.
- BIST Central Controller :- BIST Controller controls all the signals which carried to BIST Wrapper around every Memory IP.

- Output Muxing :- This block is responsible to carried away output bus to the padframe.
- PIPE-MBG :- Pipling used for operating faster clock ans MBG(Macro Backgroung Logic) is used for generation of different type input combination.
- IG-Gating :- Memory has special IG pin used for blocking input data to the memory pins when enable.
- Output Muxing :- This block is responsible to carried away output bus to the padframe.

From TOP of TestChip, there are many blocks and blocks are divided as per design. For any selection of Blocks, BLOCKSEL[N-1:0] Register is placed in TOP Level of Testchip,where N is maximum block number. How to select BLOCKSEL is described after this section. For more testability, boundary scan is added to the top level input and output pins.

3.2.2 MEMBLCOK LEVEL

Below TOP LEVEL, Many memblocks and block of other IP are included. These Memblocks have many cut blocks which contain memory IP and other blocks used for characterization different memory parameter.Memblock contains BISC(BUILT IN SELF CHARACTERIZATION) Controller which controls all BISC related operation to all Memory IP and pass to output to TOP LEVEL.

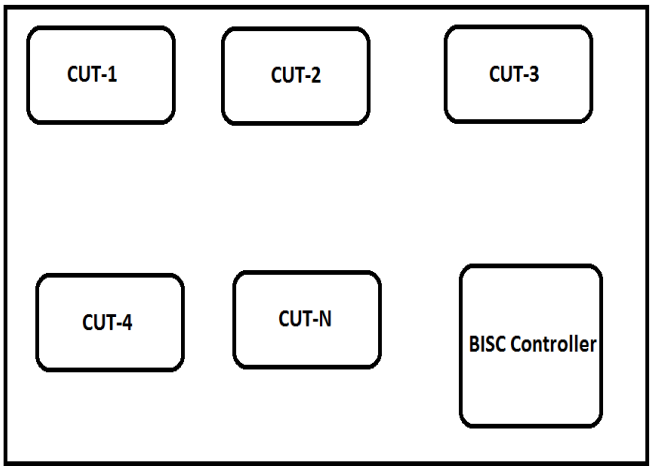

Figure 3.3: MEMBLOCK Structure

- CUT :- CUT has Memroy IP and Other blocks used for testing and characterizing memory. There are maximum 32 CUTS in a Memblock.
- BISC Controller :- It is dedicated to one memblock for which characterizes memory parameter like setup time, access time and maximum frequency of memory.

3.2.3 CUT LEVEL

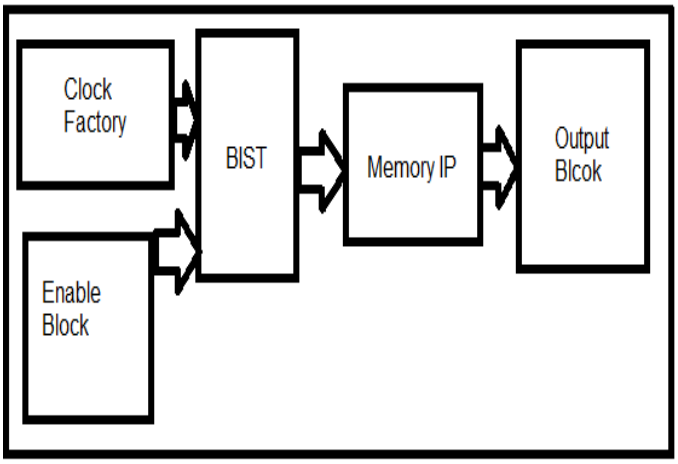

Figure 3.4: CUT Structure

CUT is block which preserves memory IP with BIST wrapper and other blocks which enables memory through itself. CUT type od block is repeatedly designed in MEMBLOCK. One CUT memory IP is different compared with other CUT memory IP with respect to physical area of memory, size of memory, operating frequency of memory.

- CLK Factory :- Block is used for generation of clock while characterizing the memory.
- Enable block :- It is for Chip Selection Pin selected for desired CUT only.
- BIST Wrapper :- It captures BIST control signal from BIST MAIN Controller and passes through this wrapper only.
- Memroy IP :- Memory IP is targeted IP which used to silicon Qualification. It has different address bits and different data bits according to test specification.
- Output Block :- It used to pass the output logic to upper hierarchy for external world.

3.3 Block Select and CUT(IP) Select

Any VLSI Chip has limited number input pins from External world and limited output pins to external world. Chip also have power supply pins and ground pin.Due to limited pins are being used from TOP level, How to get select particular Memblock and for that Memblock how to get select one Memory IP is Big challenge to Designers.Second challenge Memory IP contains different Address and Data bus due many Memory IP integrated in Single IP.

Testchip has two special input pins used for programming of mode.It has BLOCKSEL[1:0] pins from padframe.

Table 3.1: Programming Mode

CTRL[1]	CTRL[0]	Programming Mode
0	0	Serial Mode using TAP
0	1	Parallel Register Mode
1	0	Internal MEMBLOCK Mode
1	1	Normal Operation

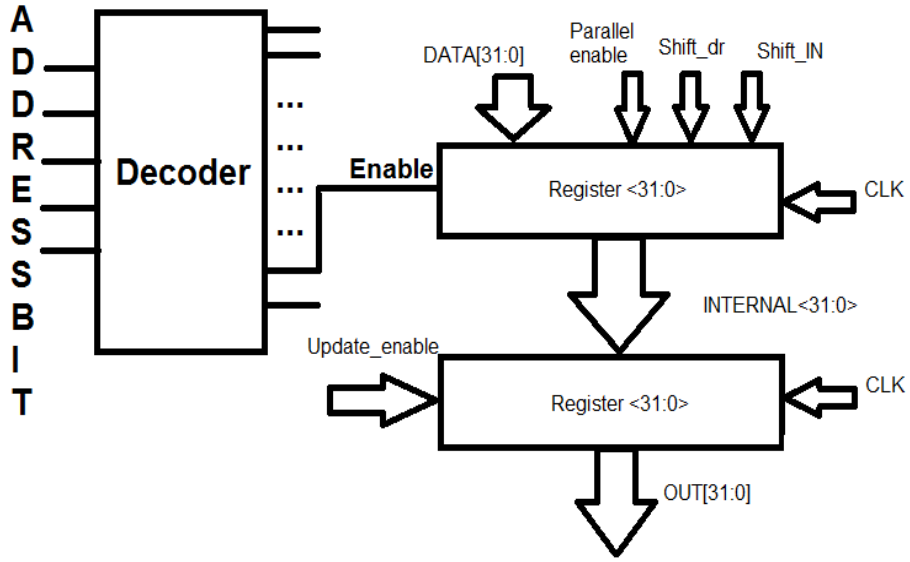

Figure 3.5: Data Register used for BLOCKSEL and IPSEL(CUTSEL)

- CTRL[1:0] = 01 bits are used with Parallel programming mode for TOP Register bank loading
- BLOCKSEL[31:0] is one TOP REGISTER BANK which is programmed after power on time.
- Every Block has its own BLOCKSEL[n] (here n is block number) pin which enable particular block. BLOCKSEL[31:0] is mapped with TOP DATA[31:0] bus.
- All Register pins of inputs [31:0] are connected with TOP DATA[31:0] BUS but Enable is on for only one of the register bank which is coming through decoder output. Decoder inputs are 5 bit address pins which is called Register Opcode.Decoder is used to reduced the TOP input pins.Here with 5 bit address bits, 32 TOP registers are going access. e.g. BLOCKSEL Register opcode = 00001
- After Block selection, there is one more IPSEL[31:0] register bank which is programmed with parallel mode. TOP DATA[31:0] bus is also mapped to IPSEL[31:0]. Every CUT has its predefined IPSEL number through which it can access the memory IP. e.g. IPSEL Register opcode = 00010
- After IP selection, there is one more MODESEL[3:0] register bank which is programmed with above same procedure. TOP DATA[31:0] bus is also mapped to MODESEL[3:0](Other pins are not connected).MODESEL indicated which mode are going to used. When Direct Memory Test(DMT) starts, no need of BIST Controller usage so it would be bypass in DMT. When BIST used, BIST controller utilized in this mode.e.g. MODESEL Register opcode = 00011
- Same technique is used for Memblock Regsiter Bank but CTRL[1:0] = 10. In Memblock level, One Register bank used so that some of Memory IP pins are access through this register and TOP Pins are going to decreased.

3.4 Mode of Operation

- DMT (Direct Memory Test) :
- BIST (Built In Self Test)
- BISC (Built In Self Characterization)
  - ATC (Access Time Characterization)
  - STC (Setup Time Characterization)
  - MFC (Maximum Frequency Characterization)
- DMT MODE:- In this mode, The address bits, the data bits and other memory inputs reach all the memory irrespective of any value on Cut select . But the chip select of all cut will be kept at inactive state except the selected cut . The output at the pads is also decided by the value of cut select bus, i.e., the output of Memblock will corresponds to the selected cut only.
- BIST MODE:- In this mode Memory is run along with BIST. Depending upon whether a shared or dedicated BIST architecture is used the memory is tested and data input is given to memory by BIST collar. Once BIST operation is complete it communicates the result through bend and bbad signals. In case of shared BIST architecture, once the BIST operation is complete, it sends the result(bbad,bend,etc) to the controller as well as the output.
- BISC MODE:- BISC or Built in self characterization is the mode in which different memory parameters are characterized using a Central controller and different BISC macros.These parameters includes Access Time of memory, Setup time of any memory pin, Maximum frequency of operation of BIST+Memory. Following are the sub modes of BISC operation.

Chapter 4

Test Patterns of Memory Testchip

4.1 Test Patterns

Test Patterns require to access to testchip at time of testing. These are predefined cycle based patterns which are logic low or logic high input value depending on particular pattern. One test pattern is related to one CUT targeted with selecting the respective Memblock and their related Mode Selection. Test Patterns give strobing to the output so tester can expect ideal logic value comparing with actual logic value coming.

Test Patterns are written with cycle base language developed by STMicroelectronics. These patterns are deliver to the Testing team for silicon testing of Test chip. Test patterns of any function faults has been written with algorithm basics so that Tester at testing time need not larger size of memory where as for ATE(Automatic Test Equipment) does require.

Test Pattern is input combination which can drive chip and can tested the functionality of the chip. Test patterns are given to the Fabrication Lab so that their testing engineer would be fired these test patterns and ensures that silicon chips have not any physical defects or faults. The good and bad chips are filtered out. Faulted Testchips are used for the faults and physical defect analysis. There are

different test pattern algorithms are used for these testing like example Checkerboard Pattern,BIST Pattern,Direct Memory Test Patterns. Checker board Patterns are separated with two cell groups-odd memory address group and even address group. Now with such groups are written particularly with logic value 1 in one group and others are 0 logic value. These patterns find the SAF as well as Address Decoder Faults. BIST Patterns are initialize the BIST internal registers, internal registers driven the data bus ,address bus and output verifies with expected output. Direct Memory Test Gives to access the whole memory from the outer world and can be driven any test pattern, reflects the output at chip output bus.

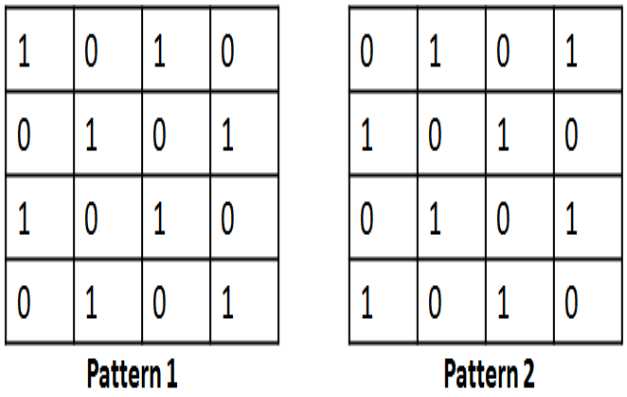

Figure 4.1: Checkerboard Pattern

4.1.1 Advantage of Test Pattern

- Test Vectors are not needed due to Usage of Test Pattern.
- Tester has lesser size of memory so Test Patterns overcome tester limiation.
- Reusable of cycles which are part of Test Patterns.
- Ensures good testing quality.
- Testchip Test Patterns are in written in STMicroelectronics with help of the utile Language which is cycle based language. It requires all the input chip pin has logic value. It ensures that any of TOP pin do not keep floating because tester does not 'X' as well as can ambiguous the output of the chip.
- Loops are used with given pin logic value with every time clock is given and toggles in cycles which easily debugged by the Test Engineer.
- Cycle is combination of driven input value. When main algorithm file use EXE "Cycle_name", Cycle of "Cycle_name" is executed and drive values to input pins. Different Cycle file have to been used for different modes.
- This utile language is converted into verilog which used for the simulation and debug these test patterns at Simulation level.
- After testing the Chip, testing output would be forwarded to the design team and verify the CAD level chip and testing chip output.
- Testchip give better fabrication chip defects and fault models for latest technology development and gives low financial loss if technology is not reliable and stability.

4.2 Test Patterns supported files functionality

- First step to define the constant file which has constant that are used in algorithm at any stage. It also has clock cycle time and other time constant defined.
- Second step to define mapping pin information, in test chip memory pins mostly same but their pins are varied with top level mapping, so every time to make a pattern is very tedious job. To define compiler wise mapping and its algorithm is most practical and connivent way.
- Third step to define variables those are used later in the algorithms and give the defaults value to their.
- After variable definition writing the procedure files which are used to define value to TOP Pins.
- Next to define cycles depend on Mode where each every cycle has different pin values according to the functionality.
- Main algorithms is defined the pins of top and gives it value according to algorithm iteration or as per the functionality demands.Cycle passes these value to pins and clock is driven after these.
- These repetitive manner of algorithm executes until the proper functionality is not verified.

4.3 Flow of Test Patterns

In Test Pattern, above figure showed the way of pattern written, here detailed about how these patterns are worked with design.

- First the constant,variable,mapping,procedure files have to defined.
- Starting with algorithm, first Reset High and Reset Low cycle executes which give High logic at reset and low logic respectively.
- After this Block selection is mandatory. Block selection is done with data pins and some of the address pins.
- Next,CUT selection is mandatory. CUT Selects based on the memory block indexing so same value(indexing value) have to pass for selection of CUT though from TOP side CUT Number is not as same as Index value.
- After selection of CUT, Providing the mode selection value with same methodology of data pins and some of the address pins form top.
- Test chip is now accessible to Memory IP or any other IP to perform the operation on it.

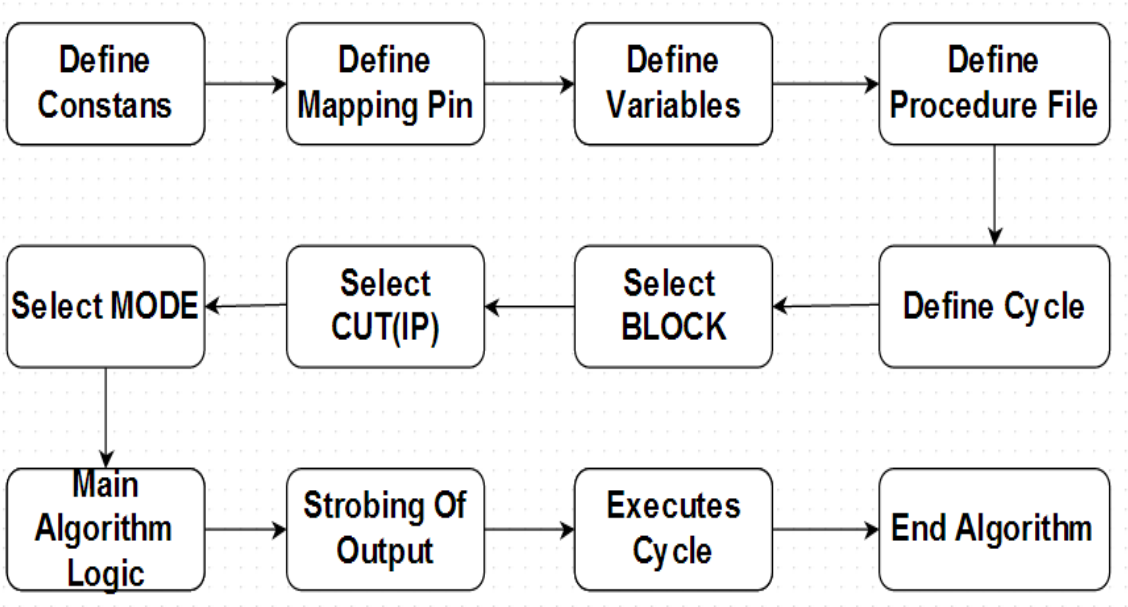

Figure 4.2: Flow of Patterns

Chapter 5

Auto Test Pattern Generation Tool

Test Pattern of DMT MODE, BIST MODE, BISC MODE are used to verify their functionality at testing time. These Patterns are almost same to respective MODES, except IPSEL Register Value is changed depends on which CUT is being targeted. That is why automation is needed for generating patterns. Manually, Test patterns take time of 10-13 days.

5.1 Need of Automation Tool

- Lesser time to generation of automation Pattern.

- Quality of Test Patterns are very much improved due to every single patterns are verified at silicon level.

- Similar Automated Test patterns(conversion to Verilog testbench) utilized in quick validation of RTL and netlsit of Design because this tool only need design document which deliver when RTL is ready.

5.1.1 Problem Statement and Its Solution

SOC integration starts after the test chip or parallel with testchip design. There is any delay in test chip development as SOC will have to be delayed. There is challenge to reduce time for test chip. It reduce time to market SOC or ASIC if it may reduce the time for test chip.

Any SOC or Test chip reduce time to market by how fast verification is performed so reduce time to verified the Design of Test Chip is very important. Design of Test chip is almost reached at least time. So Challenge is be to verified Test Chip so that we can ensure that SOC might have been right functionality except any fabrication defects.

By Introducing AUTO TEST PATTERN GENERATION TOOL, It generates test patterns automatically by giving the Design mapping Document of IP and Design activation IP Documents.Design mapping Document has the mapping information that which top pins related to the IP pins at the low level hierarchy and their execution cycle file values of top pins. Design activation IP Document has its block select value which used for active particular block and its down hierarchy block called as CUT where actual IP and their supported driven blocks.Design mapping Document also has input data bus width and address bits.

Basically Test chip have different Memory IP with compiler supported. Different Test Chip have same compiler but have different mapping pins from the Memory IP pins to TOP level so that Every time test patterns have to written according to the Test chip. Now After developing AUTO TEST PATTERN GENERATION TOOL, Patterns are related to a Compiler not TEST CHIP so It would be easy to maintain patterns algorithm templet according to compiler because Memory IP compilers are almost repeatedly in all TEST CHIP.

Tool makes the Patterns to not related to Specific Test chip because the top of TEST CHIP always being changed,not MEMORY IPs. Design Mapping Document

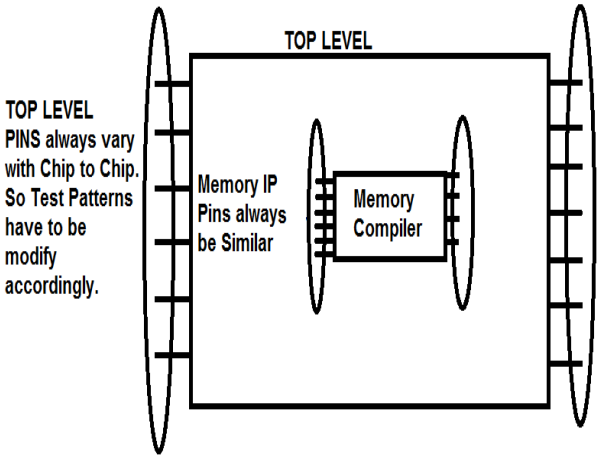

Figure 5.1: TOP level to memory compiler

of Specific Test chip is provided by the Test Chip Developers which are used to generate the mapping files in the patterns and other files and algorithms are always being generic to Memory IP. Tool has the list of the patterns of algorithms and list of Memory IP those are being likely to generate.

Memory IP of different type are stated above chapter 2. Memory IP which have similar address, data bits, output bits called COMPILER.Compiler types are given as below:-

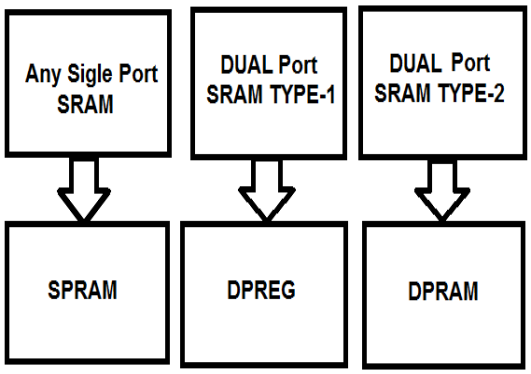

Figure 5.2: Compiler TYPE

As Stated above chapter 4 that Different mode have different cycles. Tool is generated these cycle files from Design mapping Document file.

5.2 Auto Test Pattern Generation Tool

Tool is generated patterns automatically providing input of Design mapping Document and Design IP Information document. Design mapping documents (CSV file) contains information of top pin to IP pins and Design IP Information document has list of patten to generate for IP,compiler of IP,address range of the memory,data bus width of memory and particular memory block and its CUT activation index.

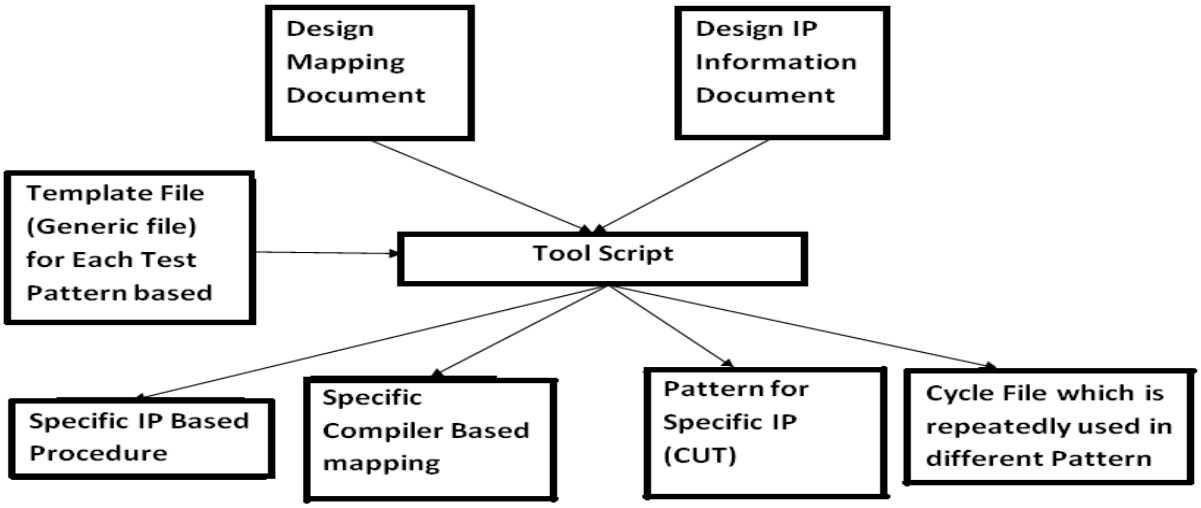

Figure 5.3: Tool Structure

Tool is generated mapping file which is related to compiler of Memory. Pattern Algorithms Pins which are specific memory IP pins. Mapping file used #define mapping_pin TOP_PIN (Processor directive) for test patterns.

#define mapping_pin TOP_PIN

- Here Design Mapping Document, First column is TOP level Pins.
- Second, Direction of pinto respective of TOP level which defines circuit description file of Test chip
- Third column is Memregbank Pin. Memreg pin is memblock level register bank pin used to tie with memory IP pin which is not going to TOP Level.

TOP PIN	DIRECTIO	REGISTER PIN	TOP REG CYCLE	REGMEM CYCLE	CIRCUIT RESET	CIRCUIT R	SP DMT MODE DEFAULT	SP DMT MODE MAPPING	DPREG DMT MODE DEFAULT	DPREG DMT MODE MAPP
CUTSEL_0	INPUT	N/A	0	0	0	0	N/A	SP_WORDSEL_0	N/A	DPREG_WORDSEL_0
CUTSEL_1	INPUT	N/A	0	0	0	0	N/A	SP_WORDSEL_1	N/A	DPREG_WORDSEL_1
CUTSEL_2	INPUT	N/A	0	0	0	0	N/A	SP_WORDSEL_2	N/A	DPREG_WORDSEL_2
CUTSEL_3	INPUT	N/A	0	0	0	0	N/A	SP_WORDSEL_3	N/A	DPREG_WORDSEL_3
CUTSEL_4	INPUT	N/A	0	0	0	0	N/A	SP_WORDSEL_4	N/A	DPREG_WORDSEL_4
CUTSEL_5	INPUT	N/A	0	0	0	0	N/A	SP_WORDSEL_5	N/A	DPREG_WORDSEL_5
BLOCKSEL_0	INPUT	N/A	1	0	0	0	1	SP_CTRL_0	1	DPREG_CTRL_0
BLOCKSEL_1	INPUT	N/A	0	1	0	0	1	SP_CTRL_1	1	DPREG_CTRL_1
CTRL_13	INPUT	N/A	0	0	0	0	N/A	SP_CSN	N/A	DPREG_WCSN
CTRL_14	INPUT	N/A	0	0	0	0	N/A	SP_WEN	N/A	DPREG_WEN
CTRL_2	INPUT	N/A	0	0	0	0	0	N/A	0	N/A
CTRL_3	INPUT	N/A	0	0	0	0	0	N/A	0	N/A
CTRL_4	INPUT	N/A	1	1	1	0	1	SP_RESET_1	1	DPREG_RESET_1
CTRL_5	INPUT	N/A	0	0	0	0	0	N/A	N/A	DPREG_RCSN
CTRL_6	INPUT	N/A	0	0	0	0	0	N/A	0	N/A
CTRL_7	INPUT	N/A	0	0	0	0	0	N/A	0	N/A
CTRL_8	INPUT	N/A	0	SPL_PIN	0	0	N/A	SP_INITN	N/A	DPREG_INITN

Figure 5.4: Design Mapping Documents

- Fourth and Fifth columns are Reset high and Reset low when used in initial cycle. These column is defined here because sometimes Logic high and logic low of reset is used so whatever values are given here their value reflect in reset cycles.
- Fifth cycle is Default value of particular cycle which is constant for cycle.
- Sixth cycle is Mapping name of particular cycle and compiler. Mapping name and default values are changed with compiler so columns are added for compiler of one cycle.
- Every Mode and Compiler has Default and Mapping file. DMT Mode cycle with one compiler has own column.
- E.G. SP_DMT_MODE_DEFAULT_CYCLE, SP_DMT_MODE_MAPPING_PIN

BLOCKSELECT	IPSELECT	CUT_num	Addrs	Q_bits	CUT_type	Address_b	Word_sele	DMT_MODE
`0000_0000_0000_0000_0000_0000_0000_0010	1	4	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	2	60	512	288	DPREG	9	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	3	95	8192	80	DPRAM	13	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	4	3	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	5	59	512	288	DPREG	9	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	6	94	8192	80	DPRAM	13	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	7	97	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	8	123	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	9	1	64	4	SP	6	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	10	2	2048	4	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	11	5	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	12	6	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	13	7	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	14	56	16	8	DPREG	4	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	15	57	16	288	DPREG	4	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	16	58	512	8	DPREG	9	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	17	91	32	80	DPRAM	5	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	18	92	2048	4	DPRAM	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	19	93	2048	32	DPRAM	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	20	96	8192	80	DPRAM	13	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	21	98	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:
`0000_0000_0000_0000_0000_0000_0000_0010	22	124	2048	160	SP	11	5	CHECKER:CHECKER_PIPE:

Figure 5.5: Design IP information Documents

- Here Design IP Information Document, First column is BLOCKSEL[31:0] Register value.
- Second column is IPSEL[31:0] Register value which is index of CUT that enables CUT, contains Memory IP and third column is CUT number which gives their CUT Name.
- Fourth and Fifth column are Address range and input/output bs of Memory IP.
- Sixth Column is Compiler of Memory which is used to select pattern template.
- Seventh Column is Address bit used for Memory IP.
- Last column is list of Pattern that which Patterns want to generate.

5.3 Feature of Tool

- Less Time consuming to generate test patterns. Design Mapping and IP information CSV are going to make in one hour.
- Tool takes time to generate test pattern are only 10 min.
- Tool with Sanity Checks, any undefined format of input is not acceptable, flash ERROR and Quit to process.
- Test Pattern template make and once verify on silicon wafer then after assurance that these patterns have not any bug so QUALITY of TEST PATTERNS are improved very much.
- STMicroelectronis has tool which convert these test patterns to verilog file which used for simulation and validation purpose so Validation of RTL and NETLIST is very quick and easy.

5.4 Future Work FOR TOOL

- To maintain the Template of Test Patterns.
- Make Tool useful for BIST AND BISC MODE right now only DMT MODE Patterns are generated.

Chapter 6

Work Contribution and Result

- Developed Tool Pattern Generation Tool
- Making Test Pattern for the Test Chip
- Automation for Design Flow to reduce time for tape out used SHELL and PERL Script
- Modification of Verilog Memory Behavioural Code
- Validation of RTL and NETLIST design

6.1 Validation Flow

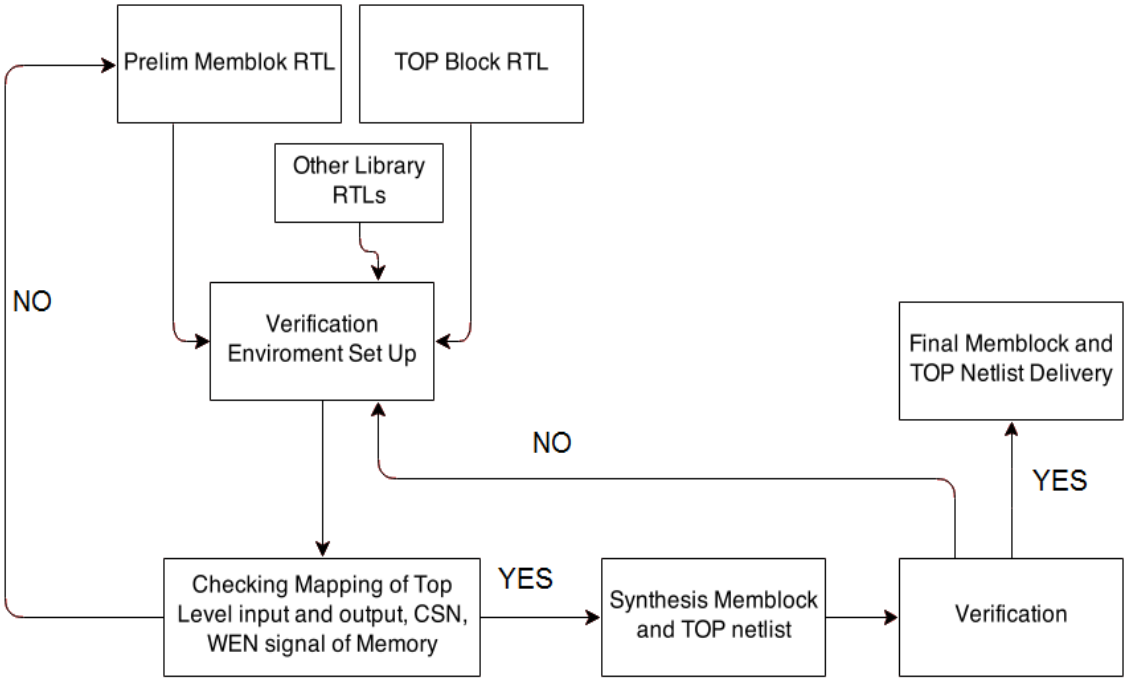

Figure 6.1: Validation Flow

6.2 Simulation Graphs

6.2.1 Memory IP Write

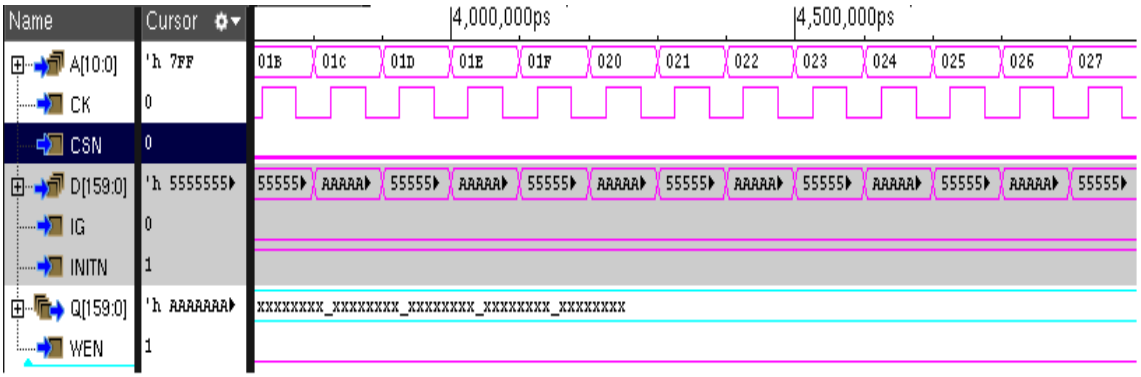

Figure 6.2: Memory Write at Memory IP Level

6.2.2 Memory IP Write

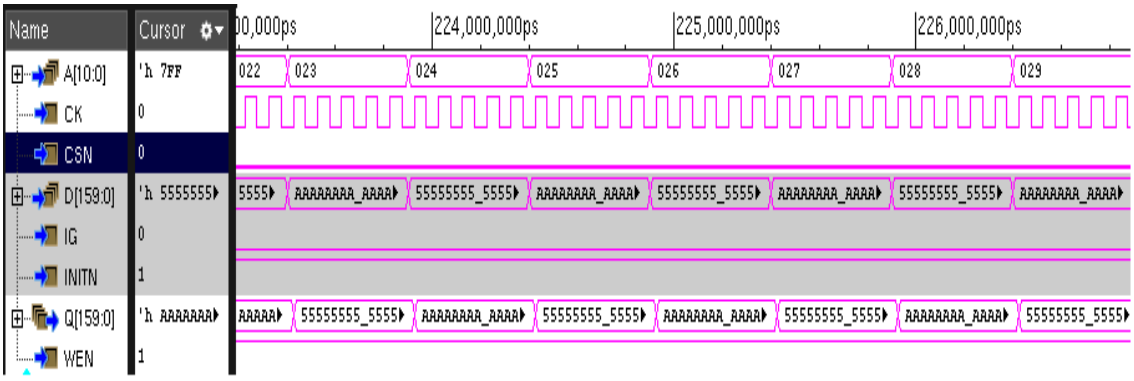

Figure 6.3: Memory Read at Memory IP Level

6.2.3 Memory Write from TOP

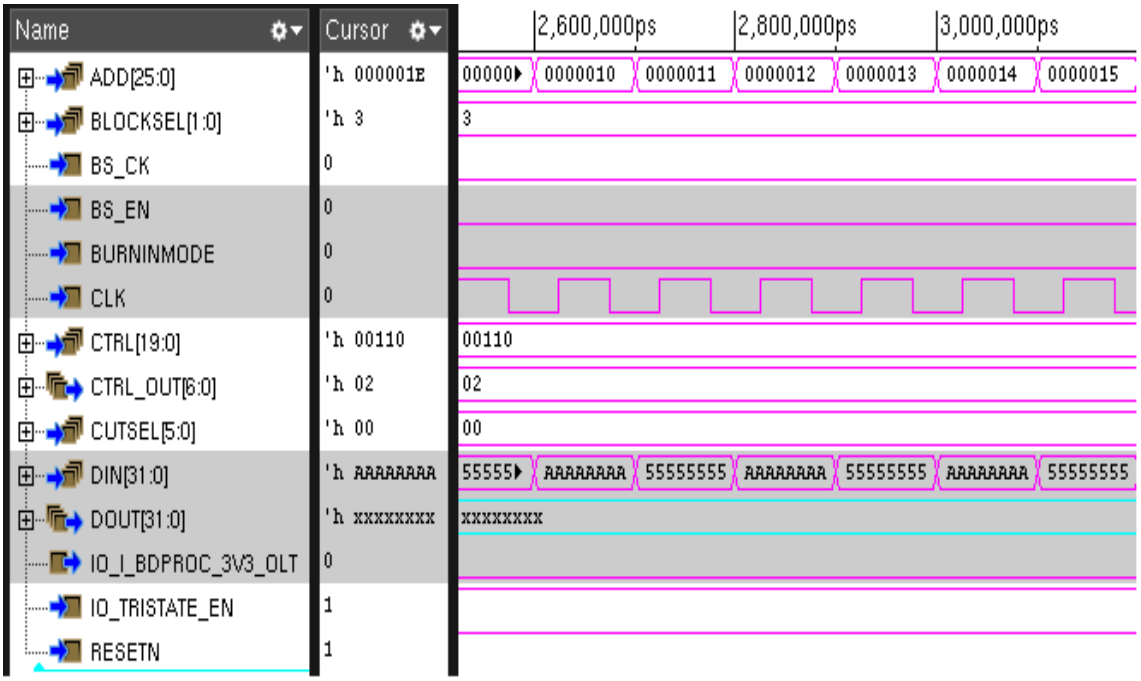

Figure 6.4: Memory Write at TOP Level

Here,CSN,WEN are CTRL_13 and CTRL_14 pins. CLK pin is operating clock for memory.CTRL_0 is READ Clock for DPREG/DPRAM Memory.

6.2.4 Memory Read from TOP

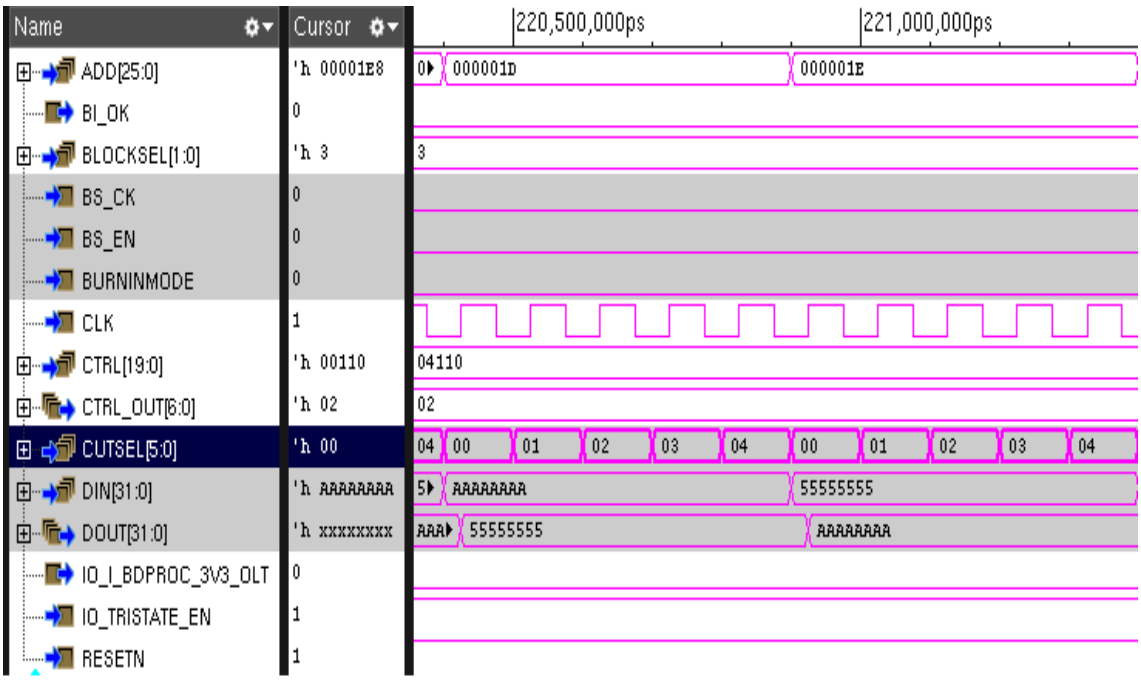

Figure 6.5: Memory Read at TOP Level

Here,Outword Pins fetch out memory output irrespective of width of Output bus. When OUTWORD is 0,first 32 output data is fetched out. When OUTWORD is 1, Second 32 bits are fetched out and so on....

Chapter 7

Tools

- Incisive unified simulator (IUS)
- Shell Scripting

7.1 Incisive unified simulator

Incisive is a suite of tools from Cadence Design Systems related to the design and verification of ASICs, SOCs, and FPGAs. Incisive is commonly referred to by the name NCSIM in reference to the core simulation engine. Depending on the design requirements, NCSIM has many different bundling options of the following tools.

7.2 Shell Scripting

A shell script is a computer program designed to be run by the Unix shell, a command line interpreter. The various dialects of shell scripts are considered to be scripting languages.It uses for automation, text and file manipulation.

Tool	Command	Description
NC verilog	ncvlog	The NC-Verilog compiler performs syntactic and static semantic checking on the Verilog HDL design units (modules, macro modules, or UDPs). If no errors are found, compilation produces an internal representation for each HDL design unit in the source files.
NC VHDL	ncvhdl	The NC-VHDL compiler performs syntactic and static semantic checking on the input source files or VHDL design units. If no errors are found, compilation produces an internal representation for each HDL design unit in the source files.
NC Elaborator	ncelab	Unified linker / elaborator for Verilog and VHDL. The elaborator constructs a design hierarchy based on the instantiation and configuration information in the design, establishes signal connectivity, and computes initial values for all objects in the design.
NCSim	ncsim	Unified simulation engine for Verilog and VHDL. Loads snapshot images generated by NC Elaborator. This tool can be run in GUI mode or batch command line mode. In GUI mode, ncsim is similar to the debug features of Modelsim.
Sim Vision	simvision	SimVision is a unified graphical debugging environment for Cadence simulators. One can use SimVision to debug digital, analog, or mixed-signal designs written in Verilog, SystemVerilog and VHDL.

Figure 7.1: IUC Command

Conclusion

- Testchip provides necessity post-silicon validation data before any mass production of SOC and also ensure maturity any technology library.
- Test patterns are cycle based patterns which give advantage of less time for testing and implementation reusability of cycle.
- Test Patterns are similar algorithms except minor modification needed so automation tool is developed which have improved test patterns quality and less human interruption.
- Tool , reduced human efforts , is developed test patterns which untimely time saving and used in validation of RTL and Netlist in early days of Design.

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