Standard Cell Characterization And Packaging

Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Ardeshana Gauravkumar P.

(12MECV33)

Department of Electronics & Communication Engineering

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Nirma University

Ahmedabad-382 481

May 2014

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Declaration

This is to certify that

1. The thesis comprises of my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

2. Due acknowledgement has been made in the text to all other material used.

Ardeshana Gauravkumar P.

CERTIFICATE

This is to certify that the Major Project entitled **"Standard Cell Characterization And Packaging"** submitted by **Mr. Ardeshana Gauravkumar P. (12MECV33)**, towards the partial fulfillment of the requirements for the degree of **Master of Technology in VLSI Design** of **Nirma University of Science and Technology, Ahmedabad** is the record of work carried out by him under our supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for the examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Abstract

Standard cells are basic building blocks for ASIC (Application-Specific Integrated Circuit) design. Semi-custom design flows are a key factor for the rapid growth of integrated circuits and systems. They lower the design complexity through the use of pre-designed and pre-characterized functional components called standard cells, instead of assuming that designers have to draw, place and connect each transistor. Cell Characterization is the process of simulating a standard cell with a spice simulator (like ELDO) and an automated characterization tool to extract this information and convert into a format that other tools can utilize.

Using spice ELDO (Mentor Graphics tool) simulator timing, power & noise information is extracted for each cell. All this data has to be consolidated in a library (in Synopsys Technology Format) along with some important views & documentation in form of a package. The libraries are used by synthesis tools for extracting gate level netlist of the digital circuit from RTL level design & these are also used in place and route tools.

In the initial phase of my dissertation work, I understood the working of tools (like ELDO, Automatic Library Tool etc.) and the flow for characterization & packaging. I will also learn the methodologies used to evaluate timing, power, constraints & noise parameters. In the second phase, standard cell characterization & packaging will be done for nanometer Technology designs for different libraries. The impact of various parameters such as Threshold voltage, Process, Temperature, Drive Strength, Body Biasing and Gate Length on standard cell is analyzed.

The prime focus in this work is firstly to characterize (extract timing, power, noise information) set of standard cells at various PVT (Process, Voltage, Temperature) corners for a fixed set of input slopes & load capacitances and compare it with previous technology, secondly to consolidate the characterized data of each cell in a .lib (Synopsys Technology Format) also including some important views (Back end, Front end, Packaging, etc.) in a package that is later used by SOC designers.

ST Microelectronics At A Glance

- A world leader in providing the semiconductor solutions that help our customers improve quality of life for everyone, both today and in the future
- Among the world's largest semiconductor companies
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- A leading technology innovator (around 12,000 researchers approx. 21,500 patents)
- Key strengths in Multimedia Convergence, Power Applications and Sensors
- Rich, balanced portfolio (ASICs, Application-Specific Standard Products and Multi-Segment Products)
- A pioneer and visionary leader in sustainability
- President and CEO: Carlo Bozotti
- 2011 revenue $9.73 billion
- Approximately 50,000 employees including STEricssion at December 31, 2011
- Advanced research and development centers in 10 countries
- 12 main manufacturing sites
- Corporate Headquarters Geneva, Switzerland

- Global presence with sales offices all around the world
- Public since 1994 - shares traded on New York Stock Exchange (NYSE: STM), Euronext Paris, and Borsa Italiana
- Created as SGS-THOMSON Microelectronics in June 1987, from merger of SGS Microelettronica (Italy) and Thomson Semiconducteurs (France)
- Renamed ST Microelectronics in May 1998

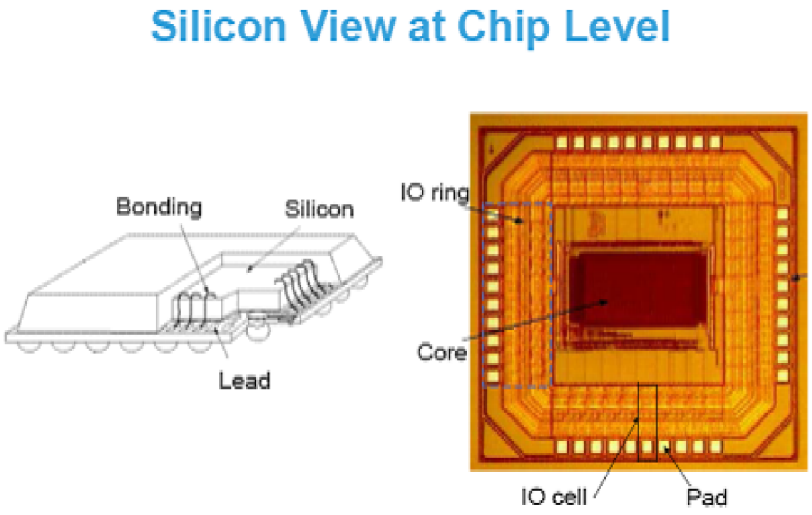
Group Introduction

The TR&D is a group in ST which works on integrated products (IPs). Its work is to provide quality Library Solutions and services to divisions, in the company's drive in time to market, IP Reuse and Super Integration. There are various types of IPs:

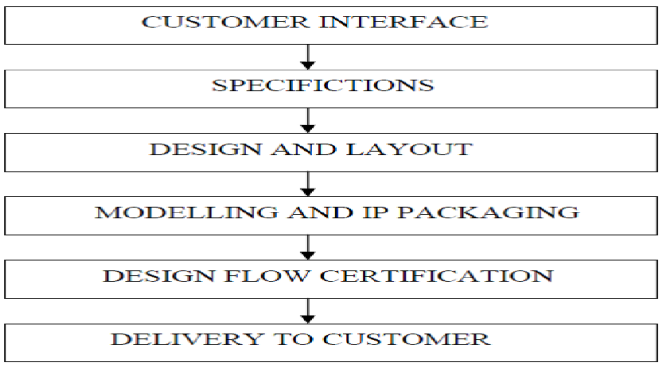
- Digital Design : It is the layout of basic sequential and combinational circuits which are used to make bigger circuits. It is the basic building block of all the circuits. It is a component within an integrated circuit with known functional and timing characteristics, which can be used as an element in building a larger circuit. Example of standard cells include Inverter, Flip-flop (FD), Latch (LD), Multiplexer (MUX), NAND, NOR, AND, OR, XOR, XNOR, Full Adder (FA), Half Adder (HA).

- Memories : A device or an electrical circuit used to store a single bit (0 or 1) is called a memory cell. Examples of memory cell are flip flop, a charged capacitor etc. Semiconductor memories are capable of storing large amount of Digital information. The amount of memory required in a particular system depends on the type of application but the no. of transistors required for storage of data are always much larger than the no of transistors used for logic operations and other purposes. The ever increasing demand of high storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently towards higher data storage densities.

- I/Os (input/output cells) : I/O's are the input/output cells, placed on the periphery of the chip. Any I/P signal which comes from off-chip environment (external voltages are at a typical voltage Vdde level of 2.5V, 3.3V or 5V) is connected to the core (logic part of the chip) is connected through them and vice versa.



- Developement Flow : The customer, as per his requirements, gives the specifications to the flow team. These requirements are analyzed and as the needs, the features required for the design are noted. These are sent to the Back End Team for the designing. After the design is ready, it is checked for the specifications and then sent to the Front End for the characterization and functional modeling.



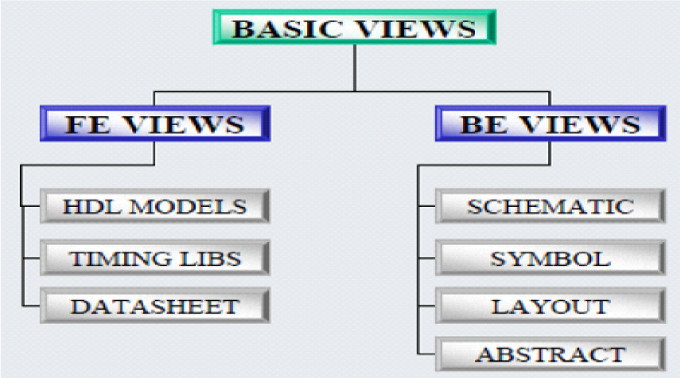
- Concept Of Library : A library is collection of cells all of which reference the same technology file. The cells are the smallest functional unit. Attached to every library is a technology file. A technology file is a large data file that specifies, in one central location, all of the technology-dependent parameters

associated with that particular library. The purpose of library is to reduce the design cycle of the designer.

- Basic building blocks: Digital (AND, OR); Analog (amplifier).
- Complex building block: Digital (Microcontroller); Analog (PLL, DAC).
- Memories: Single or dual port SRAM, ROM etc.

The cells are delivered as a set of different views. These views are used by different tools in a given Design flow. These cells are used until the physical implementation.

- Cell Views : A particular representation of a cell is referred to as a view. Each cell may have a layout view, schematic view, symbolic view, timing view, etc. Each view object has attached property objects that are specific to the view, such as grid units, scale and display of axes etc. A cell is delivered as a set of view and each view is used by a different tool in a given design flow.



- BE (Back End) VIEWS: Views Related to the Physical Design of a Cell
- FE (Front End) VIEWS: Views Related to the Timings/Modeling of the Cell the various views can also be classified as Primary and Secondary views.

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Chapter 1

Introduction

1.1 Standard Cell

RTL design into a large collection of lower-level constructs called standard cells. A Standard Cell is a group of transistor and interconnect structures that provides a Boolean logic function (e.g. AND, OR, XOR, XNOR, inverter, buffers) or a storage function (flip flop or latch). The simplest cells are direct representations of the elemental NAND, NOR and XOR Boolean function, although cells of much greater complexity are commonly used (such as 2-bit full adder). They are logic units of any digital circuit of same geometry (same height). Standard cells usually come in libraries for a specific technology. The standard cells are typically specific to the planned manufacturer of the ASIC.

1.1.1 Standard Cell Views

A cell has number of inherent properties/attributes. These include its name, owner, creation time and access privileges. Similarly each view has inherent attributes. Each view object has attached property objects that are specific to the view, such as grid units, scale and display of axes etc. The following various views include.

1.1.1.1 Schematic View

A schematic view includes component instances, wires and pins. A component instance represents lower level of abstraction in the design. Component instances are generally the instances of symbol view of the cell. An instance is identified by the cell it represents and the instance name. Pins are the inputs and outputs of the schematic.

1.1.1.2 Symbol View

Symbol graphics define what we will see when this symbol is used in the schematic. The shape of the symbol can indicate the cells function. Labels in the symbol are used to add to the documentation of the design.

1.1.1.3 Abstract View

Abstract view gives information about the metal layers running in the layout view. This view is useful while routing. Routing is an activity in which we put set of cells adjacent to each other and provide interconnection between them and the power and ground rails.

1.1.1.4 Layout View

Layout view is the actual physical description of the chip that goes on the silicon. We use different layers in a cad environment to draw the physical structure keeping in mind a set of rules that need to be followed.

1.2 Standard Cell Library

A standard cell library is a consolidated data used in designing a SOC (system on chip). It is a collection of low level logic functions such as AND, OR, Inverter, flip-flops, latches and buffers. These cells are realized as fixed height variable width

full-custom cells. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. The cells are typically optimized full custom layout, which minimize delay and area.

There are various types of standard cell libraries, some of them are described below :

1. **Core Library :** These libraries contains basic/core standard cells such as AND, OR, MUX, Flip-Flop, Adder, etc.

2. **High Performance Core Library :** These are the core library which are specially generated for high performance applications.

3. **Clock Library :** These library are used in clock network. They contain cells such as Inverter, Buffer, etc.

4. **Placement and Routing Library :** They are used in placement and routing purpose. They contains filler cells (used for filling empty areas to maintain minimum area requirement), decoupling capacitor cells (used to maintain required supply to different cells) and protection cells such as diode (used for protection purpose).

5. **Shifter Library :** Contains level shifter cells which can be used for shifting level of a signal while going from one power domain to another.

1.3 Standard Cell Based ASIC Design

It is the most common ASIC development technology. Each standard cell vendor has its own library of circuits that range from primitive logic gates to more complex functions Based on the customer's design. ASIC vendors provide a library of pre-characterized cells that the customers can use to implement their design.

The resulting collection of standard cells, plus the needed electrical connections between them, is called a gate-level Netlist. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. The gate-level netlist is next processed by a placement tool which places the standard cells onto a region representing the final ASIC. The required circuits are placed on the chip and connected using "place-and-route" software. It attempts to find a placement of the standard cells, subject to a variety of specified constraints. The routing tool takes the physical placement of the standard cells and uses the netlist to create the electrical connections between them. Given the final layout, circuit extraction computes the parasitic resistances and capacitances. In the case of a digital circuit, this will then be further mapped into delay information, from which the circuit performance can be estimated, usually by static timing analysis. This, and other final tests such as design rule checking and power analysis (collectively called signoff) are intended to ensure that the device will function correctly over all extremes of the process, voltage and temperature.

When this testing is complete the information is released for chip fabrication. This report addresses the various issues come into sight while developing a cell library.

Advantage :

- It provides the best design flexibility.
- High performance and High density.
- Low power consumption.

Limitation :

- With smaller geometries, the mask costs have increased exponentially and fabrication turnaround time has become longer.
- Not economically viable except for very large volume production.

1.4 Why Create Libraries?

There are following main reason for create standard cell library :

- Complexity of the design is continuously increasing.
- Full-custom design is no longer feasible.
- Use of synthesis and Placement and Route (PNR) tools have become mandatory.
- PNR tools need layout of library .
- Synthesis tools need logic models of the cells in the layout library, which includes timing and power dissipation models.

1.5 About Project: Standard cell characterization

Standard cell characterization is a process of simulating a standard cell with an analog simulator (like ELDO) to extract cell information such as delay, power dissipation, etc and convert into a format that other tools can utilize. Characterization requires adequate logic, timing, power consumption for each cell in the library. Cell characterization can be completed by analog simulation using SPICE simulator, whose output can be given to automated tool like Advance library tool(ALTO) to arrange or tabulate the timing characterization data in a specific format that the other tools can understand. The automated tool uses an analog simulator to simulate the design and wrap up a nice interface to automate the process and give the results in standard Synopsys Technology format. So, this generated set of high quality models, accurately and efficiently define cell behavior.

These models are used by several digital design tools for different purpose like:

- Synthesis tool

- Placement and Routing tool
- Hardware Description Language (HDL) simulators (Verilog and VHDL).
- Floor planning tools
- Physical Placement Tools
- Static Timing Analysis (STA) tools
- Power analysis tools
- Format verification tools
- Automatic test program generation (ATPG) tools
- Library compiler

1.6 Packaging

Once the set of standard cells are characterized, timing, power and noise information is extracted for each cell. All this data has to be consolidated (in a library of STF) along with some important views and documentation in the form of a package. This product (package) is then used by designer for designing ASIC chips. The libraries are used by synthesis tools for extracting gate level netlist of the digital circuit from RTL level design & these are also used in place and route tools. Figure 1.1 shows different views that are generally included in the product.

There are some primary views (common to different tools) & secondary views (derived from primary) are present in the library:

- Timing views include .lib, primetime mapping file (for mapping and back annotation).
- Physical views which include .cdl (circuit description language), .spi (spice parasitic information), gds.

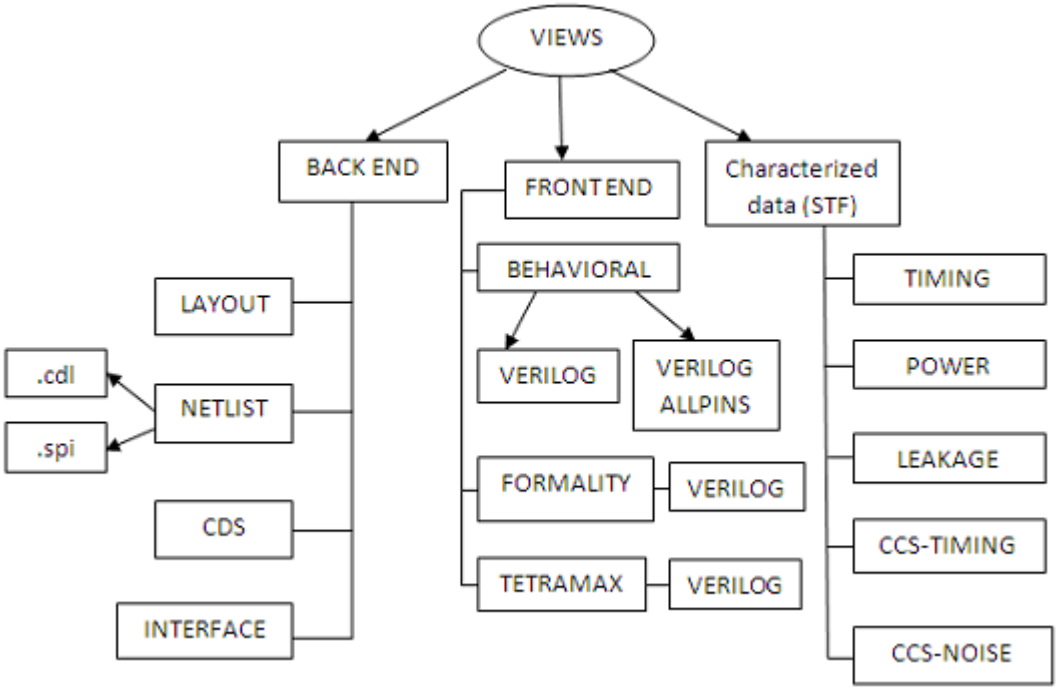


Figure 1.1: Different views in library

  - CDL : Circuit Descriptive Language is a derived textual view of a schematic. CDL file describes connectivity at the transistor level. It comprises of the logical elements (primitives). Every type of primitive logic element called by the schematic must have a corresponding sub circuit definition in CDL.
  - SPI : Spice Parasitic Information is a derived textual view of a layout. It contains all the devices, parasitic, etc. extracted from the layout view, including the MOSFETS, resistances, capacitances etc.

- Behavioral views which includes verilog and vhdl views. Verilog views include .v, .v_allpins (this includes supply pins in every cell module), Synopsys formality view, hdl emulator views and Synopsys tetramax views.
- Documentation which includes release notes, KPS (Known Problems and Solutions), user manual and datasheets on various operating conditions.
- Packaging views which include .ptbl, .info, .libinfo and vc.bbview files.

1.7 Organization of the Dissertation Report

In this work, it is described how to characterize standard cells and generate libraries (.lib in STF) that contains their timing and power information. Moreover, this will briefly describe how packaging of all this data in the form of a product is done. Chapter II briefly describes the measurement methodologies that are required to calculate timing, power, input capacitance, timing check measurement, etc. It also describes the necessary requirements prior to the characterization process. This chapter will also explain about novel delay calculation methods being used for higher accuracy delay results. Chapter III describe about the MOSFET technology and FD-SOI technology, also compare both technology and explain about the advantage of the FD-SOI. Chapter IV describe about the tools which is used for characterization. Chapter V present the characterization results and the impact of various parameters such as Threshold voltage, Process, Temperature, Drive Strength, Body Biasing and Gate Length on standard cell. Chapter VI describe the conclusion the future scope.

Chapter 2

Measurement Methodology

2.1 Introduction

Characterization is a process of exhaustively analyzing an entity at a low level of abstraction to extract all relevant and meaningful information about it, and then to faithfully represent that information in a model at a higher level of abstraction. The measurements done on library cell are as follows :

- Input Capacitance
- Propagation Delay
- Power (leakage, internal)
- Output Transition i.e. slope
- Constraints (Setup, Hold, Pulse Width, Recovery, Removal)

Apart from above, following checks are also performed :

- Functional check (during pre-characterization)
- Glitch check (during characterization)
- Rebound check (during characterization)

The fully characterized data extracted from the library is then transformed into a standard library file i.e. Synopsys Technology Format (STF) file in .lib format. The STF has a standard representation for different cell attributes.

2.2 Pre-characterization

Before characterization, pre-characterization is done. In this step functional verification of the cells in library is done. Pre-characterization is performed at single PVTSC (process, voltage, temperature, input slope, load capacitance).

Thus if there is problem with the functionality of the cell, it can be detected at this stage instead of detecting it after performing characterization for all PVTSC conditions which is time consuming.

2.3 Characterization Flow

1. **Netlist Extraction**

   Transistors, capacitors and resistors are extracted with the help of special tools and saved as spice netlist.

2. **Parameters Specification**

   Library parameter are specified in library specification file which contain all the necessary library related attributes like

   - PVT Corner Selection (Process, Voltage, Temperature)
   - Unit Definition
   - Threshold Values (Time, Capacitance, Slope)
   - Limits (Max output load, Max transition time)
   - Tolerance (Glitch, Peak, etc.)
   - Supply Voltage Definition

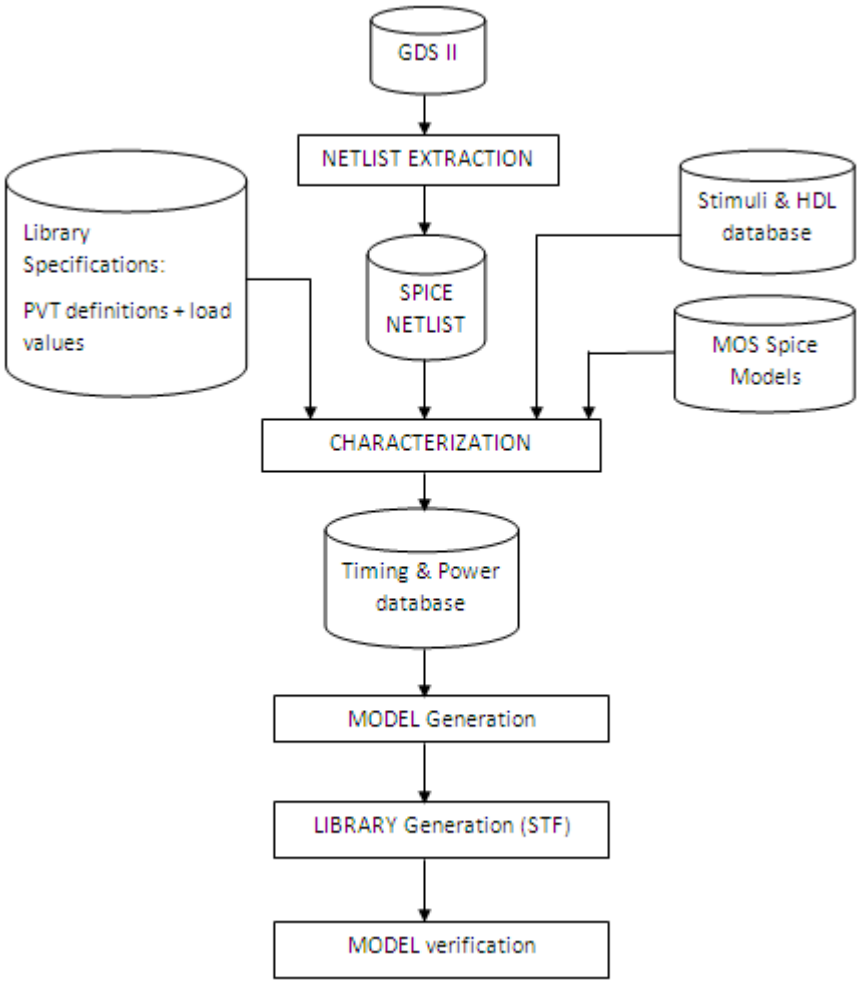


Figure 2.1: Characterization Process Flow

- Slope (input slope) and Cload (load capacitance) Definition
- Miscellaneous attributes like Power extraction units, simulation commands, name off views to be generated etc.

3. **Measurement**

   The cells are simulated with ELDO simulator to obtain the required data like Delay, Slope and Power for all the PVTSC corners as specified in library specification file.

4. **Model Generation**

   The obtained data is fed into the models and libraries in STF format are generated.

5. **Verification**

   Different checks are performed to ensure the correctness of the characterization. The standard cell libraries are fully characterized at different PVTSC corners to validate the design over wide range of Temperature, Voltage and Slope conditions.

2.3.1 PVTSC

These are the characterization corners decided by the customer and come as a specification for the design where,

P = Process like Best, Worst and Nominal :

- Best Case (bc) - Where the threshold voltage of the MOS is low. This means that the transistors will switch quickly and hence power dissipation will be more. Delays from input to output will be less.

- Worst Case (wc) - Where the threshold voltage of MOS is high. This means that the transistors will not switch quickly and hence power dissipation will be low. The delays from input to output will be more.

- Nominal Case (nom) - Where the threshold voltage is between the best case and worst case.

V = Voltage like 1.8V, 1.32V

T = Temperature like $-40°C$

S = Input Slope like 0.375ns, 0.485ns

C = Output Load like 1.2pf, 0.342pf

2.4 Thresholds used for characterization

For the library characterization, various thresholds values needed to be specified in library specification file, which includes slope threshold and timing threshold.

(a) Slope threshold

The slope thresholds that are defined for the library are the thresholds for which output slope is measured. The output slope cannot be measured between 0 - 100% as the result will be too pessimistic. The slope thresholds must be defined so that the linear part of the output slope is taken.

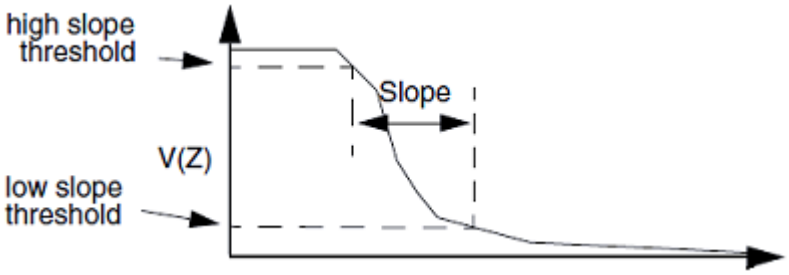


Figure 2.2: Slope Threshold[5]

(b) Timing threshold

Timing thresholds are used to measure propagation delay, timing checks and pulse measurements. Generally, delay is measured as 50% of transition at the input (50% of VDD) to 50% of transition at the output (50% of VDD). But many times gate shows different responses for rising and falling edges of input so, different timing thresholds for rising and falling edges used for more accuracy.

The output signal transition time depends on RC time constant (τ) of the discharge circuit. The charge accumulated on the output load (C_{load}) of the inverter is discharged through the on resistance of the NMOS (R_{on}). The RC time constant (τ) is defined as,

$$\tau = R_{on} \times C_{load}$$

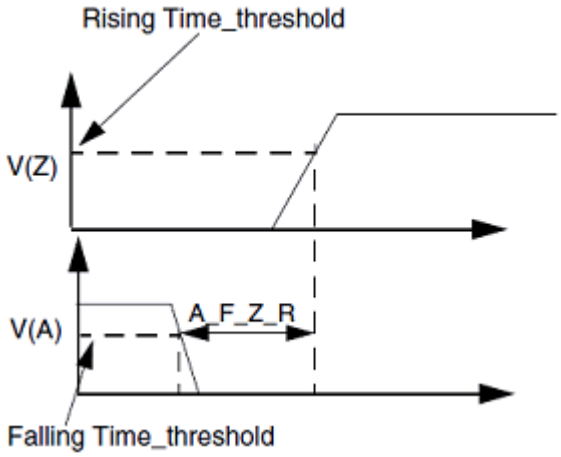


Figure 2.3: Timing Threshold[5]

So, the output rise transition depends on the input signal transition time (slew) and the output load (C_{load}) of the inverter. A similar argument can be made for a fall transition of the signal. The total effective load at the output pin of a gate is due to the on resistance of the driver cell, interconnect impedance and input impedance of the receiver cell. The effective output impedance of an inverter will have a contribution of the resistance from the output node to the VDD and VSS via the PMOS and NMOS respectively. This output resistance of the inverter is very high as compare to the interconnect resistance in higher technology nodes. Thus the resistive component of the interconnect can be ignored, and this will introduce a negligible error in delay calculation. Also note that due to very small dimension of the interconnect, the inductance of the interconnect is small. In a low frequency circuit, the equivalent impedance due to this inductance is very small in comparison with the equivalent impedance due to the resistance and capacitance of the interconnect and can be ignored.

The timing thresholds are used for propagation timings, timing checks and pulse measurements. The time threshold is the input VDD value for which the output starts changing its value. In standard cell libraries, this value is given in percent of VDD. For a given technology, same threshold values are kept for all cells of all

libraries. A timing arc appears when a transition at the input of the cell generates transition at the output, for example: A_R_Z_F means rise transition on the input pin A causes a fall transition on output pin Z.

For the timing arcs, the output slope and delay characterized for different couples of input slopes and output loads are provided. The results are two dimensional output slope and delay tables. Delay is measured by using timing threshold while the slope can be measured using the slope threshold.

2.5 Timing characterization - Delay models

Various methodologies have been proposed to model the gate behavior for the delay estimation. Traditionally, the Non - Linear Delay Model (NLDM) has been used for delay estimation. However due to increase in frequency and device shrinking, the relative error introduced by NLDM is no longer acceptable. The various improved modeling schemes have been proposed. The Composite Current Source (CCS) and Effective Current Source Model (ECSM) are well known industry standard modeling schemes.

1. **Non - Linear Delay Model :**

   NLDM is traditionally used modeling scheme, in which gate delay is modeled using look up tables. If the resistive component of the impedance is neglected from the effective load of a cell, then the delay is dependent on two parameters i.e. input signal slew and output effective capacitive load (for a specified Process, Voltage and Temperature (PVT)). The MOSFET behavior depends on the input signal transition i.e. rise transition and fall transition. In NLDM, cell delay is modeled in a two dimensional lookup table for each transition as shown in table 2.1. Here S_{in} is the input signal slew, C_{out} is the effective output capacitive load of a cell and t_{delay} is the gate delay.

   These gate delays are obtained from multiple SPICE simulations for every

Table 2.1: NLDM based cell delay (t_{delay}) lookup table

Input Signal Slew	Effective Output Capacitance		
	C_{out1}	C_{out2}	C_{out3}
S_{in1}	t_{delay}	t_{delay}	t_{delay}
S_{in2}	t_{delay}	t_{delay}	t_{delay}
S_{in3}	t_{delay}	t_{delay}	t_{delay}

set of S_{in} and C_{out}. Since lookup table contains only a small set of S_{in} and C_{out}, interpolation or extrapolation are required to evaluate t_{delay} and S_{out}. Being a very simple lookup table, NLDM makes delay calculations very fast at the cost of less accuracy. The primary cause of accuracy loss is due to interpolation, process variation, on chip variation, and complex behavior of MOSFET at the smaller technology nodes.

Several more advanced modeling techniques have been developed in which the complex behavior of the cell and the signal waveforms can be captured more accurately. These advanced modeling schemes reduce relative error in the delay calculation. The Composite Current Source (CCS) model from Synopsys and the Effective Current Source Model (ECSM) from Cadence are the most well known industry standard modeling schemes of this type.

2. **Composite Current Source model :**

Similar to NLDM, characterization in a CCS model is also carried out with a small set of combinations of input signal slew and output effective capacitance load. However, in contrast with NLDM, CCS contains the output current waveform in the lookup table. Here $I_{out}(t)$ is the output current waveform. It is represented by a set of output current and time values. In the library file, two vectors are used to store simulation time and corresponding output current value for every pair of S_{in} and C_{out}.

In contrast with NLDM, CCS does not define gate delay values for a given set of input signal slew and an effective output capacitive load. Instead of this

Table 2.2: CCS based output current waveform ($I_{out}(t)$) lookup table

Input Signal Slew	Effective Output Capacitance		
	C_{out1}	C_{out2}	C_{out3}
S_{in1}	$I_{out}(t)$	$I_{out}(t)$	$I_{out}(t)$
S_{in2}	$I_{out}(t)$	$I_{out}(t)$	$I_{out}(t)$
S_{in3}	$I_{out}(t)$	$I_{out}(t)$	$I_{out}(t)$

CCS has output current waveform which needs to be processed to extract the delay values. The inaccuracy introduced by the current waveform interpolation in CCS is smaller than the inaccuracy introduced by the delay and slew interpolation in NLDM.

3. **Effective Current Source Model :**

Effective Current Source Model (ECSM) is another well-known industry standard modeling scheme for standard cell delay measurement. In contrast with CCS, it contains output voltage waveform of the cell ($V_{out}(t)$) in look up table instead of current waveform. Similar to CCS, the voltage waveform in ECSM is represented by a set of paired voltage and time values. They are stored in the library file using two vectors, one for simulation time and another one for corresponding output voltage magnitude. The lookup table of ECSM based output voltage waveform $V_{out}(t)$ is shown in the following table 2.3.

Table 2.3: ECSM based output voltage waveform ($V_{out}(t)$) lookup table

Input Signal Slew	Effective Output Capacitance		
	C_{out1}	C_{out2}	C_{out3}
S_{in1}	$V_{out}(t)$	$V_{out}(t)$	$V_{out}(t)$
S_{in2}	$V_{out}(t)$	$V_{out}(t)$	$V_{out}(t)$
S_{in3}	$I_{out}(t)$	$V_{out}(t)$	$V_{out}(t)$

Similar to delay calculations in CCS, the output voltage waveform of ECSM needs to be processed to extract the delay values. The inaccuracy introduced by the voltage waveform interpolation in ECSM is smaller than that of NLDM.

2.6 Capacitance characterization

Capacitance characterization is calculation of input pin capacitance when transition is occurring on that particular pin. Suitable threshold value for Vdd is chosen to calculate input pin capacitance of a cell.

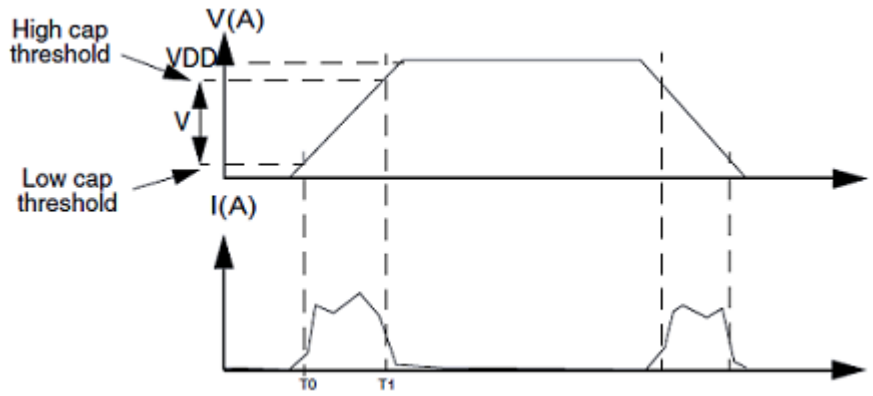


Figure 2.4: Capacitance measurement and capacitance threshold[5]

The input capacitance can be calculated using following formula,

$$C_{input} = \frac{\int_{t1}^{t2} I(t)dt}{V}$$

In standard cell libraries capacitances are provided for input and inout pins.

2.7 Power characterization

2.7.1 Power of Components :

Basically there are two types of power dissipations present in the CMOS digital integrated circuits :

1. Static Power
2. Dynamic Power

1. **Static Power**

   Static power is the power dissipated in the gate when it is not switching i.e. when it is inactive or static. This leakage is mainly because of following current components :

   - **Reverse diode leakage :** which occurs when the p-n junction between the drain and bulk of the transistor is reverse biased. The reverse biased drain junction then carries a reverse saturation current which is drawn from the power supply.
   - **Sub-threshold current :** which is due to carrier diffusion between source and drain regions of the transistor in week inversion. The amount of this leakage is significant when gate to source voltage is smaller than, but very close to threshold voltage of the device.
   - **Tunneling current through gate oxide :** SiO_2 is a very good insulator, but at very small thickness levels, electrons can tunnel across the very thin insulation; the probability drops off exponentially with oxide thickness. Tunneling current becomes very important for transistors below 130nm technology with gate oxides of 20Å or thinner.

2. **Dynamic Power**

   Dynamic power is the power dissipated when the circuit is active. A circuit is active anytime the voltage on a net change due to stimulus applied to the circuit. Since voltage on any input net can change without necessary resulting in logic transition on the output, dynamic power can be dissipated even when output does not change its logic state. So dynamic power is calculated for two cases; first when input is changing but output is stable and second when output is changing along with inputs. Dynamic power has two components :

- Internal Power

  Internal power is the energy dissipated by any cell during switching. It includes the following components :

  - Short circuit current between P and N transistors of the cell, when both of them are momentarily ON during switching.
  - Energy consumed by any internal capacitance of the cell.
  - Energy consumed due to parasitic capacitances.

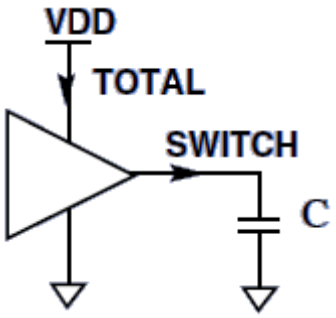


Figure 2.5: Intenergy measurement[5]

- Switching Power

  The switching or capacitive power of driving cell is the energy dissipated in charging and discharging any load capacitance at the output of the cell.

  Thus, two kinds of power information is provided in standard cell libraries :

  - Leakage: Cell static power (due to leakage currents when inputs are not switching).
  - Power: Cell power due to short circuit current from supply to ground.

2.7.2 Measurement

1. **Leakpower Measurement**

   Leakage power is the power dissipated into the cell when inputs are stable. The leakage is measured for different combinations of input pins. Usually a leakage power value for each timing arc is present in standard cell library.

2. **Intenergy measurement**

   Current is required to charge the capacitive load, during rise transition. During the transition from either '0' to '1' or '1' to '0', both the n and p transistors are ON simultaneously for a short time. It results in short circuit current from Vdd to Vss.

   With no loading, the short circuit current is quite evident. As the capacitive load is increased, the discharge or charge current starts to dominate the current drawn from the power supplies.

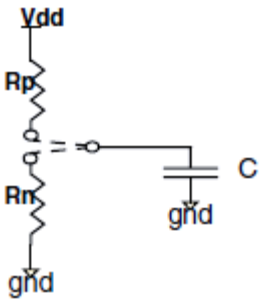


Figure 2.6: Intenergy general measurement[5]

Intenergy calculation is divided in three parts :

(a) **Total energy :**

It is the total energy supplied from the supply during transition. Total energy is calculated by integrating the current drawn from each supply over a period of time multiplied by voltage level of that supply.

Energy drawn from the supply during rising transition is U_{rising}

$$U_{rising} = \int_0^t V_{dd} * I(t)dt$$
$$U_{rising} = V_{dd} * \int_0^t I(t)dt$$
$$U_{rising} = V * Q$$
$$U_{rising} = CV^2$$

Energy drawn from supply during falling transition = 0

Hence, energy drawn from supply in complete cycle is CV^2

(b) **Switching energy :**

Out of total energy supplied from the supply some part of energy dissipated in the MOSFET, which is called as intenergy, while remaining part of energy is stored in load capacitor. This part of energy stored in load capacitor is called as switching energy.

Energy used in charging the capacitor is $E_{switching}$

$$E_{switching} = \int_0^t V(t) * I(t)dt$$
$$E_{switching} = \int_0^t V(t) * \frac{dQ(t)}{dt} \cdot dt$$
$$E_{switching} = \int_0^Q V(t) \cdot d(Q(t))$$
$$E_{switching} = \int_0^Q \frac{Q(t)}{C} \cdot d(Q(t))$$
$$E_{switching} = \frac{1}{C} * \frac{Q^2}{2} = \frac{(CV)^2}{2C}$$
$$E_{switching} = \frac{1}{2}CV^2$$

So, half of the energy supplied from the supply is used in charging the capacitive load at the output and half is dissipated in to the PMOS resistance.

(c) **Leakage energy :**

Leakpower is the static current flowing through the circuit when it is not switching. The problem is that this current also flows when the transition takes place in the circuit. We need to filter out this component from the energy because by definition, intenergy does not include static component of current.

This means intenergy is calculated by subtracting switching and leakage energy from the total energy.

2.8 Composite Current Source (CCS) modeling

2.8.1 CCS Timing

2.8.1.1 Introduction

Accurate delay calculation is critical for timing closure of complex digital designs. At 90nm and below, physical effects and design styles present new challenges for delay calculation. Top-level interconnect is becoming more resistive with narrower metal widths, resulting in cases where the interconnect impedance is much greater than the drive resistance of the driving cell. Analysis is needed across a wide range of Vdd values to support dynamic IR drop effects, and low-power design styles including voltage islands and dynamic voltage/frequency scaling. Inverted temperature dependence at low voltages requires analysis at intermediate temperature values. A delay model is needed which enables accuracy close to circuit simulation, but with fast calculation to support flat analysis of the largest designs. The model must support calculation of cell delay, interconnect delay, pin slew (also called “transition time”) and input pin capacitance for stages including detailed parasitics. This sec-

tion describes Synopsys' Composite Current Source model for timing (CCS Timing) which addresses these and future delay calculation needs.

Delay calculation is done for a stage at a time, where a stage consists of the driving cell arc, the output RC network, and the capacitance of the network load pins. The goal is to compute the response at the driver output and at the network load pins given an input slew or waveform at the driver input. See Figure 2.7 for an example of stage delay calculation. The responses are then used to determine the cell delay for the driver, and the input slews at the load pins.

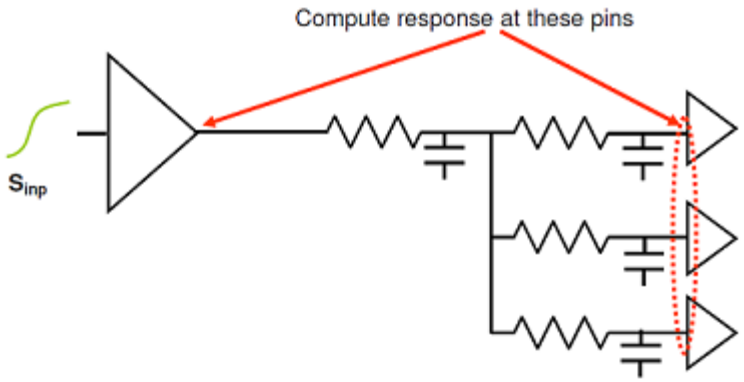


Figure 2.7: Stage Delay Calculation[3]

Previous driver models use either a time-dependent voltage source in series with a resistor (i.e. a Thevenin model), or equivalently a time dependent current source in parallel with a resistor (i.e. a Norton model). The resistor in these models is typically referred to as the "drive resistor"; it is used to express the timing arc's sensitivity to output capacitance, whereas the waveform shape itself is primarily expressed by the voltage or current source. Refinements to this type of model to account for complex aspects of transistor behavior have dealt typically with making the time-dependent nature of the voltage/current source more complex. Other approaches have tried multiple drive resistances and even arbitrary dynamic impedances.

In these models, when $R_d \ll Z_{net}$, V_{out} approaches V_{in} and the driver model can lose accuracy. There is a major limitation with conventional models when they

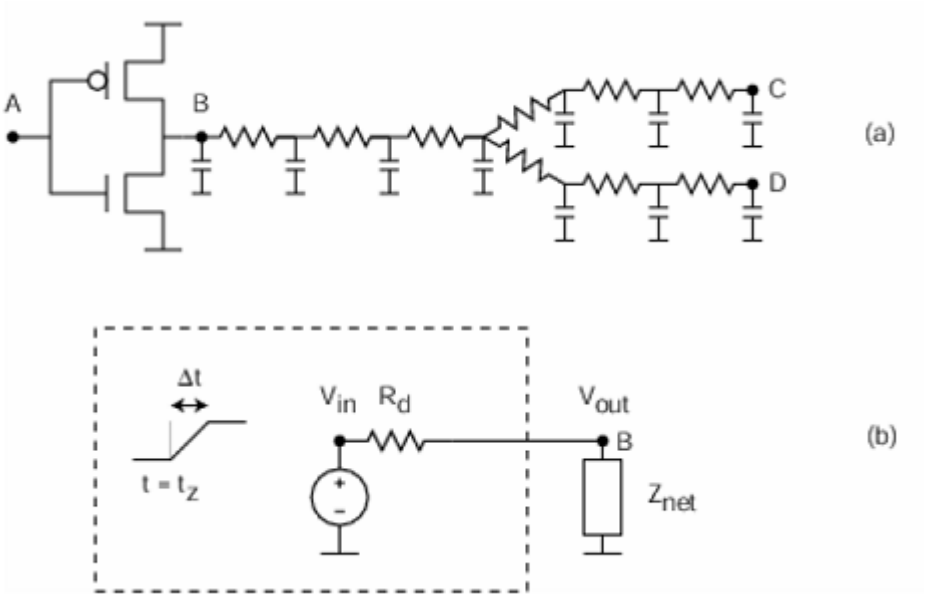


Figure 2.8: (a) shows a transistor circuit driving a detailed parasitic network at node 'B'. (b) The network presents impedance Z_{net} to the Thevenin driver model[3]

are used to drive an interconnect network with impedance Z_{net} much greater than the drive resistance R_d. Consider the Thevenin model driving a detailed parasitic network as shown in Figure 2.8.

$$\frac{V_{out}}{V_{in}} = \frac{Z_{net}}{R_d + Z_{net}}$$

which approaches unity when Rd $\ll$ Znet. This indicates that a driver model based upon a drive resistance (or arbitrary impedance) that is set independent of the network load will be ineffective in this regime. Since the transistor behavior deviates from the Thevenin voltage source nearest the power rails, this situation is typically worst when the network delay is greater than the output transition time.

The traditional receiver model is a single value of capacitance for an input pin. More recently, separate values have been allowed for rising vs falling transitions, and a min/max range has been introduced. The min/max range can bound the complex capacitance effects but this leads to pessimism during analysis.

Using a single capacitance value for the entire transition is a large source of

inaccuracy for single-stage cells where the Miller effect is significant. In such cases a single capacitance value cannot provide high accuracy for calculation of both cell delay and slew.

2.8.1.2 Characterization for CCS Timing

Characterizing a cell timing arc for CCS Timing is very similar to characterizing for nonlinear delay models (NLDM). An input stimulus is chosen to produce a specific input slew time (S_{inp}). A load capacitance (C_{out}) is connected to the output pin. Circuit simulation is run in the same way as for NLDM, but instead of measuring voltage thresholds at the output pin, current is measured through the load capacitor, and into the input pin. The current through C_{out} is used for the driver model, and the current into the input pin is used to determine the receiver model.

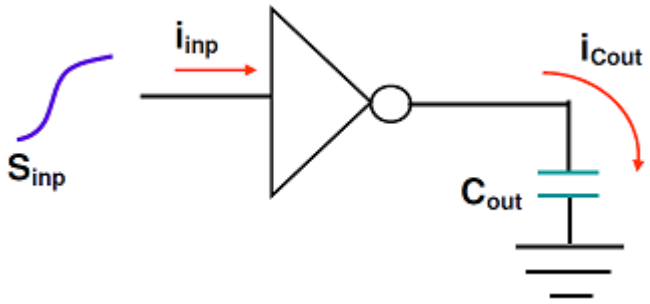


Figure 2.9: CCS Timing Characterization Measurements[3]

These characterization experiments are repeated for a table of different S_{in} and C_{out} combinations. The current through C_{out} is saved for every circuit simulation timestep, and then reduced into a much smaller set of current and time (i, t) points. The points are chosen such that $V_{out}(t)$ can be accurately reproduced for every timestep during the transition.

Figure 2.10 shows an example of the complete i(t) waveform and a reduced set of points.

The current and voltage at the input pin are saved and then used to determine C_1 and C_2 values such that gate-level delay calculation can closely match times to

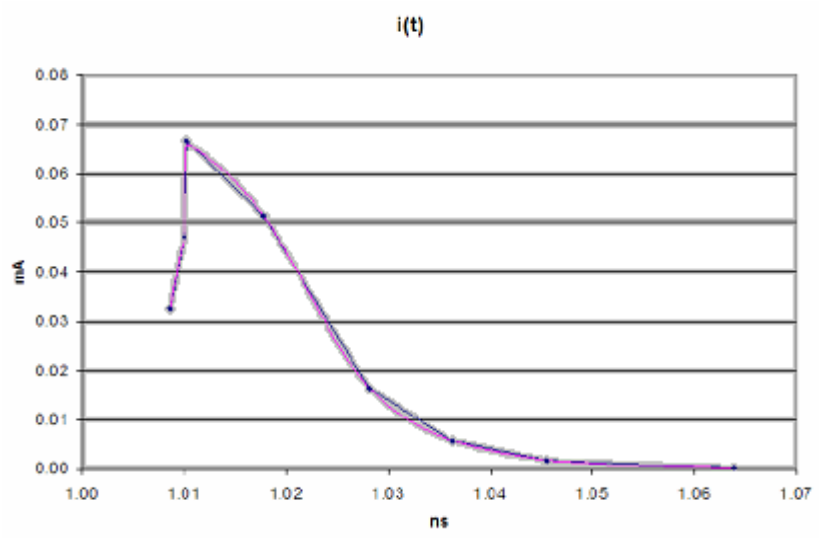


Figure 2.10: Current waveform from circuit simulation, and reduced current points[3]

the delay threshold and to the second slew threshold at the input pin. An additional piece of information, input reference time, is needed in order to calculate cell delays. The reference time is the simulation time at which the waveform at the input pin crosses the rising or falling delay threshold (often this is 50% of Vdd).

CCS Timing delay calculation provides high accuracy for cell delay, interconnect delay and pin slew. The CCS Timing receiver model produces excellent results on single stage cells with large Miller effect.

2.8.2 CCS Noise

2.8.2.1 Introduction

Increasing systems integration, physical effects like noise become sizeable. In fact using for example CMOS 45nm technology, noise phenomenon must be better modeled to provide best accuracy noise behavior models. CCS-Noise is a new advanced current-based driver model that enables accurate noise analysis with results very close to SPICE simulation. CCS-Noise model will be able to models injected

crosstalk noise bumps, propagated noise bumps and driver weakening. In this way, ccs driver model defines cell noise immunity, and cell noise propagation behavior.

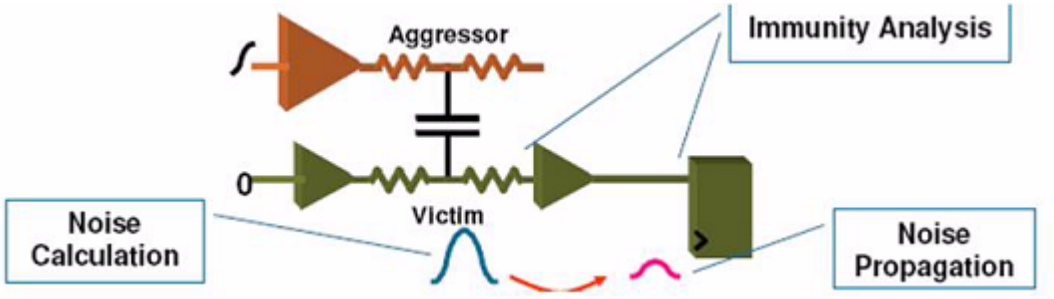


Figure 2.11: Noise Propagation[5]

Alto provides all the raw characterization data necessary to build up the CCS-Noise Synopsys models. Four CCS-Noise simulations are put in place in Alto :

- ccs-noise dc current
- ccs-noise output voltage
- ccs-noise propagation
- ccs-noise Miller capacitance

2.8.2.2 CCS Noise Concept

CCS-Noise model captures the noise properties of a cell. CCS-Noise is based on Vin/Vout current-based models. This model best capture the behavior of a single Channel-Connected Block (CCB). It gives a set of characterization data that provide information for:

- Noise failure detection on cell inputs also called immunity analysis
- bump calculation on cell outputs
- propagation through the cell

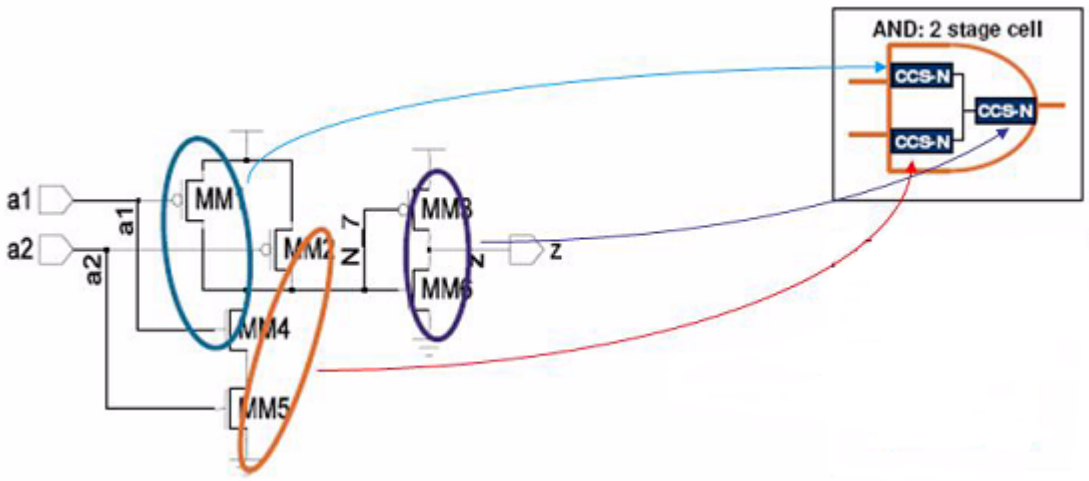


Figure 2.12: AND gate CCBs splitting[5]

For multi-stages cells, split initial neltist in multiple CCBs is needed before CCS-Noise characterization. After that noise characterization will be done for each CCB.

2.9 IR drop analysis

2.9.1 Introduction

The power supply in the chip is distributed uniformly through metal layers (Vdd and Vss) across the design. These metal layers have finite amount of resistance. When voltage is applied to these metal wires current start flowing through the metal layers and some voltage is dropped due to the resistance of metal wires and current. This Drop is called as IR Drop.

For example, a design needs to operate at 2 volts and has a tolerance of 0.4 volts on either side, we need to ensure that the voltage across its power pin (Vdd) and ground pin (Vss) in that design does not fall short of 1.6 Volts. The acceptable IR drop in this context is 0.4 volts. That means the design in this context can allow up to 0.4 volts drop which does not affect the timing and functionality of design.

IR Drop is Signal Integrity (SI) effect caused by wire resistance and current

drawn off from Power (Vdd) and Ground (Vss) grids. If wire resistance is too high or the current passing through the metal layers is larger than the predicted, an unacceptable Voltage drop may occur. The design may have different types of gates with different voltage levels. As the voltage at gates decreased due to unacceptable voltage drop in the supply voltage, the gate delays are increased non-linearly. This may lead to setup time and hold time violations depending on which path these gates are residing in the design.

As technology goes on shrinking, there is decrease in the geometries of the metal layers and the resistance of these wires increased which lead to decrease in power supply voltage. With advancement in technology the supply voltages goes on shrinking and this increased wire resistance has much more impact on circuit performance.

Apaches RedHawk tool is used for IR drop analysis to design supplies. Supports SPICE - characterized waveform data in Apache Power Libraries. RedHawk Supports :

- Full chip Static and dynamic power and voltage drop analysis.
- Full-chip RLC power-ground extraction.
- Transient simulation and (EM) electro migration analysis.
- Power integrity design fixing and optimization.
- Decoupling capacitance analysis.

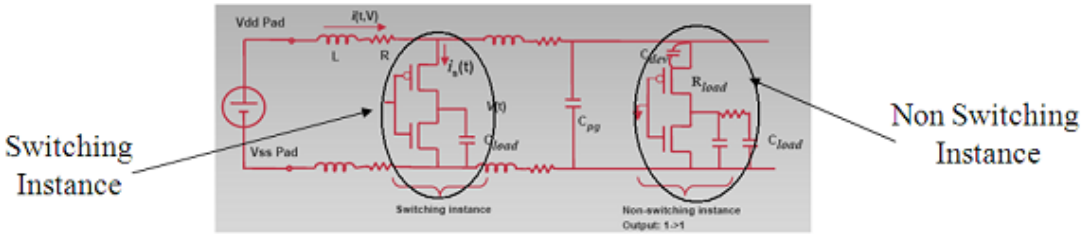


Figure 2.13: Switching and Non switching cells[10]

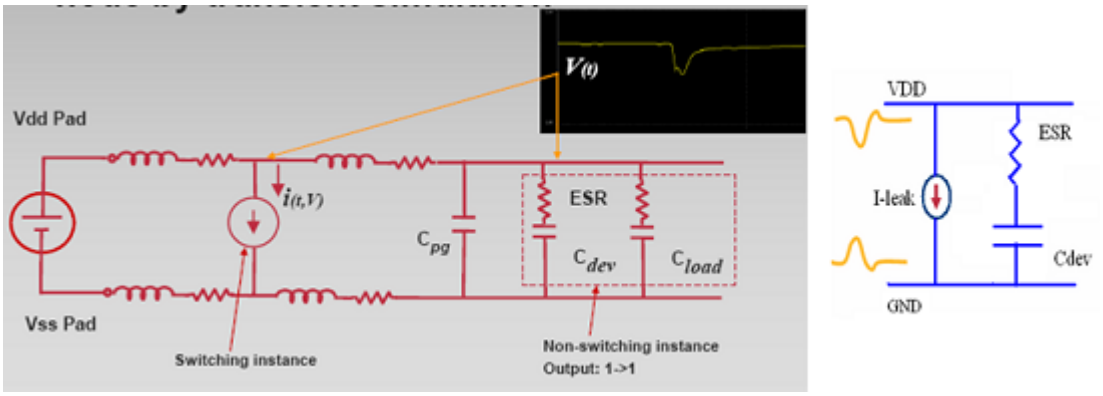


Figure 2.14: (a) cell representation for IR drop analysis (b) Non Switching cell representation[10]

For IR drop analysis for switching cell instantaneous current through the cell is calculated and for non switching cell leakage current, effective series resistance (ESR) and intrinsic capacitance (Cdev) is calculated.

2.10 Timing Checks Characterization

2.10.1 Introduction

For a Latch/Flip-Flop we have to ensure that the data signal has stabilized before latching its value. This is done by defining setup and hold arcs as timing requirements.

There are five types of timing checks : Setup, Hold, Recovery, Removal and pulse width.

1. **Setup Constraints :**

   Setup constraints describe the minimum time for which the data has to remain constant before the active edge of the clock arrives, so that the correct value is latched. If the data signal makes a transition during setup time, an incorrect value may be latched.

2. **Hold Constraints :**

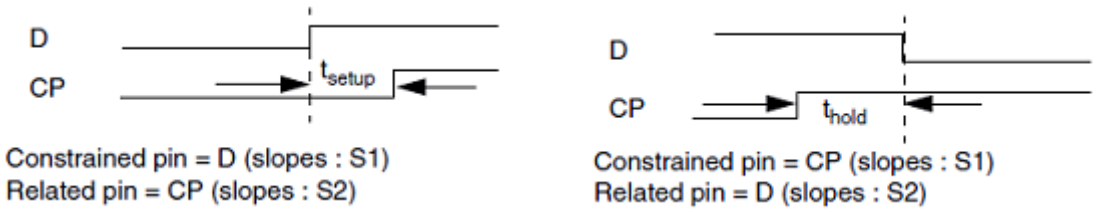


Figure 2.15: Setup and Hold definitions[5]

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. For the measurement of Hold Time, the data input signal is held stable before the active clock edge for an infinite Setup Time.

3. **Recovery Constraints :**

   Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell.

4. **Removal Constraints :**

   Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell.

5. **Minimum Pulse Width :**

   Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell.

Chapter 3

MOSFET Technology

3.1 Introduction to MOSFET

The MOSFET is a four terminal device. These are 1) Gate 2) Drain 3) Source 4) Substrate. The construction of MOSFET consists of substrate in which two diffusion region are formed named Source and Drain. The surface of the substrate region between drain and source is covered with the thin oxide layer, and a metal or polysilicon is deposited over this oxide layer. This terminal is named as gate of MOS. The voltage applied to the gate terminal determines whether current flows between the source and the drain ports. The body represents the fourth terminal of the transistor. It's function is secondary as it only serves to modulate the device characteristics and parameters.

At the most superficial level, the transistor can be considered to be a switch. When a voltage is applied to the gate that is larger than a given value called the threshold voltage V_T, a conducting channel is formed between drain and source. In the presence of a voltage difference between the drain and source terminal, current flows between them. The conductivity of the channel is modulated by the gate voltage, the larger the voltage difference between gate and source, the smaller the resistance of the conducting channel and the larger the current. When the gate volt-

age is lower than the threshold, no such channel exists, and the switch is considered open.

Two types of MOSFET devices can be identified :

The NMOS transistor consists of n+ drain and source regions, embedded in a p-type substrate. The current is carried by electrons moving through an n-type channel between source and drain.

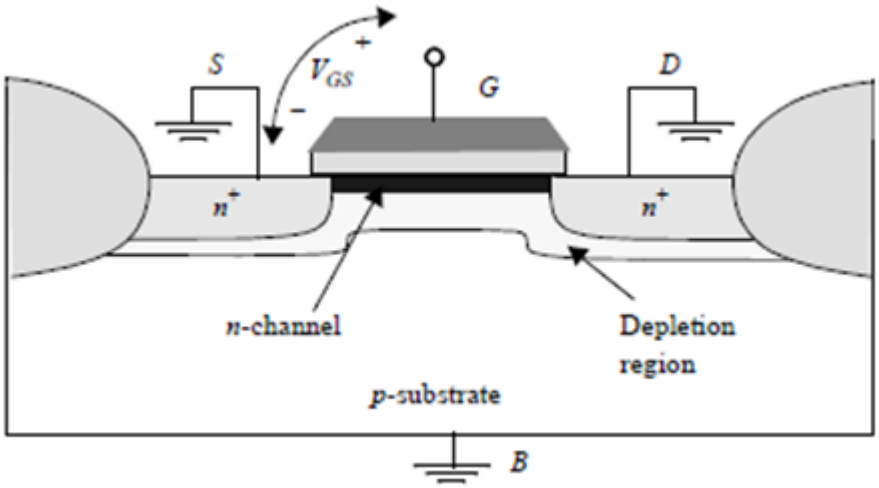


Figure 3.1: Cross section of NMOS transistor[14]

The PMOS transistor can be made by using an n-type substrate and p+ drain and source regions. In such a transistor, current is carried by holes moving through a p-type channel.

In a complementary MOS technology (CMOS), both devices are present.

3.2 The Threshold Voltage :

The minimum Voltage required at the gate terminal to form a channel between source and drain, so that current can flow through the circuit is called threshold voltage.

For a MOS device current equation can be given as

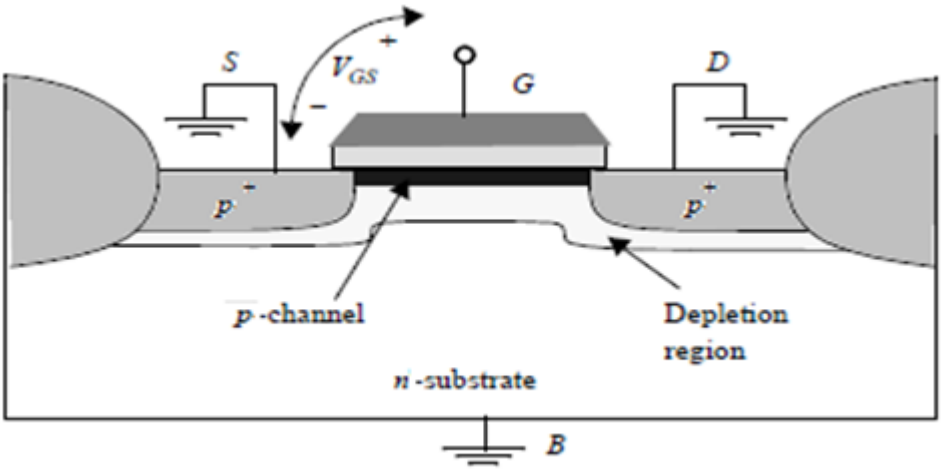


Figure 3.2: Cross section of PMOS transistor[14]

$$I_D = K'_n \frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] = K_n[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

Where,

W - width of channel

L - length of channel

V_{GS} - Voltage at gate terminal

V_T - Threshold voltage

V_{DS} - Voltage at Drain terminal

K'_n - 'process trans-conductance' parameter, can be given as

$$K'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

The product of the process trans-conductance and the (W/L) ratio of an (NMOS) transistor is called the gain factor K_n of the device.

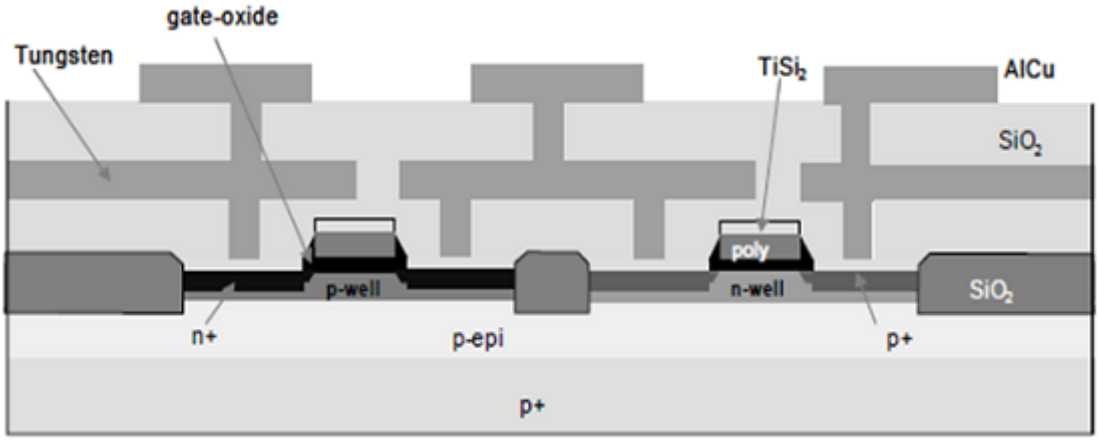


Figure 3.3: Cross section of Complementary MOS (CMOS)[14]

3.3 Temperature inversion in Deep sub-micron technologies :

Temperature inversion is observed in the advanced technology nodes like 65nm, 40nm, 28nm etc. which is not the same in case of 90nm, 180nm etc.

The delay of a cell is a function of input transition and output load of the cell but delay is also depend on the temperature because current of the cell is changed due to variation of the temperature and cell delay depends on the current of the cell. If current increase then delay decrease and vice versa.

Due to Variation of temperature following two parameter changes :

1. Mobility of the carriers.

2. Threshold voltage.

Temperature is inversely proportional to mobility of the carriers and threshold voltage. So temperature increase then mobility of the carriers and threshold voltage decrease and current of the cell is directly proportional to the mobility and inversely proportional to threshold voltage. So, with the increase in the temperature the delay of a cell can

- Increase due to decrease in carrier mobility
- Decrease due to decrease in threshold voltage

Here race condition occurs between carrier mobility and threshold voltage so delay of the cell is depending upon which one is dominant.

For > 90nm technology supply voltage used is around 1.2V. Here increase in temperature decrease the threshold voltage and decrease the carrier mobility but gate overdrive voltage ($V_{od} = V_{dd} - V_t$) is large enough that a decrease in V_t with temperature is negligible, so the mobility effect dominates and hence the delay of the gate increases with temperature.

For < 90nm technology supply voltage used is around 0.9V to 1.1V. So at 0.9v gate overdrive voltage ($V_{od} = V_{dd} - V_t$) has reduced and hence V_t decrease dominates and delay decreases with increase in temperature. So, at the advanced technology nodes though the threshold voltage has not reduced much, but the gate overdrive voltage has reduced due to the reduction of supply voltages. Therefore, temperature inversion effects are more observed in technologies 40nm and below.

Temperature inversion effect also depend on the type of MOS used (i.e. HVT, RVT, LVT). HVT (High Threshold Voltage) cells respond to the temperature inversion effect more effectively compared to RVT (Regular Threshold Voltage) and LVT (Low Threshold Voltage) cells. RVT cells show a moderate temperature inversion effect but LVT cells are almost immune to temperature inversion effect.

3.4 Process Effect :

There are following three types of process are used for standard cell characterization.

1. BEST
2. TYPICAL

3. WORST

In the BEST process both NMOS and PMOS are faster means in this process used NMOS and PMOS has lower threshold voltage. For Typical process threshold voltage is moderate and for Worst process threshold voltage is higher.

The threshold voltage of a MOSFET is defined as the gate to source voltage V_{GS} that is required to form an inversion layer in the channel at the interface between the gate oxide and the silicon surface under the gate, thus allowing a current to flow from the source to drain terminals of the transistor. The threshold voltage is one of the key device parameters in CMOS technology, since it allows transistors to act like switches and hence is a suitable device to perform logic operations.

As shown in Equations 3.1 and 3.2, threshold voltage plays a major role in device performance metrics. Not only does it determine the on state current of a transistor, but also it has an exponential impact on the leakage current and leakage current is inversely proportional to the propagation delay. If threshold voltage is decrease then current is increase and due to increase in current propagation delay decreases. In the BEST process both NMOS and PMOS has low threshold voltage so propagation delay is less compare to TYPICAL and WORST process.

$$t_{pd} = \frac{CV_{dd}}{I_D}\alpha\frac{V_{dd}}{(V_{dd-V_{th}^2})} \tag{3.1}$$

$$I_D = \mu\frac{W}{L}C_{ox}(V_{GS} - V_{th})^2 \tag{3.2}$$

As shown in equation 3.3 and 3.4, threshold voltage is determined only by the doping concentration (Na) and the oxide capacitance C_{ox}. If the doping concentration (Na) is increase then threshold voltage is decrease.

$$\phi_f = 2\frac{KT}{q} ln \frac{N_a}{n_i} \tag{3.3}$$

Where, ϕ_f is the Fermi potential, Na is the doping concentration n_i is the intrinsic carrier concentration in Si, T is the absolute temperature, K is Boltzmanns constant and q is the electron charge.

$$V_{th} = V_{fb} + 2\phi_f + \frac{\sqrt{2qN_a\varepsilon_s}}{C_{ox}}(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}) \tag{3.4}$$

Where, V_{fb} is the flat-band voltage, V_{SB} is the source-body voltage, ϕ_f is the Fermi potential, C_{ox} is the oxide capacitance and ε_s is the permittivity constant of silicon.

3.5 Drive Strength :

Drive strength is the capacity of a cell to drive a value to the cell connected to it's output. Different sizes of standard cells have different capacitance, smaller cells have small capacitance and vice versa. It is easier to drive a small cell than a large one. The load connected at the output of a cell is the combined capacitance of all the cells connected at the output. So larger the load, larger is the drive required to "force" the values at the output.

From another point of view, it is just the strength required to charge/discharge the capacitance at the output to the required value. As the drive strength increases, active area of cell increases, which means the cell is made bigger. For a cell of drive X2, compared to drive X1, active area will be increased by 2 times. Similarly for a cell of drive X4 active area will be increased by 4 time. As area increases, current drawn from the supply increase.

Due to increase in current drawn, output capacitors charge quickly and cell

become faster. This type of approach can be used in HIGH SPEED LIBARAIES where delay is on more priority than leakage.

3.6 Gate-Length Biasing :

Leakage power has become one of the most critical design concerns for the submicron region. Below 90nm, this effect increases non-linearly. While lowered supplies (and consequently lowered threshold-voltage) and aggressive clock gating can achieve dynamic power reduction, these techniques increase leakage power and therefore cause it's share of total power to increase. Leakage is composed of three major components:

1. Sub-threshold leakage
2. Gate leakage
3. Reverse biased drain substrate and source substrate junction leakage

Sub-threshold leakage is the dominant contributor to total leakage at 130nm and remains so in the future, for short channel devices, with increasing of the gate length, the threshold voltage increases, so that the leakage decreases exponentially and delay increases linearly. The gate-length biasing (GLB) technology increases the channel length of transistors to alter the threshold voltage and reduces leakage exponentially in both active and standby modes, while delay increases linearly with increasing gate length. Thus, it is possible to increase gate-length only marginally to take advantage of the exponential leakage reduction, while impairing performance only linearly.

$$L_g = L'_g + X$$

Where,

L_g - modulated gate length

L'_g - actual gate length

X - modulating factor

X - value ranges from 10% to 30%

EDP (Energy Delay Product) metric provides a good compromise between speed and delay, which is written as

$$EDP = E \times t_{delay}$$

Where, E and t_{delay} represents energy and delay respectively. We can apply gate-length modulation only to those devices that do not appear in critical paths, thus assuring zero or negligible degradation in performance. In this way we can enhance the performance of circuit while keeping the leakage minimum.

Further for leakage optimization, low drive cells have been used. As the drive strength decreases current sources from the supply decreases, which cause delay increase for charging and discharging of output load and reduces leakage. These type of configuration used in LOW LEAKAGE DESIGN LIBRARIES where leakage optimization is must.

3.7 Body Biasing Effect :

Body effect refers to the change in the transistor threshold voltage (V_T) resulting from a voltage difference between the transistor source and body. As the voltage difference between the source and body affects the (V_T) , the body can be thought of as a second gate that helps to determine how the transistor turns on and off. The strength of the body effect is usually quantified by the body coefficient gamma. Strong body effect enables a variety of effective body biasing techniques, and these techniques were used effectively in older process generations. However, body effect has diminished with transistor scaling, and conventional deep-submicron transistors have very little body effect. For this reason body bias is not widely used for 65nm and

smaller process technologies. Instead, the transistor bodies are generally connected along with the transistor source to either power (VDD) for p-channel or ground (VSS) for n-channel transistor. The strong body effect is a key enabler of low-power circuit operation for deep submicron CMOS technologies.

Body bias involves connecting the transistor bodies to a bias network in the circuit layout rather than to power or ground. The body bias can be supplied from an external (off-chip) source or an internal (on-chip) source. In the on-chip approach, the design usually includes a charge pump circuit to generate a reverse body bias voltage and/or a voltage divider to generate a forward body bias voltage.

- Reverse body bias, which involves applying a negative body to source voltage to an n-channel transistor, raises the threshold voltage and thereby makes the transistor both slower and less leaky.
- Forward body bias, on the other hand, lowers the threshold voltage by applying a positive body to source voltage to an n-channel transistor and thereby makes the transistor both faster and leakier.

The polarities of the applied bias described above are the opposite for a p-channel transistor.

3.8 Limitations of Body bias in Bulk CMOS (28nm) Technology :

In case of bulk CMOS 28nm, source/drain to substrate p-n junction will limit the range of body bias because when we apply the bias voltage to substrate terminal in either direction i.e. reverse body bias (RBB) or forward body bias (FBB) then source/drain to substrate p-n junction will be reverse bias or forward bias. This will increase leakage current through the MOS which is undesirable and that will limit the range of body bias (-300mv to 300mv) in bulk CMOS 28nm technology.

Also in bulk CMOS below 28nm the cost per gate increases with advancement in technology due to various parameter including fabrication process. Which indicate that Moore's law will no longer exist below 28nm bulk CMOS technology.

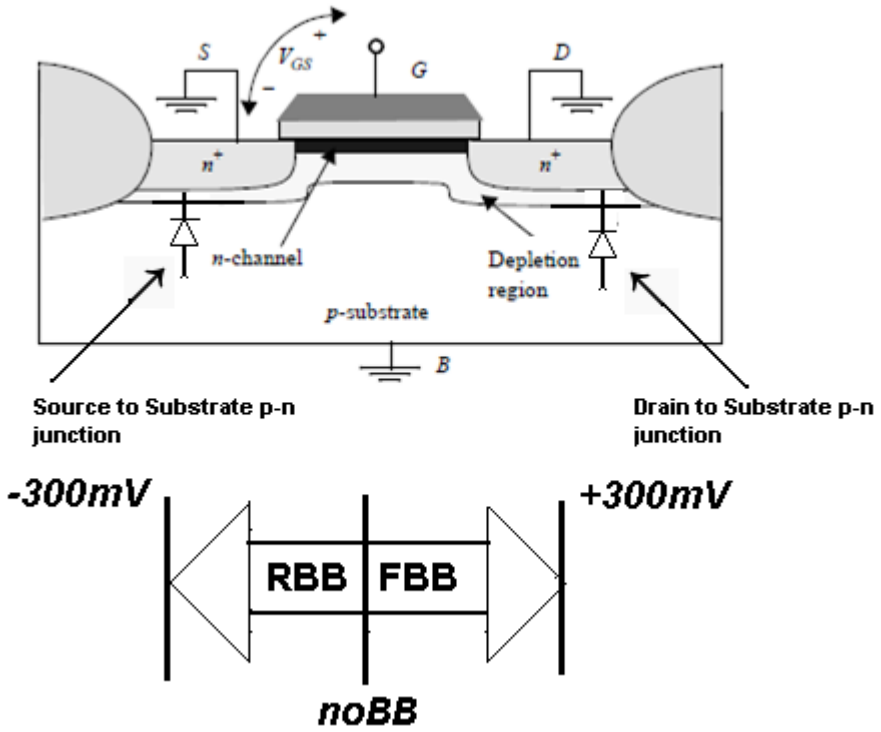


Figure 3.4: Source/Drain to bulk diode limits range of body bias in bulk CMOS

1. **No body bias (No BB)**

   Substrate terminal of PMOS (vdds) and NMOS (gnds) are connected to source terminal of PMOS (vdd) and NMOS (gnd) respectively.

2. **Forward body bias (FBB)**

   The vdds is reduced towards ground whereas gnds is increased towards vdd, to reduce threshold voltage of MOSFETs and thereby enhancing the speed of operation. But it has drawback that as we go on increasing the FBB above 300mv, the leakage increases drastically.

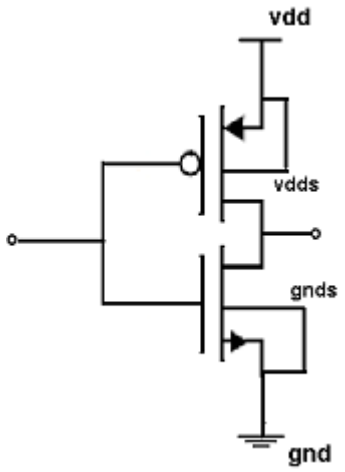


Figure 3.5: CMOS inverter using bulk 28nm[14]

3. **Reverse body bias (RBB)**

   The vdds is increased further above vdd while gnds is reduced below gnd to minimize leakage at the cost of increased delay. But it has drawback that as we go on increasing the RBB although leakage through Vdd is decreasing, the leakage associated with Vdds increases which is undesirable. Also RBB increases delay drastically, increasing power delay product (PDP).

To summarize CMOS bulk technology body biasing is limited upto 300mv only.

3.9 Introduction to FDSOI :

Fully Depleted Silicon on Insulator (FDSOI) technology gives improved speed at lower power dissipation over bulk CMOS technology by providing wide range of body biasing (-3V to 3V). Also the fabrication procedure using FDSOI technology is simpler which further reduces cost per gate.

SOI process technology for CMOS circuits is very similar to the technology for bulk devices. The main structural difference is that SOI wafers have a buried-oxide (BOX) layer between the SOI layer and the silicon substrate. In one sense, the BOX layer simplifies the fabrication process because it provides a perfect isolation

structure. On the other hand, the difficult technologies needed for processing the SOI layer, especially the thin SOI layer of FD-SOI devices, makes the SOI process more complex than the bulk one.

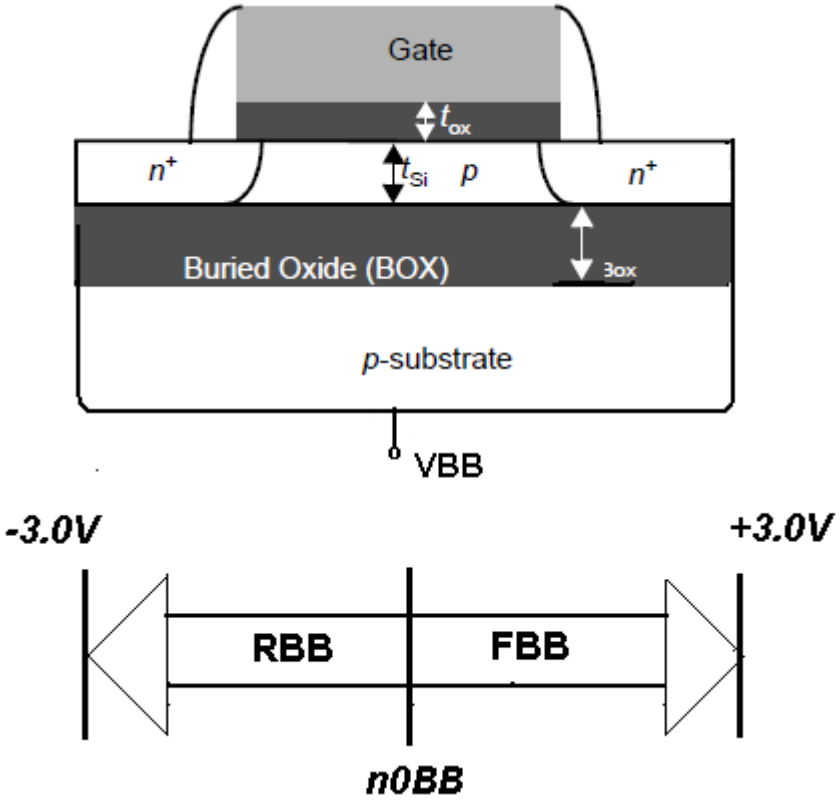


Figure 3.6: Extended body bias due to BOX layer in FDSOI

3.10 Advantages of SOI :

The BOX layer gives many advantages in SOI MOSFET over their Bulk-Si counterparts.

1. **Negligible drain to substrate capacitance :**

   Following figure 3.7 shows a schematic diagram of the capacitances in Bulk-Si and SOI MOSFET. In SOI devices, the capacitance between the drain (source) and the substrate is negligibly small because of the dielectric constant

of SiO_2, which is lower than that of Si, and the thickness of the BOX. This helps to improve the switching speed of CMOS devices. It is worth noting that this improvement in speed roughly corresponds to the performance gain obtained by jumping ahead one technology generation.

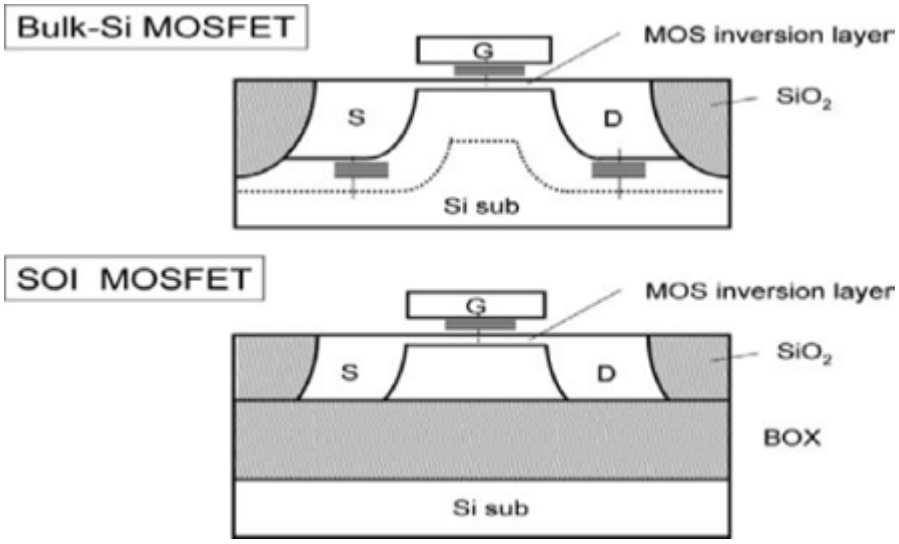


Figure 3.7: Capacitances of Bulk-Si and SOI MOSFET[11]

2. **Positive body bias improves speed of stacked gates :**

The independent body bias of SOI MOSFET makes them faster in a stacked gate structure. In the stacked gates made with Bulk-Si MOSFETs in Figure 3.8, the negative body bias of the circled transistor is generated by the current flowing to the ground. This increases the threshold voltage and lowers the operating speed. In contrast, the body bias of stacked SOI MOSFET is positive because it takes a value between the source and drain biases. This yields a lower threshold voltage for stacked transistors, thereby enhancing the operating speed. It should be noted that the advantage of stacked gates is that they reduce the area occupied by a circuit.

Figure 3.8 Stacked gates provide high speed. The drain current of the circled MOSFET is enhanced in an SOI structure due to the lack of body

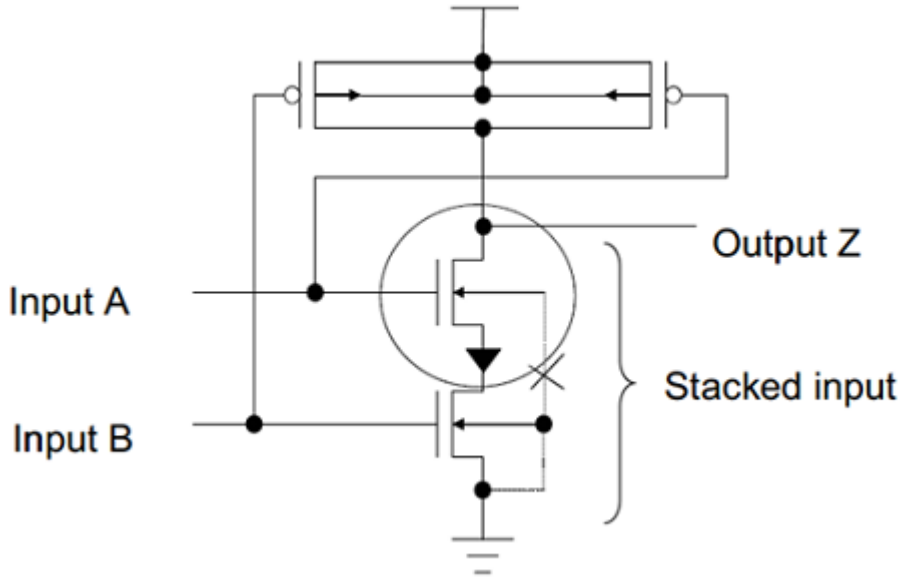


Figure 3.8: Stacked gates provide high speed. The drain current of the circled MOSFET is enhanced in an SOI structure due to the lack of body effects[11]

effects.

3. **Small p-n junction leakage :**

   The leakage current of a p-n junction is significantly smaller in an SOI structure because the impurities in the n+ and p+ regions diffuse deeply into the thin Si film, leaving a p-n junction only at the sidewall of the diffused area. A low p-n junction leakage current is generally beneficial in every type of application; but it is especially important in applications requiring a low stand-by power, such as mobile phones and PDAs, because it prolongs battery life.

4. **Extended range of body bias :**

   In case of bulk CMOS 28 nm, source/drain to substrate p-n junction will limit the range of body bias because when we apply the bias voltage to substrate terminal in either direction i.e. reverse body bias (RBB) or forward body bias (FBB) then source/drain to substrate p-n junction will be forward

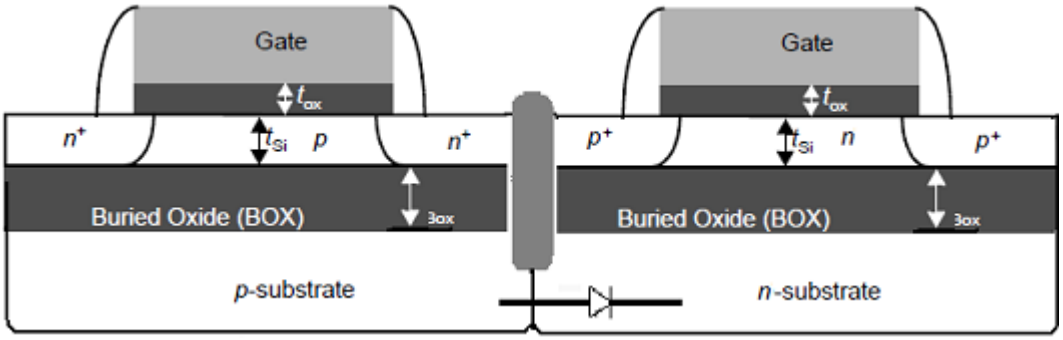


Figure 3.9: In FDSOI p-n junction present only at the sidewall

bias. This will increase leakage current through the MOS which is undesirable and that will limit the range of body bias in bulk CMOS 28nm technology. But in case of FDSOI due to use of BOX layer the range of body bias increases.

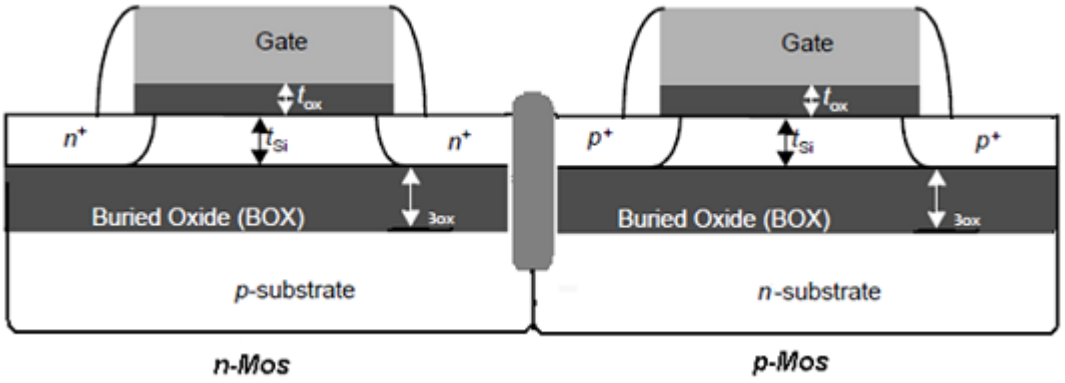


Figure 3.10: In FDSOI p-n junction present only at the sidewall

Chapter 4

Tools

4.1 ST internal Characterization Tool

It is a standard cell library production tool. It does following three tasks for a particular set of standard cells :

- Extracts timing and timing checks and calculate the truth table and generates stimuli.
- Characterize cells and produce technology dependent database.
- Generate front-end models such as Synopsys Technology Format (STF) file, verilog, etc. and technology dependent database.

The most important inputs needed for cell characterization are :

1. **Cell Specific Information :** A file that contains the name of the cell, the name of its input and output pins, its netlist (which describes its functionality), its output load and other switches. We have to describe the supply per pin, the load per pin and the input slope per pin.
2. **Library Specification file :**This file contains the specifications used for measurements (delay, power) also it includes :

- Default units (usually ns, pf, V, mW)
- Supplies definition
- PVT definition
- Description of characterization methodology

3. **Stimuli Database :** This database consists of truth table, stimuli, pin and constraint information, related to the cell (only for sequential cells). .stim files are stimuli files. Some of them contain arcs on which later characterization is done.

4. **Netlist :** It is a netlist file which contains the transistor information along with the parasitic (capacitances and resistances) information between various nodes of the cell.

5. **Models :** The models contain the definitions of the transistors present in the netlist which includes various parameters like its C_{ox} (oxide capacitance) and t_{ox} (oxide thickness).

4.2 ELDO

The ELDO analog simulator is the core component of a comprehensive suite of analog and mixed signal simulation tools. ELDO offers a unique partitioning scheme allowing the use of different algorithms on differing portions of design. It allows the user a flexible control of simulation accuracy using a wide range of device model libraries, and gives a high accuracy yield in combination with high speed and high performance. A brief description of mainly used files is given below :

CIR File : The main ELDO control file, containing circuit netlist, stimulus and simulation control commands. This file is SPICE compatible, the ELDO control language being a superset of the Berkeley SPICE syntax.

CHI File : SPICE compatible output log file containing ASCII data, including results and error messages.

WDB File : A binary output file for mixed-signal JWDB format files. Can be viewed with the EZ wave waveform viewer.

SWD File : A saved windows file used by the EZ wave waveform viewer. This file contains information on waveforms and their display and cursor settings, window format settings and complex waveform transition settings.

It requires following input files to simulate the circuit :

- Model parameter values defining the specific device models to be used.
- Stimuli
- Subcircuit definition and netlist
- Simulation option & commands

The file which contains all above inputs is called as .cir file (circuit simulation file). After running ELDO a file is generated that contains output log file containing ASCII data, including result and error messages. The waveform can be viewed from the files generated.

The subcircuit definition in .cir file for inverter shown in figure 4.2 will be as follows :

```
*Subcircuit definition
.subckt inv 1 2 3
m2 2 1 0 0 nmos [m=1] w=10u l=4u
m1 2 1 3 3 pmos [m=1] w=15u l=4u
c1 2 0 0.5p
.ends inv
```

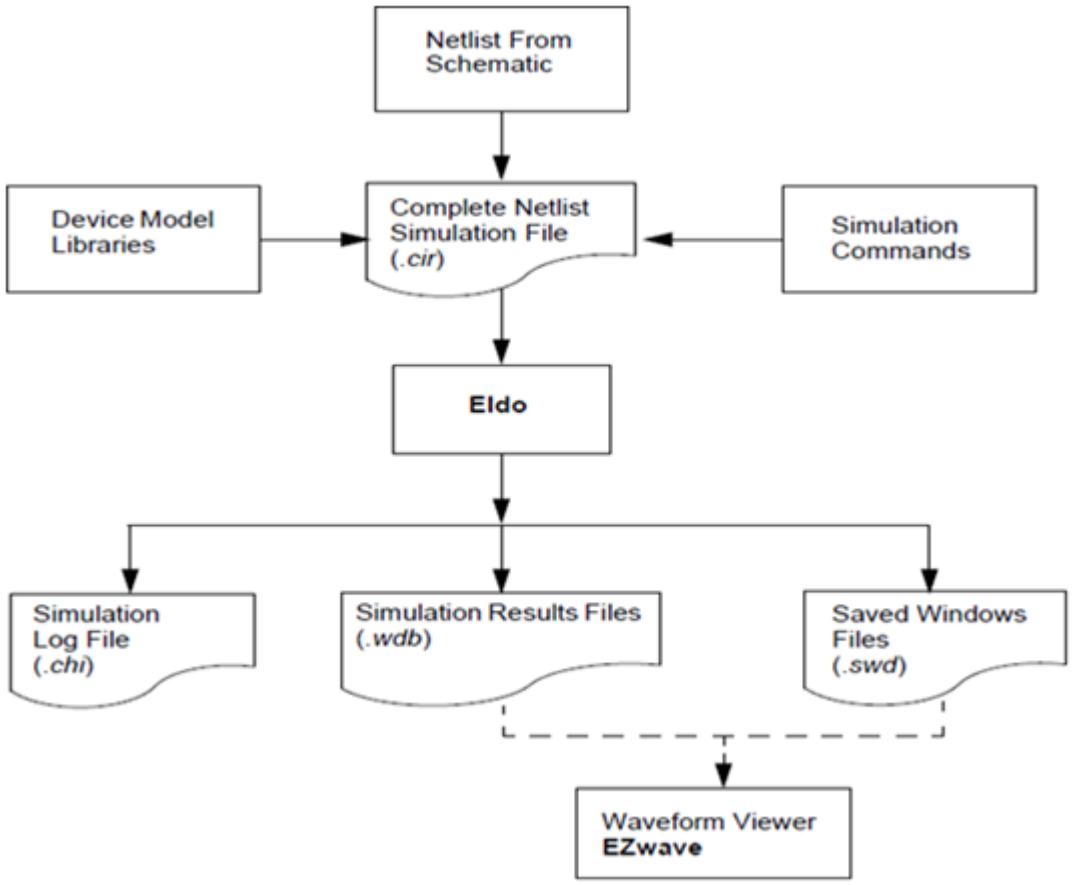


Figure 4.1: Eldo simulation flow input and output files[6]

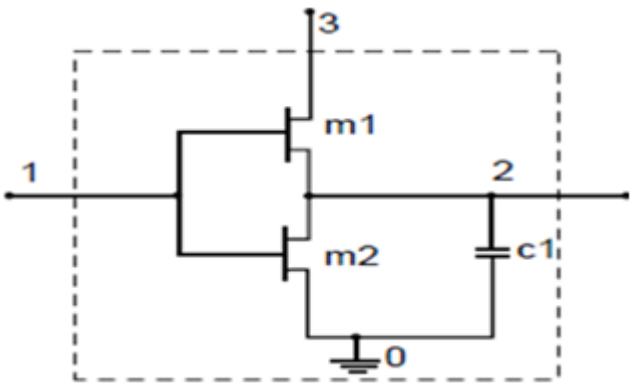


Figure 4.2: Inverter subcircuit[6]

Chapter 5

Results and Analysis

5.1 Characterization Results :

The characterization of two input AND cell is done at following operating conditions :

Process: Best case

Operating voltage: 1.1V

Temperature: 105°C

C_{load}: 0.066pf

Slope: 0.21ns

1. **Propagation Delay Measurement :**

   Propagation Delay Results :

Table 5.1: Propagation delay measurement

Transition	Delay(ns)
A_R_Z_R_1	0.13547
A_F_Z_F_1	0.14367
B_R_Z_R_1	0.13493
B_F_Z_F_1	0.14093

Propagation Delay for A_R_Z_R Transition: 13ps

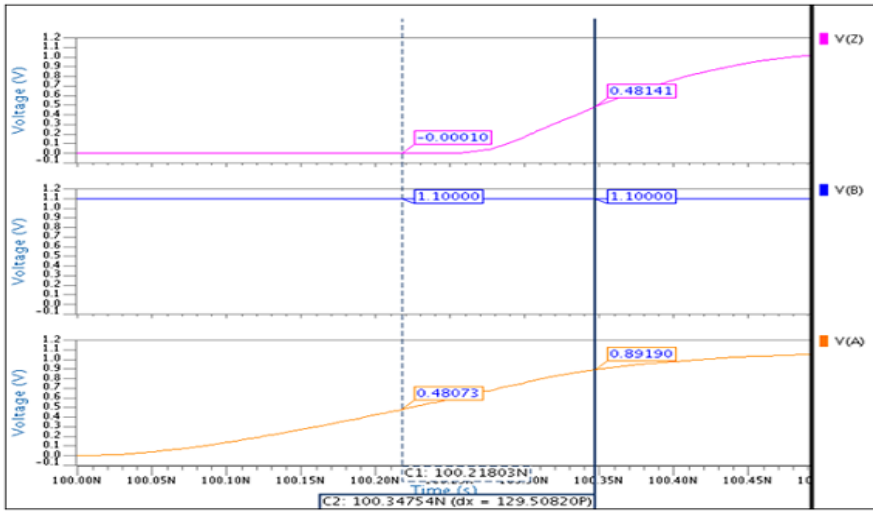


Figure 5.1: Delay measurement for A_R_Z_R transition

Propagation delay for B_F_Z_F Transition: 15ps

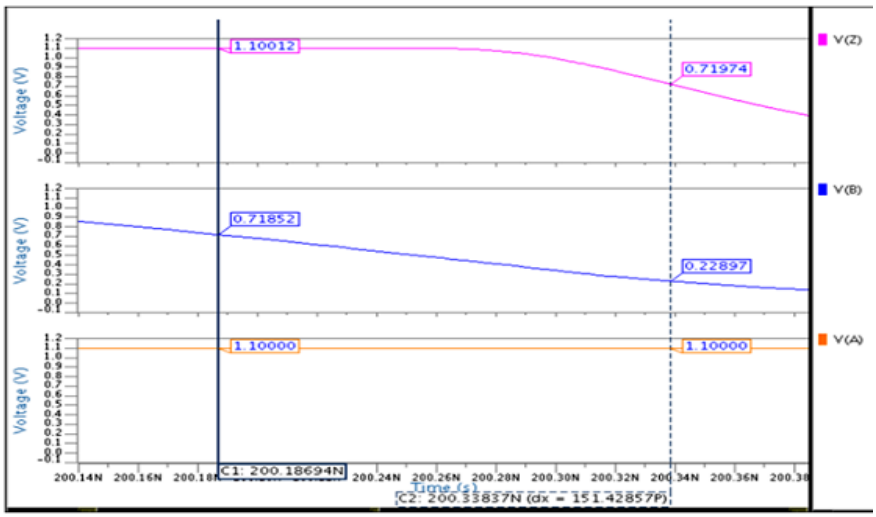


Figure 5.2: Delay measurement for B_F_Z_F transition

2. **Output Slope Measurement :**

Slope for A_R_Z_R Transition: 13ps

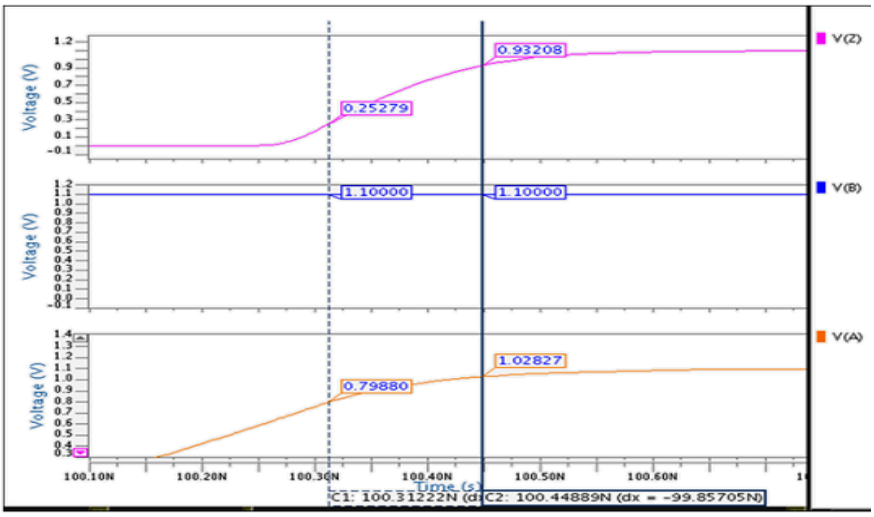


Figure 5.3: Slope measurement for A_R_Z_R Transition

Slope for B_F_Z_F Transition: 10ps

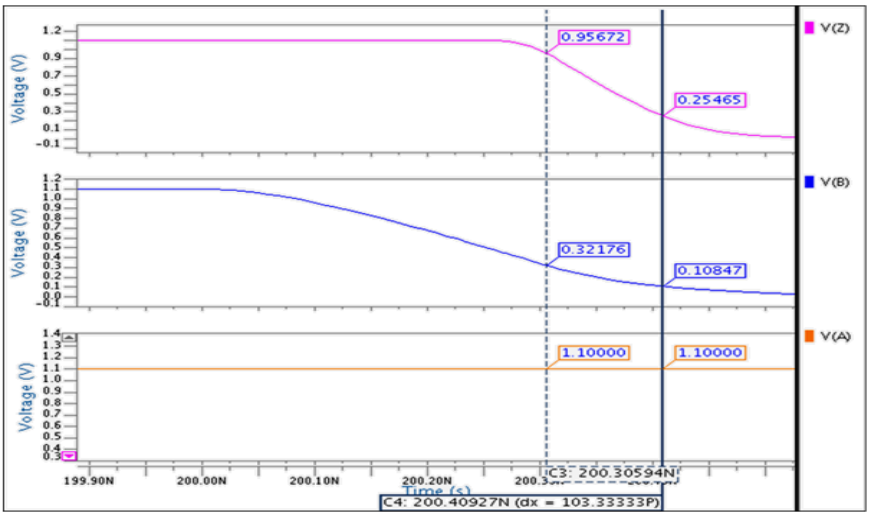


Figure 5.4: Slope Measurement for B_F_Z_F Transition

Output Slope Results :

Table 5.2: Slope measurement

Transition	Output Slope
A_R_Z_R_1	0.1238
A_F_Z_F_1	0.099306
B_R_Z_R_1	0.1235
B_F_Z_F_1	0.099682

3. **Input Capacitance Measurement :**

Table 5.3: Input capacitance measurement

Transition	Input Capacitance
A_R_Z_R_1	0.001398
A_F_Z_F_1	0.0013863
B_R_Z_R_1	0.0013237
B_F_Z_F_1	0.0013225

4. **Internal Energy Measurement :**

Table 5.4: Intenergy measurement

Transition	Total	Switch	Supply
A_R_Z_R_1	0.10882	0.0812	Vdd
A_R_Z_R_1	-2.8846e^{-5}	0.0	Vdds
A_F_Z_F_1	0.028561	0.0	Vdd
A_F_Z_F_1	3.1827e^{-5}	0.0	Vdds
B_R_Z_R_1	0.10941	0.081	Vdd
B_R_Z_R_1	-4.242e^{-5}	0.0	Vdds
B_F_Z_F_1	0.029198	0.0	Vdd
B_F_Z_F_1	4.5276e^{-5}	0.0	Vdds

5. **Leakage Power Measurement :**

Table 5.5: Leakage power measurement

Condition	Leakpower	Supply
A0_B0	$5.0405e^{-4}$	Vdd
A0_B0	$5.3068e^{-8}$	Vdds
A0_B1	$6.1095e^{-4}$	Vdd
A0_B1	$5.3072e^{-8}$	Vdds
A1_B0	$6.4743e^{-4}$	Vdd
A1_B0	$5.3073e^{-8}$	Vdds
A1_B1	$6.6022e^{-4}$	Vdd
A1_B1	$4.2701e^{-8}$	Vdds

The characterization results of 2 input NOR cell are as follows:

Cell: 2 input NOR (inputs: A, B; output: Z)

Technology: Bulk CMOS (28nm - LVT)

Process: Best, Voltage: 0.85V, Temperature: 125°C

Slope: 0.69 ns, output load capacitance (C_{load}): 0.0448 pf

Table 5.6: Propagation Delay for NOR cell

Transition	Delay(ns)
A_R_Z_F_0	0.18151
A_F_Z_R_0	0.25664
B_R_Z_F_0	0.17222
B_F_Z_R_0	0.25205

Table 5.7: Output Slope for NOR cell

Transition	Output Slope
A_R_Z_F_0	0.17516
A_F_Z_R_0	0.1773
B_R_Z_F_0	0.17831
B_F_Z_R_0	0.20633

Table 5.8: Input Capacitance for NOR cell

Transition	Input Capacitance
A_R_Z_F_0	0.004973
A_F_Z_R_0	0.0050305
B_R_Z_F_0	0.0051963
B_F_Z_R_0	0.005184

Table 5.9: Intenergy for NOR cell

Transition	Total	Switch	Supply
A_R_Z_F_0	0.028666	0.0	Vdd
A_R_Z_F_0	0.0015092	0.0	Vdds
A_F_Z_R_0	0.078731	0.03233017	Vdd
A_F_Z_R_0	-0.0014992	0.0	Vdds
B_R_Z_F_0	$5.5488e^{-4}$	0.0	Vdd
B_R_Z_F_0	$5.5488e^{-4}$	0.0	Vdds
B_F_Z_R_0	0.080393	0.03232725	Vdd
B_F_Z_R_0	$-5.6225e^{-4}$	0.0	Vdds

Table 5.10: Leakage Power for NOR cell

Condition	Leakpower	Supply
A0_B0	0.0020063	Vdd
A0_B0	$7.4792e^{-9}$	Vdds
A0_B1	$9.6073e^{-4}$	Vdd
A0_B1	$1.4052e^{-7}$	Vdds
A1_B0	$6.7704e^{-4}$	Vdd
A1_B0	$3.0405e^{-7}$	Vdds
A1_B1	$1.4104e^{-4}$	Vdd
A1_B1	$2.3253e^{-7}$	Vdds

5.2 Effect of threshold voltage :

Delay increases with the threshold voltage of the MOSFET. The following graph shows the increase in the delay as we move from low threshold voltage (LVT) MOSFET to regular threshold voltage (RVT) MOSFET.

Cell: 2 input NOR (inputs: A, B; output: Z)

Technology: Bulk CMOS (28nm)

Process: Best, Voltage: 0.85V, Temperature: 125°C

Slope: 0.69 ns, output load capacitance C_{load}: 0.0448 pf

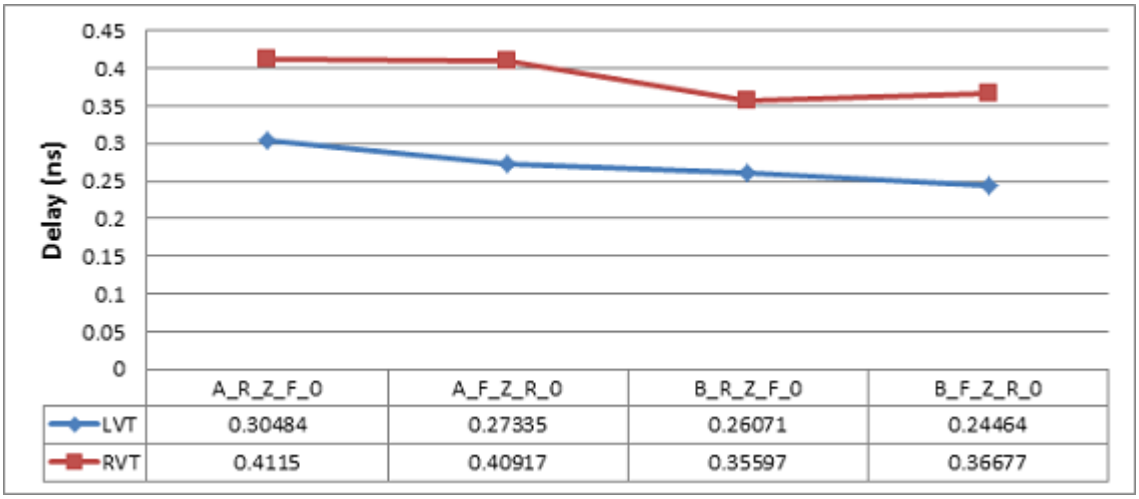


Figure 5.5: Effect of threshold voltage on delay

5.3 Effect of Process :

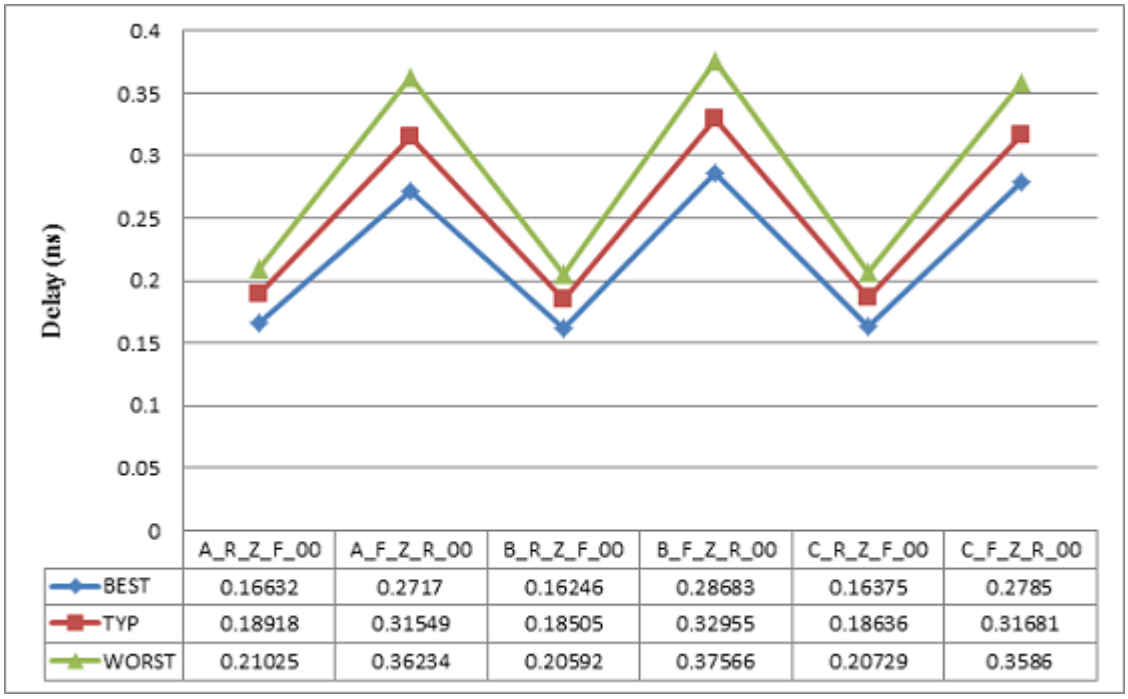
Change in process parameters makes significant impact on MOS performance. The process variation is divided in three categories viz. BEST (FF), TYP (TT) and WORST (SS). The BEST process gives smallest delay but highest power dissipation. In contrast WORST process has largest delay but smallest power dissipation. The effect of process variation is shown in the following graph.

Cell: 3 input NOR (inputs: A, B, C; output: Z)

Technology: Bulk CMOS (28nm)

Process: Worst, Voltage: 0.95V, Temperature: 0°C

Slope: 0.32 ns, Output load capacitance C_{load}: 0.02245 pf



	A_R_Z_F_00	A_F_Z_R_00	B_R_Z_F_00	B_F_Z_R_00	C_R_Z_F_00	C_F_Z_R_00
BEST	0.16632	0.2717	0.16246	0.28683	0.16375	0.2785
TYP	0.18918	0.31549	0.18505	0.32955	0.18636	0.31681
WORST	0.21025	0.36234	0.20592	0.37566	0.20729	0.3586

Figure 5.6: Effect of process variation on delay

5.4 Effect of Temperature :

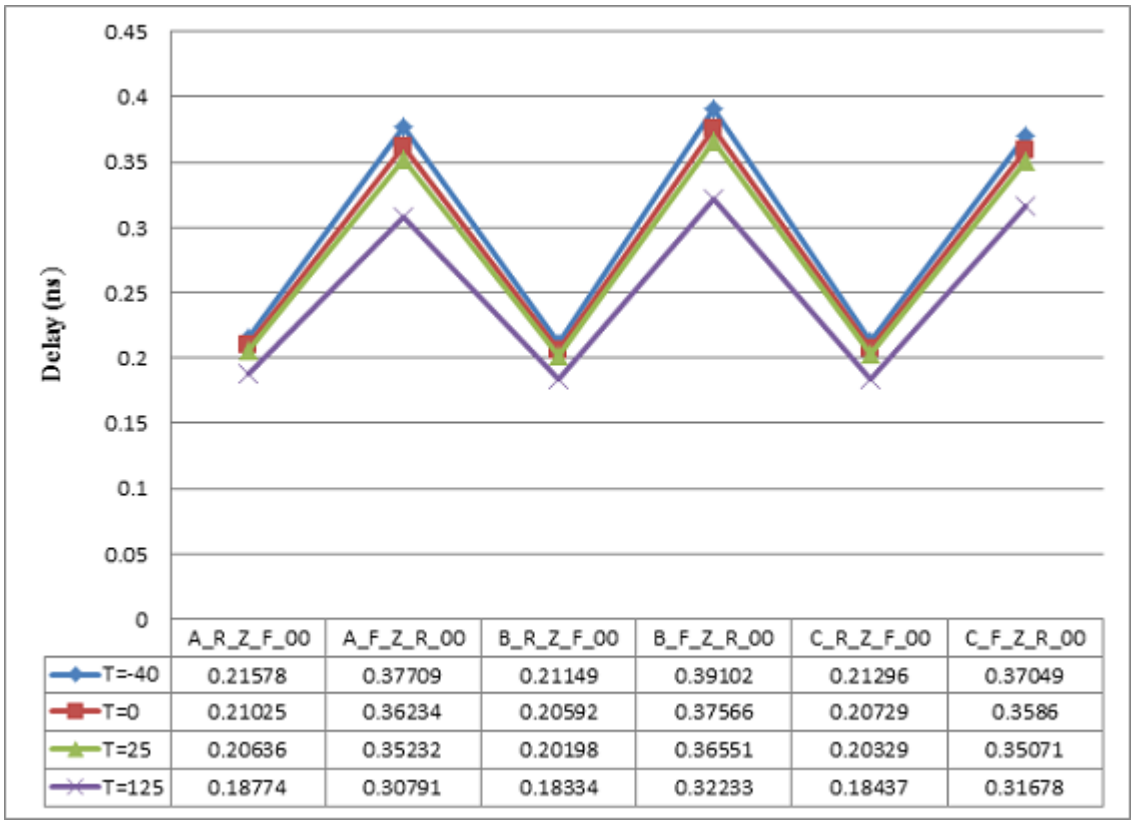
Delay decrease with increase in the temperature. The following graph shows decrease in the delay with rise in temperature.

Cell: 3 input NOR (inputs: A, B, C; output: Z)

Technology: Bulk CMOS (28nm)

Process: Worst, Voltage: 0.95V, Temperature: 0°C

Slope: 0.32 ns, Output load capacitance C_{load}: 0.02245 pf



	A_R_Z_F_00	A_F_Z_R_00	B_R_Z_F_00	B_F_Z_R_00	C_R_Z_F_00	C_F_Z_R_00
T=-40	0.21578	0.37709	0.21149	0.39102	0.21296	0.37049
T=0	0.21025	0.36234	0.20592	0.37566	0.20729	0.3586
T=25	0.20636	0.35232	0.20198	0.36551	0.20329	0.35071
T=125	0.18774	0.30791	0.18334	0.32233	0.18437	0.31678

Figure 5.7: Variation of delay with temperature T (0°C)

5.5 Effect of drive strength :

Drive strength decides the output current supply capability of the cell. So the cell with higher drive strength will have higher output current supply capability. Hence delay decreases with increase in drive strength. The following figure 5.8 shows effect of drive strength on delay in NOR cell.

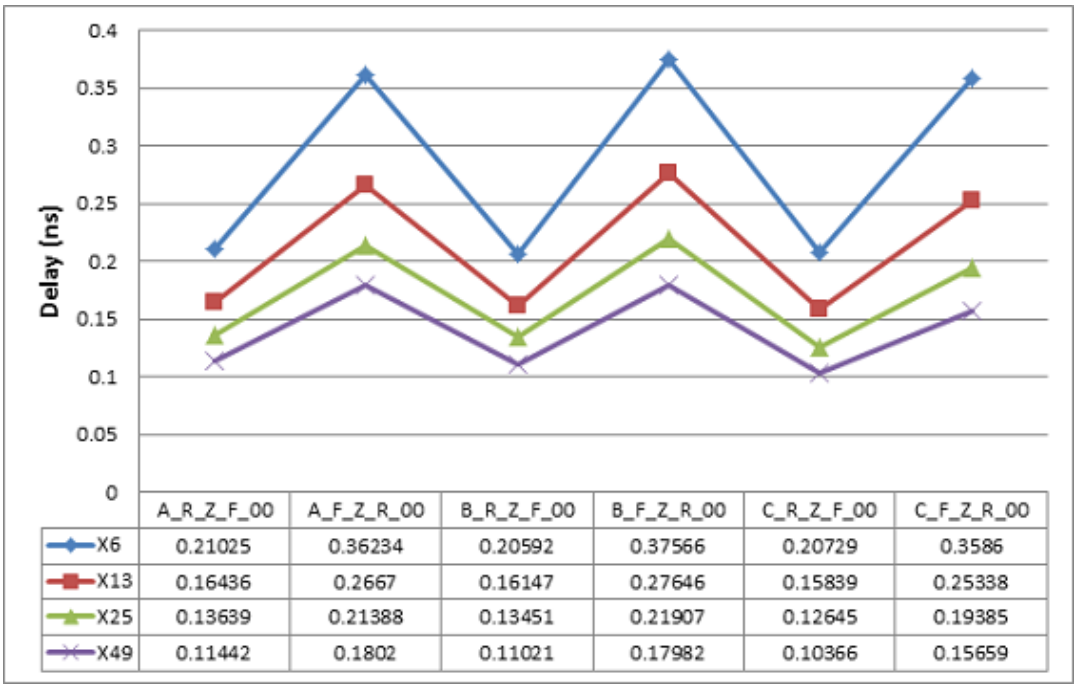
Cell: 3 input NOR (inputs: A, B, C output: Z)

Technology: Bulk CMOS (28nm)

Process: Worst, Voltage: 0.95V, Temperature: 0°C

Slope: 0.32 ns, Output load capacitance C_{load}: 0.02245 pf

In NOR cell pull-up network consist of series combinations of PMOSs. Hence drive strength has more impact on delay during rise transition of output than fall



	A_R_Z_F_00	A_F_Z_R_00	B_R_Z_F_00	B_F_Z_R_00	C_R_Z_F_00	C_F_Z_R_00
X6	0.21025	0.36234	0.20592	0.37566	0.20729	0.3586
X13	0.16436	0.2667	0.16147	0.27646	0.15839	0.25338
X25	0.13639	0.21388	0.13451	0.21907	0.12645	0.19385
X49	0.11442	0.1802	0.11021	0.17982	0.10366	0.15659

Figure 5.8: Effect of drive strength on delay in NOR cell

transition of output. This can be observed from the above graph.

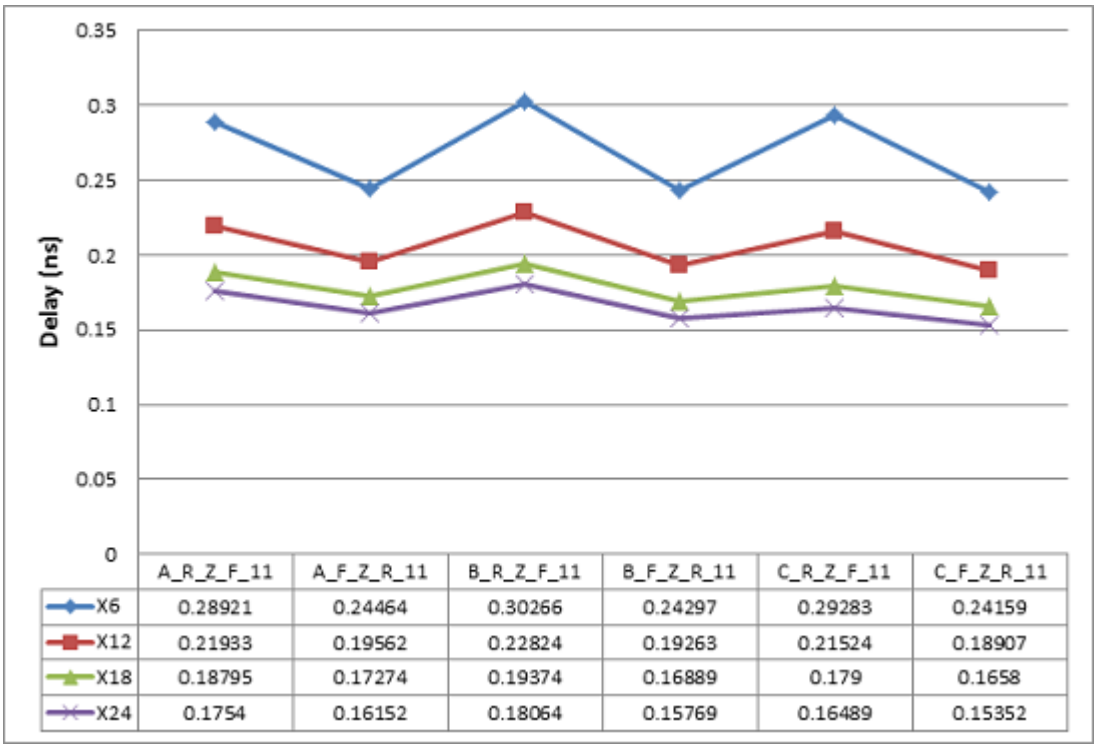
Similarly in case of NAND gate falling edge of the output will have more impact of drive strength as pull-down network has series combination of NMOSs. The following figure 5.9 shows impact of drive strength on delay in NAND cell.

Cell: 3 input NAND (inputs: A, B, C output: Z)

Technology: Bulk CMOS (28nm)

Process: Worst, Voltage : 0.95V, Temperature: 0°C

Slope: 0.32 ns, Output load capacitance C_{load}: 0.02245 pf



	A_R_Z_F_11	A_F_Z_R_11	B_R_Z_F_11	B_F_Z_R_11	C_R_Z_F_11	C_F_Z_R_11
X6	0.28921	0.24464	0.30266	0.24297	0.29283	0.24159
X12	0.21933	0.19562	0.22824	0.19263	0.21524	0.18907
X18	0.18795	0.17274	0.19374	0.16889	0.179	0.1658
X24	0.1754	0.16152	0.18064	0.15769	0.16489	0.15352

Figure 5.9: Effect of drive strength on delay on NAND cell

5.6 Effect of body biasing :

Body biasing is nothing but process of varying the substrate voltage with respect to source. In forward body biasing (FBB) NMOS substrate has positive voltage while PMOS substrate has negative voltage with respect to the source. The forward body biasing improves the speed by reducing the threshold voltage. In reverse body biasing (RBB) the substrate of NMOS is connected to negative bias while substrate of PMOS is connected to positive bias with respect to the source.

Cell: 2 Input NOR (inputs: A, B, output: Z)

Technology: Bulk CMOS (28nm)

Process: Worst, Voltage: 0.85V, temperature: 125°C

Slope: 0.69 ns, Output load capacitance C_{load}: 0.0448 pf

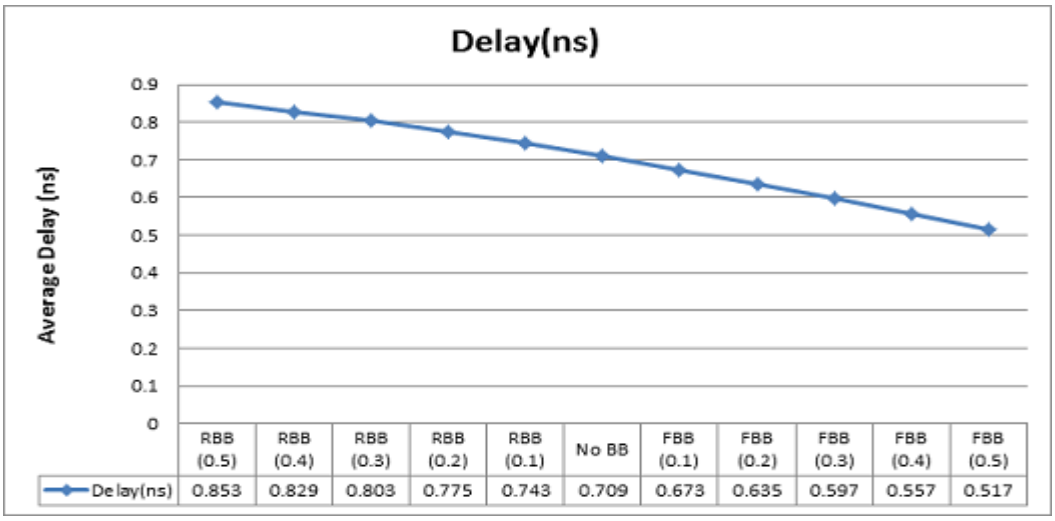


Figure 5.10: Effect of body biasing on Average Delay

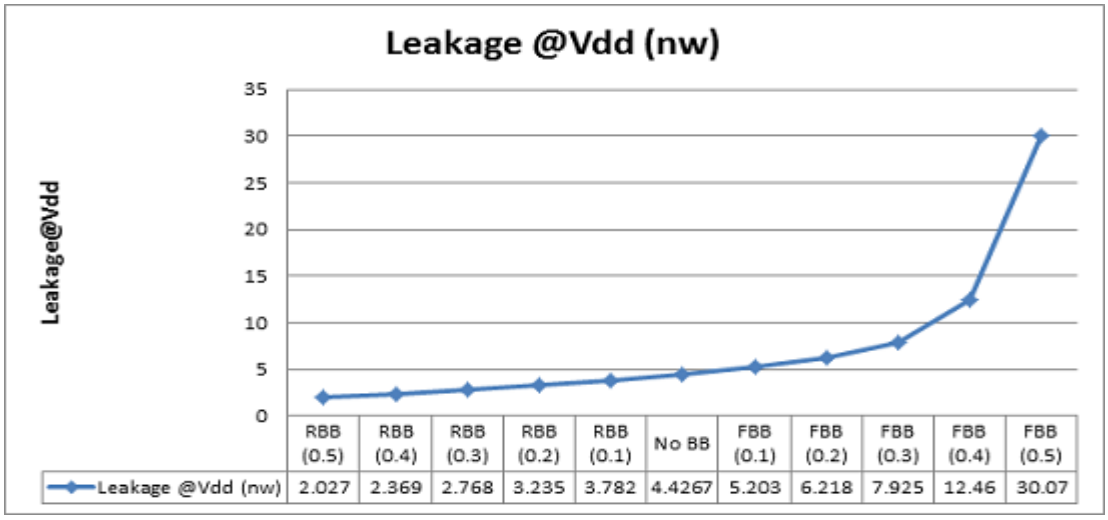


Figure 5.11: Effect of body biasing on Leakage power @Vdd

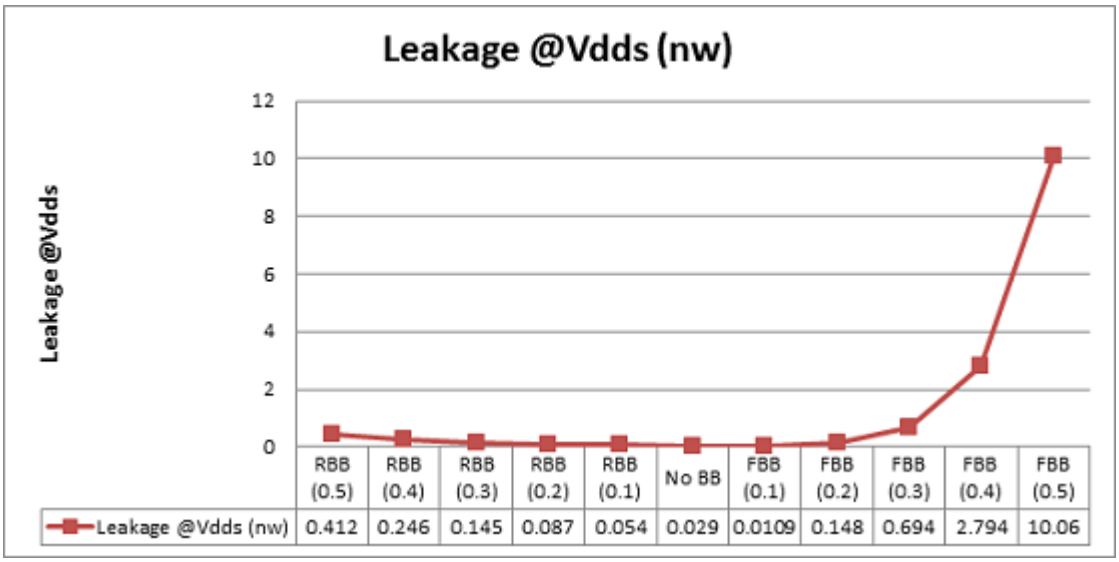


Figure 5.12: Effect of body biasing on Leakage power @Vdds

As seen from the above graphs, for increased Forward Body Biasing (FBB) delay decreases whereas leakage corresponding to both Vdd and Vdds increases. Also it can be observed that FBB above 300mv leakage starts increasing rapidly.

As we go on increasing the RBB although leakage through Vdd is decreasing, the leakage associated with Vdds increases which is undesirable. Also RBB increases delay rapidly, increasing power delay product (PDP).

5.7 Effect of Gate Length biasing :

Cell: 2 Input NOR (inputs: A, B, output: Z)

Technology: Bulk CMOS (28nm)

Process: Worst, Voltage: 0.9V, Temperature: 125°C

Slope: 1 ns, Output load capacitance C_{load}: 0.2384 pf

With increase in the gate length the cell delay increases and leakage power with respect to both Vdd and Vdds decreases.

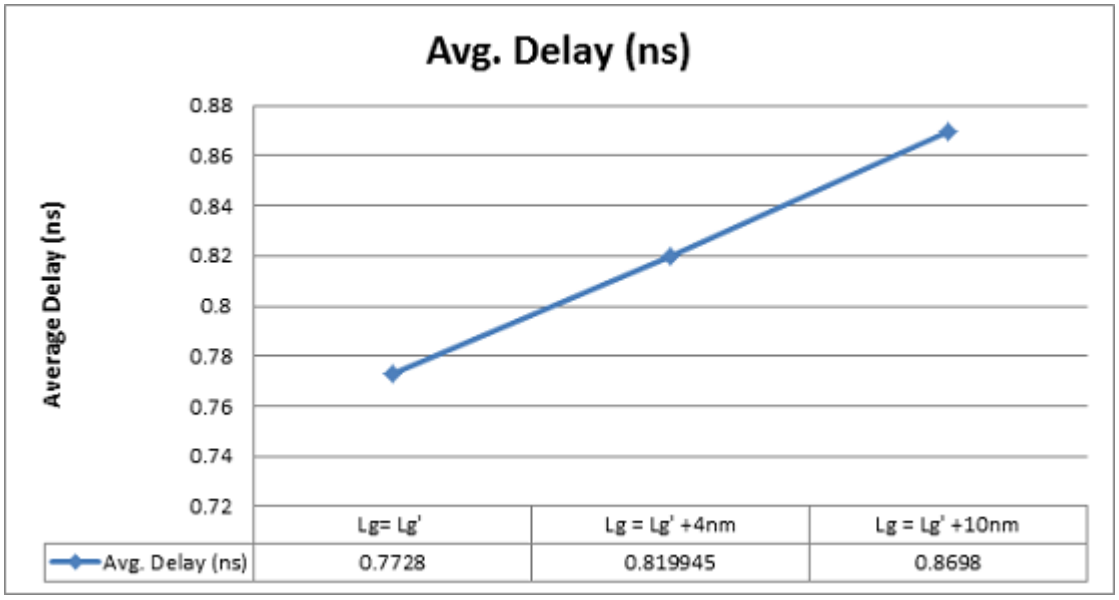


Figure 5.13: Effect of Gate length biasing on Average Delay

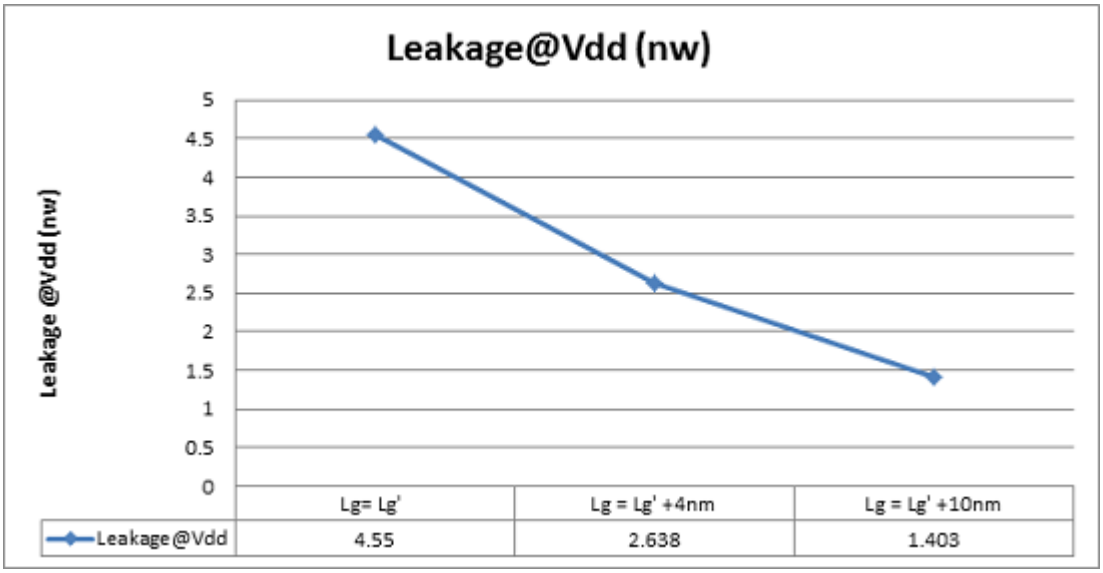


Figure 5.14: Effect of Gate length biasing on Leakage @Vdd

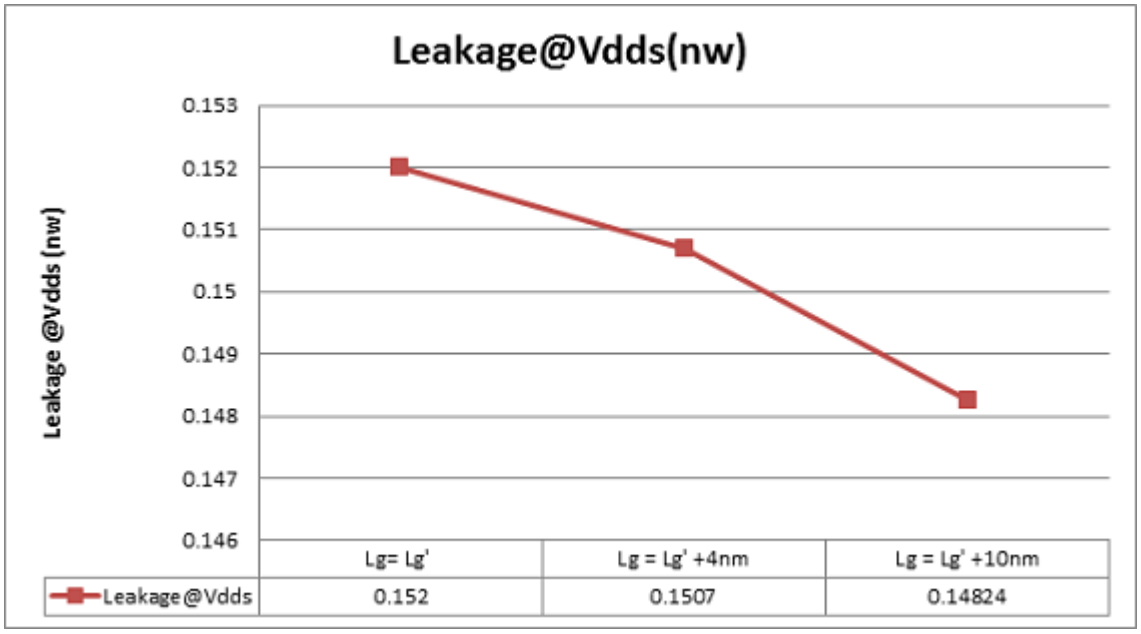


Figure 5.15: Effect of Gate length biasing on Leakage @Vdds

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

The standard cell libraries are the heart of semi-custom ASIC design. The library creation involves two major steps i.e. characterization of standard cells and packaging them in the form of .lib along with documents. The complete characterization and packaging flow is analyzed. Also the methodologies used for delay, power, input capacitance, timing check measurement, etc. are analyzed. The noise and IR drop analysis methods are understood.

The impact of various parameters such as Threshold voltage, Process, Temperature, Drive Strength, Body Biasing and Gate Length on standard cell is analyzed. For analysis purpose AND and NOR cells are characterized.

- Delay increase with the threshold voltage of the MOSFET so delay increase as we move from LVT to HVT.
- As we move from BEST to WORST process delay increase but power dissipation decrease.
- Delay decrease with increase in the temperature for Deep sub-micron technology.

- The cell with higher drive strength will have higher output current supply capability. Hence delay decreases with increase in drive strength.
- For FBB delay decrease and leakage power increase and for RBB delay increase and leakage power decrease.
- With increasing in gate length delay increase and leakage power decrease.

The basic concepts of advanced FD-SOI technology are learned and compare it with the Bulk CMOS technology.

- In the FD-SOI technology 50% perfomance increase at low voltage and 35% performance increase at nominal and high voltage.
- FD-SOI technology cooler then Bulk CMOS technology and it consume 35% less Power at high performance and in standby.

6.2 Future Scope

The work has design and characterization of the 28nm FD-SOI standard cell library. So in future it need to shrink the FD-SOI technology and design the standard cell library in the 14nm & 10nm. Also it need to characterize the library of 14nm & 10nm and analyze the various parameter like area, timing, power etc. and compare it with the previous technology.

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