PMB(Process Monitoring Box) Sensor Development And Verification

Major Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

In

Electronics & Communication Engineering

(VLSI Design)

By

Biral R Patel

(12MECV20)

Under the Internal Guidance of

Dr. Amisha Naik

and

External Guidance of

Mr. Alok kumar Tripathi

Department of Electronics & Communication Engineering

Institute of Technology

Nirma University

Ahmedabad-382 481

Declaration

This is to certify that

1. The thesis comprises of my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

2. Due acknowledgement has been made in the text to all other material used.

Biral R Patel

CERTIFICATE

This is to certify that the Major Project entitled **"PMB(Process Monitoring Box) Sensor Development And Verification"** submitted by **Mr. Biral R Patel (12MECV20)**, towards the partial fulfillment of the requirements for the degree of **Master of Technology in VLSI Design** of **Nirma University of Science and Technology; Ahmedabad** is the record of work carried out by him under our supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for the examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

External Guide

Mr. Alok kumar Tripathi

Manager

Digital Design, TR&D

STMicroelectronics India Pvt. Ltd.

Internal Guide

Dr. Amisha Naik

Sr. Associate Professor

VLSI Design

Nirma University

PG Co-ordinator

Dr. N. M. Devashrayee

VLSI Design

HOD

Dr. P. N. Tekwani

Professor, EE

Director

Dr. K Kotecha

Director, IT-NU

Date: _____

Place: Ahmedabad

Acknowledgement

I would have never succeeded in completing my Thesis without the cooperation, Encouragement and help provided to me by various people.

Firstly, my sincere thanks to the Digital Design team, especially the PMB(Process Monitoring Box) team, for their help during this training. Their wisdom, clarity of thought and support motivated me to bring this project to its present state.

I am highly indebted to my Group manager **Namerita Khanna** project manager, **Mr. Alok kumar Tripathi**, my immediate supervisors **Mr. Surendra kumar** and **Mr. Rohit Goel** for providing necessary information regarding the project and also for their constant guidance, supervision, kind co-operation, and invaluable support in all aspects. My thanks and appreciations also go to my colleagues and team members in developing the project and for providing me with a lively and energetic work environment.

I would like to express my sincere gratitude to **Dr. Ketan Kotecha** (Director, Nirma University, Ahmedabad) for his continuous guidance, support and enthusiasm. I would take this opportunity to thank **Dr. P. N. Tekwani** (Head of Department, Electrical Engineering), **Dr. N. M. Devashrayee** (Professor and Program Coordinator, M.Tech - EC (VLSI Design)), Internal Guide **Dr. Amisha Naik** (Sr. Associate Professor, M.Tech - EC (VLSI Design)) and all the faculties at **Nirma University (VLSI Design)**, for their vision and relentless effort, support, and encouragement to provide me with this excellent opportunity to carry out my project work in such a highly renowned and esteemed organization, ST Microelectronics. I am equally thankful to **ST Microelectronics** for providing me the invaluable exposure to the industry and the current market trends.

Finally, I would like to express my heartfelt thanks to my parents and colleagues for their blessings and for their constant love and support.

Biral R Patel

(12MECV20)

Abstract

PM CONTROL is a sensor to be used for process monitoring, on chip compensation to save power. It measures the performance of the chip in terms of leakage power and speed. The process monitoring can be used at EWS (wafer level test) to check that the chip remains within predefined process limits or at application level during product lifetime for temperature monitoring, compensation, debug and failure analysis. Each process option is measured with a dedicated sensor including two oscillators. One oscillator measures the speed of NMOS and PMOS separately and other measures the leakage.PM CONTROL supports two types of sensors, NON-CPR and CPR sensors. CPR sensor which is used for critical path's transistors performance measurement and RC interconnect effect measurement. Unlike the PMB NON-CPR sensors, has two rings implemented as a hard macro and soft macro. PMB sensor integrated inside chip. Sensor integrated on chip which is connected to PMB wrapper.PMB wrapper is interfaced with PMB controller. So, PMB sensor integrated on chip accessed through PMB controller.PMB controller can be operated in three different mode JTAG mode, APB interface and parallel mode.

As circuit becomes larger and more complex and the technology moves to lower nodes, manual creation of the digital modules of these design become more difficult. To simplify and speed up the design process, synthesis and place-and-route tools are used to automate much of the design of the digital domain. To support this requirement my work also moves around development of such standard cell libraries.

The internship mainly involved backend verification of PMB sensors and making layouts of Standard cell libraries from given schematics and packaging PMB libraries. In the flow, firstly the schematics are made. Then layouts are made from the schematics. I am responsible for DRC, LVS , DFM and LFD issues regarding these layouts. Then CDL and GDS files extracted from the schematic and layout. Apart from this, i am responsible for cad data generation using eldo simulator and have to check voltage sensitivity, rc impact and temperature sensitivity of PMB

sensor.

ST Microelectronics At A Glance

- A world leader in providing the semiconductor solutions that help our customers improve quality of life for everyone, both today and in the future
- Among the world's largest semiconductor companies
- A leading Integrated Device Manufacturer serving all electronics segments
- A leading technology innovator (around 12,000 researchers approx. 21,500 patents)
- Key strengths in Multimedia Convergence, Power Applications and Sensors
- Rich, balanced portfolio (ASICs, Application-Specific Standard Products and Multi-Segment Products)
- A pioneer and visionary leader in sustainability
- President and CEO: Carlo Bozotti
- 2011 revenue $9.73 billion
- Approximately 50,000 employees including STEricssion at December 31, 2011
- Advanced research and development centers in 10 countries
- 12 main manufacturing sites
- Corporate Headquarters Geneva, Switzerland

- Global presence with sales offices all around the world
- Public since 1994 - shares traded on New York Stock Exchange (NYSE: STM), Euronext Paris, and Borsa Italiana
- Created as SGS-THOMSON Microelectronics in June 1987, from merger of SGS Microelettronica (Italy) and Thomson Semiconducteurs (France)
- Renamed ST Microelectronics in May 1998

Group Introduction

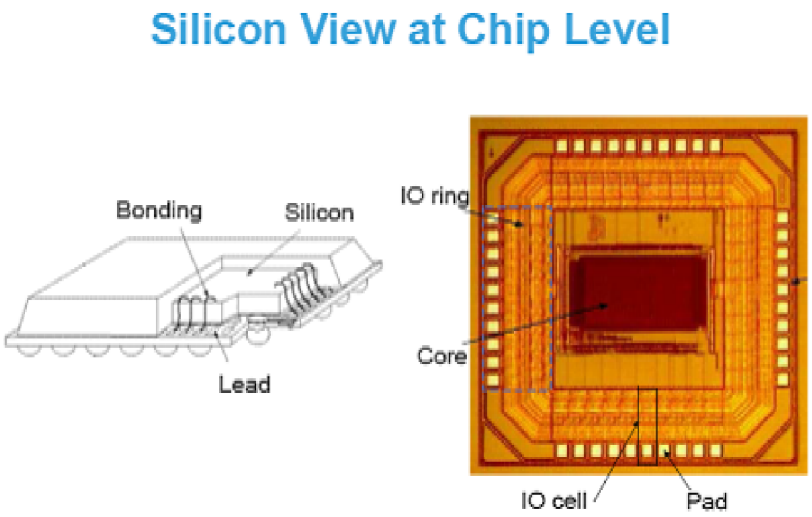
The TR&D is a group in ST which works on integrated products (IPs). Its work is to provide quality Library Solutions and services to divisions, in the company's drive in time to market, IP Reuse and Super Integration. There are various types of IPs:

- Digital Design : It is the layout of basic sequential and combinational circuits which are used to make bigger circuits. It is the basic building block of all the circuits. It is a component within an integrated circuit with known functional and timing characteristics, which can be used as an element in building a larger circuit. Example of standard cells include Inverter, Flip-flop (FD), Latch (LD), Multiplexer (MUX), NAND, NOR, AND, OR, XOR, XNOR, Full Adder (FA), Half Adder (HA).PMB is to be used for process monitoring, on chip compensation to save power.The process monitoring can be used at EWS (wafer level test) to check that the chip remains within predefined process limits or at application level during product lifetime for temperature monitoring, compensation, debug and failure analysis.leakage.PM CONTROL supports two types of sensors, NON-CPR and CPR sensors.

- Memories : A device or an electrical circuit used to store a single bit (0 or 1) is called a memory cell. Examples of memory cell are flip flop, a charged capacitor etc. Semiconductor memories are capable of storing large amount of Digital information. The amount of memory required in a particular system depends on the type of application but the no. of transistors required for storage of data are always much larger than the no of transistors used for logic operations and other purposes. The ever increasing demand of high storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently towards higher data storage densities.

- I/Os (input/output cells) : I/O's are the input/output cells, placed on the

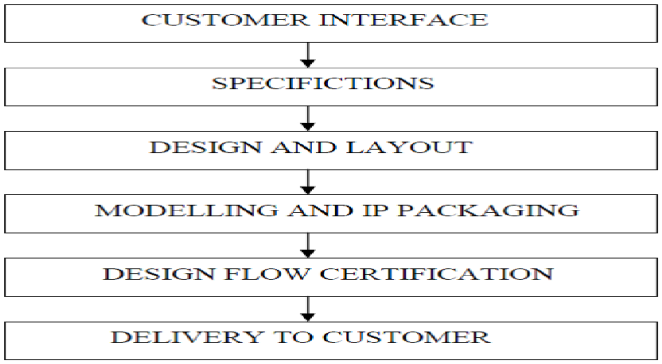
periphery of the chip. Any I/P signal which comes from off-chip environment (external voltages are at a typical voltage Vdde level of 2.5V, 3.3V or 5V) is connected to the core (logic part of the chip) is connected through them and vice versa.



- Developement Flow : The customer, as per his requirements, gives the specifications to the flow team. These requirements are analyzed and as the needs, the features required for the design are noted. These are sent to the Back End Team for the designing. After the design is ready, it is checked for the specifications and then sent to the Front End for the characterization and functional modeling.

- Concept Of Library : A library is collection of cells all of which reference the same technology file. The cells are the smallest functional unit. Attached to every library is a technology file. A technology file is a large data file that specifies, in one central location, all of the technology-dependent parameters associated with that particular library. The purpose of library is to reduce the design cycle of the designer.

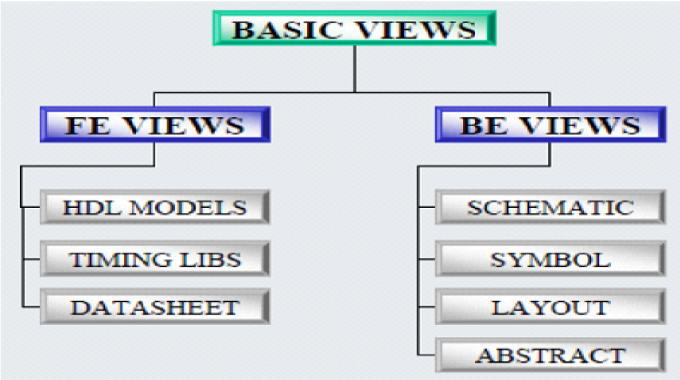
  – Basic building blocks: Digital (AND, OR); Analog (amplifier).



- Complex building block: Digital (Microcontroller); Analog (PLL, DAC).
- Memories: Single or dual port SRAM, ROM etc.

The cells are delivered as a set of different views. These views are used by different tools in a given Design flow. These cells are used until the physical implementation.

- Cell Views : A particular representation of a cell is referred to as a view. Each cell may have a layout view, schematic view, symbolic view, timing view, etc. Each view object has attached property objects that are specific to the view, such as grid units, scale and display of axes etc. A cell is delivered as a set of view and each view is used by a different tool in a given design flow.



- BE (Back End) VIEWS: Views Related to the Physical Design of a Cell

– FE (Front End) VIEWS: Views Related to the Timings/Modeling of the Cell the various views can also be classified as Primary and Secondary views.

Contents

List of Figures

Chapter 1

Introduction

A Cell is a group of transistor and interconnect structures, which provides a Boolean logic function or a storage function (flip-flop or latch). A cell library is a collection of cells with functions such as AND, OR, INVERT, flip-flops, latches and buffers. These cells are realized as fixed height, variable width full custom cells. The cells are typically optimized full custom layouts, which minimize delays and area.

RTL design into a large collection of lower-level constructs called standard cells. These constructs are taken from a standard-cell library consisting of pre-characterized collections of gates (such as 2 input nor, 2 input NAND, inverters, etc.). The standard cells are typically specific to the planned manufacturer of the ASIC.

The resulting collection of standard cells, plus the needed electrical connections between them, is called a gate-level Netlist. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. The gate-level netlist is next processed by a placement tool which places the standard cells onto a region representing the final ASIC. It attempts to find a placement of the standard cells, subject to a variety of specified constraints. The routing tool takes the physical placement of the standard cells and uses the netlist to create the electrical connections between them. Given the final layout, circuit extraction computes the parasitic resistances and ca-

pacitances. In the case of a digital circuit, this will then be further mapped into delay information, from which the circuit performance can be estimated, usually by static timing analysis. This, and other final tests such as design rule checking and power analysis (collectively called signoff) are intended to ensure that the device will function correctly over all extremes of the process, voltage and temperature.

When this testing is complete the information is released for chip fabrication. This report ad-dresses the various issues come into sight while developing a cell library.

1.1 STD Cell Based ASIC Design

A cell library is a collection of low level logic functions such as AND, OR, INVERT, flip-flops, latches and buffers. These cells are realized as fixed height, variable width full custom cells. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. The cells are typically optimized full custom layouts, which minimize delays and area.

It is the most common ASIC development technology. Each standard cell vendor has its own library of circuits that range from primitive logic gates to more complex functions Based on the customer's design, the required circuits are placed on the chip and connected using "place-and-route" software. ASIC vendors provide a library of pre-characterized cells that the customers can use to implement their design.

Advantage

- It provides the best design flexibility.
- High performance and High density.
- Low power consumption.

Limitation

- With smaller geometries, the mask costs have increased exponentially and fabrication turnaround time has become longer.
- Not economically viable except for very large volume production.

1.2 System Reference

Power management is becoming an increasingly urgent problem for almost every category of design, as power density measured in watts per square millimeter rises at an alarming rate. Because of the increased circuit speed and density, power consumption in CMOS VLSI chips, due to global warming effects and other environmental impacts. Power is emerging as the most critical issue in system-on-chip design today.

The technology development now not only driven to improve the circuit speed and density, but also concentrating on reducing the power consumption. It is important to have detailed understanding of the power consumption behavior of a chip, such as controlling the power consumption in a digital CMOS VLSI chip, the dominant part of power consumption in different parts of the chip and reducing power consumption during the early design phase and controlling the power consumption of IC.

The controlling of the power consumption of IC and its associated variability while warranting their functionality is now one of the major challenges in integrated system design. The process induced variability, which is a matter of a few atoms or less, appears as an important additional issue that cannot be neglected. Indeed, leakage power varies now exponentially with key process parameters such as gate length, oxide thickness, threshold voltage, in addition to variability related to local transistor environment and wires including circuit layout, pattern dependency and density.

This increasing variability has led designers to introduce additional design margins which increases pessimism and thus reduces both timing and power performances. To overcome the variability issue, a close cooperation between system design and technology development teams is required for the future technology nodes as technological solutions can no longer compensate for all the effects of scaling.

In order to reduce the power consumption, the process control techniques combined with on-chip performance monitoring and compensation technique for reducing power consumption, maintaining a reasonable margins and maximizing the number of chips that will meet power and delay constraints. The design used to monitor power consumption of IC's is called Process Monitoring Controller.

1.3 About Project: PMB Sensor

PM CONTROL is efficient method to send or receive the on chip process data. The process monitoring can be used at Wafer Level Test to check that the chip remains within predefined process limits, for monitoring temperature, compensation and debug and failure analysis.

PM CONTROL is a cell to be used for process monitoring, on chip compensation technique for reducing the supply voltage of fast circuits in order to reduce the power consumption and also for maintaining the specified operating frequency.

Each process option is measured with a dedicated sensor including two oscillators. One oscillator measures the speed and the other measure the leakage. In addition, the speed measurement is done separately for N and P mos. Each oscillator provides a numerical value that can be accessed through a JTAG interface or APB interface or direct access to data and control registers. Those values can then be compared to predefined limits to measure the process of each individual chip.

Post silicon tuning technique now recognized as mandatory for the design of low power and/or high speed circuits in advanced technologies, their use require the definition and the qualification of sage post silicon design and test flows. These

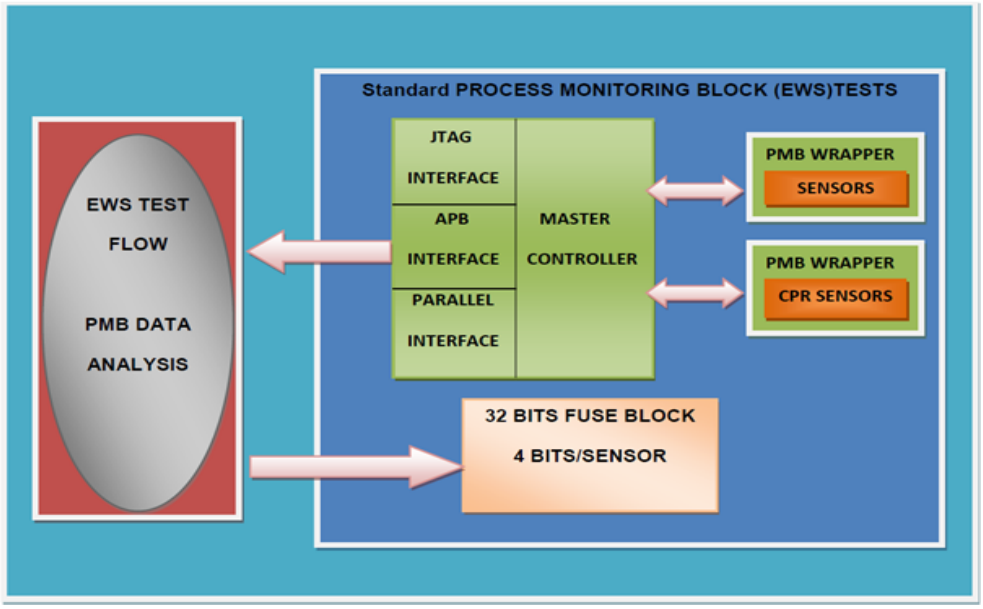


Figure 1.1: Design Implementation

flows, to be efficient, must target the best tradeoff between delays, flexibility and design overhead in addition to exhaustive validation method at each step of the flow.

Chapter 2

Tools Information

2.1 ELDO Simulator

The ELDO analog simulator is the core component of a comprehensive suite of analog digital and mixed-signal simulation tools.

2.1.1 Analog Simulation Capabities

Eldo offers a unique partitioning scheme allowing the use of different algorithms on differing portions of design. It allows the user a flexible control of simulation accuracy using a wide range of device model libraries, and gives a high accuracy yield in combination with high speed and high performance.

2.1.2 Waveform Analysis

The EZwave graphical post-processor enables waveform analysis and post-processing. The native waveform format of EZwave, called wdb, is extremely efficient for manipulating huge databases. EZwave can load gigabytes of data in seconds. EZwave can also load most popular waveform formats, and operates on both analog and digital signals.

2.1.3 Eldo Simulation Flow

The following flow describes the Eldo simulation process.

- Setup a netlist with the circuit description and simulation options and commands
- Run Eldo on the netlist to simulate your design
- Analyze the results of your simulation during or after simulation

2.1.4 Eldo Input And Output Files

Figure shows the input files that must be provided for an Eldo simulation run and the main output files that Eldo produces.

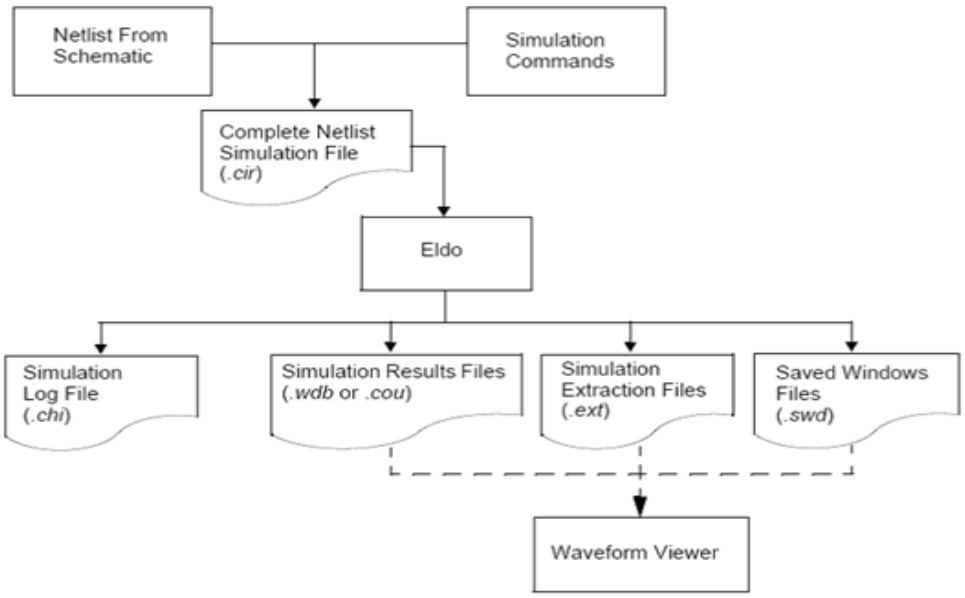


Figure 2.1: Eldo input output flow

2.1.4.1 Input File

Filename.cir The main Eldo control file, containing circuit netlist, stimulus and simulation control commands. This file is SPICE compatible, the Eldo control

language being a superset of the Berkeley SPICE syntax.

To run an Eldo simulation, a .cir control file must be supplied to the simulator. This file must include the following:

- netlist which is used for circuit connectivity
- Model parameter values defining the specific device models to be used.
- Electrical stimuli sources.
- Simulation options and commands.

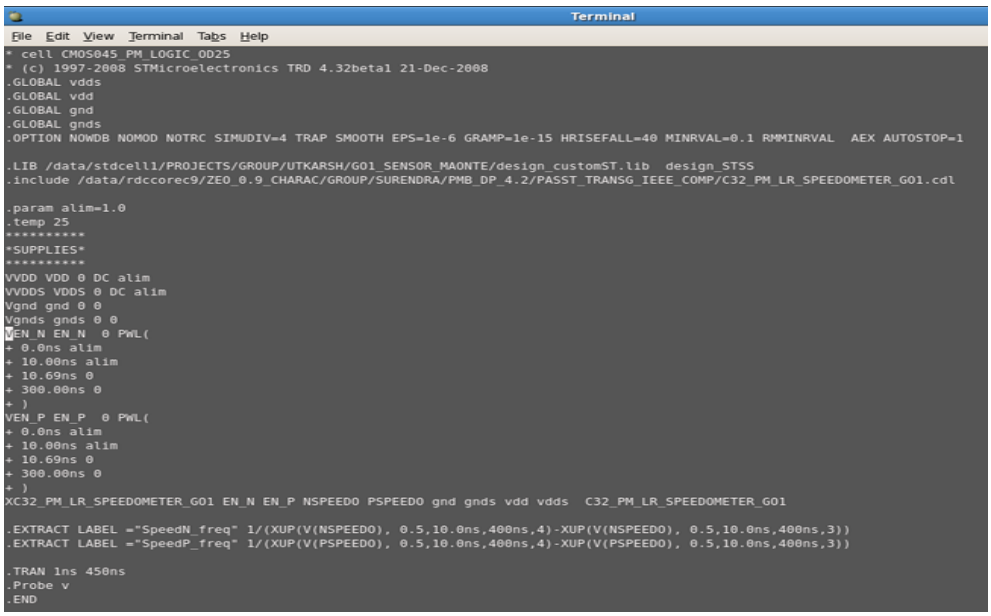


Figure 2.2: sample netlist

2.1.4.2 Output Files

SPICE compatible output log file containing ASCII data, including results and error messages. filename.wdb A binary output file for mixed-signal JWDB format files. This is always generated by default. Viewed with the EZwave waveform viewer. By default, using the .wdb format, the .EXTRACT and .MEAS waveforms

are also saved inside the EXT folder in the main .wdb file. Waveforms defined by .DEFWAVE commands combined with .PLOT are saved inside the appropriate analysis folder in the main .wdb file. filename.swd A saved windows file used by the EZwave waveform viewer. This file contains information on waveforms and their display and cursor settings, window format settings and complex waveform transition settings.

2.1.5 Simulation Results

After the simulation has been completed, Eldo writes simulator information to the .chi file. This file will contain details of the simulation including any warning or error messages, which may have been encountered during simulation. A binary .wdb file is also generated by default as an output of simulation. You can view the results written to the .wdb file with the EZwave viewer. The .wdb file can be opened in the EZwave viewer the using the following command: ezwave filename.wdb

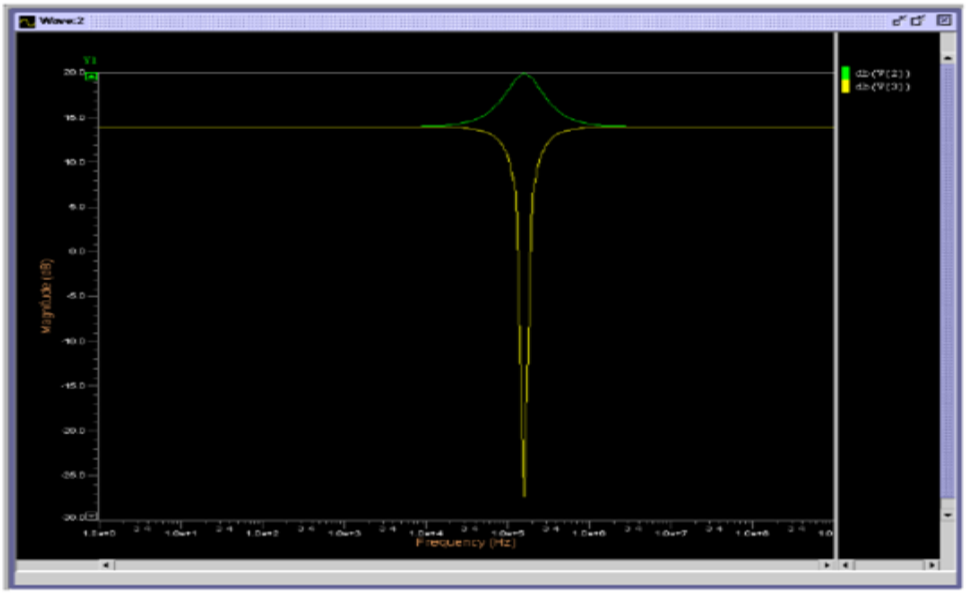


Figure 2.3: ezwave waveform

2.2 Cadense Virtuoso

2.2.1 Introduction

Cadence is an Electronic Design Automation environment which allows different applications and tools to integrate into a single framework thus allowing to support all the stages of IC design and verification from a single environment. These tools are completely general, supporting different fabrication technologies.

2.2.2 Benefits

Easy creation and navigation of complex designs with unlimited hierarchy support coupled with a multi-window editing environment. Accelerated layout entry using easy-to use and easily accessed editing functions Increased productivity and design optimization using P cells Efficient, high-performance handling of large designs using the Open Access database.

2.2.3 Various Design Steps

- Firstly a schematic view of the circuit is created using the Cadence Composer Schematic Editor. Alternatively, a text netlist input can be employed.
- Then, the circuit is simulated using the Cadence analog simulation environment.
- Once circuit specifications are fulfilled in simulation, the circuit layout is created using the Virtuoso Layout Editor. The resulting layout must verify some geometric rules dependent on the technology (design rules). For enforcing it, a Design Rule Check is performed.
- Then, the layout should be compared to the circuit schematic to ensure that the intended functionality is implemented. This can be done with a Layout Versus Schematic check.

- Finally, a netlist including all layout parasitics should be extracted, and a final simulation of this netlist should be made. This is called a PostLayout simulation, and is performed with the same Cadence simulation tools. Once verified the layout functionality, the final layout is converted to a certain standard file format depending on the foundry GDSII, CIF using the Cadence conversion tools.

Chapter 3

Montecarlo Analysis

Monte Carlo analysis determines the uncertainty in estimates for dependent variables of interest. It focuses on data and how uncertainty in data propagates through computations. Eldo reads a netlist describing the circuit and translates it into mathematical equations. The inputs are the various design parameters, the process parameters, and the environmental conditions. The output space is characterized by the circuit performance of interest. Monte Carlo-based uncertainty analysis is performed on multiple model evaluations with randomly selected model input variables. The results of these evaluations (experiments) are then used to determine the uncertainty in model predictions, and the input variables that gave rise to this uncertainty. In order to use Monte Carlo analysis in Eldo, you must do the following:

- Provide a working netlist with one or more user-defined circuit performances based on other analyses

- Specify the .MC statement in the netlist.

- Introduce some statistical variations on circuit parameters, model parameters and/or environmental conditions.

3.1 Specifying Statistical Variation

Generally, models are written as functions of both process parameters and geometrical parameters.

3.1.1 Process Parameters

These parameters determine the behavior of the instantiated devices, such as junction depths, sheet resistances, dielectric thickness and doping levels.

3.1.2 Montecarlo Input File

filename.cir here includes some extra options to specify monte carlo simulation. To specify a Monte Carlo analysis, include a .MC statement in your netlist. Optional parameters for run-length (or convergence) control, the control of graphical output in EZwave, and the sampling algorithm can be specified. The NRUNMAX argument is mandatory: .MC NRUNMAX (RUN CONTROL PARAMETERS)(OUTPUT CONTROL PARAMETERS)(SAMPLING METHOD PARAMETERS)

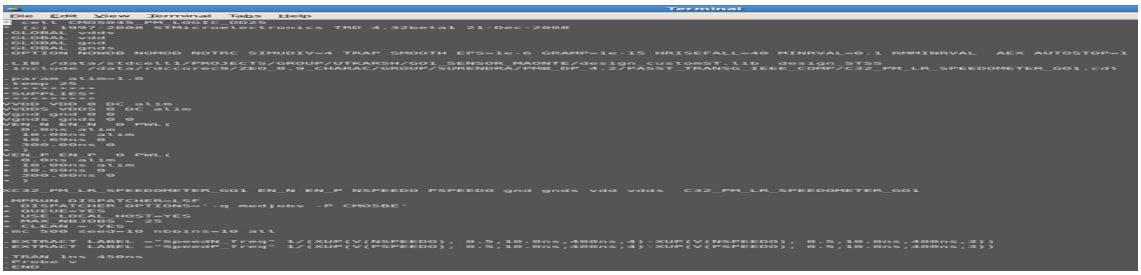


Figure 3.1: sample montecarlo run cir

3.2 Montecarlo Result

500 runs to calculate frequency of nmos and pmos in a circuit and then frequencies are plotted on a graph. Then percentage deviation of all corners i.e., SS, SF,

FS, FF with respect to TT corner is calculated for further analysis.

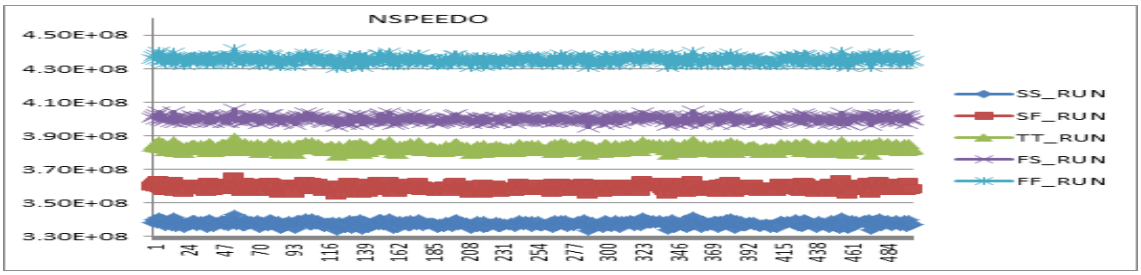


Figure 3.2: nmos frequency

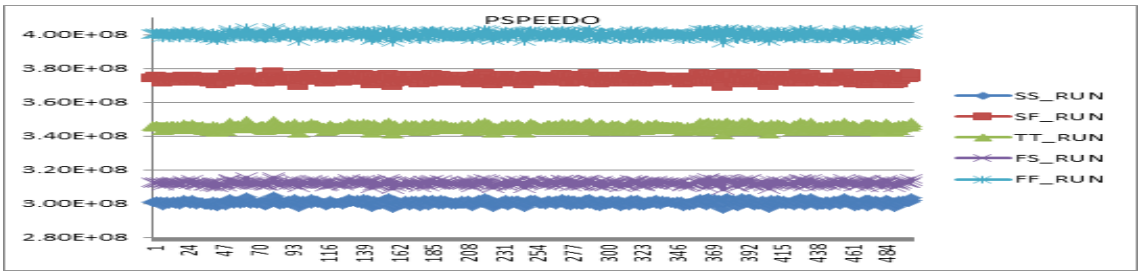


Figure 3.3: pmos frequency

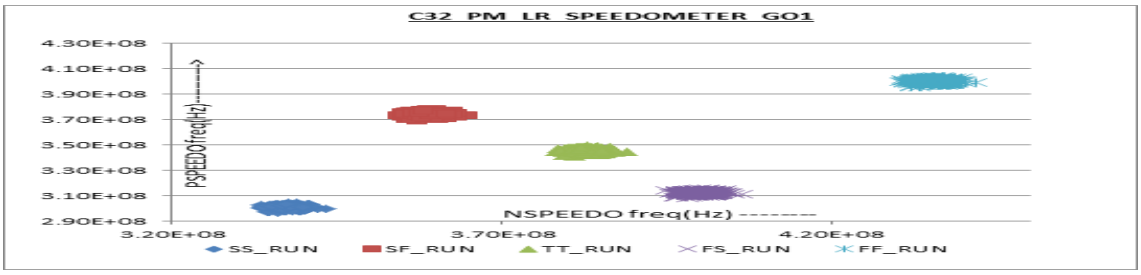


Figure 3.4: nmos vs pmos frequency

Chapter 4

Standard Cell Library

4.1 Standard Cell

A Standard Cell is a group of transistor and interconnect structures that provides a Boolean logic function (e.g., AND, OR, XOR, XNOR, inverters, Full Adder, Half Adder) or a storage function (flip flop or latch).Standard cell is a component performing a basic function. More a digital design concept comprising of Boolean and basic function (AND, OR). It is the layout of basic sequential and combinational circuits which are used to make bigger circuits. Standard cell is a component within an integrated circuit with known functional and timing characteristics, which can be used as an element in building a larger circuit. They are logic units of any digital circuit of same geometry (fixed-height, variable-width).

4.2 Standard Cell Library

A Standard Cell Library is a consolidated data used in designing a SoC. These libraries contain logic cells that are the building blocks for automation design tools. It is a collection of low-level logic functions such as AND, OR, INVERT, flip-flops, latches, and buffers. The key aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated

digital layout. Standard cell Libraries often provide a huge number of cells, up to 300 or even 500. The standard cell libraries provide three separate architectures, high-speed (HS), high-density (HD) and ultra high-density (UHD), to optimize circuits for performance, power and area tradeoffs. There are various types of libraries:

- Core Libraries. (group of standard cells performing basic logic function like: AND,OR etc
- IO Libraries. (group of cells called IO buffers)
- Memories. (these contain memories of various architectures like: SRAM etc)
- Analog and Mixed Signal. (PLL, DAC etc)

4.3 Special Purpose Cell Used For PMB Sensor

4.3.1 Tie-high and Tie-low cells

Tie-high and Tie-low cells are used to connect the gate of the transistor to either power or ground. In deep sub micron processes, if the gate is connected to power/ground the transistor might be turned on/off due to power or ground bounce. The suggestion from foundry is to use tie cells for this purpose. The cells which require Vdd, comes and connect to Tie high (so tie high is a power supply cell); while the cells which want Vss connects itself to Tie-low.

4.3.2 Antenna protection cells

Antenna rules are required by some IC manufacturers to ensure that the transistors of the chip are not destroyed during fabrication. In such processes, the wafer is bombarded with ions in order to create the polysilicon and metal layers. These ions must find a path through the wafer (to the substrate and active layers at the bottom). If there is a large area of poly or metal, and if it connects ONLY to the

gates of transistors (not to source or drain or any other active material) then these ions will travel through the transistors. If the ratio of the poly or metal layers to the area of the transistors is too large, the transistors will be destroyed due to a buildup of charge.

4.3.3 Decap Cells

Decap cells are basically capacitors used for decoupling. The gates in a circuit consume most power (dynamic) only at the clock edges. No voltage source is perfect hence glitches are produced on the power line due to huge current draw at the clock edges. Decap filler cells are small capacitors which are placed between vdd and ground all over the layout. All these small capacitors add up to a big capacitor between vdd and ground. This helps to smoothen out the glitches.

4.3.4 Bus-Hold Cells

The bus-hold cell can act as a memory element in a synchronous pipeline easing the timing constraints placed on adjacent LSI devices. This feature does have its own drawbacks in mixed voltage systems and must be used with caution.

4.3.5 Transmission gate cells

These cells are fast in terms of timing and any functionality can be implemented with fewer logic gates but have a low reliability as far as driving capability is concerned and also, there is a concern for back current.

4.3.6 Tristate buffers and invertors

These are used to reduce glitch transitions with the help of its enable input. So, need to be used cautiously as it brings overhead with it in terms of larger layout footprint and characterization effort.

4.3.7 Level shifters

Level-shifters are used to communicate between the two voltage islands and have a functionality of buffer with much larger area, slower timing and more power consumption as compared to a normal buffer. So, need to be cautious to get them used only when required; otherwise could get used for buffer and die size increases exponentially.

4.3.8 Delay Cells

Delay cells are used specifically for providing a particular delay and also expecting its variation of delay across the corners to be very minimal. So, these are special customized cells designed with much larger layout footprint as compared to a normal buffer.

4.3.9 Filler Cells

Filler cells are used for connecting the gaps between the cells after placement and to maintain the uniformity.

4.4 Cell Characteristics

- Structure- The cell, bus, and pin structure that describes each cells connection to the outside world.
- Function- The logical function of every output pin of each cell that digital design tools use to map the logic of a design to the actual technology.
- Process- The scaling factor accounts for variations in the outcome of the actual semiconductor manufacturing steps. Corners are FF(fast fast) SS (slow slow) TT(typical typical).
- Temperature- The ambient temperature in which the design is to operate.

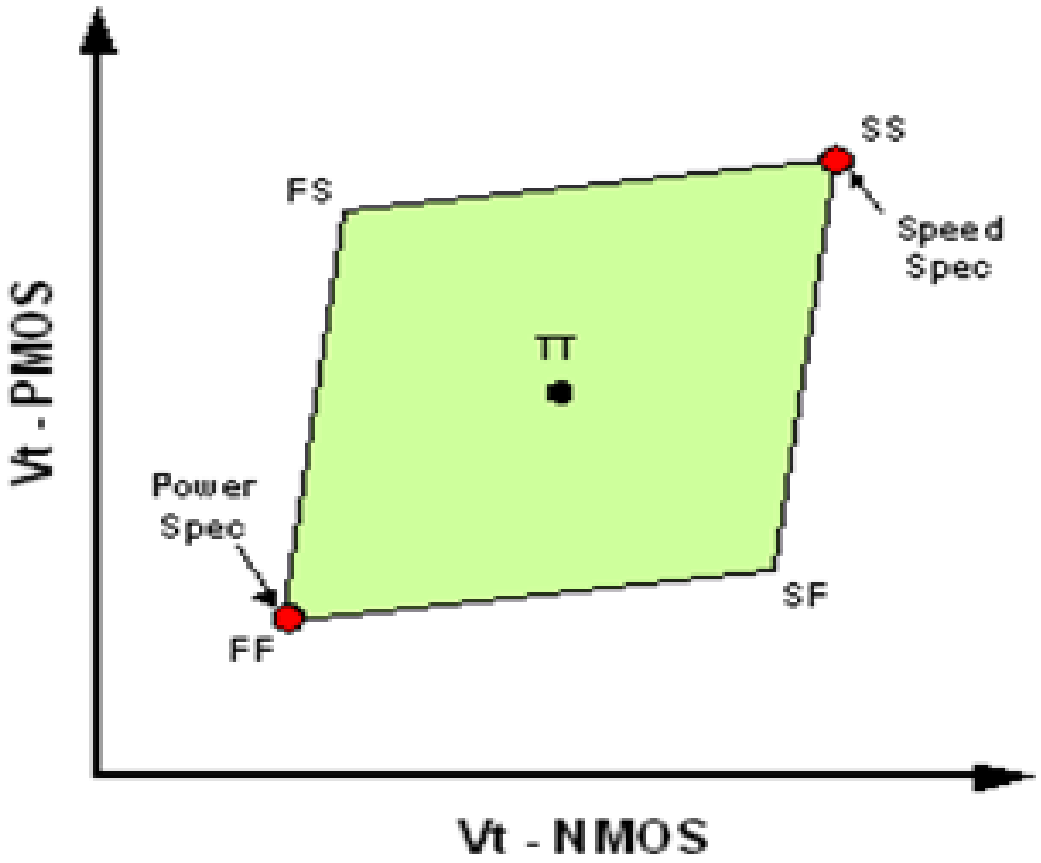


Figure 4.1: Process Corners

- Voltage- The operating voltage of the design.
- Power rail- The voltage value for a power supply.
- Drive Strength- The greater the number of devices (gates and interconnects) connected to a net, the greater drive strength required to sustain maximum clock speed. As a result, there is a need to design cells with a wide range of buffer drive strengths in the library, in order to support the synthesizer and PR tool in the optimal buffering of large nets. A 2X cell drives twice the load driven by 1X cell, a 4X twice that of a 2X and so on.
- Performance properties- The standard cell libraries include multiple voltage

threshold implants (VTs) at most processes. HVT stands for high threshold, SVT stands for standard threshold and LVT stands for low threshold transistor cells. This is used for leakage power optimization.

- Slack- Slack is nothing but the propagation time difference of a path and what is seen practically. If slack is negative then timing violation occurs in the design, if slack is zero then design is working critically and if its positive then there is no timing violation.

4.5 DRC Problems

Design Rules are a series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of a mask set. Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that most of the parts work correctly.If the spacing is not 'X' between two metals then there will be one error for this. As shown in figure below when any metal line with its width less than 'Y' is passing near boundary, with distance less than 'X/2' from PR Boundary, this type of problem occurs. Here individual layout doesn't give any DRC Errors. But when this type of cells placed near each other in PNR, it will gives DRC errors, because it requires distance between two metals larger than 'X' when their individual width is less than 'Y'. This problem can be solved by two ways. Modify these layouts in such a way. that each metal running parallel to the PR Boundary than its width is larger or equal to 'Y'. Modify these layouts in such a way that distance between this type of metals is always larger or equal to 'X'.

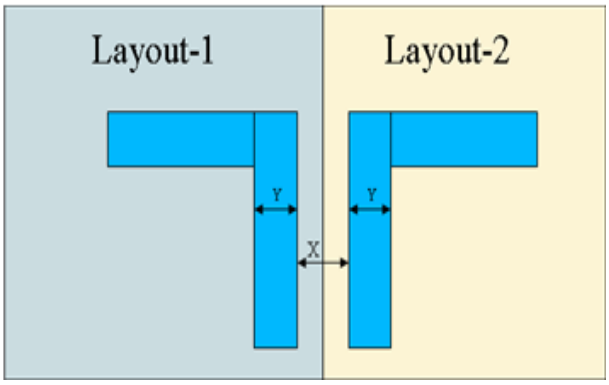


Figure 4.2: DRC Spacing Rule Violation

4.5.1 VIA Coverage Problem

If the via is not given minimum coverage then there will be problem for that. The via coverage rule is predefined and is fixed for opposite sides.

4.5.2 Access Point Problem

At the time of PNR it will connect two cells using metal layers using higher than metal-1. So if your pin is of metal-1 than first it will place via and then connect metal-1 to metal-2. And this metal-2 is used in other connection. Access points are available only on the grid and if the coverage is half of 'X' on the both side of the grid. Means the track should be on the grid. So if you are already using metal-2 in your cells and it is passing above metal-1 pin as shown in fig than it is not possible to connect that pin to any other cell at the time of This problem can be solved using two methods. Shift this metal two in such a way that it is not passing above any metal-1 contains pin. Change in layout in such a way that metal-1 pin shift its position where it is not lying below metal-2

4.5.3 Minimum Area Violation

Every metal patch should have a minimum required area that is necessary for the manufacture of the metal patch. The area should be at least as per the DRC.

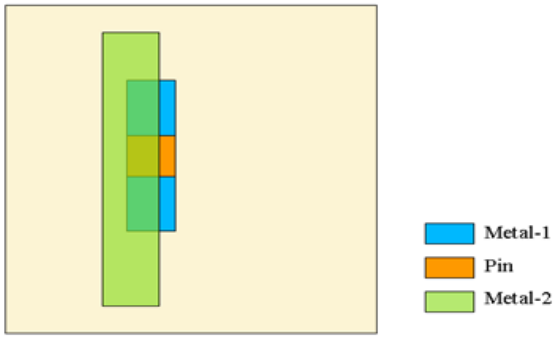


Figure 4.3: ACCESS Point Problem

4.5.4 Contact Coverage Violation

Minimum contact coverage should be given as per the DRC Rules.

4.5.5 Metal Width

It should be at least 'X'. If metal width is less than 'X' there will be a DRC error.

4.5.6 VIA to VIA Spacing

The via to via spacing if on the different nets should be much more than 'X' if the via are parallel if non parallel then the spacing required is less than the parallel case but more than the minimum spacing 'X'. But on the same net the minimum required spacing is 'X'.

4.6 LVS Problems

LVS (Layout Vs Schematic) is a tool that compares the connections in the schematic with the connection in the layout. If there is a mismatch between the connections it shows an error. Some of the common LVS Errors are discussed below

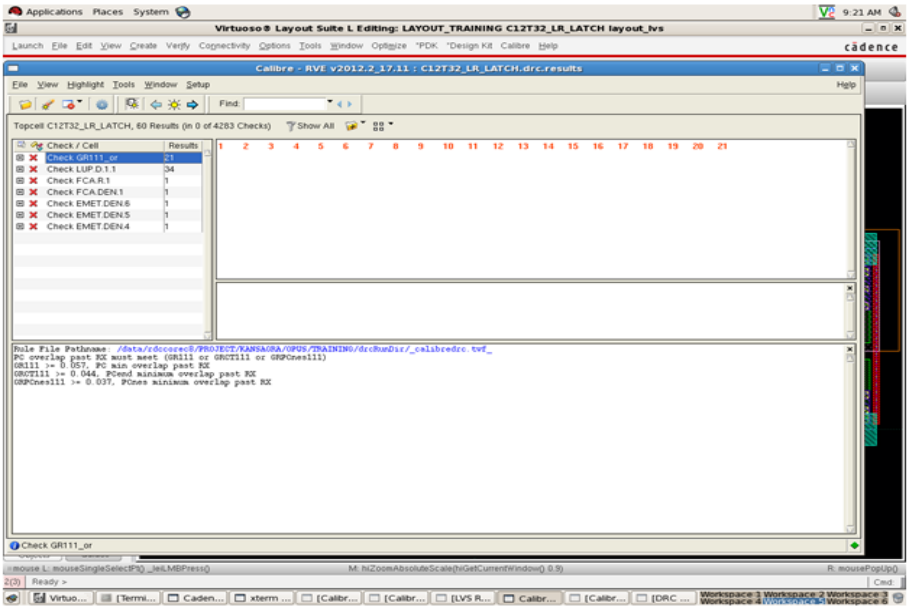


Figure 4.4: DRC Result Report

4.6.1 Property Errors

The property errors are related to the width of the transistors. If the width of a transistor is not same in the layout and the schematic then it will show a property error. This can be resolved by adjusting the width of the transistors in the schematic or layout.

4.6.2 Missing Instances

If some connection that is present in the schematic is missing in the layout or if any label pre-sent in the schematic is missing in the layout or the number of transistors are not equal in the layout and the schematic.

4.6.3 Incorrect Nets

This problem arises due to mismatch in connections between the schematic and in the layout.

4.6.4 Missing Ports

Problem arises if labels are missing in the layout that are present in the schematic or the labels are not put in the correct layer i.e. pin layer.

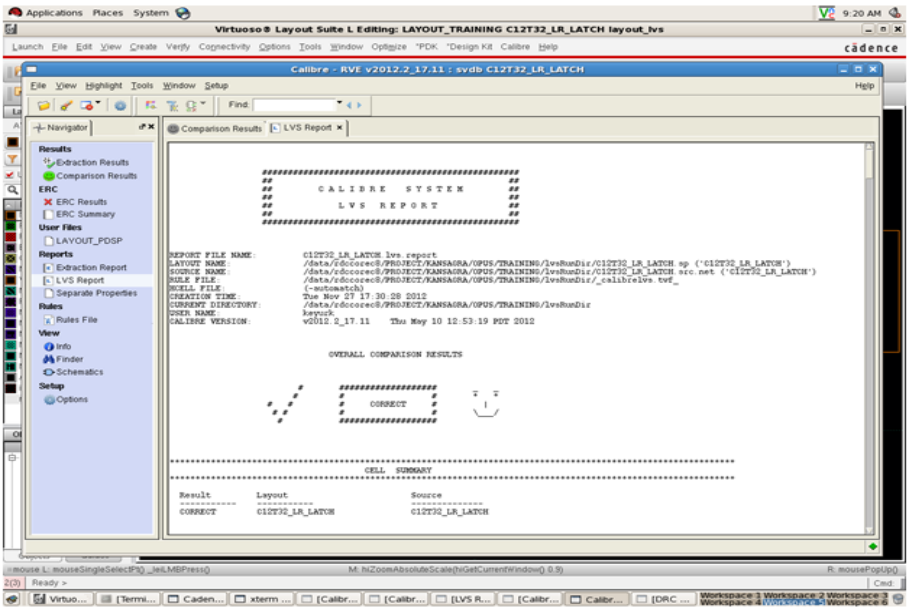


Figure 4.5: LVS Result Report

4.7 Packaging and Integrating Library

After extracting all the information the next step is to properly consolidate all the data and also provide various versions of the data as required. Packaging is the process of consolidating all the data into a proper organized format. A package consists of two types of data, Primary and secondary or derived data. Primary data consists of the main information regarding the library and cell designs. Derived data is translation of the primary data into various forms. In designing a chip many CAD tools are used and these tools come from various companies. Each tool requires data in a predetermined format. Packaging of library is done to provide different formats of the same data so that all the tools have their required data in corresponding

formats.

4.7.1 Generation

A package consists of the following information. Physical contains the actual contents of a library i.e. the gds, the cdl and the spi of the library.

Behaviour contains the verilog or VHDL view of the cells in the library.

Libs is the folder containing all the .lib of the library under various PVT conditions.

INTERFACE is a folder which contains the Interface.lib. This file contains information regarding all the pins present in each cell of the library.

CADENCE folder contains all the library information in cadence format. It contains two folders, CDSOA and LEF. CDSOA contains all the cells of the library and all the views attached to each cell. Hence CDSOA is a format of representing the library by Cadence. LEF contains the .lef file of the library in which all the metals and VIAS present in each cell are rep-resented in textual form.

LEF folder contains the same lef as in cadence folder but this lef has more information and is more processed. Packaging folder contains vc.bbview file. This file is a map file which maps all the data in the package. This file is used by tools to locate data in the package.

Docs folder contains all the documentation of the library.

4.7.2 Verification

A set of checks are run on the library and these checks are automated by Perl scripts which also have some code written in skill language. Skill is a language developed by cadence and it allows processing of the layouts and schematics drawn in virtuoso. The set of checks run on a library are

4.7.2.1 DRC AND LVS

Steps are the same as mentioned earlier. These steps are performed as a final confirmation that the entire library is aligned to the design rules and a correct logic is generated. The rest of the steps are as described. The graphic view of LEF is called abstract by Cadence or PR by Synopsys. Both essentially convey the same information in different formats. In an abstract only the metals and VIAS are shown. The geometries of all the layers below the metals are not shown. In LEF Checks the shapes of metals are checked so that no metal violates the minimum distances required from the edge of the cell. A Tech.lef file is provided as input to this check which specifies all the distance of various metals and VIAS from the boundaries of the cell in all possible directions and conditions. The rules form this Tech.lef are used to check the metal geometries in all the cells of the library to ensure proper location and geometries of the metals.

4.7.2.2 Functionality Verify

In this step the functioning and output voltages of the gate are verified under all operating conditions. For this step ELDO simulator is used. ELDO simulator is given a set of truth tables for all the cells in the library. The logic in this truth table is applied on the cells by ELDO simulator and output voltage is calculated. This output voltage is compared with the expected output voltages.

4.7.2.3 Abutment Checks

Abutment checks are performed on the library to ensure there are no errors when a cell is place in a chip. A primary layer containing all the layouts in usual orientation is placed. On top of this layer the same cells are placed but these cells are flipped in both X and Y axis. This procedure is repeated until every cell has every other cell place in this fashion.

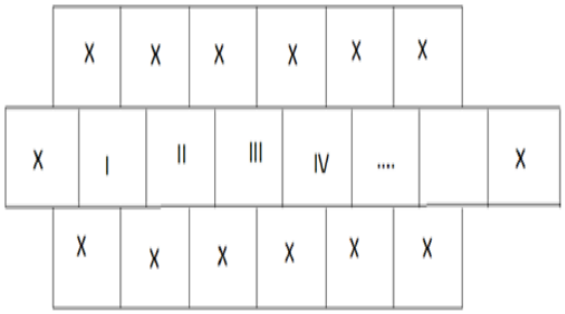


Figure 4.6: Abutment Checks

4.7.2.4 Parasitic Information

After the verification a spice based static parasitic extraction is performed on the library. Static capacitance and resistance values are extracted based on the geometries of various layers in the layout. A tool called Star RCXT is used to extract a static resistance and capacitance values. Star RCXT is a tool developed by Synopsys and it extracts resistance and capacitance from a fully routed design block. A .spi file is generated which contains resistance and capacitance information for every pin of a cell in the library. This file is used for dynamic parasitic extraction and accurate timing analysis.

Chapter 5

PMB CAD Data Generation

For PMB CAD data Generation - models, net list, simulation, and report generation.

Models file contains all information like capacitance, resistance, mosfet performance characteristics. For the different technology having different model files.

Process, Voltage , Temperature , parasitic we needed according to that model. The loop is to first develop LAYOUT, then Characterized and then SYNTHESIS, if these conditions not met then again start from LAYOUT.

For netlist extraction (device sensitivity), we need cdl, gds, cell name ,extraction method and type of extraction like nominal, Cmax, Cmin, RCmax , RCmin. From that we will get .spi files for all the cases. These files are used for simulation. RCTYP, RCMIN, RCMAX, CMAX, CMIN.

For simulation environment we need PVT values (process, voltage, and temperature), models, netlist. The ENV variable holds the current environmental variables. Environmental variables hold information about a shell's environment. Changing the value of an environmental variable from within a script will change that variable's value for the duration of the script and need to source ELDO and ALTO simulators.

These are the inputs for the environment, in PVT, we consider all corner cases, best case, worst case, and typical case and extraction type.

RCtype_bc_1.65V_m40C first is extraction type, then case (best case), voltage,

and then temp. For .spi the input file is CON file.

ABOUT ELDO

ELDO is a simulator which is the core component of comprehensive suits for analog and mixed signal simulation tools. To run ELDO simulations a .CIR control file must be supplied to the simulator, .CIR file must included the following-CIRCUIT CONNECTIVITY i.e. a NETLIST

MODELS parameter values defining the specific device models to be used ELECTRICAL STIMULI (sources) Simulation options and commands

After the simulation completed ELDO writes the simulator information to the .CHI file, this CHI file contains details of the simulation including warnings and errors messages, which may have been encountered during simulations. A binary .wdb file is also generated by default as an output of the simulation.

CDL Netlist

CDL (Circuit Design Language) netlist text file format (controlled by Cadence Design Systems) contains all of the data defining the primitive electrical devices, the electrical attributes of each primitive electrical device, the sub-circuit macros, the electrical attributes of each macro, the electrical connections for all of the primitive electrical devices and macros, and the attributes of each electrical connection including the connection point of each primitive electrical device.

GDS Netlist

GDS (Graphics Design System) netlist is the de facto industry standard for data exchange of IC layout artwork. It contains no connectivity, so after the library is read, it does not know about transistors and contacts: just layers. It is a binary format representing planar geometric shapes, text labels, and other information about the layout in hierarchical form. The data can be used to reconstruct all or part of the artwork to be used in sharing layouts, transferring artwork between different tools, or creating photo masks.

SPICE Netlist

SPICE (Simulation Program with Integrated Circuit Emphasis):An industry-

standard analog simulation language which contains models for most circuit elements and can handle complex nonlinear circuits .Also refers to a freely distributed simulation tool which simulates circuitry described in the SPICE language. SPICE netlist, extracted using the PLS (Post Layout Simulation) tools with CDL and GDS files as inputs, contains data defining all instances and sub circuits in the circuits, their electrical parameters, their interconnections and most importantly, the parasitic in the circuit.

Chapter 6

Process Monitoring IP description

- Test
  - Integrated JTAG IEEE1149.1 interface.
  - Controllable using on-chip jtag port.
  - Full-scan block except TAP controller which is non - scan by default.
- APB Bus Interface
  - Integrated APB Interface, with address and data bus size of 4 bytes.
- Parallel Interface
  - Integrated Parallel interface to directly access User Defined Registers.
- Sensors
  - Multiple micro sensor from following different possibilities
  - CPR SENSORS
- Distributed Architecture
  - Logic Wrapper (Local Controller) controls PMB sensors. Two kinds of Logic Wrappers to support sensors with 3 rings and those with 4 rings.

    - NONCPR pmb wrapper
    - CPR pmb wrapper
  - Master Controller interacts with the Logic Wrappers through synchronous serial data transfer.
  - Logic wrapper controls sensor and communicates with top controller synchronous or Asynchronous serial Data transfer.

- Three modes for each sensor are available:
  - Leakometer to monitor process leakage
  - Speedometer to monitor process speed
  - Speedometer to monitor process speed

Counters are replicated as registers. At the end of count operation first the counters content is loaded in to the corresponding register. these registers are then used for shifting data to the Main controller ring oscillator clock output from PMB logic wrapper is only available at PMB logic wrapper boundary.

For NON-CPR, there are 3 rings, and for CPR sensors there are 4 rings, these rings are optional outputs from the PMB logic wrappers. By default these outputs ports are not present.

Chapter 7

Process Controller Working

7.1 Mode Selection of PROMIP

The process monitoring cell is controlled through a JTAG interface or APB Interface or Parallel Interface. Table below describes about selecting appropriate interface or mode of PM CONTROL.

mode	Operation Mode
1	APB Interface is active. Operation on other two interfaces is not possible.
2	JTAG interface is active. Operation on other two interface not possible.
3	Parallel interface is active. Operation on other two interface not possible.

Figure 7.1: Modes of PM CONTROL

7.2 Working of PM CONTROL

- Define the time window during which the period of the oscillator will be measured. This time window is defined as a number of reference clock cycles.
- This number must be loaded in the REF COUNTER register. In APB mode

the reference time is with respect to APB clock and in other modes it is with respect to JTAG clock.

- PM CONTROL supports 3 sensor run modes.
- Parallel run, all sensors are selected and run in parallel. To run all rings of all sensors in parallel, all rings should be selected using sensor control register.
- Serial run, select a sensor, a ring of sensor. Run a sensor parallel, select a sensor and select all rings of sensor .To run the sensor set sensor run bit High in sensor control register to start the sensors and counters.
- Counters in wrappers start counting on the basis of sensor clocks until reference time elapses. Wrapper works on wrapper clock but counters counts on sensor clock. Hence the clock domain crossing involved in wrapper is handled using clock synchronization scheme.

7.2.1 Run Operation

8 bit data needs to be transferred to the Logic Wrapper which includes 4 bits for the ring selected, 2 bits for divide speed and 2 bits for divide leak.

Program the REFERENCE counter before sensor control register, reference counter defines the time window during which the period of the oscillator will be measured. This time window is defined as a number of reference clock cycles. The counted number should be loaded into the reference counter register. Two values of REFERENCE COUNTER length are supported, 16 and 32.

SENSOR CONTROL REGISTER is programmed for parallel run of all sensors or single sensor run. The values of SENSOR CONTROL REGISTER length are supported 16 bits. The 10th bit of sensor control register decides the valid run/read operations. For run operation it should be 0 and for read operation it should be 1.

After programming the ref counter and sensor control register wait for the SIGNAL to go to 0 for starting the run operation. That's called start of operation.

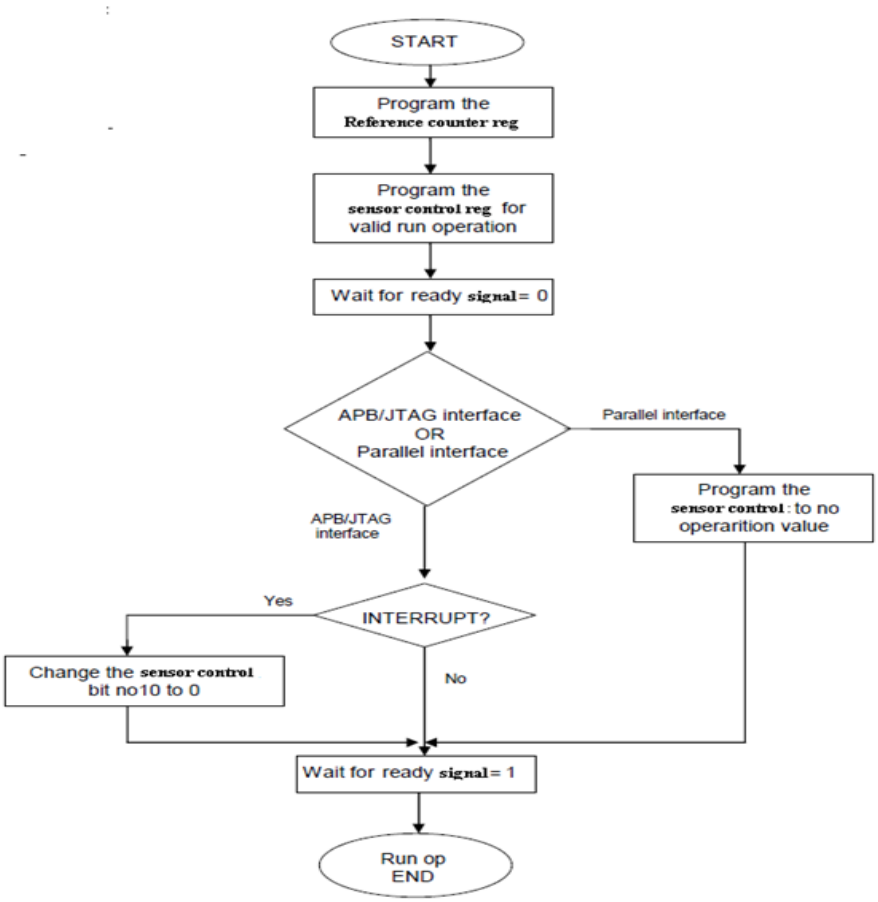


Figure 7.2: chart of PROMIP runs operation

Now for the MODE selection, that's also selected by sensor control register bit, for parallel, the data available on the input port is continuously latched on the sensor control register in every cycle when SIGNAL is 1.

After completion of operation, wait for SIGNAL to go 0 , that indicates the end of run operation. Now the sensor data is available on the counters.

7.2.2 Read Operation

4 bit data needs to be transferred to the Logic Wrapper corresponding to the ring selection the serial data to be transferred from the Logic Wrapper to the Master Controller includes as per the ring selected, the corresponding ring's counter register

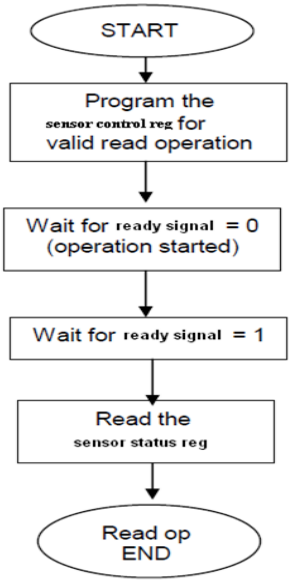


Figure 7.3: chart of PROMIP read operation

data is transferred to the Master Controller.

To start a valid read operation, first to program sensor control register, only single sensor ring data can be read at a time. After the sensor control register has been programmed, SIGNAL will go to 0 for read operation. The SIGNAL goes 1 to indicate end of read operation, and now the data is available in the sensor status output register. Read the sensor status register, for JTAG interface, select the sensor status register by loading the correct instruction code in IR of TAP and then shift the data out of the register. For APB interface, issue a read instruction, with address of sensor status register. And for PARALLEL interface, sensor status data is directly available on the output port.

Wait for reference time to elapse. PM CONTROL provides two coherent mechanisms to provide information to the user when the reference time has elapsed and sensor data is available in counters SIGNAL goes to 0 when the user gives instruction to run the sensors or read the sensor.SIGNAL goes to 1 when the reference time has elapsed and sensor data is available in counters.

Read Operation COUNTER READ is controlled by Read bit. This bit should

be ONE and Run bit should be zero for initiating COUNTER READ operation. Also there should be a change in SENSOR/RING select bits to initiate this operation. Select the valid sensor and ring.

7.2.3 On-Chip Process Monitoring

To allow on chip performance monitoring, a set of specific oscillators were designed to monitor individually the performances of NMOS and PMOS in terms of speed and leakage current. Each sensor is made of three specific oscillating structures called respectively **'Speedometer NMOS'**, **'Speedometer PMOS'** and **'Leakometer'**. The signals delivered by these structures are periodic square signals and it is the period of these signals that provides insights on the quality of the design in terms of speed and leakage. These monitors were developed and validated on different successive technology nodes for all available process options to address a large product portfolio needs. The validation of these sensors was done through a large silicon campaign characterization to prove their efficiency in tracking process skews including process corners deviations but also within wafer and within die variations.

7.3 REGISTERS

7.3.1 Sensor Control Register

Sensor control register is used to control the complete functionality of Process monitoring controller. Sensor control register is 16 bit wide.

7.3.2 Reference Counter Register

Define the time window during which the periods of the selected oscillator are counted. In some cases reference counter have any value between16 to 32 and in some cases it has any two values 16 or 32.

7.3.3 Sensor Status Register

This register contains the sensor data when read operation is performed by selecting the valid sensor and a ring. Sensor Status register size depends upon Counter size. For counters of length 16 bits, SENSOR Status register is 16 bits wide and for counter between 17(including) and 32 bits, SENSOR Status register is 32 bits wide.Total PMB is sum of all different type of sensors selected. Total PMB must not exceed 63.

7.4 Applications of PROMIP

- Static process compensation (post silicon tuning)
- Dynamic performance monitoring/compensation
- Voltage scaling
- Body biasing
- Change Frequency

Chapter 8

Specific Requirements

8.1 AMBA APB

The APB is part of the AMBA 3 protocol family. It provides a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. The APB interfaces to any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface. All signal transitions are only related to the rising edge of the clock to enable the integration of APB peripherals easily into any design flow. Every transfer takes at least two cycles.

- The write transfer starts with the address, write data, write signal and select signal all changing after the rising edge of the clock. The first clock cycle of the transfer is called the Setup phase.
- After the following clock edge the enable signal is asserted, penable, and this indicates that the Access phase is taking place. The address, data and control signals all remain valid throughout the Access phase.
- The transfer completes at the end of this cycle.
- The enable signal, penable, is deserted at the end of the transfer. The select signal, psel also goes LOW unless the transfer is to be followed immediately

Signal	Source	Description
pclk	Clock source Clock	Rising edge of pclk times all transfers on the APB.
presetn	Reset	The APB reset signal is active LOW.
paddr	APB Address INPUT	This is the APB address bus. It can be up to 32 bits wide and is driven by PROMIP user
psel	APB Select input	It indicates that the PROMIP register is selected and that a data transfer is required.
penable	APB Enable INPUT	This signal indicates the second and subsequent cycles of an APB transfer.
pwrite	APB Direction Input	This signal indicates an APB write access when HIGH and an APB read access when LOW.
pwdata	APB Write data INPUT	This bus is driven by user of PROMIP during write cycles when pwrite is HIGH. This bus can be up to 32 bits wide.
pready	PROMIP Ready O/P	In PROMIP pready is always assigned to HIGH.
prdata	PROMIP Read Data O/P	The PROMIP drives this bus during read cycles when pwrite is LOW. This bus can be up to 32-bits wide.
pslaverr	PROMIP error O/P	This signal indicates a transfer failure.

Figure 8.1: APB signal description Write transfer

by another transfer to the same peripheral.

8.1.1 Read Transfer

- The Read transfer starts with the address write signal and select signal all changing after the rising edge of the clock. The first clock cycle of the transfer is called the Setup phase.
- In Access phase the slave must provide the data before the end of the read transfer.
- The enable signal **penable** is deserted at the end of the transfer.

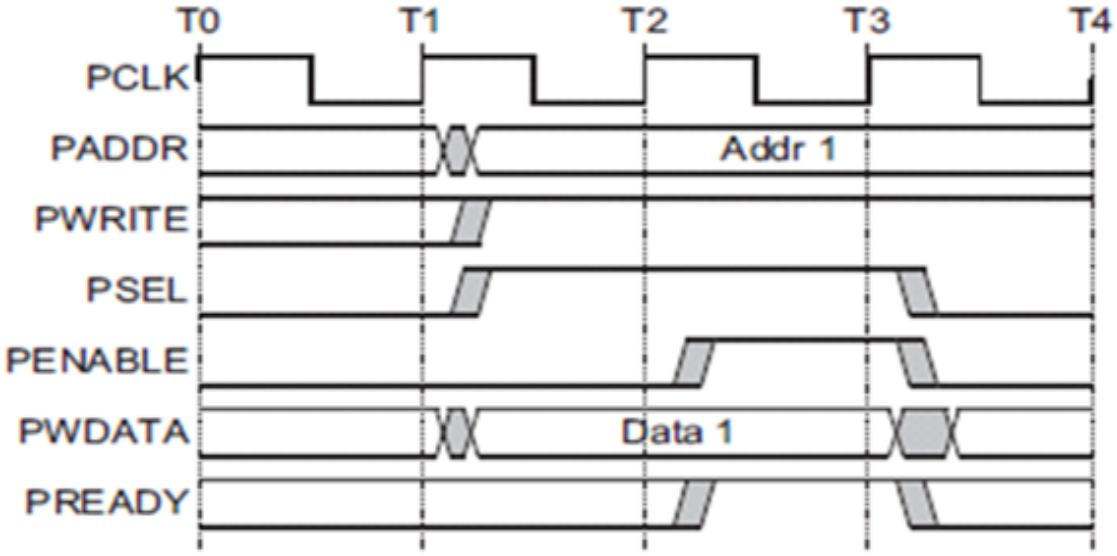


Figure 8.2: write transfer in APB mode

8.1.2 Error Response

Pslverr to indicate an error condition on an APB transfer errors condition can occur on both read and write transactions. PSLVERR is only considered valid during the last cycle of an APB transfer, when psel, penable, and pready are all HIGH. PSLVERR is driven LOW when it is not being sampled. That is, when any of psel, penable, or pready are LOW. In PROMIP PSLVERR goes high, when control and data register address are not correct, sensor status register is selected when dataready signal is low, if sensor control register to perform write operation (when dataready low and in middle of read operation) and If write operation is performed on sensor status register.

8.1.3 Operating States

The state machine operates through the following states: IDLE: This is the default state of the APB. SETUP: When a transfer is required the bus moves into the SETUP state, where the select signal, **psel**, is asserted. The bus only remains in

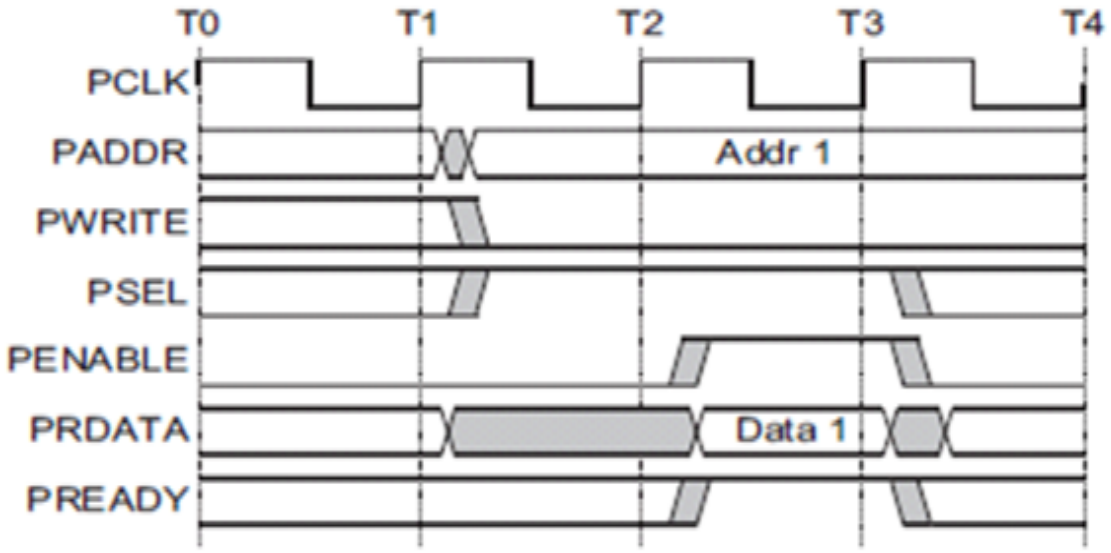


Figure 8.3: Read transfer in APB mode

the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock. ACCESS: The enable signal, **penable**, is asserted in the ACCESS state. The address, writes, select, and write data signals must remain stable during the transition from the SETUP to ACCESS state. Exit from the ACCESS state is controlled by the **pready** signal from the slave:

- If **pready** is held LOW by the slave then the peripheral bus remains in the ACCESS state.
- If **pready** is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows.

8.2 JTAG Interface: Test Access Port

The TAP is a general-purpose port that can provide access to many test support functions built into a component, including the test logic defined by this standard. It

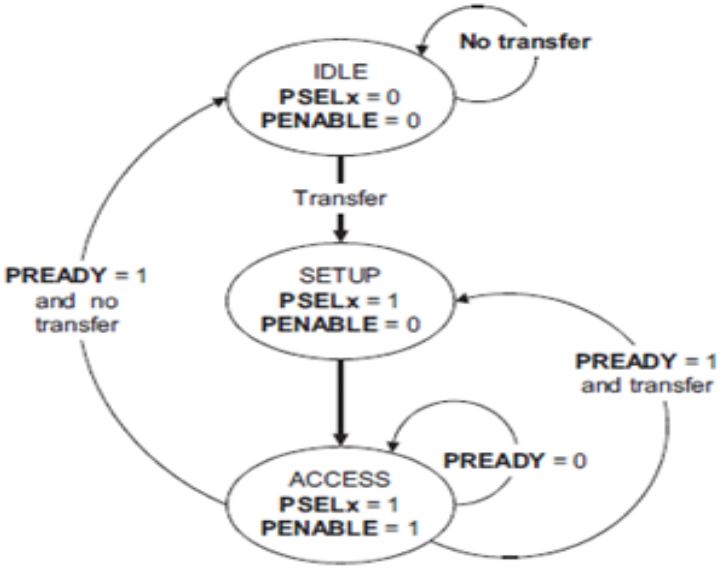


Figure 8.4: Operational activity of the APB

is composed as a minimum of the three input connections and one output connection required by the test logic defined by this standard.

Signal	Port	Description
tck	Input	Test clock input
tms	Input	Test mode select
tdi	Input	Test data input
tdo	Output	Test data output
tdo_en	Output	Test data output enable

Figure 8.5: JTAG Signal Description

All TAP inputs and outputs shall be dedicated connections to the component (i.e., the pins used shall not be used for any other purpose). Dedicated TAP connections are required to allow access to the full range of mandatory features of this standard.

Conclusion

- PROMIP introduce a simple and robust process compensation flow for high volume circuit production.
- By using this property we can save 20 - 30% of the total power consumption without impacting circuit functionality and operating frequency.
- PROMIP can be used for post-silicon tuning strategies and validation methods at both design and test steps.

Bibliography

[1] Sung-Mo Kang & Yusuf Leblebici "Cmos Digital Integrated Circuits Analysis and Design"

[2] ST Internal Documents

[3] AMBA 3 APB Protocol v1.0 by ARM Limited

[4] Igor Mohor by IEEE 1149.1 Test Access Port (JTAG)