Study And Analysis Of Failure Modes In SRAM Memory and Architecture For Self Correction

Project Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

in

Electronics & Communication Engineering

(VLSI Design)

By

Monika Kalura

(12MECV18)

Department of Electrical Engineering

Institute of Technology

Nirma University

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Under the Internal Guidance of

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Declaration

This is to certify that

1. The thesis comprises of my original work towards the degree of Master of Technology in VLSI Design at Nirma University and has not been submitted elsewhere for a degree.

2. Due acknowledgment has been made in the text to all other material used.

Monika Kalura

CERTIFICATE

This is to certify that the Major Project entitled **"Study And Analysis Of Failure Modes in SRAM Memory and Architecture For Self Correction"** submitted by **Ms. Monika Kalura (12MECV18)**, towards the partial fulfillment of the requirements for the degree of **Master of Technology in VLSI Design** of **Nirma University of Science and Technology, Ahmedabad** is the record of work carried out by her under our supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for the examination. The results embodied in this major project, to the best of our knowledge, haven't been submitted to any other university or institution for award of any degree or diploma.

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Monika Kalura

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Abstract

As the technology is shrinking down i.e voltage scaling for designs is becoming more and more complex, thereby necessitating the need for better and robust architectural designs capable of dynamically detecting and correcting failures.This thesis explores the analysis of failure modes in SRAM read and write circuitry and shows architectural changes done to detect and correct failures.In the project, changes have been made in the read circuitry by replacing single sense amplifier by a dual imbalanced sense amplifier. The changes have been validated on the silicon for a particular test chip using Ocelot Tester in R&D testing lab. The SMEM(Static Memories)Team is responsible for designing memories at different technology nodes and providing memory solutions to internal and external customers as per requirements.

ST Microelectronics At A Glance

- A world leader in providing the semiconductor solutions that help our customers improve quality of life for everyone, both today and in the future
- Among the world's largest semiconductor companies
- A leading Integrated Device Manufacturer serving all electronics segments
- A leading technology innovator (around 12,000 researchers approx. 21,500 patents)
- Key strengths in Multimedia Convergence, Power Applications and Sensors
- Rich, balanced portfolio (ASICs, Application-Specific Standard Products and Multi-Segment Products)
- A pioneer and visionary leader in sustainability
- President and CEO: Carlo Bozotti
- 2011 revenue $9.73 billion
- Approximately 50,000 employees including STEricssion at December 31, 2011
- Advanced research and development centers in 10 countries
- 12 main manufacturing sites
- Corporate Headquarters Geneva, Switzerland

- Global presence with sales offices all around the world
- Public since 1994 - shares traded on New York Stock Exchange (NYSE: STM), Euronext Paris, and Borsa Italiana
- Created as SGS-THOMSON Microelectronics in June 1987, from merger of SGS Microelettronica (Italy) and Thomson Semiconducteurs (France)
- Renamed ST Microelectronics in May 1998

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Chapter 1

INTRODUCTION

1.1 Description

The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integration technologies and large-scale systems design.

Complementary metal oxide semiconductor (CMOS) digital integrated circuits are the enabling technology for the modern information age. Because of their intrinsic features in low-power consumption, large noise margins, and ease of design, CMOS integrated circuits have been widely used to develop random access memory (RAM) chips, microprocessor chips, digital signal processor (DSP) chips, and application-specific integrated circuits (ASIC) chips. The popular use of CMOS circuits continues to grow with the increasing demands for low-power, low-noise integrated electronic systems.

For VLSI circuit design, however, it is important that the design be done in the context of global optimization with proper boundary conditions. In fact, the beauty of integrated circuits is that the final design goal is the concerted performance of all interconnected transistors, and not of individual transistors. No matter how well an individual transistor performs, if the technology fails to have equally good interconnects, the total performance can be very poor due to large parasitic capacitances and resistances; these translate into a large delay in the interconnection lines between transistors or logic gates.

The very important role of computer aided circuit simulation tools in VLSI design is well recognized. Computer simulation is, and will continue to be, an essential part of the design process, both for performance verification and for fine-tuning of circuits. However, the emphasis on simulation must be well-balanced with the emphasis on hands-on-design and analytical estimates, so that the significance of the later is not overwhelmed by the extensive use of computer-aided techniques.

In addition to the transistor-level circuit design issues, the accurate prediction and reduction of interconnect parasitic has become a very significant topic in high per-

formance digital integrated circuits, especially for deep sub-micron technologies.

Digital systems require the capability of storing and retrieving large amounts of information at high speeds. Memories are circuits or systems that store digital information in large quantity, hence are vital components in modern integrated circuits. Manufacturers of such products demand low-priced memories with low-power consumption, high-speed operation, high density, and small package size.

The semiconductor markets have embraced the fact that the architecture of the memory structure has a considerable impact on the performance of the system. Over the years, technology advances have been driven by memory designs of higher and higher density.

While designing System-on-Chip (SOC), system architects need to resolve a number of complex issues in high-performance system applications. However, one of the fundamental problems in these applications is Memories - the bottlenecks and challenges of system performance often reside in its memory architecture.

As advances in memories come to life, system designers are faced with the challenge of selecting the proper memory for their application.

Memory developers have to design memories to address the issues in bandwidth, latency, density, power and cost. Unfortunately, it is not possible for a single memory technology to address all these issues with distinct advantages - this translates to an arsenal of components available for designers to architect their system.

This initiates investigation of specific architecture in technology for Low Power and High Speed. In this project, we will look at the most common memory cell that is used today, a 6Ts SRAM cell, and then look at the other components needed to build complete memory system. We will also look at other types of memories & then do the comparative study & analysis based on various design parameters.

1.2 Data Storage Devices: An Overview

From the beginning of the electronics industry, storage of data has been a major point of consideration. Many storage devices have been developed by now, with various working principles and data storage techniques.

In general, the data storage devices can be classified by a wide variety of aspects, but most frequently they are divided by technology into the semiconductor types and the moving media types which require mechanical equipment for operation.

The five basic semiconductor types are bipolar, N-channel and P-channel MOS, complementary MOS and charge coupled devices (CCD). The moving media types include magnetic disk, optical disk and holographic storage. While magnetic bubbles are not mechanical, they require equipment for supplying a magnetic field for operation and are thus considered with the mechanical types. Since the semiconductor memories are decreasing in cost per bit faster than the other types of data storage, various attempts to configure them for the disk application are occurring.

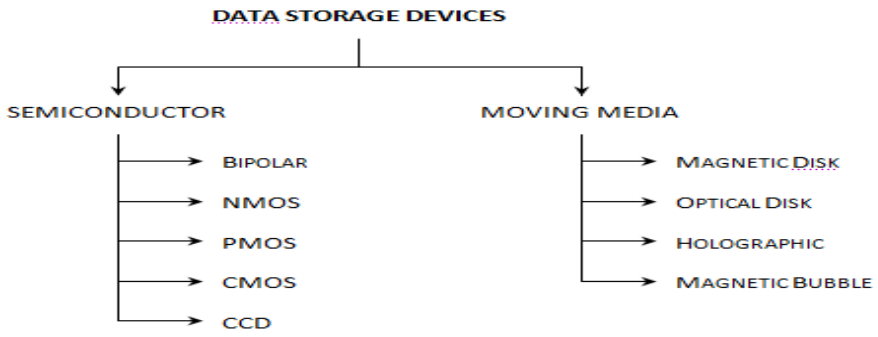

Figure 1.1: Basic classification of Data Storage Devices

MOS MEMORIES: INTRODUCTION

The ideal memory would be low cost, high performance, high density, with low power dissipation, random access, non-volatile, easy to test, highly reliable, and standardized throughout the industry.

Those memory technologies which did not offer these advantages to some extent

were one by one successfully challenged by the MOS memories. Unfortunately a single memory having all these characteristics has not yet been developed, although each of the characteristics is held by one or another of the MOS memories. Thus, MOS memories have dominated the world of memories.

The MOS memories fall into two broad categories:

- Read-Write memories: Dynamic RAMs and Static RAMs, allow the user both to read information from the memory and to write new information into memory while it is still in the system.
- Read Only Memories: ROMs, EPROMs, EEPROMs, are used primarily to store data; however, the EEPROMs can also be written into a limited number of times while in the system. Read-Only memories are non-volatile, that is, they retain their memory if the power is turned off.

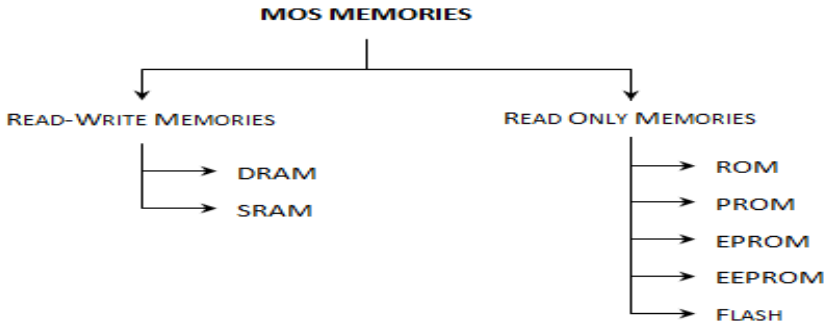

Figure 1.2: Major classes of MOS memories

Read-Write Memories Read-write random-access memories (RAM) may store information in flip-flop style circuits or simply as charge on capacitors. Because read-write memories store data in active circuits, they are volatile; that is, stored information is lost if the power supply is interrupted. The natural abbreviation for read-write memory would be RWM. However, pronunciation of this acronym is difficult. Instead, the term RAM is commonly used to refer to read-write random-access memories.

The two most common types of RAMs are the static RAM (SRAM) and the dynamic RAM (DRAM). Static RAMs hold the stored value in flip-flop circuits as long as the power is on. SRAMs tend to be high-speed memories with clock cycles in the range of 5 to 50 ns. Dynamic RAMs store values on capacitors. They are prone to noise and leakage problems, and are slower than SRAMs, clocking at 50 ns to 200 ns. However, DRAMs are much denser than SRAMs, up to four times denser in a given generation of technology.

1.3 Memory Organisation

The preferred organization for most large memories is the random-access architecture. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing.

The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called wordlines, while the vertical lines, along which data flow into and out of cells, are called bitlines.

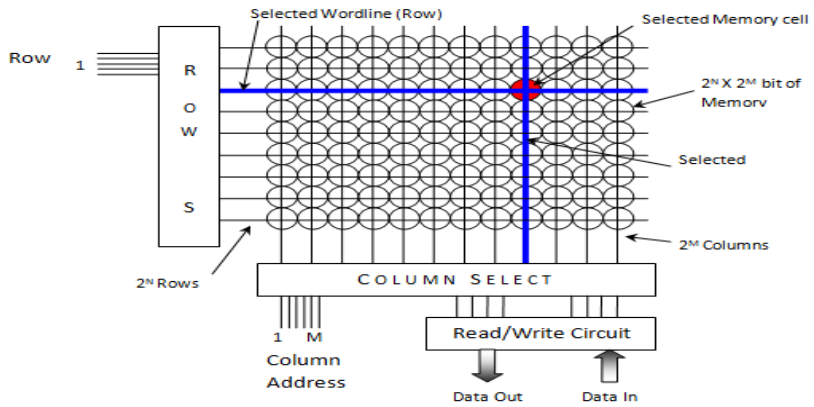

Figure 1.3: Typical Memory Organization

A cell is accessed for reading or writing by selecting its row and column. Each cell can store 0 or 1. Memories may simultaneously select 4, 8, 16, 32, or 64 columns in one row depending on the application. The row and column (or columns) to be selected are determined by decoding binary address information.
Memory exists as stand-alone component, but also as embedded blocks in system-on-chip.

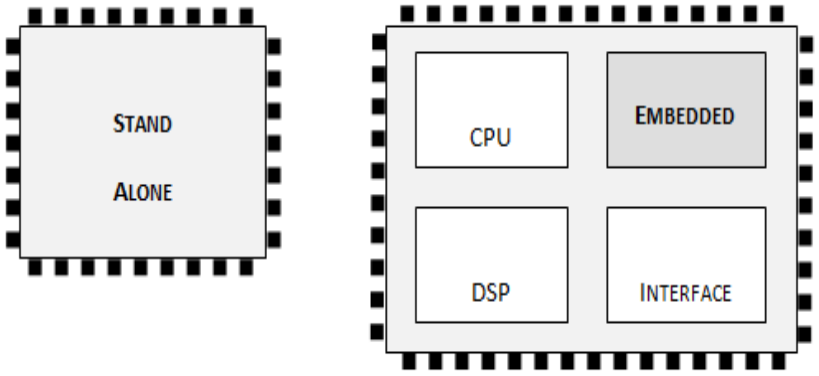

Figure 1.4: Memory existence as a stand-alone component and an embedded block

Memory cell circuits can be implemented in a wide variety of ways. In principle, the cells can be based on the flip-flop designs since their intended function is to store bits of data. However, these flip-flops require a substantial amount of area and are not appropriate when millions of cells are needed. In fact, most memory cell circuits are greatly simplified compared to register and flip-flop circuits. While the data storage function is preserved, other properties including quantization of amplitudes, regeneration of logic levels, input-output isolation, and fan out drive capability may be sacrificed for cell simplicity. In this way, the number of devices in a single cell can be reduced to one to six transistors.
At the level of a memory, the desired logic properties are recovered through use of properly designed peripheral circuits. Circuits in this category are the decoders, sense amplifiers, column precharge, data buffers, etc. These circuits are designed so

that they may be shared among many memory cells. Read-write (R/W) circuits determine whether data are being retrieved or stored, and they perform any necessary amplification, buffering, and translation of voltage levels.

1.4 Functional SRAM Chip Model

Memories are said to be static if no periodic clock signals are required to retain stored data indefinitely. Memory cells in these circuits have a direct path to VDD or Gnd or both. Read-write memory cell arrays based on flip-flop circuits are commonly referred to as Static RAMs or SRAMs.
A functional block diagram for the SRAM chip is shown below

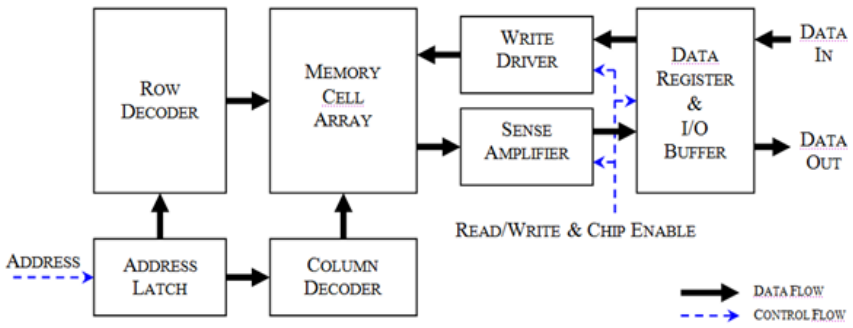

Figure 1.5: Functional SRAM chip model

- The address latch block, receives the address.
- The higher order bits of the address are connected to the row decoder, which selects a row in the memory cell array.
- The lower order address bits go to the column decoder, which selects the required columns. The number of column selected depends on the data width

of the chip that is the number of data lines of chip, which determines how many bits can be accessed during a read or write operation.

- When the read/write line indicates read operation, the contents of the selected cells in the memory cell array are amplified by the sense amplifiers, loaded in the data register & presented on the data-out line(s).
- During a write operation the data on the data-in line(s) are loaded into the data register & written in to the memory cell array through the write driver. Usually the data-in & data-out lines are combined to form bidirectional data lines, thus reducing the number of pins on the chip. The chip-select line enables the data register, together with read/write line, the write driver.

STATIC RAM CELL The basic static RAM cell is consists of two cross-coupled inverters and two access transistors. The access transistors are connected to the wordline at their respective gate terminals, and the bitlines at their source/drain terminals.

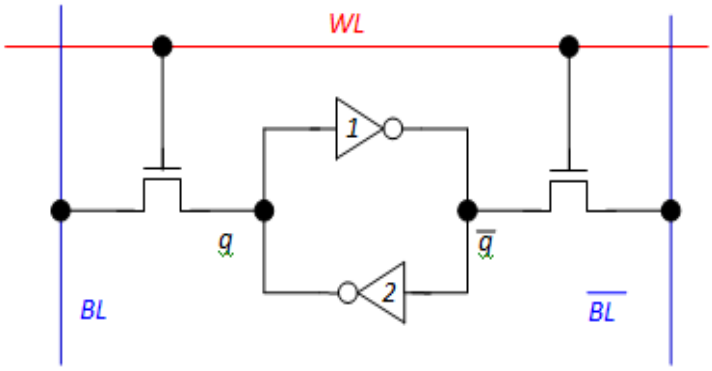

Figure 1.6: Basic SRAM cell

The wordline is used to select the cell while the bitlines are used to perform read or write operations on the cell.Internally, the cell holds the stored value on one side and its complement on the other side. For reference purposes, assume that node q

holds the stored value while node q holds its complement.The two complementary bitlines are used to improve speed and noise rejection properties.

6T SRAM Cell The six transistor (6T) static memory cell in CMOS technology is used in majority of the designs, today. The cross-coupled inverters, M1, M5 and M2, M6, act as the storage element. Major design effort is directed at minimizing the cell area and power consumption so that millions of cells can be placed on a chip.

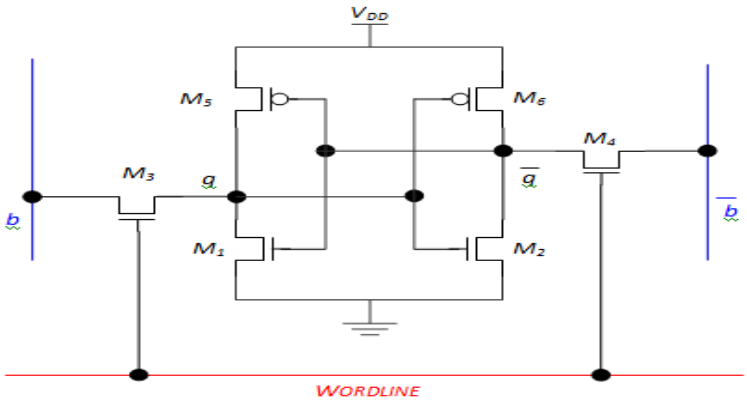

Figure 1.7: 6T SRAM cell

The steady-state power consumption of the cell is controlled by sub-threshold leakage currents, so a larger threshold voltage is often used in memory circuits. To reduce area, the cell layout is highly optimized to eliminate all wasted area.

Read Operation For a 0 is stored on the left side of the cell, and a 1 on the right side in the 6T RAM cell, M1 is on and M2 is off. Initially, b and b are precharged to a high voltage around VDD by a pair of column pull-up transistors. The row selection line, held low in the standby state, is raised to VDD which turns on access transistors M3 and M4. Current begins to flow through M3 and M1 to ground. The resulting cell current slowly discharges the capacitance Cbit. Meanwhile, on the other side of the cell, the voltage on b remains high since there is no path to ground through M2.The difference between b and b is fed to a sense amplifier to

generate a valid low output, which is then stored in a data buffer.

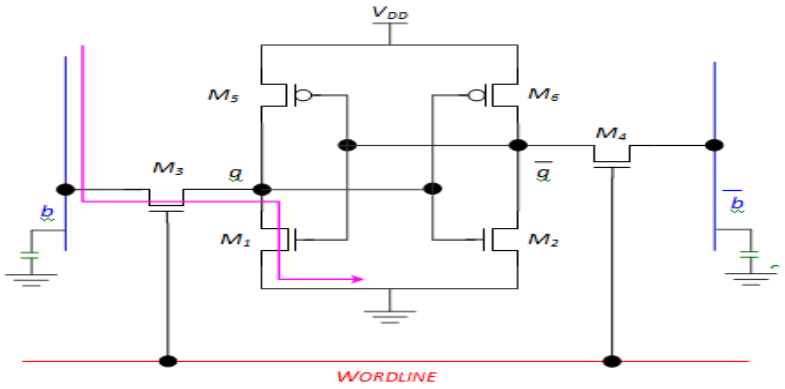

Figure 1.8: Read Operation in SRAM cell

Upon completion of the read cycle, the wordline is returned to zero and the column lines can be precharged back to a high value.
When designing the transistor sizes for read stability, it is ensured that the stored values are not disturbed during the read cycle. The problem is that, as current flows through M3 and M1, it raises the output voltage at node q which could turn on M2 and bring down the voltage at node q. The voltage at node q may drop a little but it should not fall below VS. To avoid altering the state of the cell when reading, the voltage at node q is controlled by sizing M1 and M3 appropriately. This is accomplished by making the conductance of M1 about 3 to 4 times that of M3 so that the drain voltage of M1 does not rise above VTN. In theory, the voltage should not exceed VS, but this design must be carried out with due consideration of process variations and noise. In effect, the read stability requirement establishes the ratio between the two devices.

Write Operation The operation of writing 0 or 1 is accomplished by forcing one bitline, either b or b, low while the other bitline remains at about VDD. For SRAM cell taken above, to write 1, b is forced low, and to write 0, b is forced low.

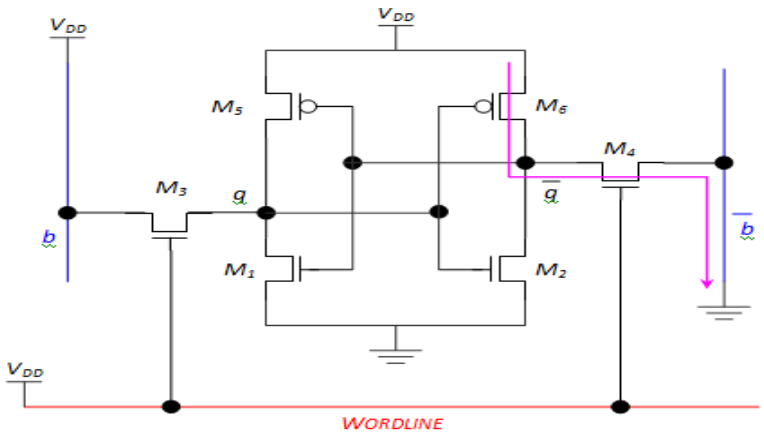

Figure 1.9: Write Operation in SRAM cell for writing 1

The cell must be designed such that the conductance of M4 is several times larger than M6 so that the drain of M2 is pulled below VS. This initiates a regenerative effect between the two inverters. Eventually, M1 turns off and its drain voltage rises to VDD due to the pull-up action of M5 and M3. At the same time, M2 turns on and assists M4 in pulling output q to its intended low value. When the cell finally flips to the new state, the row line can be returned to its low standby level.

The design of the SRAM cell for a proper write operation involves the transistor pair M6-M4. When the cell is first turned on for the write operation, they form a pseudo-NMOS inverter. Current flows through the two devices and lowers the voltage at node q from its starting value of VDD. The design of device sizes is based on pulling node q below VS to force the cell to switch via the regenerative action.

Timing Diagram of Read Operation

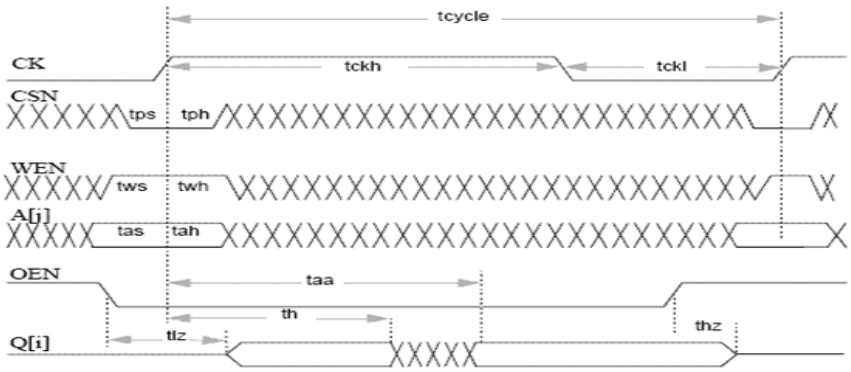

Figure 1.10: Read cycle diagram for SRAM

- tph - CSN setup time
- tas Addresss setup time
- tah - Addresss hold time
- tws WEN setup time
- twh WEN hold time
- tckh- ck high pulse width
- tckl- ck low pulse width
- taa access time
- th data valid after ck
- tps CSN setup time
- th data valid after clk
- taaw write through access time
- tds data setup time
- tdh data hold time

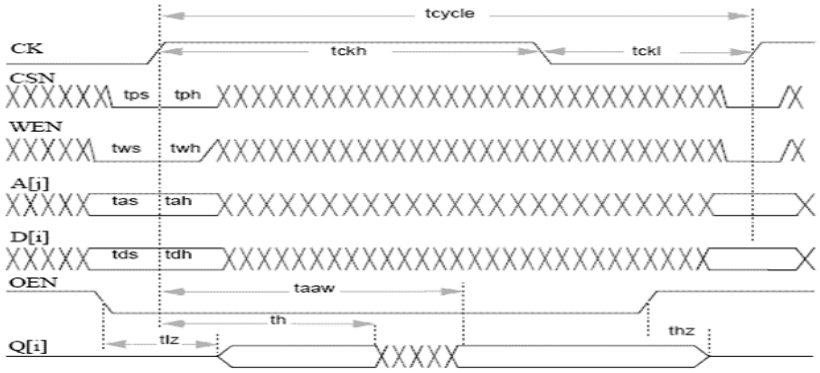

Figure 1.11: Write Cycle diagram for SRAM

1.5 Access Time

The Access Time is determined by the critical path from the Address input to the Data output as shown in fig.

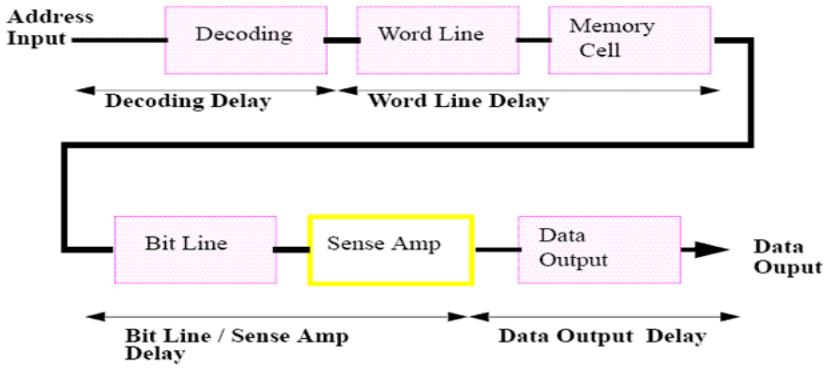

Figure 1.12: ACCESS TIME

It is the sum of following delays :

Decoder Delay, Word-Line Delay, Sensing Delay and Data Output Delay.

Chapter 2

ANALYSIS OF DYNAMIC FAULTS IN SRAM

Analysis of Dynamic Faults in SRAM Functional faults traditionally employed in RAM testing, such as stuck-at, transition faults and coupling faults are nowadays insufficient to give correct models of the effects produced by some defects in VDSM technologies.
The occurrence of resistive open defects has considerably increased in recent technologies due to presence of many interconnect layers, and an ever-growing number of connections between each layer.

Due to internal self timed architecture, two types of timing dependent faults can be identified:

1. Faults whose effect appears after more than one operation. The detection of these faults depends on clock speed.

2. Faults affecting memories external timings. These faults originate from defects in the non-self timed parts of the memory periphery, thus they depend on input signal timings

The simulations have been performed in different PVTs.

2.1 Types Of Fault Models

1. **TF (Transition Fault):** When core cell fails to undergo transition (0->1 0r 1 ->0) when it is written.

2. **RDF (Read Destructible Fault):** If the read operation performed on the core cell changes the data in the core cell and writes incorrect value on the output.

3. **IRF (Incorrect Read Fault):** Read operation performed on core cell returns incorrect logic value and correct value is still stored in the core cell.

4. **DRF (Data Retention Fault):** When memory core cell loses its previously stored logic value after a certain period of time during which it has not been accessed.

5. **DRDF (Deceptive Read Destructible Fault):** If a read operation performed on the core cell returns the correct logic value but it changes the content of the core cell.

2.2 Types Of Defects:

Following are the defects mentioned as shown in fig.10

- **Defect Df1:** Produces a delay in the charging / discharging operation of node SB. Leads to transition fault.
- **Defect Df2:** Produces delay in the output of the INV1. May lead to Read Destructible Fault (RDF).
- **Defect Df3:** Similar to Df2 and leads to Deceptive Read Destructible Fault (DRDF).
- **Defect Df4:** Placed in pull up of INV1 and leads to static and dynamic faults. May lead to DRF.
- **Defect Df5:** Resistive effect of long connection wires e.g. Wordline. It implies incorrect read fault (IRF) and TFs.
- **Defect Df6:** Fault at the input of INV2. Leads to TF in write operation.

2.3 Core Cell Simulations

Several resistive open defects have been analyzed in the memory core cell. Figure 1 depicts the scheme of a standard 6T cell with six different resistive open defects.

The criterion for the choice of defect location is layout dependent. The defects have been injected in correspondence with the interconnections where there is higher probability of their presence.

The whole operating environment range has been selected in order to maximize the fault detection probability.

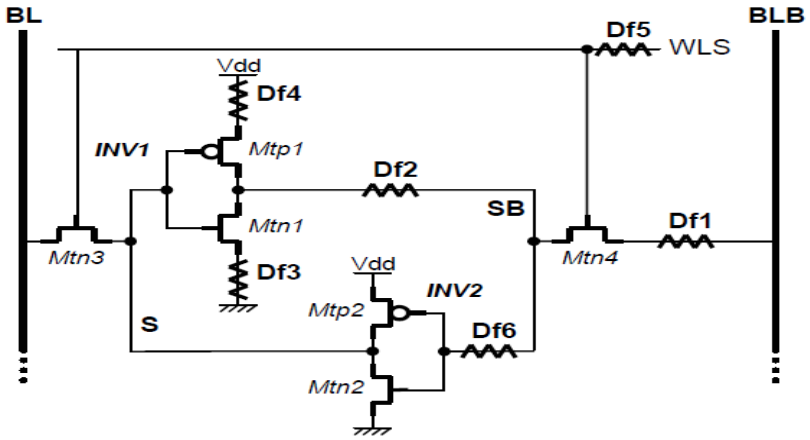

Figure 2.1: Resistive open defects in memory core cell

DEFECTS IN CELL PULL DOWN

A resistive defect in the cell pull down path of one of the core cell inverters is (Df3 in figure 1) may cause a destructive read operation. The read value can be wrong or correct, thus a second read access is necessary to detect the fault (deceptive destructible read).The impact on the defect on memory robustness has been taken into account since the fault detection is more or less reliable depending on the voltage difference between BL and BLB.

DEFECTS IN CELL PULL UP

A resistive defect in the cell pull up path of one of the core cell inverters (Df4 in figure 1), is a classic hard to detect fault. When a defect is on Mtp2 source, a dynamic read destructible fault occurs when a 0 is stored in the cell. A 0 stored corresponds to a0 on the node Sand a 1 (VDD) on node SB.

The first step of the read operation is the precharge at VDD of BL and BLB. Then

the cell connected to bitlines, the Wordline signal actives transistors Mtn3 and Mtn4, which are switched on. BLB and node SB are at same potential, while BL and node S are at different potential. As BL has high capacitance, its discharge is long. So, we can consider that BL and BLB values remain at VDD at the beginning of read operation. Moreover, the current in Mtn3 is high due to difference between BL and S. The S node is thus charged a little (0 + V). As the value at the inverter input has slightly increased, the value at its output node SB decreases because Mtp2 cannot compensate this leak of charge due to resistive defect. Consequently, SB voltage decreases a little (VDD- V) causing the degradation of logic 0 on S. If SB value becomes close to VDD/2, there is swap of value stored in the cell. In normal condition, when there is no resistive defect in the pull up path, the current in the Mtp2 transistor is sufficient to maintain the SB node close to VDD.

2.4 Address Decoder Simulations

When a resistive open defect appears between gates (inter-gate defects) it produces faults that can be detected by standard March tests. When the defect is located inside the gate (intra-gate defects) and in particular in the parallel plan of transistors, it produces dynamic fault due to its sequential behavior. Referring to NOR gate of figure 2, such a defect has been located in the drain of the transistor TN1 and it may produce a delay during pull-down of node ZA0. This fault is the dynamic one because it needs a specific sequence of operations (read and write) with a specific address sequence. When resistive open defects occur in between gates (inter gate

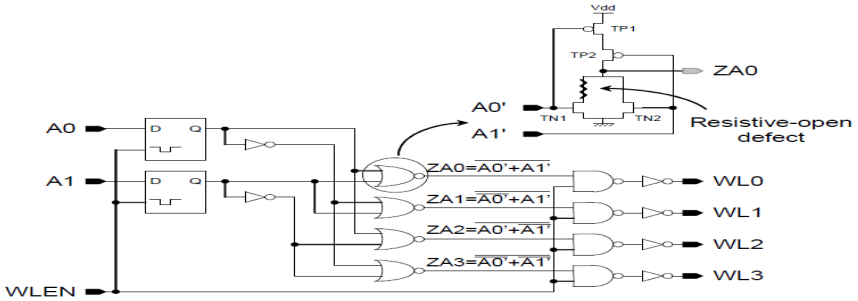

Figure 2.2: Intra gate resistive-open in pull-down path of NOR-based address predecoder

defects), it produces faults that can be detected by tests. When defect is located inside the gate (intra gate defects), it produces dynamic fault due to sequential behavior. During first cycle, WL0 is addressed and corresponding output of NOR-gate ZA0 1. During 2nd cycle, WL1 is accessed (ZA1 =1), but due to presence of defect ZA0 remains 1. Both WL0 and WL1 are selected. The 1 that is written in the cell by WL1, overwrites the 0 that was previously stocked by WL0. Hence final access at WL0 will be a read 1 instead of expected 0. The detection of resistive opens depends upon resistance value and access speed. Presence of resistive open is equivalent to degradation of address setup time for particular address sequence.

Chapter 3

CORRECTION TECHNIQUES

3.1 Sense Amplifier

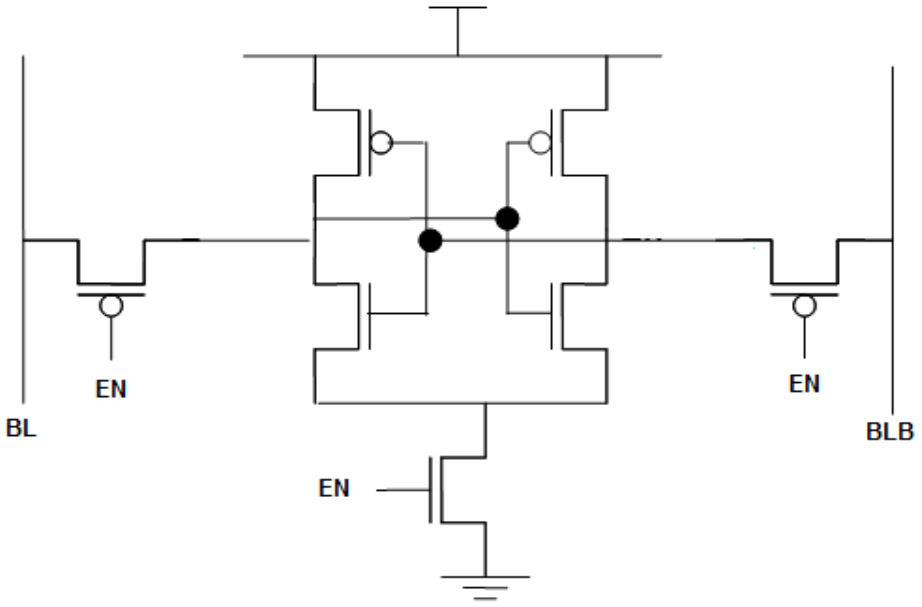

Figure 3.1: Latch type sense amplifier

- To read a bit from a particular memory cell, the wordline along the cell's row is turned on, activating all the cells in the row.
- The stored value (Logic 0 or 1) from the cell then comes to the Bit-lines associated with it.
- The sense amplifier at the end of the two complimentary bit-lines amplifies the small voltages to a normal logic level.
- The bit from the desired cell is then latched from the cell's sense amplifier into a buffer, and put on the output bus.

Sense amplifier basically has three states of operations:

1. **Precharge state:** Sense Enable signal is 0. Internal nodes of sense amplifier are precharged to VDD.
2. **Sensing state:** Sense Enable signal is low. Precharge of internal nodes is stopped. Sense amplifier is sensing voltage status of BIT lines.
3. **Resolving state:** Sense Enable signal is high. Internal nodes are cutoff from BIT lines. And sense amplifier resolves BIT line voltage into logic 0 or 1. This logic is reflected in internal nodes.

Drawbacks:

- Cant detect whether enough Vdiff is generated or not.
- Cant recover the wrong detection.

3.2 Dual Imbalanced Sense Amplifier

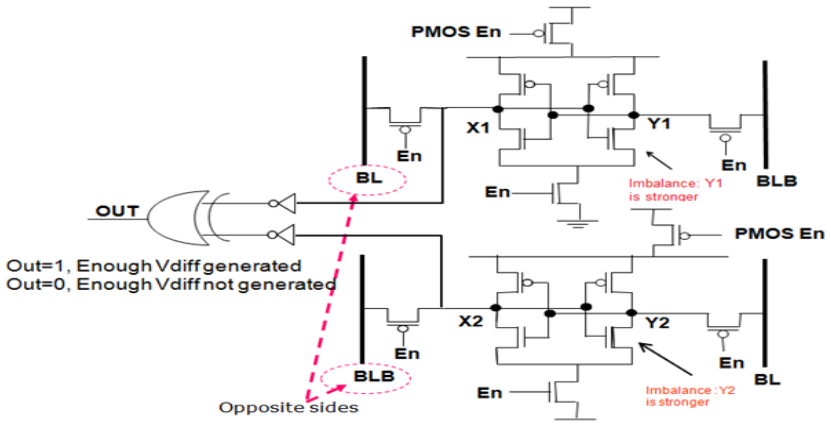

Figure 3.2: Dual Imbalanced Sense Amplifier

- Initially, for read operation, BL and BLB are precharged to VDD.
- And internal nodes of the sense amplifier are initialized with VDD.

For read 1 operation:

1. Sense amplifier 1, BLB begins to fall and imbalance is supporting it.
2. Sense amplifier 2, BLB begins to fall making nodes X2=0 and Y2=1, but as imbalance is in Y2 side it will make Y2=0, if enough Vdiff is not created by falling BLB.

For read 0 operations:

1. Sense amplifier 2, BL begins to fall and imbalance is supporting it.
2. Sense amplifier 1, BL begins to fall making nodes X1=0 and Y1=1, but as imbalance is in Y1 side it will make Y1=0, if enough Vdiff is not created by falling BLB.

For correct operation output will come as '1', and in case of failure output is '0'.
Three states of internal nodes are possible:

- 11: Enough Vdiff has not been formed.
- 10: Enough Vdiff has been formed and **BITLINE** has fallen.
- 01: Enough Vdiff has been formed and **BITLINEBAR** has fallen.

Chapter 4

OCELOT TESTER

4.1 Specifications

- A personal Ocelot can be configured with 64,128,256 general purpose data pins
- 500 MHz data rates.
- 400MHz high performance clock channels
  - Dynamic waveform switching for AC scan applications
  - Free running mode for BIST applications.
- Advanced Pattern Memory architecture
  - Up to 64 Mv pattern memory per pin
  - Dynamic Data Matrix
    - Flexible memory remapping
    - Extends scan depths up to 4GV
- Up to 32M of capture memory per pin
  - Full tester rate data capture
  - Fail capture or data record modes
- PMU(Parametric Measurement Unit) per 64 pins, switchable to any pin
- Frequency measure up to 200MHz
- Standard DPS: Four 2.5A, 0 to 6V channels
- Optional Power Resource Group adds:
  - One 5A and three 2.5A channels
  - Current measure and programmable current limits
  - Eight 0.2A, 0 to 16V channels.

- Uses external PC running Windows XP
  - USB tester interface
- STYLYS tester operating system
  - Based on STIL (IEEE 1450)
  - Comprehensive suite of interactive analysis and debug tools.

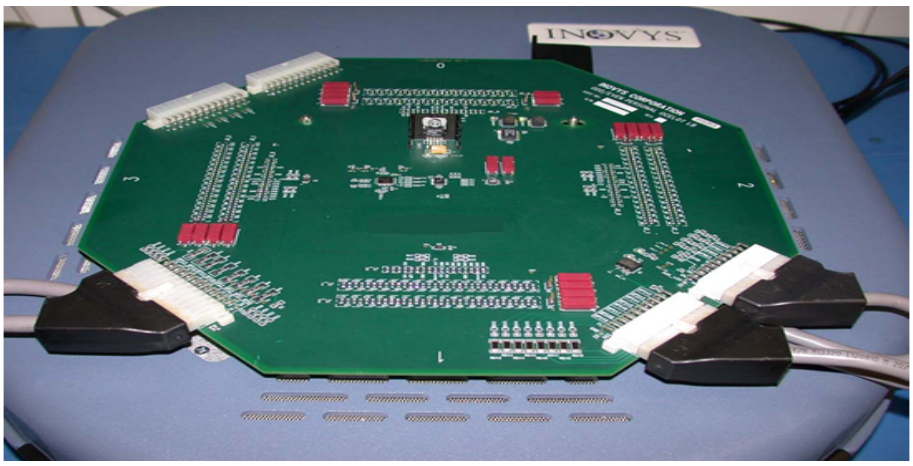

Figure 4.1: Ocelot Tester

4.2 Key Benefits

- Reduce design debug from weeks to hours.
- Optimize failure analysis process.
- Slice weeks from test program development.
- Characterize speed performance down to design element level.
- Improve engineering productivity.

Reduce Design Debug from Weeks to Hours:

The challenges in successfully debugging new semiconductor designs are compounding, and include: increasing gate count and density, new technology nodes, decreasing external access, and increasing defect and fault mechanisms. The best response to address these challenges is implementation of Design for Test (DFT) and leveraging structural test methodologies. Employing the Personal Ocelot structural test capability can track failures back to individual flip-flops in the design. This is achieved through seamless bidirectional links between ATE and EDA including the latest tools from Cadence, Mentor Graphics and Synopsys using the IEEE1450 Standard Test Interface Language (STIL) in native format. This unique combination of structural and functional test capability reduces the typical design debug and validation effort from weeks to hours.

Optimize Failure Analysis Process:

Failure analysis of manufacturing failures or customer field returns can be a difficult and resource intensive task. Now, the time consuming scheduling and setup time of high-cost production ATE is replaced with the compact, low cost Personal Ocelot, located on the engineers desk, and always ready to use. Traditional functional test datalogs failures from outside the device, while structural test data logs failures from inside the device. The personal Ocelot can perform both and significantly increases the ability to observe and diagnose the failure. Combining this with the Inovys real-time feedback loop to EDA ATPG diagnosis tools, linked to EDA layout tools, enables precise localization of process and design failures down to the gate level. This results in a significant reduction in failure analysis time and cost.

Slice Weeks from Test Program Development:

Test programs are quickly generated directly using the output of the EDA ATPG tools in native STIL eliminating the time consuming and error prone translation process required by other ATE proprietary test languages. In addition, the personal Ocelot features a comprehensive, industry-leading suite of interactive

debug tools. Test vectors and programs can be quickly developed and debugged on the Personal Ocelot, including powerful tools for Scan test debug. These activities can all be performed more efficiently and effectively at the engineers desk and removes the need to take an expensive production tester offline. Typical test program generation and debug effort is reduced from more than four weeks to a few days.

Characterize Speed Performance Down to Design Element Level:

The Personal Ocelot is a valuable tool for characterizing the speed performance of a new design. Traditional at-speed functional testing only provides the speed characteristics of the design as a whole. Using AC Scan with the Personal Ocelots AC Performance Package can provide a designs speed performance down to the individual building blocks. The High Performance Clock Channels (HPCC) in the Personal Ocelot enables AC performance testing up to 400MHz as standard. By using the PLLs internal to the device during scan capture cycles this AC performance characterization can be further extended into Gigahertz ranges. The Personal Ocelot is complemented by a comprehensive suite of AC Scan tools which provide in depth analysis of the distribution of AC performance across individual design elements, highlighting path delay and transition delay faults.

Improve Engineering Productivity:

The Personal Ocelot leverages structural test to meet the requirements of debugging multiple device generations, preserving capital investment and scales with Moores Law. The Personal Ocelot is simple to use, has a short learning curve and allows customers to typically be productive within one day. These attributes result in significant improvement in test engineering productivity while lowering engineering costs.

Chapter 5

RESULTS

5.1 Eldo Simulator

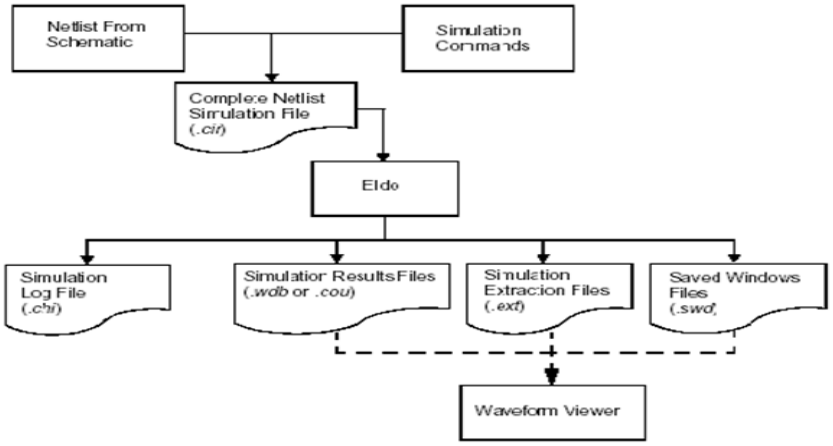

Figure 5.1: ELDO input output file

KEY ELDO FILES

⟨*file*⟩**.cir**

The main ELDO control file, containing circuit NETLIST, stimuli, models and simulation control commands. This is an input file normally called circuit file.

⟨*file*⟩**.chi**

ASCII output log file containing data, including results and error messages. This is an output file.

⟨*file*⟩**.cou**

Binary file containing ELDO analog simulation results data. This is an output file.

⟨*file*⟩**.wdb**

Viewed with the EZwave waveform viewer. The resulting output file is smaller than cou file. This is an output file.

5.2 Simulation Results

Sense amplifier:

PVT: min_N, max_P, 0.9V, -40 C

PROCESS: NMOS min, PMOS max

VOLTAGE: 0.9 V

TEMPERATURE: -40 C

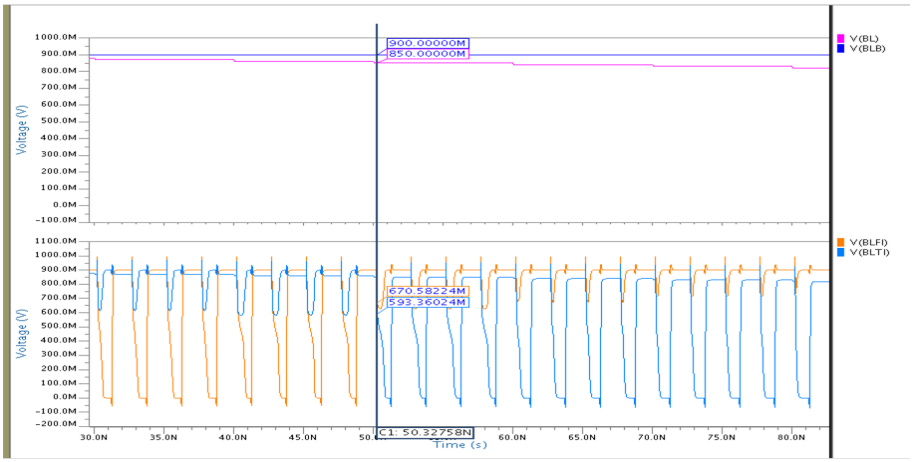

Figure 5.2: Sense amplifier waveform

Dual imbalanced sense amplifier:

PVT: min_N, max_P, 0.9V, -40 C

PROCESS: NMOS min, PMOS max

VOLTAGE: 0.9 V

TEMPERATURE: -40 C

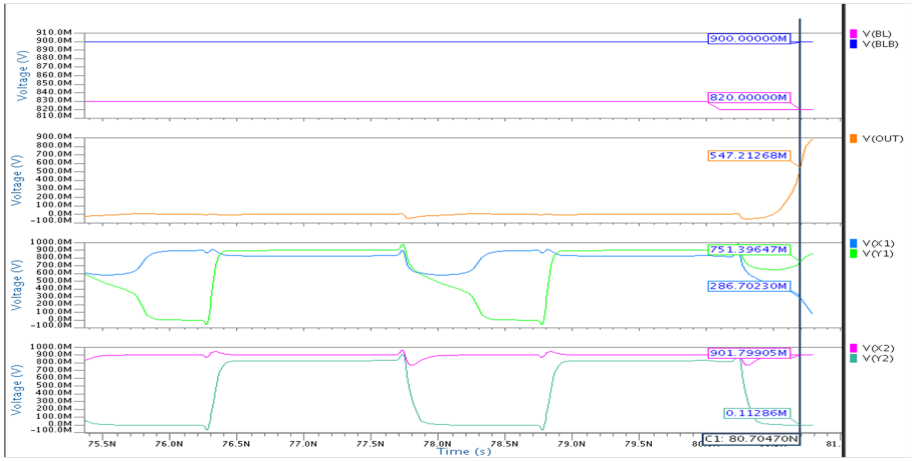

Figure 5.3: (a)

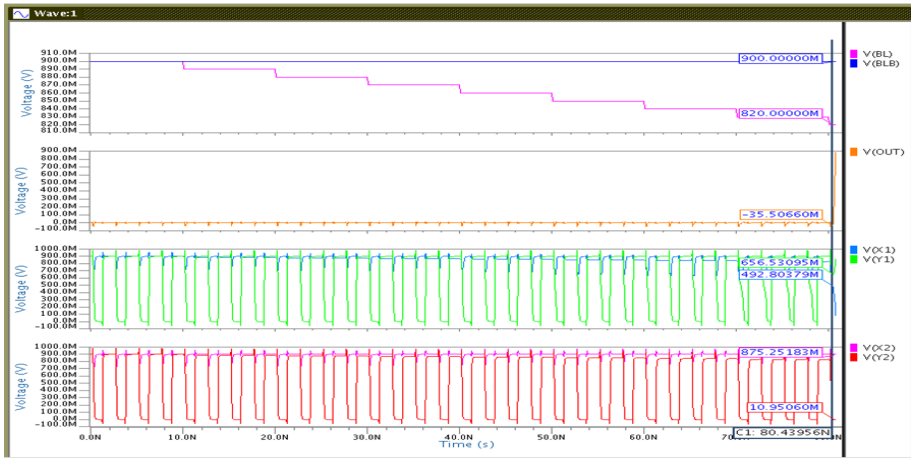

Figure 5.4: (a)and(b) showing waveform of dual imbalanced sense amplifier

Conclusion

In the company, the work I have done has greatly increased my knowledge in the field of design flow. I have learnt a lot about the working and the architecture of the memory and how the various operations are performed in a memory. In this project I have studied failure modes of SRAM and have done architecture level of arrangement of SRAM memory to take of dynamic recovery of memory failures. I have done architecture changes in the sense amplifier which is the part of read circuitry and other changes in the control block responsible for clock mixing and address predecoding etc. I got to work in different technology like 90nm, 40nm, 28nm technology. I have also done testing of a memory chip using OCELOT tester. The particular memory chip which I tested was in 90nm technology. I got exposure of different areas during my project which helped me a lot in increasing my knowledge.

Bibliography

[1] Simone Borri and Magali Hage-Hassan Analysis of Dynamic faults in embedded SRAM: Implication for memory test.

[2] IIi Shairah Abdul Halim et al, Comparative Study on CMOS SRAM Sense Amplifiers using 90nm Technology, 2013 International Conference on Technology, Informatics, Management, Engineering & Environment (TIME-E 2013) Bandung, Indonesia, June 23-26,2013

[3] Alexandre Ney et al, Analysis of Resistive-Open Defects in SRAM Sense Amplifiers, IEEE Transactions on very large scale integration(VLSI) systems, VOL. 17, NO. 10, October 2009

[4] ELDO tool user manual.

[5] SP10 LLC Compiler Usermanual @STMicroelectronics

[6] MARCEL J. M. PELGROM, Matching Properties of MOS Transistors, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 5, OCTOBER 1989

[7] Kiyoo Itoh, Adaptive Circuits for the 0.5-V Nanoscale CMOS Era, ISSCC 2009 SESSION 1 PLENARY 1.2